

Digital Circuits

Tutorial 8

1. Realise the following sets of function using a single decoder module and output logic:

$$f_1(A, B, C, D) = \sum m(2, 4, 10, 11, 12, 13)$$
$$f_2(A, B, C, D) = \prod M(0, 1, 2, 3, 6, 7, 8, 9, 12, 14, 15)$$
$$f_3(A, B, C, D) = B'C + ACD$$

2. Design a code converter whose input is a 4-bit code (C3, C2, C1, C0) representing hexadecimal code (0, 1, 2,8, 9, A, B, C, D, E and F) with the output driving a seven segment display digit to display the corresponding character. (The letters B and D are normally displayed in lower case to distinguish them from the numerals 8 and 0 respectively).
3. Find the output $f(a, b, c)$ for the circuit shown in Figure 1.

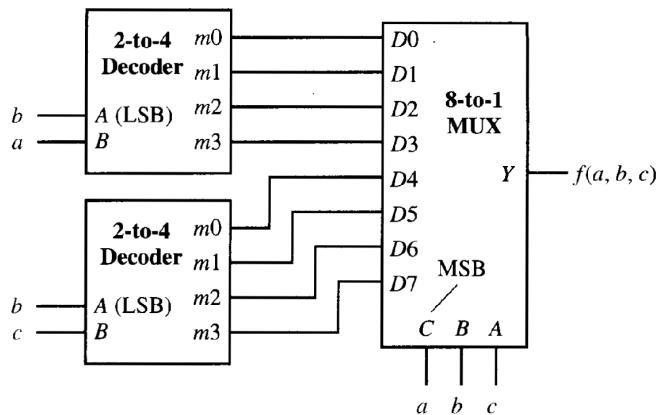
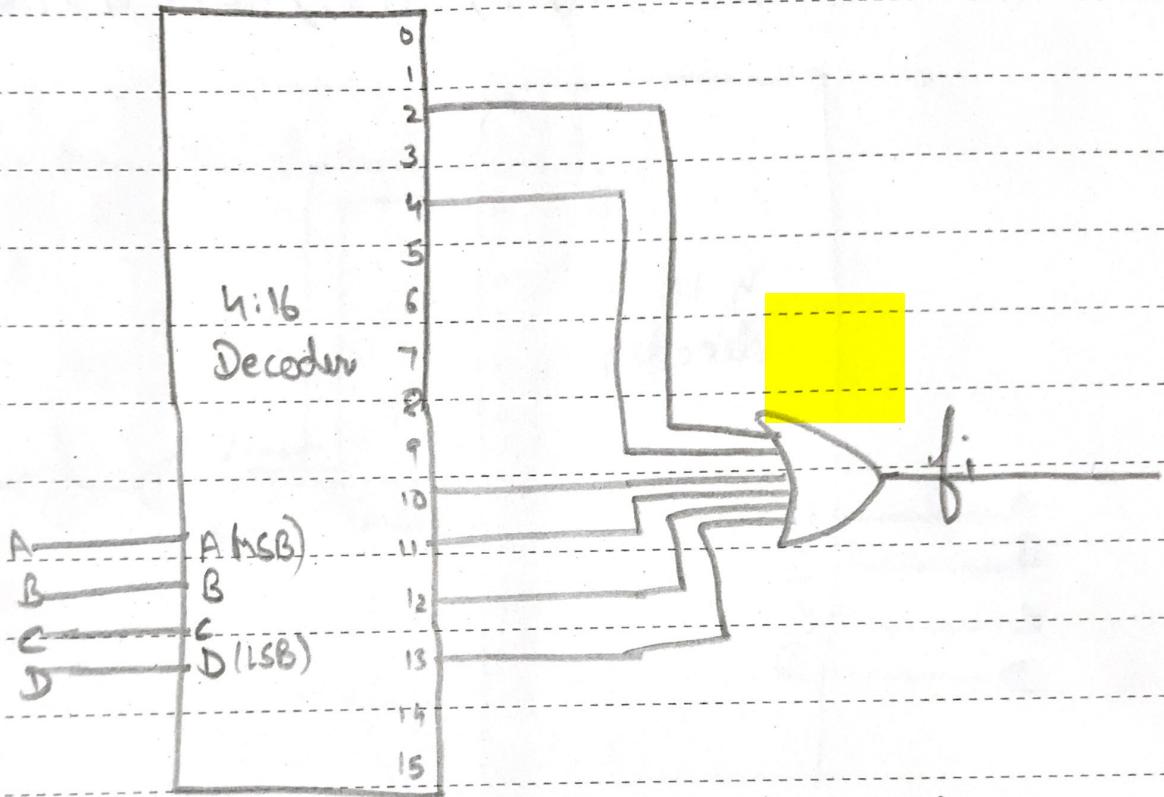


Figure 1

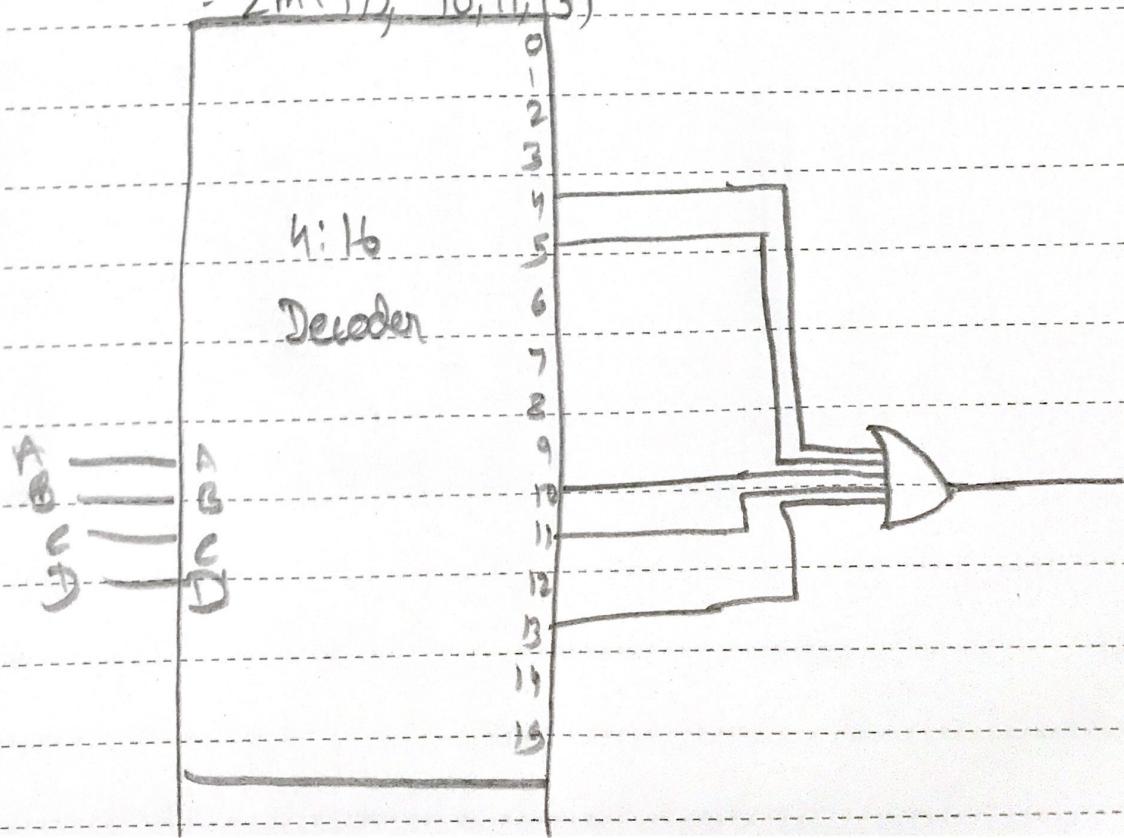
4. Design a 3-bit magnitude comparator with inputs $A = (a_2a_1a_0)_2$ and $B = (b_2b_1b_0)_2$ and three outputs: EQ($A=B$), GT($A>B$), and LT($A<B$).
5. Design a three input /3bit multiplexer. Use only NAND gates.

$$Q1 \text{ or } f_1(A, B, C, D) = \sum m(2, 4, 10, 11, 12, 13)$$

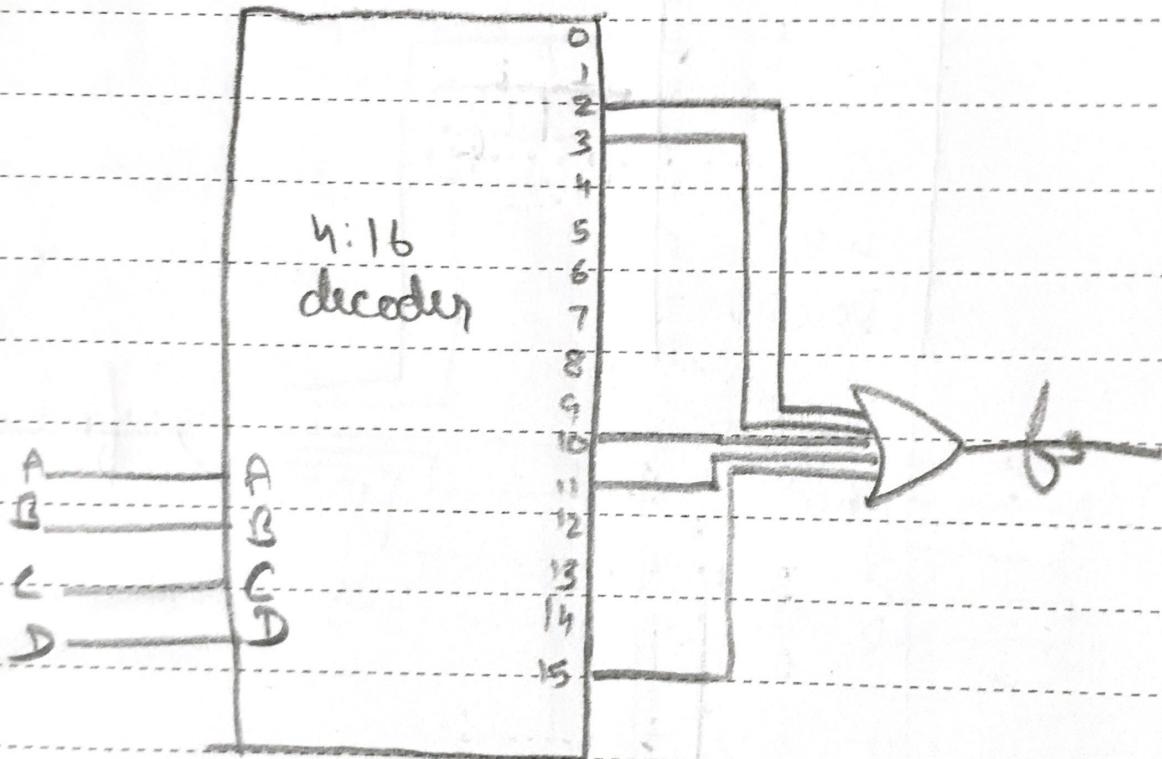


$$f_2(A, B, C, D) = \prod M(0, 1, 2, 3, 6, 7, 8, 9, 12, 14, 15)$$

$$= \sum m(4, 5, 10, 11, 13)$$



$$\begin{aligned}
 f_5(A, B, C, D) &= B'C + ACD \\
 &= AB'C + A'B'C + ABCD + AB'CD \\
 &= AB'CD' + ABC'D + A'BCD' + A'BCD + ABCD + AB'CD \\
 &= \sum m(10, 11, 2, 3, 15) = \sum m(2, 3, 10, 11, 15)
 \end{aligned}$$

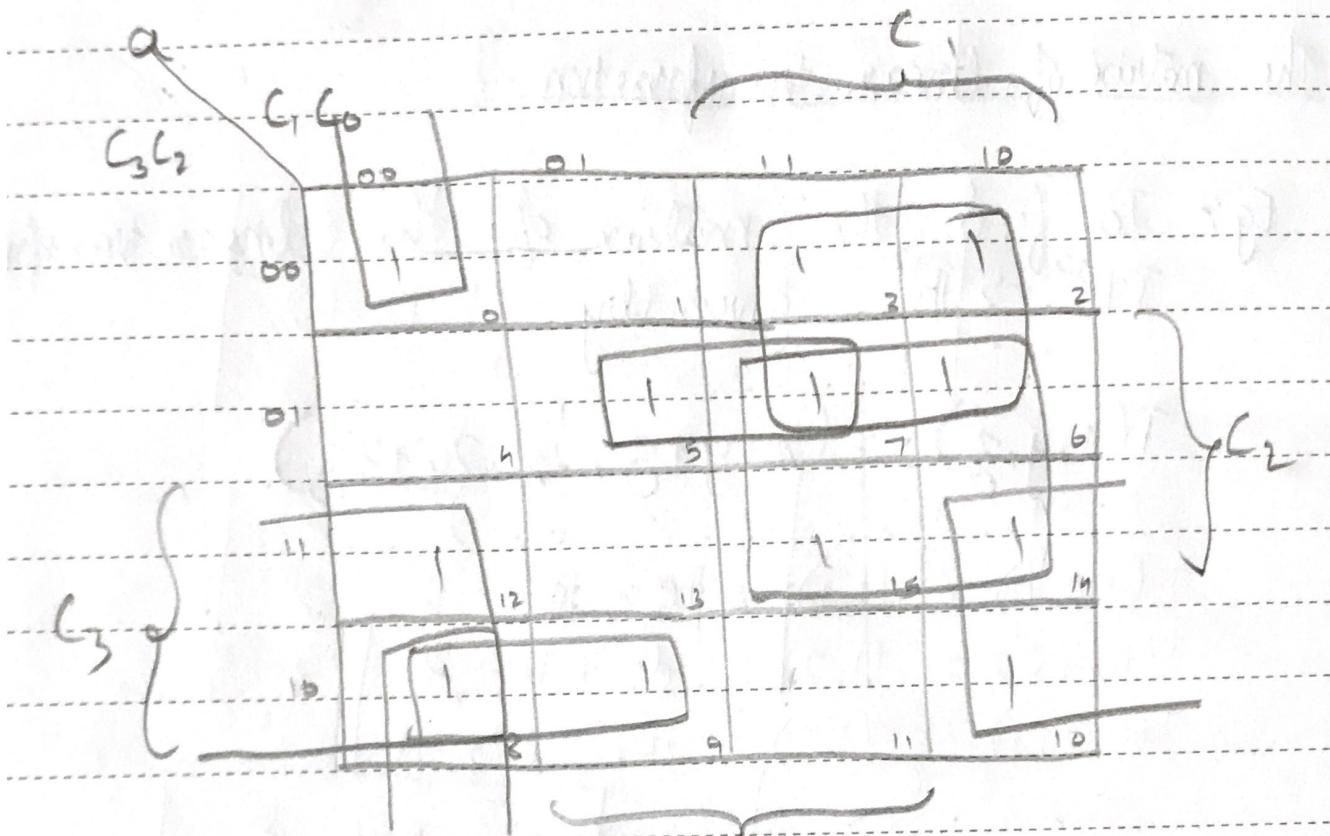


02

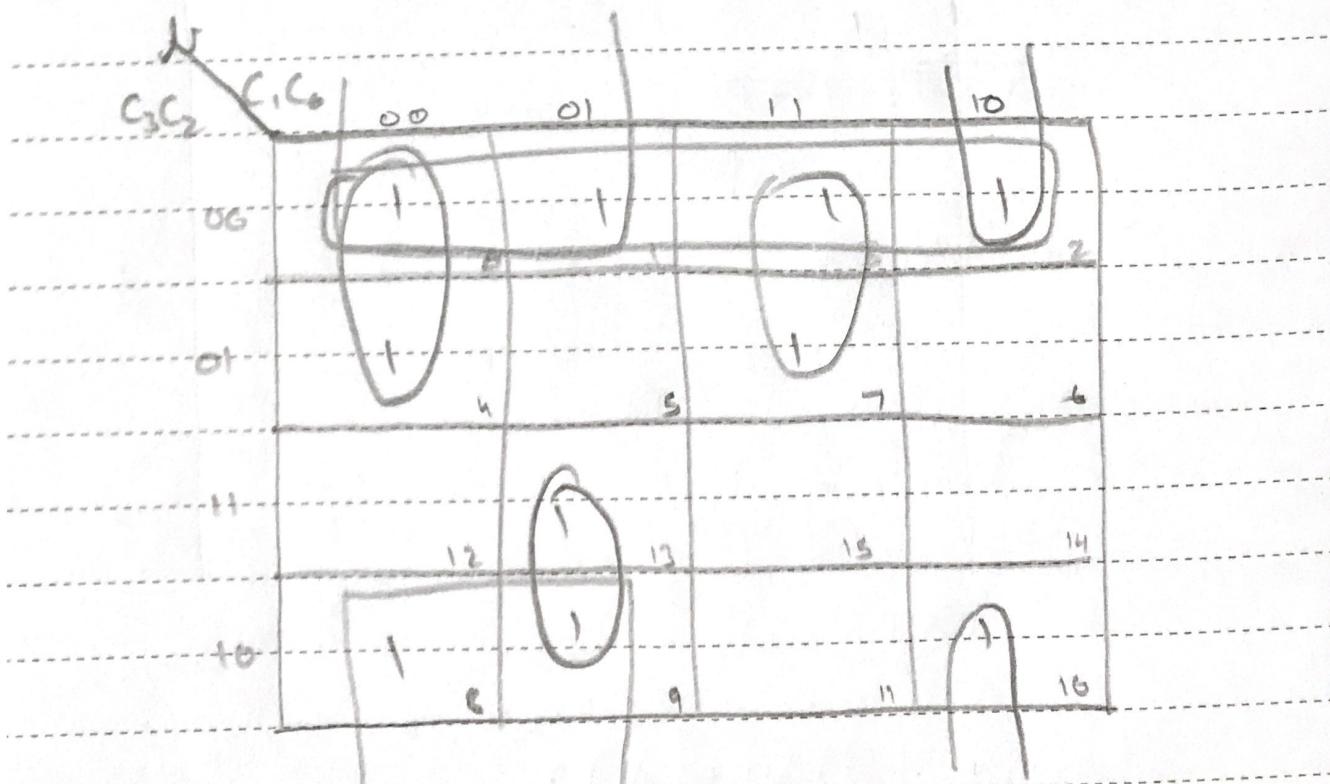


0123456789ABCDEF

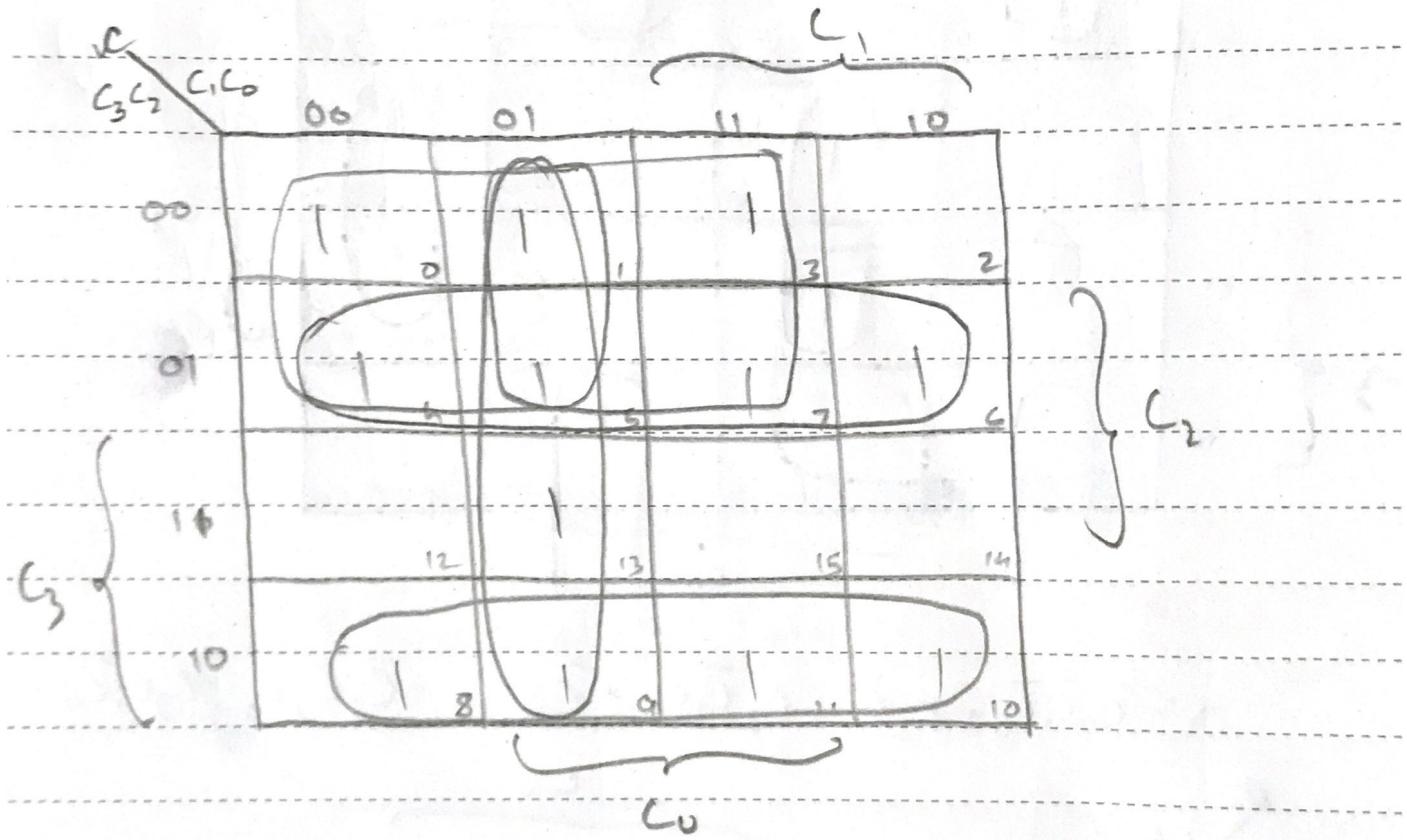
C_3	C_2	C_1	C_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	1	0	0
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1



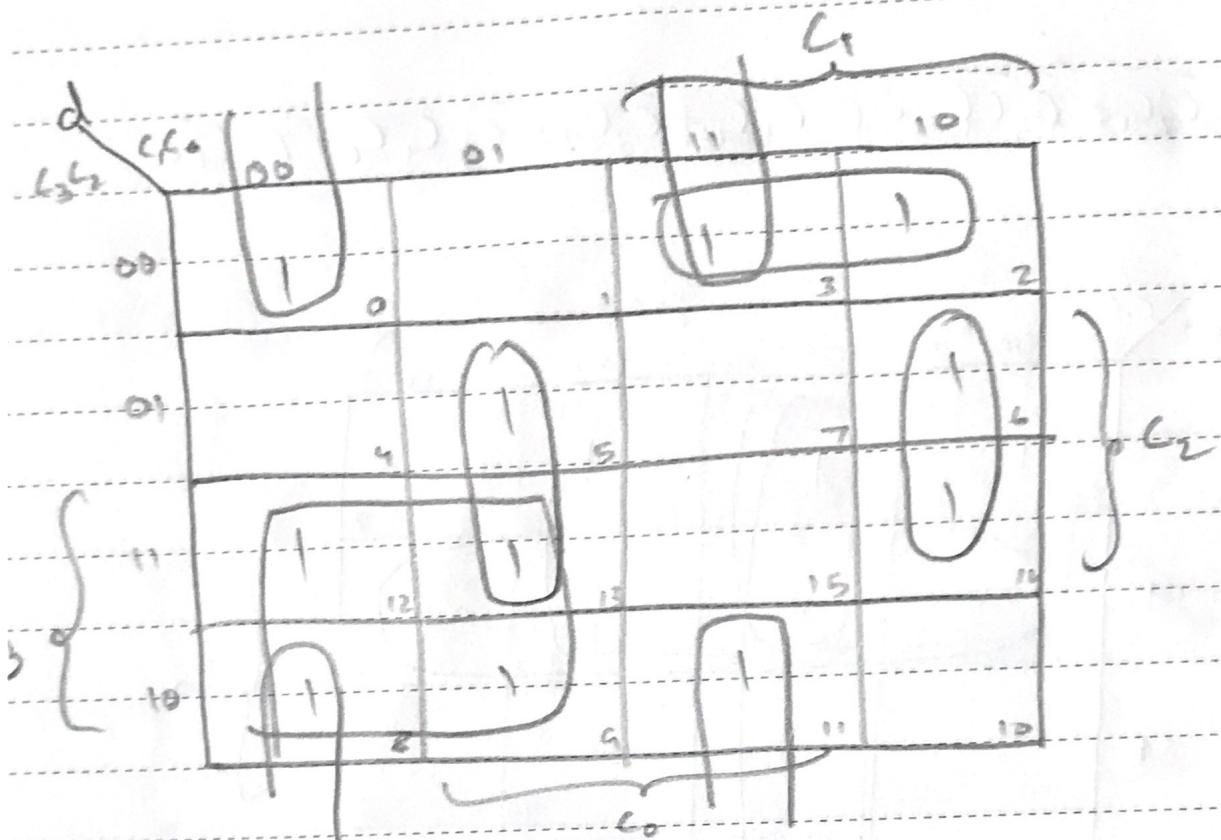
$$a = \bar{C}_3 C_1 + C_3 \bar{C}_0 + \bar{C}_2 \bar{C}_1 \bar{C}_0 + C_3 \bar{C}_2 \bar{C}_1 + \bar{C}_3 C_2 C_0 + C_2 C_1$$



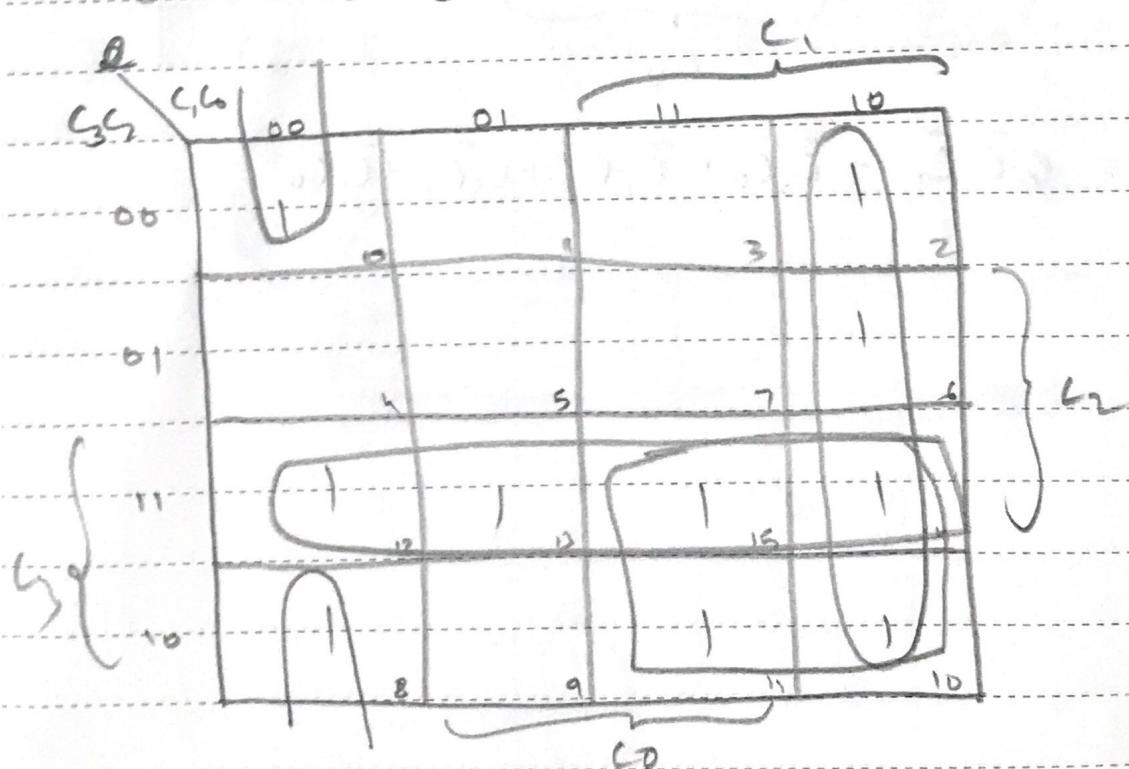
$$d = \bar{C}G + \bar{C}_3\bar{C}\bar{f}_0 + C_3\bar{C}_1C_0 + \bar{C}_3\bar{C}_2 + \bar{C}_3C_1C_0 + \bar{C}_2C_1\bar{C}_0$$



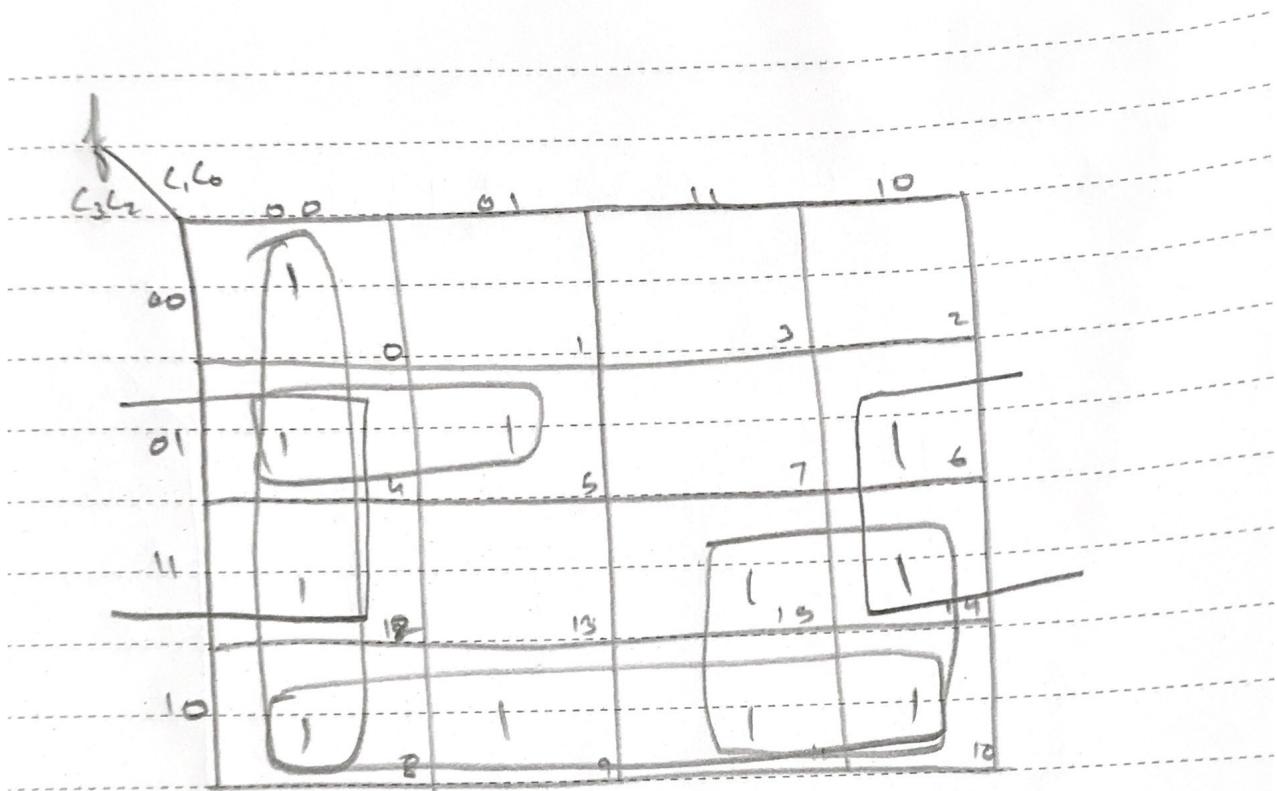
$$c = \bar{C}\bar{C}_3\bar{C}_1 + \bar{C}_3C_0 + \bar{C}_3\bar{C}_2 + C_3\bar{C}_1 + \bar{C}_1C_0$$



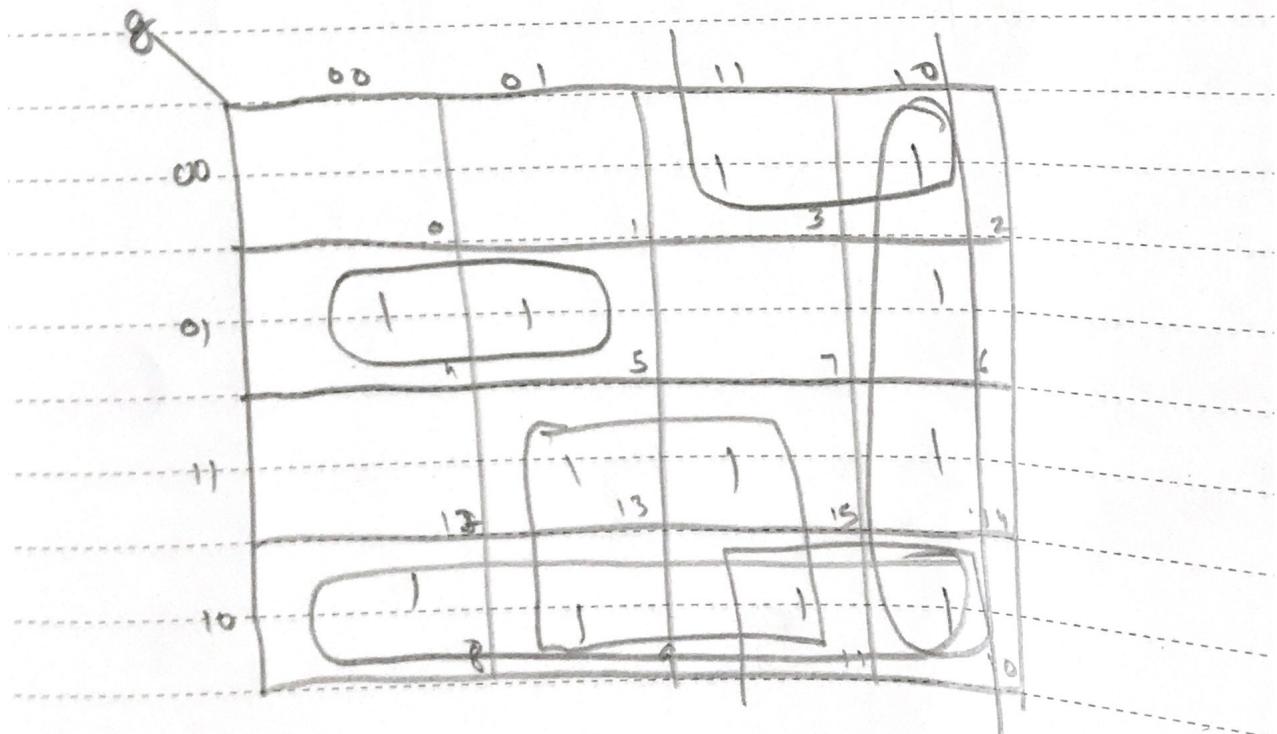
$$d = \bar{C}_2 \bar{C}_1 C_0 + C_3 \bar{C}_1 + C_2 \bar{C}_1 C_0 + \bar{C}_2 C_1 C_0 + \bar{C}_3 C_2 C_1 + C_2 C_1 \bar{C}_0$$



$$e = \bar{C}_2 C_1 C_0 + C_3 C_2 + C_3 C_1 + C_1 C_0$$

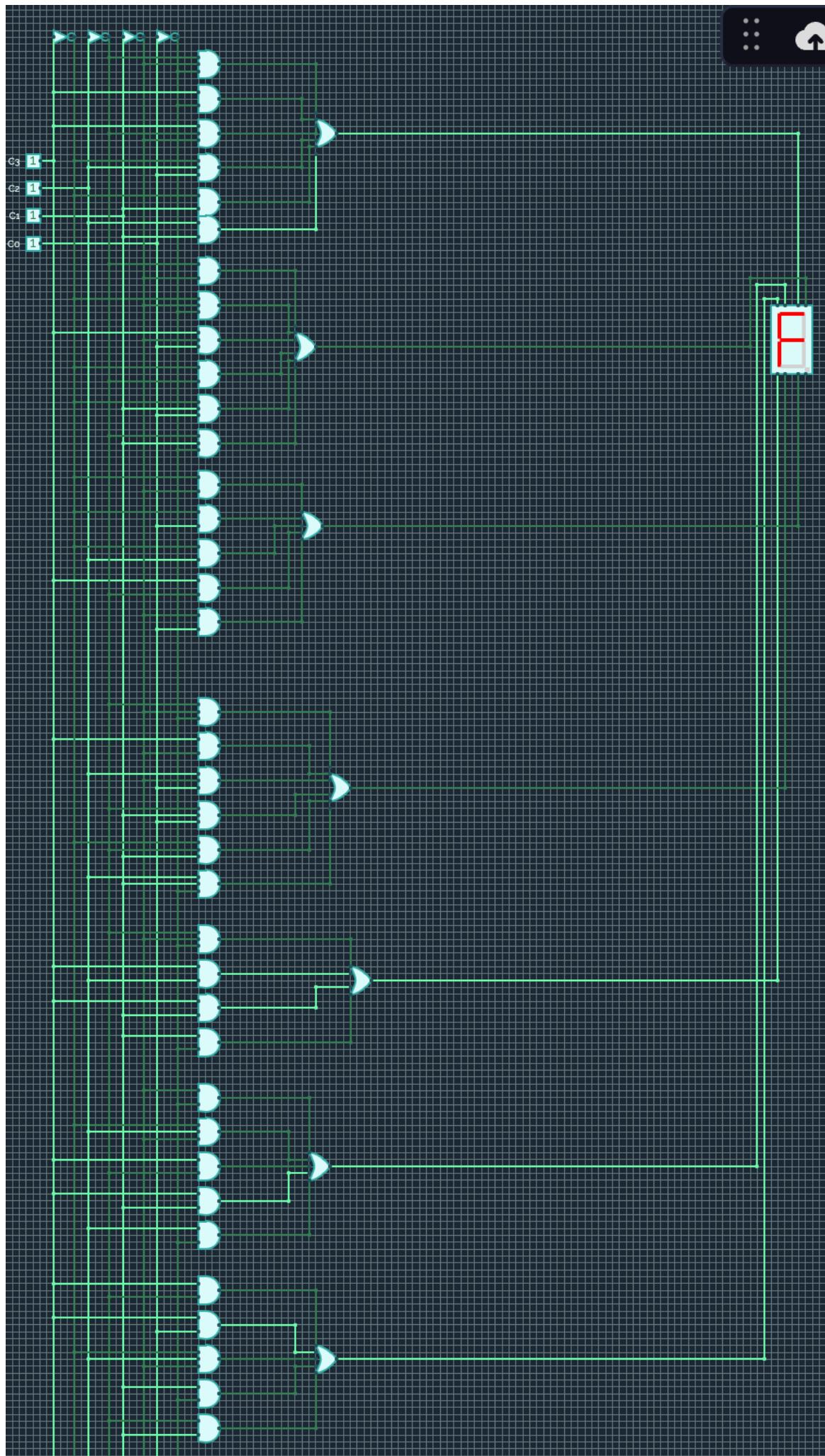


$$f = \overline{C_1} \overline{C_0} + \overline{C_3} C_2 \overline{C_1} + C_3 \overline{C_2} + C_3 C_1 + C_2 \overline{C_0}$$



$$g = C_3 C_2 + C_3 C_0 + \overline{C_3} C_2 \overline{C_1} + C_3 \overline{C_0} + \overline{C_3} C_1$$

Circuitverse link- <https://circuitverse.org/users/116502/projects/tut08>



a	b	c	k
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

$$\Rightarrow f = \sum m(0, 4, 5, 6, 7)$$

$$= \bar{a}\bar{b}\bar{c} + a\bar{b}\bar{c} + a\bar{b}c + a\bar{b}\bar{c} + abc$$

$$f = \bar{a}\bar{c} + a(b \oplus c) + abc$$

Q4

Let us take 1-bit mag. comparator

a ₀	b ₀	gt	lt	eq
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

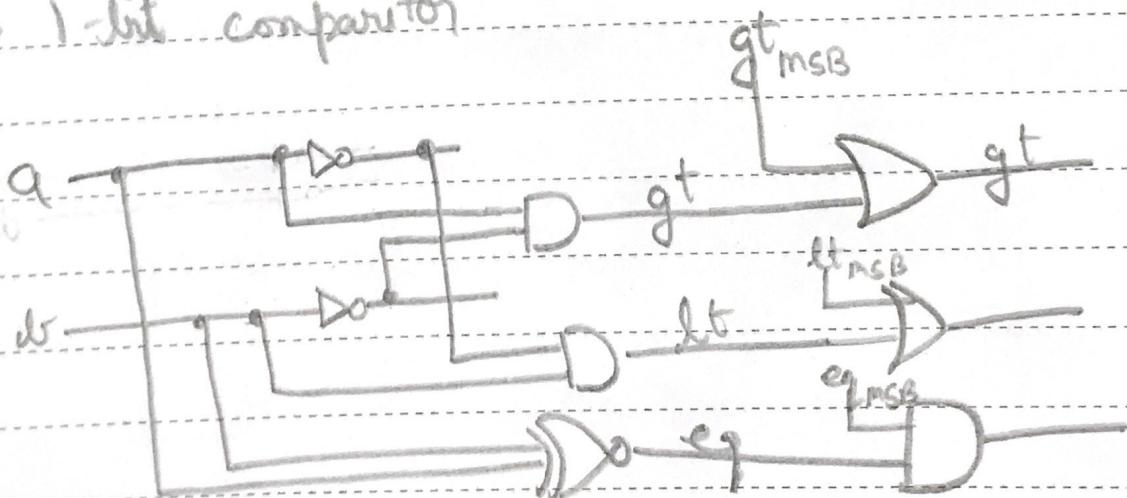
$$\Rightarrow gt = a_0 \bar{b}_0$$

$$lt = b_0 \bar{a}_0$$

$$eq = \bar{a}_0 \bar{b}_0 + a_0 \bar{b}_0 + a_0 b_0 = a_0 \oplus b_0$$

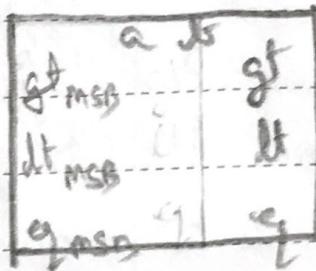
- ∴ If ~~the~~ more significant bit is gt or lt
then other bits doesn't matter
↳ For equal all the bits must be equal

→ 1-bit comparator

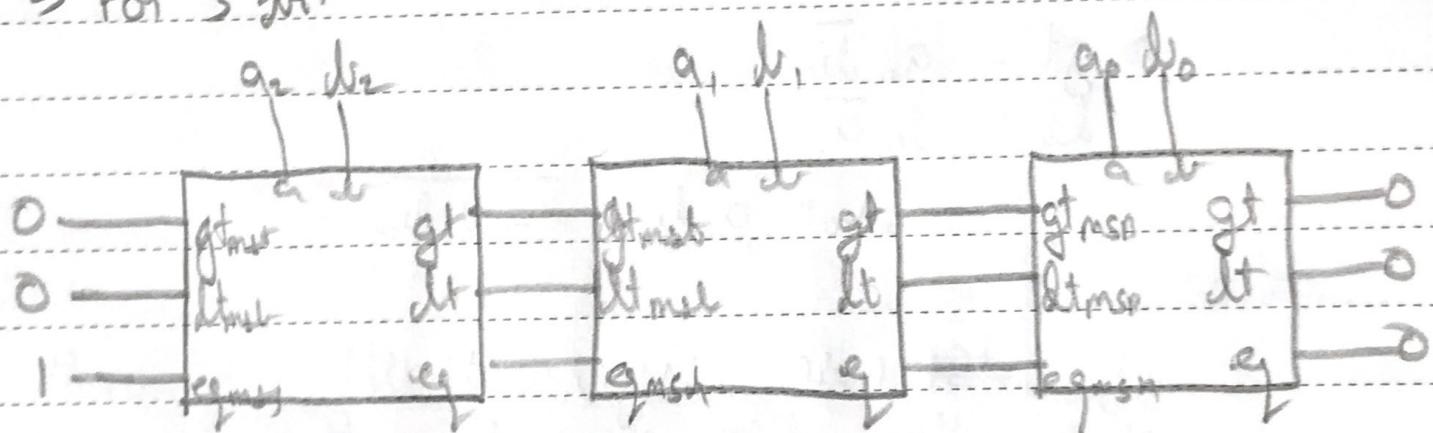


here, MSB means More significant bit

Let's consider how computers do subtraction
as



⇒ For 3-bit



Q5

a	b	f
0	0	I_0
0	1	I_1
1	0	I_2
1	1	Invalid

