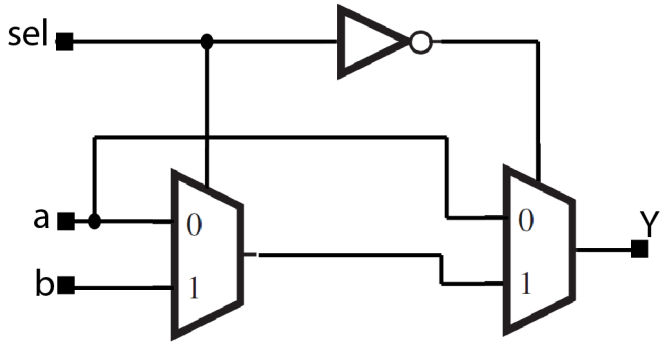
INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI

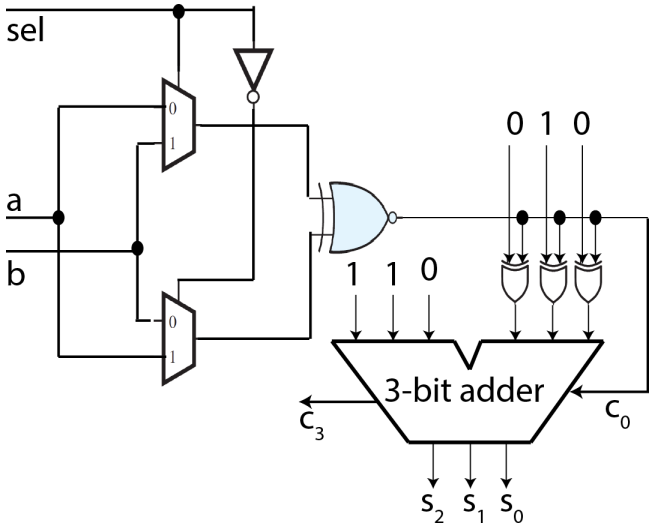
PRACTICE PROBLEM VIII

ECE 111 DIGITAL CIRCUITS

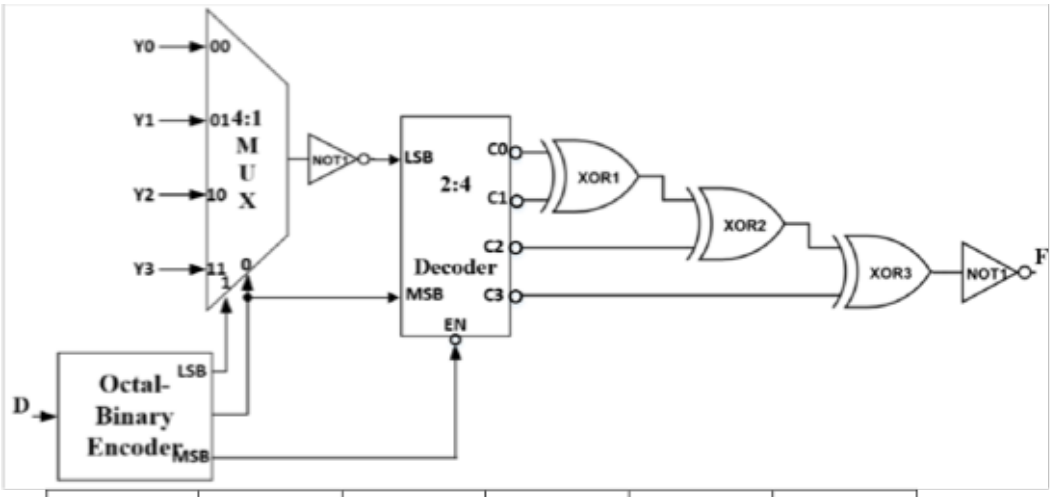
1. Write a simplified Boolean expression for the output Y(a,b,sel) described by the circuit diagram given below.



2. For the circuit shown below, the inputs are a, b and sel. The outputs are c_3, s_2, s_1 and s_0. The inputs to the 3-bit adder are {110} and {010}, as shown in the figure. Giving explanation to your answer, predict the value at the outputs c_3, s_2, s_1 and s_0.



3. Consider the combinational circuit shown below. The value of the inputs at different time instants are given below. Find the corresponding values of the output.



Time -->	1	2	3	4	5
Y0	0	1	1	0	1
Y1	1	1	1	1	0
Y2	0	1	1	0	1
Y3	0	1	0	0	0
D	3	5	7	2	1
F	**?**	**?**	**?**	**?**	**?**

4. Using 2:4 decoders, OR gates and one 4:1 multiplexers design a circuit with the following properties: It has two 2-bit binary number inputs (X=x_1x_0, Y=y_1y_0) and it has one 2-bit input (F=f_1f_0) to select the function of the circuit:

   - When F=0, the output is 1 if two inputs are equal
   - When F=1, the output is 1 if X > Y
   - When F=2, the output is 1 if X<= Y
   - When F=3, the output is 0.

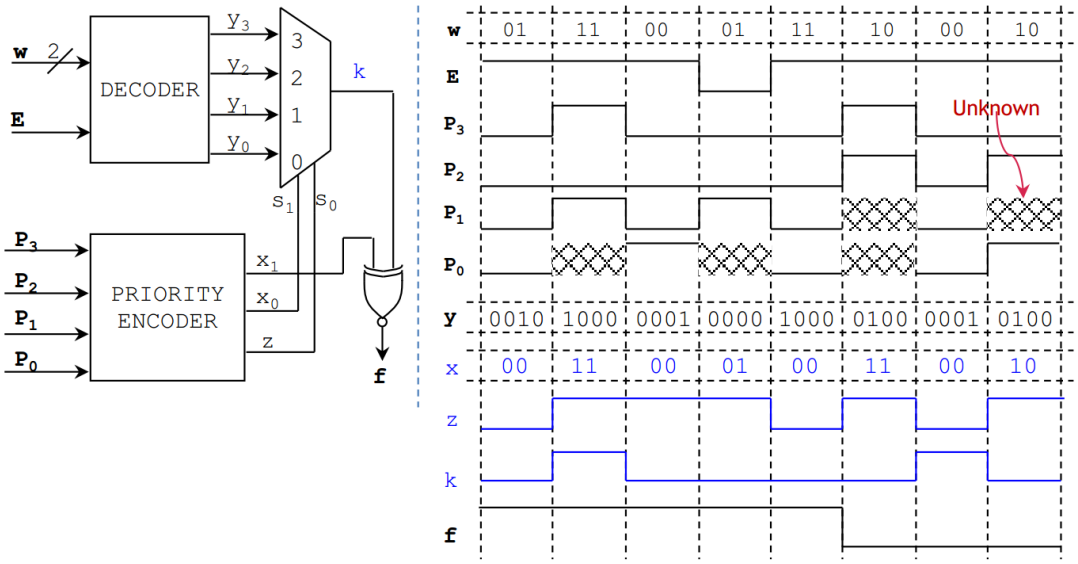
   Design the circuit using minimum number of 2:4 decoders with enables (i.e. if enable is 0, all the outputs are 0, otherwise the output is 1 for the minterm corresponding to the input), one 4:1 multiplexer and a minimum number of OR gates. Draw the final circuit assuming block diagrams for decoders and MUX.

5. A 3-bit offset binary representation is given by the equivalence: -4 = 000, -3 = 001, -2 = 010, -1 = 011, 0 = 100, +1 = 101, +2 = 110, +3 = 11. This scheme is used in Analog to Digital and Digital to Analog conversions

   (a) Design a circuit to convert a 3-bit offset-binary number into a 3-bit 2's complement representation, and vice-versa.

   b) Give an approach to design an adder that adds two 3-bit offset-binary numbers and gives the 4-bit result in the 3-bit offset-binary format.

6. Complete the timing diagram of the circuit shown below. The output z of the priority encoder is the valid bit indicator. The signal x and y is to be represented compactly as x_1x_0 and $y_3y_2y_1y_0$, respectively.



7. Derive the state diagram and characteristic equation of the latch circuit shown in Figure 1.

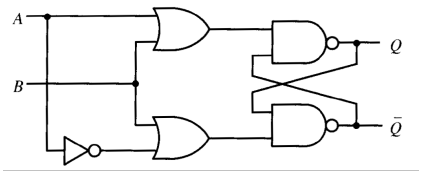


Figure 1

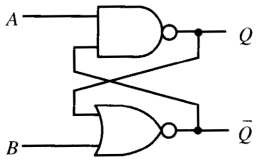


Figure 2

8. Find the excitation table of the latch circuit shown in Figure 2 and describe its behavior in words.

9. Given the JK FF of Figure 3a, complete the timing diagram shown in Figure 3b by determining the waveform of the output Q.

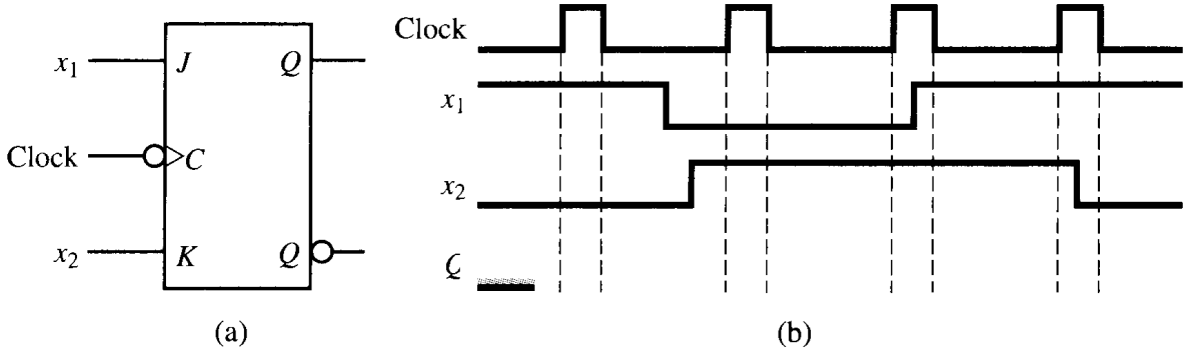


Figure 3

10. In our laboratory, some of J-K Flip Flops, bought from Chandni Chawk, had an internal defect. In all these ICs, for each of the J-K Flip Flop, the J and K terminals (pins) were internally shorted. Suggest a logic function to be used at

the J and K input of the J-K Flip Flops so that the defective ICs could be used as normal J-K Flip Flops in our experiments.

11. Given the SR FF of Figure 4a, complete the timing diagram shown in Figure 4b by determining the waveform of the output Q. Note that the FF is triggered on the positive edge of the clock signal. The condition S = R = 1 is produced twice by the inputs. Will this lead to unstable operation? Explain.

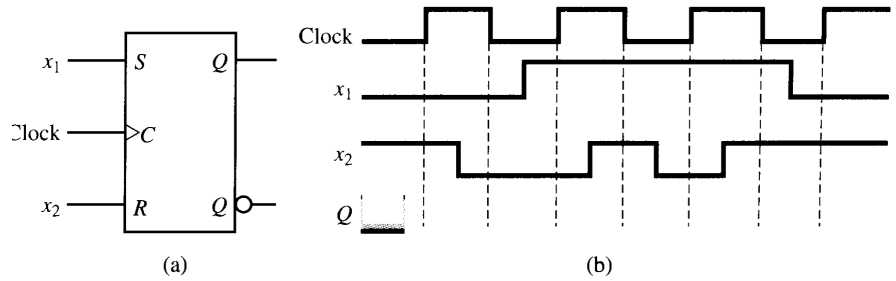


Figure 4

12. The waveforms of Figure 5 are applied to 7476 JK flip flop. Complete the timing diagram by drawing the waveform outputs Q and Q'.

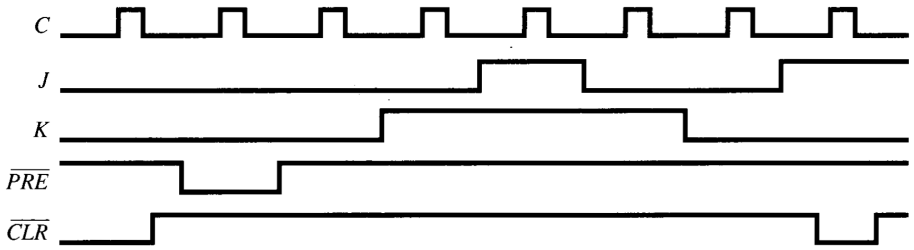


Figure 5

13. The circuit of Figure 6a contains D latch, a positive edge triggered D flip flop and a negative edge triggered D flip flop. Complete the timing diagram of Figure 6b by drawing waveforms of signal y1, y2 and y3.

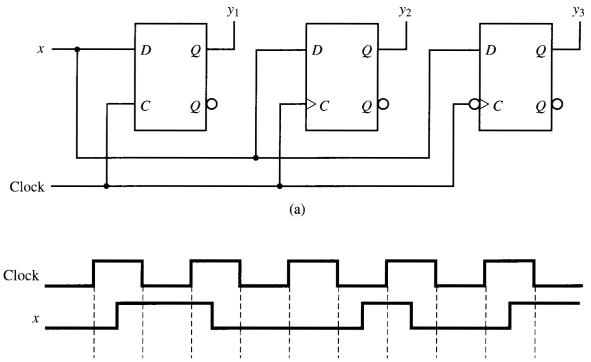


Figure 6