Digital Circuits

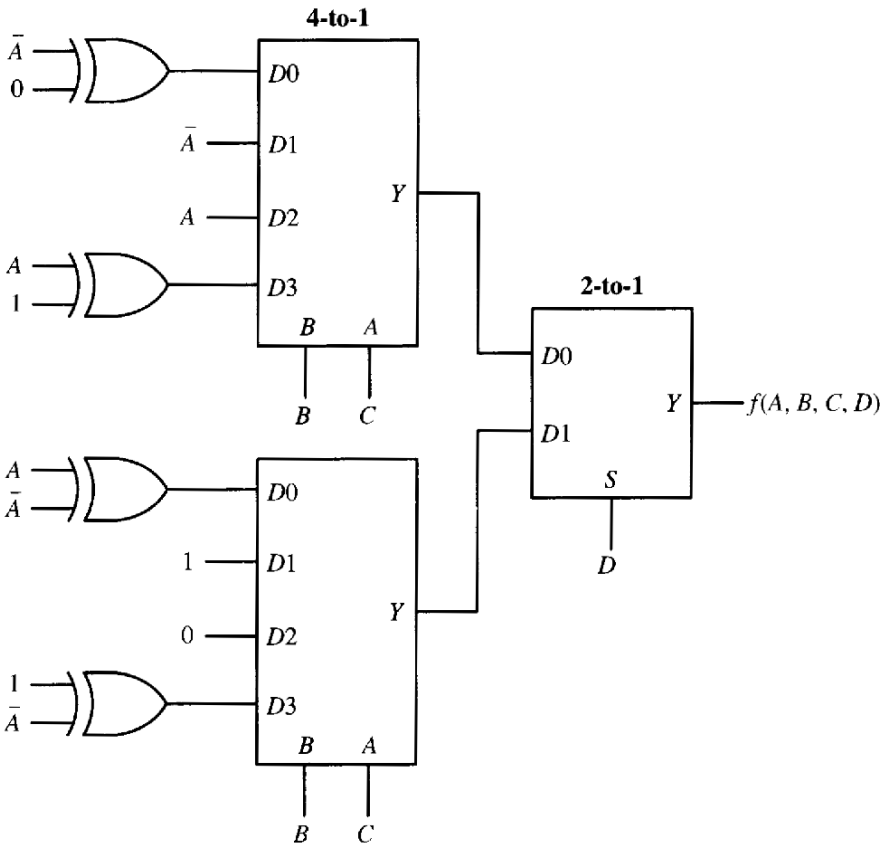
Practice Problems VI

1. Design a 4 to 16 decoder using logic gates. The encoded inputs are (A, B, C, D) and the outputs are active low: (O_0, O_1, …..,O_{15}). The decoder should have one active high enable line, E.
2. Realise the following sets of function using a single decoder module and output logic:

   a. $f_1(A, B, C, D) = \sum m(2, 4, 10, 11, 12, 13)$
   $f_2(A, B, C, D) = \prod M(0, 1, 2, 3, 6, 7, 8, 9, 12, 14, 15)$
   $f_3(A, B, C, D) = B'C + ACD$

   b. $f_1(A, B, C, D) = \sum m(0, 1, 7, 13)$
   $f_2(A, B, C, D) = ABC' + ACD$
   $f_3(A, B, C, D) = \prod M(0, 1, 2, 5, 6, 7, 8, 9, 11, 12, 15)$

3. Find the minterms of the function f(A, B, C, D) realized by the circuit shown in Figure 1.



Fiigure 1

4. Given the function f (Q, R, S, T) = $\sum$ m(4, 5, 6, 7, 8, 13, 14, 15). Using the circuits given in Figure 3, implement the function by appropriately connecting Q, R, S, T to the NAND gates and to 4 to 1 multiplexer and by connecting the NAND gate output to appropriate input(s) of the multiplexer. The only available inputs are Q, R, S, T; no 0 or 1 nor Q' R' S; T' is available as an input. (Nine connections are required: three for NANA circuit and six for MUX.) Consider B to be MSB for multiplexer.

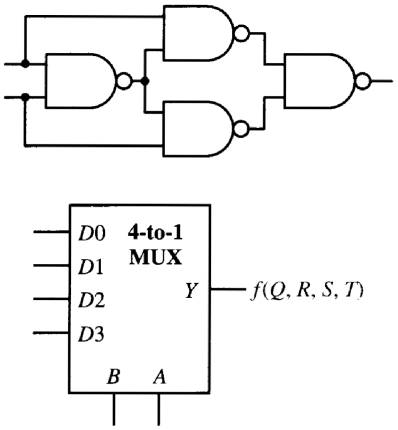


Figure 3

5. Using only half-adders, draw a circuit that will add 3 bits, x_i, y_i, z_i, together, producing carry and sum bits c_i, s_i as shown in following truth table.

x_i	y_i	z_i	c_i	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

6. Design a 3 bit full adder using carry look ahead, rather than ripple carry.
7. Design a 1 bit full subtracter module, using only NOR gates, and then construct a 4 bit subtracter using only these module.
8. Describe the overflow condition as applied to two's complement addition and subtracter.
9. Design a BCD adder that adds two BCD digits and produces a BCD result and a carry output.
10. Design a logic circuit that multiplies two bit numbers, $(a1a0)_2$ and $(b1b0)_2$ using only NAND gates, the product should be a 4 bit numbers $(p3p2p1p0)_2$.
11. It is necessary to compare three 4 bit numbers X = $(x3x2x1x0)_2$ $(y3y2y1y0)_2$, and Z = $(z3z2z1z0)_2$. Draw a circuit that will implement the following truth table, you can use 7485 magnitude comparators and associated logic to implement this function. Use Google to download circuit and truth table of 7485.

Condition	f_0	f_1	f_2	f_3	f_4	f_5	f_6	f_7
$X > Y > Z$	1	0	0	0	0	0	0	0
$X > Z > Y$	0	1	0	0	0	0	0	0
$Y > X > Z$	0	0	1	0	0	0	0	0
$Y > Z > X$	0	0	0	1	0	0	0	0
$Z > X > Y$	0	0	0	0	1	0	0	0
$Z > Y > X$	0	0	0	0	0	1	0	0
$X = Y = Z$	0	0	0	0	0	0	1	0
Any other case	0	0	0	0	0	0	0	1