

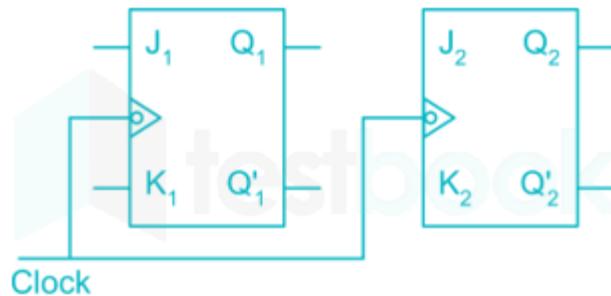
## TUTORIAL 9

Q1. Three 4 bit shift registers are connected in cascade as shown in figure below. Each register is applied with

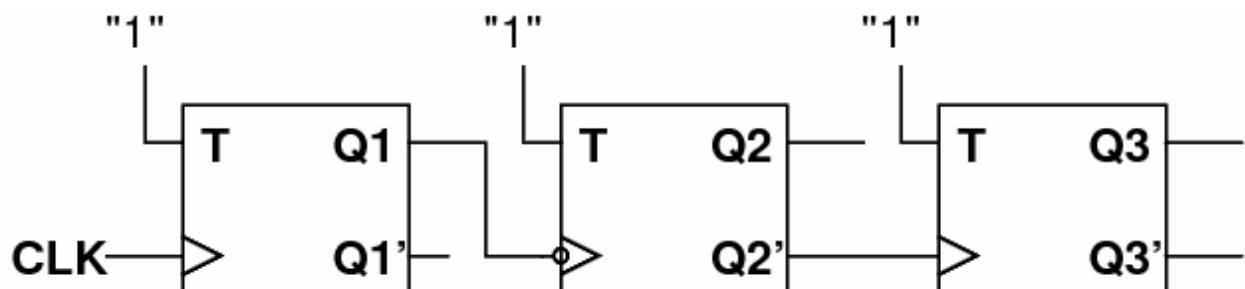


A 4 bit data 1011 is applied to the shift register 1. Find the minimum number of clock pulses required to get the same output data as the input data with the same clock pulses.

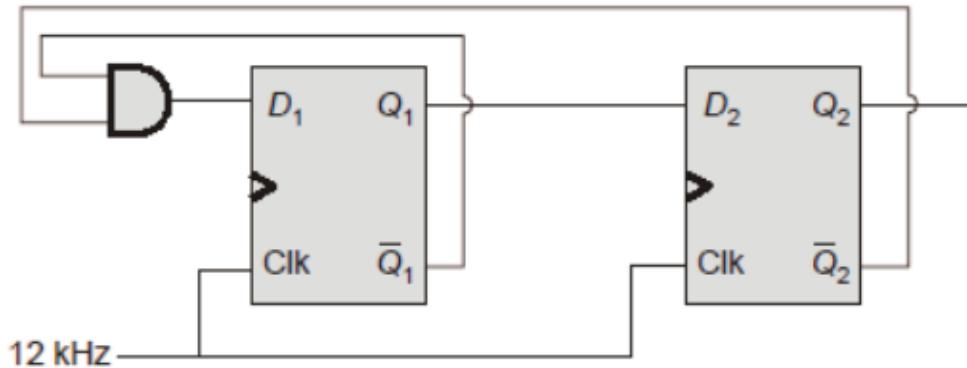
Q2. A synchronous counter using two J-K flip flops that goes through the sequence of states:  $Q_1Q_2 = 00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00$  is required. To achieve this, find the inputs of the flip flops?



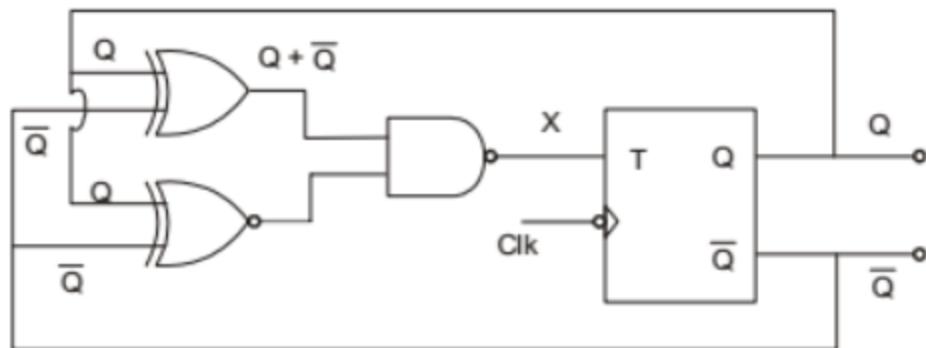
Q3. Draw output waveforms ( $Q_1$ ,  $Q_2$ ,  $Q_3$ ) of the given T FFs along with the CLK signal for 5 Clock cycles. Consider the initial states of  $Q_1=Q_2=Q_3=0$ .



Q4. In the circuit shown the frequency of the clock signal is 12 KHz. The frequency of the signal at Q<sub>2</sub> will be ?



Q5 The clock frequency for the following circuit is 2kHz. If the initial state of the output Q of FF is '0', then the frequency of the output Q in kHz.



Q6. Design serial n-bit adder using 1-bit adder and shift registers.

Q7. Design a counter, which counts the sequence 4-5-6-7-8-9-4.... Using active low clear and active low preset.

Q8. Assume that you have an oscillator which provides clock signal with frequency 8 Hz. Design modulo-6 counter which increments its output count every second. Design a modulo 7 ripple counter.

Q1 4-clock cycle is needed to input 4-bit serial input by shift reg 1.

Also, 4 addition cycle will be needed to output it by shift reg 1, and get as an input by shift reg 2.

0 clock cycle is needed ~~in the~~ to transfer 4-bit parallel data from shift reg 2 to 3.

4 clock cycles are needed to output 4-bit serial output by shift reg 3.

$$\Rightarrow \text{clock cycles} = 4 + 4 + 0 + 4 = 12$$

	S1SO	S1PO	P1SO
Initial	0000	0000	0000
1.	1000	0000	0000
2.	1100	0000	0000
3.	0110	0000	0000
4.	1011	0000	0000
5.		1000	0000
6.		1100	0000
7.		0110	0000
8.		1011	0000
9.			1011
10.			x 101
11.			x x 10
12.			x x x 1
			x x x x

$Q_2$	$J_1$	$K_1$	$J_2$	$K_2$	$Q_1$	$Q_0$		
0	1	0	1		0	0		
1	1	0	0		1	0		
1	1	1	1		0	1		
1	1	0	0		1	1		
1	1	1	1		0	0		

Q3

Qk

Q1

Q2

Q3

$$Q^4 \quad D_1 = \overline{Q}_1 Q_2$$

$$D_2 = Q_1$$

~~$Q_2 D_2 = 0$~~ , ~~(By characteristic eq' of J-FF)~~

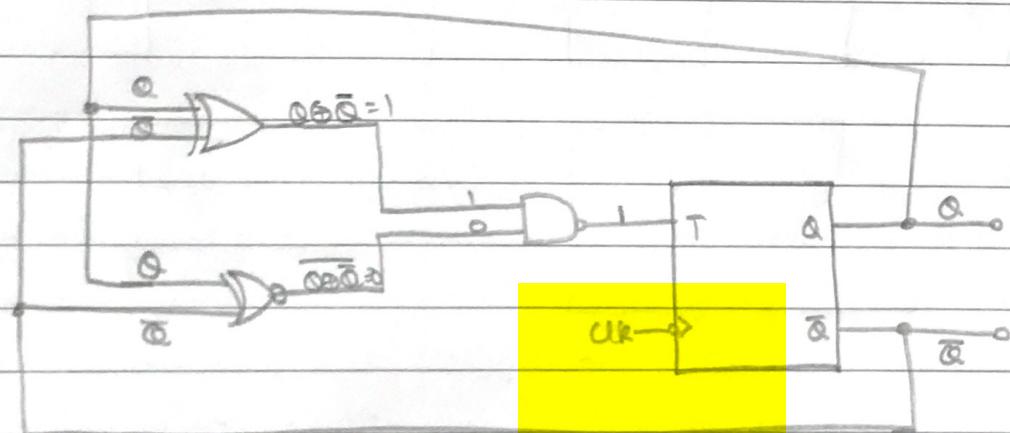
clk	$Q_{1n}$	$Q_{1n}$	$Q_{2n}$	$Q_{2n}$	$D_1$	$D_2$
0	0	1	0	0	1	0
1	1	0	0	1	0	1
2	0	0	1	0	0	0
3	0	1	0	0	1	0

$\Rightarrow$  There are 3 states only

$$\Rightarrow \text{freq} = \frac{\text{clk}}{3} = \frac{12}{3} = 4 \text{ kHz}$$

$$\Rightarrow Q_2 \text{ freq} = 4 \text{ kHz}$$

Q5



clk

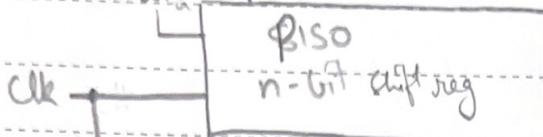
Q

$$\Rightarrow \text{freq of } Q = \text{freq of clk} / 2$$
$$= 1 \text{ kHz}$$

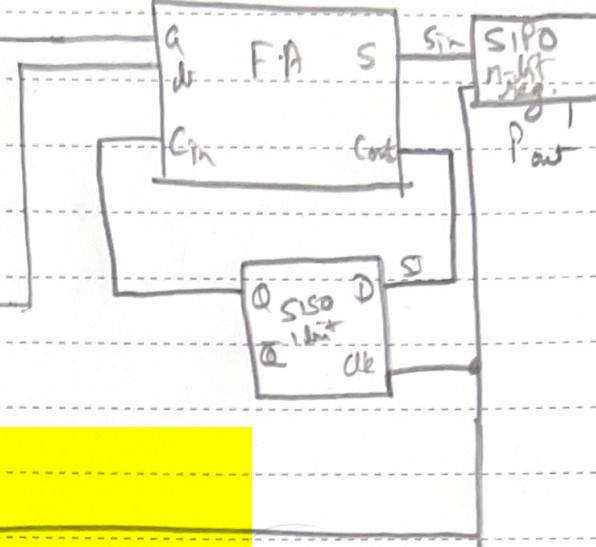
Q6

A

n-bit P-input



SD\_out

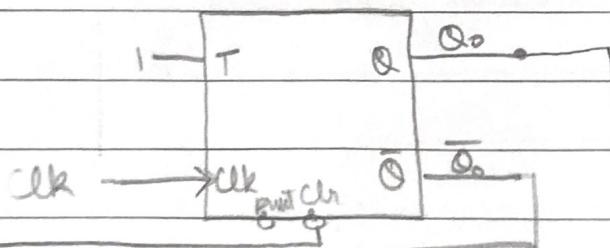


The adder bit are received one by one from  
The two bits of A, B are received one by one from  
the PISO shift reg, which is lead into the adder, with a

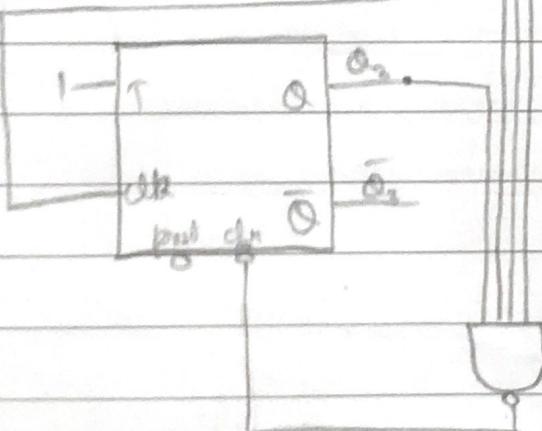
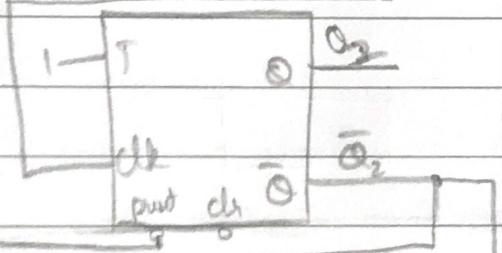
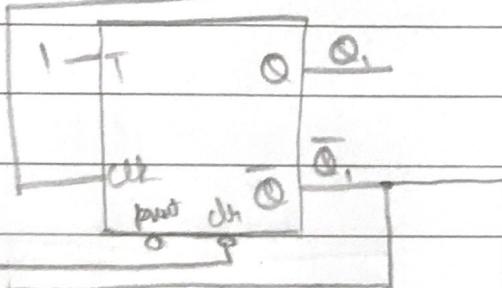
The sum obtained from the Full adder is passed to a  
n-bit SIPO adder shift reg & P\_out is the result.

The carry out bit is sent to a 1-bit SISO shift  
reg. to delay the carry out by 1-bit and send  
it to carry in.

Q7

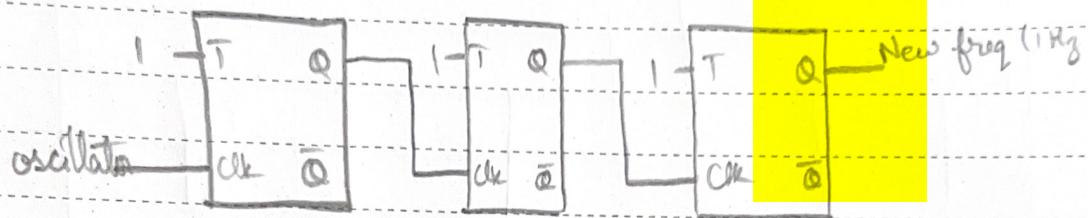


$$\Rightarrow \text{4-bit counter} = Q_3 Q_2 Q_1 Q_0$$

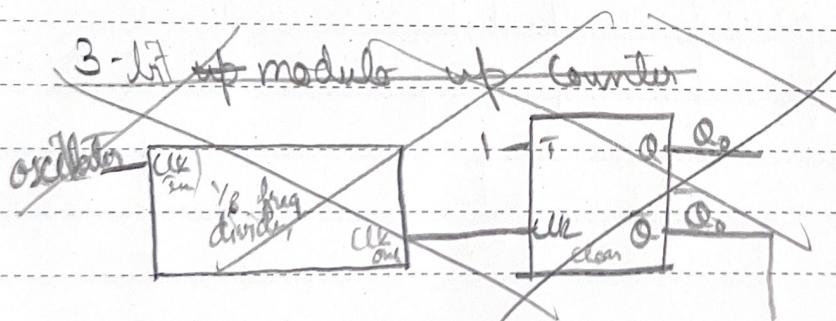
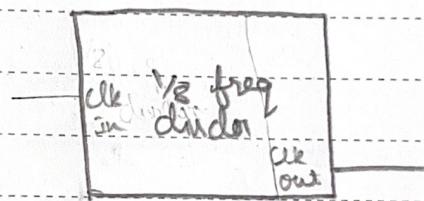


Q8

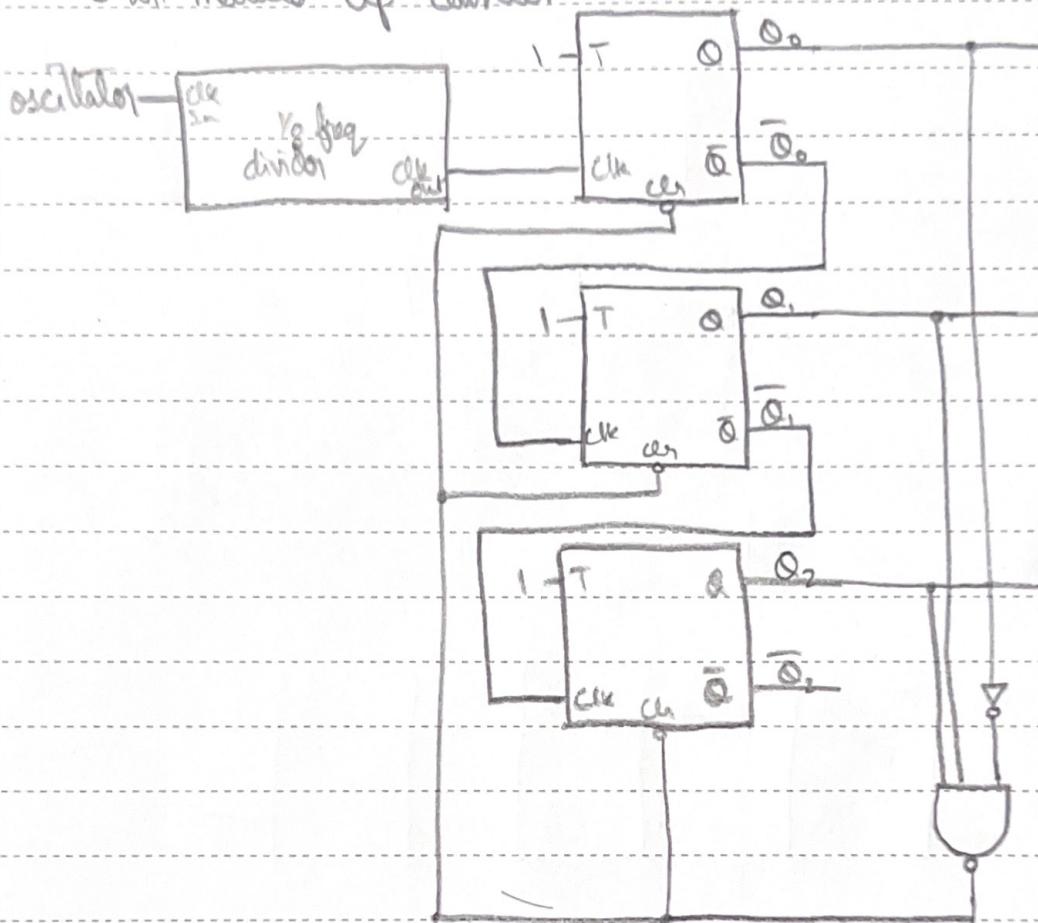
To reduce a 8Hz clock signal to 1Hz we  
use a freq. divider consisting of  $\log_2 8 = 3$   
T-flip flops.



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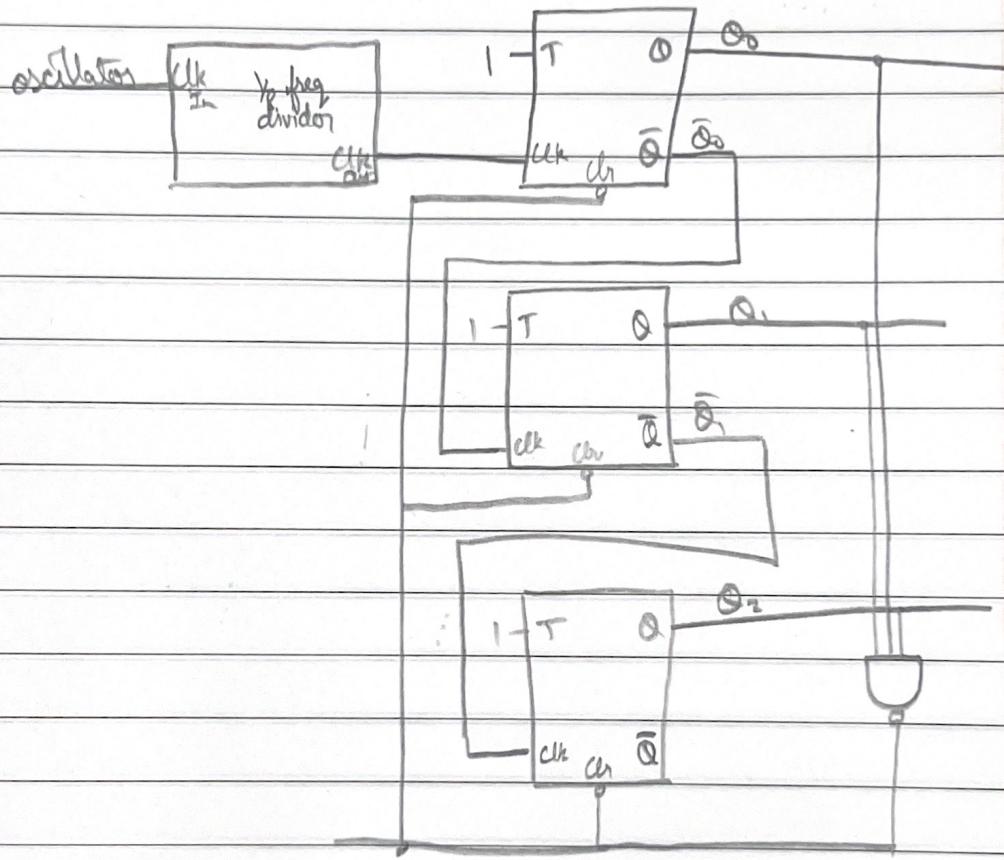


3-bit modulo up counter



$(Q_2 Q_1 Q_0)_2$  is the required counter

3-bit modulo 7 ripple counter



$(Q_2, Q_1, Q_0)$  is the required counter