



INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Department
of
Electronics & Communication Engineering

ECE111|Digital Circuits
Section: B

Dr S.S. Jamuar

Lab_7:

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14 Mar 2022

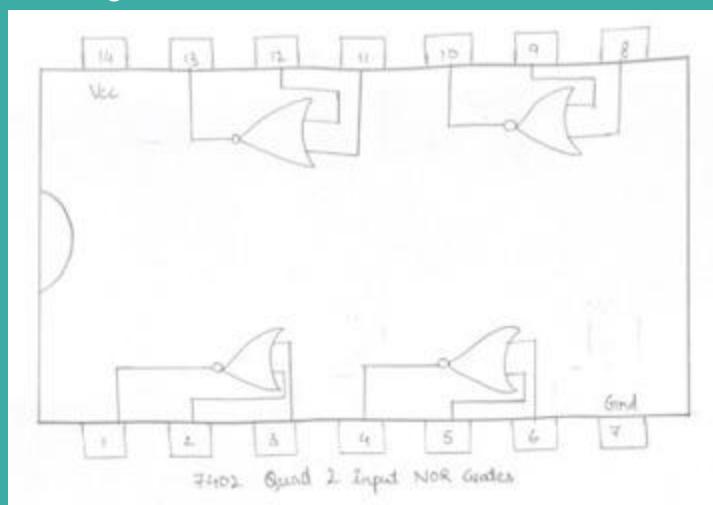
Aim: To create a SR Latch in TinkerCAD using NOR gates

Components/ICs Used: Breadboard, wires, LEDs, resistors, slide switches, power supply, NOR gate

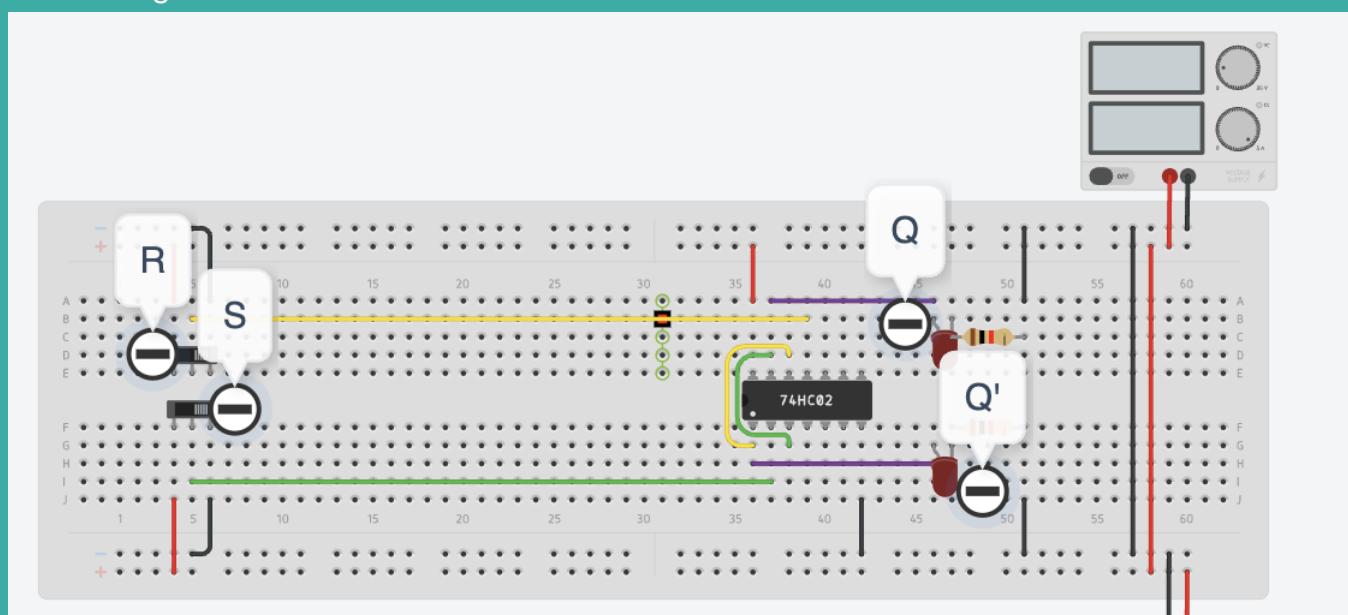
Link of TINKERCAD Workspace:

<https://www.tinkercad.com/things/jCRaNbOJfGo-srlatch/editel?sharecode=fqoAD2abph7GCSsDSv4GKAzvBGp7vFVdItIra-R3yqeY>

Pin Diagram of the IC:



Circuit Diagram:



Characteristics equation:

$$Q_n = S + R'Q_{n-1}$$

Characteristic Table and Excitation Table:

| S | R | Q | \bar{Q} | |
|---|---|---|-----------|-----------|
| 0 | 1 | 0 | 1 | |
| 0 | 0 | 0 | 1 | |
| 1 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | |
| 1 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | |
| 1 | 1 | 0 | 0 | (Invalid) |
| 0 | 0 | 0 | 1 | |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | 0 | (Invalid) |
| 0 | 0 | 1 | 0 | |

| S | R | Q _n | \bar{Q}_n | |
|---|---|------------------|-----------------|--|
| 0 | 0 | Q _{n-1} | \bar{Q}_{n-1} | |
| 0 | 1 | 0 | 1 | |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | Invalid | | |

Observations/Results: Created a SR Latch using NOR gate and checked its implementation

Application: SR Latch is used to store a bit of data

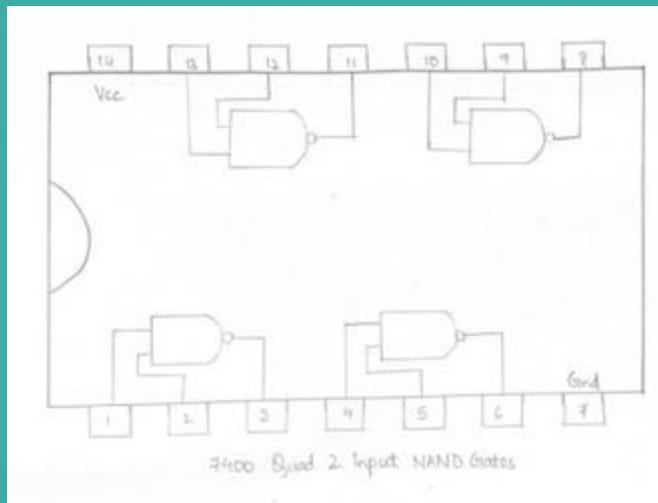
Aim: To create a SR Latch in TinkerCAD using NAND gates

Components/ICs Used: Breadboard, wires, LEDs, resistors, slide switches, power supply, NAND gate

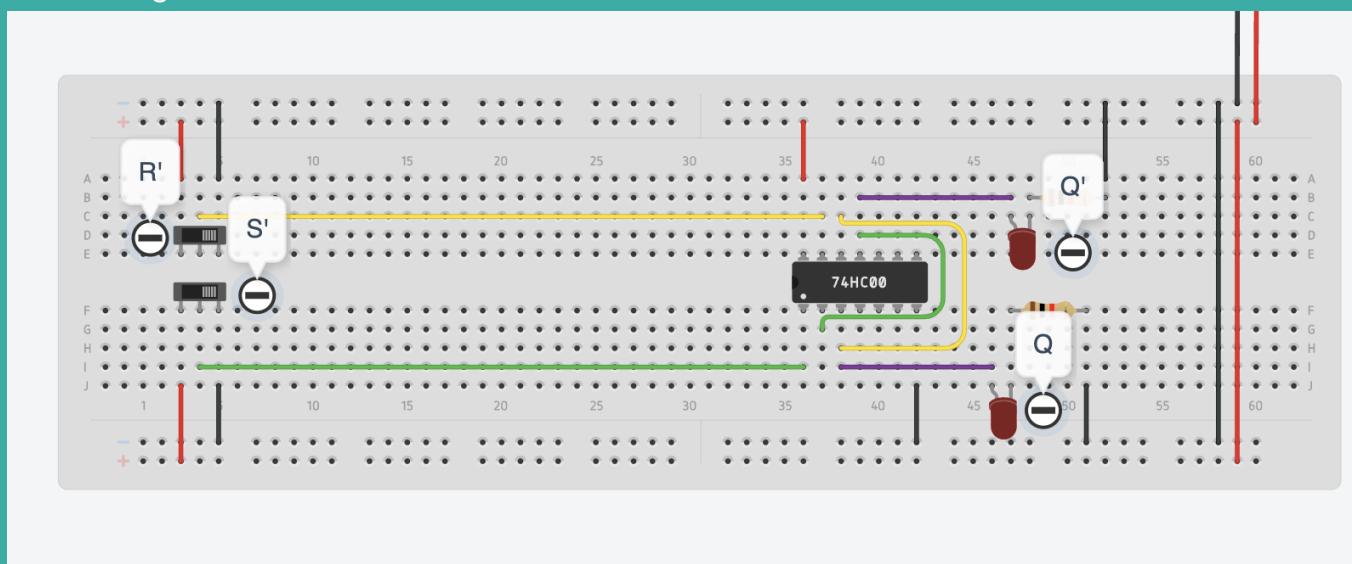
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Pin Diagram of the IC:



Circuit Diagram:



Characteristics equation:

$$Q_n = S' + R Q_{n-1}$$

Characteristic Table and Excitation Table:

| S' | R' | Q | \bar{Q} | |
|----|----|---|-----------|-----------|
| 1 | 0 | 0 | 1 | |
| 1 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | |
| 0 | 0 | 1 | 1 | (Invalid) |
| 1 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 0 | |
| 0 | 0 | 1 | 1 | (Invalid) |
| 1 | 1 | 1 | 0 | |

| S' | R' | Q _n | \bar{Q}_n | |
|----|----|------------------|-----------------|---------|
| 1 | 1 | Q _{n-1} | \bar{Q}_{n-1} | |
| 1 | 0 | 0 | 1 | |
| 0 | 1 | 1 | 0 | |
| 0 | 0 | 0 | 1 | Invalid |

Observations/Results: Created a SR Latch using NAND gate and checked its implementation

Application: SR Latch is used to store a bit of data