AUTUMN MID-SEMESTER EXAMINATION-2024-25
School of Computer Engineering
Kalinga Institute of Industrial Technology
Deemed to be University

3rd Semester

Subject: Digital System Design (EC20005) (Regular)

Format-1

Instructions:-

- 4 (four) questions are to be attempted.
- Question Paper consists of 4 (four) Sections i.e. **A, B, C and D.**
- Section **A** is Compulsory.
- The Examinee has to attempt any 1 (one) question each from the Sections **B, C and D.**

Time: 1.5 hours **Full Marks: 20**

The figures in the right-hand side indicate full marks.
All parts of a question should be answered at one place only.

Question No	Section-A	Question	CO Mapping	Marks
Q1.	Question Type (SAT)	Answer the following questions in short.		[1x5]
a		Draw the block diagram of VLSI Design flow.	CO1	
b		If a=4'b0111, and b=4'b1100, then find out $f_3=(\sim a) \wedge (\sim b)$	CO2	
c		How can an XOR gate function as an inverter?	CO3	
d		Explain the Moore's Law	CO1	
e		If $f = \sum(1,4,5,6,7)$, then find the complement of this function *f*.	CO3	
		Section-B		
Q2.		(i)Draw and explain the working of a 4-bit Adder-Subtractor circuit using Full adders and XNOR gates only. (ii)Write the Verilog design code for the above circuit assuming the Full adder module is existing with the module name "*Full_Adder*".	CO4, CO2	[3+2]
Q3.		(i) Write the Verilog design code using gate-level modeling technique for a Full Subtractor, including the simulation code of it's corresponding test bench. (ii)Design a Full Subtractor circuit using two Half Subtractors	CO4, CO2	[3+2]
		Section-C		
Q4		(i) Express the function F=XY+X'Z as a POS. (ii) Simplify the Boolean function given belowusing K-map,and implement the simplified expression using NOR logic only $F(A,B,C,D) = \prod M(0,1,4,6,8,10,11,15).d(2,12,14)$	CO3	[1+2+2]

Q5		(i) Express the function F=(A+B').(B+C') as a SOP. (ii) Represent the following Boolean function $F(A,B,C,D) = \sum m(1,5,6,12,13,14) + d(2,4)$ with its simplest SOP format using K-map, and implement the same using NAND logic.	CO3	[1+2+2]
		Section-D		
Q6		Design a BCD to XS-3 code converter. Also write the Verilog code for the same circuit using data-flow modelling technique	CO4, CO2	[4+1]
Q7		Design a Gray to Binary code converter. Also write the Verilog code for the same circuit using gate-level modelling technique	CO4, CO2	[4+1]