AUTUMN MID SEMESTER EXAMINATION-2023

School of Computer Engineering
Kalinga Institute of Industrial Technology, Deemed to be University
Digital System Design
[EC 20005]

Time: 1 1/2 Hours   Full Mark: 40

Answer any four Questions including Question No. 1 which is compulsory.
The figures in the margin indicate full marks. Candidates are required to give their answers in their own
words as far as practicable and all parts of a question should be answered at one place only.

1.   Answer all the questions.   [2 x 5]

   a) Write some advantages of using digital systems over analog systems? What are the three
      major design specifications for an IC chip?
   b) Perform the following operation using signed 2's complement method: -6-(-13).
   c) Design a full subtractor circuit using two half subtractors.
   d) Differentiate between bit-wise and logical operators with examples.
   e) Simplify the Boolean function $f = AB+(A+B).\overline{(A+B)}$

2.   a) What is Moore's prediction? Explain the major stages of VLSI design flow with relevant
      block diagram.

      b) What are the different types of modelling techniques in Verilog? Explain any two of them
      using suitable example.

                                                              [5+5 Marks]

3.   a) Obtain the minimized expression for the following 4 variable Boolean expression using K-
      map method and implement the minimized expression using NOR gates only.

                  $F(A,B,C,D)= \sum m(11,12,14) + d(3,4,6)$

      b) Prove the following using Boolean algebra: $(A+B).\overline{(A+C)}.(B+C) = (A+B).\overline{(A+C)}$
                                                              [5+5 Marks]

4.   a) Convert gray code 11011 to binary. Design a 4-bit gray to binary code converter with
      proper steps.

      b) Write HDL code for the 4-bit gray to binary converter in gate-level modelling technique
      with test bench code.   [5+5 Marks]

5.   a) What is the difference between encoder and decoder? Write the HDL code for a 3:8
      decoder in data-flow modelling technique with test bench code.

      b) Implement the following boolean function using 3:8 active low decoder circuit:

                  $F(A,B,C,D)= \sum m(1,3,4,5,7)$ [5+5 Marks]

*** Best of Luck ***