

1.Q. Explain the control flags of 8086 Microprocessor.

Ans:- Generally, a 1-Register contains 16 bits.

It has 9 flags and 6 status flags + 3 control flags.

15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
x	x	x	x	0	D	I	T		S	Z	x	NC	x	P	x	C

control flags.

(1). Direction Flag (D) :-

used for stringed (multiple bytes) operations.

if  $D=0$  Auto increment mode : lower address to higher Address

if  $D=1$  Auto decrement mode : higher Address to lower Address.

(2). Interrupt Flag (I) :-

if  $I=1$  : enable all maskable interrupts.

if  $I=0$  : disable all maskable interrupts.

(No effect on Non-maskable).

(3). Trap/ Trace (T) :- Enter into single step execution mode  
for debugging i.e executes 1 instruction and enters into single  
step ISR (Interrupt service Routine)

if  $T=1$  CPU automatically generate an internal interrupt after each instruction

if  $T=0$  no function is performed / No ISR

2. Find out the state of conditional flags of the 8086 microprocessor after execution of following arithmetic operation

②.  $4FH + 48H$  (using 8-bit operation)

$$\begin{array}{r} 01001111 \\ 01001000 \\ \hline 1001 \quad 0111 \\ \text{---} \quad \text{---} \\ \text{OF} \quad \text{SF} \end{array}$$

$$\begin{aligned} OF &= 0 \\ SF &= 0 \\ ZF &= 0 \\ ACF &= 1 \\ PF &= 0 \\ CF &= 0 \end{aligned}$$

⑤.  $FFFFH + 0001H$  (using 16-bit operation)

$$\begin{array}{cccc} \text{1111} & \text{1111} & \text{1111} & \text{1111} \\ \text{0000} & \text{0000} & \text{0000} & \text{0001} \\ \hline (1) \quad 0000 & 0000 & 0000 & 0000 \end{array}$$

$$\begin{aligned} ZF &= 1 \\ ACF &= 1 \\ PF &= 1 \\ CF &= 1 \\ OF &= 1 \\ SF &= 0 \end{aligned}$$

④ F5H - 3FH (Using 8-bit operation)

$$\begin{array}{r}
 \begin{array}{c} 000 \\ \text{F5H} \end{array} \quad \begin{array}{c} 101 \\ \text{3FH} \end{array} \\
 - \begin{array}{c} 0011 \\ \text{1111} \end{array} \\
 \hline
 \begin{array}{c} 1011 \\ \text{B} \end{array} \quad \begin{array}{c} 0110 \\ \text{6} \end{array}
 \end{array}$$

$$OF = 0$$

$$SF = 0$$

$$ZF = 0$$

$$ACF = 0$$

$$PF = 0$$

$$CF = 0$$

⑤ Derive the logical expression of control signal for following operations in 8086 microprocessor.

(a) Memory read operation

(b) memory write operation

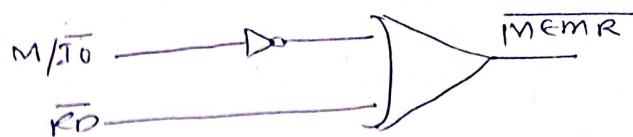
Ans:  $\overline{RD} = 0$ , read operation  
 $= 1$ , no read operation.

$\overline{WR} = 0$ , write operation  
 $= 1$ , no write operation.

$M/\overline{IO} = 0$ , from I/O device  
 $= 1$ , from memory.

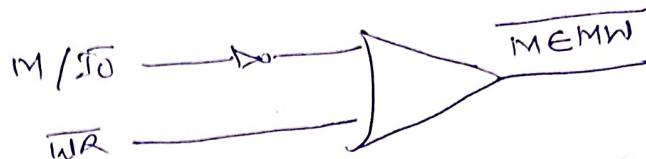
$\overline{RD}$	$M/I\bar{O}$	$\overline{MEMR}$
0	0	1
0	1	0
1	0	1
1	1	1

$$\overline{MEMR} = \overline{M/I\bar{O}} + \overline{RD}$$



$\overline{WR}$	$M/I\bar{O}$	$\overline{MEMW}$
0	0	1
0	1	0
1	0	1
1	1	1

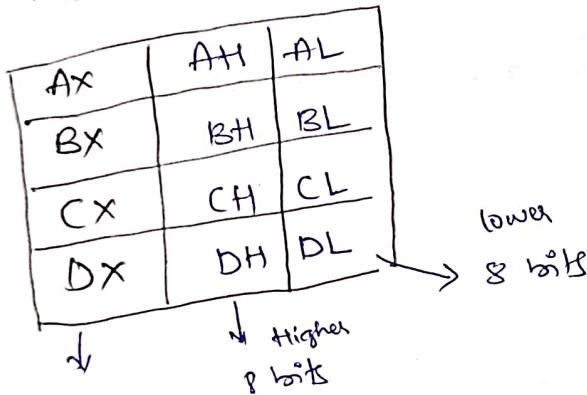
$$\overline{MEMW} = \overline{M/I\bar{O}} + \overline{WR}$$



4. Explain general purpose registers of 8086 microprocessor.

Ans: General purpose Registers.

We have 4 General purpose Registers.



16 bits  
represented

\* For 8 bit operation;

AX: Default accumulator                                  Indirect addressing mode

BX: Base address / offset write

CX: Default counter for loop

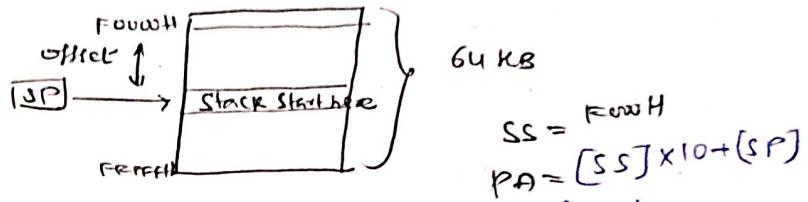
DX: Default destination / implicit operand / string instructions.

Q6. What is stack pointer and what is the need of stack?

Ans: In the context of the 8086 processor, the stack pointer is a register that holds the memory address of the top of the stack. The stack is a region of memory used for temporary storage of data during program execution.

- The stack pointer keeps track of the current position on the stack.
- The operation is on LIFO (Last-in-first-out)
- The stack pointer is initially set to point to an empty location at the top of the stack.

### Needs of stack:



① Function call: When a program calls a subroutine or a function, it needs to pass parameters and return addresses.

2. Local variables: The stack can be used to allocate memory for local variables within a subroutine.

3. interrupt handling: When an interrupt occurs, the processor needs to temporarily suspend the current program execution and handle the interrupt.

4. stack-based operations: The stack also facilitates various stack-based operations, such as push and pop instructions, which make it easier to manipulate data and control program flow.

By utilizing stack, the 8086 processor can efficiently manage function calls, local variables, interrupts, and other operations, making it a fundamental component of program execution and memory management.

## MID SEMESTER EXAMINATION

1. What do you mean by addressing modes? What are the different addressing modes supported by 8086? Explain each of them with suitable examples.

Ans: Different ways in which source operand is denoted in an instruction is called Addressing modes.

1. Immediate Addressing mode:

The addressing mode in which the data operand is part of the instruction itself.

- constant value

Exn: `MOV CX, 9430H`  
`MOV AL, E6H.`

2. Register Addressing mode:

It means that the register is the source of an operand for an instruction.

Exn: `MOV CX, AX;`

Both are registers. copies the content of 16-bit AX register move into 16 bit CX register.

3. Direct Register Addressing mode:

- The address mode in which the effective address of memory location is written directly in the instruction.

Exn: `MOV AX, [192H]`

offset  
→ direct address  
memory location

#### 4. Register indirect addressing mode:

This addressing mode allows data to be addressed at any memory location through an offset [logical address] address held in any of the following like

1. Base pointer [BP]. destination index (DI)
2. base register [BX] source index (SI).

Ex: `Mov AX, [BX];`

Suppose the register BX contains 4895 H, then the contents 4895 H moved to AX.

#### 5. Based addressing mode:

The offset address [logical address] of the operand is given by the sum of contents of BX/BP register and 8/16 bit displacement.

Ex: `Mov BX, [BX + 04];`

Same as adding the displacement to the indirect addressing mode.

#### 6. Indirect addressing mode:

The operand offset [logical address] address is found by adding the contents of source index (SI) / destination index (DI) register & 8 bit / 16 bit displacement.

Ex: `Mov BX, (SI+16);`

#### 7. Based Indirect addressing mode:

The offset address of operand that is computed by adding the base register to the content of indexed register

Ex: `ADD CX, [AX+SI];`

(2). What are the different instruction types of 8086 ? ⑧

Ans: 8086 processor supports 8 types of instructions.

- ① Data transfer instructions
- ② Arithmetic instructions
- ③ Bit manipulation instructions
- ④ String instructions
- ⑤ Program execution transfer instruction
- ⑥ Process control instruction
- ⑦ Iteration control instruction
- ⑧ Interrupt instruction.

## 2. Data Transfer Instructions:

These instructions are used to transfer the data from the source operand to the destination operand.

- instruction to transfer a word : MOV, PUSH, POP, XCHG...etc.
- instruction to transfer a address : LEA, LDS, LES ...etc...
- instruction to transfer input/output port : IN, OUT.
- instruction to transfer flag register : LAHF,  
SAHF,  
PUSHF,  
POPF.

## 2. Arithmetic Instructions:

These instructions are used to perform arithmetic operation like addition, subtraction, multiplication, division.. etc..

- instruction to perform addition : ADD, ADC, INC, AAA..etc,
- instruction to perform multiplication : MUL, IMUL, AAM..etc,
- instruction to perform subtraction : SUB, SBB, DEC..etc,
- instruction to perform division : DIV, IDIV, AAD..etc

### ③ Bit Manipulation Instructions:

(9)

These instructions are used to perform operations where data bits are involved i.e. operations like logical shift etc...

- (i) NOT, AND, XOR, TEST.
- SHL, SAL, SHR, SRR
- ROL, ROR, RCR, RCL.

### ④ String Instructions:

String is a group of bytes/words and their memory is always allocated in a sequential order.

- REP
- REPE / REPZ
- REPNE / REPNZ
- MOVS / MOVS B / MOVS W
- CMPS / CMPS B / CMPS W
- INS / INS B / INS W
- OUTS / OUTS B / OUTS W

### ⑤ Program Execution Transfer Instructions:

Used to transfer / branch the instruction during an execution

- CALL, RET, JMP.
- JC, JE, JZ, JNC, JS, JO..etc..

### ⑥ Processor Control Instructions:

Used to control the processor action by setting / resetting the flag values.

- STC, CLC, CMC, STD, CLD, STR, CLI..

### ⑦ Iteration Control Instruction:

Used to execute the given instruction for number of times.

- LOOP / LOOPZ
- LOOPNE / LOOPNZ
- JCXZ.

③ Draw the register organization of 8086 and explain typical applications of each register. (10)

The 8086 microprocessor has a complex register organization, consisting of several general-purpose registers, segment registers, index registers, and control registers. Here is a simplified representation of the register organization of the 8086:

### 1. General-Purpose Registers:

• AX : Accumulator register (16 bits)

Typical applications: arithmetic operations, data storage, and data manipulation.

• BX : Base register (16 bits)

Typical applications: used as a pointer to data in memory or as an offset for addressing.

• CX : Count register (16 bits)

Typical applications: used as a counter in loop operations and shifts.

• DX : Data register (16 bits)

Typical applications: used in I/O operations, as a temporary storage, or as a divisor in multiplication and division instructions.

Note: Each general-purpose register can be accessed as two 8-bit registers, such as AH/AL, BH/BL, CH/CL, and DH/DL.

### 2. Segment Registers:

1 MB of memory segmented to 16 parts each of 64 KB.

Memory can be classified as 4 types of segments.

#### (i) code segment:

- stores codes

- stores address of its line of code.

### ② Data segment:

- stores data / values
- stores address of its data in memory segment.

### (iii) Stack segment:

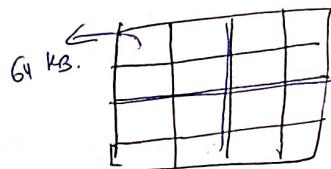
- used as stack LIFO memory
- used to store address of top of stack.

### (iv) Extra segment:

- store address of embark data.

- Each code, Data, stack and Extra segments can hold 16 words of data  
 - but physical address is of 20 bits.

$$2^{16} = 64 \text{ KB memory location}$$



### ③ pointer and index register:

- pointer: we have three pointers.

- Instruction pointer (IP)
- Segment pointer (SP)
- Base pointer (BP)

After each instruction IP will be increasing by 2 (not CS.)

- CS X 10H + IP (segment pointer)
- DS X 10H + BP (segment pointer)
- SS X 10H + SP (segment pointer)

### ④ index register:

we have two types of index register.

- Source index (SI)

- Destination index (DI)

(i) source index: store / locate / pointer source data  
 $DS \times 10H + SI$

(ii) destination index (DI): pointer destination data.  
 $DS \times 10H + DI$

(1) Draw and discuss flag registers of 8086 in brief. (12)

v Flags in 8086:

9 flags - 1 Register - 8 bits

x	x	x	0	D	P	T	S	Z	X	AC	X	P	X	C
Do														

Dir

- Sign Flag(S): MSB of resultant is copied

1 → neg Number  
0 → positive Number

- Zero Flag(Z):

If resultant is 0, then flag is 1.

- (Auxiliary carry) AC = 1: whenever carry from lower nibble to higher nibble  
to higher nibble {3rd bit to 4th bit {index starting from 0} during  
BCD; used internally by processor.

$$\begin{array}{r} & & \text{(C)} \\ & 0011 & | & 1001 \\ 0101 & | & 1001 \\ \hline & & 0010 \end{array}$$

AC = 1.

- parity flag(P): It check the no. of one's in result.

even parity: no. of 1's in resultant = 2

odd parity: no. of 1's is odd then → 0.

- carry flag(C): carry / borrows if generated during arithmetic operation  
then it is '1' else if is '0'.

→ overflow(O): The flag is set to one, if an overflow occurs, i.e. if the

result of signed operation is greater than the destination register.

MN B

1 → negative  
0 → positive

- Resultant is > 15 bits, signed operation means  
MSB is reserved for sign → 0 = 1.

## \* control flags:

- direction flag (D):
  - $D=0$  : autoincrement mode; move address to higher address.
  - $D=1$  : autodecrement mode; move address to lower address.
- interrupt flag (I):
  - $1$  : enable all maskable interrupts
  - $0$  : disable all maskable interrupts  
(no effect on non-maskable)

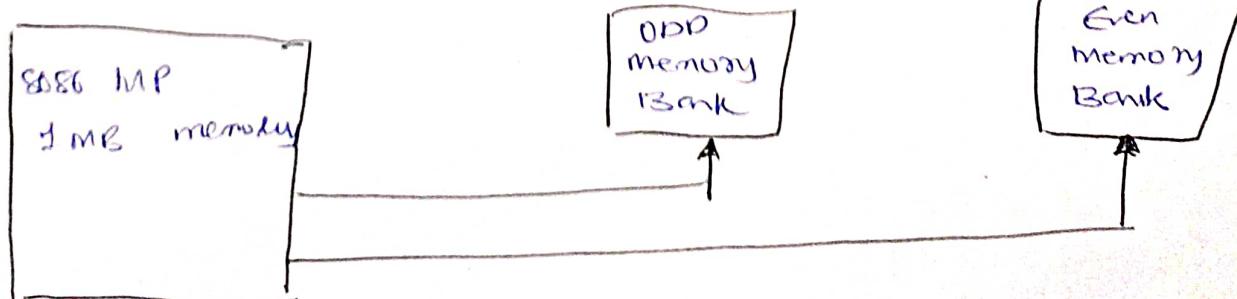
- trap/trap: enter into single step execution mode for debugging i.e. executes 1 instruction and enter into single step ISR (interrupt service Routine).
  - $1 \rightarrow$  CPU automatically generates.
  - $0 \rightarrow$  no function is performed / no ISR.

## ⑤. Explain the physical memory organization in an 8086 system:

there are 20 address lines in the 8086 microprocessor. This gives us 2<sup>20</sup> different memory locations. Hence the total size is 2<sup>20</sup> bytes, which is equal to 1 MB.

- Even the memory is byte-addressable yet the 8086 microprocessor can easily handle up to 16 bytes of data at a time through its 16 data lines so, to organize the memory efficiently, the entire memory in 8086 divided into two memory banks.

odd bank and even bank.



OR

## Concept of segmented memory:

(14)

The concept of segmented memory is a memory organization scheme used in the 8086 microprocessor and similar architectures.

In segmented memory, the total addressable memory space is divided into segments, each identified by a segment address and an offset address.

In the 8086 architecture, a segment is a continuous block of memory, is divided into multiple segments, and each segment is addressed using a 16-bit segment register and a 16-bit offset register.

$$\text{Physical Address} = (\text{Segment Reg} \times 10) + \text{Offset Register}$$

### \* Advantages of segmented memory:

1. Increased Addressable Memory
2. Flexibility in memory management
3. code and data separation
4. Efficient memory access.
5. Support for real mode and protected mode

6. Answer the following questions.

(i). What is the range of physical address if  $CS = FF59H$ ?

$$PA = FF590 + 0000 = FF590H$$

$\begin{array}{r} 1111111010110000 \\ 1111111111111111 \\ \hline 10000111010110001111 \end{array}$

$$\text{last PA} = FF590 + FFFF = 0F58FH$$

(ii) Which register(s) are used to access the stack?

Ans: the base pointer and stack pointer registers.

(iii). If control is transferred outside the current code segment, is it NEAR or FAR?

Ans: If the control is outside the current code segment it is FAR.

(iv). In unsigned multiplication of AX and BX, in which register, the product is placed in?

Ans: AX and DX

(v). To set all bits of an operand to 1, it could be ORed with 1.

(vi). To set all bits of an operand to 0, it could be ANDed with 0.

7. Explain the following instruction of 8086 with suitable examples

(i) MOV. - Move is used to transfer the data from source to destination.

Ex:  $MOV AX, 5000H$

$MOV DS, AX$

$MOV AH, 2000H$

(ii) PUSH: push is used to add the data in stack.

Ex:-  $MOV BX, 2000H$   
 $PUSH BX.$

(iii) POP: pop is used to remove or delete the data in stack.

Ex:-  $MOV BX, 2000H$   
 $PULL BX$   
 $POP 16X.$

(iv) ADD: used to addition of destination and source.

Ex:-  $ADD AL, 20H$   
 $ADD AH, AL$   
 $ADD AX, BX$

(v) MUL: used to multiple two instructions .. only the source  
- if the source is of 8 bits , it will multiply with AL and result  
will be stored in AX register.  
- if the source is of 16 bits , it will multiply with AX and  
result will be stored in DX-AX register.

Ex:-  $MUL BL;$   
 $MUL BX;$

(vi) DIV: source.

- It divides a word(16) by byte(8) and a double word by word.  
- If divisor is of 8 bits , it will divide with AX and result  
of 8 bits , it will divide with AX and result of quotient  
will be store in AH register and remainder stored in AH

Ex:-  $DIV BL$   
 $DIV BX$

(vii) CMP: Destination, Source.

- used to comparison
- if designation is greater than source , carry flag = 0
- if designation is less than source , carry flag = 1.
- if designation is equal to source , zero flag = 1.

Ex: CMP AL, BL

CMP, CL, BH

CMP BX, AX.

(viii) DAA: Decimal adjust after addition

- in any microprocessor , we perform addition in binary / hexa-decimal
- But in real world , we understand things in decimal addition.
- so DAA instruction is used after addition to show adjustment which gives decimal addition.

Add 0FH with AL . if lower nibble &gt; 9

on Auxiliary Carry = 1

Add 60H with AL, higher nibble &gt; 9

or carry = 1.

Ex: ADD AL, BLif  $AL = 20H$   
 $BL = 40H$ AL. 60H(ix) AND: Destination, source.

- perform logical AND operation b/w destination and source.
- destination can be register or memory location
- source can be register or memory location

Ex: AND AL, BL.if  $AL = 42H$  $BL = 56H$ 

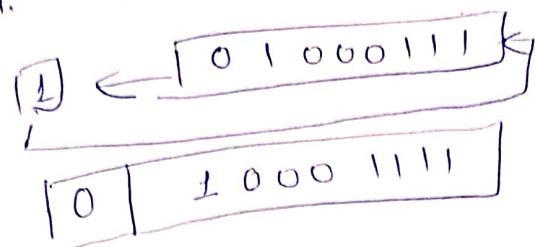
0100 1011 6

0011 0110 5

0000 0110 = 06H

- RCL: destination, cant.
- This instruction performs Rotate bits left with carry.
  - If cant is greater than d, then it has to be stored in CL register.

Ex: RCL, DH, 1  
if DH = 47H. = 0100 0111 b and carry = 1.



$$\text{DH} = 8\text{FH}, \\ \text{CF} = 0.$$

After execution  
RCL.

JMP Used to Jump

Ex:

- JMP MLT 2P;
- JMP BX;
- JMP WORD PTR [BX];
- JMP DWRD PTR[SE];

xii) JB/JC/JNAE: (Jump if above or equal / Jump if not below)  
Jump if no carry.

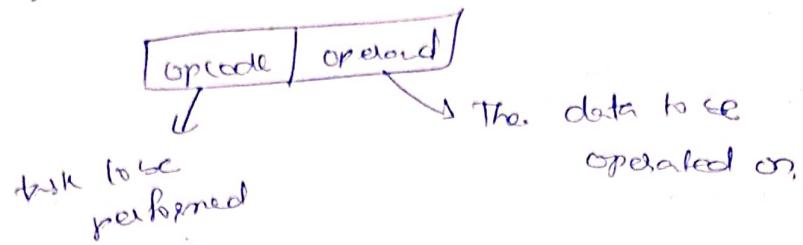
Ex:

CMP AX, 4371H;  
JNB NEXT;

## INSTRUCTION FORMATS:

Instruction: is a command given to the CPU to perform a specific task on specified data.

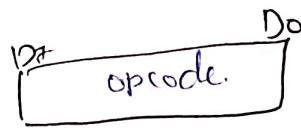
Each instruction has 2-parts



- There are 6-instruction formats for 8086:

- (i) One byte instruction
- (ii) Register to register
- (iii) Register to / from memory with no displacement
- (iv) Register to / from memory with displacement
- (v) Immediate operand to register
- (vi) Immediate operand to memory with displacement.

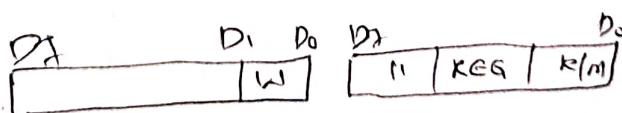
(ii) One byte instruction:



This format is only one byte long.

- This format is only one byte long.
- It may have implied data for register operand.
- The least significant 3-bits of opcode represent the register operand if any.

Ex: DAA.



(ii) Register to Register:

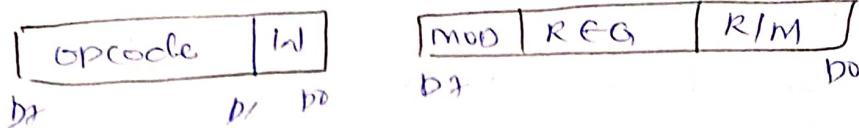
- This format is two bytes long.
- The first byte represents opcode and width of the operand & specifies w=1 for 16-bit operand and w=0 for 8-bit operand.

w=1 for 16-bit operand  
w=0 for 8-bit operand

Ex: MOV AX, BX.

20

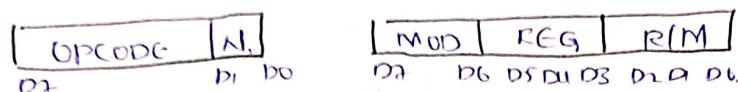
Register to / from memory with no displacement.



- This format is also two bytes long, and similar to Register to Register formats except MOD field.

Ex: MOV AX, [SI]

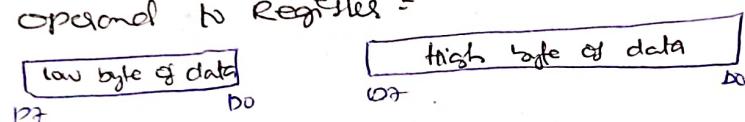
(IV). Register to / from memory with DISP (Displacement).



- The format contains one (or) two additional bytes for DISP along with 2-byte format of register to / from memory without displacement.

Ex: MOV AX, [SI + 2000H].

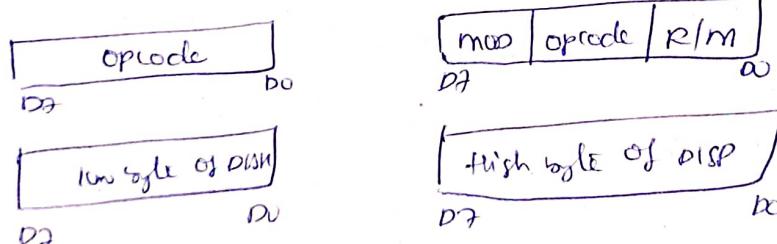
(V). Immediate operand to Register =



- In this format, the first byte and 3-bits from the second byte are used to represent the opcode.

Ex: MOV AX, 1234H.

(VI). Immediate operand to memory with displacement ?



- This format is 5 or 6 bytes long.

- The first 2-bytes represent opcode, mod and R/M fields.
- The next 2-bytes represents displacement.
- The last 2-byte represents immediate data.