ECE2002 –Digital logic And Design

Embedded Lab-

Fall semester 2020~2021

Slot: L41+L42

E-Record

Experiment No. : 2

Submitted by

Name of the Student: ARPIT PATAWAT

Reg. no.: 19BEC0358

1)

If a student Reg.NO is 17BEC0134, then the following minterms (canonical form) will give logical high output

m1	m7	m11	m14	m12	m0	m1	m3	m4

Suppose the same minterm is repeated, consider one time only for making the function.
For example m1 is repeated, hence m1 is considered one time only. The function which is given to the student is given below.

$$f(a,b,c,d)=\sum m(0,1,3,4,7,11,12,14)$$

a) Write the truth table for your function **(1M)**

b) Determine the Sum of Product (SOP) for your function **(1M)**

c) Draw the logic circuit for the SOP **(0.5M)**

d) Draw the NAND alone circuit for the SOP **(0.5M)**

e) Determine the Product of Sum (POS) for your function **(1M)**

f) Draw the logic circuit for the POS **(0.5M)**

g) Draw the NOR alone circuit for the POS **(0.5M)**

h) Write a Verilog gate level and data flow modeling and verify it **(2.5M)**

Note: from a) to g) solve it on A4 sheet.

Ans –

DLD Lab → 41 + 42

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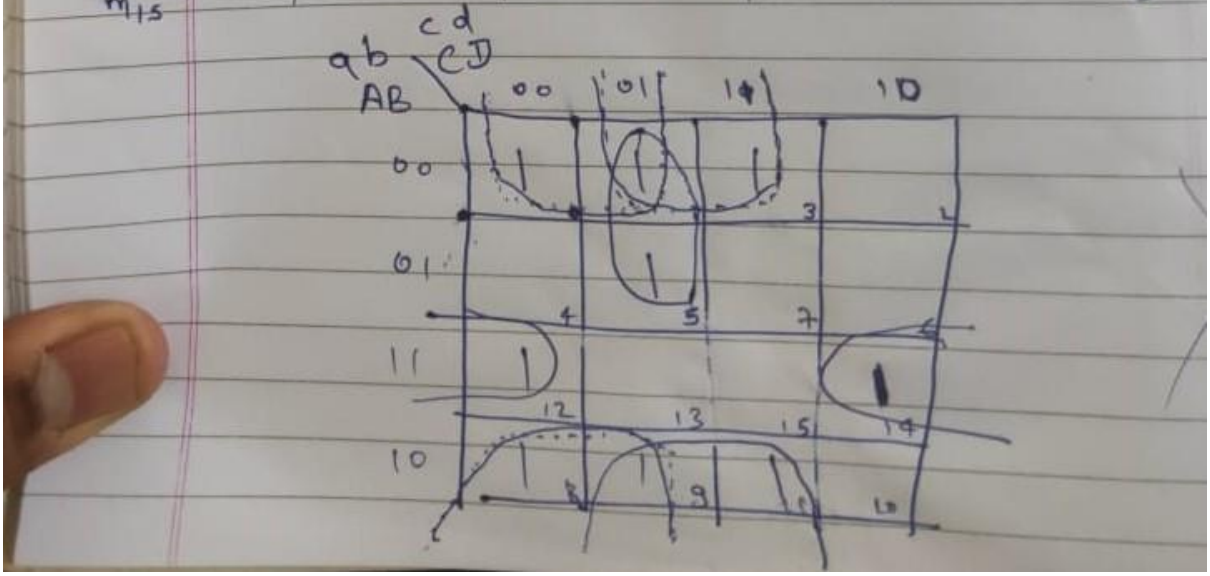
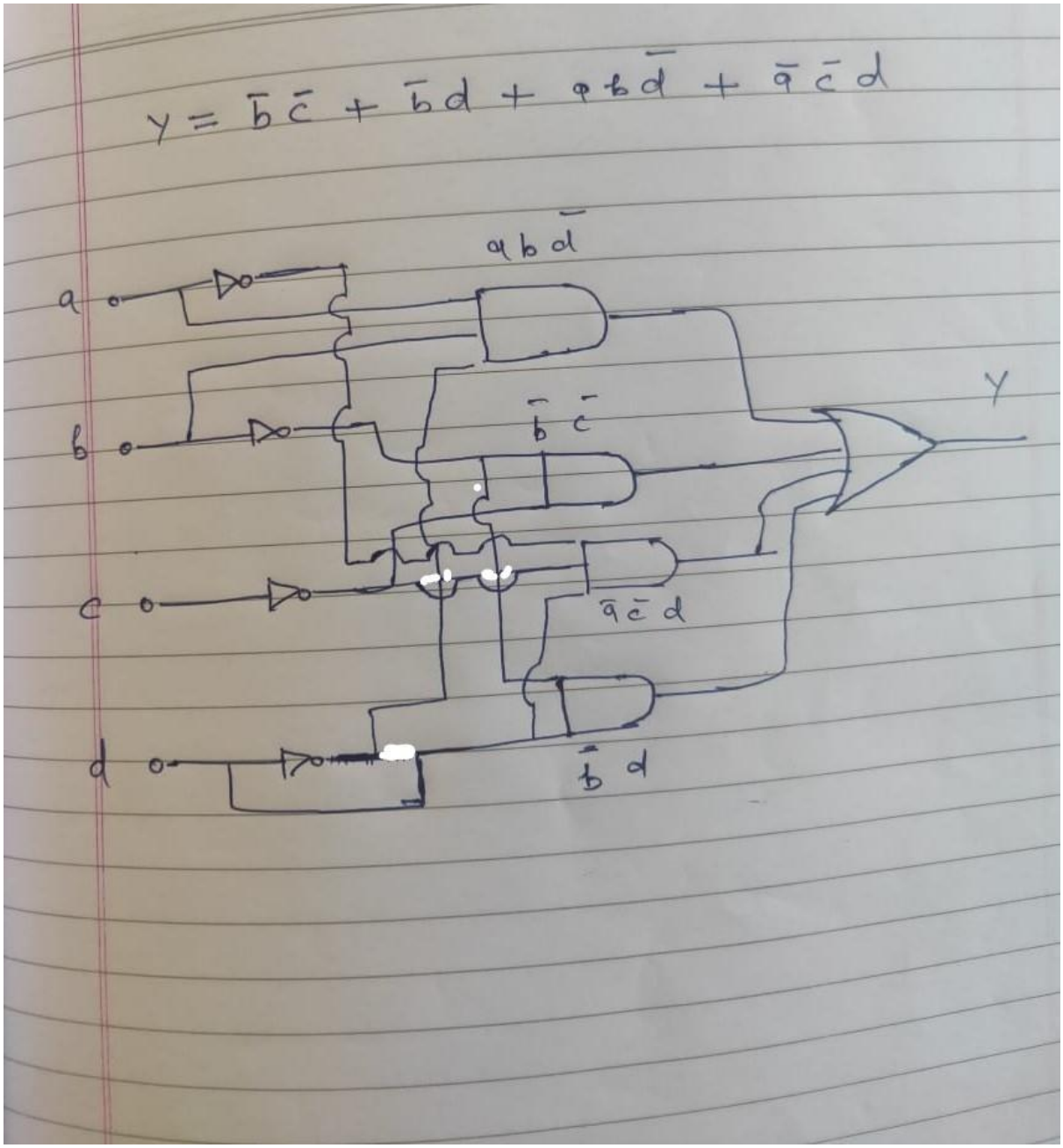
a) Reg. no. = 19BEC0358

$f(a,b,c,d) = \Sigma m(0,1,3,5,8,9,11,12,14)$

Truth table

min term number	a	b	c	d	Y
m_0	0	0	0	0	1
m_1	0	0	0	1	1
m_2	0	0	1	0	0
m_3	0	0	1	1	1
m_4	0	1	0	0	0
m_5	0	1	0	1	1
m_6	0	1	1	0	0
m_7	0	1	1	1	0
m_8	1	0	0	0	1
m_9	1	0	0	1	1
m_{10}	1	0	1	0	0
m_{11}	1	0	1	1	1
m_{12}	1	1	0	0	1
m_{13}	1	1	0	1	0
m_{14}	1	1	1	0	1
m_{15}	1	1	1	1	0




$Y = \bar{b}\bar{c} + \bar{b}d + a\bar{b}\bar{d} + \bar{a}\bar{c}d$
$a\bar{b}\bar{d}$
a
b
c
d
$\bar{b}\bar{c}$
Y
$\bar{a}\bar{c}d$
$\bar{b}d$

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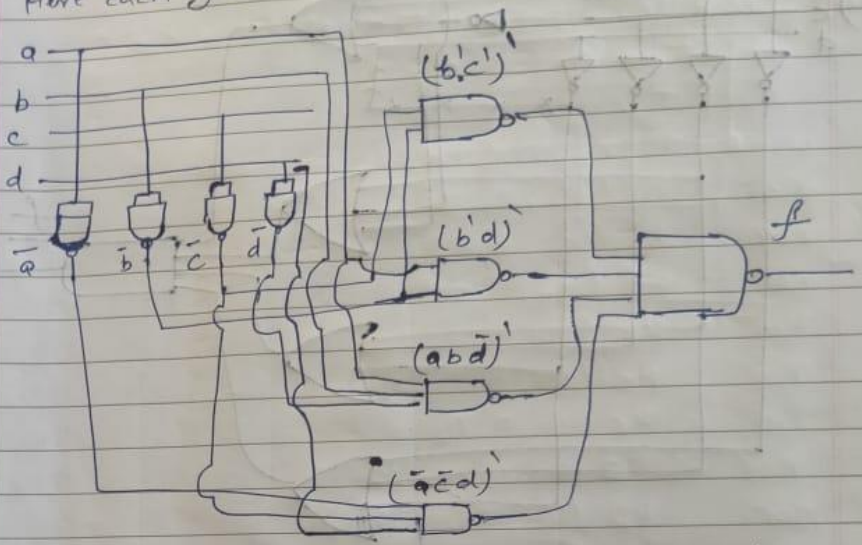
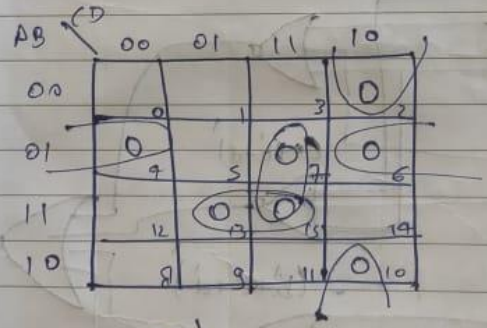
Here each gate is nand gate

d)



e) for Pos taking F Compliment

$M = \sum(2, 4, 6, 7, 10, 13, 15)$



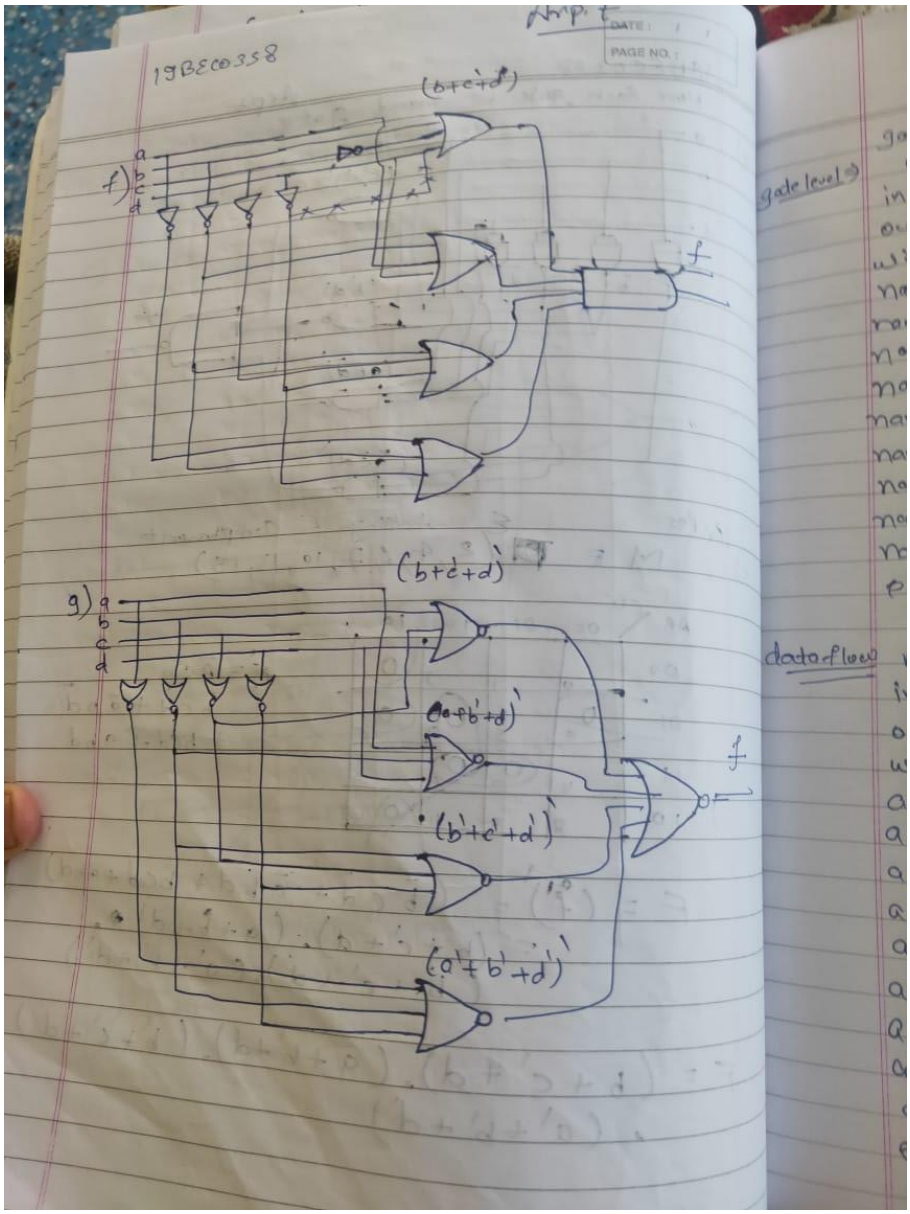
~~$F = \bar{B}C\bar{D}$~~

$\bar{f} = \bar{b}c\bar{d} + \bar{a}b\bar{d} + b\bar{c}d + abd$

$F = (\bar{f})' = (\bar{b}c\bar{d} + \bar{a}b\bar{d} + bcd + abd)'$

$= (b + c' + d).(a + b' + d).(b' + c' + d').(a' + b' + d')$

$F = (b + c' + d).(a + b' + d).(b' + c' + d').(a' + b' + d')$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f)
a
b
c
d
(b+c'+d')
f
gate level
g)
a
b
c
d
(b+c'+d')'
(a+b'+d)'
(b'+c'+d')'
(a'+b'+d')'
f
data flow

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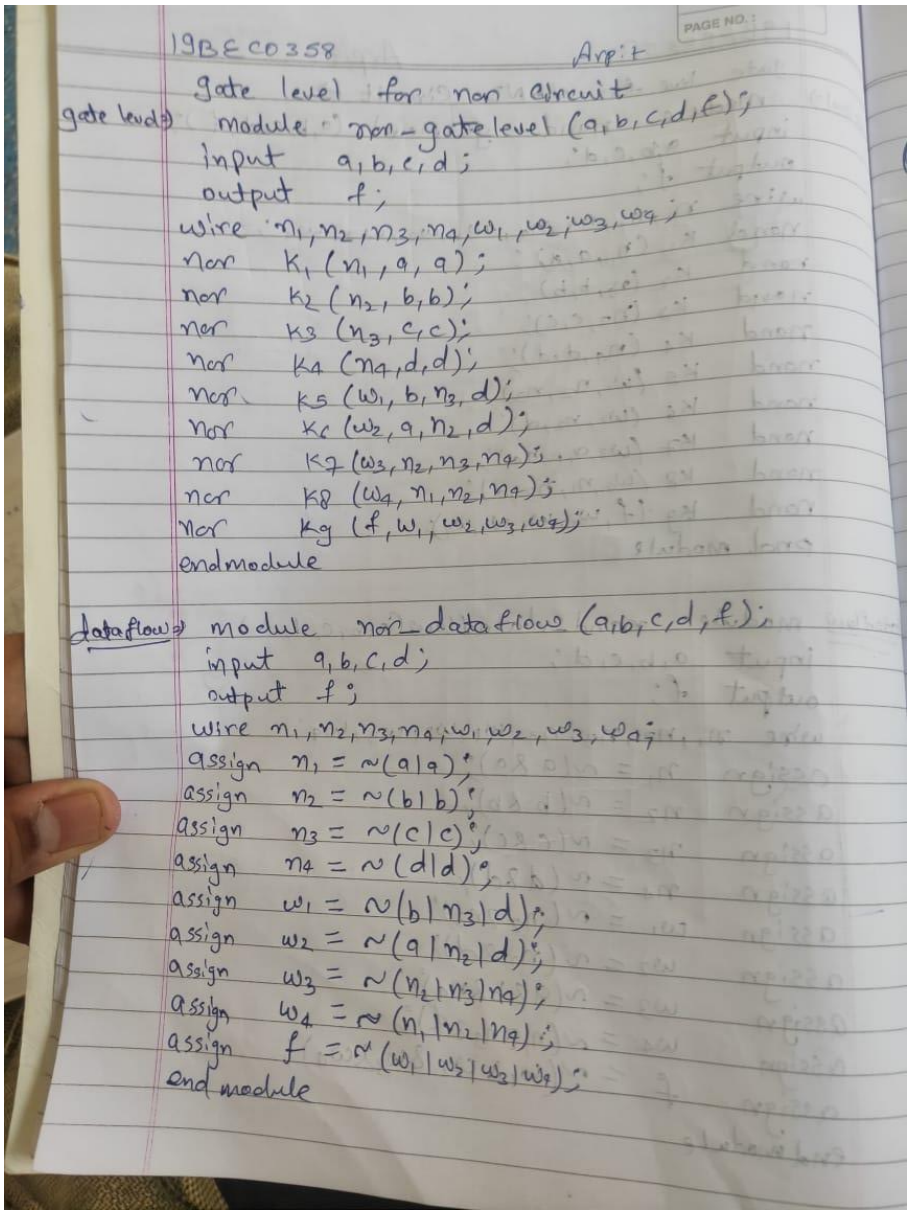
gate level for NAND Circuit →

gate level →

```
module nand_gatelevel (a,b,c,d,f);
input a,b,c,d;
output f;
wire n1,n2,n3,n4,w1,w2,w3,w4;
nand K1 (n1,a,a);
nand K2 (n2,b,b);
nand K3 (n3,c,c);
nand K4 (n4,d,d);
nand K5 (w1,n2,n3);
nand K6 (w2,n2,d);
nand K7 (w3,a,b,n4);
nand K8 (w4,n1,n3,d);
nand K9 (f,w1,w2,w3,w4);
endmodule
```

dataflow

```
module nand_dataflow (a,b,c,d,f)
input a,b,c,d;
output f;
wire n1,n2,n3,n4,w1,w2,w3,w4;
assign n1 = ~(a &a);
assign n2 = ~(b &b);
assign n3 = ~(c &c);
assign n4 = ~(d &d);
assign w1 = ~(n2 &n3);
assign w2 = ~(n2 &d);
assign w3 = ~(a&b&n4);
assign w4 = ~(n1&n3&d);
assign f = ~(w1& w2 &w3&w4);
endmodule
```



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gate level

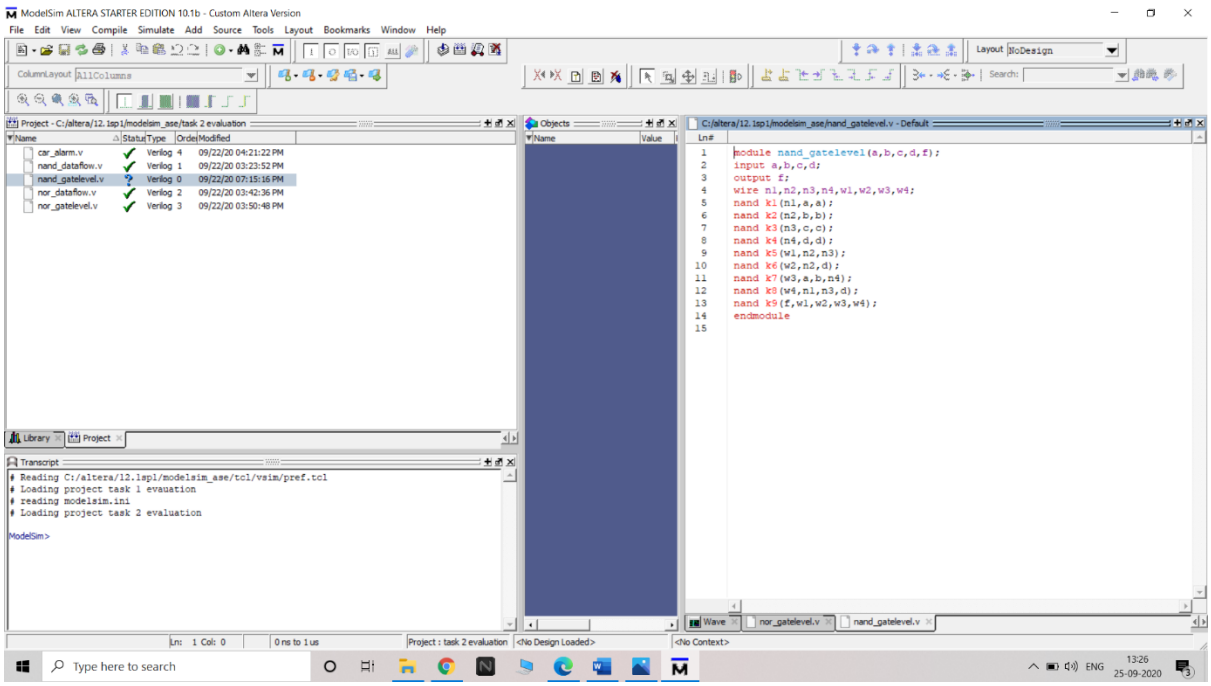
```
module nor_gate_level (a,b,c,d,f);
input a,b,c,d;
output f;
wire n1,n2,n3,n4,w1,w2,w3,w4;
nor K1 (n1,a,a);
nor K2 (n2,b,b);
nor K3 (n3,c,c);
nor K4 (n4,d,d);
nor K5 (w1,b,n3,d);
nor K6 (w2,a,n2,d);
nor K7 (w3,n2,n3,n4);
nor K8 (w4,n1,n2,n4);
nor K9 (f,w1,w2,w3,w4);
endmodule
```

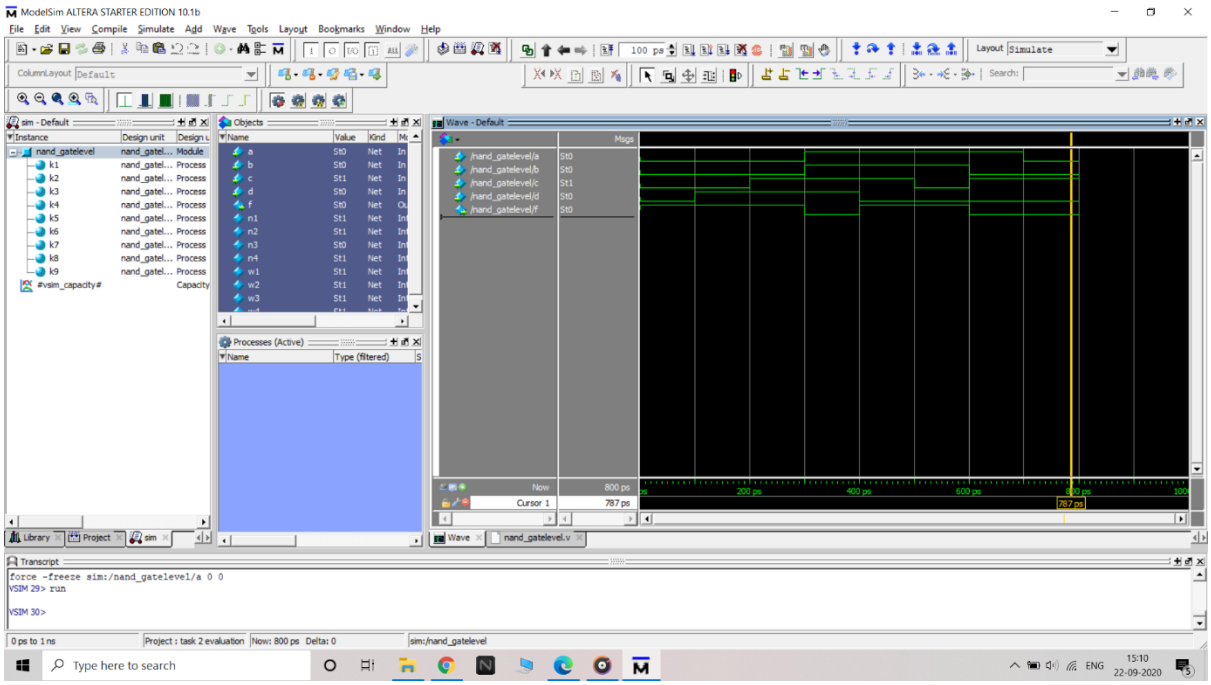
dataflow

```
module nor_dataflow (a,b,c,d,f);
input a,b,c,d;
output f;
wire n1,n2,n3,n4,w1,w2,w3,w4;
assign n1 = ~(a|a);
assign n2 = ~(b|b);
assign n3 = ~(c|c);
assign n4 = ~(d|d);
assign w1 = ~(b|n3|d);
assign w2 = ~(a|n2|d);
assign w3 = ~(n2|n3|n4);
assign w4 = ~(n1|n2|n4);
assign f = ~(w1|w2|w3|w4);
endmodule
```

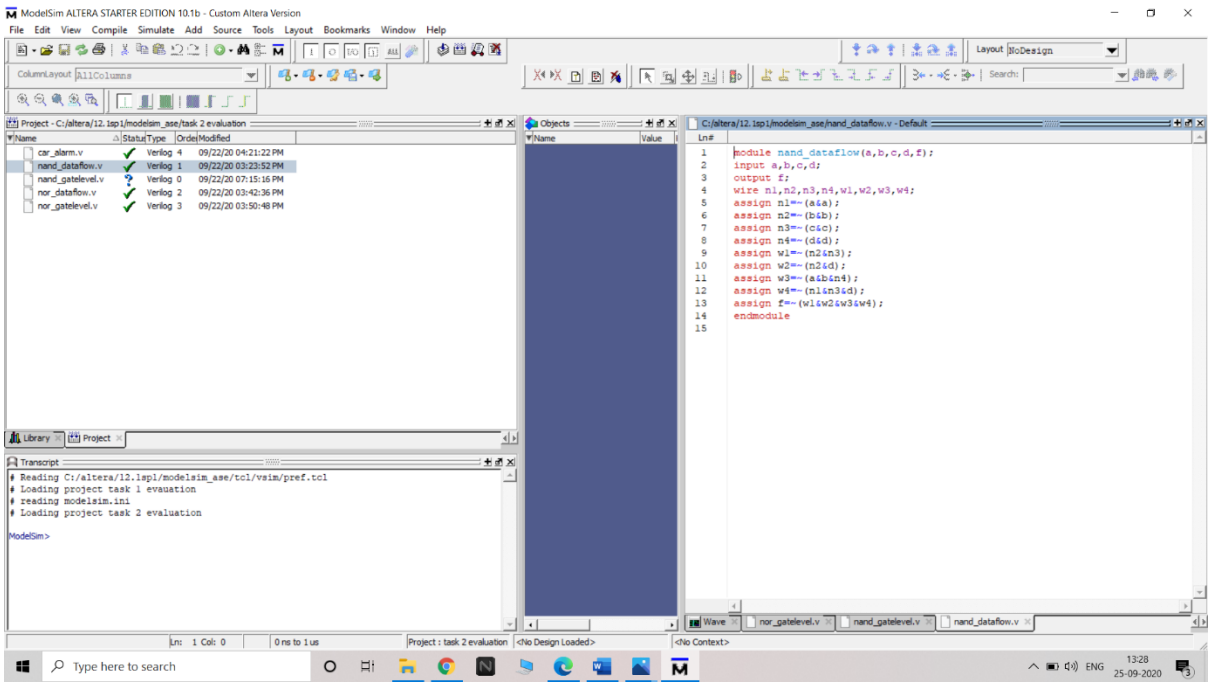
Verilog code –

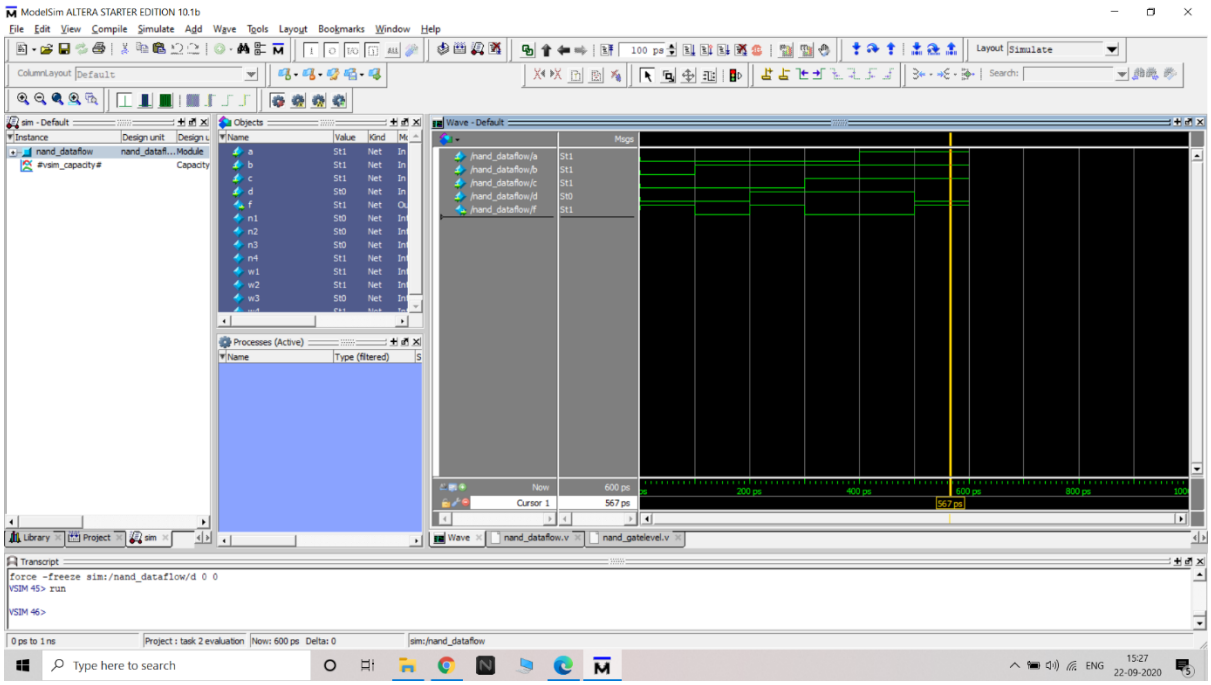
Nand gatelevel



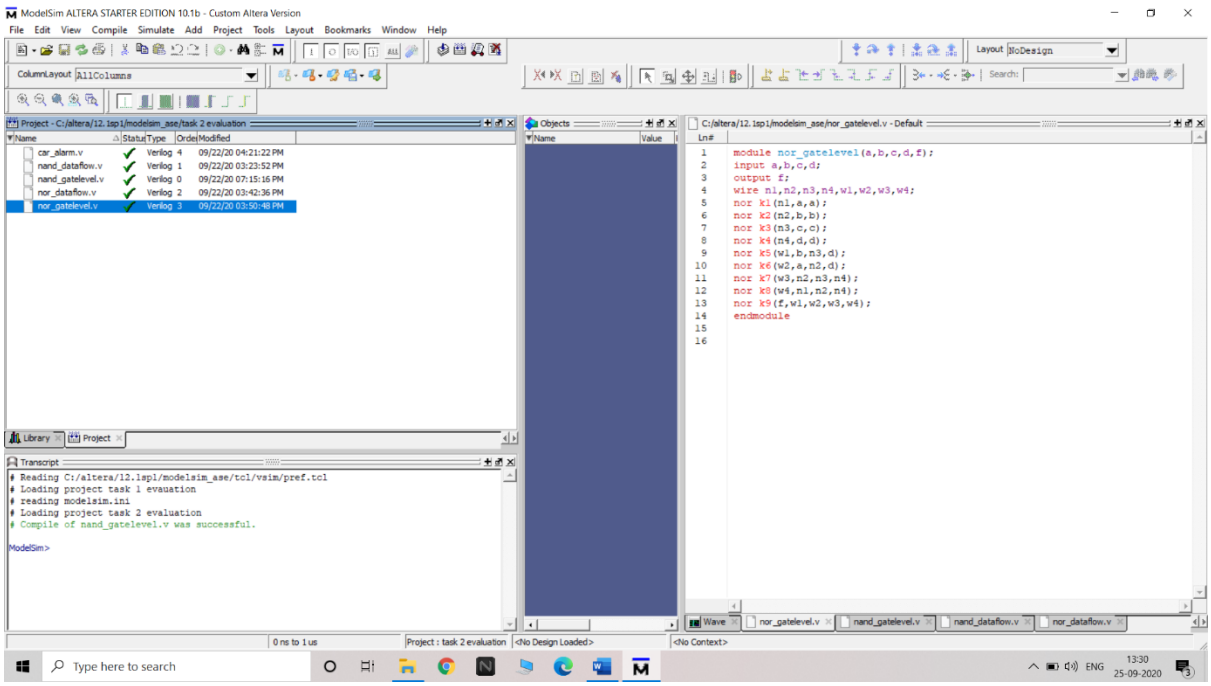


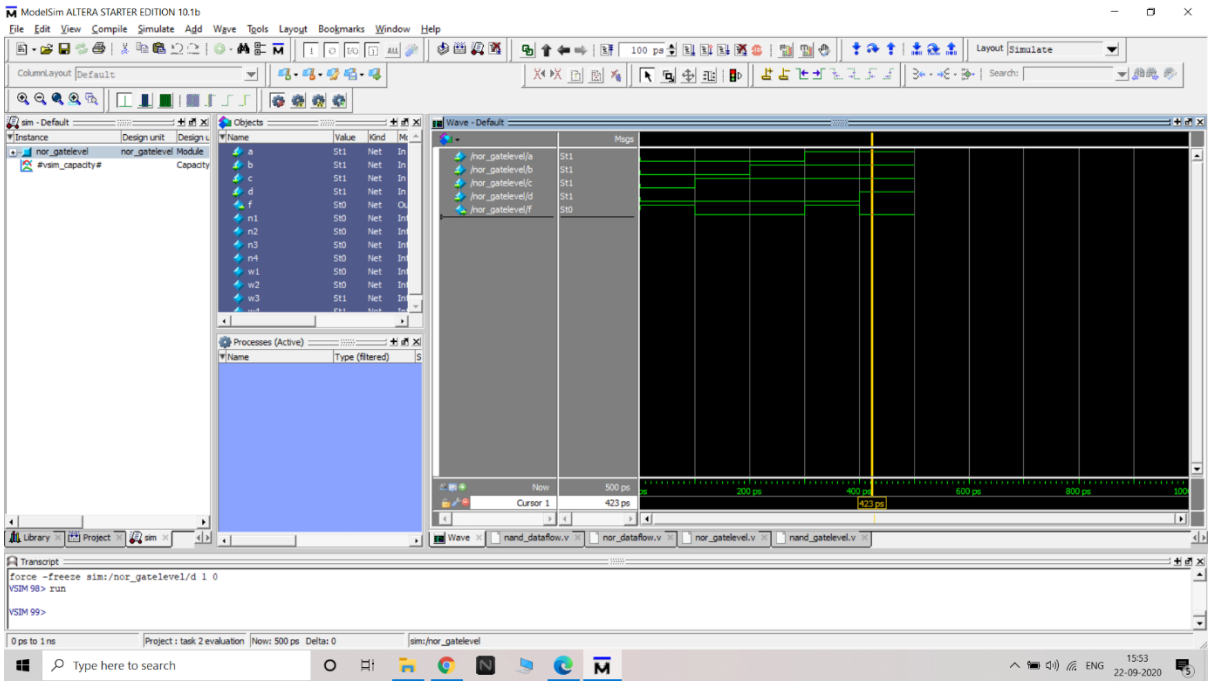
Nand dataflow



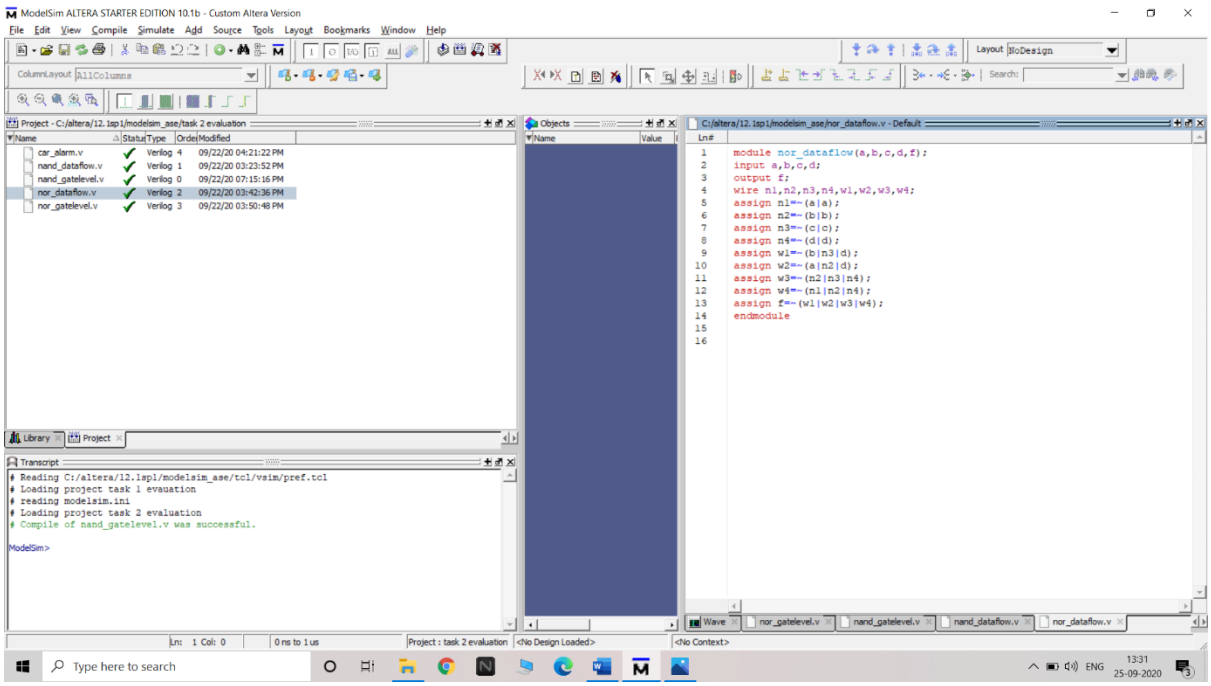


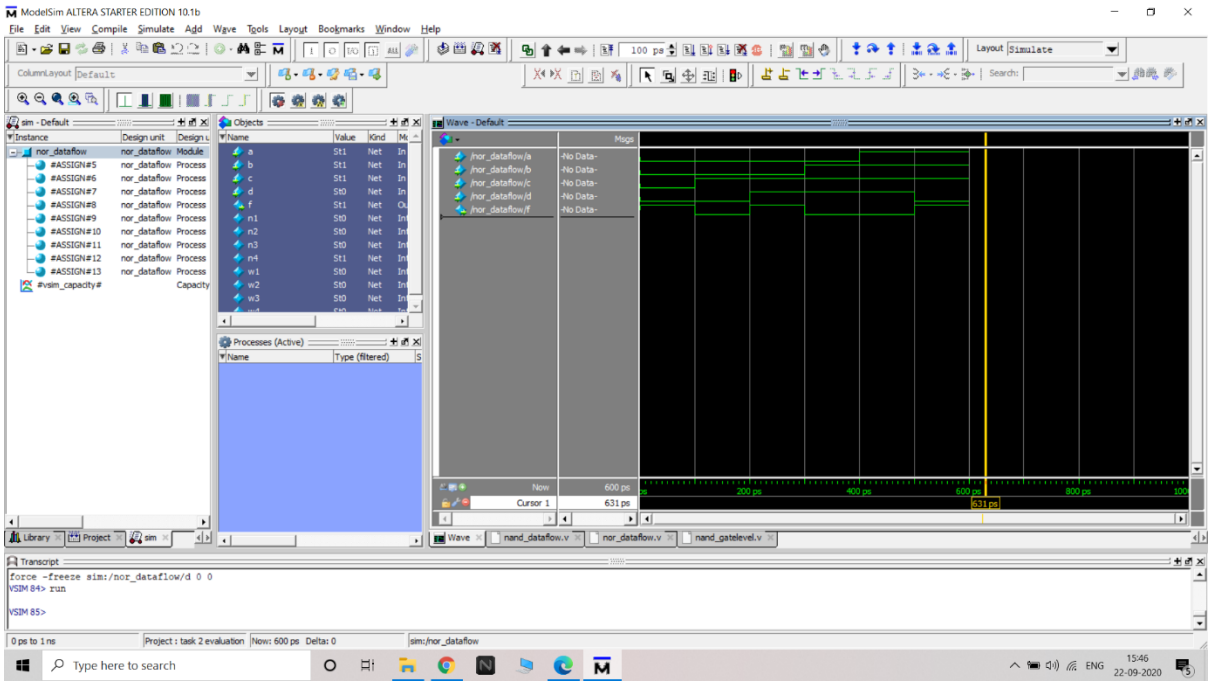
Nor gate level





Nor dataflow





Q2

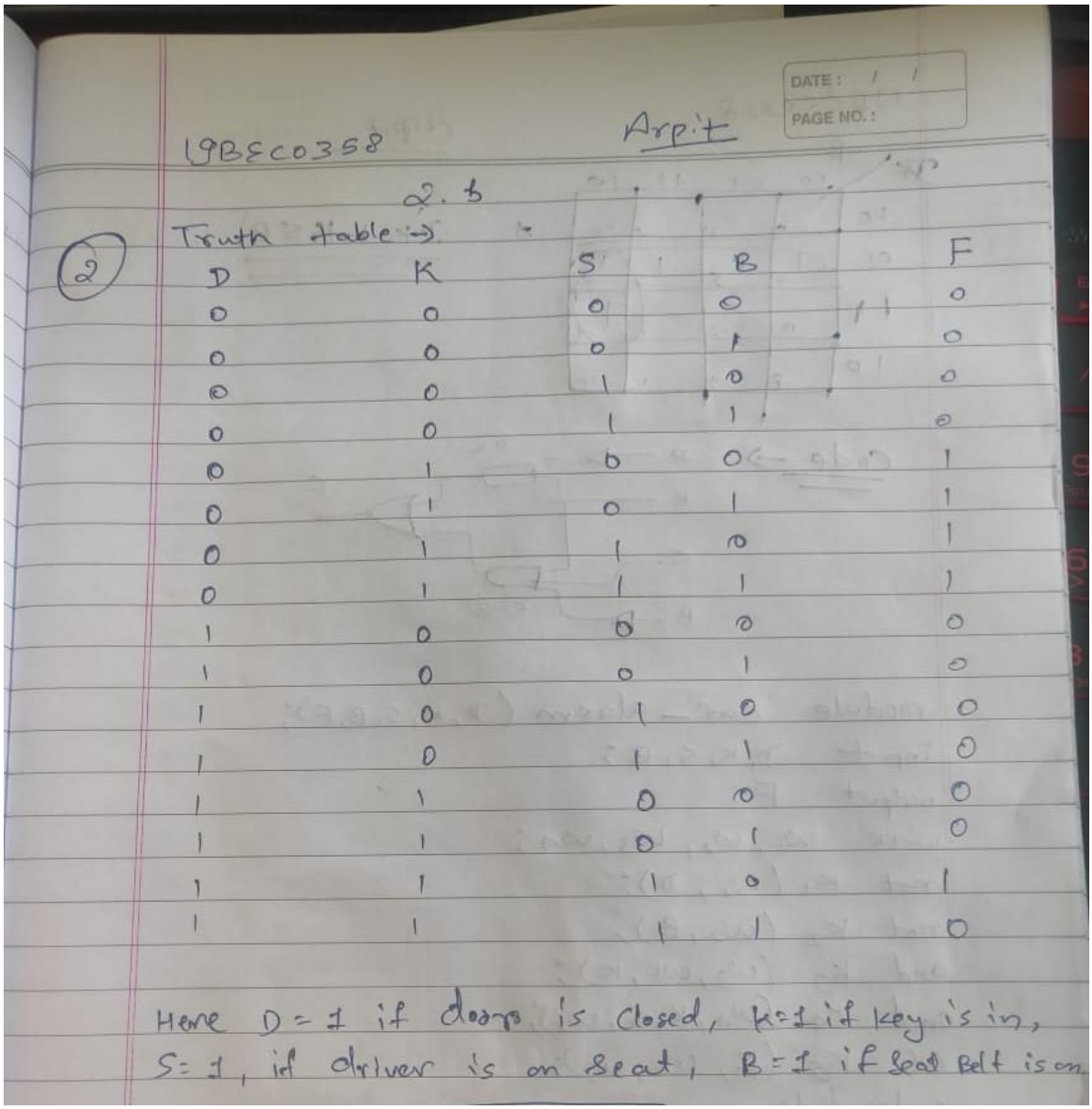
Design a car safety alarm using Logic gates considering four inputs.

Door closed (D), Key in (K), Seat pressure (S) and Belt (B).

Alarm (A) should sound if

- The key is in, and door is not closed, or
- The door is closed and the key is in and the driver is on seat, but seat belt is not strapped.

ANS -



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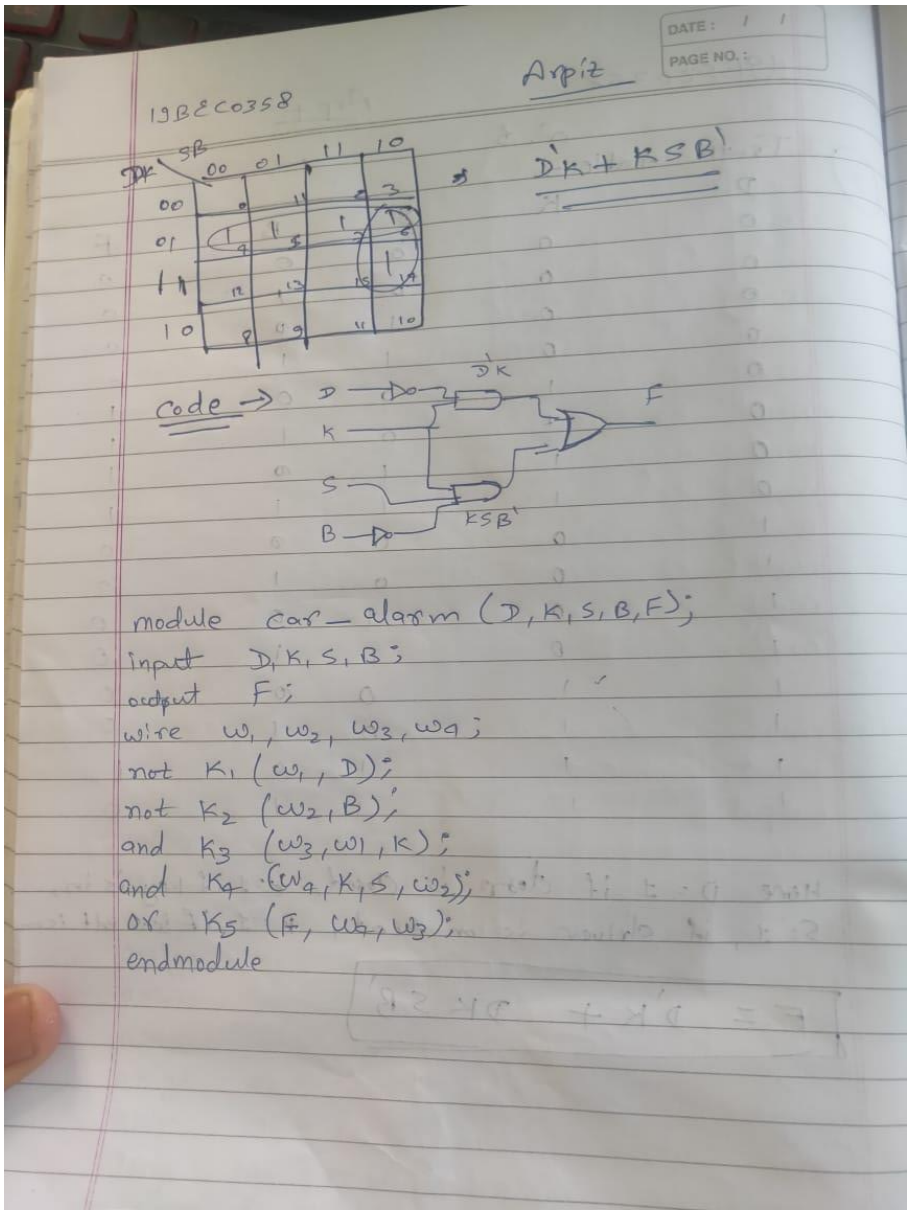
(2) Truth table →

D	K	S	B	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Here D = 1 if doors is closed, K = 1 if key is in, S = 1, if driver is on seat, B = 1 if Seat Belt is on



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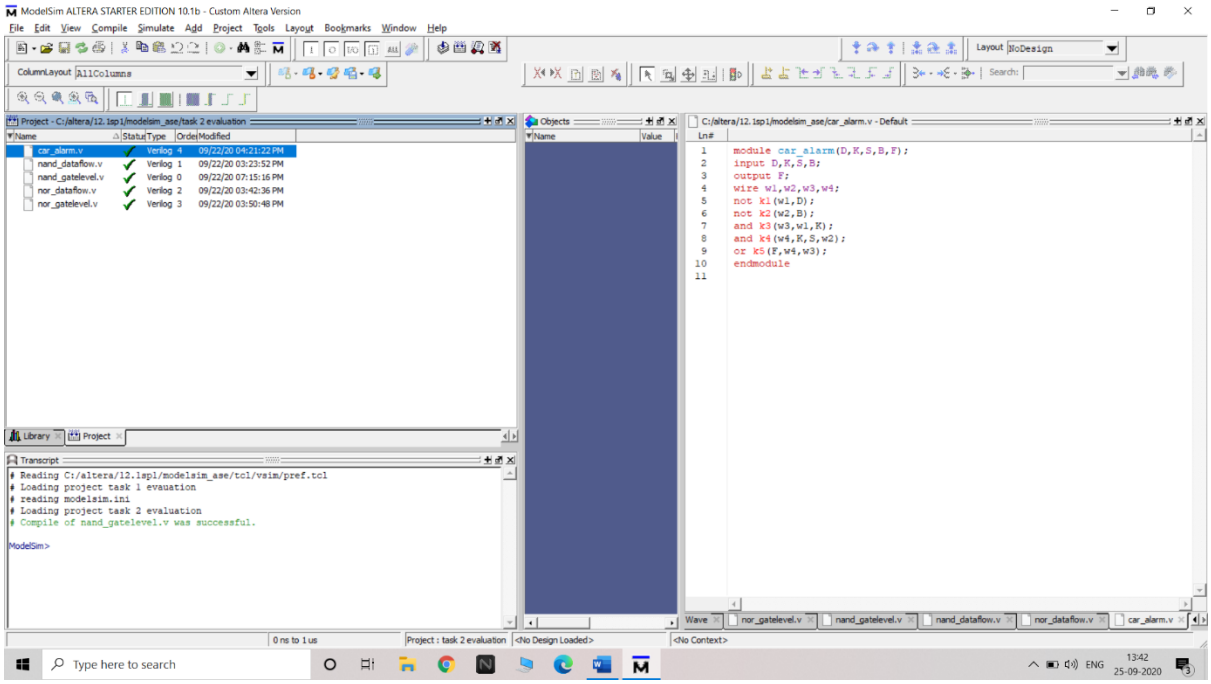
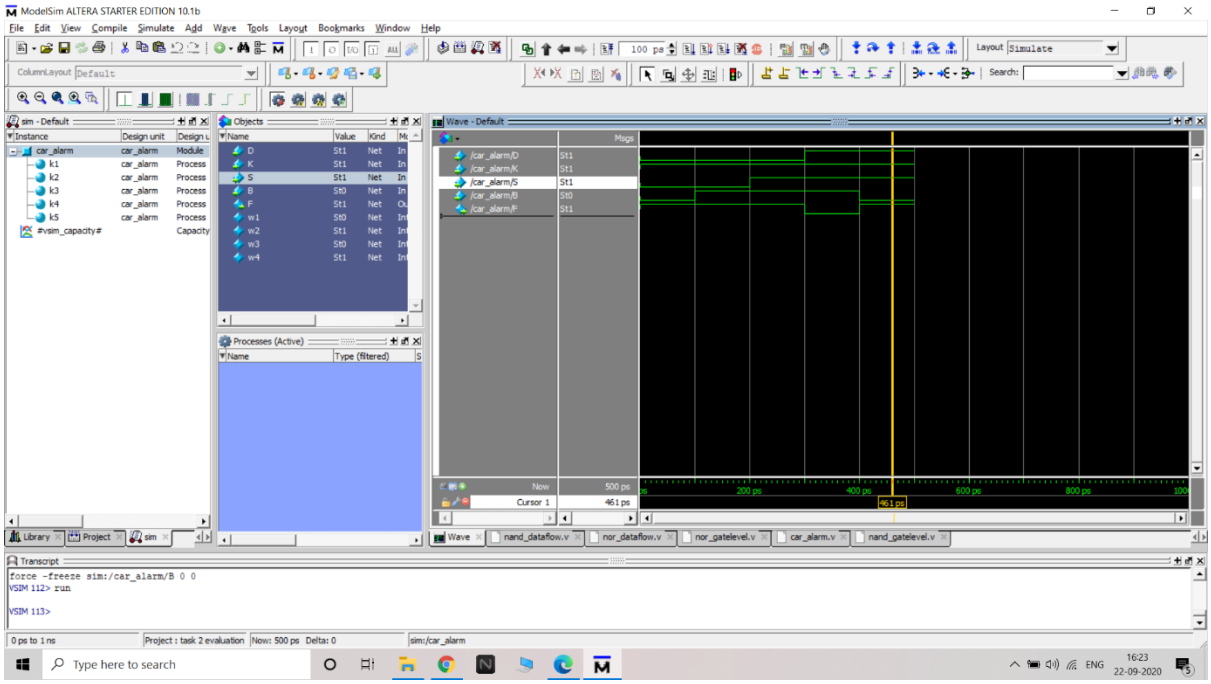
DK \ SB	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

D'K + KSB'

Code →


```
module car_alarm (D,K,S,B,F);
input D,K,S,B;
output F;
wire w1, w2, w3, w4;
not K1 (w1, D);
not K2 (w2, B);
and K3 (w3, w1, K);
and K4 (w4, K, S, w2);
or K5 (F, w4, w3);
endmodule
```


ModelSim ALTERA STARTER EDITION 10.1b - Custom Altera Version
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Project - C:/altera/12.1sp1/modelsim_ase/task 2 evaluation
car_alarm.v Verilog 4 09/22/20 04:21:22 PM
nand_dataflow.v Verilog 1 09/22/20 03:23:52 PM
nand_gatelevel.v Verilog 0 09/22/20 07:15:16 PM
nor_dataflow.v Verilog 2 09/22/20 03:42:36 PM
nor_gatelevel.v Verilog 3 09/22/20 03:50:48 PM
Objects
C:/altera/12.1sp1/modelsim_ase/car_alarm.v - Default
1 module car_alarm(D,K,S,B,F);
2 input D,K,S,B;
3 output F;
4 wire w1,w2,w3,w4;
5 not k1(w1,D);
6 not k2(w2,B);
7 and k3(w3,w1,K);
8 and k4(w4,K,S,w2);
9 or k5(F,w4,w3);
10 endmodule
Transcript
Reading C:/altera/12.1sp1/modelsim_ase/tcl/vsim/pref.tcl
Loading project task 1 evaluation
reading modelsim.ini
Loading project task 2 evaluation
Compile of nand_gatelevel.v was successful.
ModelSim>
Type here to search
ENG
13:42
25-09-2020


ModelSim ALTERA STARTER EDITION 10.1b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
Processes (Active)
Transcript
force -freeze sim:/car_alarm/B 0 0
VSIM 112> run
VSIM 113>
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ENG
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