ECE2002 –Digital logic And Design

Embedded Lab-

Fall semester 2020~2021

Slot: L41+L42

E-Record

Experiment No. : 1

Submitted by

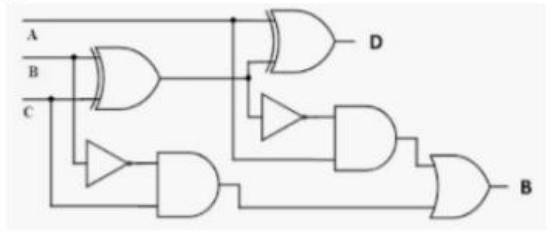
Name of the Student: ARPIT PATAWAT

Reg. no.: 19BEC0358

Q1 -

16	19BEC0358	5. Structural Level	6. Structural Level	7. Gate level	8. Gate level	I.O,I.O,I.O,I.O

5.



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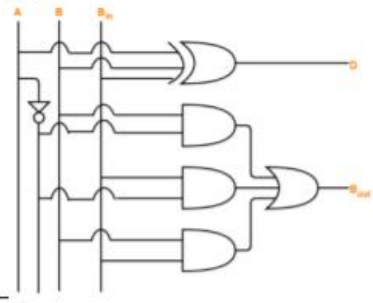

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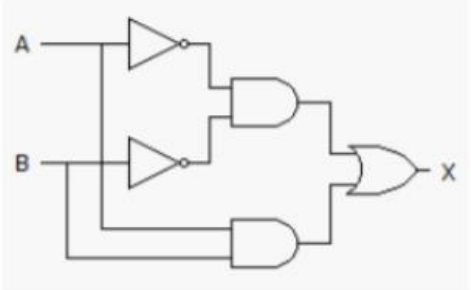

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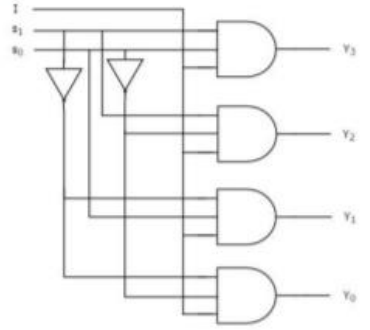

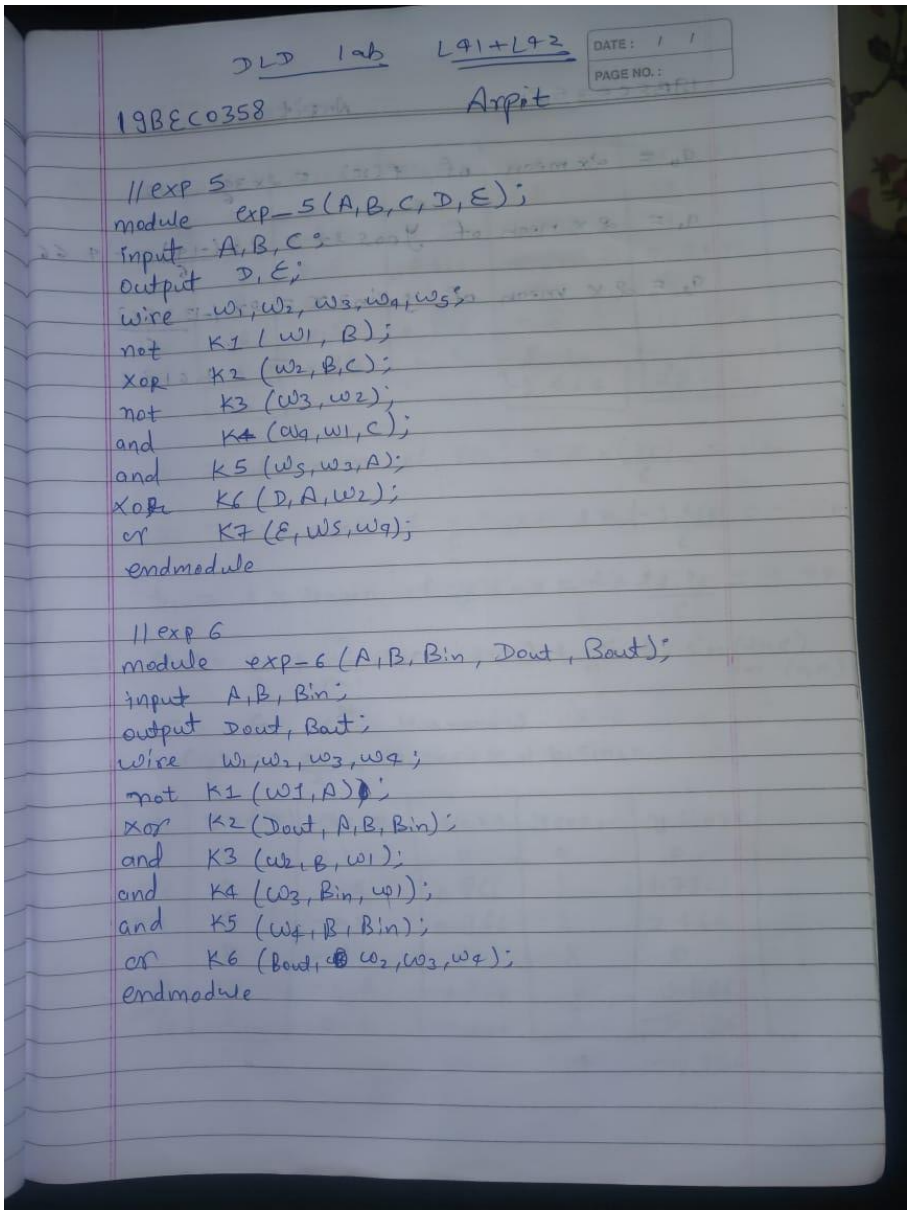

DLD lab L41+L42 DATE: / /
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19BEC0358 Arpit

```
//exp 5
module exp-5(A,B,C,D,E);
input A,B,C;
output D,E;
wire w1,w2,w3,w4,w5;
not K1(w1,B);
xor K2(w2,B,C);
not K3(w3,w2);
and K4(w4,w1,C);
and K5(w5,w3,A);
xor K6(D,A,w2);
or K7(E,w5,w4);
endmodule

//exp 6
module exp-6(A,B,Bin,Dout,Bout);
input A,B,Bin;
output Dout,Bout;
wire w1,w2,w3,w4;
not K1(w1,A);
xor K2(Dout,A,B,Bin);
and K3(w2,B,w1);
and K4(w3,Bin,w1);
and K5(w4,B,Bin);
or K6(Bout,w2,w3,w4);
endmodule
```

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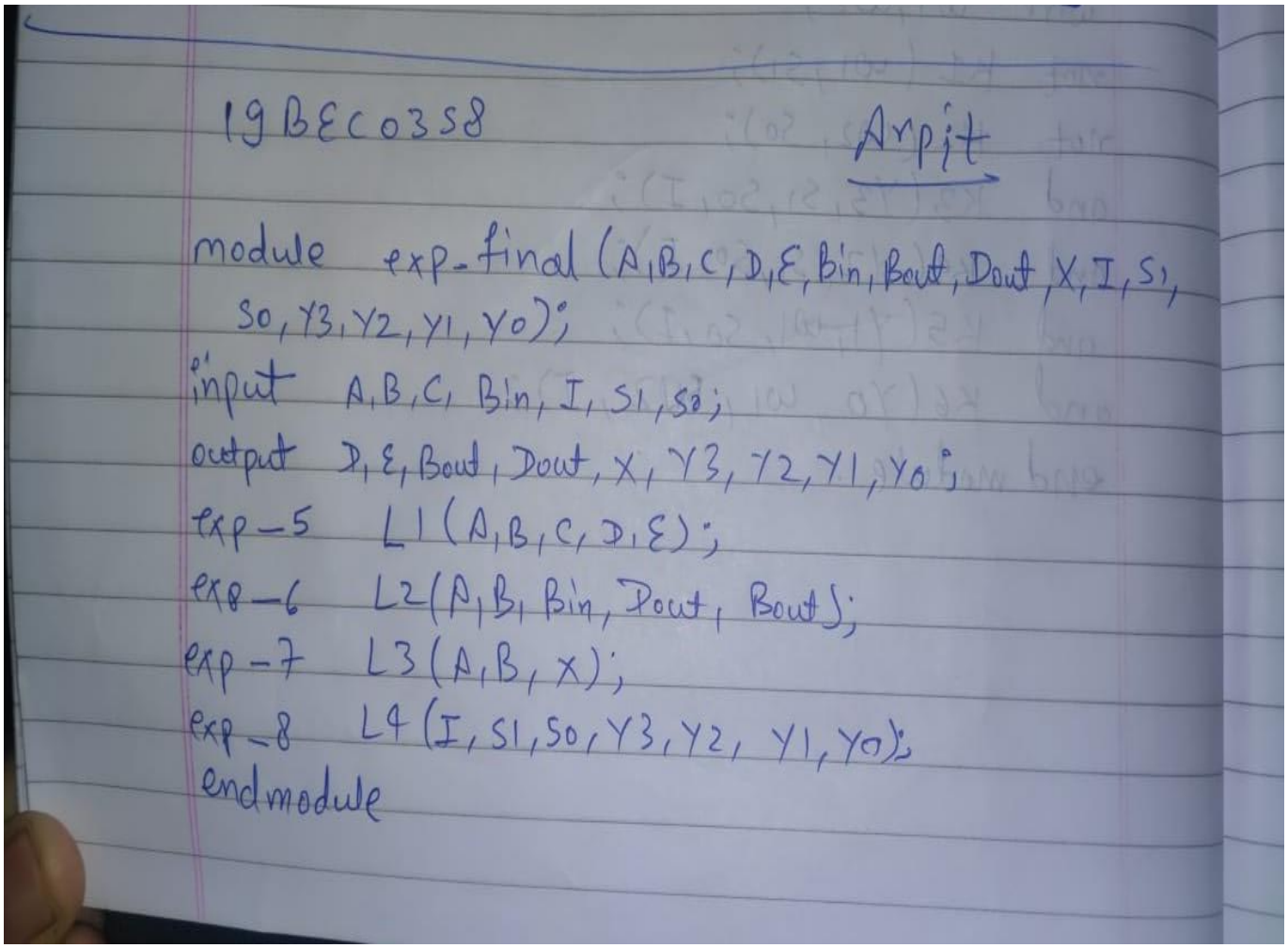
```
// exp 7
module exp-7 (A,B,X);
input A,B;
output X;
wire w1,w2,w3,w4;
not K1 (w1,A);
not K2 (w2,B);
not K3 (w3,w1,w2);
and K4 (w4,A,B);
or K5 (X,w3,w4);
endmodule
```

```
// exp 8
module exp-8 (I,S1,S0,Y3,Y2,Y1,Y0);
Input I, S1, S0;
output Y3, Y2, Y1, Y0;
wire w1,w2;
not K1 (w1,S1);
not K2 (w2,S0);
and K3 (Y3,S1,S0,I);
and K4 (Y2,S1,S0,I);
and K5 (Y1,w1,S0,I);
and K6 (Y0,w1,w2,I);
end module.
```



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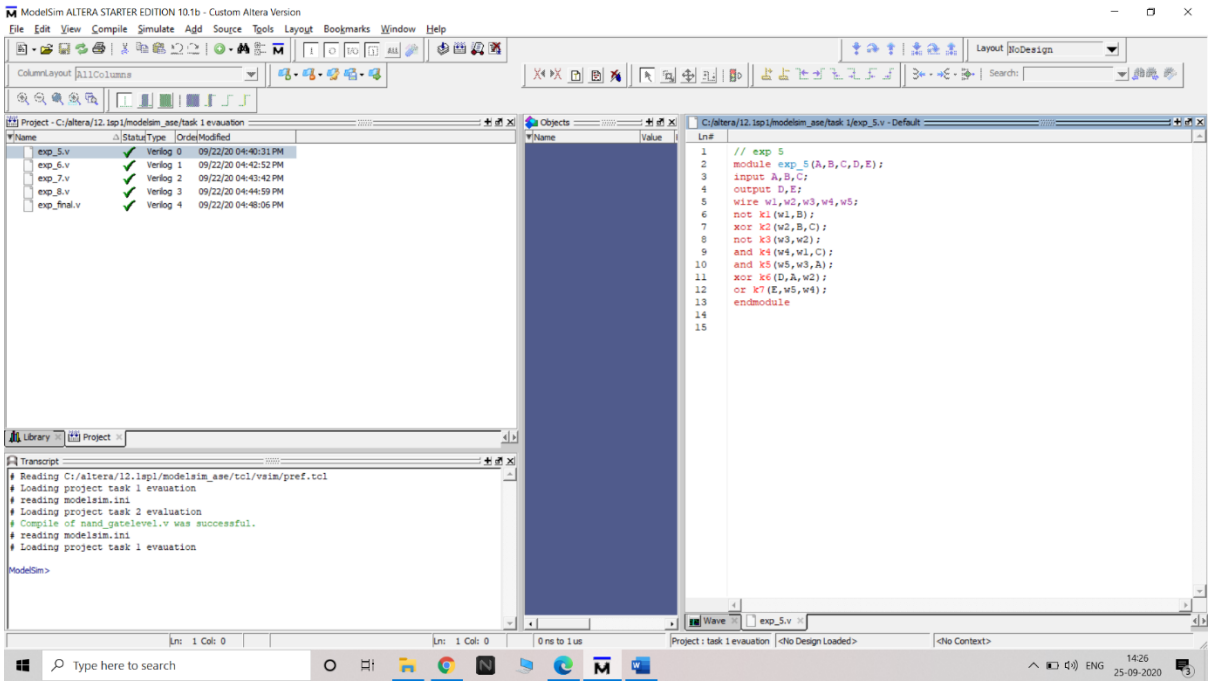
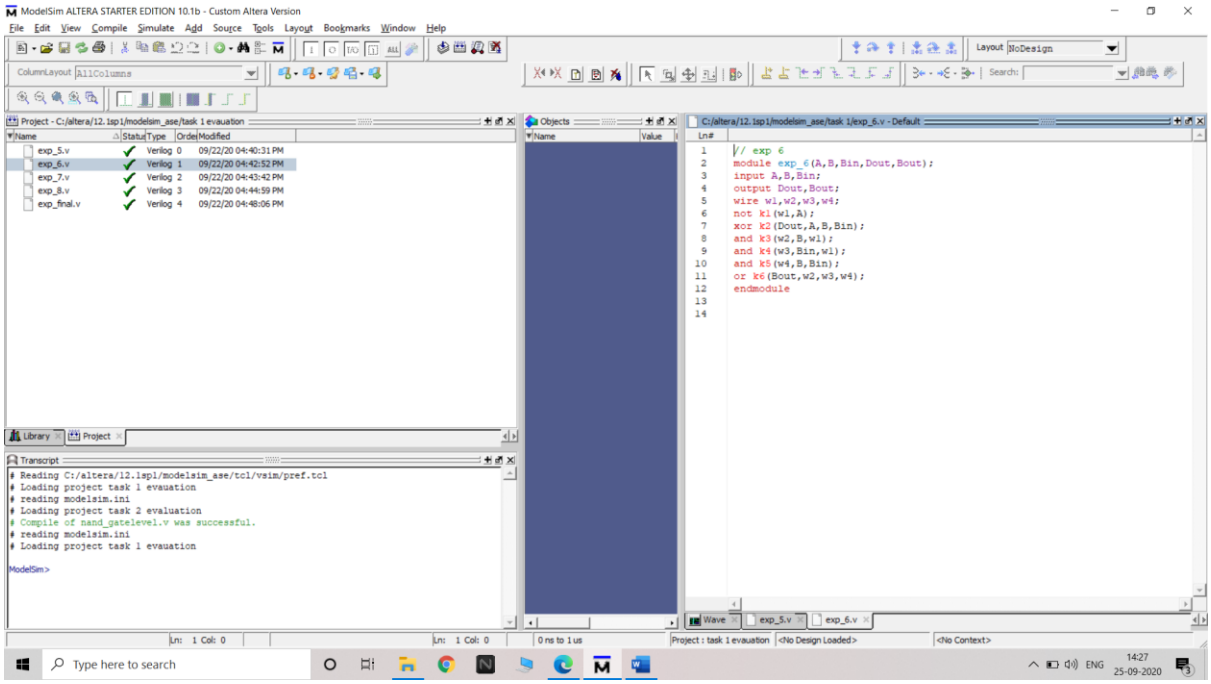
```
module exp_final (A,B,C,D,E,Bin,Bout,Dout,X,I,S1,
  S0,Y3,Y2,Y1,Y0);
input A,B,C, Bin, I, S1,S0;
output D,E,Bout, Dout, X, Y3, Y2,Y1,Y0;
exp_5  L1(A,B,C,D,E);
exp_6  L2(A,B, Bin, Dout, Bout);
exp_7  L3(A,B, X);
exp_8  L4(I, S1,S0,Y3,Y2, Y1,Y0);
endmodule
```

Coding –




ModelSim ALTERA STARTER EDITION 10.1b - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Project - C:/altera/12.1sp1/modelsim_ase/task 1 evauation
exp_5.v Verilog 0 09/22/20 04:40:31 PM
exp_6.v Verilog 1 09/22/20 04:42:52 PM
exp_7.v Verilog 2 09/22/20 04:43:42 PM
exp_8.v Verilog 3 09/22/20 04:44:59 PM
exp_final.v Verilog 4 09/22/20 04:48:06 PM
Transcript
Reading C:/altera/12.1sp1/modelsim_ase/tcl/vsim/pref.tcl
Loading project task 1 evauation
reading modelsim.ini
Loading project task 2 evaluation
Compile of nand_gatelevel.v was successful.
reading modelsim.ini
Loading project task 1 evauation
ModelSim>
C:/altera/12.1sp1/modelsim_ase/task 1/exp_6.v - Default
// exp 6
module exp_6(A,B,Bin,Dout,Bout);
input A,B,Bin;
output Dout,Bout;
wire w1,w2,w3,w4;
not k1(w1,A);
xor k2(Dout,A,B,Bin);
and k3(w2,B,w1);
and k4(w3,Bin,w1);
and k5(w4,B,Bin);
or k6(Bout,w2,w3,w4);
endmodule
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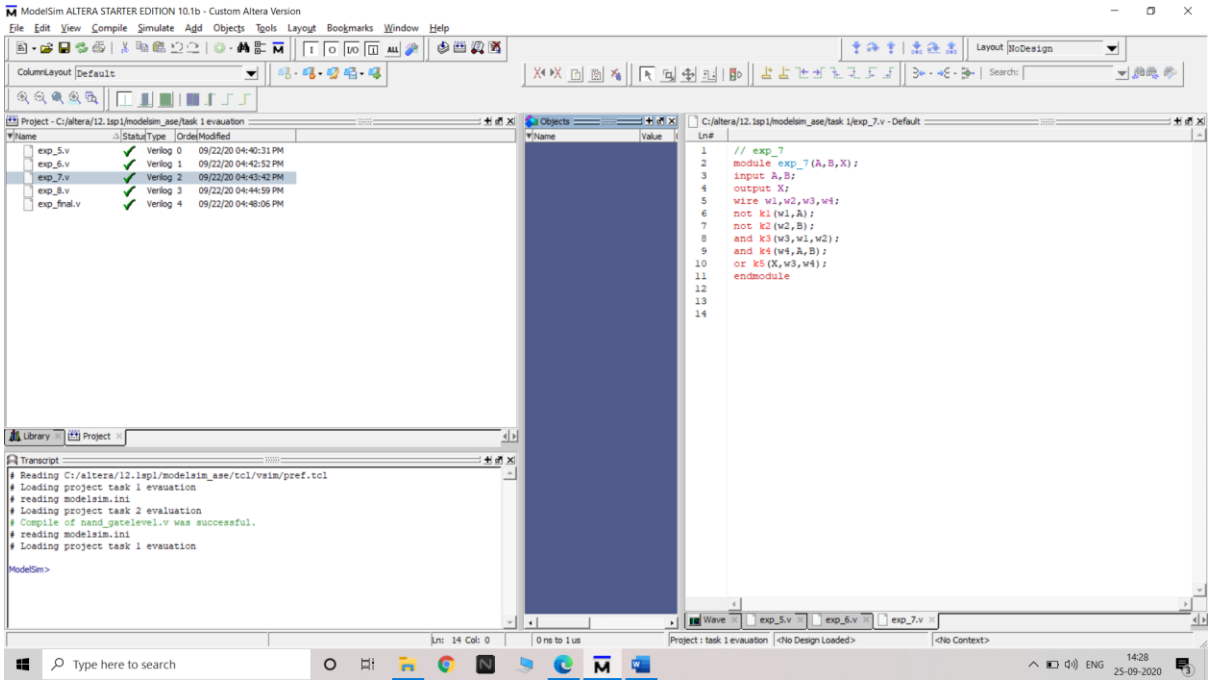
25-09-2020


ModelSim ALTERA STARTER EDITION 10.1b - Custom Altera Version
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reading modelsim.ini
Loading project task 2 evaluation
Compile of nand_gatelevel.v was successful.
reading modelsim.ini
Loading project task 1 evauation
ModelSim>
C:/altera/12.1sp1/modelsim_ase/task 1/exp_7.v - Default
// exp_7
module exp_7(A,B,X);
input A,B;
output X;
wire w1,w2,w3,w4;
not k1(w1,A);
not k2(w2,B);
and k3(w3,w1,w2);
and k4(w4,A,B);
or k5(X,w3,w4);
endmodule
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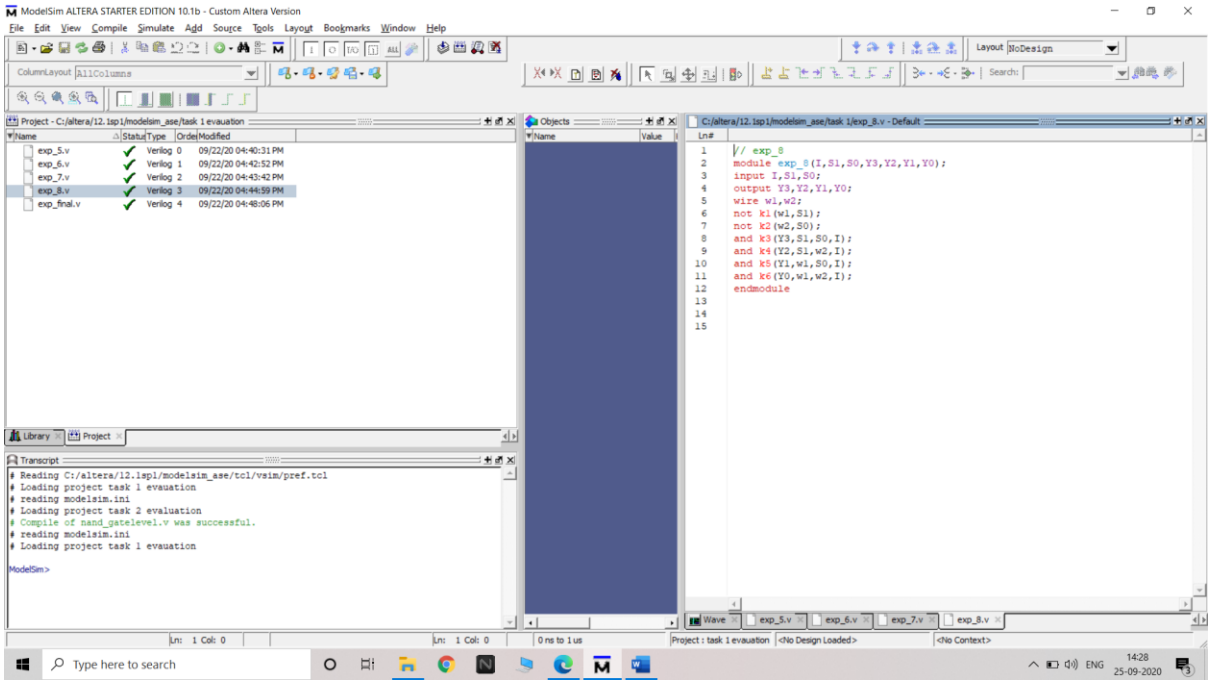
25-09-2020


ModelSim ALTERA STARTER EDITION 10.1b - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Project - C:/altera/12.1sp1/modelsim_ase/task 1 evaluation
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exp_final.v Verilog 4 09/22/20 04:48:06 PM
Transcript
Reading C:/altera/12.1sp1/modelsim_ase/tcl/vsim/pref.tcl
Loading project task 1 evaluation
reading modelsim.ini
Loading project task 2 evaluation
Compile of nand_gatelevel.v was successful.
reading modelsim.ini
Loading project task 1 evaluation
ModelSim>
C:/altera/12.1sp1/modelsim_ase/task 1/exp_8.v - Default
// exp_8
module exp_8(I,S1,S0,Y3,Y2,Y1,Y0);
input I,S1,S0;
output Y3,Y2,Y1,Y0;
wire w1,w2;
not k1(w1,S1);
not k2(w2,S0);
and k3(Y3,S1,S0,I);
and k4(Y2,S1,w2,I);
and k5(Y1,w1,S0,I);
and k6(Y0,w1,w2,I);
endmodule
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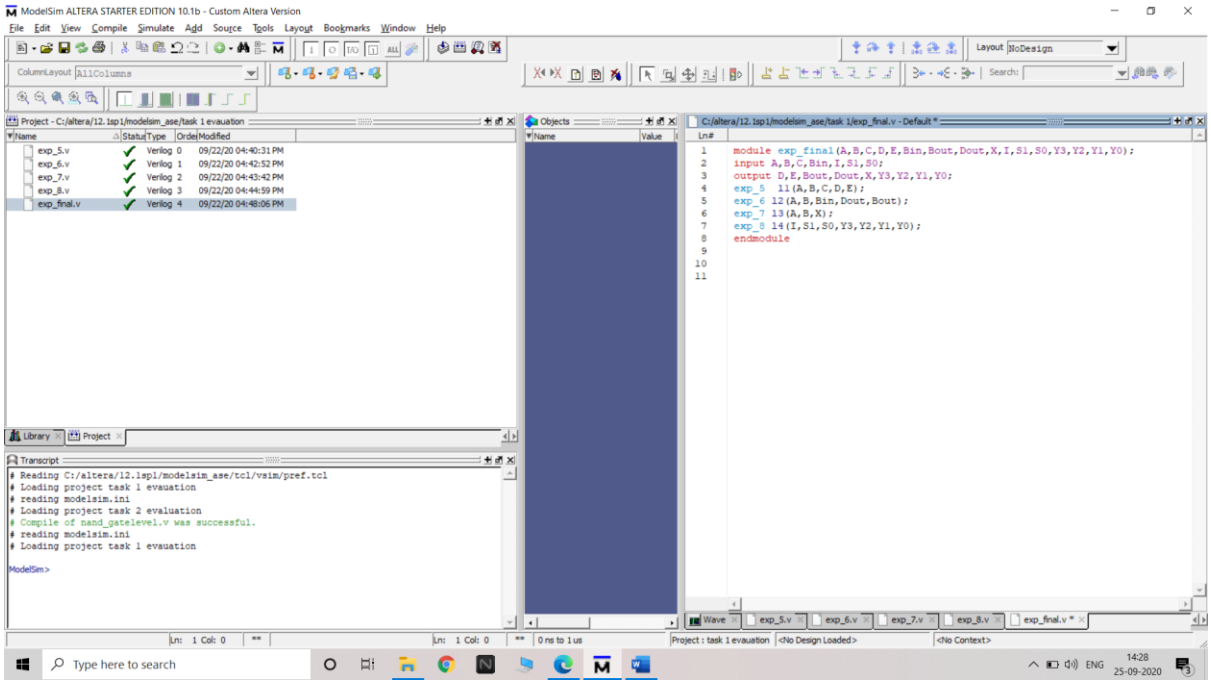
ModelSim ALTERA STARTER EDITION 10.1b - Custom Altera Version
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Project - C:/altera/12.1sp1/modelsim_ase/task 1 evaluation
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exp_7.v Verilog 2 09/22/20 04:43:42 PM
exp_8.v Verilog 3 09/22/20 04:44:59 PM
exp_final.v Verilog 4 09/22/20 04:48:06 PM
Transcript
Reading C:/altera/12.1sp1/modelsim_ase/tcl/vsim/pref.tcl
Loading project task 1 evaluation
reading modelsim.ini
Loading project task 2 evaluation
Compile of nand_gatelevel.v was successful.
reading modelsim.ini
Loading project task 1 evaluation
ModelSim>
C:/altera/12.1sp1/modelsim_ase/task 1/exp_final.v - Default *
module exp_final(A,B,C,D,E,Bin,Bout,Dout,X,I,S1,S0,Y3,Y2,Y1,Y0);
input A,B,C,Bin,I,S1,S0;
output D,E,Bout,Dout,X,Y3,Y2,Y1,Y0;
exp_5 l1(A,B,C,D,E);
exp_6 l2(A,B,Bin,Dout,Bout);
exp_7 l3(A,B,X);
exp_8 l4(I,S1,S0,Y3,Y2,Y1,Y0);
endmodule
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ENG
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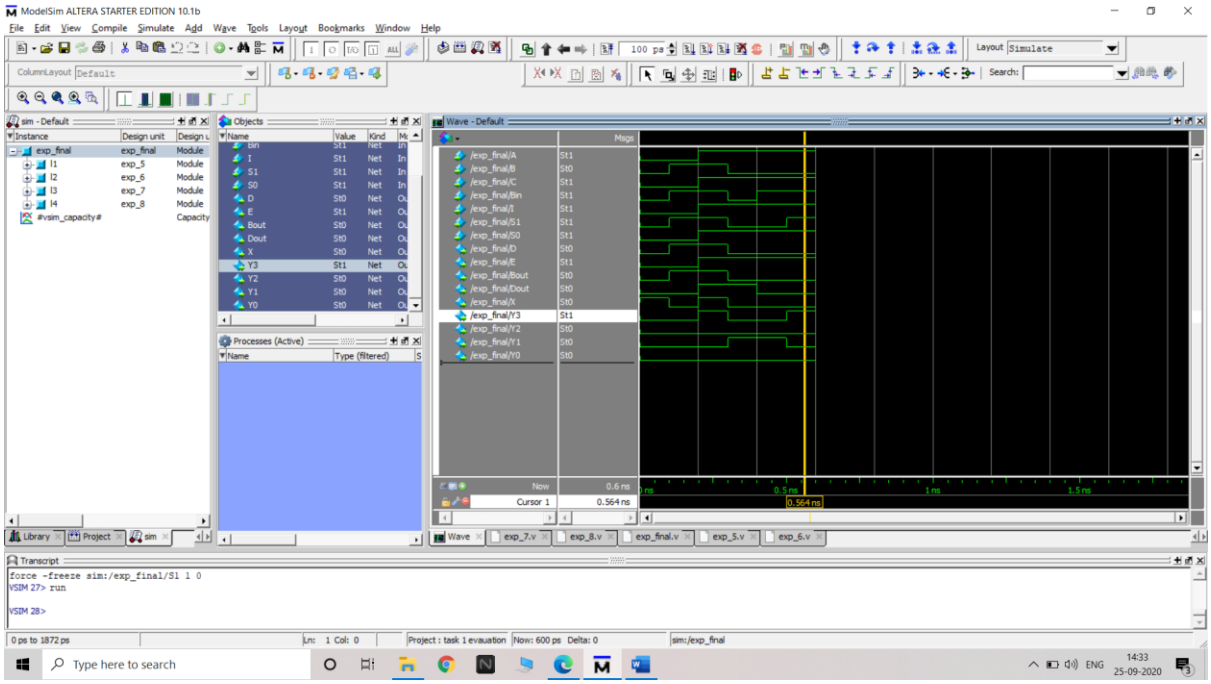
25-09-2020


ModelSim ALTERA STARTER EDITION 10.1b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
Processes (Active)
Transcript
force -freeze sim:/exp_final/S1 1 0
VSIM 27> run
VSIM 28>
Type here to search
ENG
14:33
25-09-2020