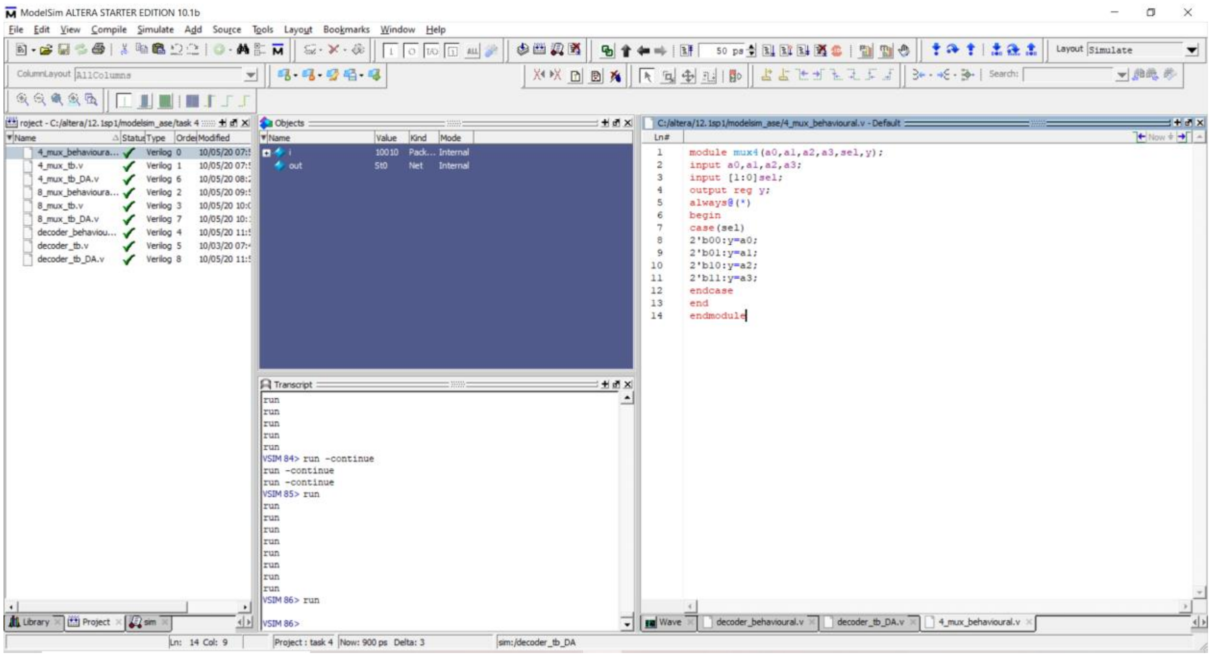
DLD TASK 4

SLOT L41+L42

19BEC0358 ARPIT PATAWAT

a) 4X1 mux behaviour modelling



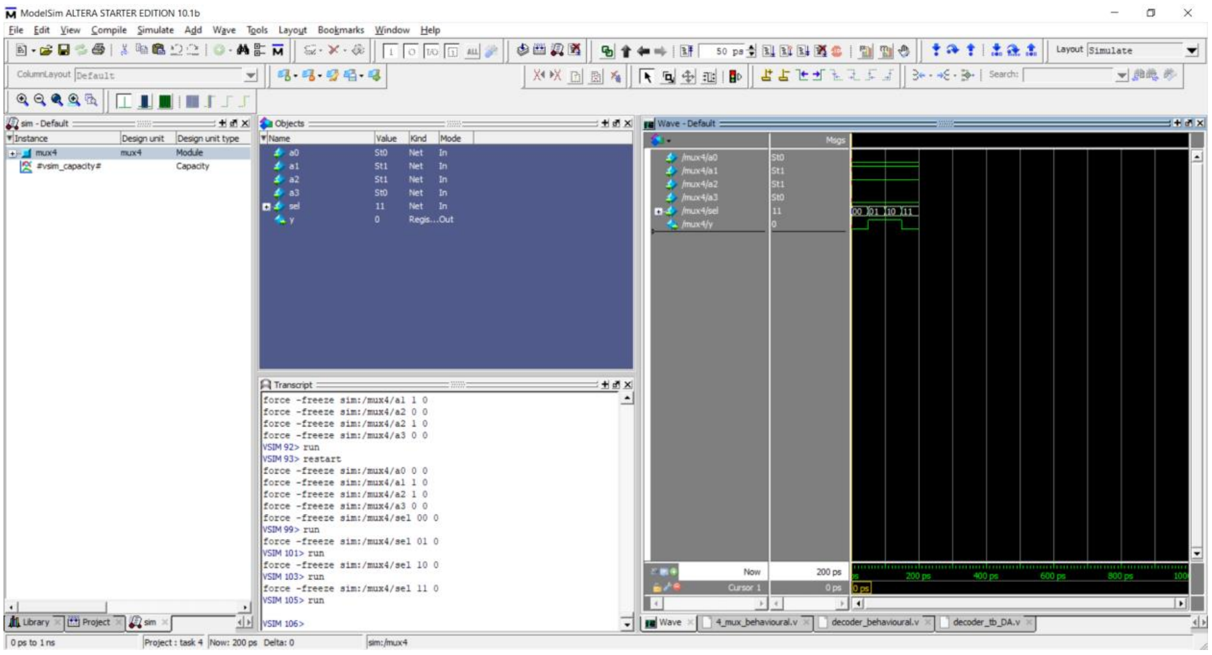
C:/altera/12.1sp1/modelsim_ase/4_mux_behavioural.v - Default

```verilog
module mux4(a0,a1,a2,a3,sel,y);
input a0,a1,a2,a3;
input [1:0]sel;
output reg y;
always@(*)
begin
case(sel)
2'b00:y=a0;
2'b01:y=a1;
2'b10:y=a2;
2'b11:y=a3;
endcase
end
endmodule
```

```
run
run
run
run
run
VSIM 84> run -continue
run -continue
run -continue
VSIM 85> run
run
run
run
run
run
run
run
run
VSIM 86> run

VSIM 86>
```

Project : task 4   Now: 900 ps   Delta: 3   sim:/decoder_tb_DA

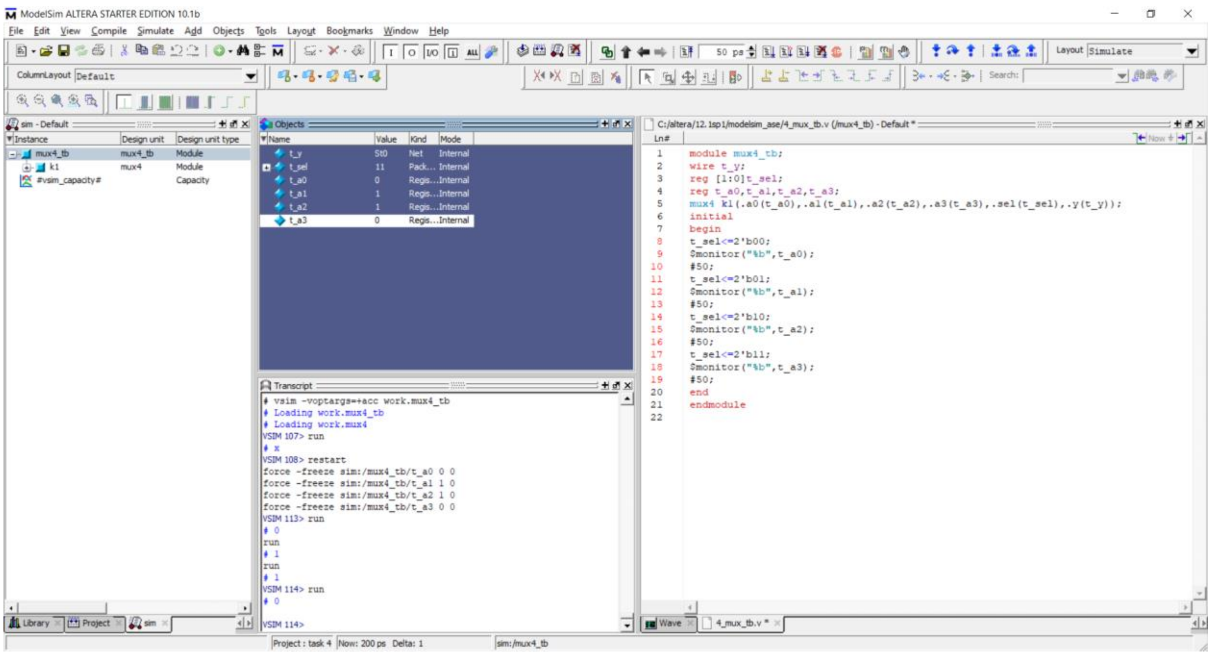


```
force -freeze sim:/mux4/a1 1 0
force -freeze sim:/mux4/a2 0 0
force -freeze sim:/mux4/a2 1 0
force -freeze sim:/mux4/a3 0 0
VSIM 92> run
VSIM 93> restart
force -freeze sim:/mux4/a0 0 0
force -freeze sim:/mux4/a1 1 0
force -freeze sim:/mux4/a2 1 0
force -freeze sim:/mux4/a3 0 0
force -freeze sim:/mux4/sel 00 0
VSIM 99> run
force -freeze sim:/mux4/sel 01 0
VSIM 101> run
force -freeze sim:/mux4/sel 10 0
VSIM 103> run
force -freeze sim:/mux4/sel 11 0
VSIM 105> run

VSIM 106>
```

Project : task 4   Now: 200 ps   Delta: 0   sim:/mux4

4X1 mux test bench



ModelSim ALTERA STARTER EDITION 10.1b

sim - Default

Instance	Design unit	Design unit type
mux4_tb	mux4_tb	Module
k1	mux4	Module
#vsim_capacity#		Capacity

Objects

Name	Value	Kind	Mode
t_y	St0	Net	Internal
t_sel	11	Pack...	Internal
t_a0	0	Regis...	Internal
t_a1	1	Regis...	Internal
t_a2	1	Regis...	Internal
t_a3	0	Regis...	Internal

C:/altera/12.1sp1/modelsim_ase/4_mux_tb.v (/mux4_tb) - Default *

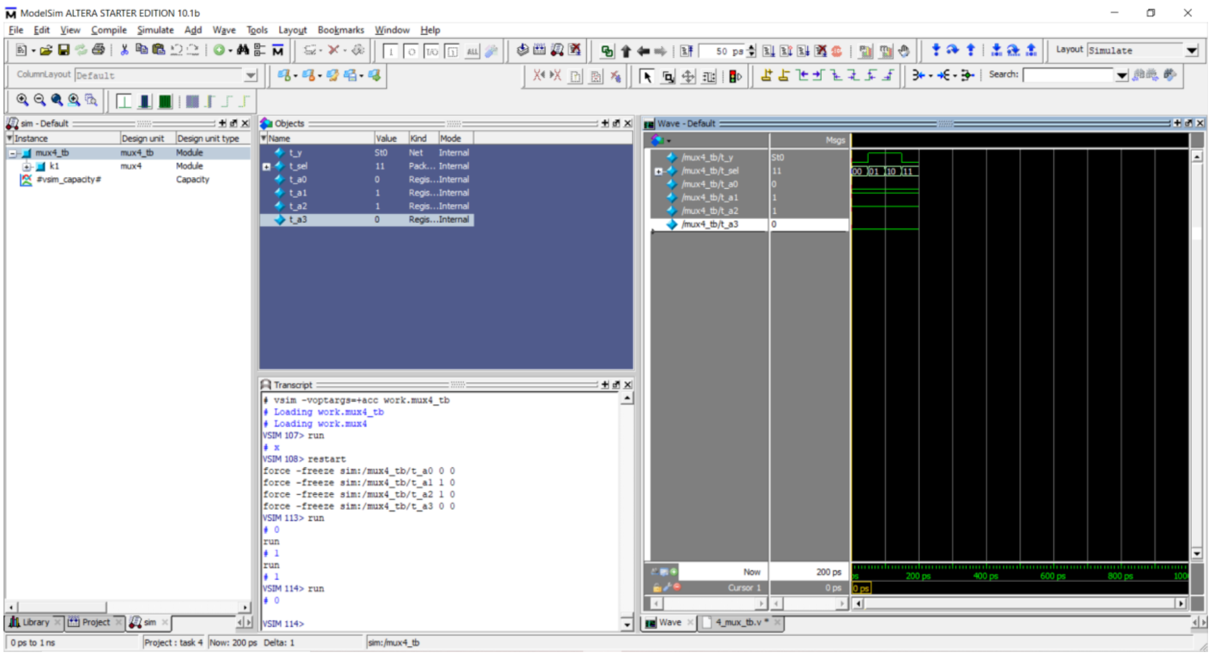
```
module mux4_tb;
wire t_y;
reg [1:0]t_sel;
reg t_a0,t_a1,t_a2,t_a3;
mux4 k1(.a0(t_a0),.a1(t_a1),.a2(t_a2),.a3(t_a3),.sel(t_sel),.y(t_y));
initial
begin
t_sel<=2'b00;
$monitor("%b",t_a0);
#50;
t_sel<=2'b01;
$monitor("%b",t_a1);
#50;
t_sel<=2'b10;
$monitor("%b",t_a2);
#50;
t_sel<=2'b11;
$monitor("%b",t_a3);
#50;
end
endmodule
```

Transcript

```
# vsim -voptargs=+acc work.mux4_tb
# Loading work.mux4_tb
# Loading work.mux4
VSIM 107> run
# x
VSIM 108> restart
force -freeze sim:/mux4_tb/t_a0 0 0
force -freeze sim:/mux4_tb/t_a1 1 0
force -freeze sim:/mux4_tb/t_a2 1 0
force -freeze sim:/mux4_tb/t_a3 0 0
VSIM 113> run
# 0
run
# 1
run
# 1
VSIM 114> run
# 0

VSIM 114>
```

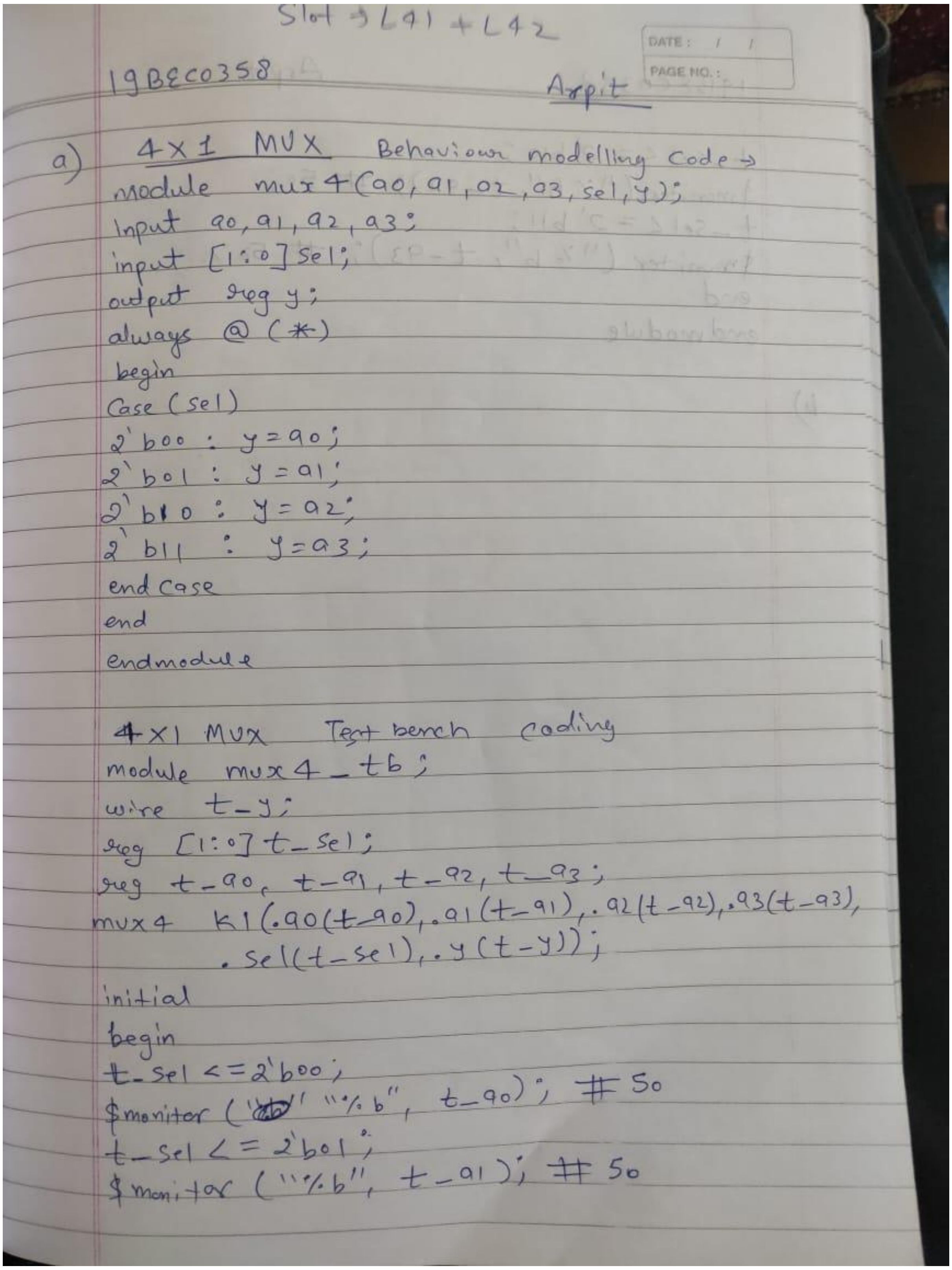
Project : task 4 Now: 200 ps Delta: 1 sim:/mux4_tb



Name	Value	Kind	Mode
t_y	St0	Net	Internal
t_sel	11	Pack...	Internal
t_a0	0	Regis...	Internal
t_a1	1	Regis...	Internal
t_a2	1	Regis...	Internal
t_a3	0	Regis...	Internal

```
# vsim -voptargs=+acc work.mux4_tb
# Loading work.mux4_tb
# Loading work.mux4
VSIM 107> run
# x
VSIM 108> restart
force -freeze sim:/mux4_tb/t_a0 0 0
force -freeze sim:/mux4_tb/t_a1 1 0
force -freeze sim:/mux4_tb/t_a2 1 0
force -freeze sim:/mux4_tb/t_a3 0 0
VSIM 113> run
# 0
run
# 1
run
# 1
VSIM 114> run
# 0

VSIM 114>
```



Slot → L41 + L42

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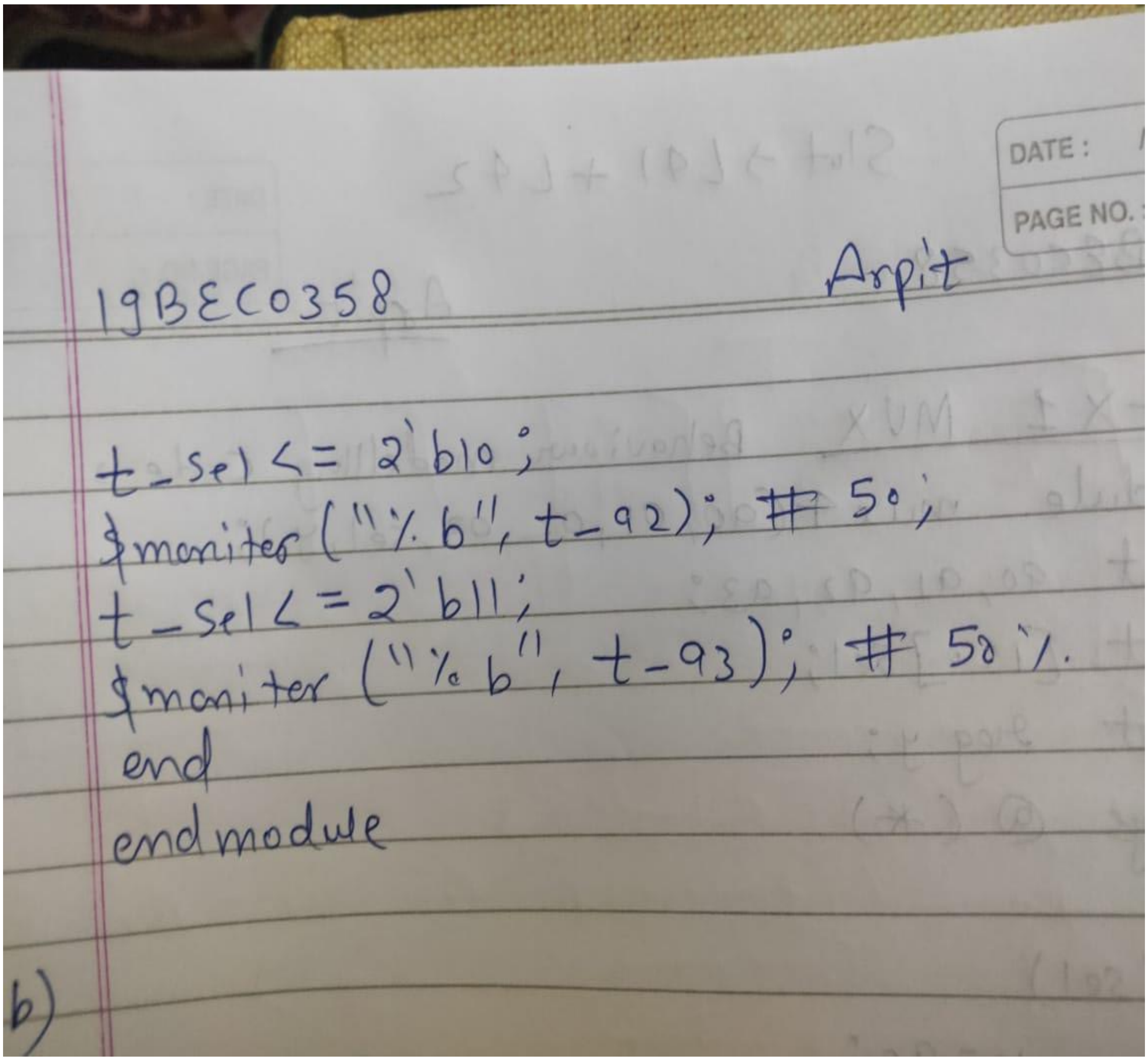
a) 4x1 MUX Behaviour modelling Code →

```
module mux4(a0,a1,a2,a3,sel,y);
input a0,a1,a2,a3;
input [1:0] sel;
output reg y;
always @ (*)
begin
case (sel)
2'b00 : y=a0;
2'b01 : y=a1;
2'b10 : y=a2;
2'b11 : y=a3;
end case
end
endmodule
```

4x1 MUX Test bench coding

```
module mux4_tb;
wire t_y;
reg [1:0] t_sel;
reg t_a0, t_a1, t_a2, t_a3;
mux4 k1(.a0(t_a0),.a1(t_a1),.a2(t_a2),.a3(t_a3),
        .sel(t_sel),.y(t_y));
initial
begin
t_sel <= 2'b00;
$monitor ( "%b", t_a0); #50
t_sel <= 2'b01;
$monitor ("%b", t_a1); #50
```



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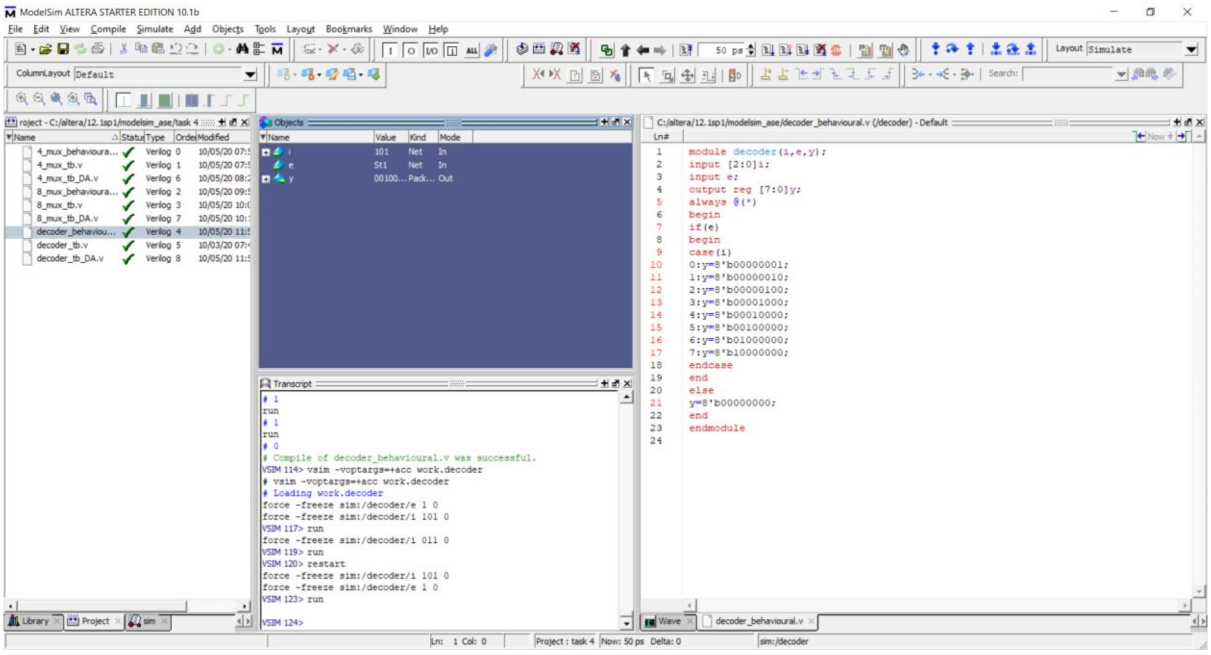
```
t_sel <= 2'b10;
$moniter ("%b", t_q2); #50;
t_sel <= 2'b11;
$moniter ("%b", t_q3); #50;
end
endmodule
```

b)

b) decoder behaviour modelling



C:/altera/12.1sp1/modelsim_ase/decoder_behavioural.v (/decoder) - Default

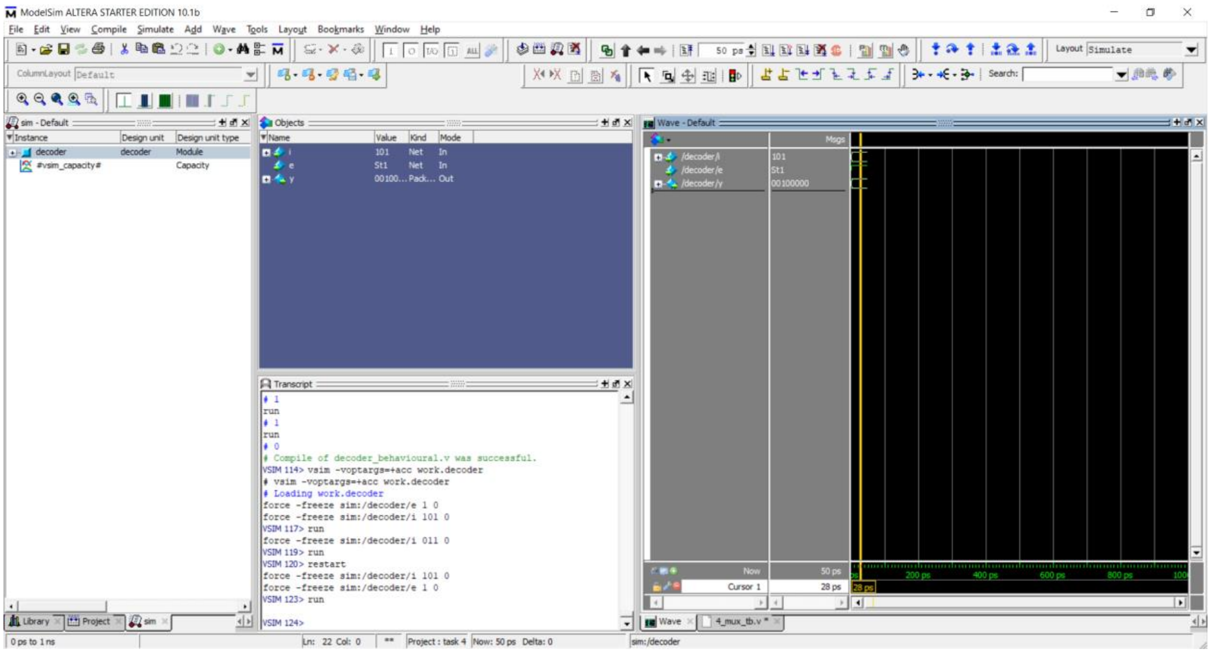
```verilog
module decoder(i,e,y);
input [2:0]i;
input e;
output reg [7:0]y;
always @(*)
begin
if(e)
begin
case(i)
0:y=8'b00000001;
1:y=8'b00000010;
2:y=8'b00000100;
3:y=8'b00001000;
4:y=8'b00010000;
5:y=8'b00100000;
6:y=8'b01000000;
7:y=8'b10000000;
endcase
end
else
y=8'b00000000;
end
endmodule
```

```
Name  Value   Kind     Mode
i     101     Net      In
e     St1     Net      In
y     00100... Pack... Out
```

Transcript

```
# 1
run
# 1
run
# 0
# Compile of decoder_behavioural.v was successful.
VSIM 114> vsim -voptargs=+acc work.decoder
# vsim -voptargs=+acc work.decoder
# Loading work.decoder
force -freeze sim:/decoder/e 1 0
force -freeze sim:/decoder/i 101 0
VSIM 117> run
force -freeze sim:/decoder/i 011 0
VSIM 119> run
VSIM 120> restart
force -freeze sim:/decoder/i 101 0
force -freeze sim:/decoder/e 1 0
VSIM 123> run

VSIM 124>
```

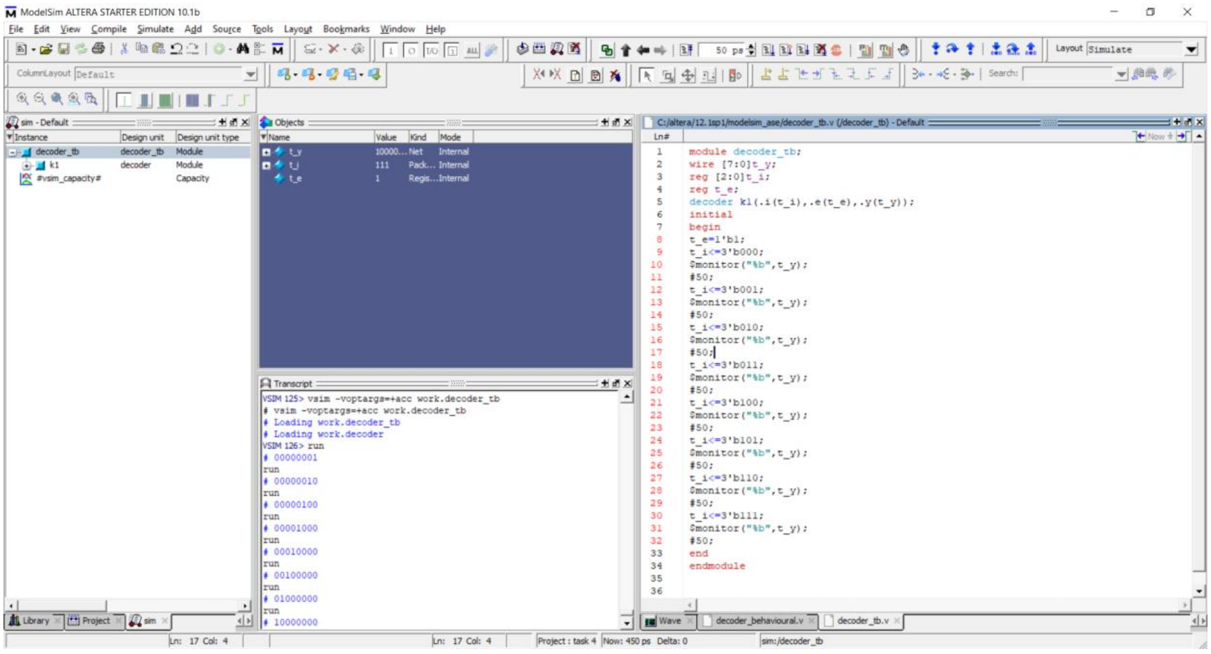


```
/decoder/i   101
/decoder/e   St1
/decoder/y   00100000
Now          50 ps
Cursor 1     28 ps
```

```
# 1
run
# 1
run
# 0
# Compile of decoder_behavioural.v was successful.
VSIM 114> vsim -voptargs=+acc work.decoder
# vsim -voptargs=+acc work.decoder
# Loading work.decoder
force -freeze sim:/decoder/e 1 0
force -freeze sim:/decoder/i 101 0
VSIM 117> run
force -freeze sim:/decoder/i 011 0
VSIM 119> run
VSIM 120> restart
force -freeze sim:/decoder/i 101 0
force -freeze sim:/decoder/e 1 0
VSIM 123> run

VSIM 124>
```

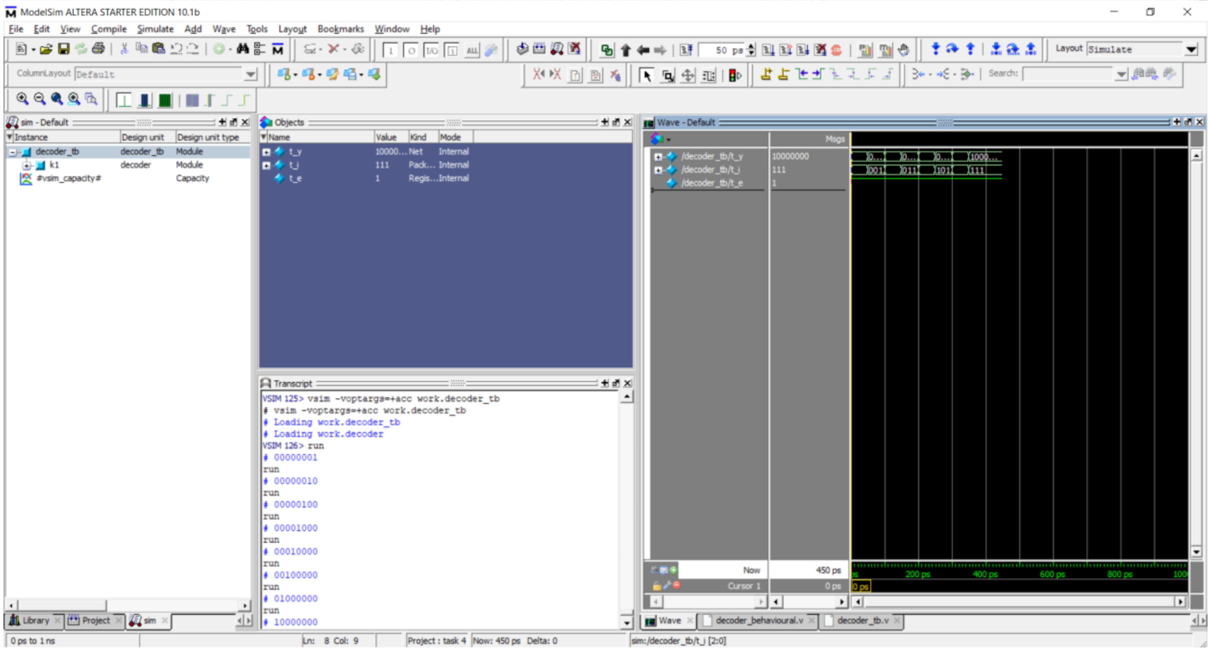
Decoder test bench



C:/altera/12.1sp1/modelsim_ase/decoder_tb.v (/decoder_tb) - Default

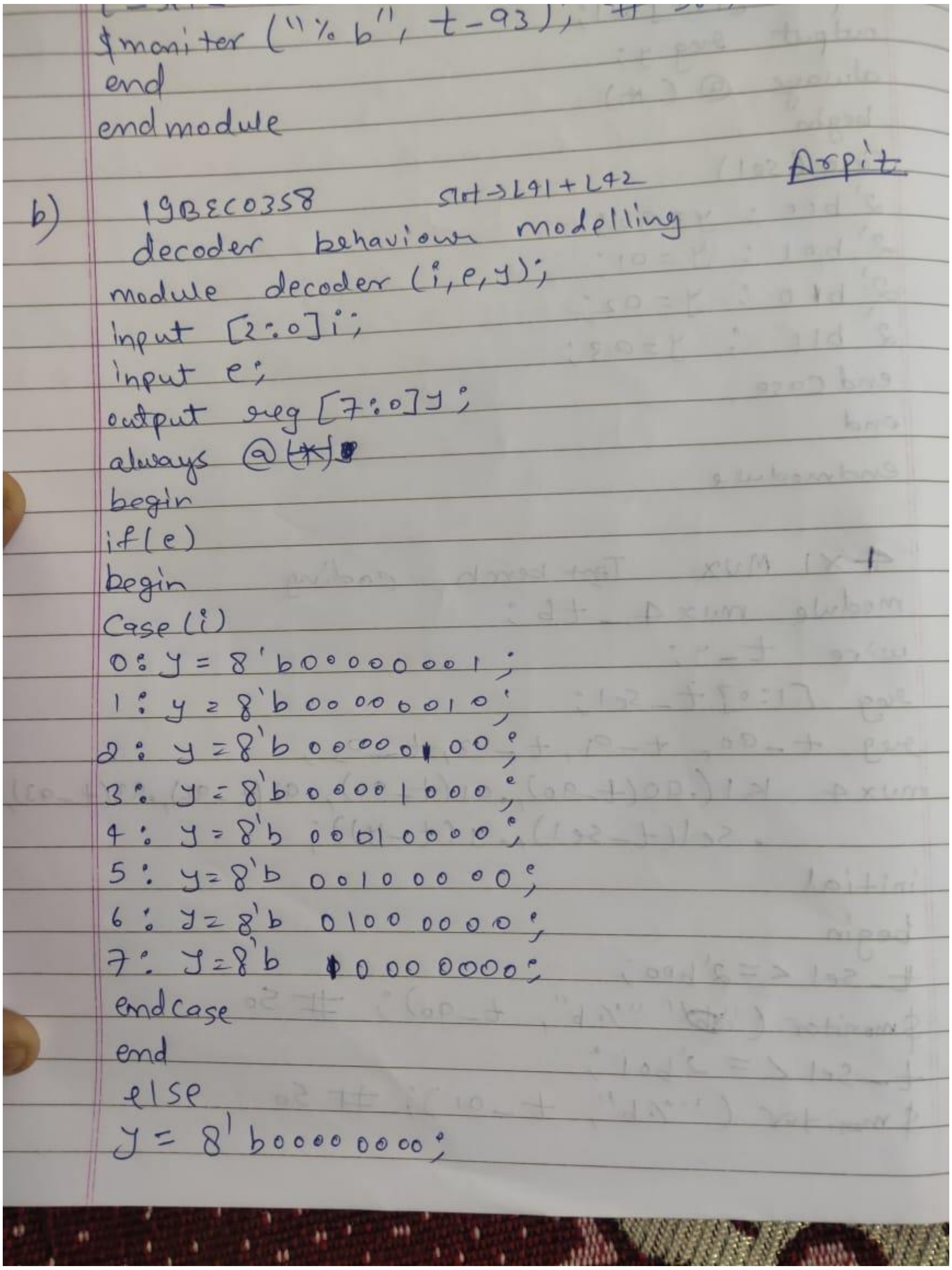
```
module decoder_tb;
wire [7:0]t_y;
reg [2:0]t_i;
reg t_e;
decoder k1(.i(t_i),.e(t_e),.y(t_y));
initial
begin
t_e=1'b1;
t_i<=3'b000;
$monitor("%b",t_y);
#50;
t_i<=3'b001;
$monitor("%b",t_y);
#50;
t_i<=3'b010;
$monitor("%b",t_y);
#50;
t_i<=3'b011;
$monitor("%b",t_y);
#50;
t_i<=3'b100;
$monitor("%b",t_y);
#50;
t_i<=3'b101;
$monitor("%b",t_y);
#50;
t_i<=3'b110;
$monitor("%b",t_y);
#50;
t_i<=3'b111;
$monitor("%b",t_y);
#50;
end
endmodule
```

```
VSIM 125> vsim -voptargs=+acc work.decoder_tb
# vsim -voptargs=+acc work.decoder_tb
# Loading work.decoder_tb
# Loading work.decoder
VSIM 126> run
# 00000001
run
# 00000010
run
# 00000100
run
# 00001000
run
# 00010000
run
# 00100000
run
# 01000000
run
# 10000000
```



```
VSIM 125> vsim -voptargs=+acc work.decoder_tb
# vsim -voptargs=+acc work.decoder_tb
# Loading work.decoder_tb
# Loading work.decoder
VSIM 126> run
# 00000001
run
# 00000010
run
# 00000100
run
# 00001000
run
# 00010000
run
# 00100000
run
# 01000000
run
# 10000000
```

```
/decoder_tb/t_y   10000000
/decoder_tb/t_i   111
/decoder_tb/t_e   1
Now 450 ps
Cursor 1 0 ps
```



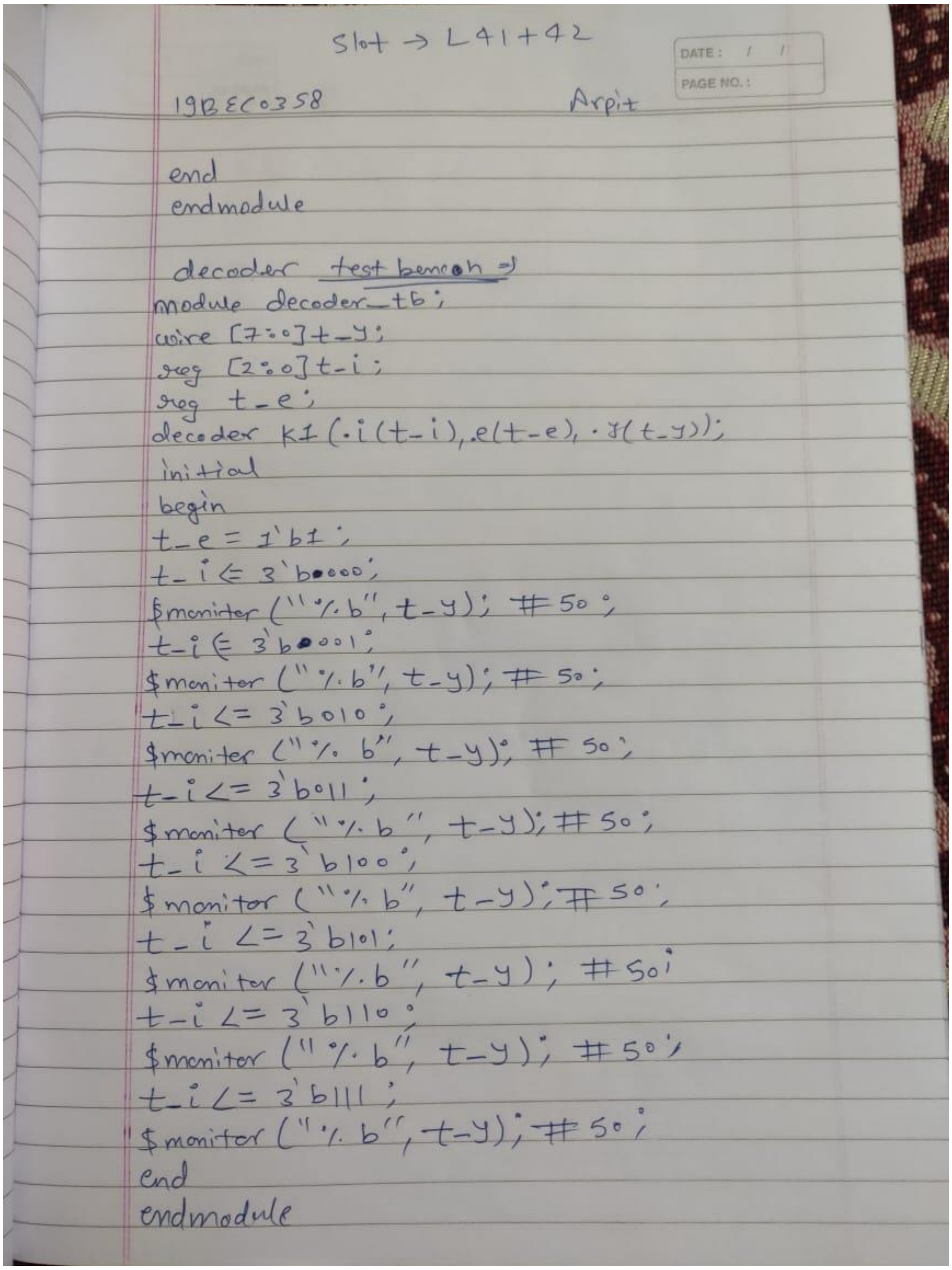
```
$moniter ("%b", t-93);
end
endmodule
```

Arpit

b) 19BEC0358   slot→L41+L42

decoder behaviour modelling

```
module decoder (i,e,y);
input [2:0]i;
input e;
output reg [7:0]y;
always @(*)
begin
if(e)
begin
case(i)
0: y = 8'b00000001;
1: y = 8'b00000010;
2: y = 8'b00000100;
3: y = 8'b00001000;
4: y = 8'b00010000;
5: y = 8'b00100000;
6: y = 8'b01000000;
7: y = 8'b10000000;
endcase
end
else
y = 8'b00000000;
```



Slot → L41+42

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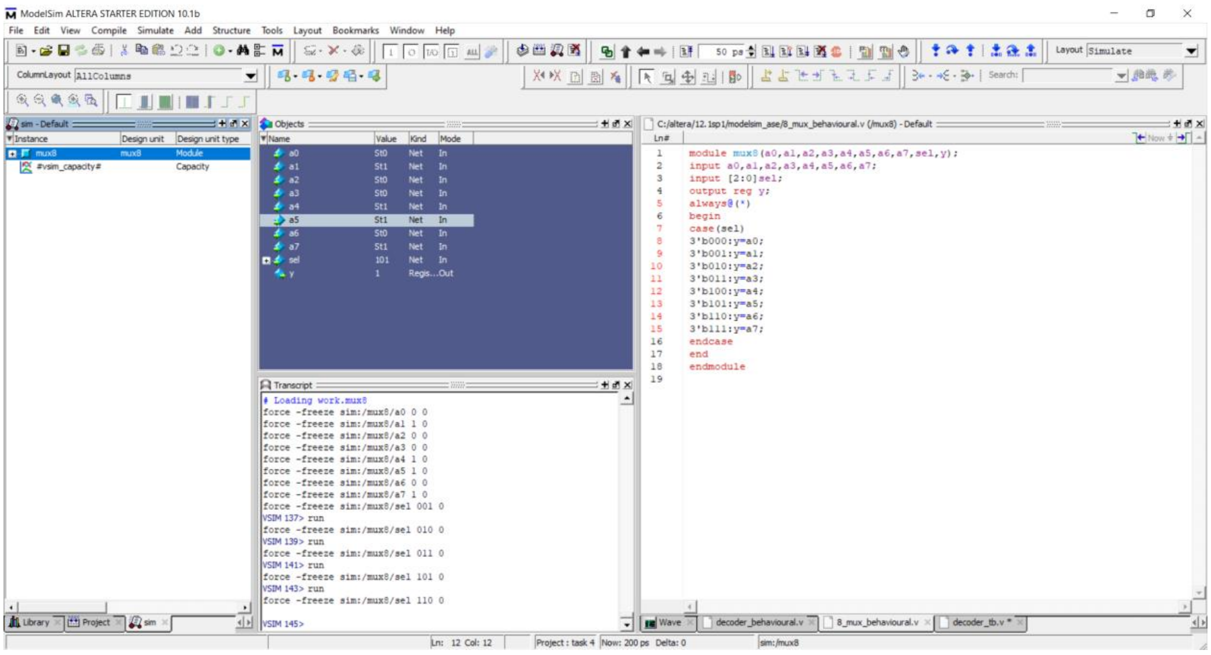
```
end
endmodule

decoder test bench =>
module decoder_tb;
wire [7:0]t_y;
reg [2:0]t_i;
reg t_e;
decoder k1 (.i(t_i),.e(t_e), .y(t_y));
initial
begin
t_e = 1'b1;
t_i <= 3'b000;
$moniter ("%b",t_y); #50;
t_i <= 3'b001;
$moniter ("%b",t_y); #50;
t_i <= 3'b010;
$moniter ("%b", t_y); #50;
t_i <= 3'b011;
$moniter ("%b", t_y); #50;
t_i <= 3'b100;
$monitor ("%b", t_y); #50;
t_i <= 3'b101;
$moniter ("%b", t_y); #50;
t_i <= 3'b110;
$monitor ("%b", t_y); #50;
t_i <= 3'b111;
$monitor ("%b", t_y); #50;
end
endmodule
```

c) 8X1 mux behavioural modelling



C:/altera/12.1sp1/modelsim_ase/8_mux_behavioural.v (/mux8) - Default

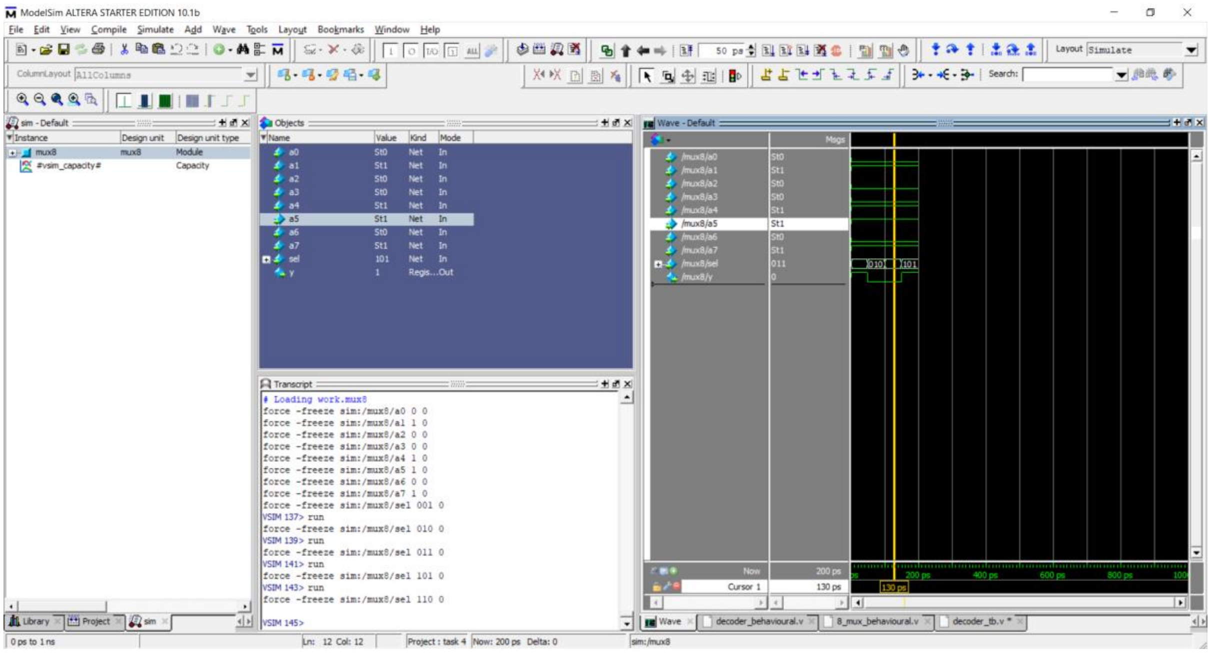
```
module mux8(a0,a1,a2,a3,a4,a5,a6,a7,sel,y);
input a0,a1,a2,a3,a4,a5,a6,a7;
input [2:0]sel;
output reg y;
always@(*)
begin
case(sel)
3'b000:y=a0;
3'b001:y=a1;
3'b010:y=a2;
3'b011:y=a3;
3'b100:y=a4;
3'b101:y=a5;
3'b110:y=a6;
3'b111:y=a7;
endcase
end
endmodule
```

Name	Value	Kind	Mode
a0	St0	Net	In
a1	St1	Net	In
a2	St0	Net	In
a3	St0	Net	In
a4	St1	Net	In
a5	St1	Net	In
a6	St0	Net	In
a7	St1	Net	In
sel	101	Net	In
y	1	Regis...Out	

```
# Loading work.mux8
force -freeze sim:/mux8/a0 0 0
force -freeze sim:/mux8/a1 1 0
force -freeze sim:/mux8/a2 0 0
force -freeze sim:/mux8/a3 0 0
force -freeze sim:/mux8/a4 1 0
force -freeze sim:/mux8/a5 1 0
force -freeze sim:/mux8/a6 0 0
force -freeze sim:/mux8/a7 1 0
force -freeze sim:/mux8/sel 001 0
VSIM 137> run
force -freeze sim:/mux8/sel 010 0
VSIM 139> run
force -freeze sim:/mux8/sel 011 0
VSIM 141> run
force -freeze sim:/mux8/sel 101 0
VSIM 143> run
force -freeze sim:/mux8/sel 110 0

VSIM 145>
```

Ln: 12 Col: 12 | Project : task 4 | Now: 200 ps Delta: 0 | sim:/mux8



Wave - Default

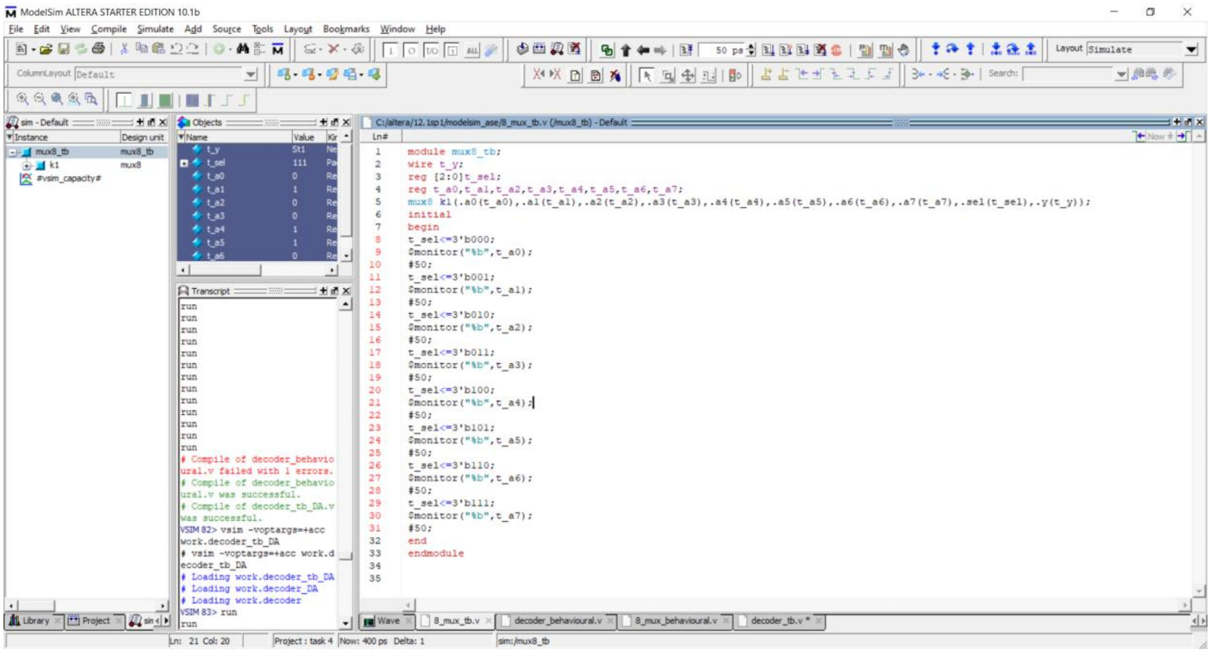
```
/mux8/a0    St0
/mux8/a1    St1
/mux8/a2    St0
/mux8/a3    St0
/mux8/a4    St1
/mux8/a5    St1
/mux8/a6    St0
/mux8/a7    St1
/mux8/sel   011
/mux8/y     0
Now         200 ps
Cursor 1    130 ps
```

```
# Loading work.mux8
force -freeze sim:/mux8/a0 0 0
force -freeze sim:/mux8/a1 1 0
force -freeze sim:/mux8/a2 0 0
force -freeze sim:/mux8/a3 0 0
force -freeze sim:/mux8/a4 1 0
force -freeze sim:/mux8/a5 1 0
force -freeze sim:/mux8/a6 0 0
force -freeze sim:/mux8/a7 1 0
force -freeze sim:/mux8/sel 001 0
VSIM 137> run
force -freeze sim:/mux8/sel 010 0
VSIM 139> run
force -freeze sim:/mux8/sel 011 0
VSIM 141> run
force -freeze sim:/mux8/sel 101 0
VSIM 143> run
force -freeze sim:/mux8/sel 110 0

VSIM 145>
```

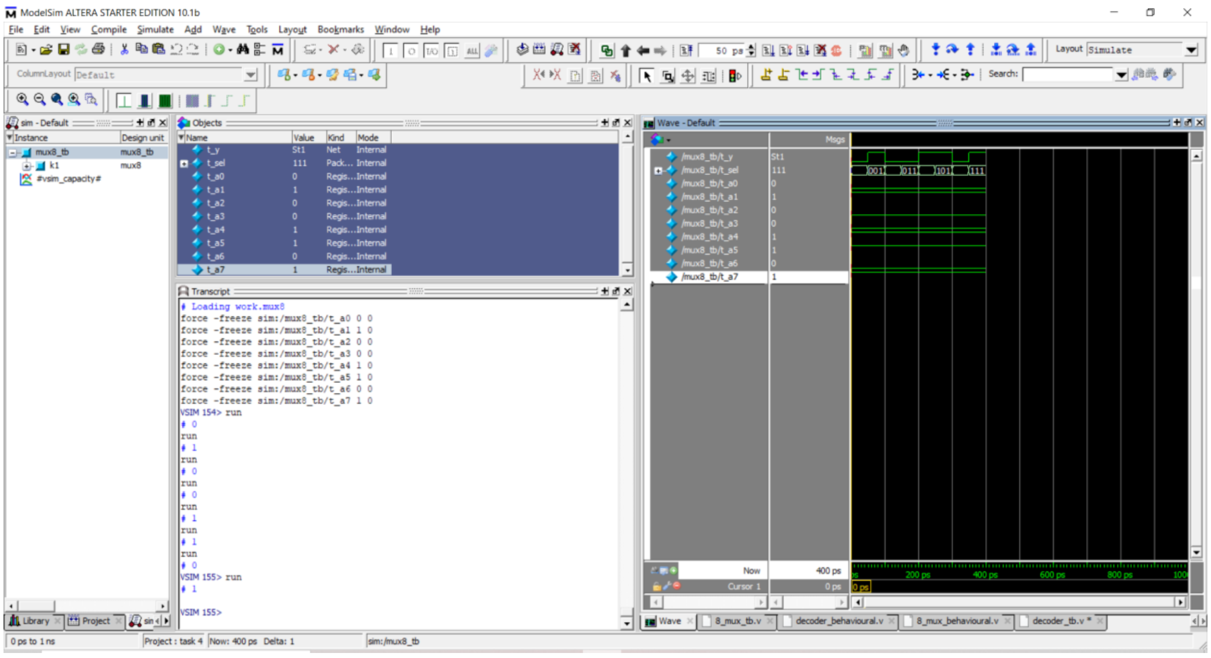
0 ps to 1 ns | Ln: 12 Col: 12 | Project : task 4 | Now: 200 ps Delta: 0 | sim:/mux8

8X1 mux test bench



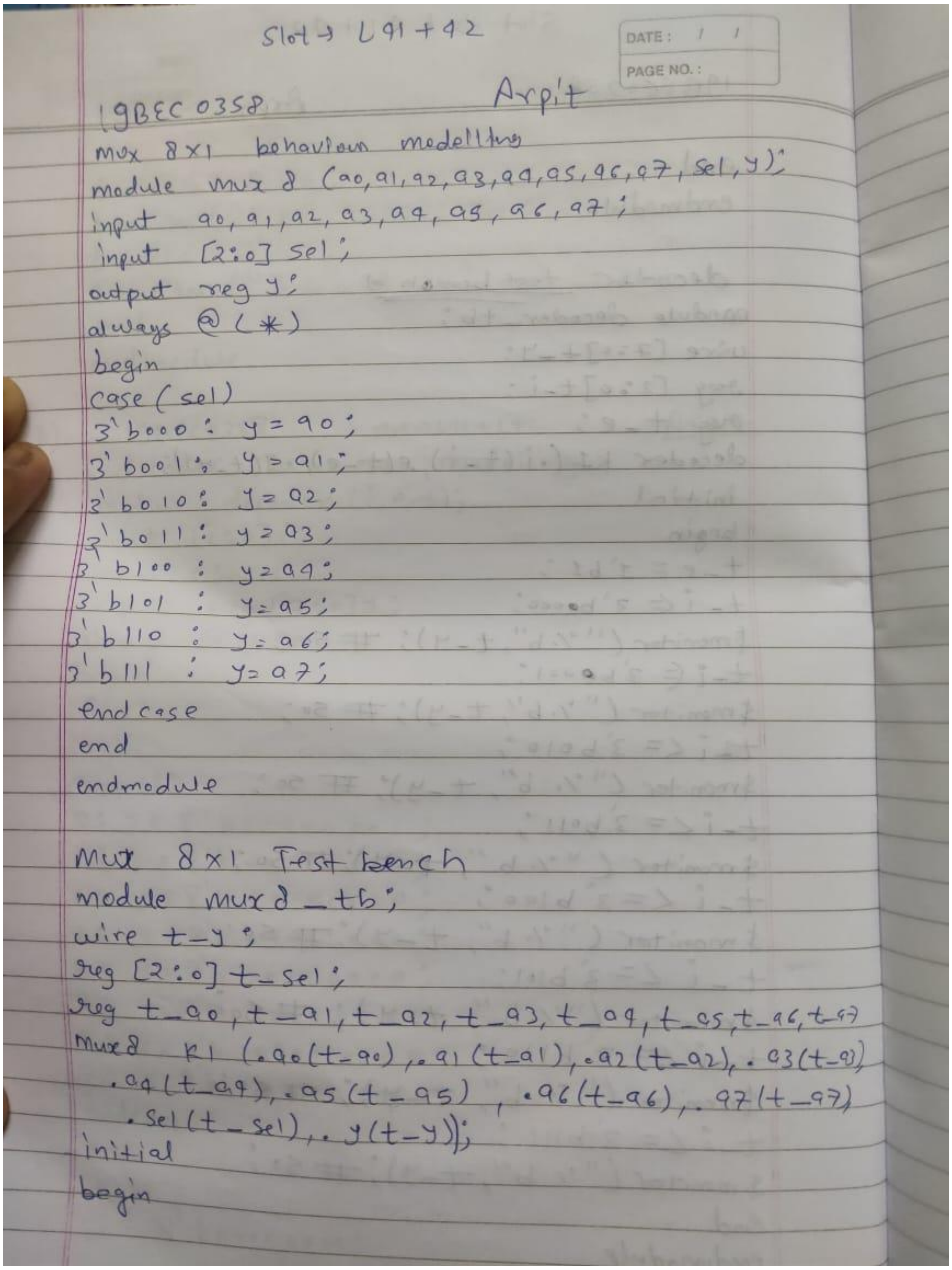
```
module mux8_tb;
wire t_y;
reg [2:0]t_sel;
reg t_a0,t_a1,t_a2,t_a3,t_a4,t_a5,t_a6,t_a7;
mux8 k1(.a0(t_a0),.a1(t_a1),.a2(t_a2),.a3(t_a3),.a4(t_a4),.a5(t_a5),.a6(t_a6),.a7(t_a7),.sel(t_sel),.y(t_y));
initial
begin
t_sel<=3'b000;
$monitor("%b",t_a0);
#50;
t_sel<=3'b001;
$monitor("%b",t_a1);
#50;
t_sel<=3'b010;
$monitor("%b",t_a2);
#50;
t_sel<=3'b011;
$monitor("%b",t_a3);
#50;
t_sel<=3'b100;
$monitor("%b",t_a4);
#50;
t_sel<=3'b101;
$monitor("%b",t_a5);
#50;
t_sel<=3'b110;
$monitor("%b",t_a6);
#50;
t_sel<=3'b111;
$monitor("%b",t_a7);
#50;
end
endmodule
```

```
run
run
run
run
run
run
run
run
run
run
run
run
run
# Compile of decoder_behavioural.v failed with 1 errors.
# Compile of decoder_behavioural.v was successful.
# Compile of decoder_tb_DA.v was successful.
VSIM 82> vsim -voptargs=+acc work.decoder_tb_DA
# vsim -voptargs=+acc work.decoder_tb_DA
# Loading work.decoder_tb_DA
# Loading work.decoder_DA
# Loading work.decoder
VSIM 83> run
run
```



```
# Loading work.mux8
force -freeze sim:/mux8_tb/t_a0 0 0
force -freeze sim:/mux8_tb/t_a1 1 0
force -freeze sim:/mux8_tb/t_a2 0 0
force -freeze sim:/mux8_tb/t_a3 0 0
force -freeze sim:/mux8_tb/t_a4 1 0
force -freeze sim:/mux8_tb/t_a5 1 0
force -freeze sim:/mux8_tb/t_a6 0 0
force -freeze sim:/mux8_tb/t_a7 1 0
VSIM 154> run
# 0
run
# 1
run
# 0
run
# 0
run
# 1
run
# 1
run
# 0
VSIM 155> run
# 1

VSIM 155>
```



Slot → L41 + 42

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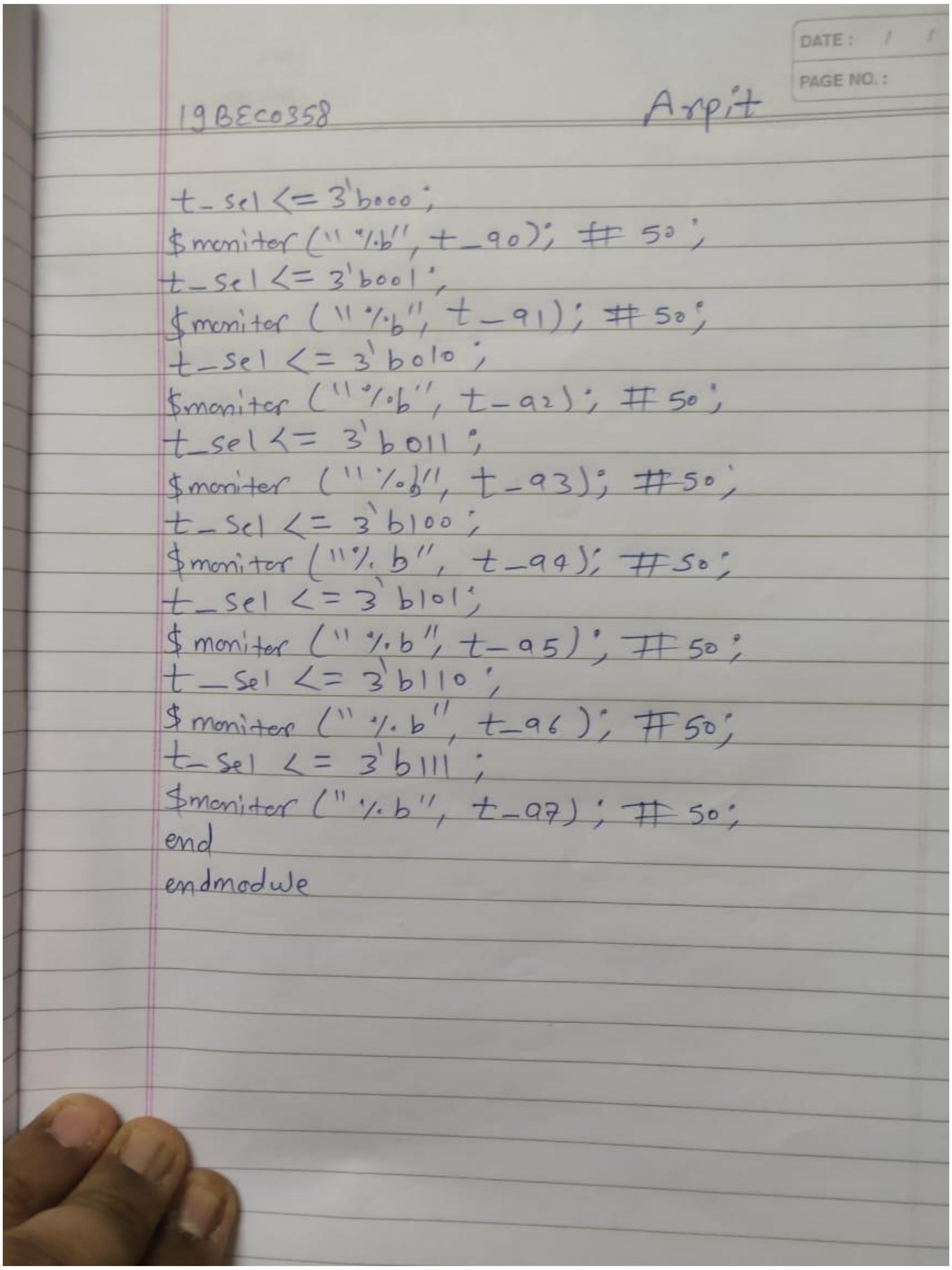
mux 8x1 behaviour modelling

```
module mux 8 (a0,a1,a2,a3,a4,a5,a6,a7, sel,y);
input a0, a1, a2, a3, a4, a5, a6, a7;
input [2:0] sel;
output reg y;
always @ (*)
begin
case (sel)
3'b000 : y = a0;
3'b001 : y = a1;
3'b010 : y = a2;
3'b011 : y = a3;
3'b100 : y = a4;
3'b101 : y = a5;
3'b110 : y = a6;
3'b111 : y = a7;
end case
end
endmodule
```

Mux 8x1 Test bench

```
module mux8_tb;
wire t_y;
reg [2:0] t_sel;
reg t_a0, t_a1, t_a2, t_a3, t_a4, t_a5, t_a6, t_a7
mux8 k1 (.a0(t_a0), .a1(t_a1), .a2(t_a2), . a3(t_a3)
  .a4(t_a4), .a5(t_a5) , .a6(t_a6), . a7(t_a7)
  .sel(t_sel), . y(t_y));
initial
begin
```



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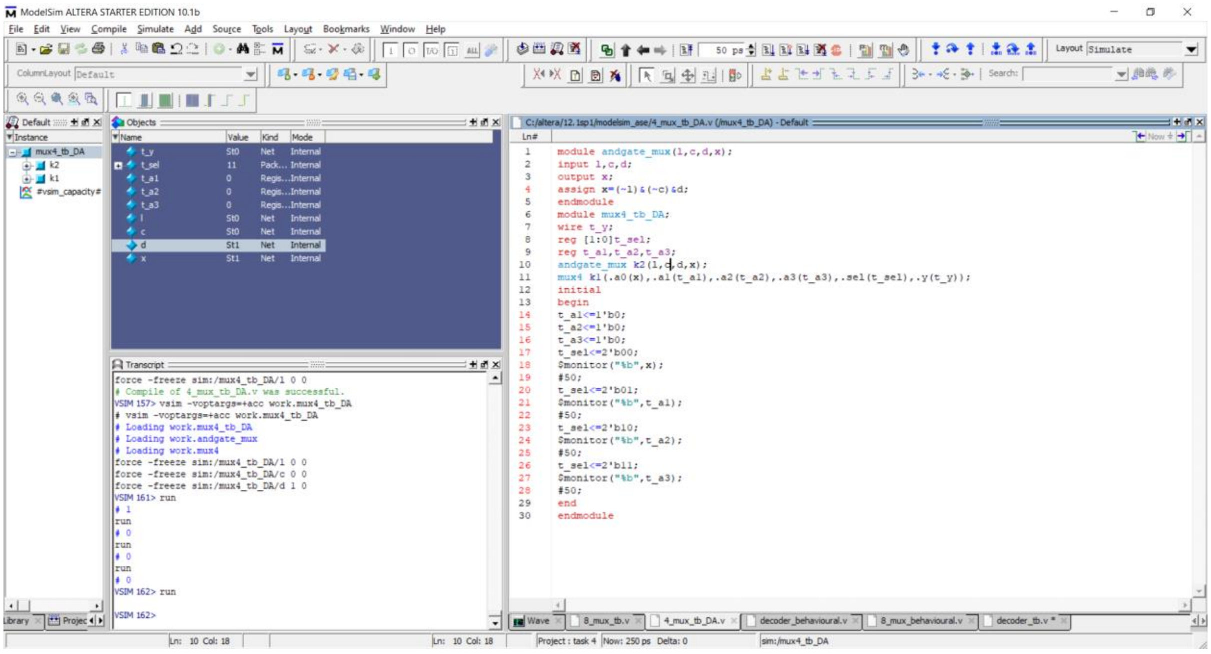
```
t_sel <= 3'b000;
$moniter ("%b", t_a0); #50;
t_sel <= 3'b001;
$moniter ("%b", t_a1); #50;
t_sel <= 3'b010;
$moniter ("%b", t_a2); #50;
t_sel <= 3'b011;
$moniter ("%b", t_a3); #50;
t_sel <= 3'b100;
$moniter ("%b", t_a4); #50;
t_sel <= 3'b101;
$moniter ("%b", t_a5); #50;
t_sel <= 3'b110;
$moniter ("%b", t_a6); #50;
t_sel <= 3'b111;
$moniter ("%b", t_a7); #50;
end
endmodule
```

d) 4X1 mux



ModelSim ALTERA STARTER EDITION 10.1b

C:/altera/12.1sp1/modelsim_ase/4_mux_tb_DA.v (/mux4_tb_DA) - Default

```verilog
module andgate_mux(l,c,d,x);
input l,c,d;
output x;
assign x=(~l)&(~c)&d;
endmodule
module mux4_tb_DA;
wire t_y;
reg [1:0]t_sel;
reg t_a1,t_a2,t_a3;
andgate_mux k2(l,c,d,x);
mux4 k1(.a0(x),.a1(t_a1),.a2(t_a2),.a3(t_a3),.sel(t_sel),.y(t_y));
initial
begin
t_a1<=1'b0;
t_a2<=1'b0;
t_a3<=1'b0;
t_sel<=2'b00;
$monitor("%b",x);
#50;
t_sel<=2'b01;
$monitor("%b",t_a1);
#50;
t_sel<=2'b10;
$monitor("%b",t_a2);
#50;
t_sel<=2'b11;
$monitor("%b",t_a3);
#50;
end
endmodule
```

Objects

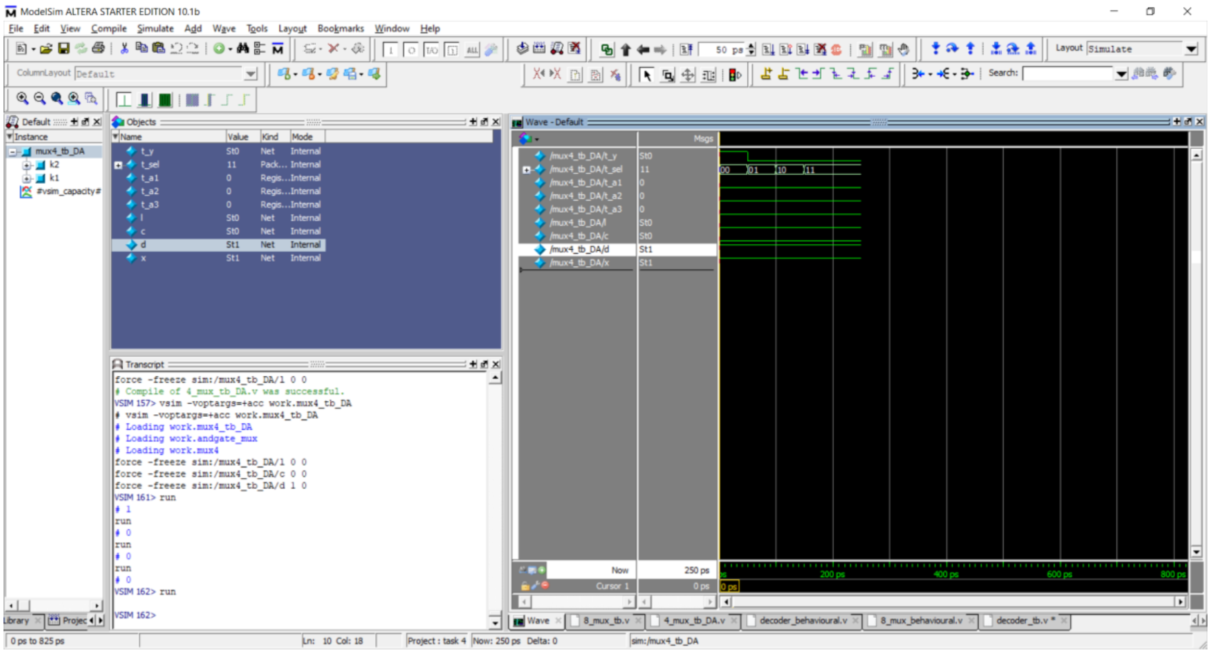
Name	Value	Kind	Mode
t_y	St0	Net	Internal
t_sel	11	Pack...	Internal
t_a1	0	Regis...	Internal
t_a2	0	Regis...	Internal
t_a3	0	Regis...	Internal
l	St0	Net	Internal
c	St0	Net	Internal
d	St1	Net	Internal
x	St1	Net	Internal

Transcript

```
force -freeze sim:/mux4_tb_DA/l 0 0
# Compile of 4_mux_tb_DA.v was successful.
VSIM 157> vsim -voptargs=+acc work.mux4_tb_DA
# vsim -voptargs=+acc work.mux4_tb_DA
# Loading work.mux4_tb_DA
# Loading work.andgate_mux
# Loading work.mux4
force -freeze sim:/mux4_tb_DA/l 0 0
force -freeze sim:/mux4_tb_DA/c 0 0
force -freeze sim:/mux4_tb_DA/d 1 0
VSIM 161> run
# 1
run
# 0
run
# 0
run
# 0
VSIM 162> run

VSIM 162>
```

Project : task 4 Now: 250 ps Delta: 0 sim:/mux4_tb_DA



ModelSim ALTERA STARTER EDITION 10.1b

Wave - Default

```
/mux4_tb_DA/t_y      St0
/mux4_tb_DA/t_sel    11     00 | 01 | 10 | 11
/mux4_tb_DA/t_a1     0
/mux4_tb_DA/t_a2     0
/mux4_tb_DA/t_a3     0
/mux4_tb_DA/l        St0
/mux4_tb_DA/c        St0
/mux4_tb_DA/d        St1
/mux4_tb_DA/x        St1

Now       250 ps
Cursor 1  0 ps
```

Objects

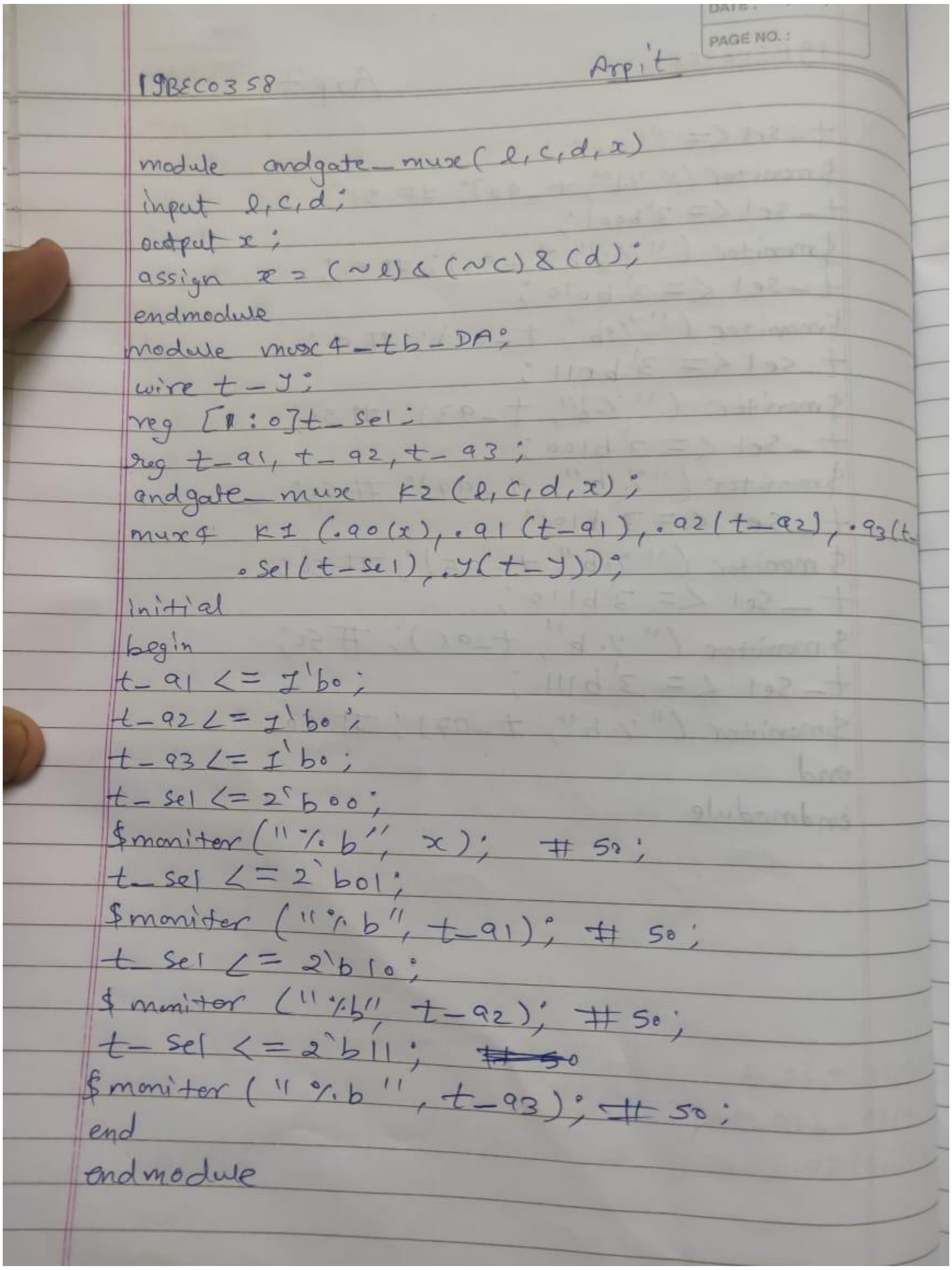
Name	Value	Kind	Mode
t_y	St0	Net	Internal
t_sel	11	Pack...	Internal
t_a1	0	Regis...	Internal
t_a2	0	Regis...	Internal
t_a3	0	Regis...	Internal
l	St0	Net	Internal
c	St0	Net	Internal
d	St1	Net	Internal
x	St1	Net	Internal

Transcript

```
force -freeze sim:/mux4_tb_DA/l 0 0
# Compile of 4_mux_tb_DA.v was successful.
VSIM 157> vsim -voptargs=+acc work.mux4_tb_DA
# vsim -voptargs=+acc work.mux4_tb_DA
# Loading work.mux4_tb_DA
# Loading work.andgate_mux
# Loading work.mux4
force -freeze sim:/mux4_tb_DA/l 0 0
force -freeze sim:/mux4_tb_DA/c 0 0
force -freeze sim:/mux4_tb_DA/d 1 0
VSIM 161> run
# 1
run
# 0
run
# 0
run
# 0
VSIM 162> run

VSIM 162>
```

0 ps to 825 ps Project : task 4 Now: 250 ps Delta: 0 sim:/mux4_tb_DA



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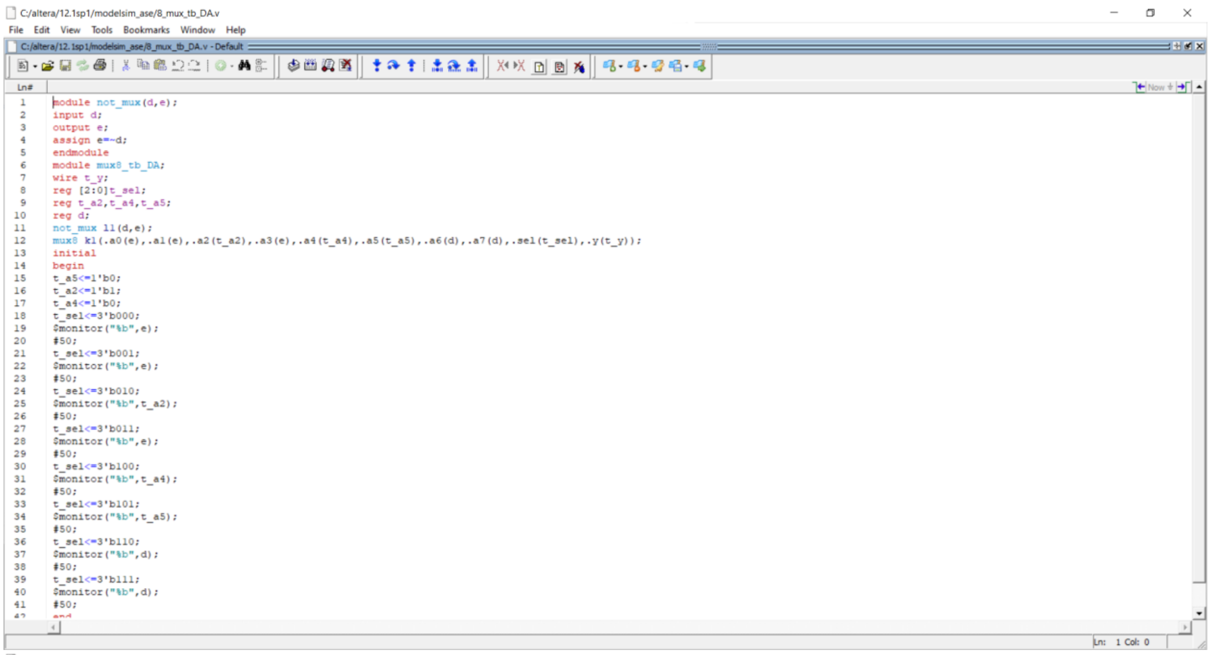
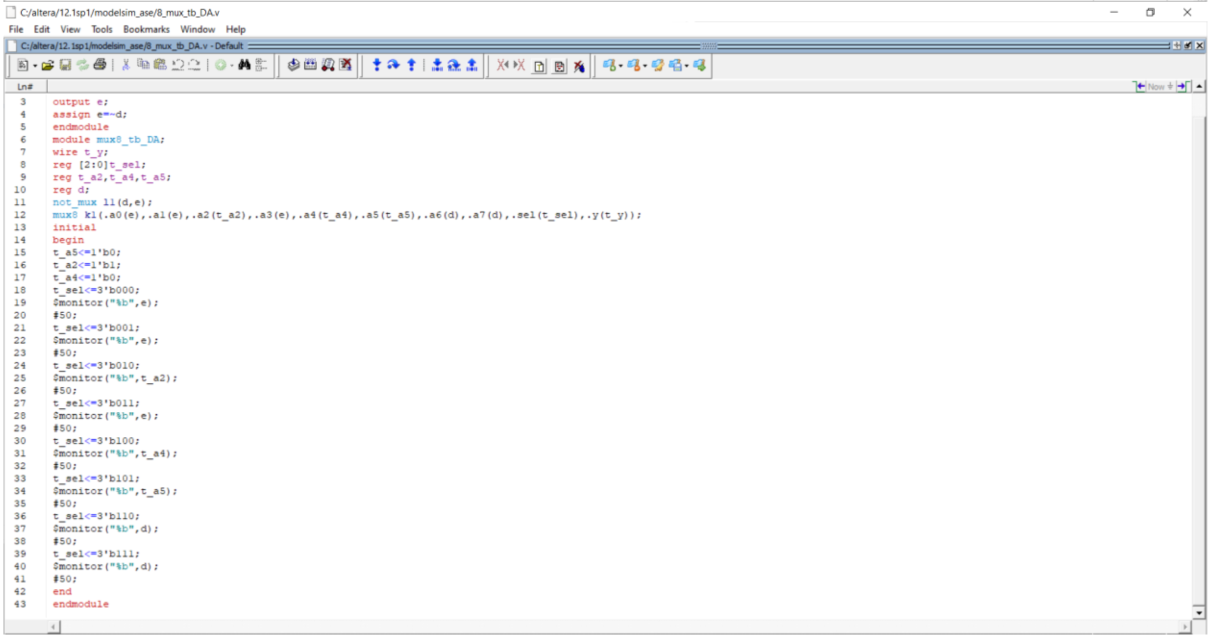
```
module andgate_mux(l,c,d,x)
input l,c,d;
output x;
assign x = (~l)&(~c)&(d);
endmodule
module mux4_tb_DA;
wire t_y;
reg [1:0]t_sel;
reg t_a1, t_a2, t_a3;
andgate_mux k2(l,c,d,x);
mux4 k1(.a0(x), .a1(t_a1), .a2(t_a2), .a3(t_
        .sel(t_sel), .y(t_y));
initial
begin
t_a1 <= 1'b0;
t_a2 <= 1'b0;
t_a3 <= 1'b0;
t_sel <= 2'b00;
$monitor("%b", x);   #50;
t_sel <= 2`b01;
$moniter ("%b", t_a1); #50;
t_sel <= 2`b10;
$monitor ("%b", t_a2); #50;
t_sel <= 2`b11;   ~~#50~~
$moniter ("%b", t_a3); #50;
end
endmodule
```

8X1 mux

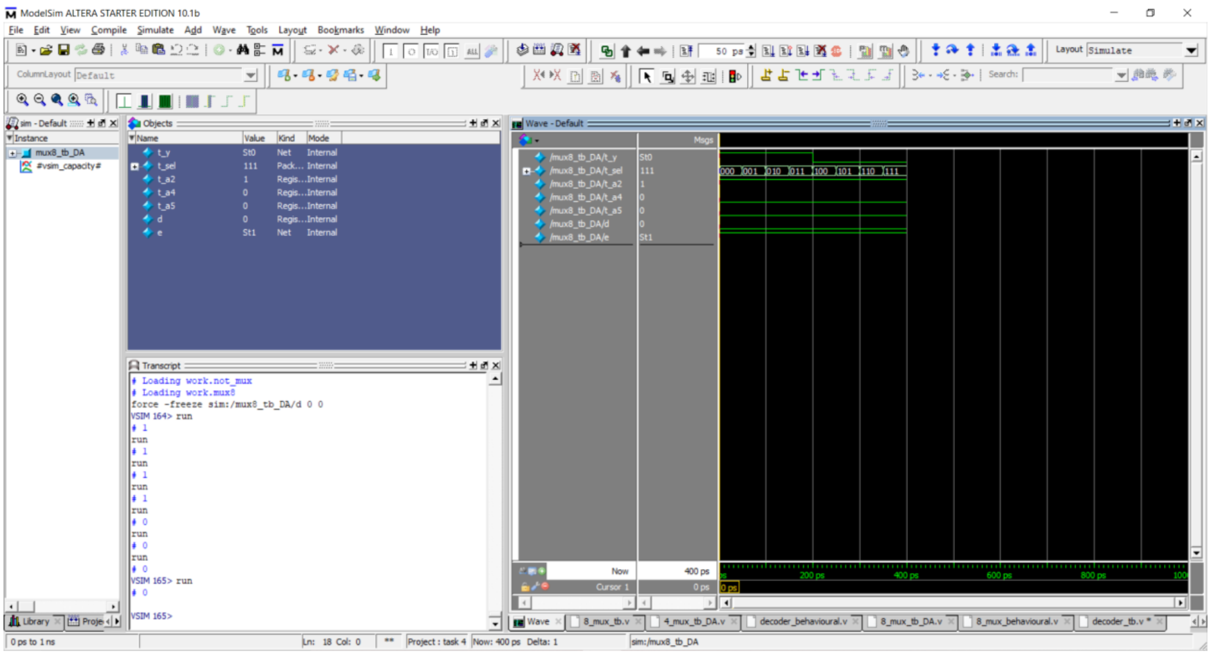

C:/altera/12.1sp1/modelsim_ase/8_mux_tb_DA.v
File Edit View Tools Bookmarks Window Help
C:/altera/12.1sp1/modelsim_ase/8_mux_tb_DA.v - Default
Ln#
Now
Ln: 1 Col: 0

```
module not_mux(d,e);
input d;
output e;
assign e=~d;
endmodule
module mux8_tb_DA;
wire t_y;
reg [2:0]t_sel;
reg t_a2,t_a4,t_a5;
reg d;
not_mux l1(d,e);
mux8 k1(.a0(e),.a1(e),.a2(t_a2),.a3(e),.a4(t_a4),.a5(t_a5),.a6(d),.a7(d),.sel(t_sel),.y(t_y));
initial
begin
t_a5<=1'b0;
t_a2<=1'b1;
t_a4<=1'b0;
t_sel<=3'b000;
$monitor("%b",e);
#50;
t_sel<=3'b001;
$monitor("%b",e);
#50;
t_sel<=3'b010;
$monitor("%b",t_a2);
#50;
t_sel<=3'b011;
$monitor("%b",e);
#50;
t_sel<=3'b100;
$monitor("%b",t_a4);
#50;
t_sel<=3'b101;
$monitor("%b",t_a5);
#50;
t_sel<=3'b110;
$monitor("%b",d);
#50;
t_sel<=3'b111;
$monitor("%b",d);
#50;
```


C:/altera/12.1sp1/modelsim_ase/8_mux_tb_DA.v
File Edit View Tools Bookmarks Window Help
C:/altera/12.1sp1/modelsim_ase/8_mux_tb_DA.v - Default
Ln#
Now

```
output e;
assign e=~d;
endmodule
module mux8_tb_DA;
wire t_y;
reg [2:0]t_sel;
reg t_a2,t_a4,t_a5;
reg d;
not_mux l1(d,e);
mux8 k1(.a0(e),.a1(e),.a2(t_a2),.a3(e),.a4(t_a4),.a5(t_a5),.a6(d),.a7(d),.sel(t_sel),.y(t_y));
initial
begin
t_a5<=1'b0;
t_a2<=1'b1;
t_a4<=1'b0;
t_sel<=3'b000;
$monitor("%b",e);
#50;
t_sel<=3'b001;
$monitor("%b",e);
#50;
t_sel<=3'b010;
$monitor("%b",t_a2);
#50;
t_sel<=3'b011;
$monitor("%b",e);
#50;
t_sel<=3'b100;
$monitor("%b",t_a4);
#50;
t_sel<=3'b101;
$monitor("%b",t_a5);
#50;
t_sel<=3'b110;
$monitor("%b",d);
#50;
t_sel<=3'b111;
$monitor("%b",d);
#50;
```

```
end
endmodule
```



Name	Value	Kind	Mode
t_y	St0	Net	Internal
t_sel	111	Pack...	Internal
t_a2	1	Regis...	Internal
t_a4	0	Regis...	Internal
t_a5	0	Regis...	Internal
d	0	Regis...	Internal
e	St1	Net	Internal

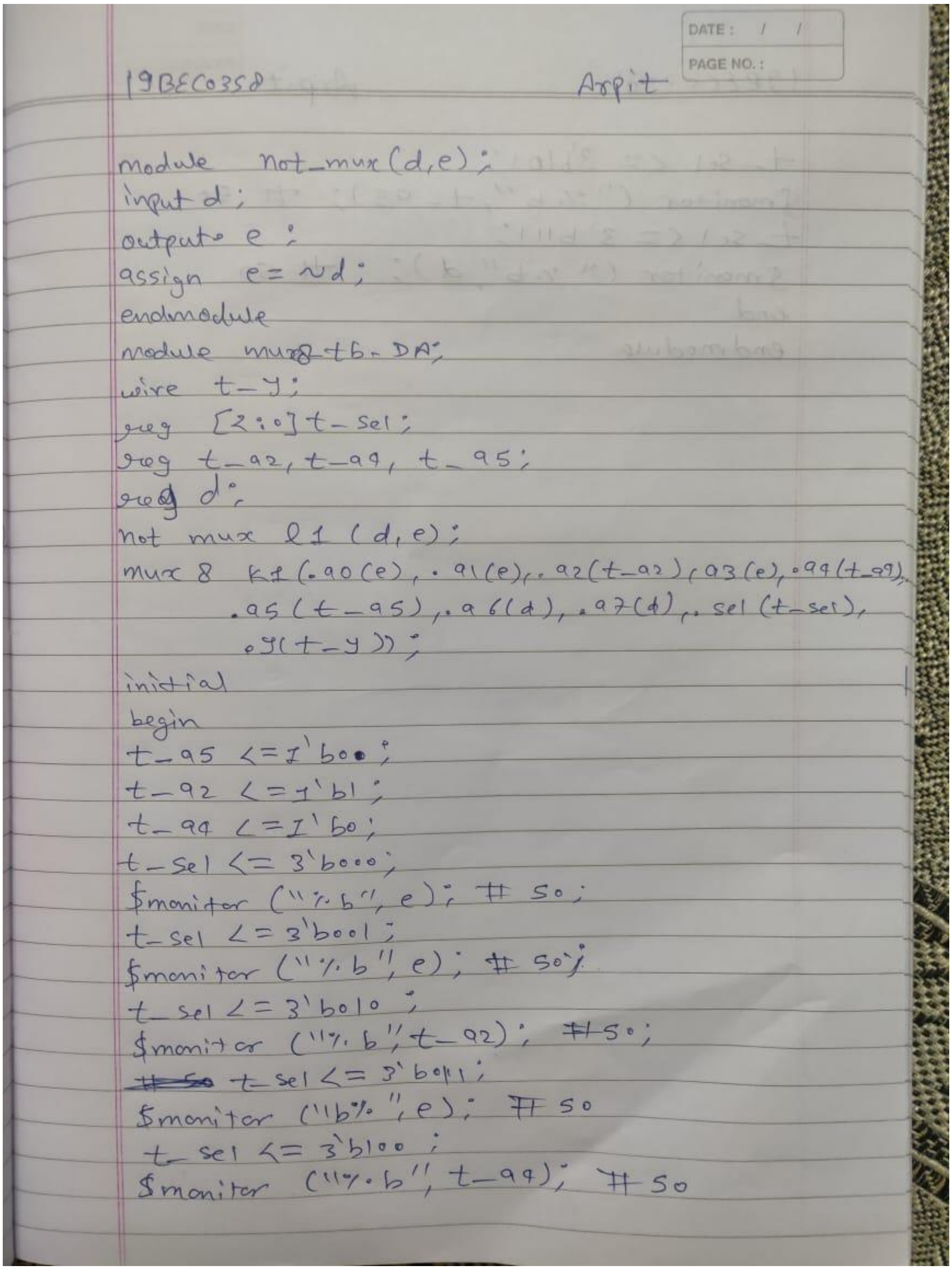
```
/mux8_tb_DA/t_y      St0
/mux8_tb_DA/t_sel    111    000 001 010 011 100 101 110 111
/mux8_tb_DA/t_a2     1
/mux8_tb_DA/t_a4     0
/mux8_tb_DA/t_a5     0
/mux8_tb_DA/d        0
/mux8_tb_DA/e        St1
```

Transcript

```
# Loading work.not_mux
# Loading work.mux8
force -freeze sim:/mux8_tb_DA/d 0 0
VSIM 164> run
# 1
run
# 1
run
# 1
run
# 1
run
# 0
run
# 0
run
# 0
VSIM 165> run
# 0

VSIM 165>
```

```
0 ps to 1 ns    Ln: 18 Col: 0    **    Project : task 4    Now: 400 ps  Delta: 1    sim:/mux8_tb_DA
```



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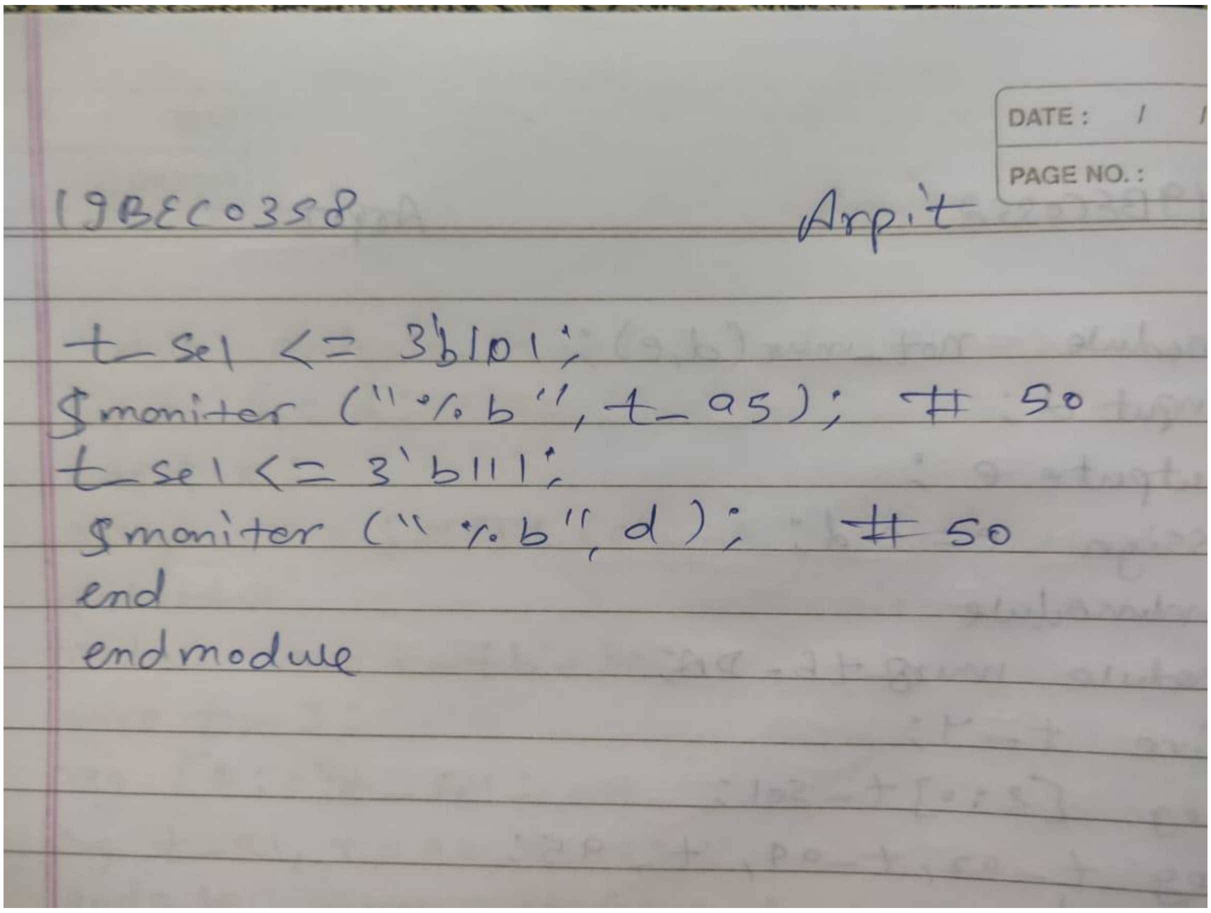
```
module  not_mux(d,e);
input d;
output e;
assign  e=~d;
endmodule
module  mux8_tb_DA;
wire  t_y;
reg  [2:0] t_sel;
reg  t_a2, t_a4,  t_a5;
reg  d;
not mux  l1 (d,e);
mux 8  k1(.a0(e), .a1(e), .a2(t_a2), a3(e), .a4(t_a4),
         .a5(t_a5), .a6(d), .a7(d), .sel(t_sel),
         .y(t_y));
initial
begin
t_a5  <= 1'b0;
t_a2  <= 1'b1;
t_a4  <= 1'b0;
t_sel <= 3'b000;
$monitor ("%b", e); # 50;
t_sel  <= 3'b001;
$monitor ("%b", e); # 50;
t_sel <= 3'b010;
$monitor  ("%b", t_a2);  #50;
~~#50~~ t_sel <= 3'b011;
$monitor ("b%", e); # 50
t_sel <= 3'b100;
$monitor  ("%b", t_a4); # 50
```



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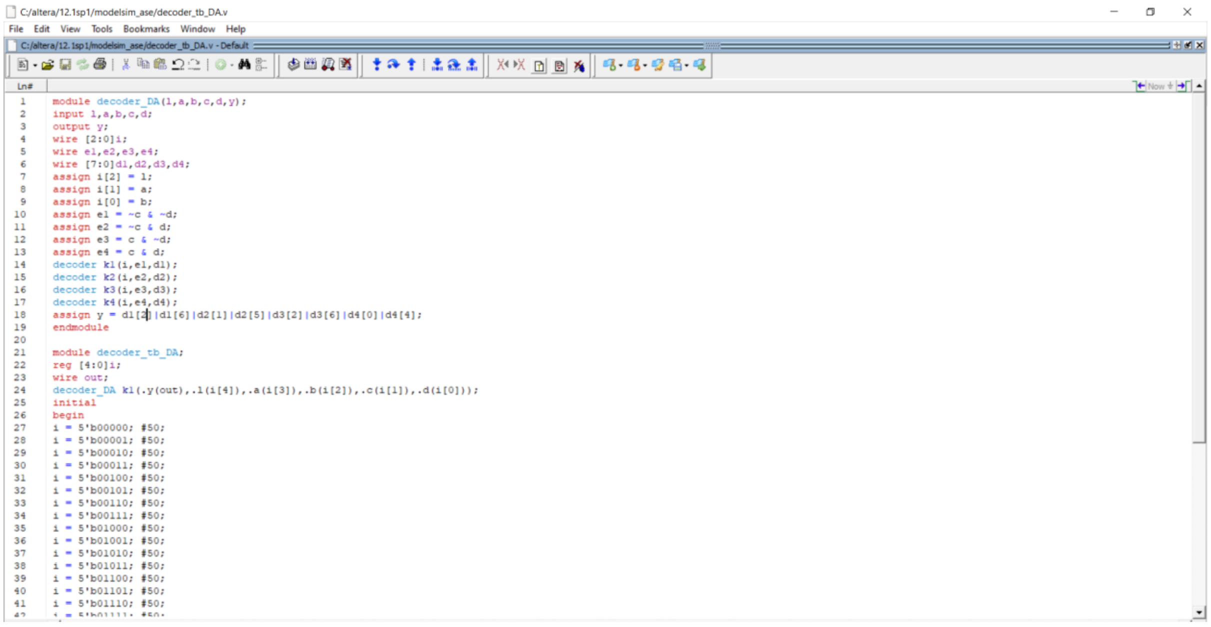
```
t_sel <= 3'b101;
$moniter ("%b", t_a5); #50
t_sel <= 3'b111;
$moniter (" %b", d); #50
end
endmodule
```

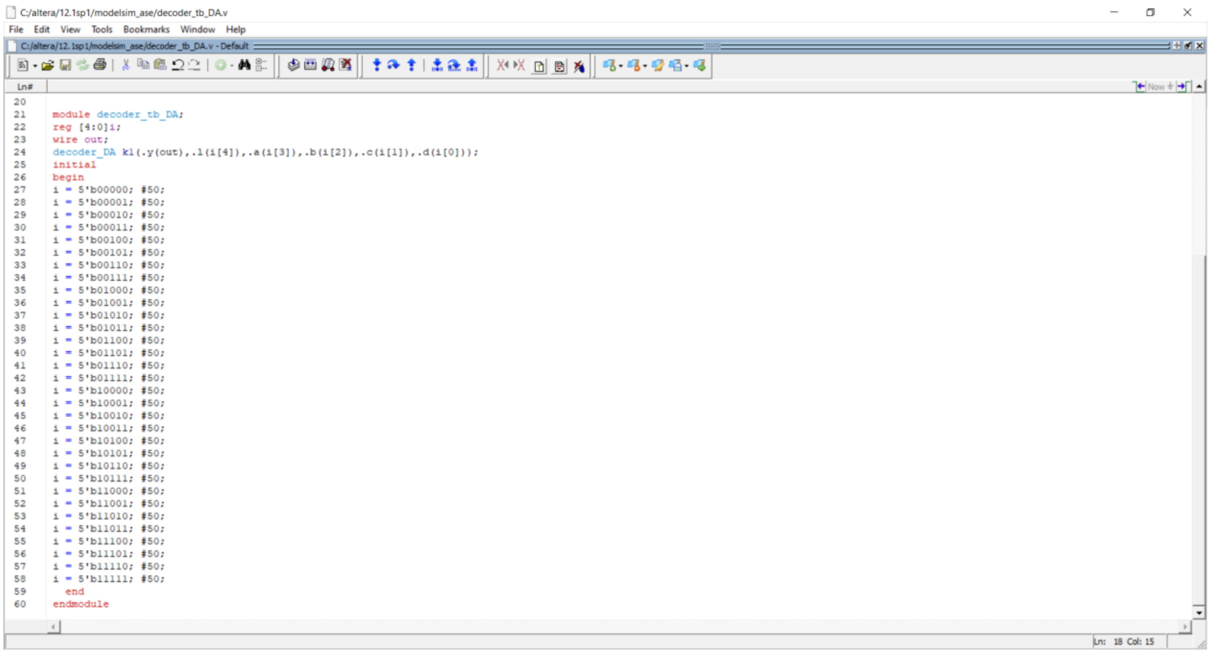
3X8 decoder coding –



C:/altera/12.1sp1/modelsim_ase/decoder_tb_DA.v

```
module decoder_DA(l,a,b,c,d,y);
input l,a,b,c,d;
output y;
wire [2:0]i;
wire e1,e2,e3,e4;
wire [7:0]d1,d2,d3,d4;
assign i[2] = l;
assign i[1] = a;
assign i[0] = b;
assign e1 = ~c & ~d;
assign e2 = ~c & d;
assign e3 = c & ~d;
assign e4 = c & d;
decoder k1(i,e1,d1);
decoder k2(i,e2,d2);
decoder k3(i,e3,d3);
decoder k4(i,e4,d4);
assign y = d1[2]|d1[6]|d2[1]|d2[5]|d3[2]|d3[6]|d4[0]|d4[4];
endmodule

module decoder_tb_DA;
reg [4:0]i;
wire out;
decoder_DA k1(.y(out),.l(i[4]),.a(i[3]),.b(i[2]),.c(i[1]),.d(i[0]));
initial
begin
i = 5'b00000; #50;
i = 5'b00001; #50;
i = 5'b00010; #50;
i = 5'b00011; #50;
i = 5'b00100; #50;
i = 5'b00101; #50;
i = 5'b00110; #50;
i = 5'b00111; #50;
i = 5'b01000; #50;
i = 5'b01001; #50;
i = 5'b01010; #50;
i = 5'b01011; #50;
i = 5'b01100; #50;
i = 5'b01101; #50;
i = 5'b01110; #50;
```



C:/altera/12.1sp1/modelsim_ase/decoder_tb_DA.v

```

module decoder_tb_DA;
reg [4:0]i;
wire out;
decoder_DA k1(.y(out),.l(i[4]),.a(i[3]),.b(i[2]),.c(i[1]),.d(i[0]));
initial
begin
i = 5'b00000; #50;
i = 5'b00001; #50;
i = 5'b00010; #50;
i = 5'b00011; #50;
i = 5'b00100; #50;
i = 5'b00101; #50;
i = 5'b00110; #50;
i = 5'b00111; #50;
i = 5'b01000; #50;
i = 5'b01001; #50;
i = 5'b01010; #50;
i = 5'b01011; #50;
i = 5'b01100; #50;
i = 5'b01101; #50;
i = 5'b01110; #50;
i = 5'b01111; #50;
i = 5'b10000; #50;
i = 5'b10001; #50;
i = 5'b10010; #50;
i = 5'b10011; #50;
i = 5'b10100; #50;
i = 5'b10101; #50;
i = 5'b10110; #50;
i = 5'b10111; #50;
i = 5'b11000; #50;
i = 5'b11001; #50;
i = 5'b11010; #50;
i = 5'b11011; #50;
i = 5'b11100; #50;
i = 5'b11101; #50;
i = 5'b11110; #50;
i = 5'b11111; #50;
  end
endmodule
```

Ln: 18 Col: 15

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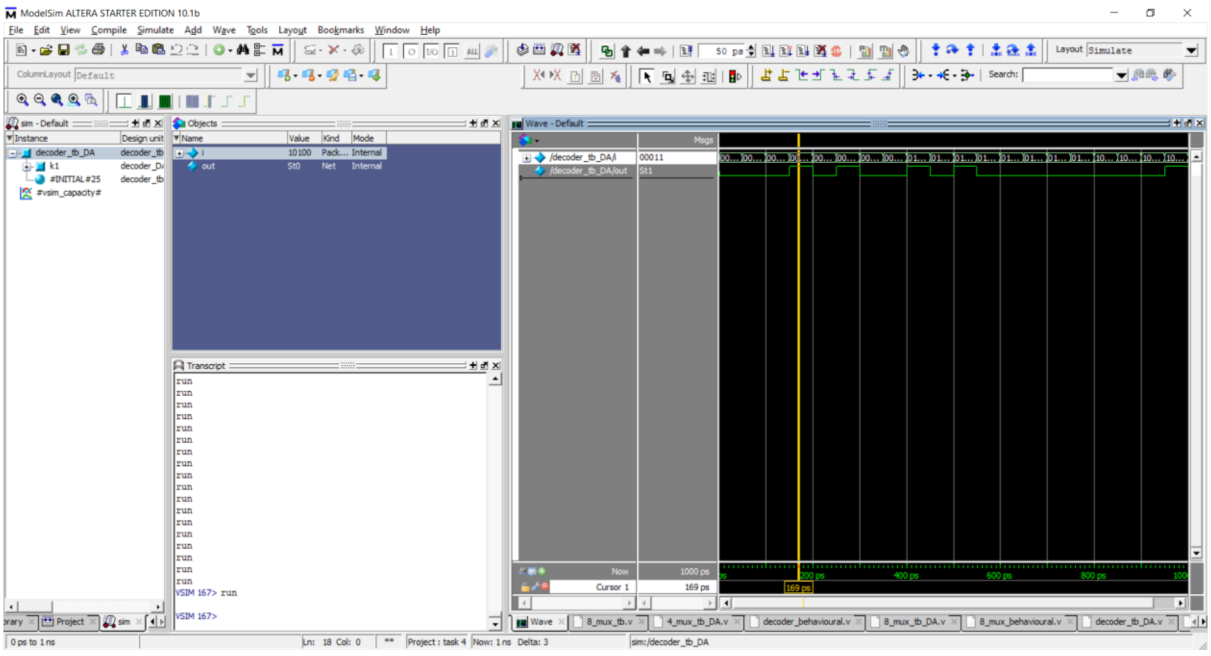

Instance	Design unit
decoder_tb_DA	decoder_tb
k1	decoder_D
#INITIAL#25	decoder_tb
#vsim_capacity#	

Name	Value	Kind	Mode
i	10100	Pack...	Internal
out	St0	Net	Internal

```
run
run
run
run
run
run
run
run
run
run
run
run
run
run
run
run
run
run
VSIM 167> run

VSIM 167>
```

```
/decoder_tb_DA/i     00011   00... 00... 00... 00... 00... 00... 00... 00... 01... 01... 01... 01... 01... 01... 01... 01... 10... 10... 10... 10...
/decoder_tb_DA/out   St1
Now      1000 ps     ps  200 ps  400 ps  600 ps  800 ps  100
Cursor 1  169 ps     169 ps
```

```
0 ps to 1 ns    Ln: 18 Col: 0   **   Project : task 4   Now: 1 ns  Delta: 3    sim:/decoder_tb_DA
```