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Course Name	VLSI system design		
Program Title	Lab Assignment 5		
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1. Design a positive latch and a negative latch.

2. Verify with inputs and outputs.

3. Create a symbol for the positive and negative latches.

4. Design a positive and negative edge trigger Flip flops using positive and negative latches symbol.

5. Verify with inputs and outputs.

1).

Aim → To design positive and negative latch

Circuit Diagram →

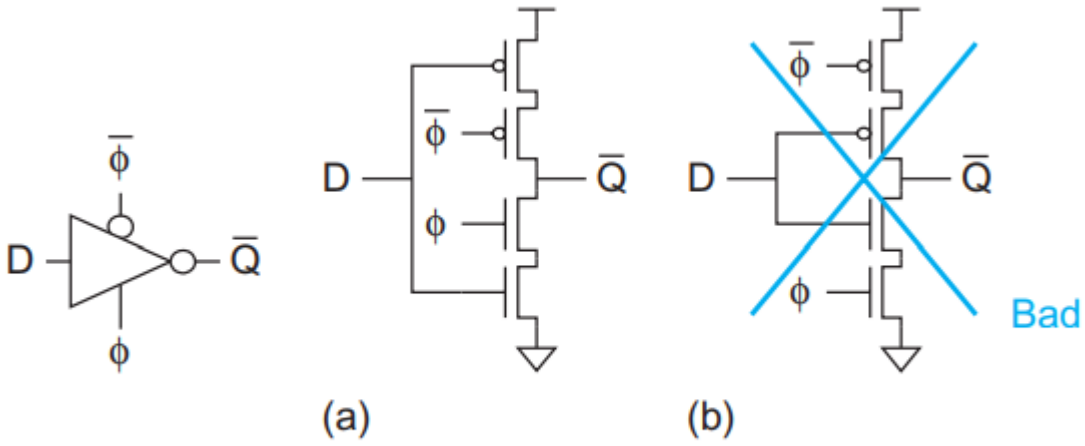
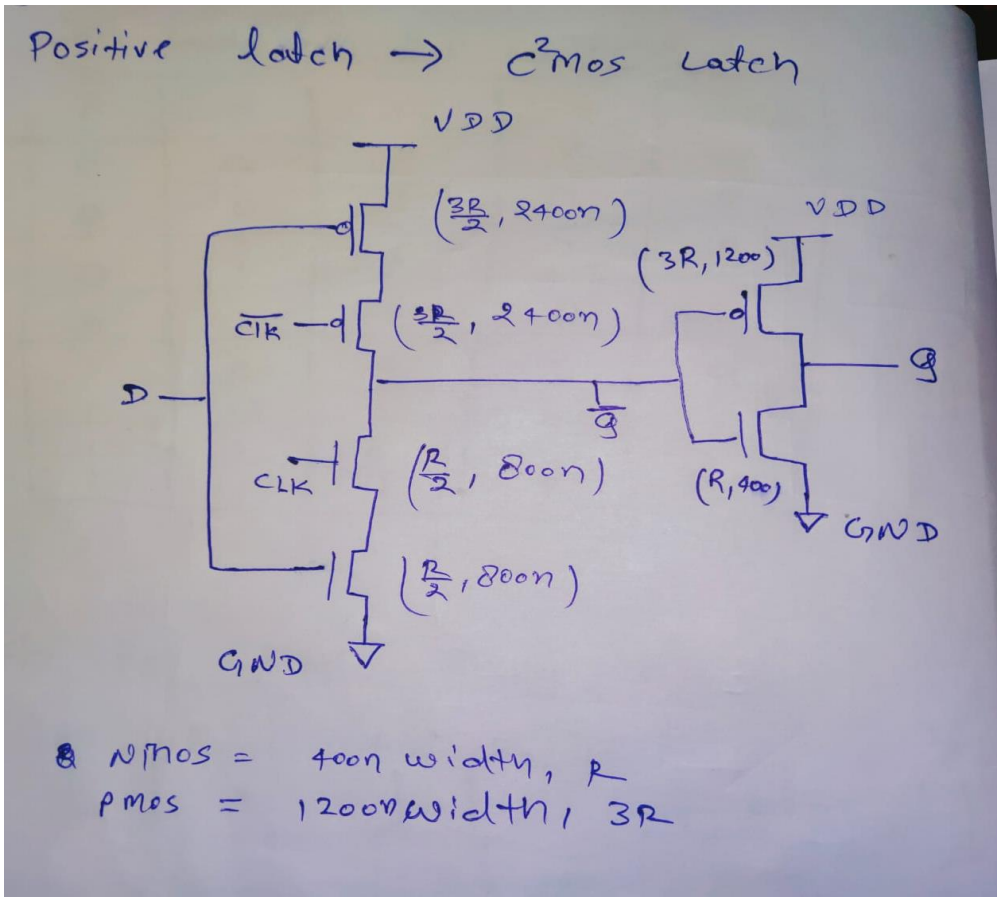


FIGURE 10.18 C²MOS Latch

Note: circuit is refereed from CMOS VLSI DESIGN BOOK



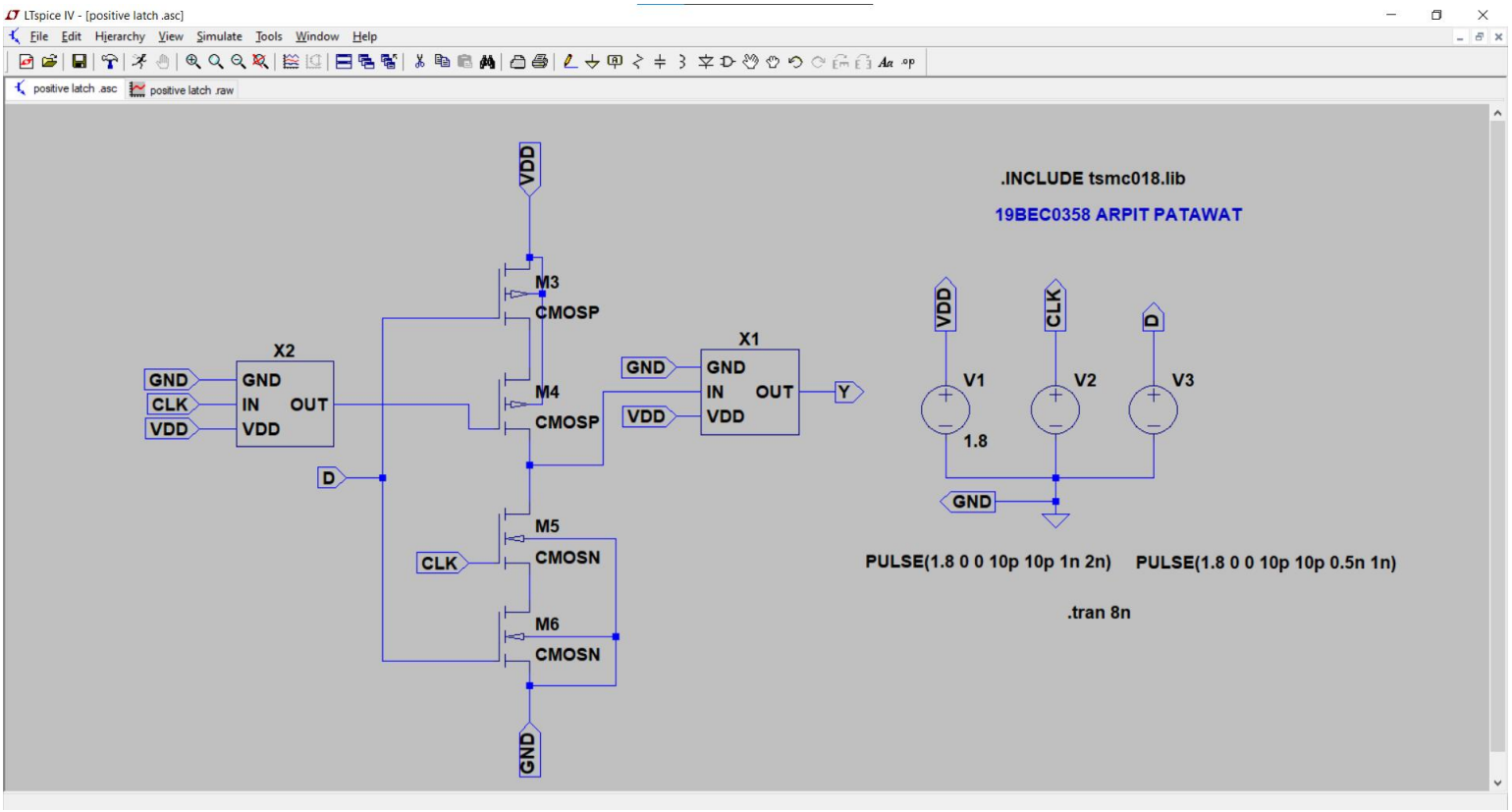
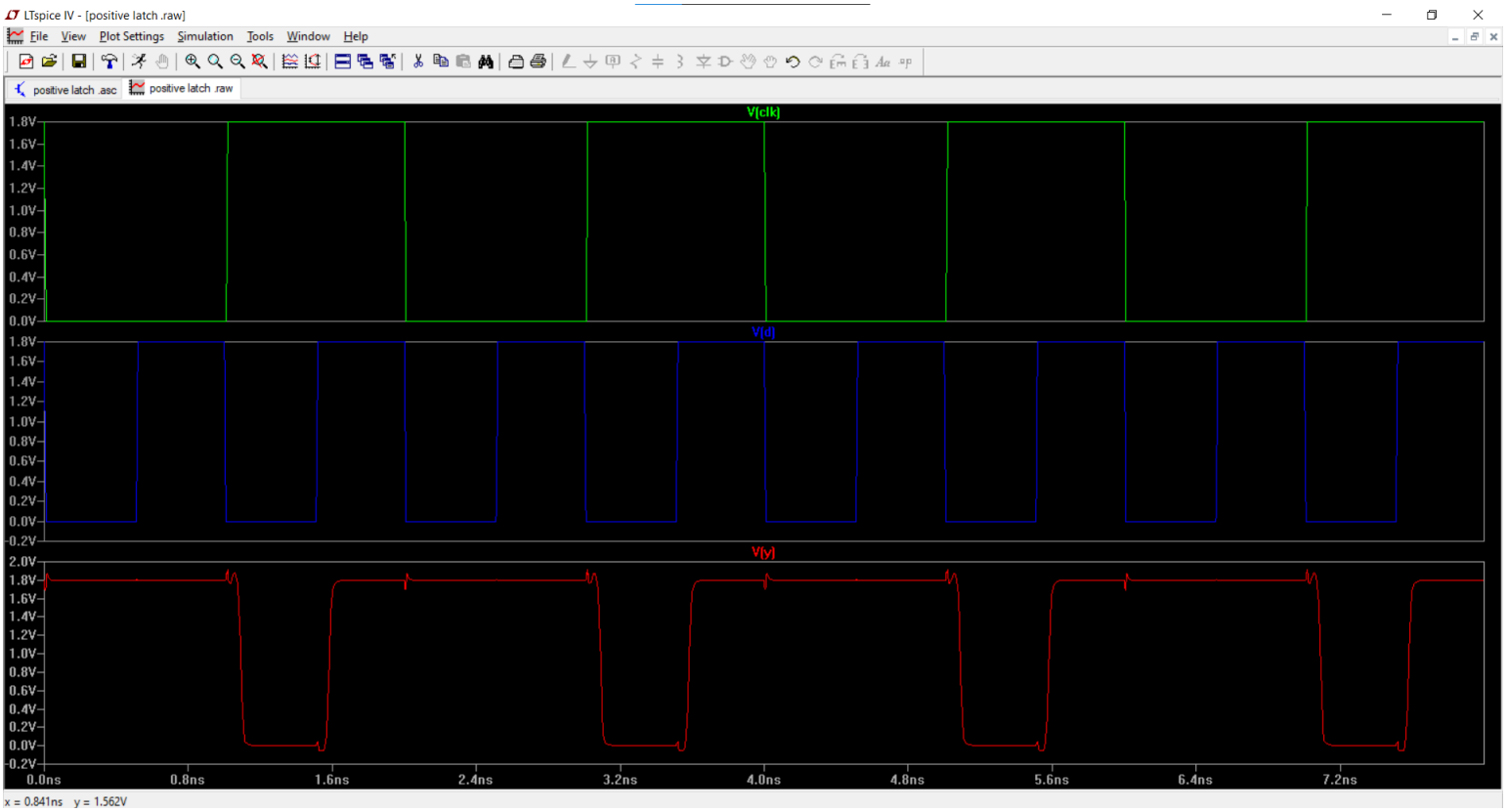
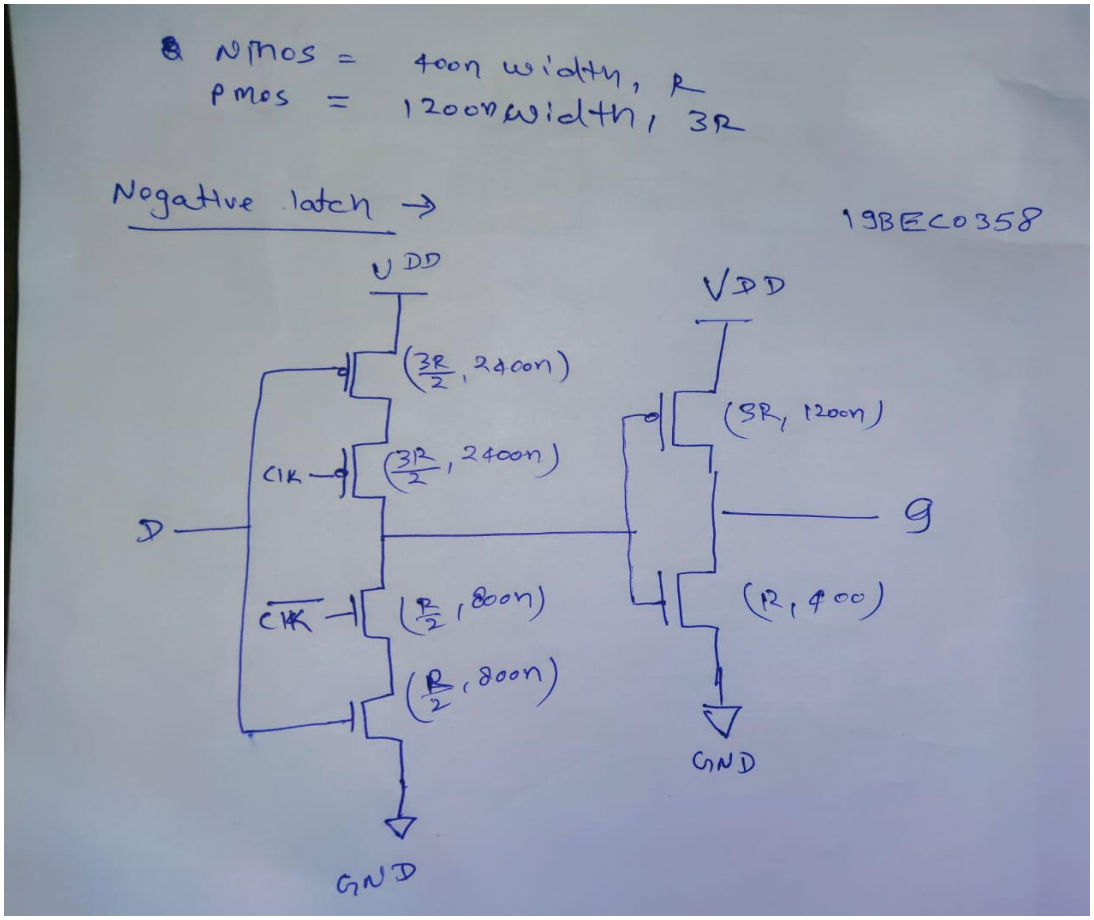


Fig – positive latch with X1 and X2 symbol for inverter



Whenever clock is high, output signal is data signal (transparent mode) and when clock is low, the last value of data will keep as output (hold mode)



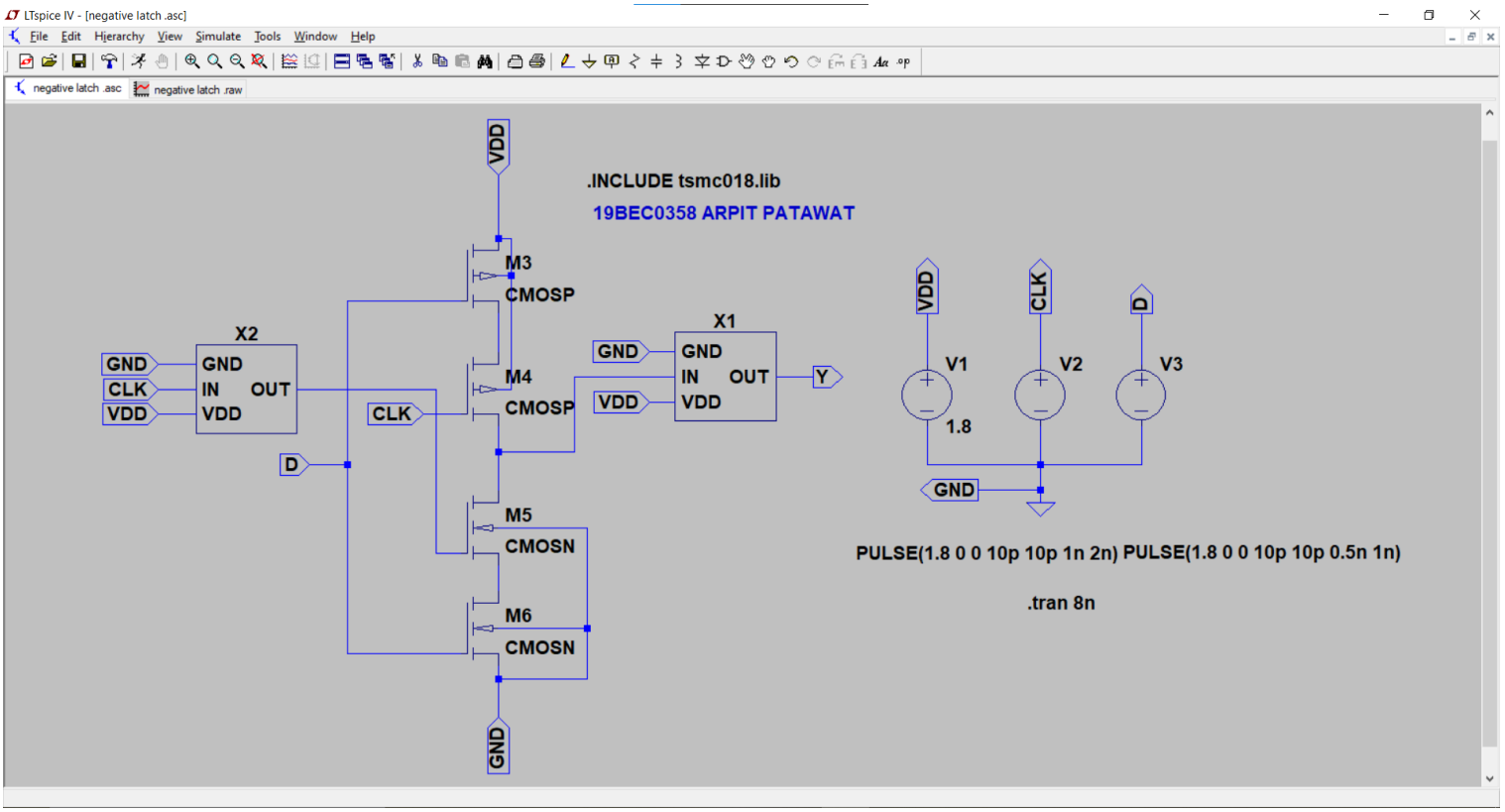
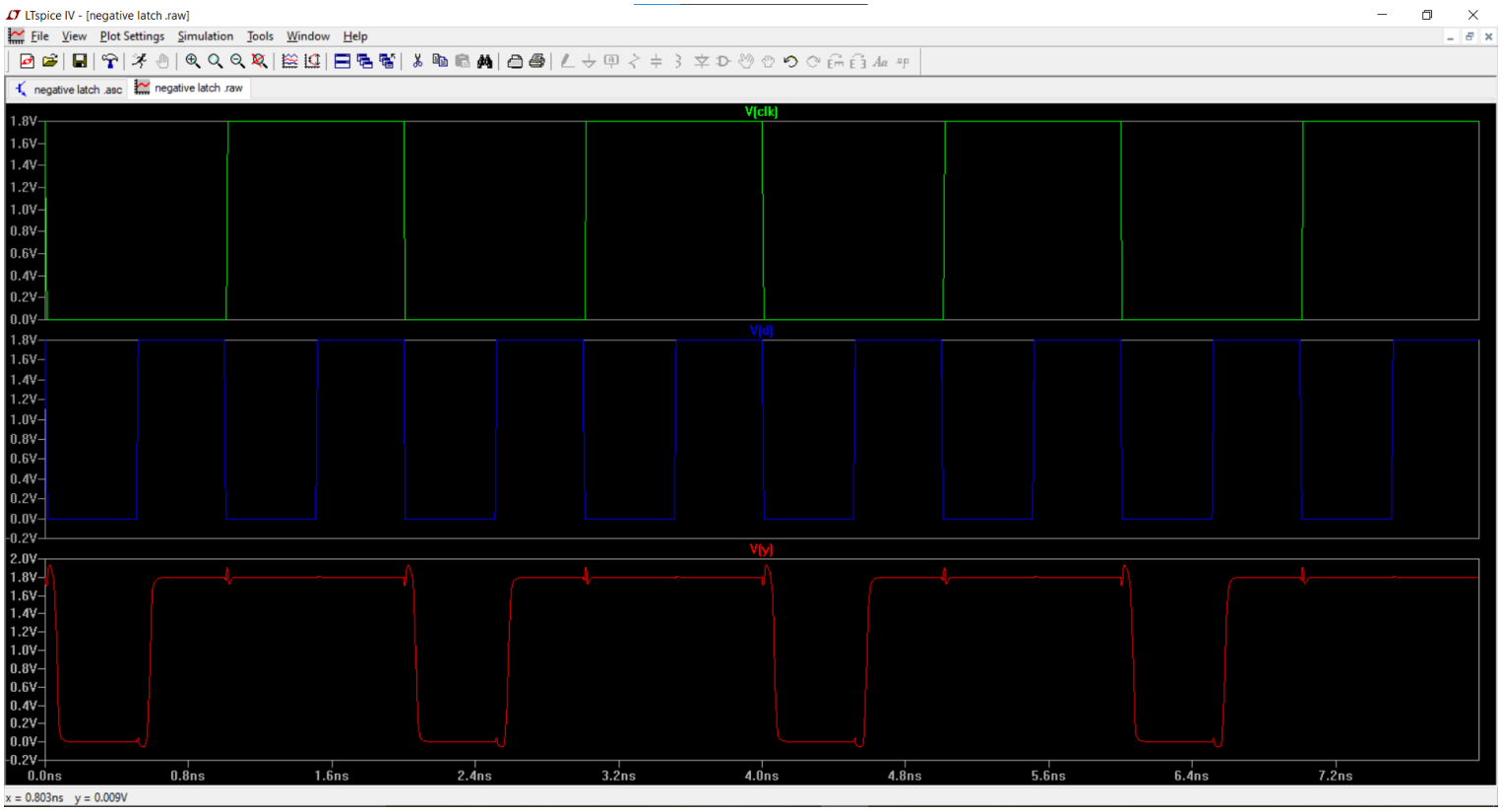


Fig – Negative latch with X1 and X2 symbol for inverter



Whenever clock is Low, output signal is data signal (transparent mode) and when clock is High, the last value of data will keep as output (hold mode).

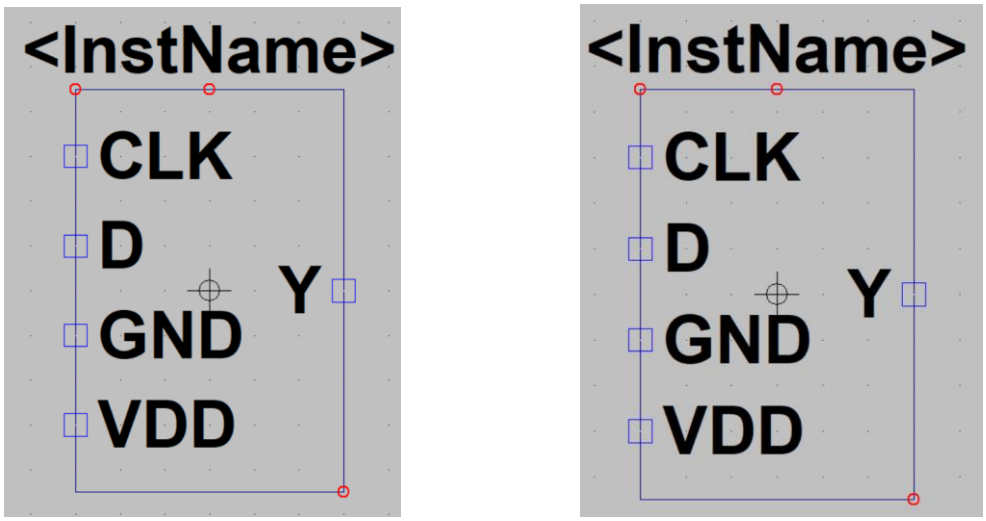
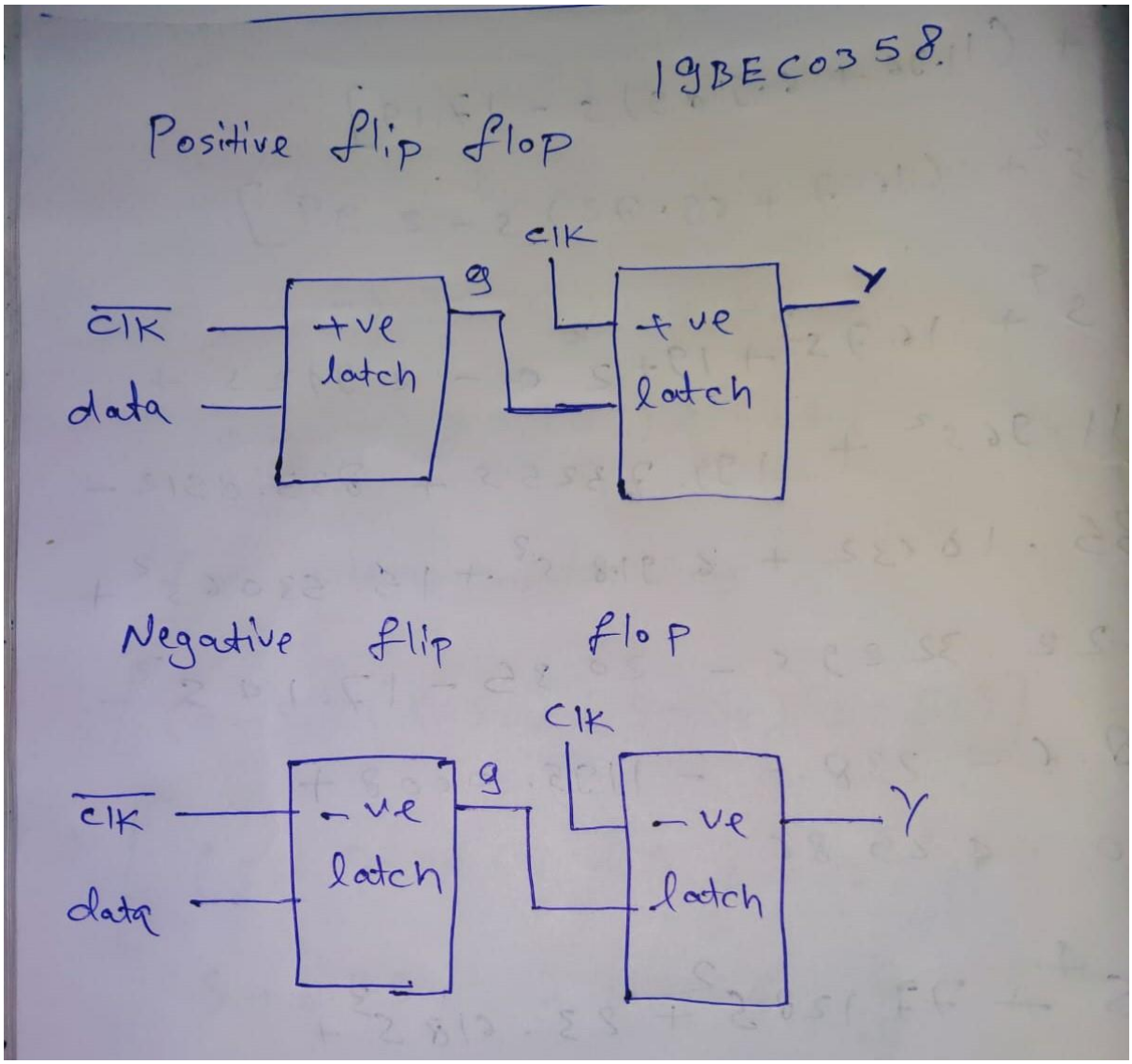


Fig – symbol for positive and Negative respectively. While doing both the latches, before adding volage sources, I copied both the circuit for symbol creation.

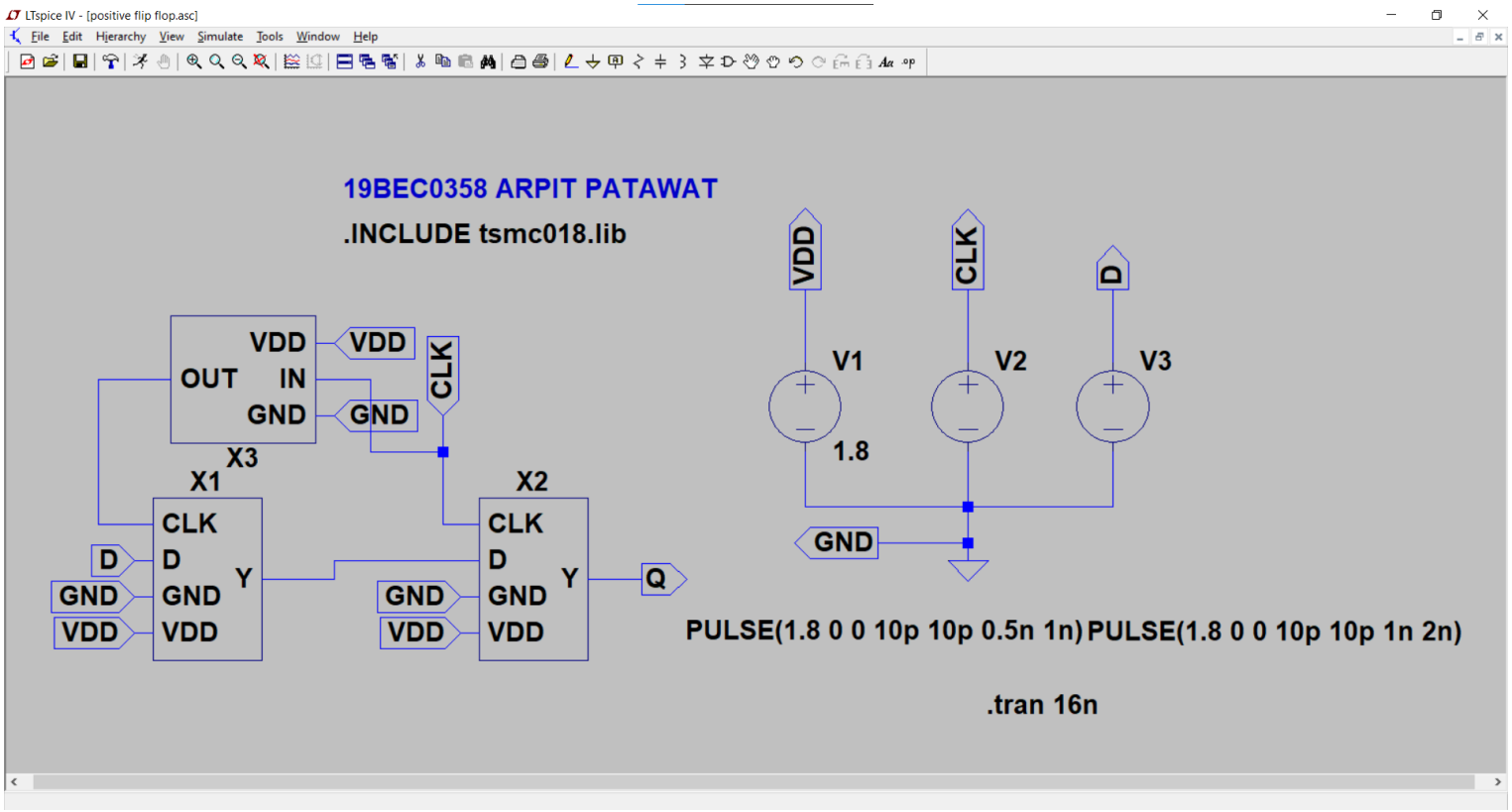
2).

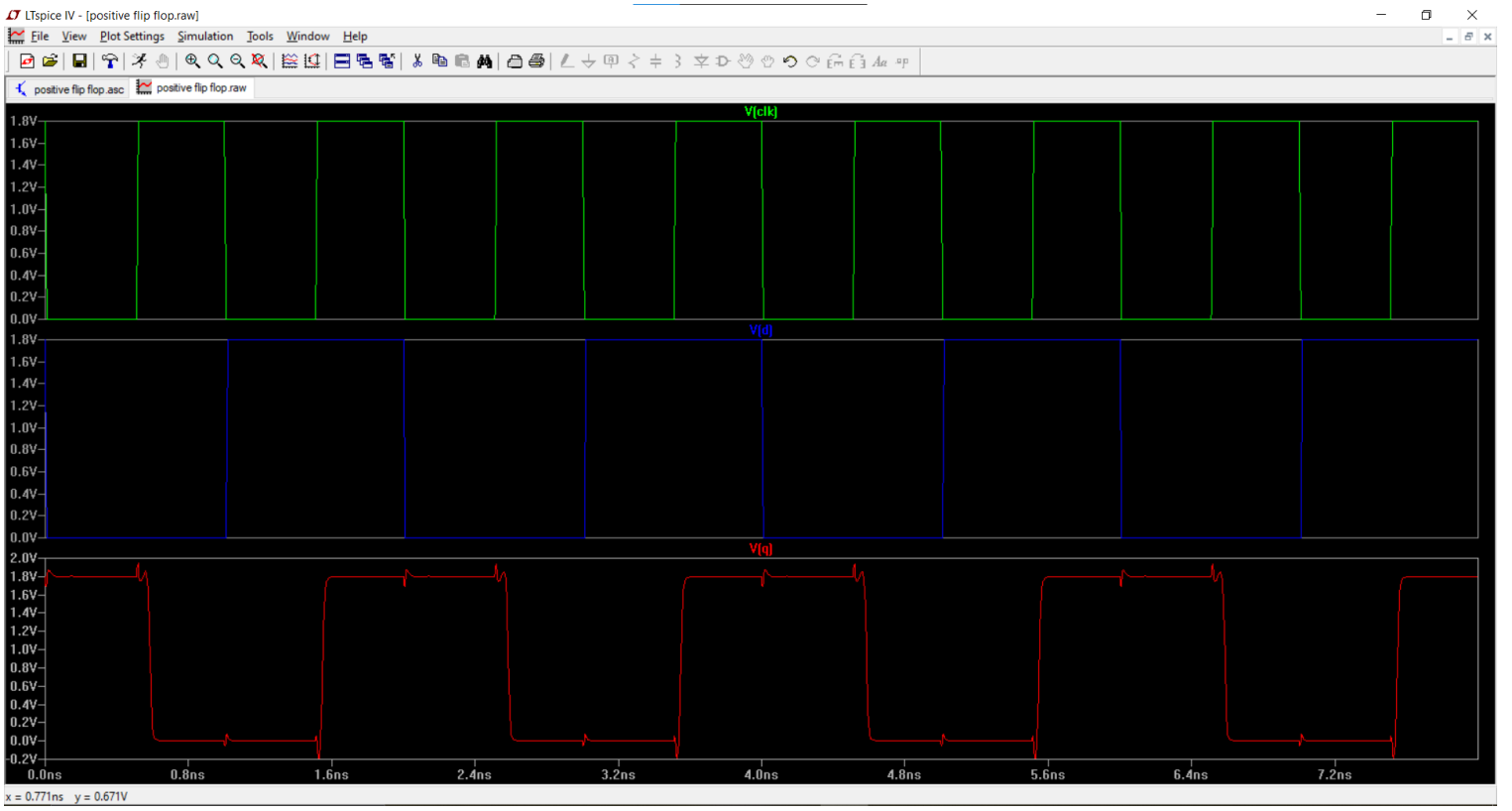
Aim → To design positive and negative flip flop

Circuit Diagram →



POSITIVE FLIP FLOP → Whenever clock is Rising or for the rising edge of the clock, whatever the value of data, output signal will keep following that until the next rising edge





NEGATIVE FLIP FLOP →

for the falling edge of the clock, whatever the value of data, output signal will keep following that until the next falling edge