Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Reg.No	19BEC0358		
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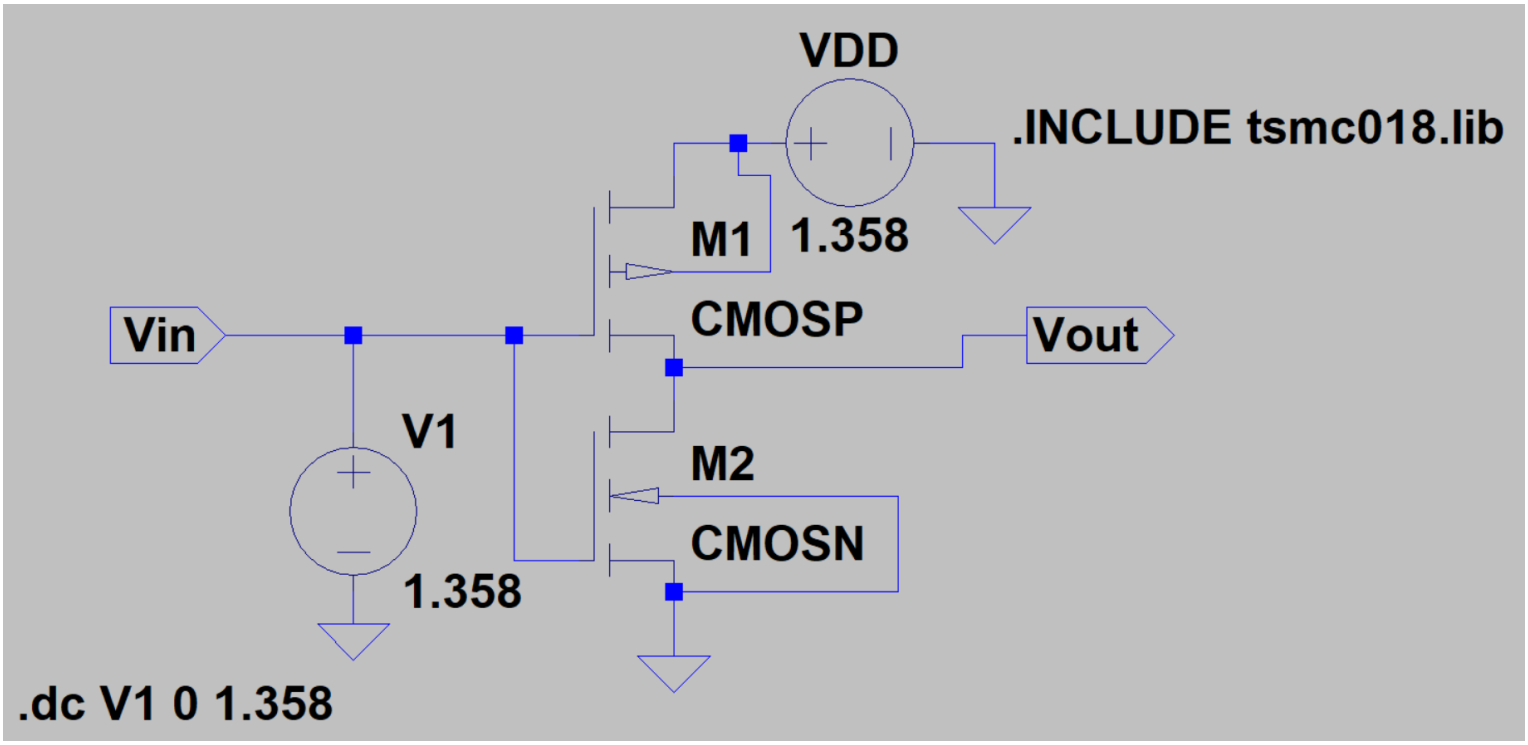
Course Code	ECE3002	**Slot & Semester**	L43+L44 WINTER -- 2021-22
Course Name	VLSI system design		
Program Title	Lab Assignment 3		
Faculty	Dr. Ragunath G		

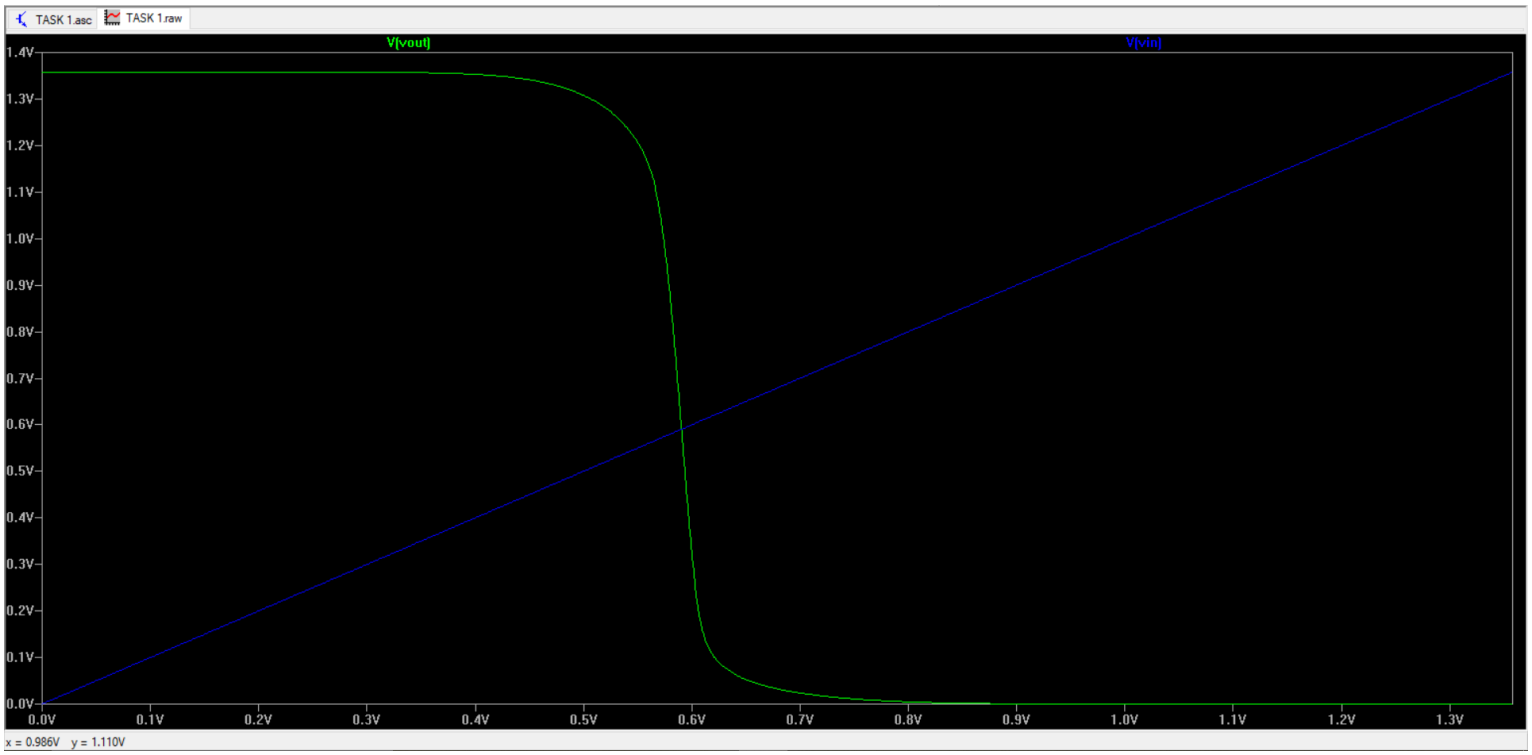
School of Electronics Engineering ,VIT, Vellore

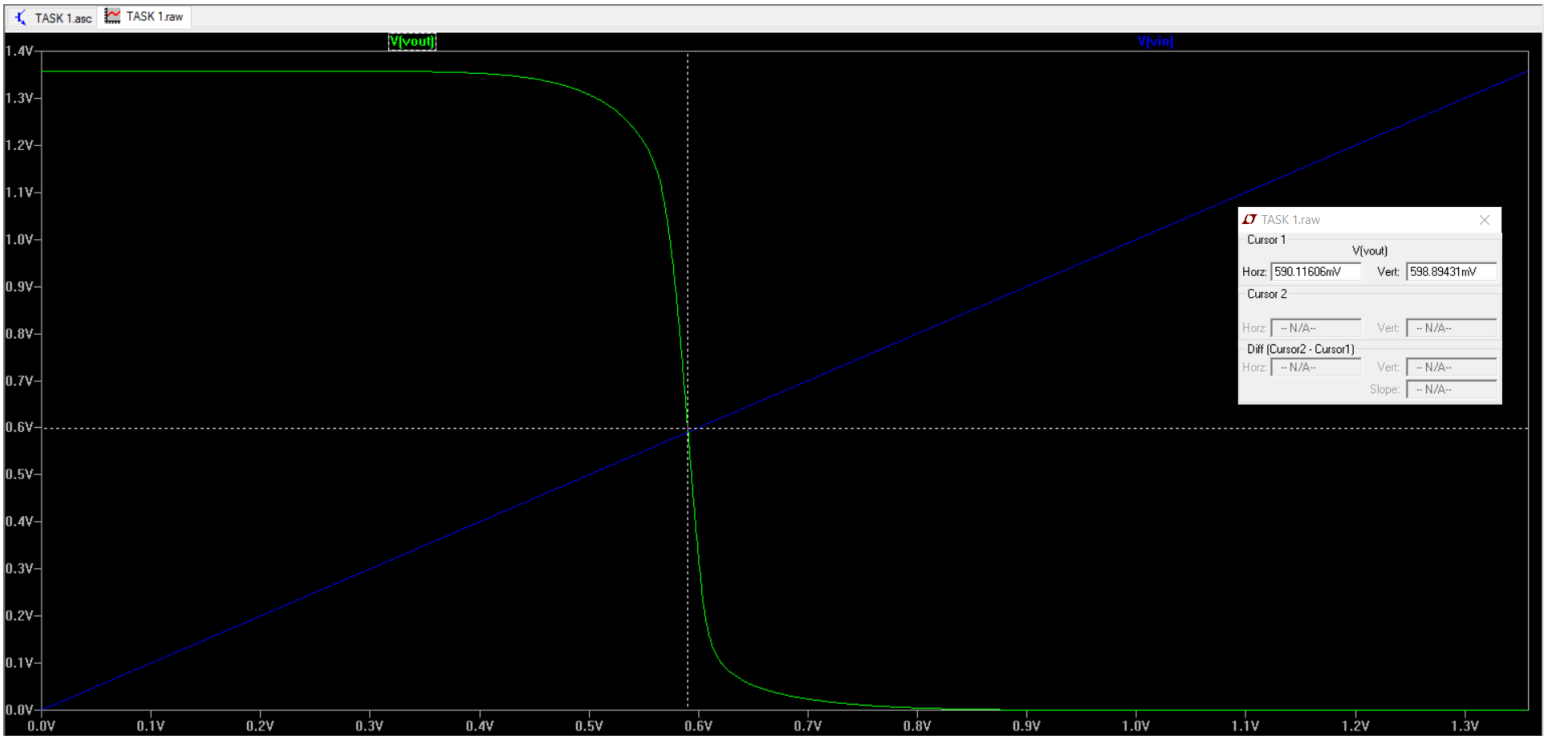
1).

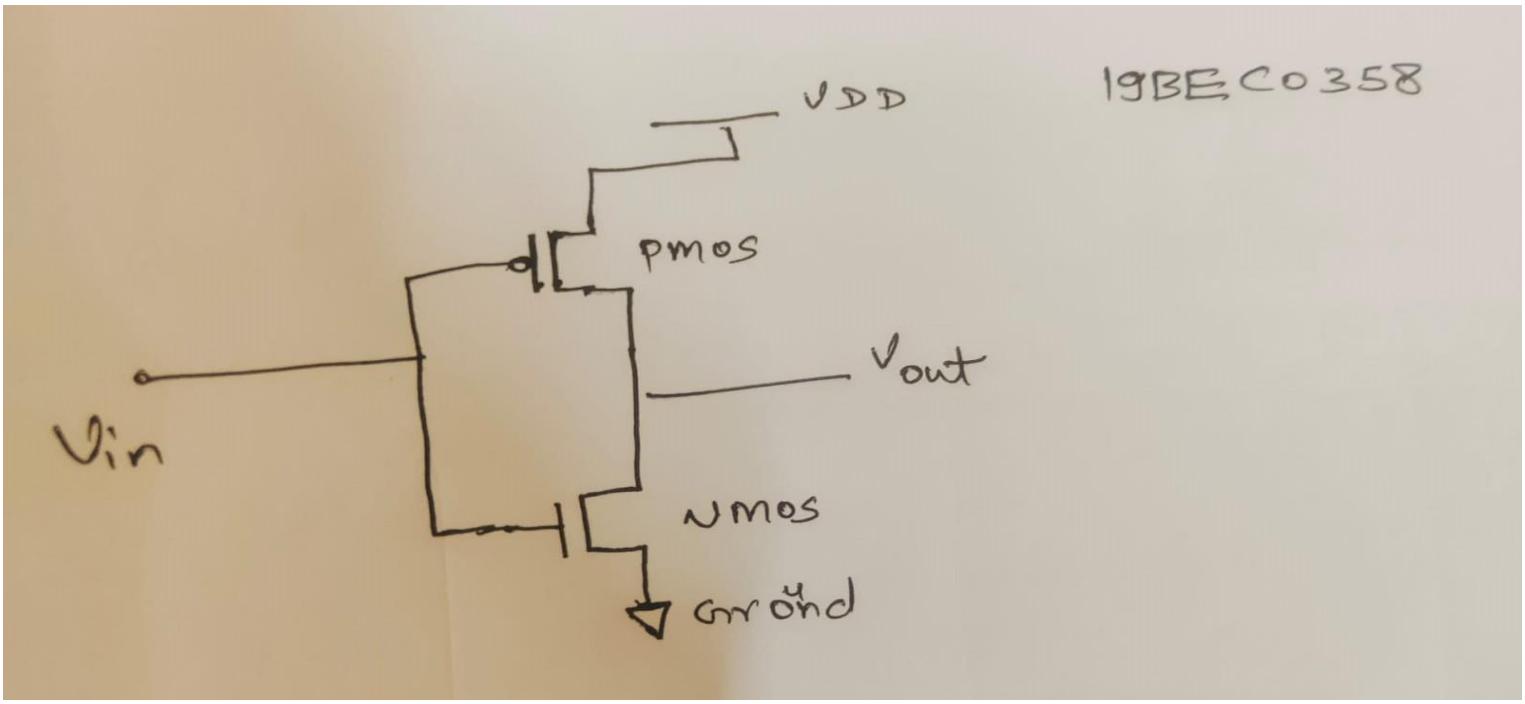
Aim → to plot the voltage transfer characteristics of CMOS inverter

Circuit Diagram → length = 180 nm, Width = 400nm(PMOS and NMOs)









Threshold voltage = 598.89mV (at PMOS width of 400nm)

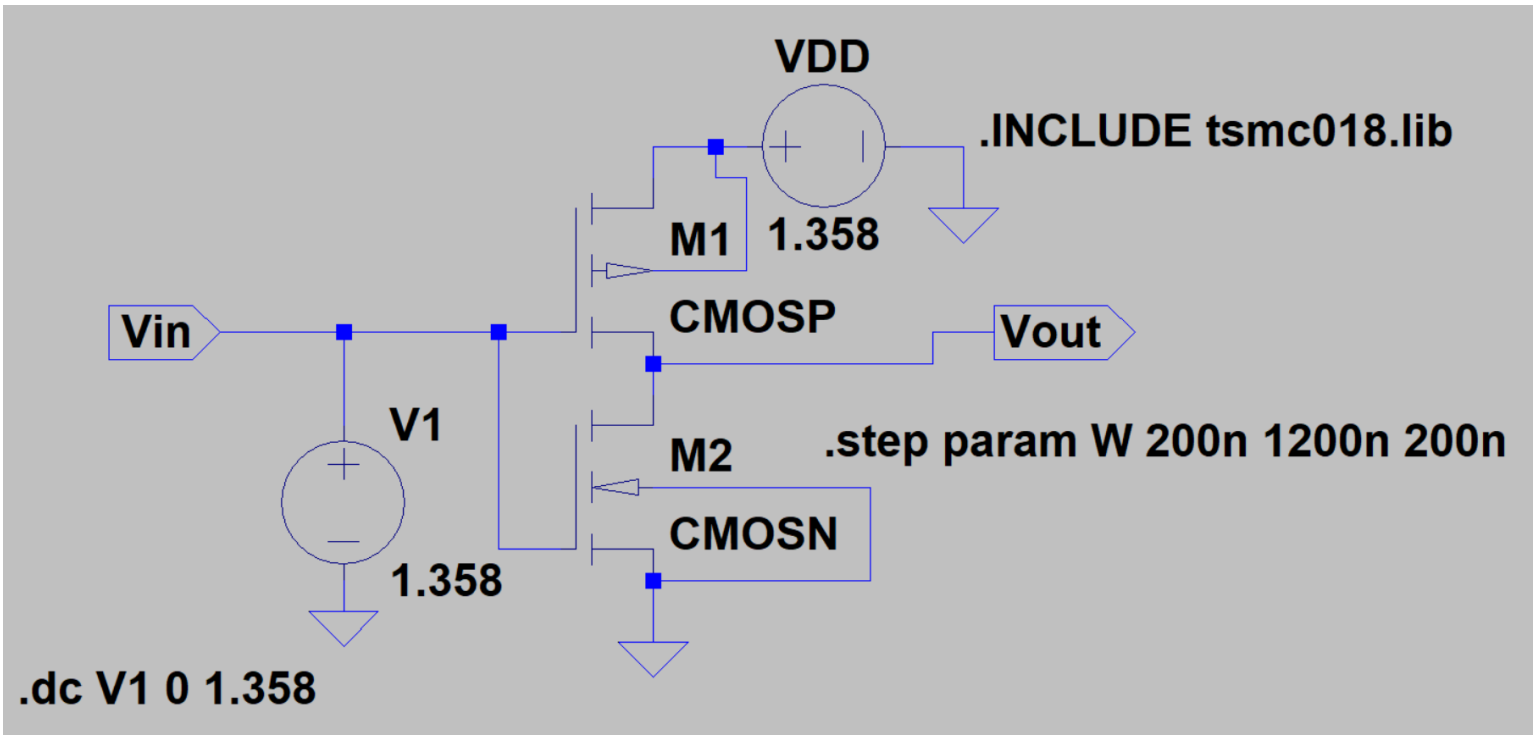
Result →

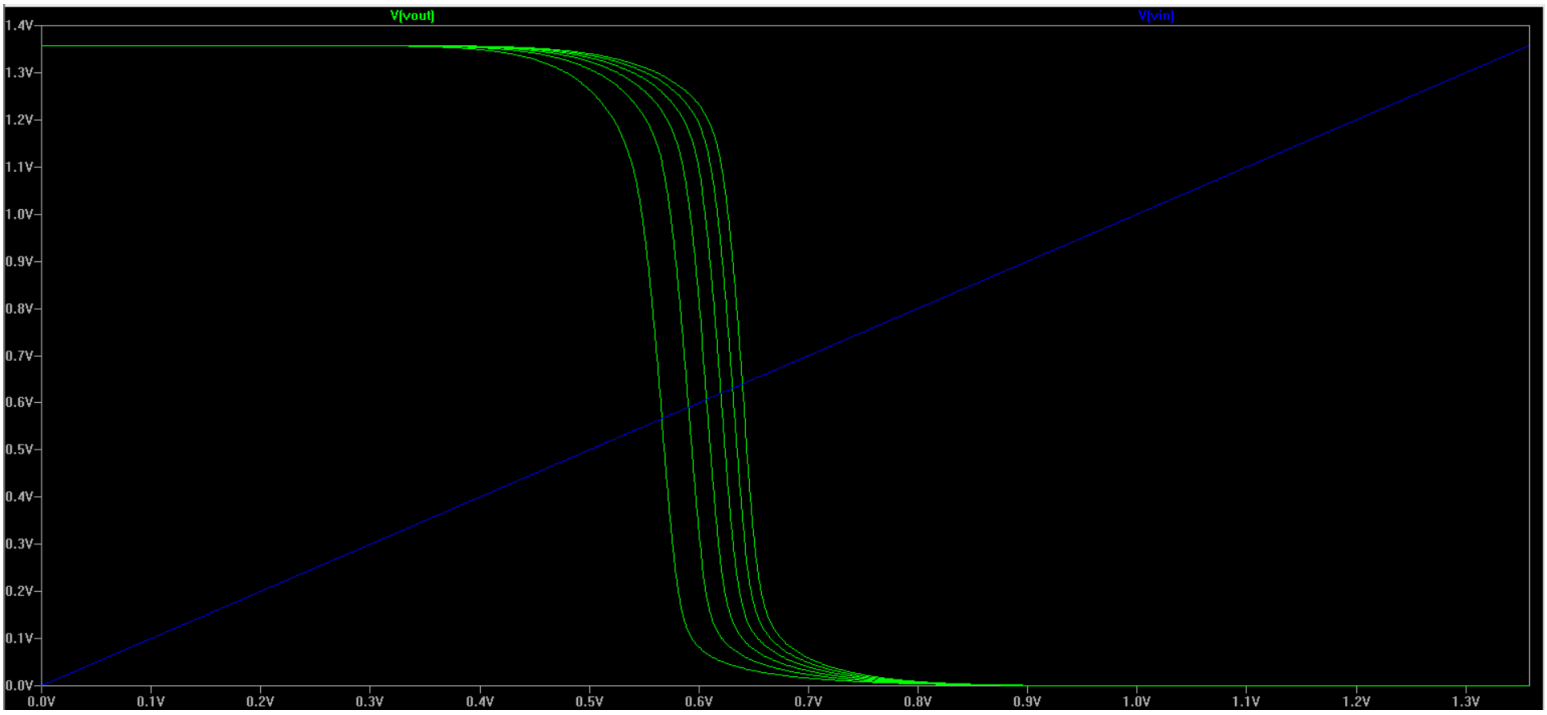
Threshold voltage is expected to be half of VDD. Here I took VDD = 1.358 so expected threshold voltage is 0.679mV but due to value of width of PMOS it is less than expected (598mV approx.). Hence, I was able to visualize the DC characteristics of CMOS inverter.

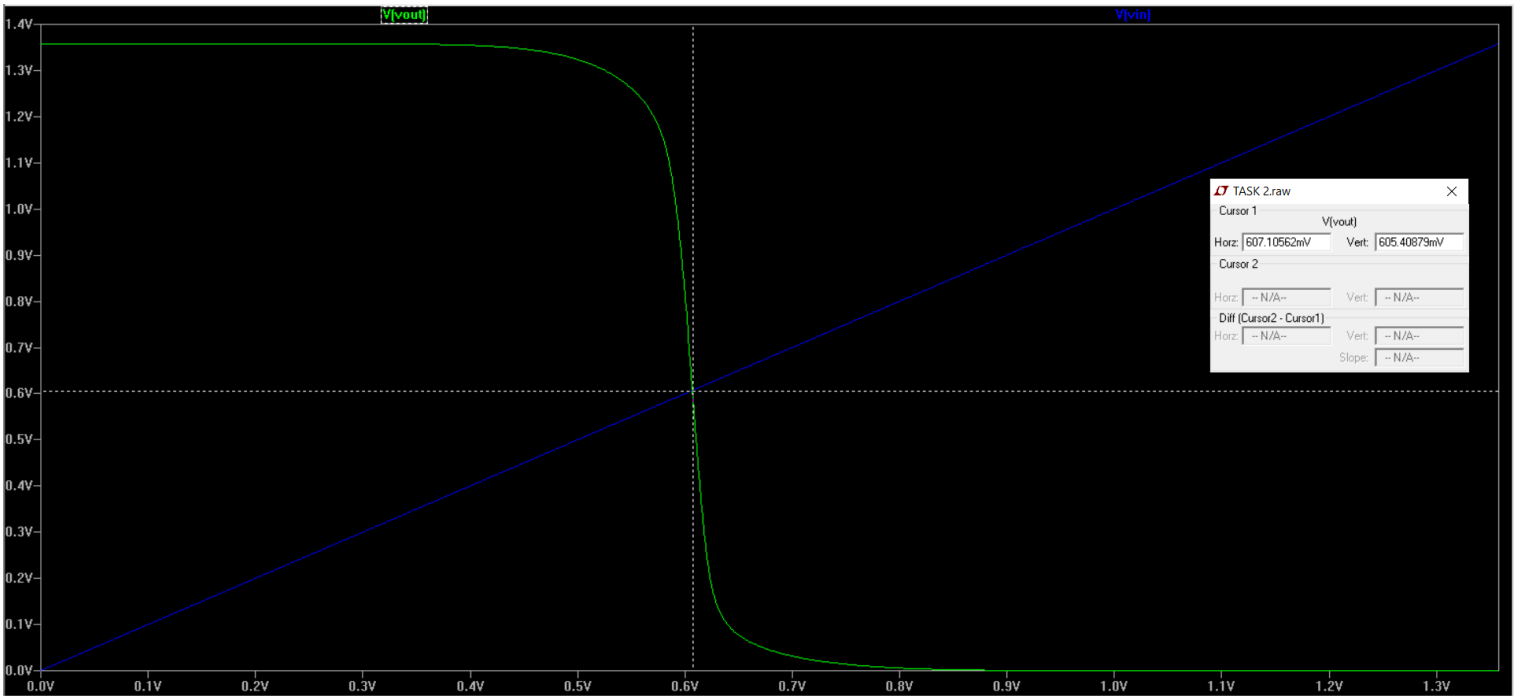
2).

Aim → to plot the voltage transfer characteristics of CMOS inverter for different width of PMOS

Circuit Diagram → length = 180 nm, Width (NMOS) = 400nm

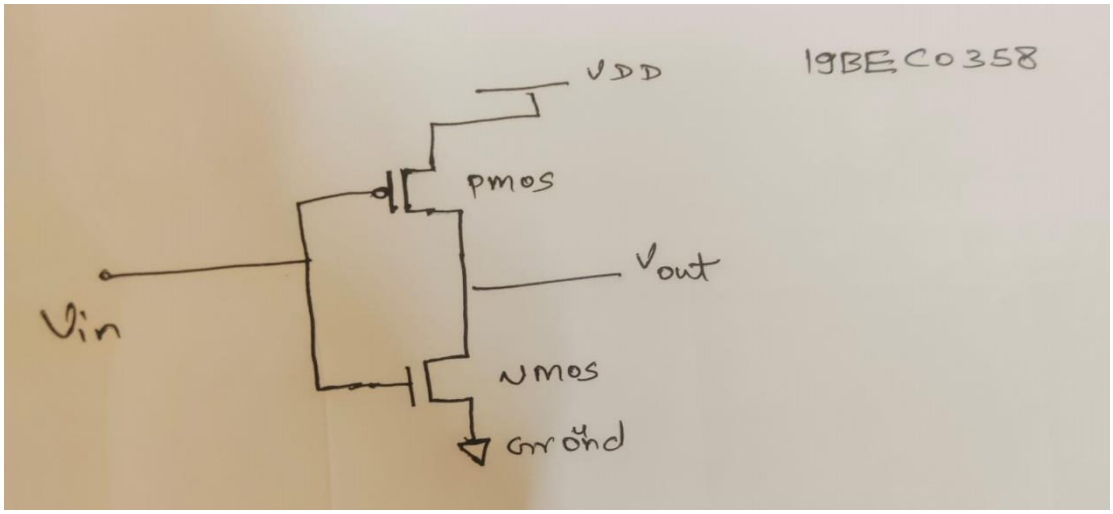






At 600nm width of PMOS ↑

S. No.	PMOS Width	Threshold Voltage of the CMOS inverter
1	400n	598.89mV
2	600n	605.40mV
3	800n	620.23mV
4	1000n	634.61mV
5	1200n	639.73mV



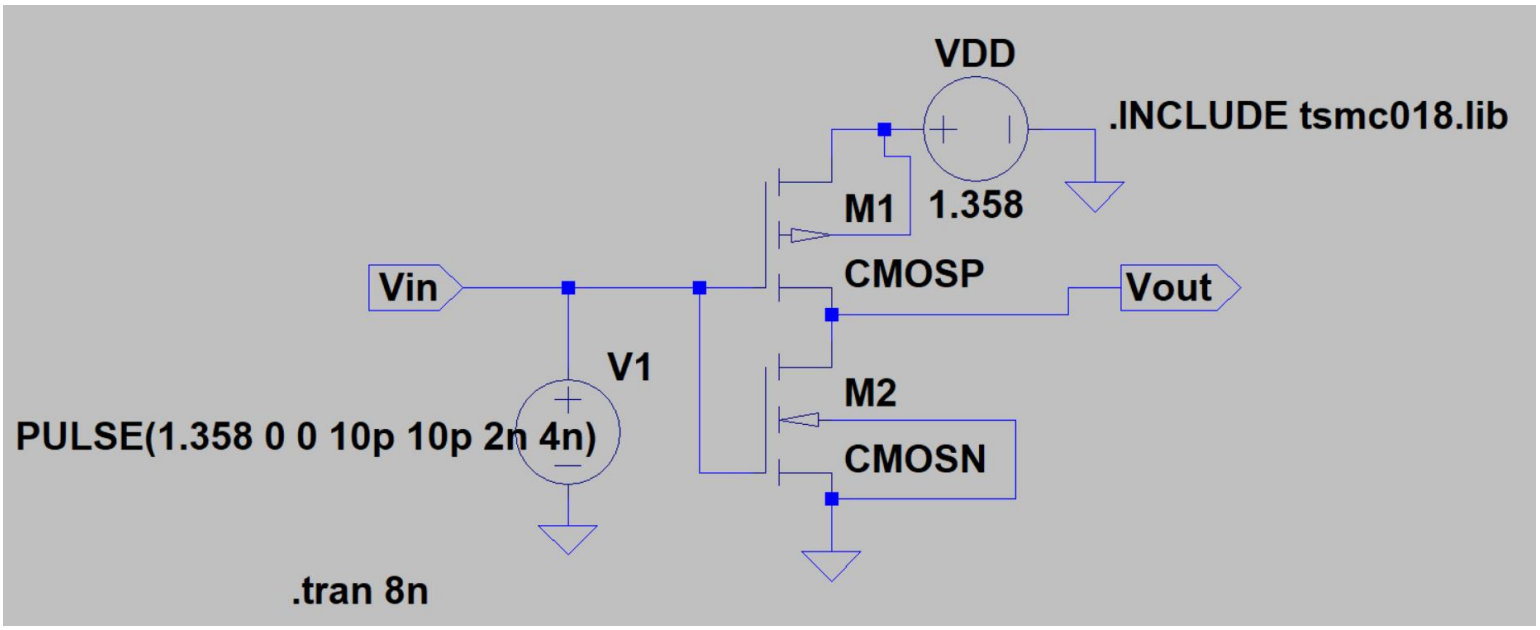
Result →

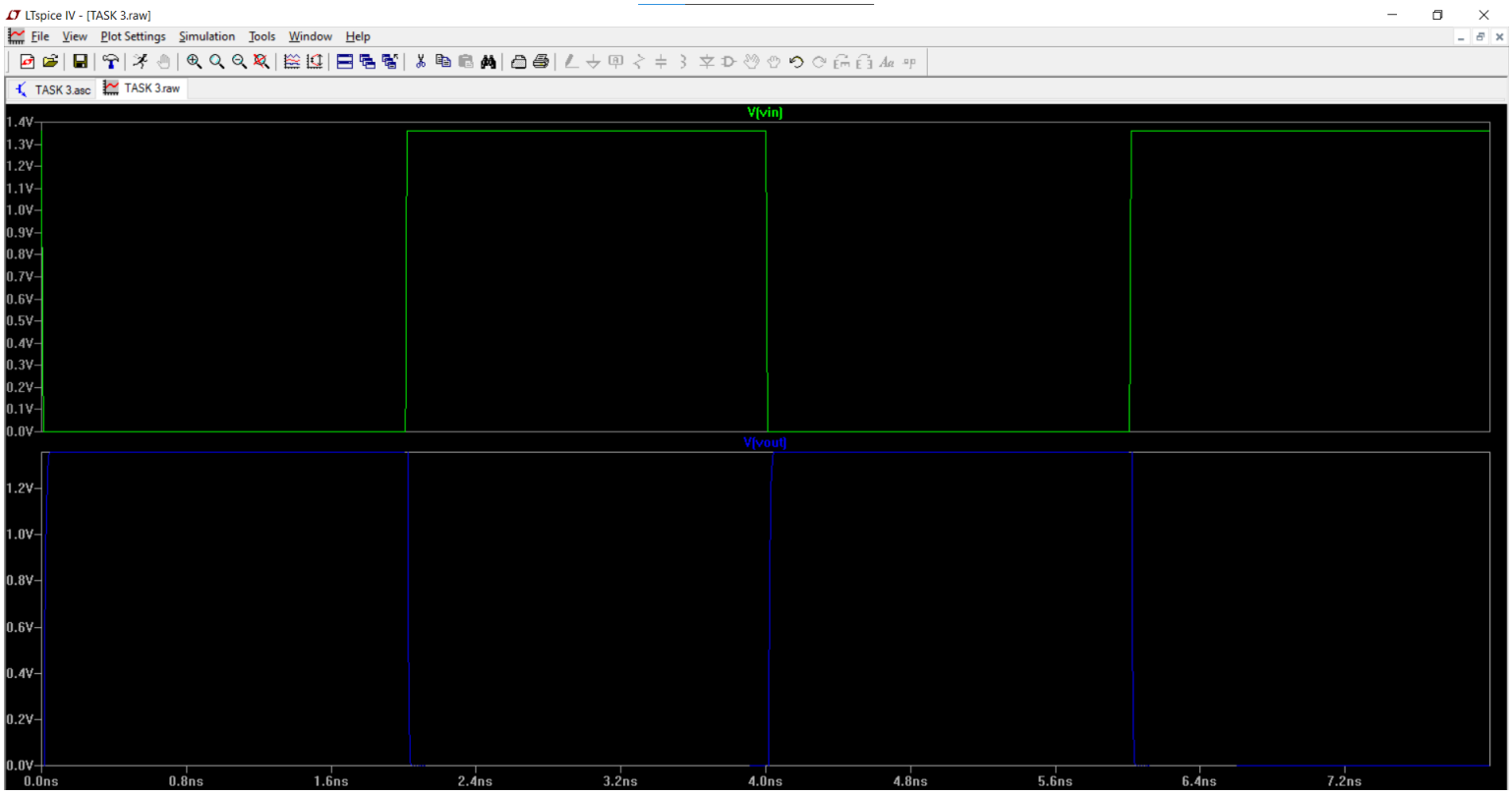
As the width of PMOS starts increasing, the threshold voltage of inverter also increases.

3).

Aim → to plot the Pulse input inverter characteristics

Circuit Diagram → length = 180 nm, Width (NMOS) = 400nm, Width (PMOS) = 400n

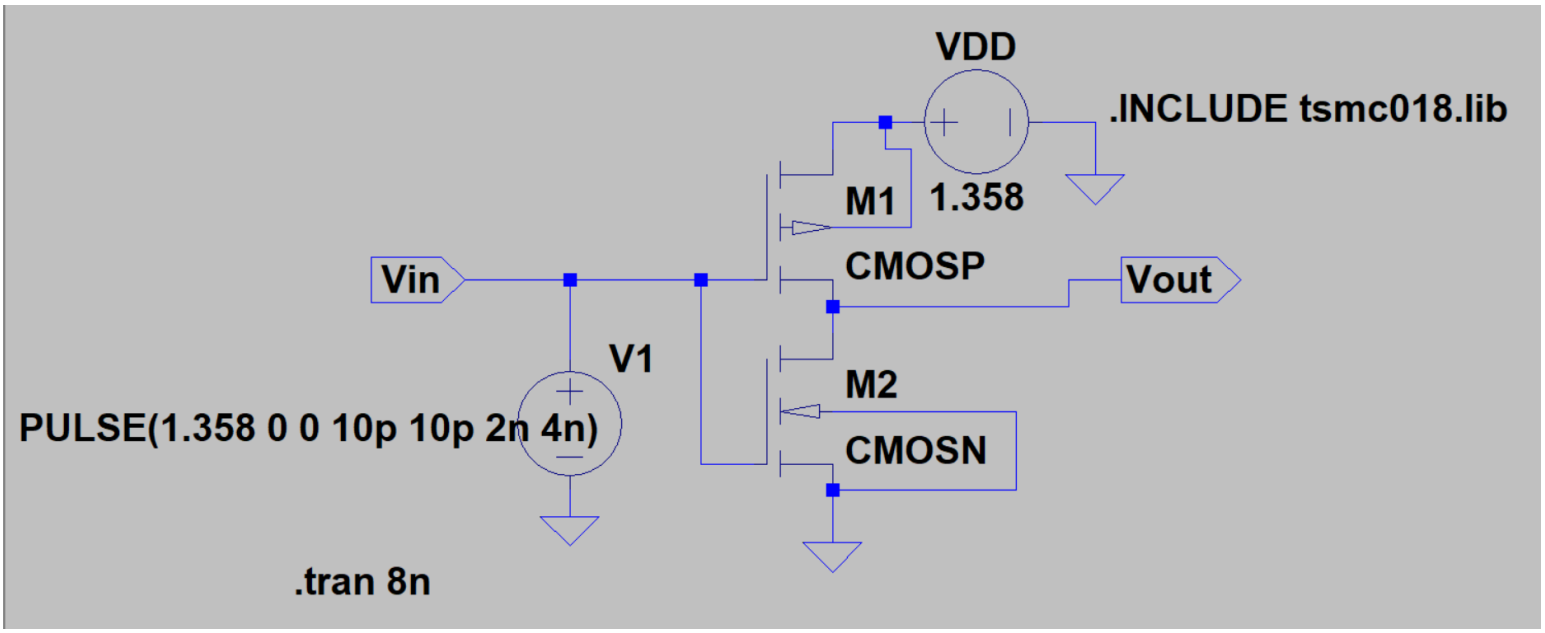


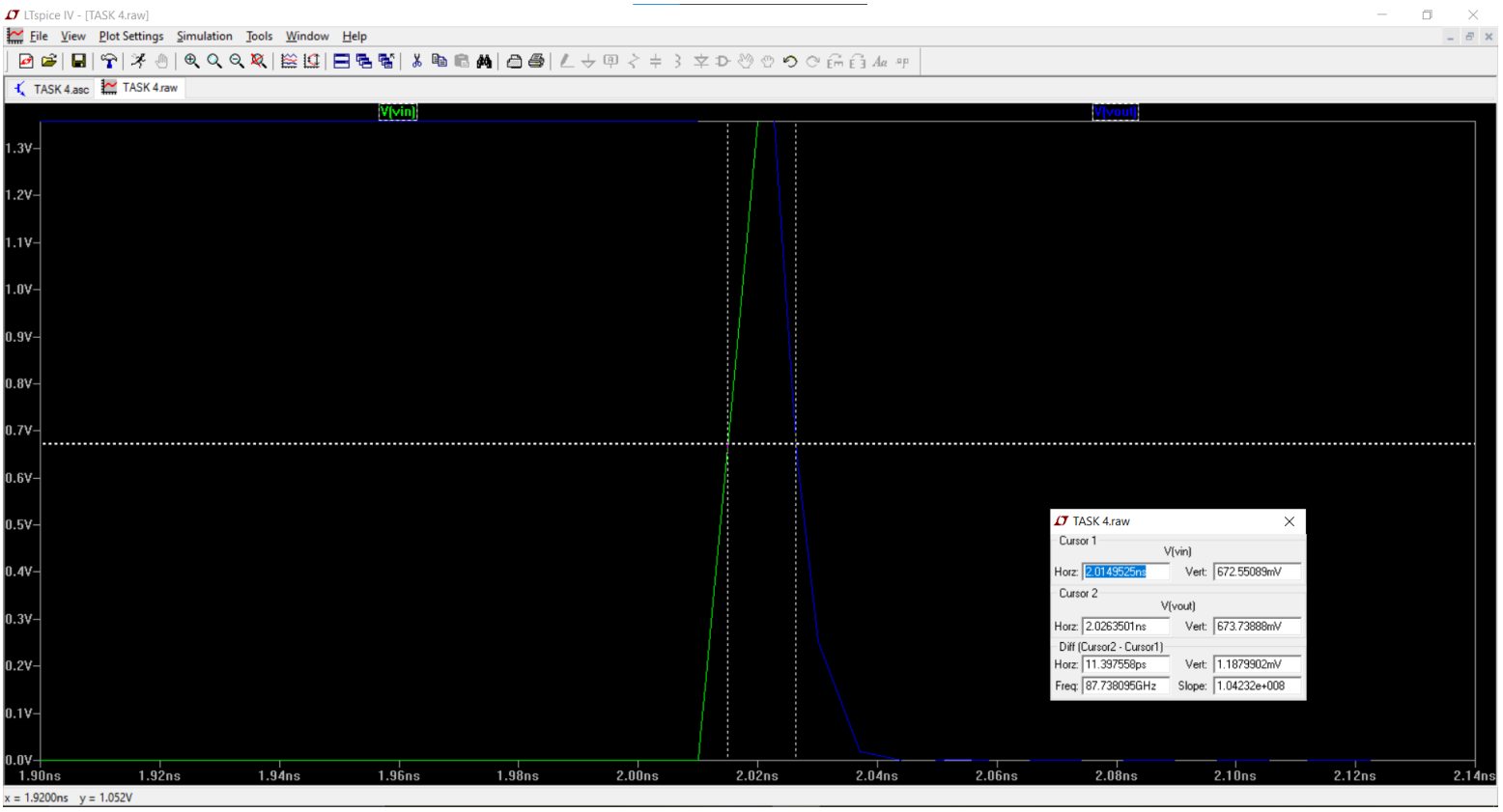


Result → CMOS inverter output waveform is as expected (compliment of input)

4).

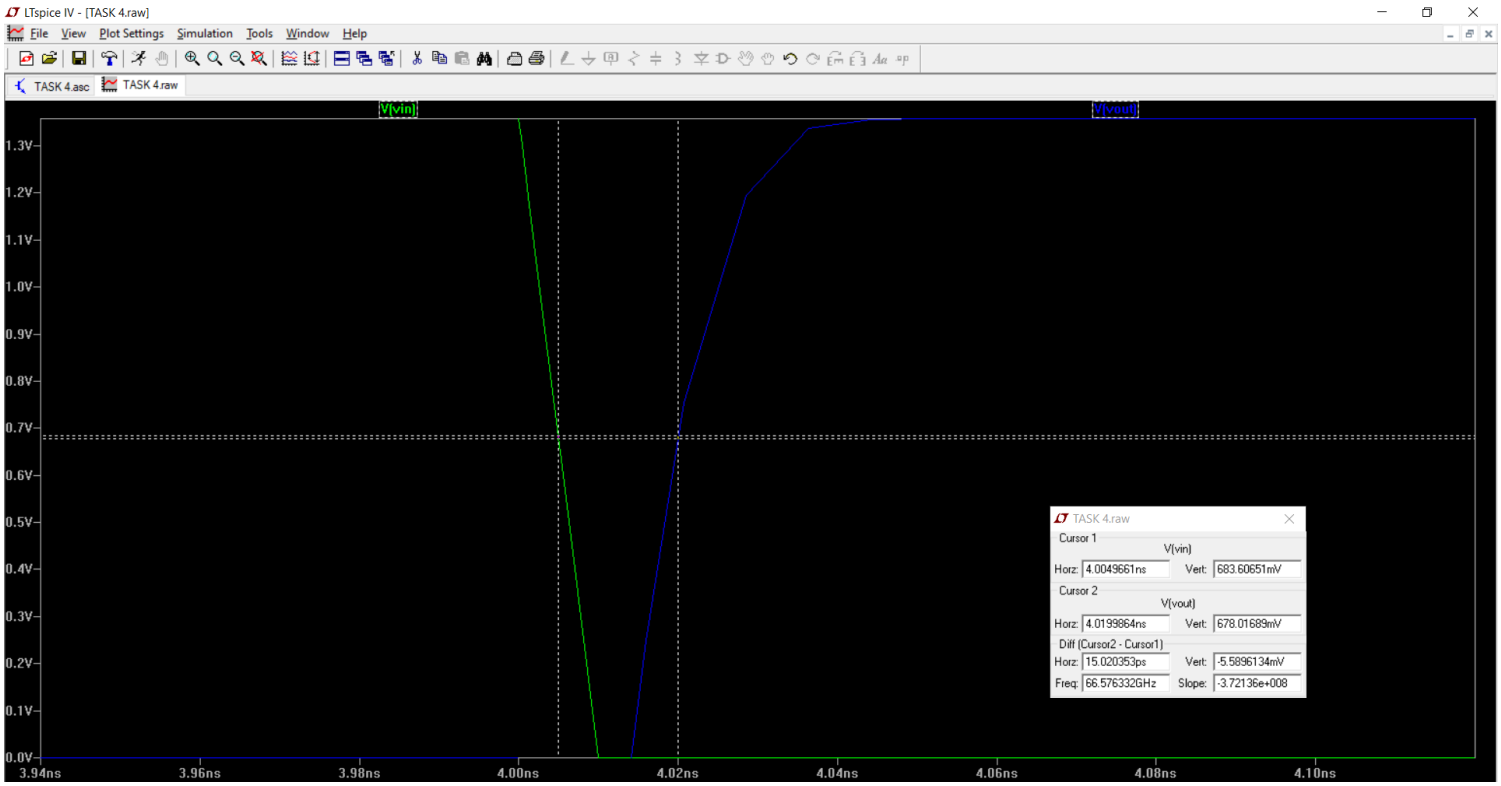
Aim → to find rise time, fall time and propagation delay





Green – input wave, blue – output wave

TPDF = 11.397ps



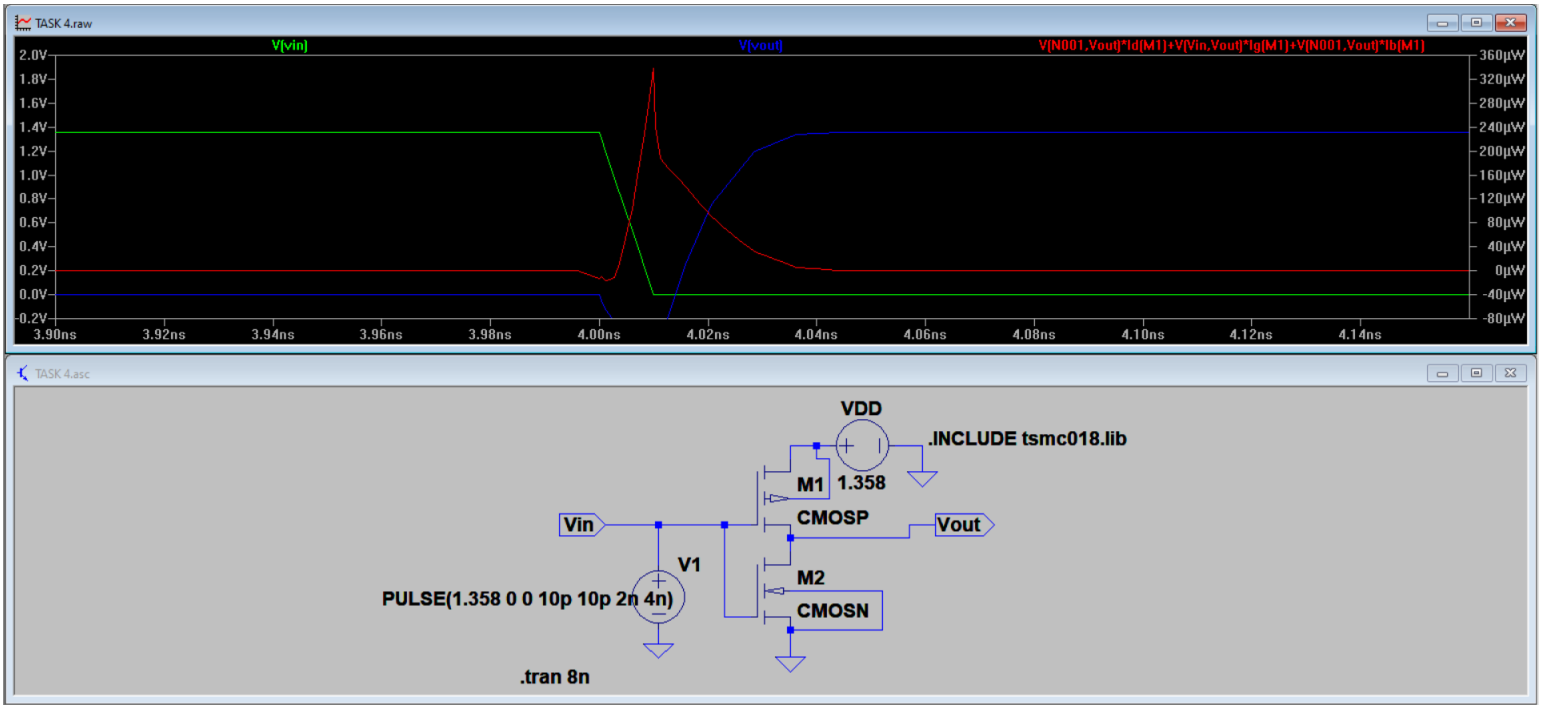
TPDR = 15.020ps

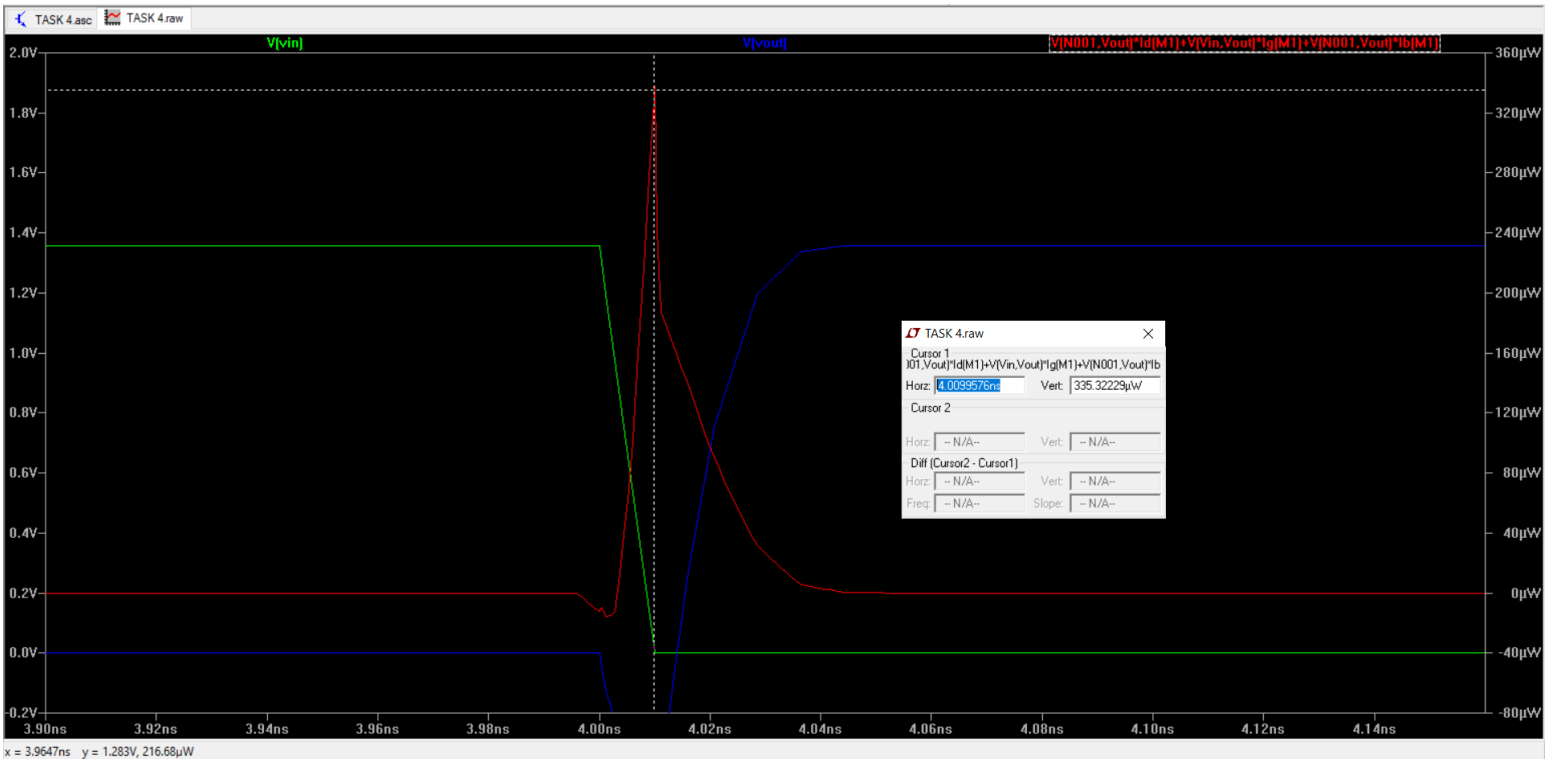
TPDF	11.397ps
TPDR	15.020ps
Propagation delay TPD	13.2085ps

Result → TPD is average of TPDF and TPDR

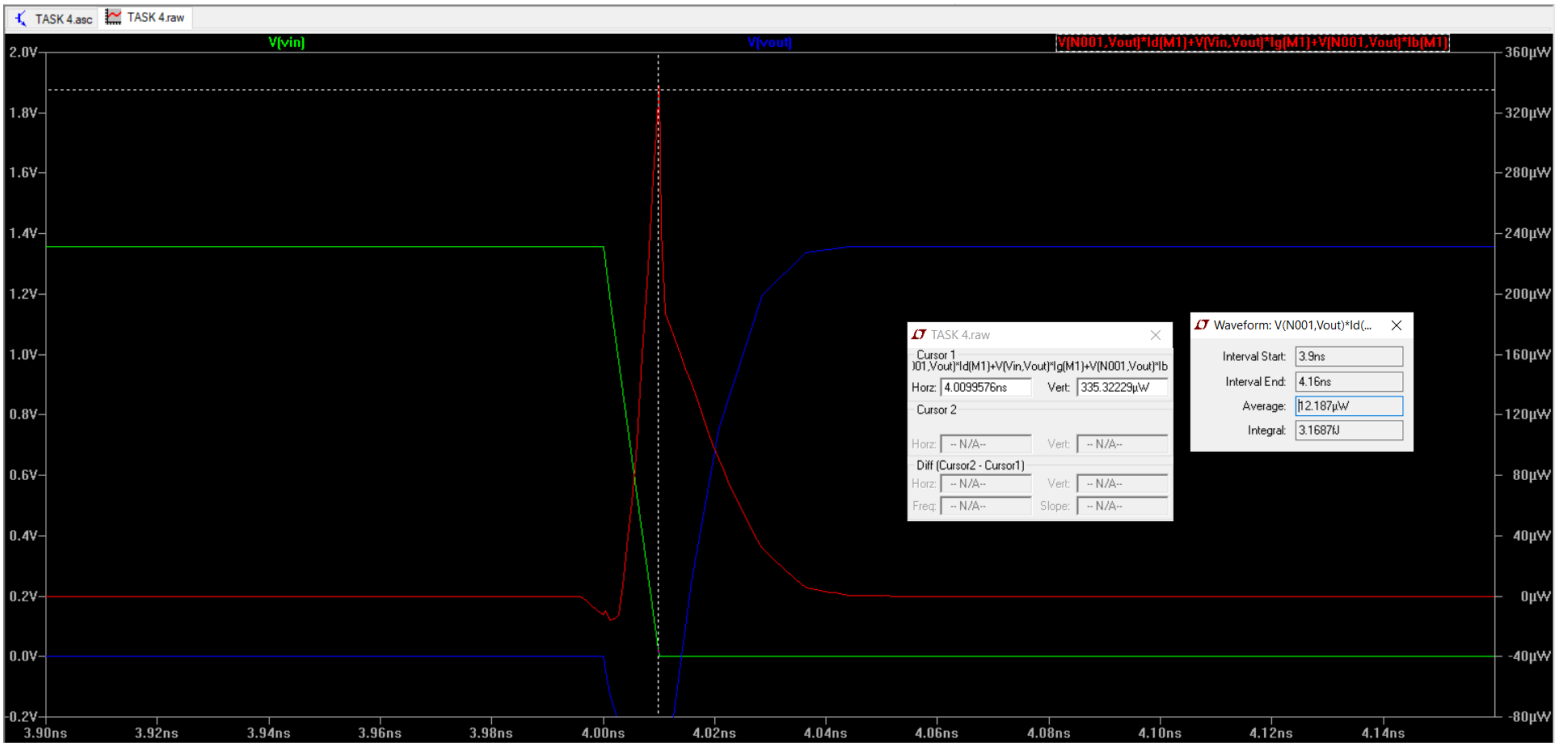
3).

Aim → to plot output power signal and observe peak and average power





Peak power = 335.32micro watt



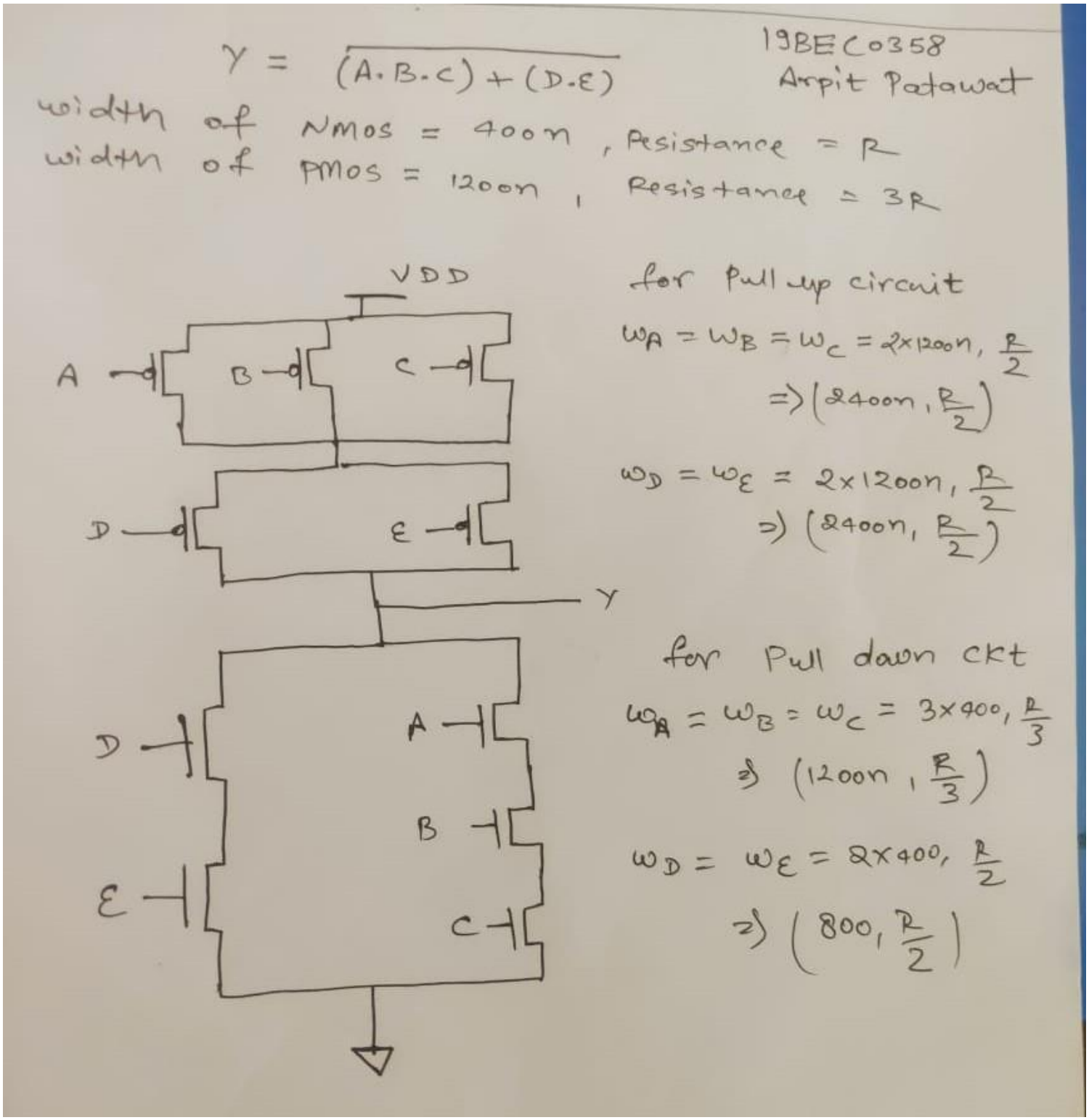
Average power = 12.187micro watt

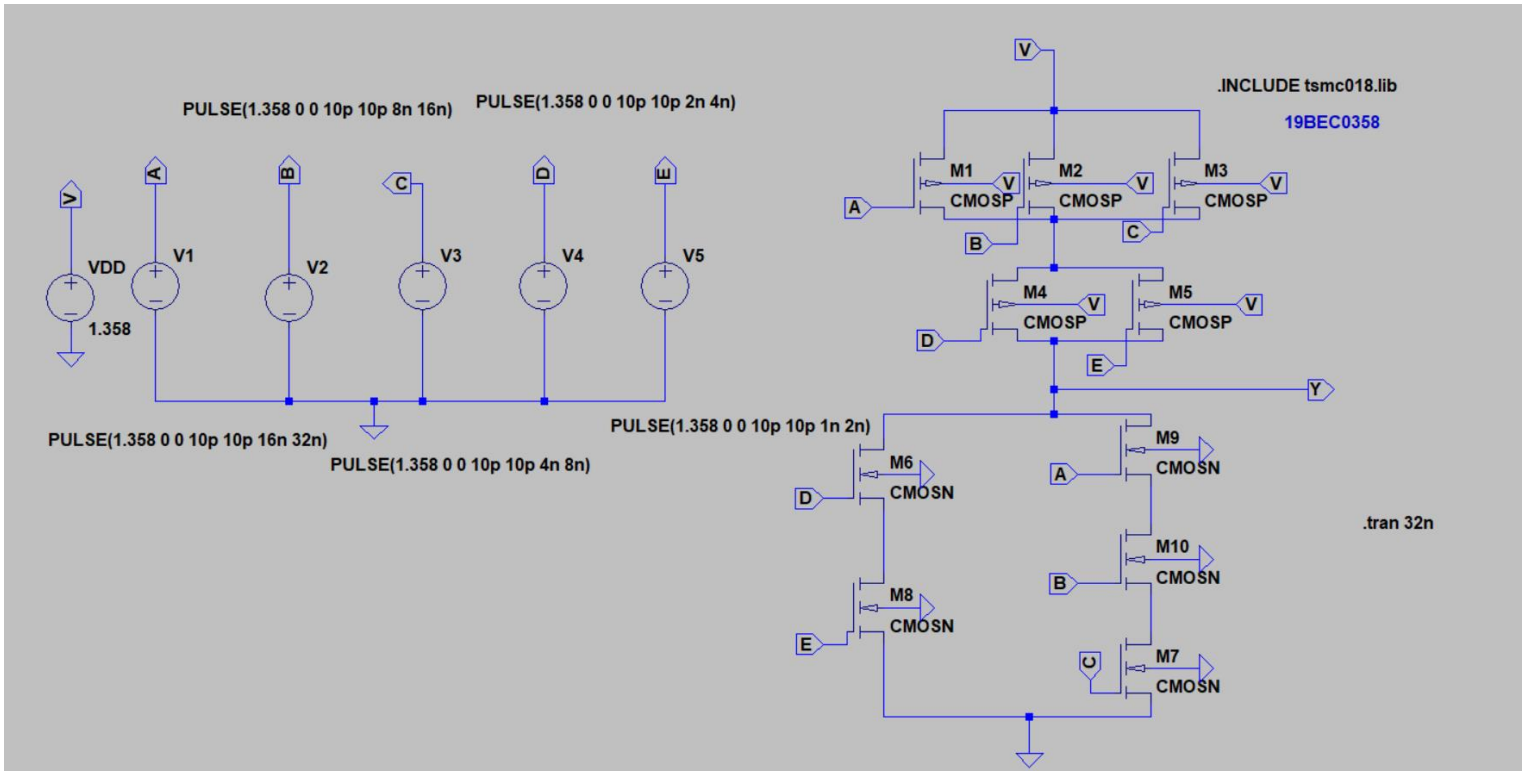
5)

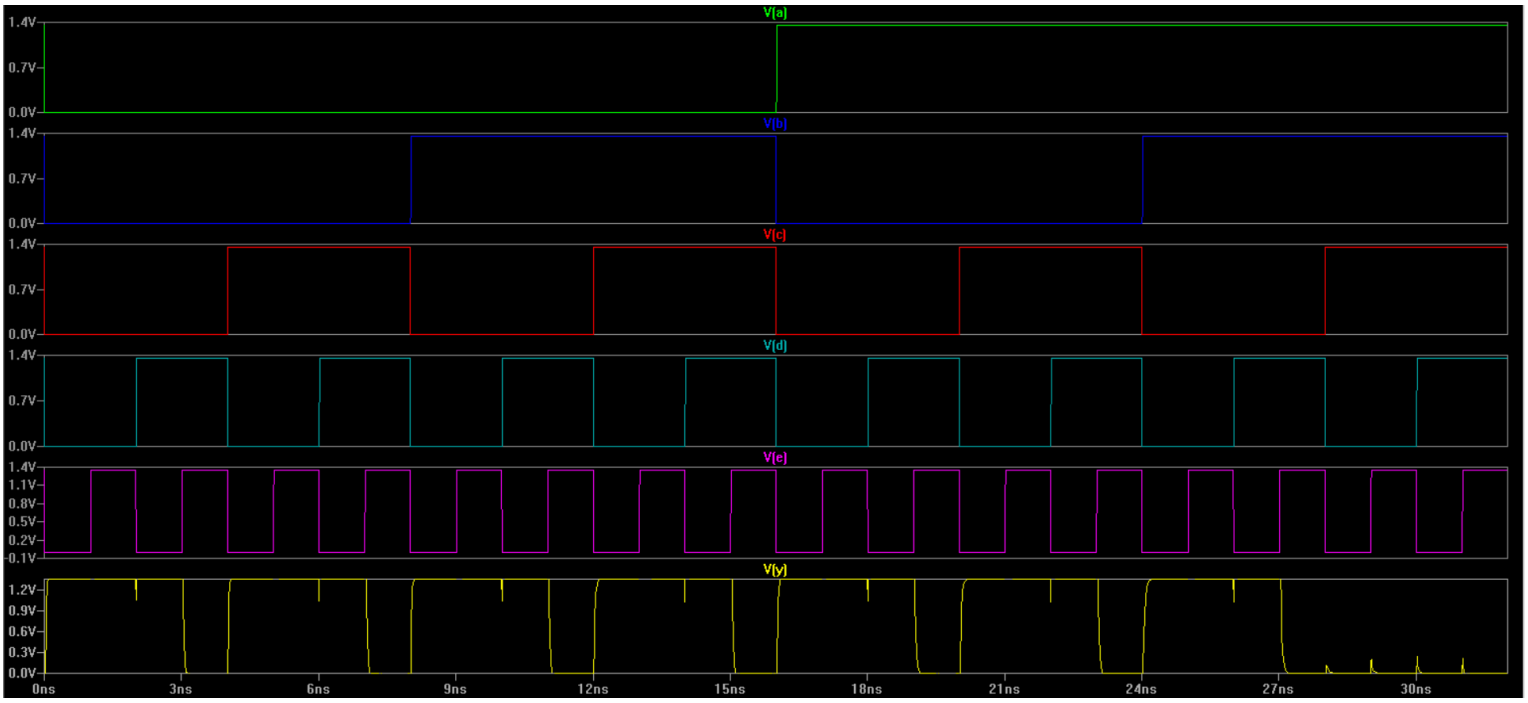
Aim → to design a 5-variable function

Circuit Diagram → length = 180 nm,

Here I took Y = ((A.B.C) + (D.E))' function




PULSE(1.358 0 0 10p 10p 8n 16n)
PULSE(1.358 0 0 10p 10p 2n 4n)
VDD
1.358
V1
V2
V3
V4
V5
PULSE(1.358 0 0 10p 10p 16n 32n)
PULSE(1.358 0 0 10p 10p 4n 8n)
PULSE(1.358 0 0 10p 10p 1n 2n)
.INCLUDE tsmc018.lib
19BEC0358
M1 CMOSP
M2 CMOSP
M3 CMOSP
M4 CMOSP
M5 CMOSP
M6 CMOSN
M7 CMOSN
M8 CMOSN
M9 CMOSN
M10 CMOSN
.tran 32n


V(a)
V(b)
V(c)
V(d)
V(e)
V(y)
0ns
3ns
6ns
9ns
12ns
15ns
18ns
21ns
24ns
27ns
30ns

Truth Table →

A	B	C	D	E	Y
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	0

Result → our final output waveform matches with truth table. Hence, we were successfully able to build circuit using CMOS design.

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