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Reg.No	19BEC0358		
Student Name	ARPIT PATAWAT		
Course Code	ECE3002	**Slot & Semester**	L43+L44 WINTER -- 2021-22
Course Name	VLSI system design		
Program Title	Lab Assignment 2		
Faculty	Dr. Ragunath G		

School of Electronics Engineering ,VIT, Vellore

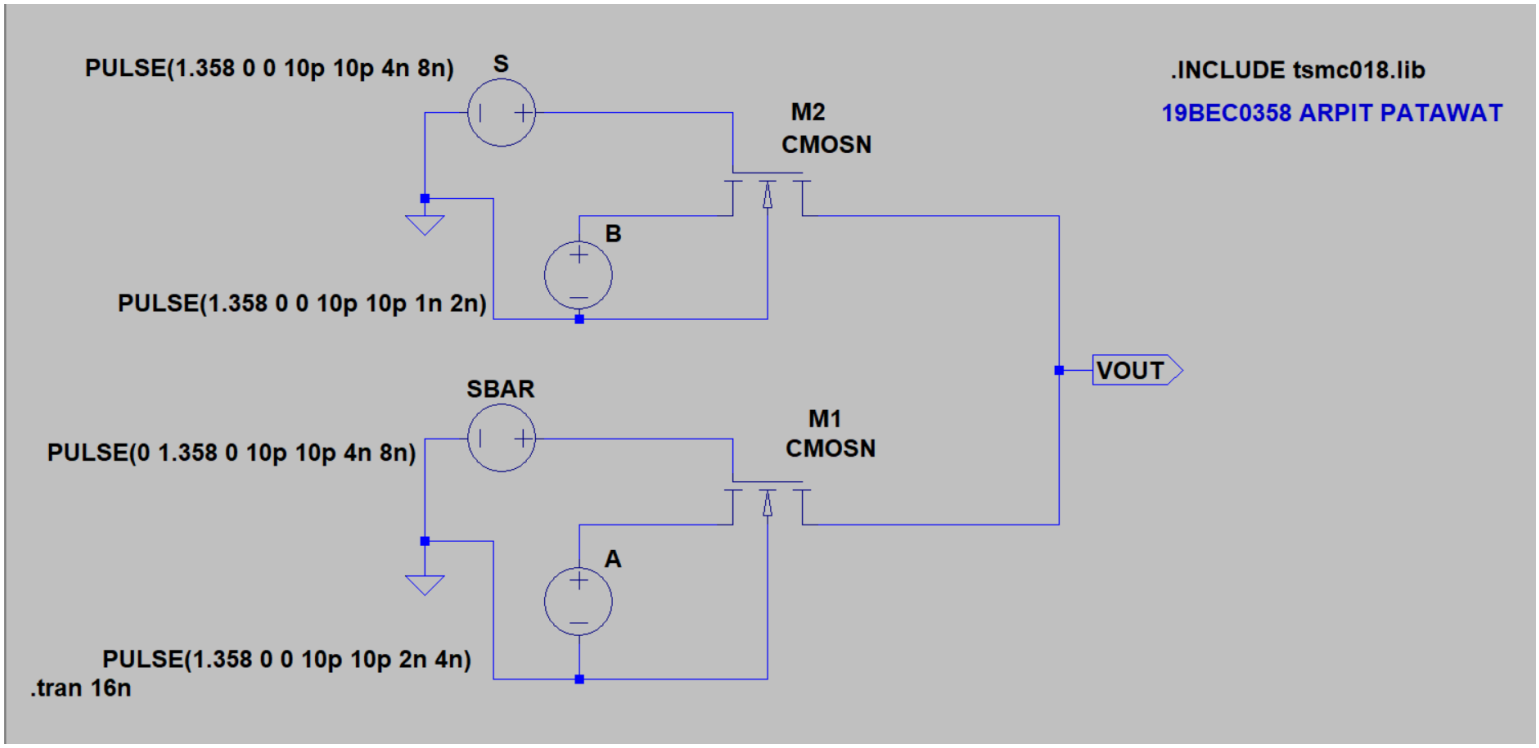
1. Design a 2 input MUX using Pass Transistor Logic (using NMOS)

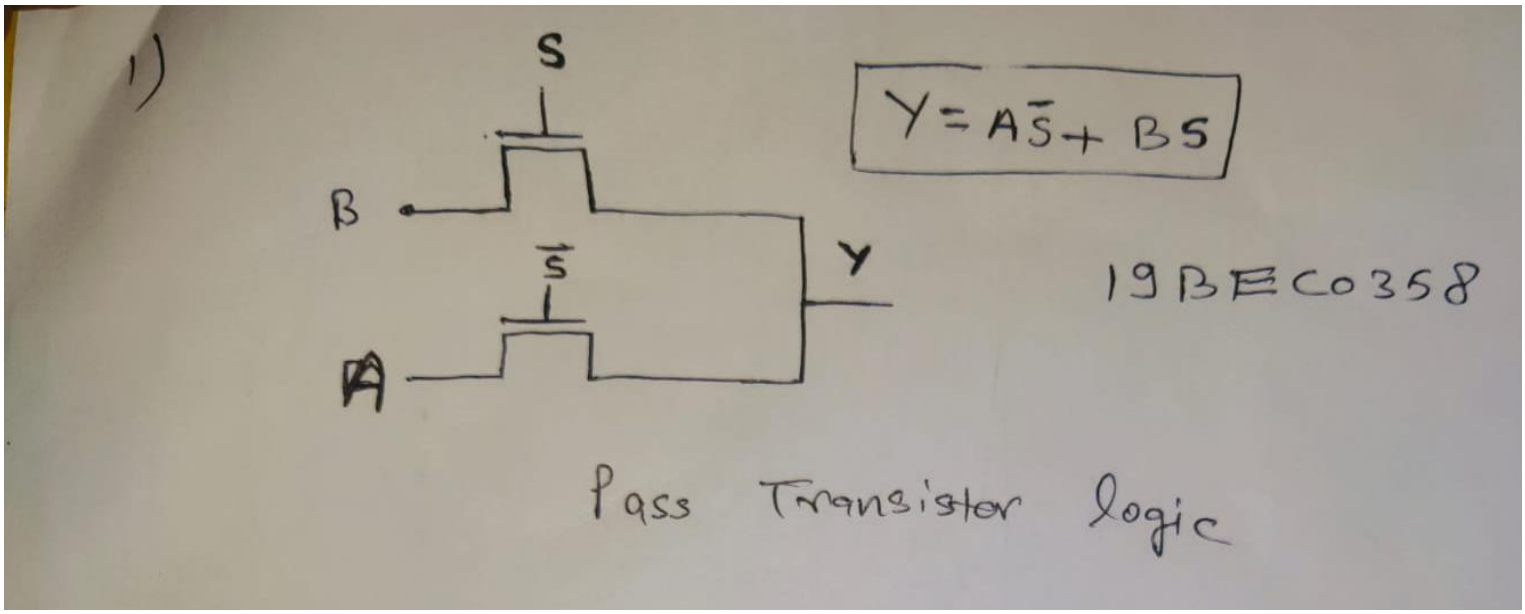
2. Design a 2 input MUX using Transmission Gate Logic.

1).

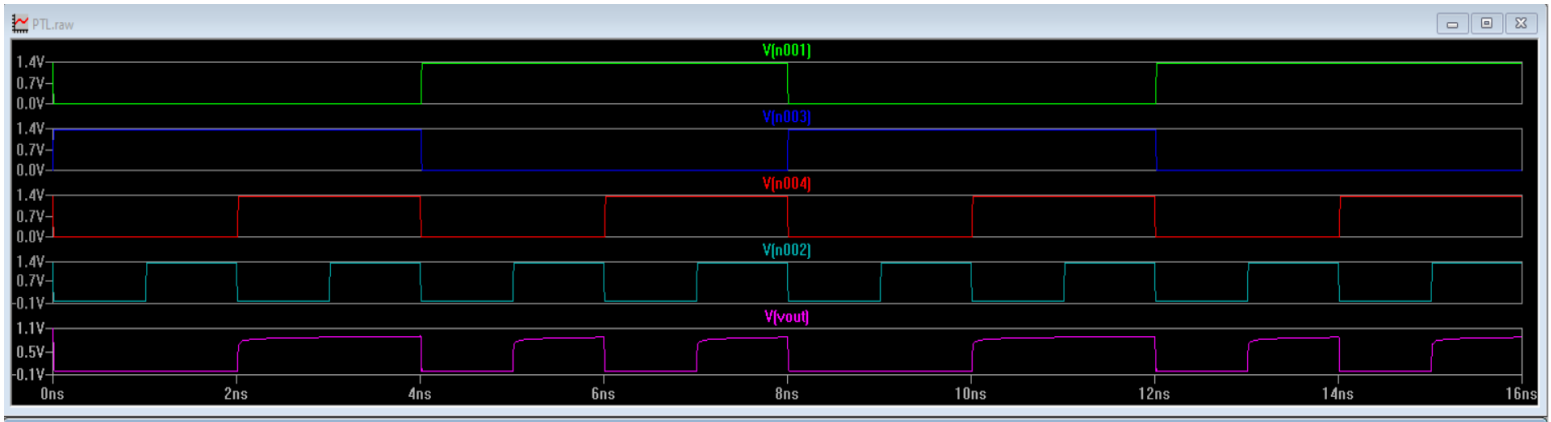
Aim → to design MUX using pass transistor logic

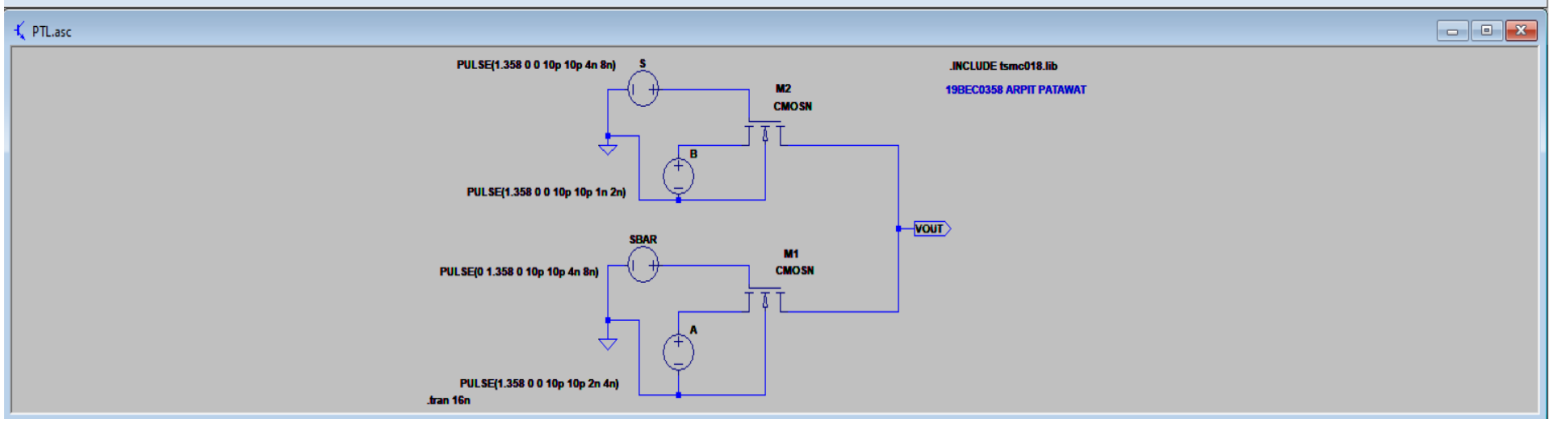
Circuit Diagram → Width = length = 180 nm





Simulation →


PTL.raw
V(n001)
1.4V
0.7V
0.0V
V(n003)
1.4V
0.7V
0.0V
V(n004)
1.4V
0.7V
0.0V
V(n002)
1.4V
0.7V
-0.1V
V(vout)
1.1V
0.5V
-0.1V
0ns
2ns
4ns
6ns
8ns
10ns
12ns
14ns
16ns


PTL.asc
PULSE(1.358 0 0 10p 10p 4n 8n)
S
M2
CMOSN
B
PULSE(1.358 0 0 10p 10p 1n 2n)
VOUT
SBAR
M1
CMOSN
PULSE(0 1.358 0 10p 10p 4n 8n)
A
PULSE(1.358 0 0 10p 10p 2n 4n)
.tran 16n
.INCLUDE tsmc018.lib
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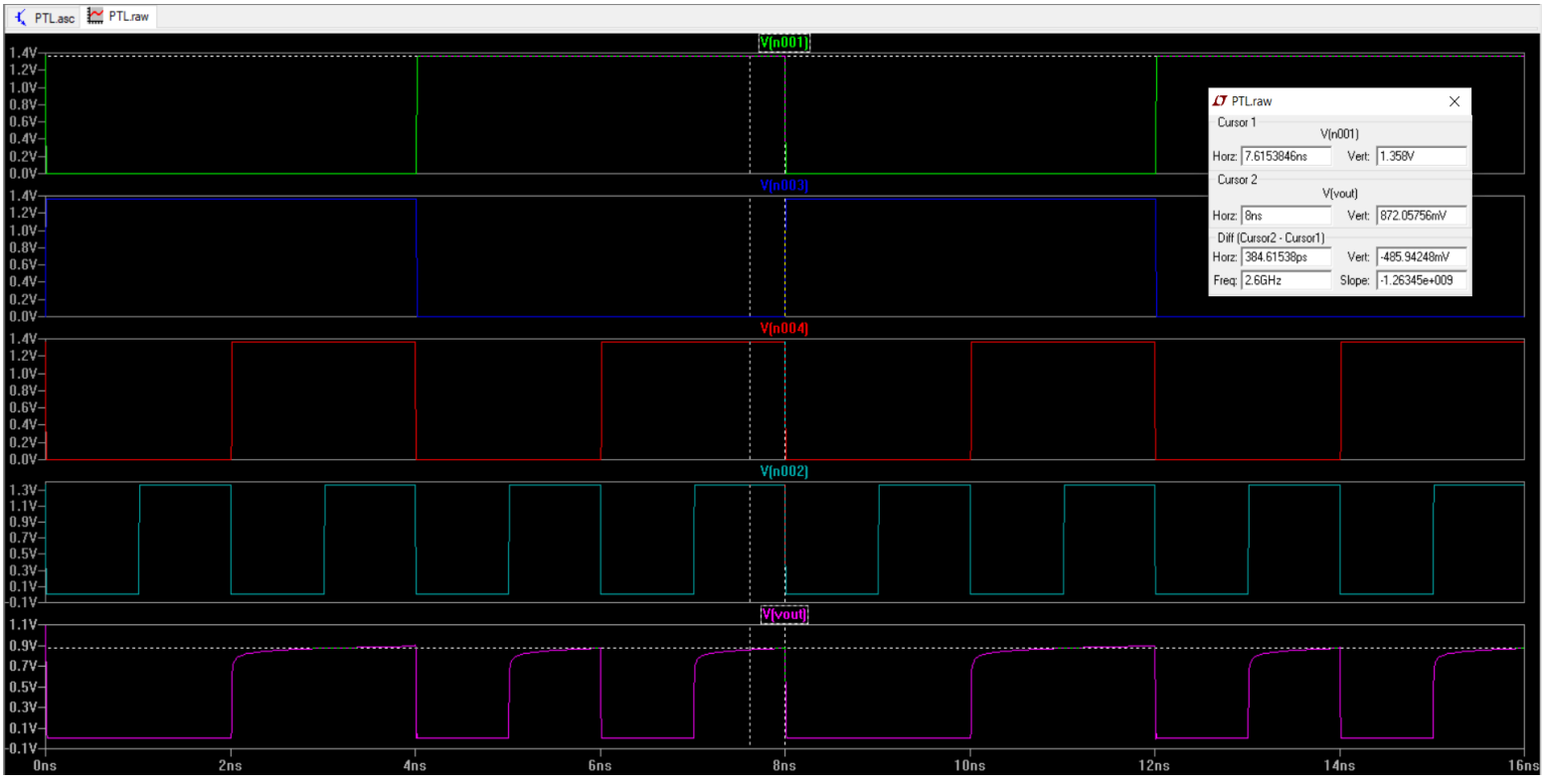

PTL.asc
PTL.raw
V(n001)
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(n003)
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(n004)
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(n002)
1.3V
1.1V
0.9V
0.7V
0.5V
0.3V
0.1V
-0.1V
V(vout)
1.1V
0.9V
0.7V
0.5V
0.3V
0.1V
-0.1V
0ns
2ns
4ns
6ns
8ns
10ns
12ns
14ns
16ns
PTL.raw
Cursor 1
V(n001)
Horz: 7.6153846ns
Vert: 1.358V
Cursor 2
V(vout)
Horz: 8ns
Vert: 872.05756mV
Diff (Cursor2 - Cursor1)
Horz: 384.61538ps
Vert: -485.94248mV
Freq: 2.6GHz
Slope: -1.26345e+009

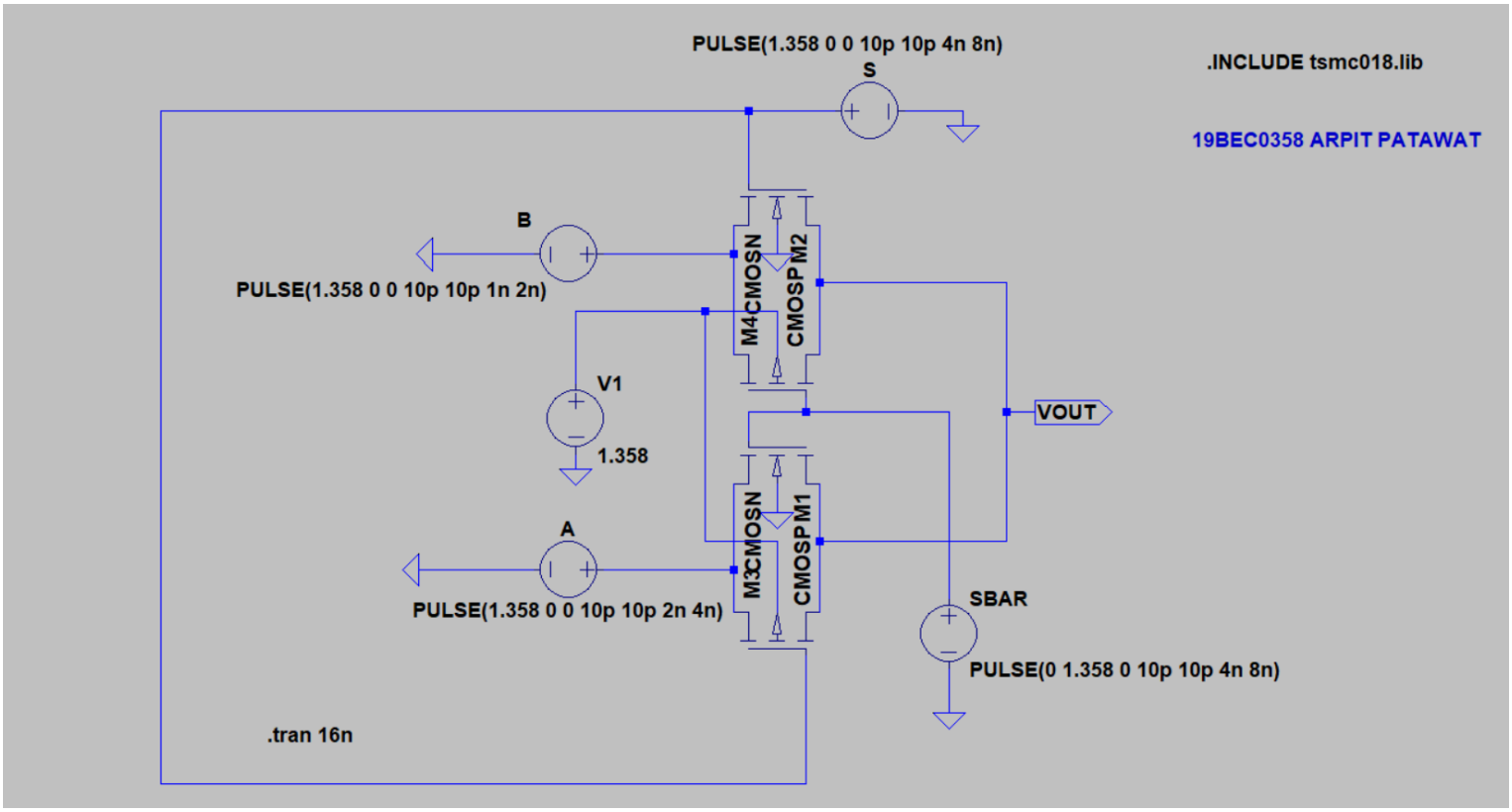
Result →

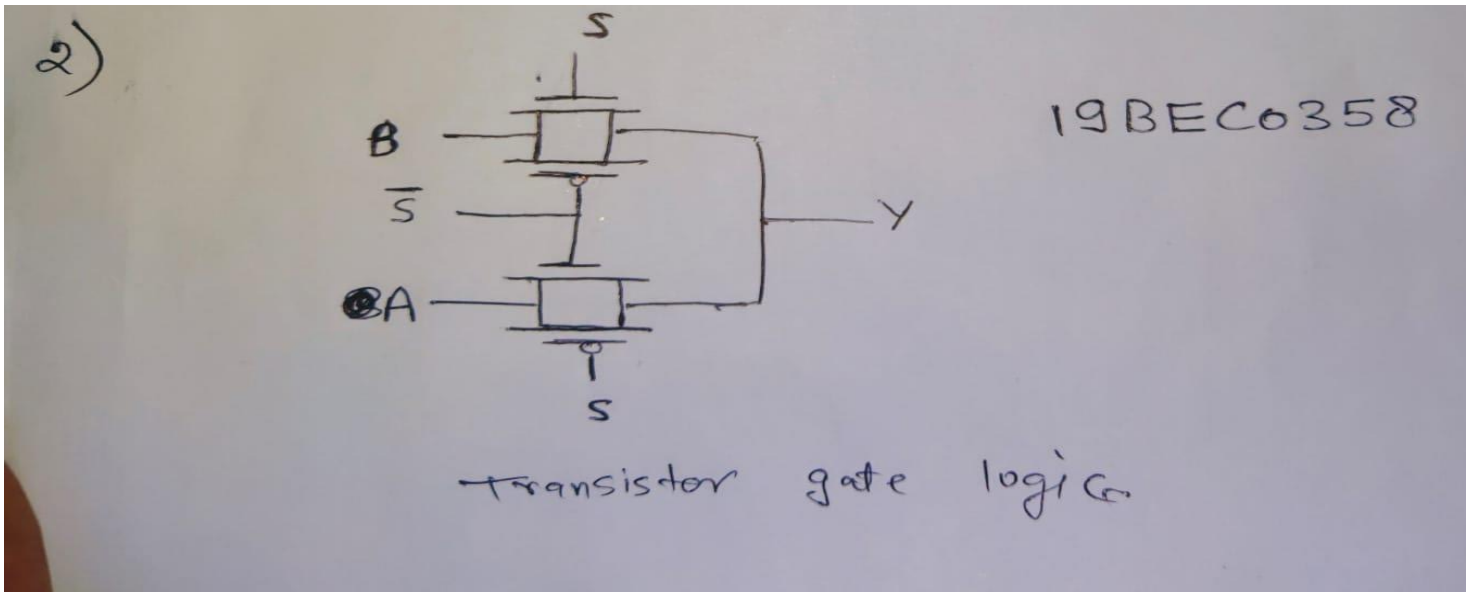
Here we can see 5 waves, which are Select line, compliment of select line, Input A, Input B and finally the Output B respectively. When Select line is 0 then output is A and when select line is 1 then output is B. since we are using pass transistor logic so we can expect degraded 1 output which can be seen as input is 1.358V(VDD) but output is 0.872V which is near to VDD – Vth or (1.358-0.45) V

2.

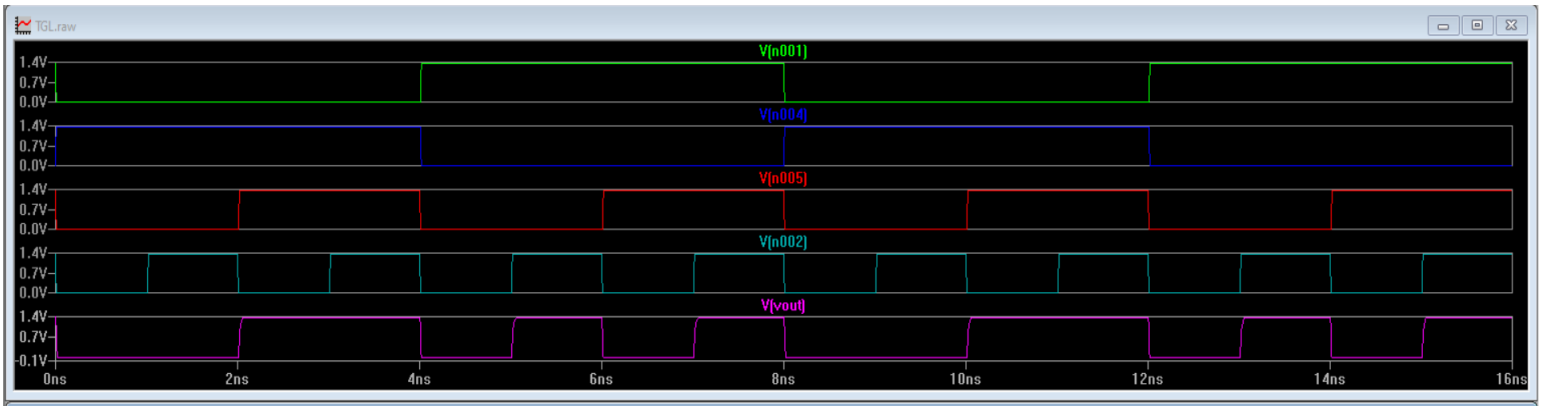
Aim → to design MUX using Transistor gate logic

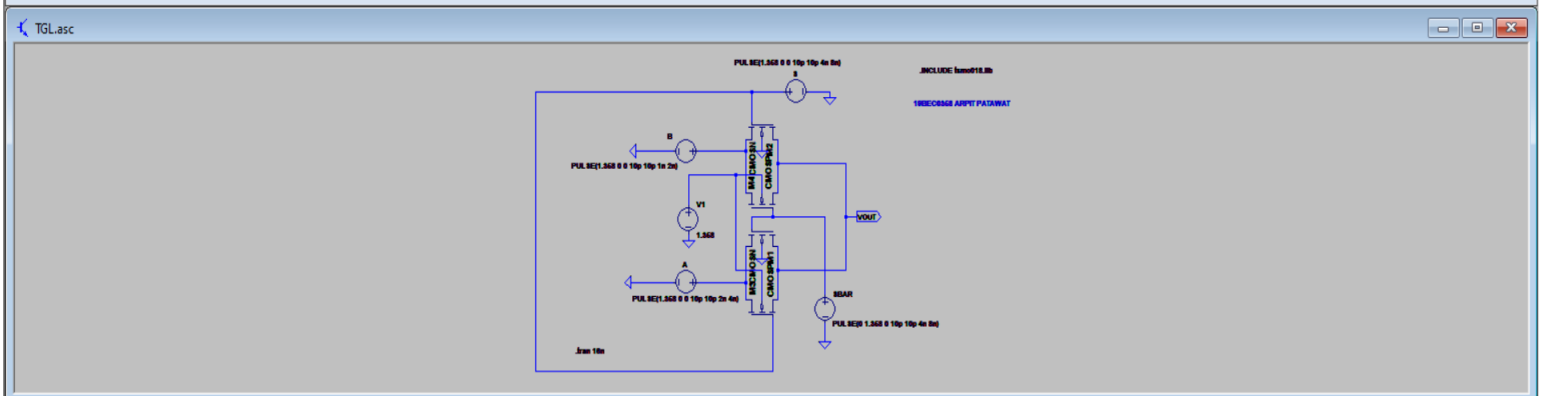
Circuit Diagram →

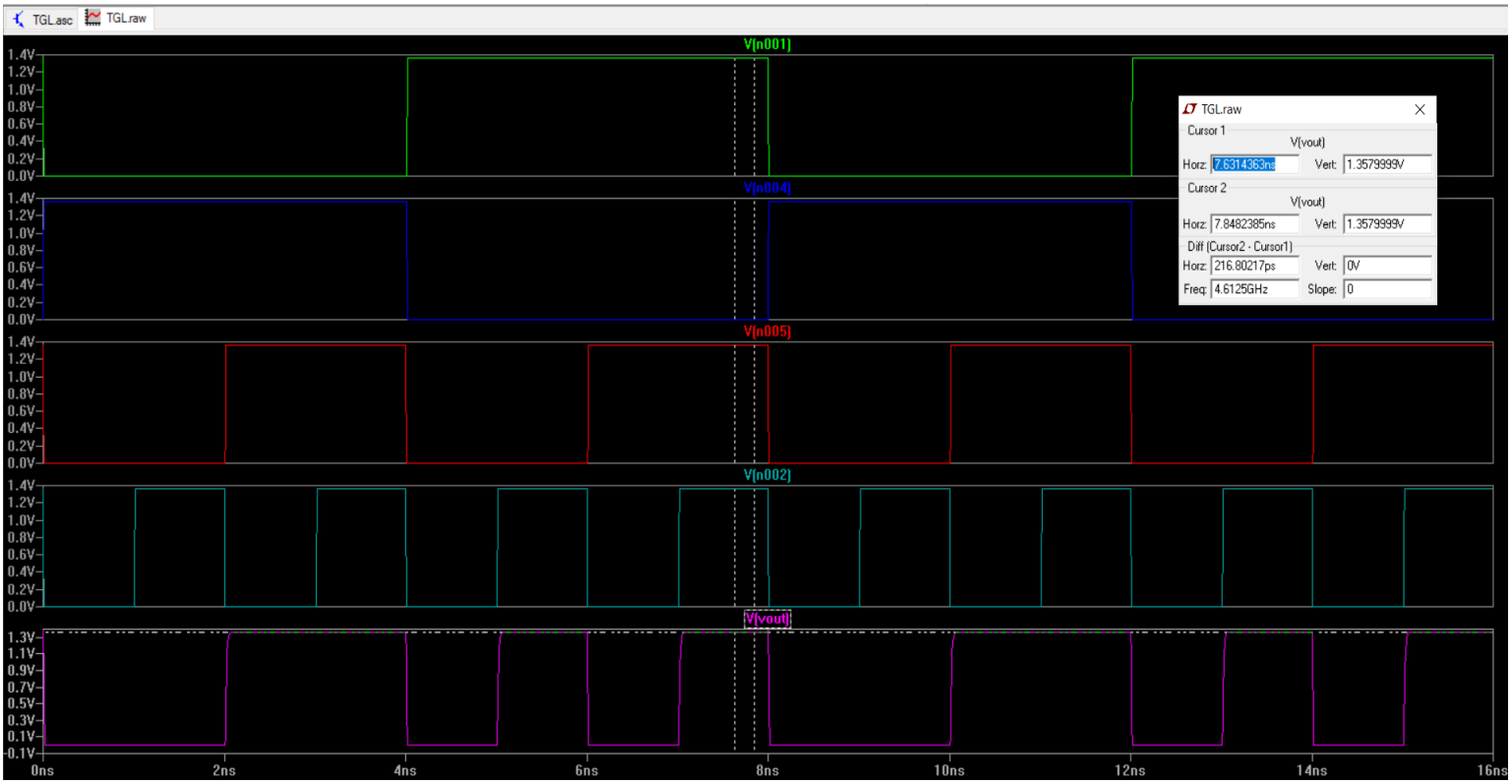



2)
S
B
S̄
A
S
Y
19BEC0358
transistor gate logic

Simulation →


TGL.raw
V(n001)
V(n004)
V(n005)
V(n002)
V(vout)
1.4V
0.7V
0.0V
-0.1V
0ns
2ns
4ns
6ns
8ns
10ns
12ns
14ns
16ns


TGL.asc
VOUT
V1
1.8V



Result →

Here we can see 5 waves, which are Select line, compliment of select line, Input A, Input B and finally the Output B respectively. When Select line is 0 then output is A and when select line is 1 then output is B. since we are using transistor gate logic so we can expect correct output VDD (1.358V).

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