

Futuristic Computational Model in the Era of NVRAM

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Arpit Gupta Advisor: Debadatta Mishra

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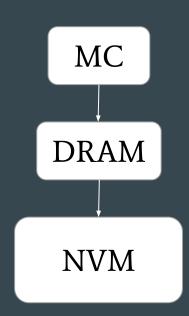
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Solution: **Hybrid Memory Systems**

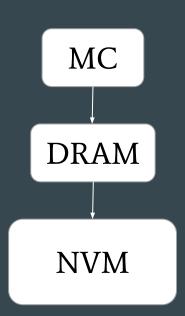
DRAM as a cache for the NVM

Capacity Loss



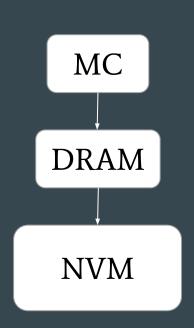
DRAM as a cache for the NVM

- Capacity Loss
- Bandwidth Loss



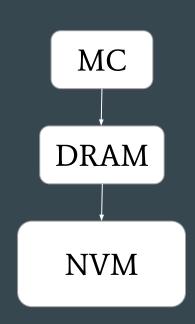
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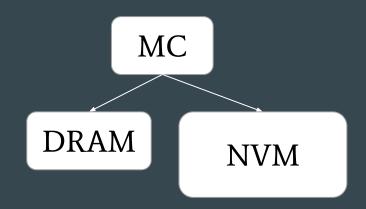
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- No OS changes required



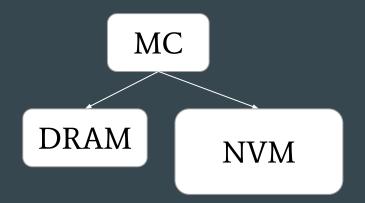
DRAM and NVM share a flat address space

More Capacity

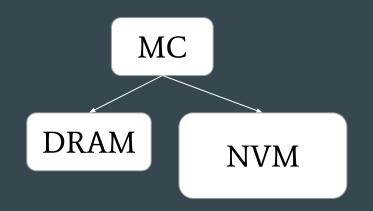


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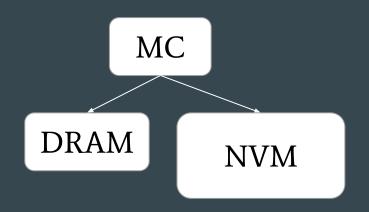


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DRAM and NVM share a flat address space

- More Capacity
- More Bandwidth
- No DRAM changes
- OS support is helpful



Surveys show that hardware and software issues needs to be tackled for successful integration of NVMs

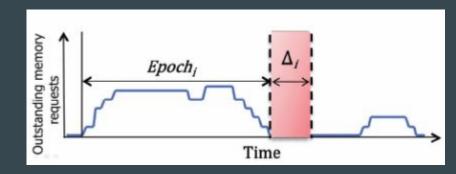
Emulation of NVMs

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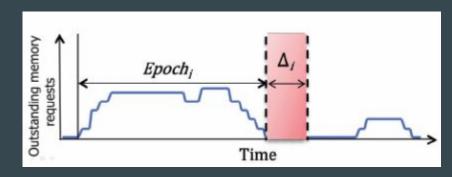
Emulation: Quartz



- Latency Model
 - Dynamically injects software created delays

$$\Delta_i = M_i.(NVM_{lat} - DRAM_{lat})$$

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- Bandwidth Model
 - o DRAM thermal control feature

Programming interface to Non Volatile Memory

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 - Resistant to memory leaks

Persistent Object Access

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- Lack of Implementation Details and Incomplete

Abstract binary files to object

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 - Pipeline Processing

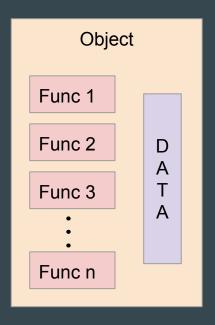
High Level View

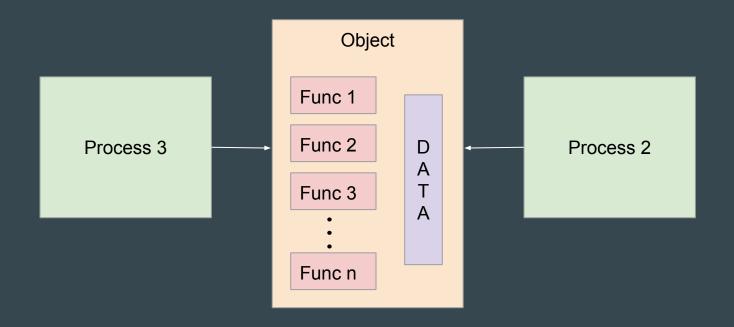
Process 1

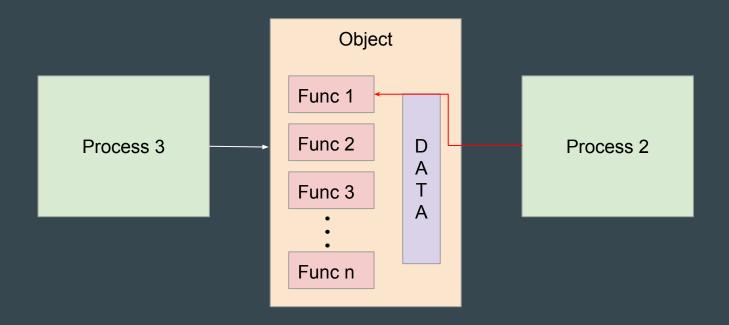
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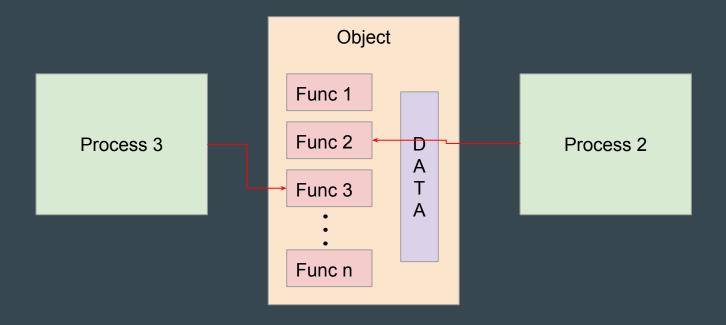
Object

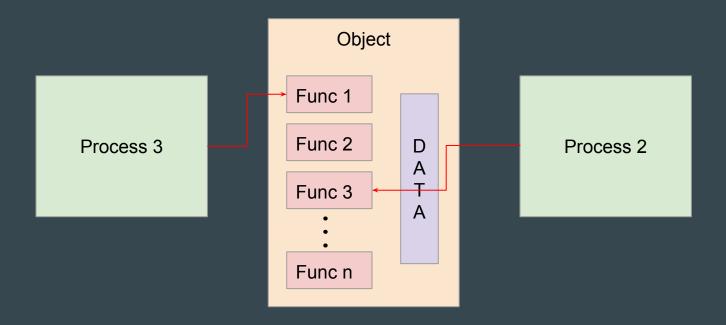
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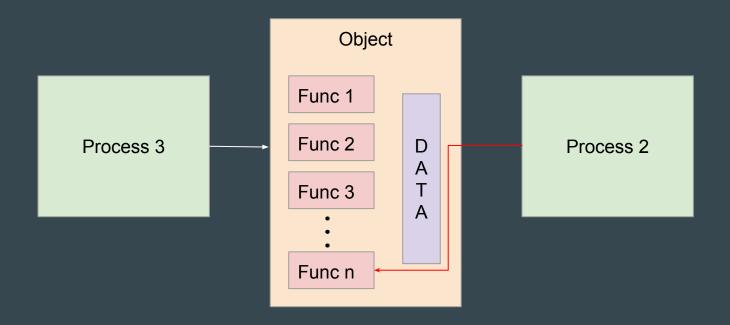


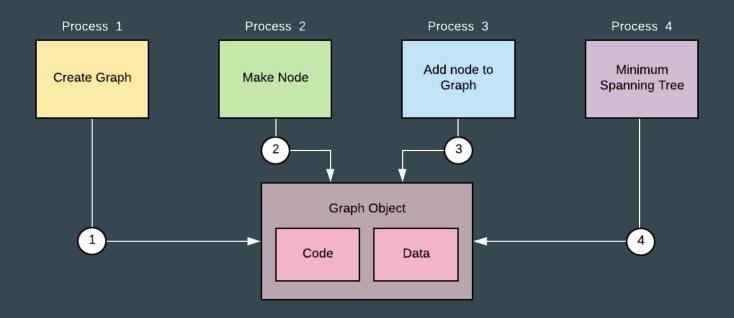


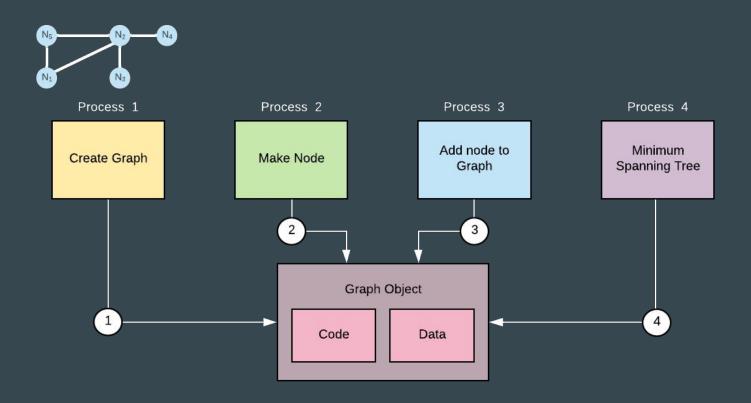


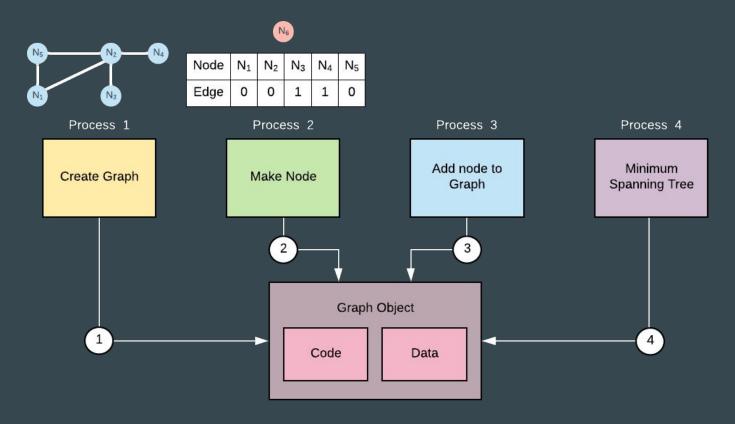


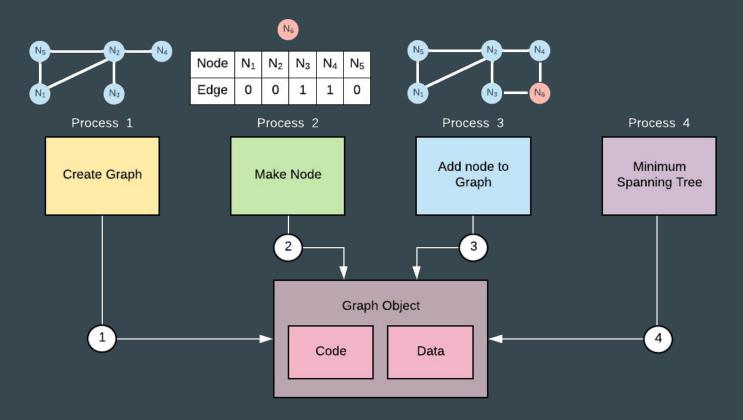


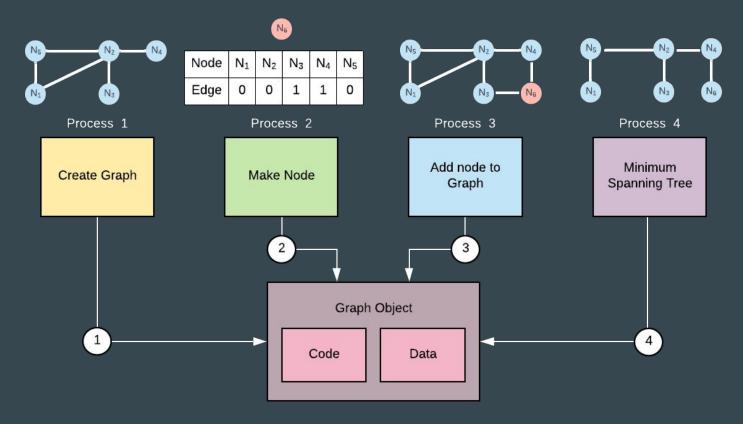












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 - Communication through IOCTL
- A user library, which needs to be linked to process
 - Responsible for making all the calls related to the object framework
 - Obtains metadata of objects and carry out the required functionality

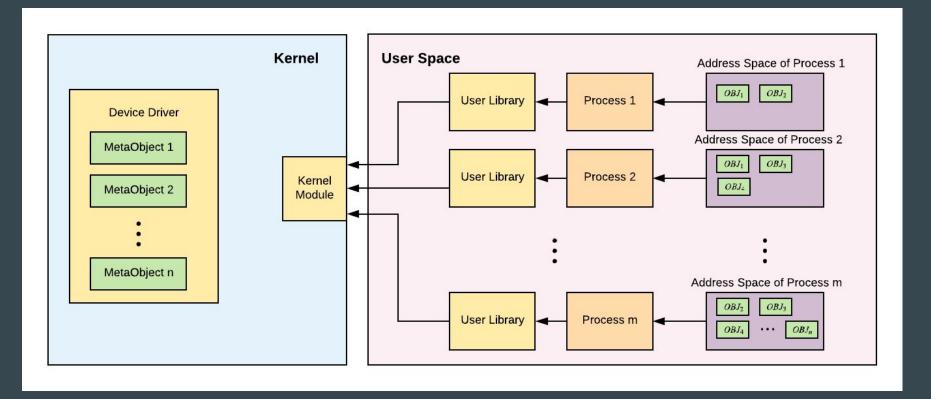
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- Attach_object (obj_id):
 - Attaches the object in process' address space
- Call_func (obj_id, func_id):
 - Calls given function from given object
- Append_code (obj_id, binary):
 - Adds the given code in object's memory segment

Implementation: Framework



- Similar to implementation of Exec
 - Map code and data in address space`

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 - Map code and data in address space
 - But we only require a small subset of features
 - High overhead, if already implemented functions are used
- Use Shared Memory Techniques
 - Shm (shmget, shmat, shmdt, shmctl)
 - Mmap

Implementation: Relocations

- Binary (code segment) of object can contain unresolved links (since binary is compiled code)
 - Functions in different library
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Implementation: Relocations

- Binary (code segment) of object can contain unresolved links (since binary is compiled code)
 - Functions in different library
 - Global Variables
- Resolved using elf library
 - Relocation section contains relevant information
 - Target address can be found in symbol table of linked libraries

Applications

Object model is a basic framework which can be used in variety of fields

- Operating System for NVRAM
- Lambda Services
- Distributed Systems

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- Objects can be handled in defined manner
- Replace process with Objects
- Make kernel itself an object
 - Requires composition of objects

Applications: Lambda Services

Modern serverless online computing

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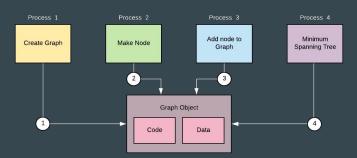
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Applications: Lambda Services

- Modern serverless online computing
- Takes code and data as input and outputs processed data using the code
- Object model fits in perfectly
 - Also provides stateful experience by keeping updated data in the object
 - Requires data input only once

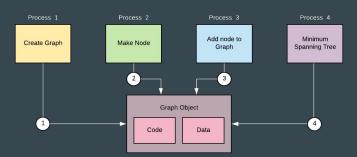
Applications: Distributed Systems

Make objects the computing entities



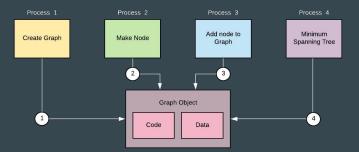
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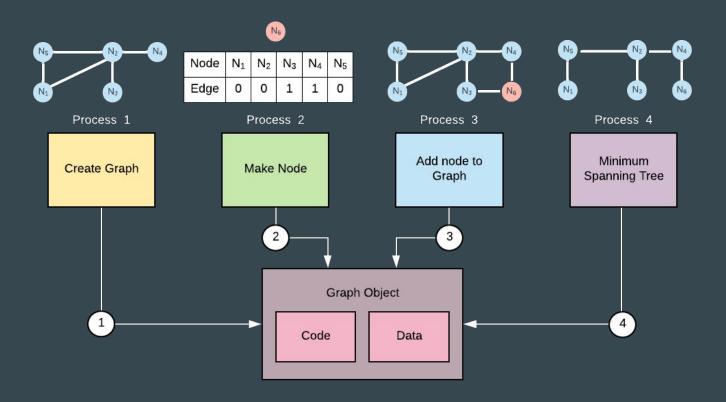
- Make objects the computing entities
- Takes the form of Pipeline computing
- Signals would automate the computing as well



Evaluation

- Basic Test Cases
 - Consistency Checks
 - Data Integrity
 - Function Calls
 - Add Code (binary)
 - Relocation checks
- Graph Processing

Evaluation: Graph Processing



Composition of objects

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- Signals from objects to objects and processes
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 - Since the object shares the space address space as process, isolation can be compromised
- Integrate our object model in different applications

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- Object model finds a lot of applications in modern day computing
- This is just a glimpse of the bigger picture that remains to come in future

Thank You!!

Back Up: NVM Characteristics

8.	SRAM	DRAM	HDD	NAND flash	STT-RAM	ReRAM	PCM	FeRAM
Cell size (F ²)	120-200	60-100	N/A	4-6	6-50	4-10	4-12	6-40
Write Endurance	10 ¹⁶	>10 ¹⁵	>10 ¹⁵ (pb: mechanical parts)	$10^4 - 10^5$	$10^{12} - 10^{15}$	10 ⁸ -10 ¹¹	108-109	$10^{14} - 10^{15}$
Read Latency	~0.2-2ns	~10ns	3-5ms	15–35μs	2-35ns	~10ns	20-60ns	20-80ns
Write Latency	~0.2-2ns	~10ns	3–5ms	200-500μs	3-50ns	~50ns	20-150ns	50-75ns
Leakage Power	High	Medium	(Mechanical parts)	Low	Low	Low	Low	Low
Dynamic Energy (R/W)	Low	Medium	(Mechanical parts)	Low	Low/High	Low/High	Medium/ High	Low/High
Maturity	Mature	Mature	Mature	Mature	Test chips	Test chips	Test chips	Manufactured