Exploration of NINE LLCs in multi-core processors

Arpit Gupta
Indian Institute of Technology Kanpur
arpitrag@iitk.ac.in

Hritvik Taneja
Indian Institute of Technology Kanpur
hritvikt@iitk.ac.in

ABSTRACT

Modern multi-core processors are usually equipped with a per-core private cache hierarchy assisted with a relatively larger shared cache (LLC). One of the key design choices while designing the memory hierarchy is the inclusion policy i.e. inclusive, non inclusive non-exclusive (NINE), or exclusive. Each choice has its own benefits and drawbacks. Cache hierarchies are kept inclusive to avoid the implementation of complex logic of choosing a forwarder.

We architect a specialised inclusion policy which treats each block individually to decide whether to make that block inclusive or exclusive. The proposed inclusion policy makes use of the access history of that particular block to decide the inclusion policy for it. Depending on the number of sharers at a given point of time and occupancy of the related set in LLC, the block is either kept in LLC or removed from it when requested by some private cache. We also propose a modified version of LRU (Least Recently Used) to support our LLC. To simulate our idea we have built a cache simulator equipped with cache coherence protocol. The simulator is used to get the performance counters like number of misses, number of messages of each type etc. by running it on different address traces.

KEYWORDS

inclusion policy, non inclusive non exclusive, last level cache, cache hierarchy

1 INTRODUCTION

In this chip-multiprocessor era, one of the main goals of a systems architect is to design efficient cache hierarchy to reduce the data access latency as much as possible. Most of the modern day systems have a cache hierarchy consisting of per-core private cache hierarchy and a relatively larger shared cache (LLC). One of the key design choices while building a cache hierarchy is to choose the inclusion policy. Each inclusion policy comes with its own benefits and drawbacks. There are drawbacks in using either of the extreme versions of the inclusion policy: purely inclusive and purely exclusive for the cache hierarchy.

Traditionally, LLC is built as an inclusive cache. Inclusive caches tend to reduce the total number of cache blocks present in cache hierarchy due to the multiple copies of cache blocks in private caches and LLC. Exclusive hierarchy overcomes this problem by its inherent nature, but it faces with a different problem. Whenever a shared block is requested by the a private cache from exclusive LLC, the LLC needs to forward the request to some other sharer which has the particular block. This increases the critical path of the request and also increases traffic of forwarder.

It is worth noting that not all of the cache blocks are shared. So for private cache blocks, it suffices to remove that block from LLC once served to the private cache since it will not be requested by any other private cache. On the other hand, requests for shared cache blocks suffer when the block is not present in LLC, since the request needs to traverse to the owner core to fetch even the clean block.

Taking into account the above two reasons, it makes little sense to deploy either purely inclusive or purely exclusive policy for the caches. So we devise a non-inclusive non-exclusive per cache block policy to get some performance improvements.

2 RELATED WORK

There hasn't been much work in exploring different NINE cache hierarchies for multi-core processors. AMD came up with an idea in its Opteron Processor code-named "Magny-Cours". Magny-Cours had a victim LLC i.e. only the evicted blocks from the lowest level private cache were added to the LLC. They used the sharing history of the cache block to classify it as exclusive or inclusive. The core that victimized the block was stored in the directory. If the next request comes from the same core, then the block is not retained in LLC whereas if it is requested by some other core a copy of the same is block is kept in LLC hoping for a sharing pattern in future. The research paper doesn't provide much details about all the cases but this seems to be simple and initial stepping stone for a deeper dive into exploring the NINE cache hierarchies.

3 MOTIVATION

Before describing the idea we would like to draw attention to some of the points that played crucial role in helping us arrive at the forth-proposed design.

(1) DRAM latency is very large as compared to LLC access latency or L2 access latency. So we try to design a model which minimises the LLC misses, before optimising anything else. Considering this we would like to cache as many data blocks in our caches (including LLC and private caches) as possible. Hence we try to build our idea towards an exclusive policy while reducing the critical length of a shared data access.
(2) If we know that a cache block is private to a particular core, then it makes little sense to store it in LLC while it is already present in one of the private caches.
(3) For a shared block the critical path of a data access increases when the requested block is not present in LLC, because of the request being forwarded to one of the sharers instead of directly serving it. Hence we should try to cache the shared blocks in LLC to lower the latency for shared cache blocks.
(4) While evicting a block from LLC, we try to maintain our principle of maximizing the total distinct cache blocks present in whole cache hierarchy. Hence we try to evict the block

which might be present somewhere else in the cache hierarchy also. So that if that block is requested again in future, it can be served without going back to the slow DRAM.

(5) The bandwidth of interconnect is an invaluable resource for transporting data and messages. Hence we also try to send as less messages as possible.

4 METHODOLOGY

Keeping the points, described in previous section, in mind, we focus on two main points while designing the inclusion policy. Firstly, the LLC misses should be reduced as much as possible. Secondly, the messages passed should be minimised. In this section we describe the cache coherence protocol, inclusion policy, replacement policy and all other details that we propose.

(a) *Inclusion Policy:* When a cache block is requested for the first time by any processor, it will result in a cold miss in LLC. When the block is fetched from the DRAM, it is not installed in LLC and directly served to the core which requested it, creating an entry in the directory. When a block is requested by a core which is not present in the LLC, directory is looked-up and if it is present in some private cache the request is forwarded to the owner/sharer(any one) of that cache block. Whenever a core requests a cache block, the core ID is noted in the directory entry for future reference. Whenever a core wants to evict a block from its private cache, the block is sent to the LLC. If none of the other cores have the block we install the block in LLC, otherwise we don't. Moreover, if the block is already present in LLC when a private cache evicts it, LLC gets updated with the latest block. In this way LLC always has the latest copy of the block, if it has one. We note that if any of the cores has a block in modified state then LLC does not have it. Once a core has evicted a block, it remains in LLC unless it is victimized by the replacement policy of LLC itself. Once all the cores sharing a block evict it from their private caches, now if a request comes for the same block the inclusion or exclusion of that block in LLC is governed by the sharing history of that particular block. If the number of core IDs for a block is 1 then we annotate the block as private else it is annotated as shared. Based on this annotation the blocks are served in the following way:
   (i) *Private:* In this case we serve the request cache block from LLC and remove it from the LLC.
   (ii) *Shared:* In this case if the set containing the block in LLC, is filled more than a threshold fraction (more in next section), which we call *set-threshold*, then we serve the request and remove the block from LLC, else we serve and continue to retain the block.

(b) *Cache Coherence Protocol:* We use the MESI protocol for our cache hierarchy. The responses to different messages are modified in accordance to the inclusion policy described above.

(c) *Replacement Policy:* We use the usual LRU policy for the private caches and the directory. However, for the shared cache we make use of a modified version of LRU. While eviction, we evict the LRU block with probability p (more in next section), which we call *private replacement probability*, and with probability $1 - p$ we do the following:
   (i) Find the LRU shared block.
   (ii) If we find one, evict it else evict the LRU block.

5 HYPERPARAMETER TUNING

In this section we describe the effect of hyperparameters on the cache misses and messages.

(a) *Set-Threshold:* Set threshold determines whether a shared block needs to be retained in the LLC or not. If this set threshold is high the probability that a shared cache block is retained in LLC after being requested by a particular core is high, otherwise low. We can use this to always have some space left in our set for the private cache blocks, since if we lose them they needs to be fetched from the slow DRAM whereas if we remove shared block it can be served from the private caches also if requested in future, which is way faster than DRAM. Experiments can be done on applications relevant to the client to get optimum value of this threshold.

(b) *Private Replacement Probability:* This controls the probability of a private block being evicted when a block needs to be evicted. We have this so that less number of private blocks are evicted from LLC as compared to the shared blocks. Experiments can be done on applications relevant to the client to get optimum value of this probability.

6 EVALUATION

We run our model on address traces generated form the PARSEC suite. We run simulations with different cache configurations which are described in *Configuration Table* in Appendix. We also use different inputs to get the address traces from the PARSEC suite like test, simsmall, simmedium simlarge, simdev and native. Different inputs are taken in order to get traces of different sizes. We run the generated address traces assuming one master threads and four auxilliary threads. So we simulate the address traces assuming 5 processors generating them. Detailed results are provided in Appendix.

It is worth noting that our idea is only concerned with the last level of private cache hierarchy and last level cache. Hence we directly feed the address trace to the last level of private cache hierarchy to make the simulation faster although it corrupts the actual address that would be received by the last level of private cache.

Since the address traces generated by running suites with test, simsmall and simmedium inputs are small, hence we scale down the cache configurations so that all the addresses don't fit in the LLC and we see the affects of our policy.

Since we are not able to run the simulations on larger inputs by the deadline we will post the results for the larger inputs here.

7 CONCLUSIONS

In our work we aim to improve the cache hierarchy performance by reducing the cache misses and interconnect messages. We accomplished this by proposing a new inclusion policy which treats each cache block individually and determines whether to keep the block in LLC or not by analysing its sharing pattern in the past. We

also proposed a replacement policy which makes use of probability to maximize the number of distinct cache blocks in the cache hierarchy without actually retaining very old cache blocks.

8 FUTURE WORK

While implementing our idea, we only tried MESI protocol. We can try different cache coherence protocols to check the best protocol that suits the access patterns with sharing addresses from different processors. Probability can be used to a better extent for the eviction policy. Infact, better replacement policies which are aware of the sharing history can be used to enhance performance.

9 APPENDIX

Abbreviations Table:

L2.i.MR	L2 Miss Rate of i-th core
L2.i.TM	L2 Total Messages of i-th core
S.MR	Shared Cache Miss Rate of i-th core
S.TM	Shared Cache Total Messages of i-th core
D.TM	Directory Total Messages

Configuration Table:

Same colour represents same configuration with different policies

Trace	L2 Block	L2 Associativity	L2 Set	L2 Size	L3 Block	L3 Associativity	L3 Set	L3 Size	Cache Hierarchy Block Size	Directory Associativity	Directory Set	Directory Size	Policy
cache1	64	8	512	262144	64	16	8192	8388608	16	64	8192	8388608	Our Policy
cache2	64	8	64	32768	64	16	8192	8388608	8	64	4096	2097152	Our Policy
cache3	64	8	64	32768	64	16	8192	8388608	8	64	16384	8388608	Our Policy
cache4	64	8	512	262144	64	16	8192	8388608	8	64	32768	16777216	Our Policy
cache5	64	8	64	32768	64	16	8192	8388608	16	64	4096	4194304	Our Policy
cache6	64	8	64	32768	64	16	8192	8388608	16	64	32768	33554432	Our Policy
cache7	64	8	512	262144	64	16	8192	8388608	16	64	8192	8388608	NINE
cache8	64	8	64	32768	64	16	8192	8388608	8	64	4096	2097152	NINE
cache9	64	8	64	32768	64	16	8192	8388608	8	64	16384	8388608	NINE
cache10	64	8	512	262144	64	16	8192	8388608	8	64	32768	16777216	NINE
cache11	64	8	64	32768	64	16	8192	8388608	16	64	4096	4194304	NINE
cache12	64	8	64	32768	64	16	8192	8388608	16	64	32768	33554432	NINE
cache21	64	8	64	32768	64	16	256	262144	16	64	256	262144	Our Policy
cache22	64	8	64	32768	64	16	256	262144	16	64	128	131072	Our Policy
cache23	64	8	64	32768	64	16	256	262144	16	64	512	524288	Our Policy
cache24	64	8	2	1024	64	16	32	32768	16	64	32	32768	Our Policy
cache25	64	8	2	1024	64	16	32	32768	16	64	16	16384	Our Policy
cache26	64	8	2	1024	64	16	32	32768	16	64	64	65536	Our Policy
cache27	64	8	2	1024	64	16	32	32768	16	64	128	131072	Our Policy
cache28	64	8	2	1024	64	16	16	16384	16	64	16	16384	Our Policy
cache29	64	8	64	32768	64	16	256	262144	16	64	256	262144	NINE
cache30	64	8	64	32768	64	16	256	262144	16	64	128	131072	NINE
cache31	64	8	64	32768	64	16	256	262144	16	64	512	524288	NINE
cache32	64	8	2	1024	64	16	32	32768	16	64	32	32768	NINE
cache33	64	8	2	1024	64	16	32	32768	16	64	16	16384	NINE
cache34	64	8	2	1024	64	16	32	32768	16	64	64	65536	NINE
cache35	64	8	2	1024	64	16	32	32768	16	64	128	131072	NINE
cache36	64	8	2	1024	64	16	16	16384	16	64	16	16384	NINE

Configuration: **cache1**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.76	475826	0.24	21320	0.21	17928	0.21	20008	0.19	16863	54.05	1061852	527667
blackscholes	test	2.95	3888	1.82	452	1.94	491	2.08	516	2.07	518	78.99	9926	4925
swaptions	test	1.52	19720	NA	0	NA	0	NA	0	NA	0	89.94	39440	19720
freqmine	test	1.45	287904	1.35	28025	1.36	28021	1.33	27805	NA	0	58.03	727391	361193
fluidanimate	simsmall	1.26	2085983	0.35	873398	0.34	875370	0.35	875591	0.34	899429	51.15	10740983	5329281
blackscholes	simsmall	0.05	15314	0.01	1105	0.01	1390	0.01	1217	0.01	938	70.08	34629	17290
swaptions	simsmall	0.01	67540	0.0	25019	0.0	25126	0.0	30729	NA	0	42.76	235138	110278
freqmine	simsmall	0.41	2129874	0.53	1937758	0.56	2042161	0.51	1846984	NA	0	41.42	15325375	7651298
blackscholes	simmedium	0.04	58172	0.0	2833	0.01	7199	0.0	2901	0.01	6940	47.65	149131	74537

Configuration: **cache2**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.87	502357	0.46	32582	0.44	28801	0.4	32808	0.38	28640	77.06	1228962	611915
blackscholes	test	3.81	8231	1.82	469	1.94	503	2.08	516	2.07	564	64.52	18837	9381
swaptions	test	2.39	36910	NA	0	NA	0	NA	0	NA	0	57.24	73820	36910
freqmine	test	1.76	348796	1.35	26938	1.37	26689	1.33	26461	NA	0	71.68	853162	425492
fluidanimate	simsmall	1.38	2286335	0.46	1061329	0.46	1091873	0.46	1070890	0.46	1119205	64.77	12928950	6441796
blackscholes	simsmall	0.06	21993	0.03	6933	0.03	7327	0.03	6978	0.03	6699	29.92	97464	48712
swaptions	simsmall	1.21	4828226	1.21	4752015	1.23	4738594	1.21	4645649	NA	0	0.23	36080408	18033695
freqmine	simsmall	0.99	4933219	1.21	4260477	1.36	4716880	1.25	4265510	NA	0	22.04	35911120	17947563
blackscholes	simmedium	0.04	60478	0.39	359062	0.39	359431	0.39	358639	0.39	359003	2.66	2991551	1495755

Configuration: **cache3**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.87	501985	0.46	31602	0.44	27811	0.4	31826	0.38	27671	48.15	1222461	609710
blackscholes	test	3.81	8231	1.82	469	1.94	503	2.08	516	2.07	564	64.52	18837	9381
swaptions	test	2.39	36910	NA	0	NA	0	NA	0	NA	0	57.24	73820	36910
freqmine	test	1.76	349172	1.35	26425	1.36	26320	1.33	26108	NA	0	49.63	851825	425394
fluidanimate	simsmall	1.38	2284465	0.46	1060153	0.46	1091152	0.46	1069850	0.46	1118730	41.53	12921135	6438944
blackscholes	simsmall	0.06	21993	0.03	6933	0.03	7327	0.03	6978	0.03	6699	29.92	97464	48712
swaptions	simsmall	1.21	4736259	1.21	4693084	1.23	4715076	1.21	4645649	NA	0	0.23	36080408	18033695
freqmine	simsmall	0.99	4927926	1.21	4253940	1.36	4711681	1.25	4260683	NA	0	17.3	35877548	17936066
blackscholes	simmedium	0.04	60478	0.39	359060	0.39	359430	0.39	358639	0.39	359003	2.66	2991551	1495755

Configuration: **cache4**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.76	475828	0.24	21154	0.21	17839	0.21	19926	0.19	16803	51.07	1061305	527486
blackscholes	test	2.95	3888	1.82	452	1.94	491	2.08	516	2.07	518	78.99	9926	4925
swaptions	test	1.52	19720	NA	0	NA	0	NA	0	NA	0	89.94	39440	19720
freqmine	test	1.45	287899	1.35	28033	1.36	28020	1.33	27805	NA	0	58.03	727391	361193
fluidanimate	simsmall	1.26	2089421	0.35	873455	0.34	875498	0.35	875670	0.34	899561	49.72	10740789	5329263
blackscholes	simsmall	0.05	15314	0.01	1105	0.01	1390	0.01	1217	0.01	938	70.08	34629	17290
swaptions	simsmall	0.01	67540	0.0	25019	0.0	25126	0.0	30729	NA	0	42.76	235138	110278
freqmine	simsmall	0.41	2136232	0.53	1943754	0.56	2045682	0.51	1850427	NA	0	41.09	15331662	7652528
blackscholes	simmedium	0.04	58172	0.0	2833	0.01	7199	0.0	2901	0.01	6940	47.65	149131	74537

Configuration: **cache5**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.87	502114	0.46	32580	0.44	28801	0.4	32808	0.38	28641	76.79	1228554	611753
blackscholes	test	3.81	8231	1.82	469	1.94	503	2.08	516	2.07	564	64.52	18837	9381
swaptions	test	2.39	36910	NA	0	NA	0	NA	0	NA	0	57.24	73820	36910
freqmine	test	1.76	349172	1.35	26824	1.37	26755	1.33	26452	NA	0	55.08	853527	425929
fluidanimate	simsmall	1.38	2285011	0.46	1060648	0.46	1091376	0.46	1070116	0.46	1118919	50.91	12923246	6439762
blackscholes	simsmall	0.06	21993	0.03	6933	0.03	7327	0.03	6978	0.03	6699	29.92	97464	48712
swaptions	simsmall	1.21	4669813	1.21	4657716	1.23	4702318	1.21	4645649	NA	0	0.23	36080408	18033695
freqmine	simsmall	0.99	4928842	1.21	4254755	1.36	4712774	1.25	4261933	NA	0	18.03	35883707	17938079
blackscholes	simmedium	0.04	60478	0.39	359060	0.39	359430	0.39	358639	0.39	359003	2.66	2991551	1495755

Configuration: **cache6**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.87	502040	0.46	31494	0.44	27794	0.4	31816	0.38	27658	46.16	1222389	609686
blackscholes	test	3.81	8231	1.82	469	1.94	503	2.08	516	2.07	564	64.52	18837	9381
swaptions	test	2.39	36910	NA	0	NA	0	NA	0	NA	0	57.24	73820	36910
freqmine	test	1.76	349138	1.35	26423	1.36	26315	1.33	26108	NA	0	49.62	851825	425394
fluidanimate	simsmall	1.38	2284227	0.46	1059481	0.46	1090630	0.46	1069359	0.46	1118180	41.47	12916777	6437454
blackscholes	simsmall	0.06	21993	0.03	6933	0.03	7327	0.03	6978	0.03	6699	29.92	97464	48712
swaptions	simsmall	1.21	4669813	1.21	4657716	1.23	4702318	1.21	4645649	NA	0	0.23	36080408	18033695
freqmine	simsmall	0.99	4922890	1.21	4250541	1.36	4709795	1.25	4260586	NA	0	17.29	35874633	17935091
blackscholes	simmedium	0.04	60478	0.39	359060	0.39	359430	0.39	358639	0.39	359003	2.66	2991551	1495755

Configuration: **cache7**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.76	479037	0.24	24502	0.21	20600	0.21	23326	0.19	19642	54.09	1077648	527541
blackscholes	test	2.95	3771	1.82	452	1.94	497	2.08	525	2.07	530	78.99	10115	4925
swaptions	test	1.52	19720	NA	0	NA	0	NA	0	NA	0	89.94	39440	19720
freqmine	test	1.45	288060	1.35	29581	1.36	29618	1.33	29405	NA	0	58.12	732564	361226
fluidanimate	simsmall	1.26	2089825	0.35	917911	0.34	916318	0.35	921148	0.34	946663	51.59	10926526	5330370
blackscholes	simsmall	0.05	16812	0.01	1160	0.01	1449	0.01	1285	0.01	1007	70.08	36533	17290
swaptions	simsmall	0.01	70023	0.0	28074	0.0	28206	0.0	35235	NA	0	42.76	249475	110278
freqmine	simsmall	0.41	2171527	0.53	1983839	0.56	2104178	0.51	1921265	NA	0	42.23	15604454	7662082
blackscholes	simmedium	0.04	59684	0.0	3061	0.01	7457	0.0	3166	0.01	7210	47.65	151860	74537

Configuration: **cache8**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.87	502533	0.46	33777	0.44	29566	0.4	35568	0.38	30791	77.14	1236393	611982
blackscholes	test	3.81	8120	1.82	463	1.94	497	2.08	525	2.07	599	64.52	19013	9381
swaptions	test	2.39	36910	NA	0	NA	0	NA	0	NA	0	57.24	73820	36910
freqmine	test	1.78	354331	1.35	27038	1.37	26784	1.33	26564	NA	0	71.51	862942	429134
fluidanimate	simsmall	1.38	2286292	0.46	1096184	0.46	1126648	0.46	1106522	0.46	1156948	63.73	13075486	6444005
blackscholes	simsmall	0.06	22063	0.03	6990	0.03	7383	0.03	7046	0.03	6768	29.92	97930	48712
swaptions	simsmall	1.21	4820309	1.21	4821073	1.23	4854914	1.21	4799601	NA	0	0.23	36701493	18033699
freqmine	simsmall	0.99	4985400	1.22	4316739	1.36	4785485	1.25	4337432	NA	0	24.61	36217109	17980872
blackscholes	simmedium	0.04	60584	0.39	359098	0.39	359495	0.39	358713	0.39	359065	2.66	2992037	1495755

Configuration: **cache9**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.87	502151	0.46	32808	0.44	28577	0.4	34606	0.38	29816	49.09	1229900	609772
blackscholes	test	3.81	8120	1.82	463	1.94	497	2.08	525	2.07	599	64.52	19013	9381
swaptions	test	2.39	36910	NA	0	NA	0	NA	0	NA	0	57.24	73820	36910
freqmine	test	1.76	349315	1.35	26660	1.36	26568	1.33	26370	NA	0	49.68	852961	425401
fluidanimate	simsmall	1.38	2284665	0.46	1091887	0.46	1122384	0.46	1101544	0.46	1153282	42.44	13051425	6439227
blackscholes	simsmall	0.06	22063	0.03	6990	0.03	7383	0.03	7046	0.03	6768	29.92	97930	48712
swaptions	simsmall	1.21	4820296	1.21	4821072	1.23	4854913	1.21	4799600	NA	0	0.23	36701473	18033695
freqmine	simsmall	0.99	4961261	1.21	4292715	1.36	4760102	1.25	4314198	NA	0	17.91	36082971	17942067
blackscholes	simmedium	0.04	60584	0.39	359098	0.39	359495	0.39	358713	0.39	359065	2.66	2992037	1495755

Configuration: **cache10**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.76	479023	0.24	24451	0.21	20612	0.21	23262	0.19	19636	54.05	1077409	527489
blackscholes	test	2.95	3771	1.82	452	1.94	497	2.08	525	2.07	530	78.99	10115	4925
swaptions	test	1.52	19720	NA	0	NA	0	NA	0	NA	0	89.94	39440	19720
freqmine	test	1.45	288047	1.35	29565	1.36	29598	1.33	29394	NA	0	58.03	732476	361193
fluidanimate	simsmall	1.26	2090664	0.35	915369	0.34	913862	0.35	918316	0.34	944506	51.13	10914721	5329212
blackscholes	simsmall	0.05	16812	0.01	1160	0.01	1449	0.01	1285	0.01	1007	70.08	36533	17290
swaptions	simsmall	0.01	70023	0.0	28074	0.0	28206	0.0	35235	NA	0	42.76	249475	110278
freqmine	simsmall	0.41	2160092	0.53	1975799	0.56	2095985	0.51	1913681	NA	0	41.57	15560001	7652528
blackscholes	simmedium	0.04	59684	0.0	3061	0.01	7457	0.0	3166	0.01	7210	47.65	151860	74537

Configuration: **cache11**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.87	502251	0.46	33777	0.44	29565	0.4	35567	0.38	30798	76.8	1235936	611804
blackscholes	test	3.81	8120	1.82	463	1.94	497	2.08	525	2.07	599	64.52	19013	9381
swaptions	test	2.39	36910	NA	0	NA	0	NA	0	NA	0	57.24	73820	36910
freqmine	test	1.76	349827	1.35	26843	1.37	26635	1.33	26411	NA	0	54.79	853905	425545
fluidanimate	simsmall	1.38	2285170	0.46	1093230	0.46	1123529	0.46	1102819	0.46	1154184	50.66	13058091	6440713
blackscholes	simsmall	0.06	22063	0.03	6990	0.03	7383	0.03	7046	0.03	6768	29.92	97930	48712
swaptions	simsmall	1.21	4820296	1.21	4821072	1.23	4854913	1.21	4799600	NA	0	0.23	36701473	18033695
freqmine	simsmall	0.99	4966759	1.21	4296584	1.36	4764401	1.25	4318435	NA	0	19.39	36107452	17948747
blackscholes	simmedium	0.04	60584	0.39	359098	0.39	359495	0.39	358713	0.39	359065	2.66	2992037	1495755

Configuration: **cache12**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.87	502082	0.46	32779	0.44	28554	0.4	34569	0.38	29794	46.91	1229640	609686
blackscholes	test	3.81	8120	1.82	463	1.94	497	2.08	525	2.07	599	64.52	19013	9381
swaptions	test	2.39	36910	NA	0	NA	0	NA	0	NA	0	57.24	73820	36910
freqmine	test	1.76	349312	1.35	26657	1.36	26565	1.33	26367	NA	0	49.62	852942	425394
fluidanimate	simsmall	1.38	2284089	0.46	1090827	0.46	1121289	0.46	1100484	0.46	1151962	41.6	13044033	6437017
blackscholes	simsmall	0.06	22063	0.03	6990	0.03	7383	0.03	7046	0.03	6768	29.92	97930	48712
swaptions	simsmall	1.21	4820296	1.21	4821072	1.23	4854913	1.21	4799600	NA	0	0.23	36701473	18033695
freqmine	simsmall	0.99	4957525	1.21	4288365	1.36	4755864	1.25	4310375	NA	0	17.3	36060271	17935136
blackscholes	simmedium	0.04	60584	0.39	359098	0.39	359495	0.39	358713	0.39	359065	2.66	2992037	1495755

Configuration: **cache21**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.88	507000	0.47	34086	0.44	30118	0.41	34250	0.38	29846	88.12	1242592	615150
blackscholes	test	3.81	8231	1.82	469	1.94	503	2.08	516	2.07	564	64.52	18837	9381
swaptions	test	2.4	37092	NA	0	NA	0	NA	0	NA	0	63.57	74116	37024
freqmine	test	1.76	351999	1.36	28163	1.37	28575	1.34	28254	NA	0	85.04	861780	426081
fluidanimate	simsmall	1.39	2306340	0.46	1142836	0.46	1164563	0.47	1146962	0.46	1192618	80.21	13301720	6493996
blackscholes	simsmall	0.06	22002	0.03	6933	0.03	7329	0.03	6978	0.03	6699	31.92	97473	48712
freqmine	simsmall	1.05	5630068	1.32	4978534	1.45	5360882	1.35	4943846	NA	0	63.17	39945812	19266397

Configuration: **cache22**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.9	513861	0.48	39493	0.45	35194	0.42	39272	0.39	33892	92.34	1276624	622100
blackscholes	test	3.82	8266	1.82	469	1.94	503	2.08	516	2.07	564	67.15	18880	9389
swaptions	test	2.42	37676	NA	0	NA	0	NA	0	NA	0	72.58	75044	37368
freqmine	test	1.76	359885	1.36	35921	1.37	37437	1.34	36786	NA	0	89.42	895277	426550
fluidanimate	simsmall	1.4	2339721	0.49	1442203	0.48	1464835	0.49	1439762	0.48	1488515	89.14	14722923	6694117
blackscholes	simsmall	0.06	23098	0.03	8437	0.04	10137	0.03	8523	0.04	9232	50.78	112864	54587
freqmine	simsmall	1.17	7089079	1.52	6673304	1.64	7071255	1.55	6643517	NA	0	82.45	49009341	21849061

Configuration: **cache23**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.88	506321	0.47	33511	0.44	29841	0.4	33595	0.38	29590	85.3	1238868	614709
blackscholes	test	3.81	8231	1.82	469	1.94	503	2.08	516	2.07	564	64.52	18837	9381
swaptions	test	2.39	36960	NA	0	NA	0	NA	0	NA	0	62.79	73900	36940
freqmine	test	1.76	350846	1.36	27917	1.37	28611	1.34	28479	NA	0	84.86	860549	425988
fluidanimate	simsmall	1.39	2303907	0.46	1122676	0.46	1149311	0.46	1128725	0.46	1177419	77.36	13214442	6479397
blackscholes	simsmall	0.06	21999	0.03	6933	0.03	7329	0.03	6978	0.03	6699	30.88	97472	48714
freqmine	simsmall	1.03	5360808	1.27	4652267	1.41	5067906	1.3	4611307	NA	0	52.55	38033778	18650708

Configuration: **cache24**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	13.12	3521720	10.15	618428	10.5	633790	9.23	581993	9.35	573657	10.85	11779633	5888666
blackscholes	test	19.37	41927	11.69	3092	11.03	2869	4.26	1210	4.31	1311	17.26	99634	49807
swaptions	test	21.09	329920	NA	0	NA	0	NA	0	NA	0	11.22	659836	329916
freqmine	test	3.73	737047	1.49	29498	1.51	29224	1.48	29142	NA	0	51.72	1645733	822456
fluidanimate	simsmall	15.96	26387136	9.56	20683073	9.78	22026778	9.68	21019746	9.97	22712366	6.47	223963442	111954481
blackscholes	simsmall	12.28	4359943	13.01	3079320	12.97	3061747	12.98	3057986	12.95	3050021	2.36	33018935	16508105

Configuration: **cache25**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	13.12	3522124	10.19	622201	10.53	637091	9.26	585535	9.38	576888	12.91	11802531	5897431
blackscholes	test	19.37	41939	11.72	3122	11.04	2893	4.27	1223	4.32	1331	19.25	99783	49855
swaptions	test	21.09	329936	NA	0	NA	0	NA	0	NA	0	12.97	659862	329926
freqmine	test	3.73	737716	1.49	29798	1.51	29504	1.49	29389	NA	0	54.7	1648009	823347
fluidanimate	simsmall	15.97	26392687	9.61	20871958	9.83	22209358	9.73	21197503	10.02	22885789	10.97	225089314	112375386
blackscholes	simsmall	12.28	4359956	13.01	3084328	12.98	3066218	12.99	3062282	12.96	3054363	2.47	33042975	16517541

Configuration: **cache26**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	13.11	3521660	10.14	618989	10.5	634067	9.22	581984	9.35	573582	10.81	11777739	5887919
blackscholes	test	19.37	41925	11.69	3094	11.03	2871	4.26	1212	4.31	1309	17.22	99621	49802
swaptions	test	21.09	329914	NA	0	NA	0	NA	0	NA	0	11.22	659826	329912
freqmine	test	3.73	736973	1.49	29471	1.5	29183	1.48	29107	NA	0	51.54	1645431	822337
fluidanimate	simsmall	15.96	26386545	9.56	20700545	9.78	22032088	9.68	21018689	9.97	22709687	6.39	223914146	111934526
blackscholes	simsmall	12.28	4361719	13.0	3098360	12.97	3074880	12.98	3067284	12.95	3057976	2.36	33046300	16522030

Configuration: **cache27**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	13.11	3521769	10.14	618305	10.49	633523	9.22	581372	9.34	573087	10.79	11774193	5886648
blackscholes	test	19.36	41918	11.69	3094	11.03	2871	4.26	1212	4.31	1309	17.21	99611	49798
swaptions	test	21.08	329908	NA	0	NA	0	NA	0	NA	0	11.22	659816	329908
freqmine	test	3.72	736619	1.48	29308	1.5	29032	1.48	28972	NA	0	51.53	1644196	821841
fluidanimate	simsmall	15.96	26385733	9.56	20679327	9.77	22012123	9.67	20998706	9.97	22689647	6.35	223787733	111887532
blackscholes	simsmall	12.28	4364114	13.0	3086454	12.97	3064778	12.98	3058526	12.95	3049512	2.34	33010678	16504859

Configuration: **cache28**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	13.12	3522124	10.19	622201	10.53	637091	9.26	585535	9.38	576888	12.91	11802531	5897431
blackscholes	test	19.37	41939	11.72	3122	11.04	2893	4.27	1223	4.32	1331	19.25	99783	49855
swaptions	test	21.09	329936	NA	0	NA	0	NA	0	NA	0	12.97	659862	329926
freqmine	test	3.73	737716	1.49	29798	1.51	29504	1.49	29389	NA	0	54.7	1648009	823347
fluidanimate	simsmall	15.97	26392687	9.61	20871958	9.83	22209358	9.73	21197503	10.02	22885789	10.97	225089314	112375386
blackscholes	simsmall	12.28	4359956	13.01	3084328	12.98	3066218	12.99	3062282	12.96	3054363	2.47	33042975	16517541

Configuration: **cache29**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.88	506879	0.47	35124	0.44	30830	0.41	36966	0.38	32117	88.69	1249475	614927
blackscholes	test	3.82	8138	1.82	469	1.94	497	2.08	534	2.1	608	64.59	19072	9401
swaptions	test	2.41	37544	NA	0	NA	0	NA	0	NA	0	66.54	74698	37154
freqmine	test	1.76	350282	1.36	27240	1.37	27016	1.34	26788	NA	0	85.7	856550	426140
fluidanimate	simsmall	1.39	2306642	0.46	1133707	0.46	1159708	0.46	1141558	0.46	1191994	80.58	13277290	6485343
blackscholes	simsmall	0.06	22222	0.03	7014	0.03	7383	0.03	7046	0.03	6768	31.77	98212	48812
freqmine	simsmall	1.04	5585855	1.3	4962494	1.44	5390905	1.33	4960662	NA	0	65.43	39754349	19075909

Configuration: **cache30**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.89	512460	0.48	38373	0.45	34561	0.41	40390	0.39	34559	92.81	1273118	619751
blackscholes	test	3.86	8381	1.82	473	1.94	504	2.08	532	2.08	611	69.39	19431	9504
swaptions	test	2.44	38953	NA	0	NA	0	NA	0	NA	0	77.09	76679	37726
freqmine	test	1.77	359299	1.36	32036	1.37	33338	1.34	32490	NA	0	90.19	882865	426622
fluidanimate	simsmall	1.4	2335803	0.48	1361269	0.47	1390129	0.48	1369762	0.47	1418076	89.88	14341955	6609431
blackscholes	simsmall	0.06	23429	0.03	8525	0.04	10001	0.04	9286	0.04	9583	51.92	115073	55266
freqmine	simsmall	1.14	6804617	1.47	6285963	1.59	6702101	1.49	6276482	NA	0	83.88	47024908	21237842

Configuration: **cache31**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	1.87	504340	0.46	34053	0.44	29729	0.4	36043	0.38	30940	87.75	1240451	613307
blackscholes	test	3.81	8120	1.82	463	1.94	497	2.08	525	2.07	599	64.52	19013	9381
swaptions	test	2.39	37002	NA	0	NA	0	NA	0	NA	0	63.8	73964	36962
freqmine	test	1.76	349058	1.36	27226	1.37	27001	1.34	26773	NA	0	85.05	855089	425948
fluidanimate	simsmall	1.39	2294164	0.46	1098775	0.46	1129282	0.46	1107725	0.46	1159520	79.86	13104724	6456332
blackscholes	simsmall	0.06	22071	0.03	6990	0.03	7383	0.03	7046	0.03	6768	31.92	97940	48714
freqmine	simsmall	1.01	5162475	1.24	4496337	1.38	4946172	1.28	4499758	NA	0	60.47	37226706	18328868

Configuration: **cache32**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	13.13	3527671	10.16	627401	10.51	643349	9.24	591559	9.36	584325	11.64	11835350	5895827
blackscholes	test	19.37	41977	11.69	3125	11.03	2912	4.27	1241	4.31	1396	18.22	99917	49824
swaptions	test	21.1	330412	NA	0	NA	0	NA	0	NA	0	12.5	660494	330082
freqmine	test	3.73	737425	1.49	29578	1.51	29363	1.48	29379	NA	0	52.22	1647182	822517
fluidanimate	simsmall	15.97	26417325	9.57	20861867	9.79	22257767	9.69	21246232	9.99	22980724	7.21	225116863	112086571
blackscholes	simsmall	12.28	4360158	13.02	3107875	12.98	3095531	12.99	3096315	12.96	3094658	2.45	33204063	16545510

Configuration: **cache33**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	13.14	3534490	10.23	638924	10.57	653895	9.3	602490	9.42	594461	14.88	11904522	5917020
blackscholes	test	19.39	42077	11.72	3156	11.03	2935	4.27	1260	4.34	1418	21.55	100192	49904
swaptions	test	21.11	331094	NA	0	NA	0	NA	0	NA	0	15.42	661416	330322
freqmine	test	3.73	738946	1.49	29874	1.51	29627	1.49	29635	NA	0	55.54	1650620	823672
fluidanimate	simsmall	15.98	26449862	9.65	21301427	9.87	22700355	9.77	21690921	10.06	23421703	13.12	227611368	112845673
blackscholes	simsmall	12.28	4360970	13.03	3121542	13.0	3109004	13.01	3110029	12.98	3108419	2.68	33277741	16569412

Configuration: **cache34**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	13.12	3524179	10.15	624882	10.5	641231	9.22	589543	9.35	582516	11.08	11818536	5890395
blackscholes	test	19.37	41932	11.69	3120	11.03	2911	4.26	1236	4.31	1390	17.4	99833	49802
swaptions	test	21.09	330108	NA	0	NA	0	NA	0	NA	0	11.61	660090	329982
freqmine	test	3.73	736821	1.48	29457	1.5	29219	1.48	29219	NA	0	51.82	1645720	822062
fluidanimate	simsmall	15.97	26398478	9.56	20794817	9.78	22188458	9.68	21178415	9.97	22912429	6.59	224709097	111958039
blackscholes	simsmall	12.28	4360012	13.01	3101863	12.97	3089261	12.98	3090210	12.95	3088483	2.38	33171270	16534786

Configuration: **cache35**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	13.12	3522864	10.14	623342	10.49	640347	9.22	588298	9.34	581935	10.92	11811243	5887976
blackscholes	test	19.37	41926	11.69	3120	11.03	2911	4.26	1236	4.31	1390	17.26	99825	49800
swaptions	test	21.09	329973	NA	0	NA	0	NA	0	NA	0	11.32	659899	329926
freqmine	test	3.72	736563	1.48	29382	1.5	29168	1.48	29157	NA	0	51.74	1645030	821805
fluidanimate	simsmall	15.97	26392160	9.56	20772513	9.78	22165115	9.68	21155615	9.97	22889709	6.47	224570154	111911582
blackscholes	simsmall	12.28	4359976	13.0	3083089	12.97	3071141	12.98	3072768	12.95	3070120	2.34	33092213	16508963

Configuration: **cache36**

Trace	Type	L2.0.MR	L2.0.TM	L2.1.MR	L2.1.TM	L2.2.MR	L2.2.TM	L2.3.MR	L2.3.TM	L2.4.MR	L2.4.TM	S.MR	S.TM	D.TM
fluidanimate	test	13.14	3534695	10.23	639199	10.57	653906	9.3	602741	9.42	594322	15.04	11905334	5917273
blackscholes	test	19.4	42084	11.74	3161	11.05	2938	4.27	1261	4.34	1421	21.65	100226	49919
swaptions	test	21.12	331160	NA	0	NA	0	NA	0	NA	0	15.46	661544	330384
freqmine	test	3.73	738924	1.49	29874	1.51	29629	1.49	29638	NA	0	55.62	1650593	823661
fluidanimate	simsmall	15.98	26450113	9.66	21314497	9.87	22710684	9.78	21700698	10.06	23432481	13.5	227680992	112873910
blackscholes	simsmall	12.28	4360968	13.03	3121582	13.0	3108962	13.01	3110023	12.98	3108427	2.68	33277702	16569388