Assignment-2

1→ Modes of 8086 microprocessor

↳ There are two modes :- ① Minimum mode ② Maximum mode.

① Minimum Mode

↳ Activated by setting the MN/MX pin to High (logic 1).

→ 8086 itself generates control signals.

→ Used for simpler systems.

→ Control signals generated by 8086 :-

• RD, WR, ALE, DT/R, DEN, etc.

② Maximum mode

↳ Activated by setting the MN/MX pin to low (logic 0).

→ Control signals are generated by an external bus controller (8288).

→ Used when multiple processors are in the system.

→ Control signals :- S_0, S_1, S_2.

2→ ⓐ Flag register of 8086

• 16-bit register containing status and control flags.

• Status flags :- CF (carry), PF (Parity), AF (Auxiliary Carry), ZF (zero), SF (Sign), OF (overflow).

• Control flags :- TF (Trap), IF (Interrupt enable), DF (direction)

ⓑ RISC vs CISC

Reduced Instruction Set	Complex Instruction Set
→ Simple, fixed-length, instructions.	→ Complex, variable-length instructions
→ Faster, needs more instructions	→ fewer instruction per task.
Ex :- ARM, MIPS	Ex :- X86 (8086) Intel.

© Memory-mapped I/O

→ I/O devices share address space with memory.

→ Instructions like MOV used.

→ 16-bit addresses

I/O-Mapped I/O

→ I/O devices have separate address space.

→ Special instruction like IN, OUT

→ 8-bit port addresses.

3. ① Immediate addressing
↳ MOV AX, 1234H.

② Register addressing
↳ MOV AX, BX

③ Direct addressing
↳ MOV AX, [1234H]

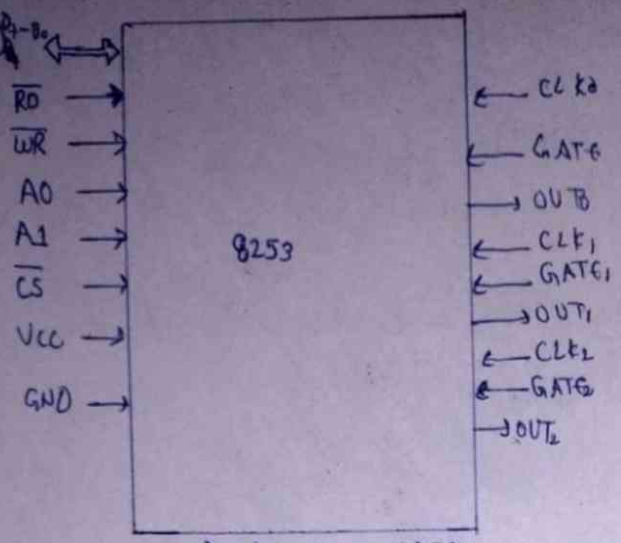
④ Register Indirect
↳ MOV AX, [BX]

⑤ Based Addressing
↳ MOV AX, [BX + 04H]

⑥ Indexed Addressing
↳ MOV AX, [SI + 10H]

⑦ Base-Indexed Addressing
↳ MOV AX, [BX + SI]

⑧ Relative Addressing
↳ JMP Label.

(4) 

Pin diagram of 8253.

- D_0-D_7 → These are data pins for transferring 8-bit data.
- RD (Read) → Used for reading data from the timer.
- WR (write) → Used to write data into the timer.
- CS (Chip select) → Enable the chip for operation.
- A_0, A_1 → Address pins used for selecting registers.
- CLK 0, CLK 1, CLK 2 → Clock input for counters.
- Out 0, out 1, out 2 → Counter outputs.
- GND & Vcc → Ground and Power connections.

Modes of operation

MODE 0 → Interrupt on terminal count.

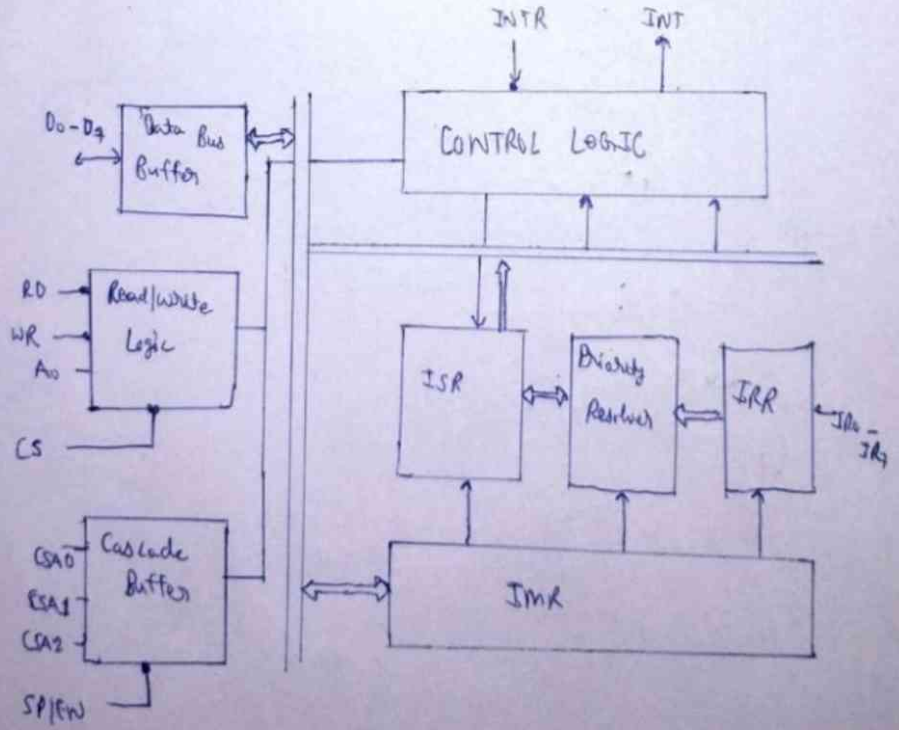
MODE 1 → Programmable one-shot.

MODE 2 → Rate generator.

MODE 3 → Square wave generator.

MODE 4 → Software triggered strobe.

MODE 5 → Hardware triggered strobe.

(5) 

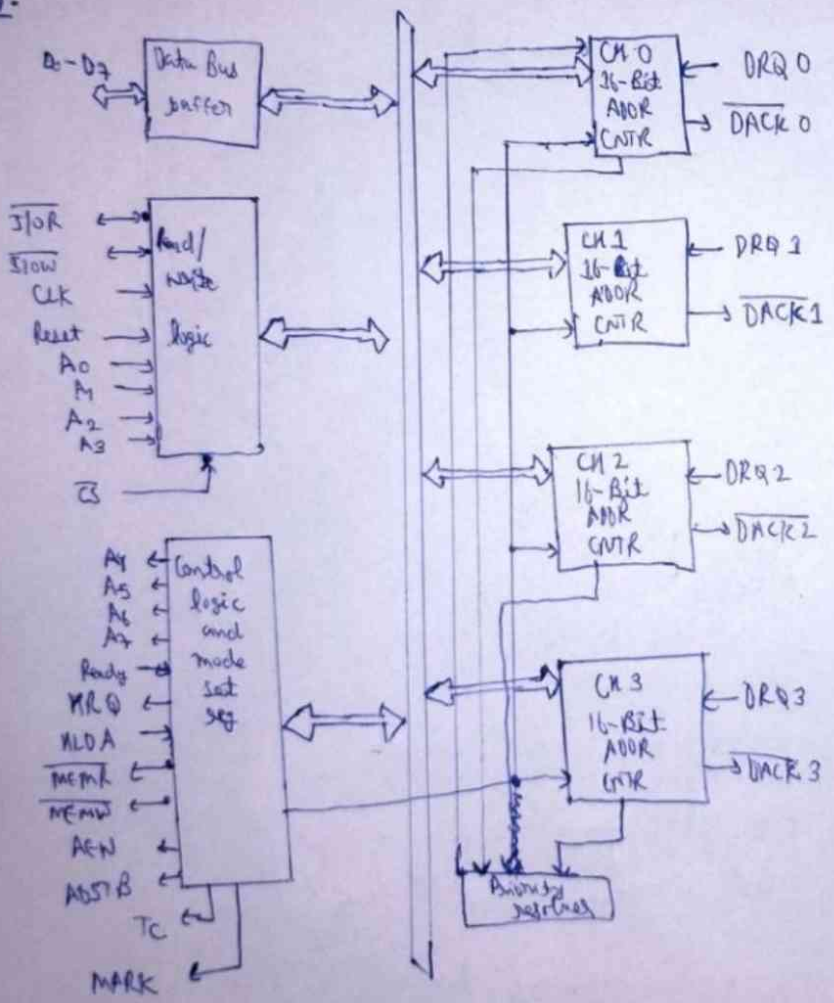
→ Master-Slave Configuration

- The master controller handles communication with the CPU.
- Slave controllers extend interrupt-handling capacity.

→ Architecture

- Control Registers :→ Initialization and operation modes are configured here.
- Interrupt Request Register (IRR) → Holds pending interrupts.
- In-Service Register (ISR) → Holds interrupts being serviced.
- Priority Resolver → Determines priority levels.
- Data bus buffer → Facilitates data transfer.

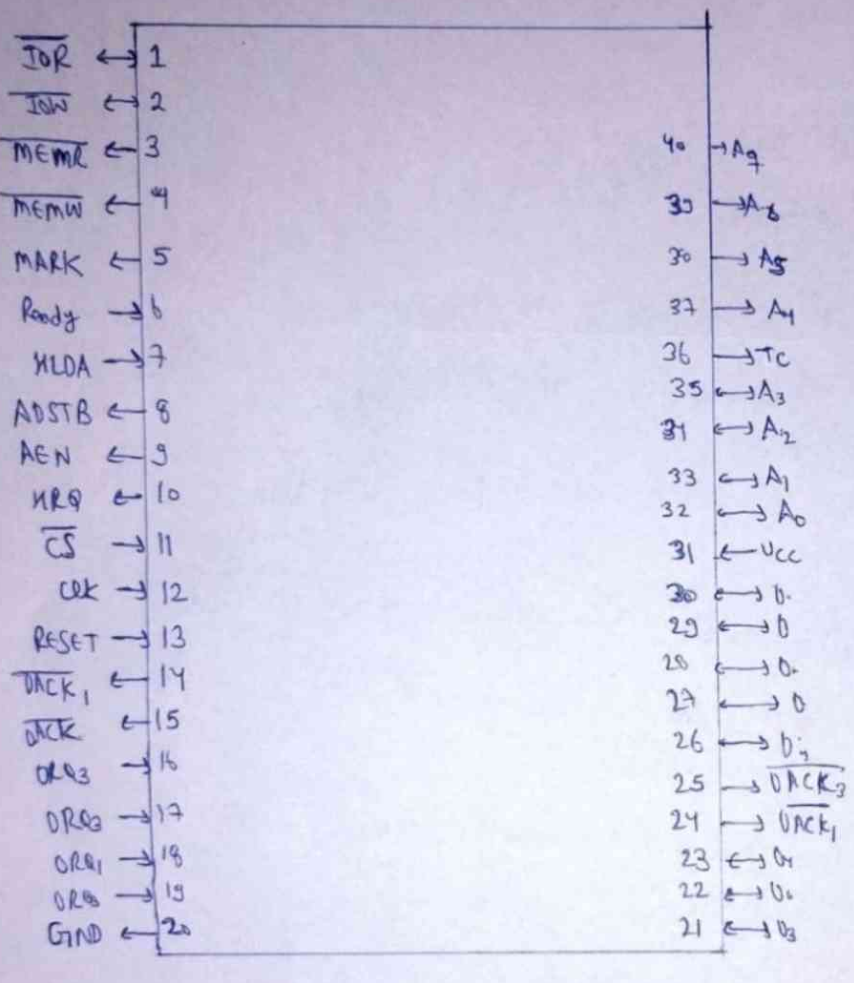
6.



8257 direct memory access controller has the following components →

1. Data bus buffer → Facilitates data transfer.
2. Address Register → Holds memory addresses for DMA transfer.
3. Control Register → Configures DMA operation modes.
4. Mode Set Register → Determines transfer modes.

7.



$D_0 - D_7$ → Data bus for transferring 8-bit data.

CS(Chip Select) → Activates the controller

IOR/IOW → I/O read and write control.

MEMR/MEMW → Memory read and write signals.

$A_0 - A_3$ → Address bus to select registers.

DREQn/DACKn → DMA request and acknowledgment for each channel.

GND/Vcc → Ground and Power.

8→ Time delays are crucial for synchronizing operations in embedded systems, ensuring appropriate intervals between tasks.

```
MOV B, 38H ; outer loop count
MOV C, FFH ; Inner loop count
DCR C      ; Decrement inner loop
JNZ        ; Jump if not zero.
DCR B      ; Decrement outer loop.
JNZ        ; Jump if not zero zero
```

9→ To calculate the number of iterations for a 1ms delay →

1. Determine the clock frequency of the system.
2. Calculate the clock period.
3. Estimate the number of clock cycles per instruction.

10→ ① I/O mode

- Mode 0 (Basic input/output) → Simple Input/output without handshaking.
- Mode 1 (Strobed Input/output) → Input/output with handshaking signals for synchronization.
- Mode 2 (Bidirectional Data Transfer) → Allows bidirectional data transfer with handshaking.

② BSR mode (Bit set/Reset) →

- This mode is used to set or reset individual bits of Port C.
- Only one bit of Port C can be modified at a time.
- The control word format for BSR mode includes:
  - D_7 → Set to 0 for BSR mode.
  - $D_3 - D_1$ → Select the bit of Port C to modify.
  - D_0 → Set to 1 to set the bit, or 0 to reset it.

→
```
MOV A2, 84H
MOV A2, A4H
MOV A2, 80H
MOV A2, A0H
```