DIGITAL ELECTRONICS [Digital Electronics and VHDL Design]





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PROBLEM

Considering following Boolean expression:

$$E_1 = a' + ab + ab'c + ab'cd$$

1. Truth Table

a	b	c	d	a'	b'	ab	ab'	ab'c	ab'cd	E1
0	0	0	0	1	1	0	0	0	0	1
0	0	0	1	1	1	0	0	0	0	1
0	0	1	0	1	1	0	0	0	0	1
0	0	1	1	1	1	0	0	0	0	1
0	1	0	0	1	0	0	0	0	0	1
0	1	0	1	1	0	0	0	0	0	1
0	1	1	0	1	0	0	0	0	0	1
0	1	1	1	1	0	0	0	0	0	1
1	0	0	0	0	1	0	1	0	0	0
1	0	0	1	0	1	0	1	0	0	0
1	0	1	0	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1	1	1	1
1	1	0	0	0	0	1	0	0	0	1
1	1	0	1	0	0	1	0	0	0	1
1	1	1	0	0	0	1	0	0	0	1
1	1	1	1	0	0	1	0	0	0	1

2. Karnaugh Map

cd \ ab	00	01	11	10
00	1	1	1	0
01	1	1	1	0
11	1	1	1	1
10	1	1	1	1

3. Simplified Equation

$$E_1 = a' + ab + ab'c + ab'cd$$

$$=$$
 a' + a(b + b'c) + ab'cd

$$= a' + a(b + c) + ab'cd \rightarrow applying De Morgan' Theorem$$

$$= a' + ab + ac + ab'cd$$

$$= a' + b + c \rightarrow taking most common part$$