Analog Devices & Intel PSG FPGA

JESD204B

Demonstration Instructions

For the
Analog Devices DAQ2 Evaluation Board
and
Intel PSG Arria 10 GX Development Kit

Version 1.0 **2/8/2017**

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1. Introduction

The Intel PSG Arria 10 GX Development Kit and Analog Devices DAQ2 Data Converter Evaluation Board together form an effective demonstration platform for the JESD204B high-speed serial interface standard. Using these components along with Analog Devices' IIO Oscilloscope software one can quickly and easily demonstrate how the Intel PSG Arria 10 FPGA and Analog Devices data converters are able to transfer data at speeds of up to 40Gbps in each direction.

This kit contains all of the hardware and software needed for this demonstration. The user only needs to provide a personal computer with an RJ45 wired Ethernet port.

Setup involves installing files from a USB flash drive, plugging in a few cables and a power supply, and connecting the demonstration kit to a host PC via the included gigabit Ethernet cable.

1.1 Theory of Operation

Fundamentally, this demonstration showcases the ability to have an Intel PSG FPGA communicate with high-speed DACs and ADCs via the JESD204B standard.

The FPGA provides many capabilities in this demonstration. To start with, the primary means of configuring the DAC outputs and receiving the ADC inputs happens via dedicated IP blocks in the FPGA fabric. A wired Ethernet connection between the FPGA and the host PC is used to transfer the data to and from the host IIO Oscilloscope application and the Linux OS running on the NIOS processor in the FPGA as well. The FPGA also provides the gigabit transceivers necessary to communicate to the JESD204B capable DAC and ADC from Analog Devices.

The data provided to the JESD204B capable DAC is supplied from one of a couple of sources. The FPGA can create a digital sine wave via a Direct Digital Synthesizer (DDS) or read in a data file representing a digital signal. The digital data is packaged and sent to the JESD204B IP block inside the FPGA then transmitted to the DAC over a FPGA Mezzanine Card (FMC) connection on four 10Gbps channels; this is defined as the transmit path.

Once the data has been received and decoded by the JESD204B DAC, it is transmitted over RF loopback cables to the JESD204B ADC. The ADC packages the received data and sends it to the FPGA over the FMC connection on four additional 10Gbps channels; the receive path.

Once the data is captured in the FPGA it is sent over the gigabit Ethernet connection the host PC running the IIO Oscilloscope application that has the ability to plot the data in time and frequency domains as well as constellation plots.

2. Data Flow/Signal Path

Here is a brief description of the signal as it flows from the FPGA across the JESD204B interface to the data converters and back. Refer to Figure 1.

2.1 Transmit Path

1. Using the ADI IIO Oscilloscope graphical user interface on a host PC and a gigabit Ethernet cable connected to the Arria 10 FPGA, a single frequency digital sine wave is parameterized in the 0-500MHz range via the FPGA's internal DDS frequency synthesizer blocks or a data file with a digital signal representation is selected.
2. This digital signal is converted into the JESD204B format via the Arria 10's internal IP and sent out across 4 lanes to an FMC connector on the Arria 10 development kit at a rate of 40Gbps (4 lanes @ 10Gbps each).
3. The data flows through the corresponding FMC connector on the AD-FMCDAQ2-EBZ board and into the AD9144 multichannel high-speed DAC where it is converted from the JESD204B standard to the proper digital format prior to being converted to analog. The AD9144 DAC generates both I and Q signals used for quadrature amplitude modulation (QAM) of the RF signal, converts it to analog and sends each signal out via SMA RF connectors connected to RG316 RF coaxial cables.

2.2 Receive Path

4. The analog RF signals flow through the two coaxial cables and back into the AD-FMCDAQ2-EBZ board through two additional SMA RF connectors routed to the AD9680 2-channel ADC. The signal is sampled and digitized and converted back into the JESD204B standard.
5. The data is sent back along 4 lanes also at a rate of 10Gbps per lane (40Gbps total) across the FMC connector to the Arria 10 GX kit where it is decoded by Arria 10 FPGA IP blocks.
6. The received data is sent to the host PC over the gigabit Ethernet connection. Using the ADI IIO Oscilloscope graphical user interface application on the host, the received data can be viewed in the time domain, frequency domain or as a polar plot.

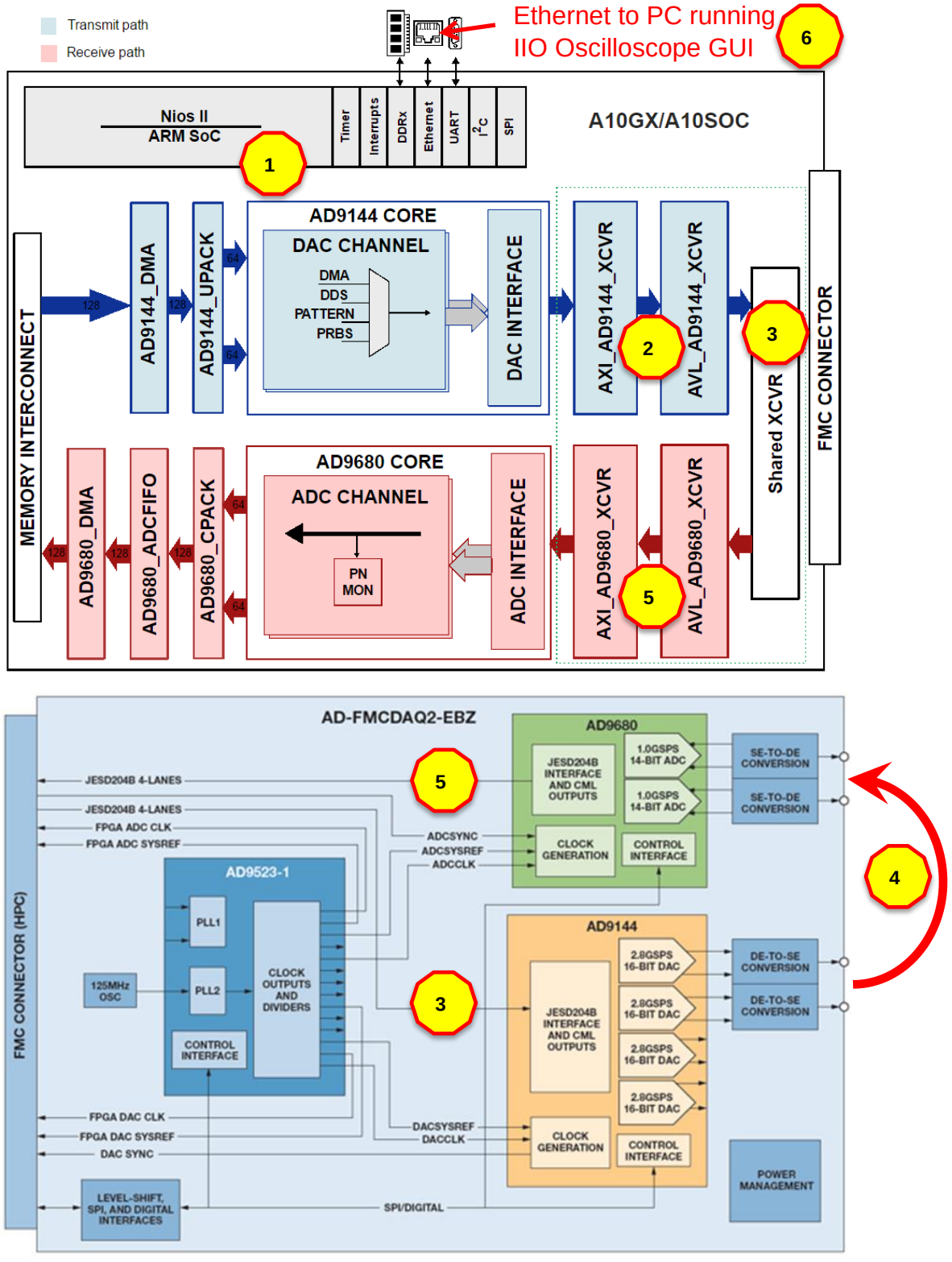


Figure 1: JESD204B Demonstration Platform Block Diagram

3. Required Hardware

3.1 Intel PSG Arria 10 GX Development Kit

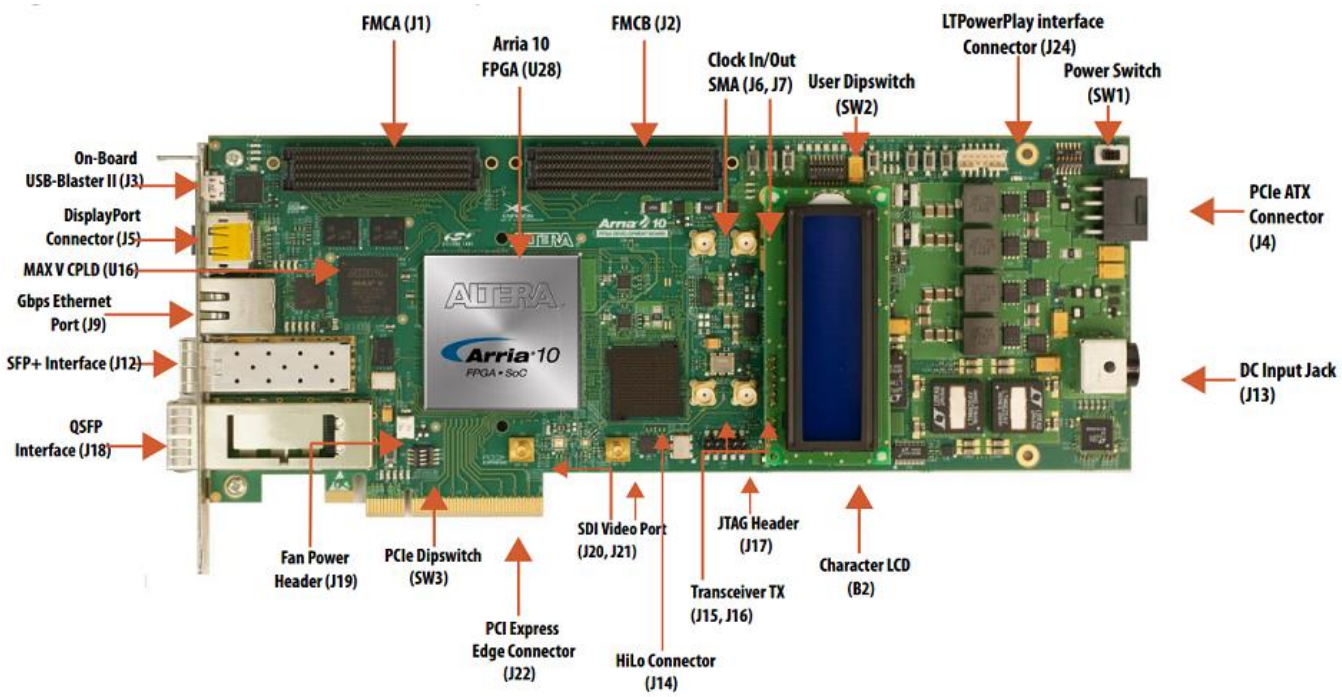


Figure 2: Arria 10 GX FPGA Development Kit (Power Supply not shown)

- https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-a10-gx-fpga.html

User guide: https://www.altera.com/content/dam/altera-www/global/en_US/support/boards-kits/arria10/FPGA/A10-FPGA-ES3-DK-UG_1.pdf

The Arria 10 GX FPGA Development Kit includes the following hardware.

- Arria 10 GX 10AX115S2F45I1SG2 FPGA
- 1 GB DDR4 SDRAM, 2GB DDR3 SDRAM, or RLDRAM3 (16 Meg x 36) (daughter cards)
- Two FMC loopback interfaces supporting gigabit transceivers, LVDS and single-ended I/Os
- One quad small-form-factor pluggable (QSFP) and one SFP+ port
- PCIe x8 edge connector
- Serial digital interface (SDI) channel
- Character LCD
- AC adapter power cables
- Ethernet and USB cables

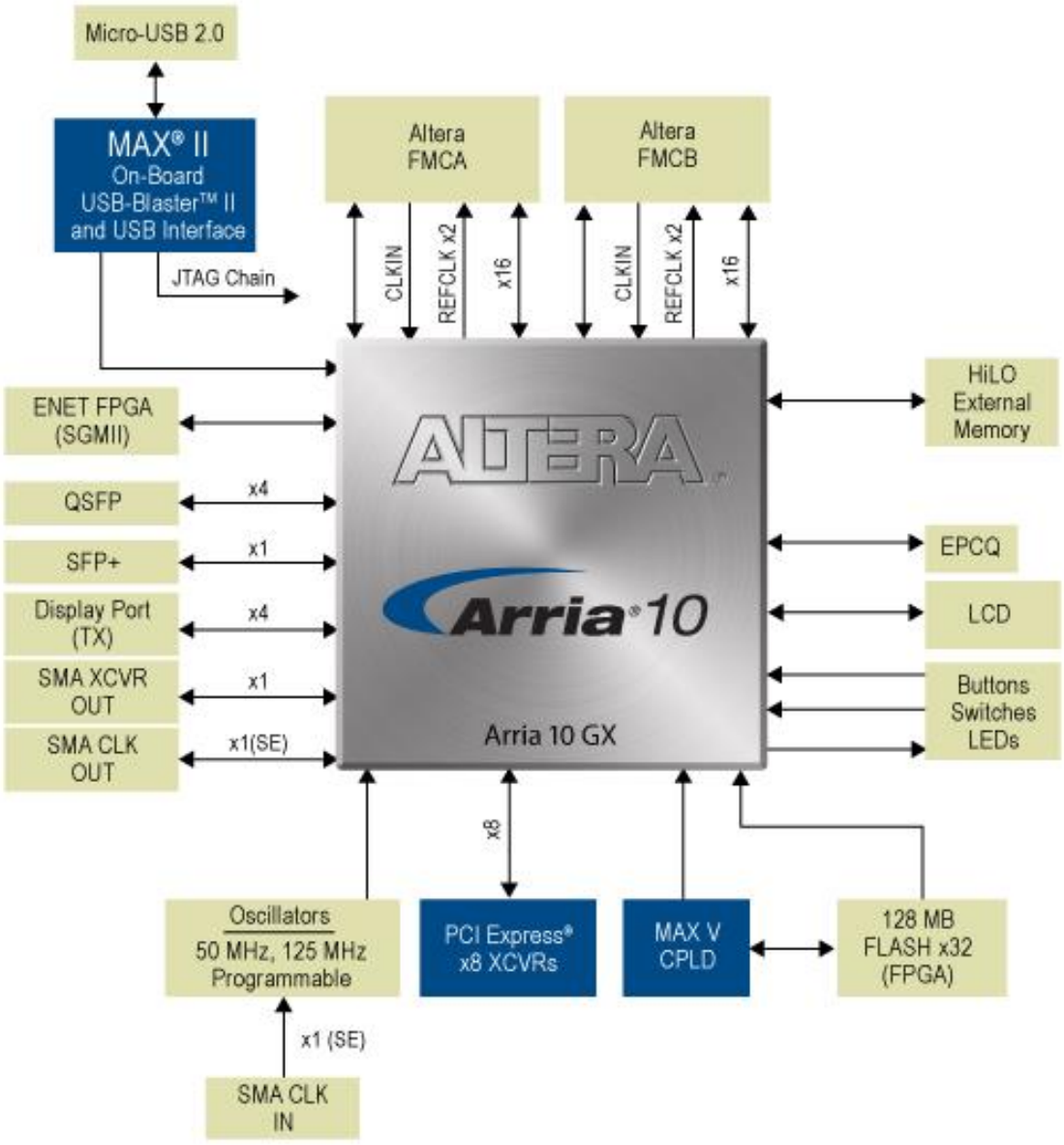


Figure 3: Arria 10 GX Development Board Block Diagram

3.2 Analog Devices DAQ2 Evaluation Board

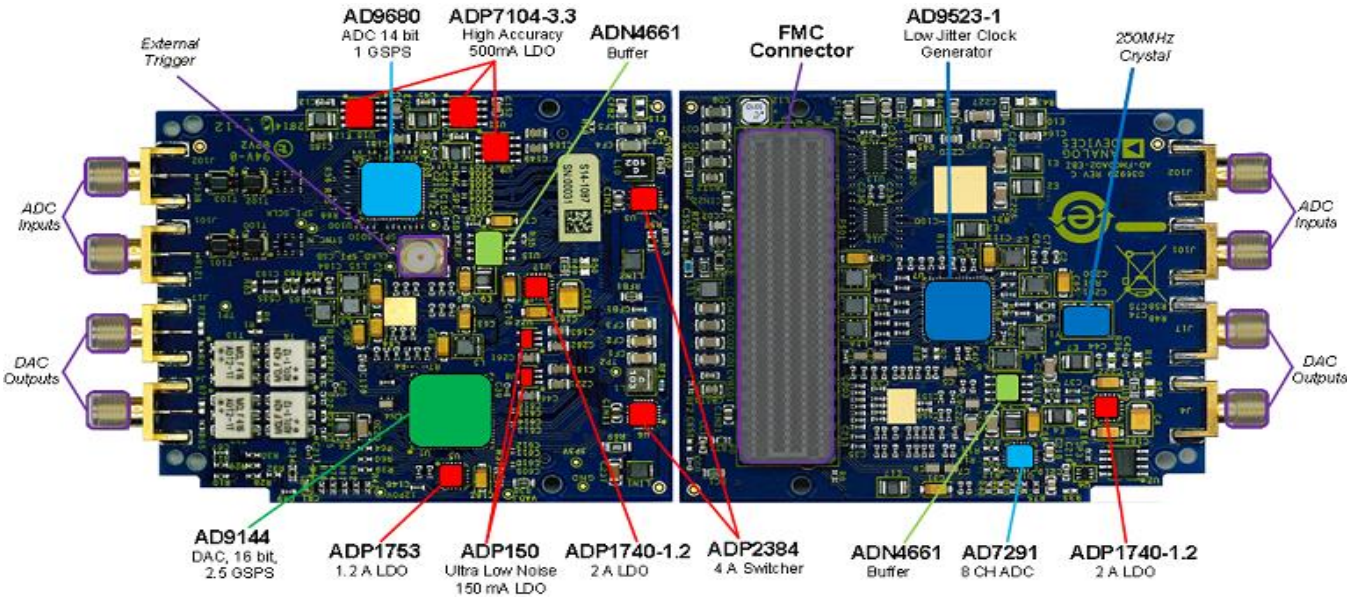


Figure 4: Analog Devices AD-FMCDAQ2-EBZ Evaluation Board Top (Left) and Bottom (Right)

- http://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad-fmcdaq2-ebz.html

The AD-FMCDAQ2-EBZ Evaluation Board contains the following.

- AD9680 2-channel 14-Bit 1.0GSPS JESD204B ADC
- AD9144 4-Channel 16-Bit 2.8GSPS JESD204B DAC
- AD9523-1 14-Output 1GHz Clock Generator
- FPGA Mezzanine Card (FMC) High-Speed Connector

Also:

- AD7291 8-Channel 12-Bit ADC
- Miscellaneous Power and Timing components

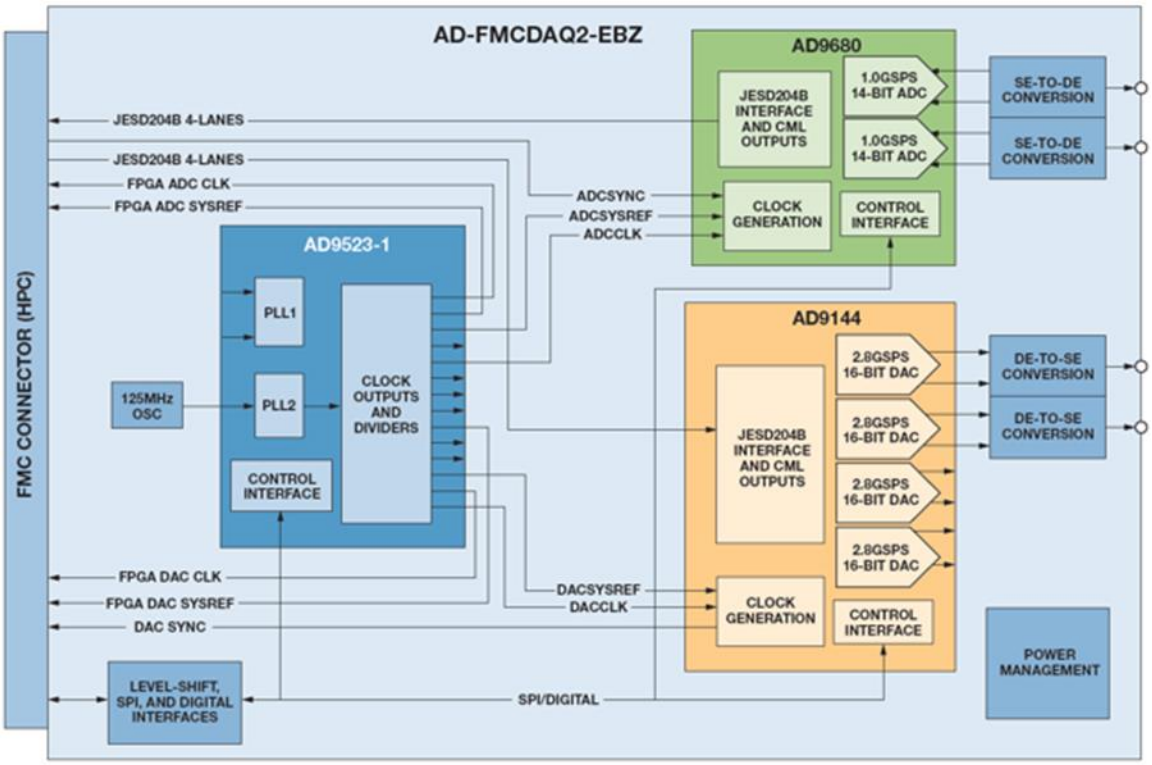


Figure 5: AD-FMCDAQ2-EBZ Evaluation Board Block Diagram

3.3 RG316 SMA RF cables (x2)

Figure 6: RF Loopback cables

- https://www.arrow.com/en/products/135101-01-06.00/amphenol

3.4 Cat-5e (or better) gigabit Ethernet patch cable

Figure 7: Gigabit Ethernet cable

3.5 Kit Contents

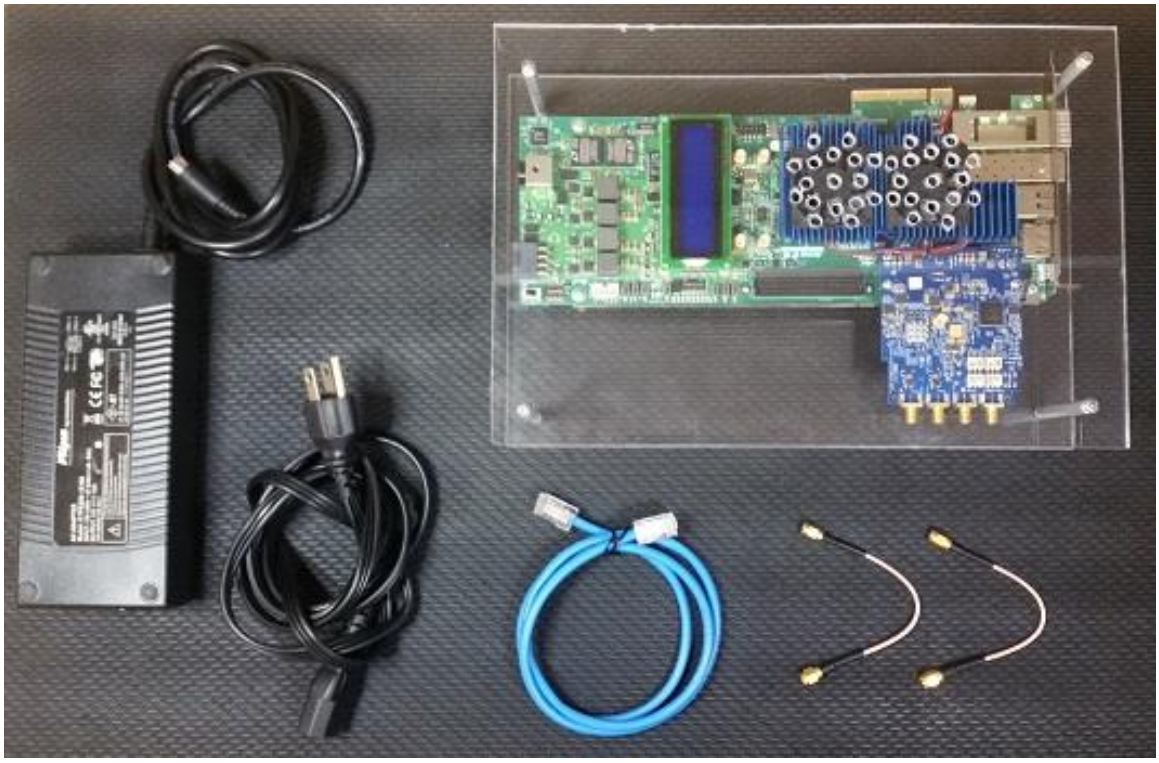


Figure 8: Contents of Intel PSG/ADI JESD204B Demo Kit (Not Shown: USB Flash drive, 'Pelican' Case)

4. Required Software

All necessary software applications and files listed below are provided in the JESD204B_Demo.zip file on the provided USB flash drive. There is no need to install the Intel PSG Quartus Prime tool chain to run this demonstration.

4.1 Applications

- Analog Devices IIO Oscilloscope – **OSC.exe**
  - The ADI IIO Oscilloscope is an example application, which demonstrates how to interface different evaluation boards from within a Linux system. The application supports plotting of the captured data in four different modes (time domain, frequency domain, constellation and cross-correlation). The application also allows a user to view and modify several settings of the evaluation board's devices.
  - The IIO Oscilloscope application installer is provided in the JESD204B_Demo.zip file.
  - Optional web link: https://github.com/analogdevicesinc/iio-oscilloscope/releases/download/v0.5-master/adi-osc-master-setup.exe
- DHCP Server – **OpenDHCPServer.exe**
  - A simple DHCP server is required so that the network interface of the Arria 10 FPGA is assigned an IP address within the same subnet as the host PC.
  - The DHCP server application is provided in the JESD204B_Demo.zip file.
  - Optional web link: https://sourceforge.net/projects/dhcpserver/

4.2 Files

- Arria 10 JESD204B Demonstration batch file – **JESD204B_Demo.bat**
  - The JESD204B_Demo.bat batch file temporarily assigns a static IP address to the host PC, starts the DHCP server then resets the host Ethernet network to DHCP on exit.
  - The batch file is provided in the JESD204B_Demo.zip file.
- DHCP Server configuration settings – **OpenDHCPServer.ini**
  - Required by the OpenDHCPServer application.
  - The configuration settings file is provided in the JESD204B_Demo.zip file.

5. Hardware Setup

The instructions in this section will guide you through the hardware setup of the JESD204B demonstration platform using the Arria 10 GX FPGA Development Kit and the Analog Devices DAQ2 JESD204B Evaluation Board.

1. The AD-FMCDAQ2-EBZ should already be connected via the FMC connector to the **PORT A** FMC connector on the Arria 10 GX board.

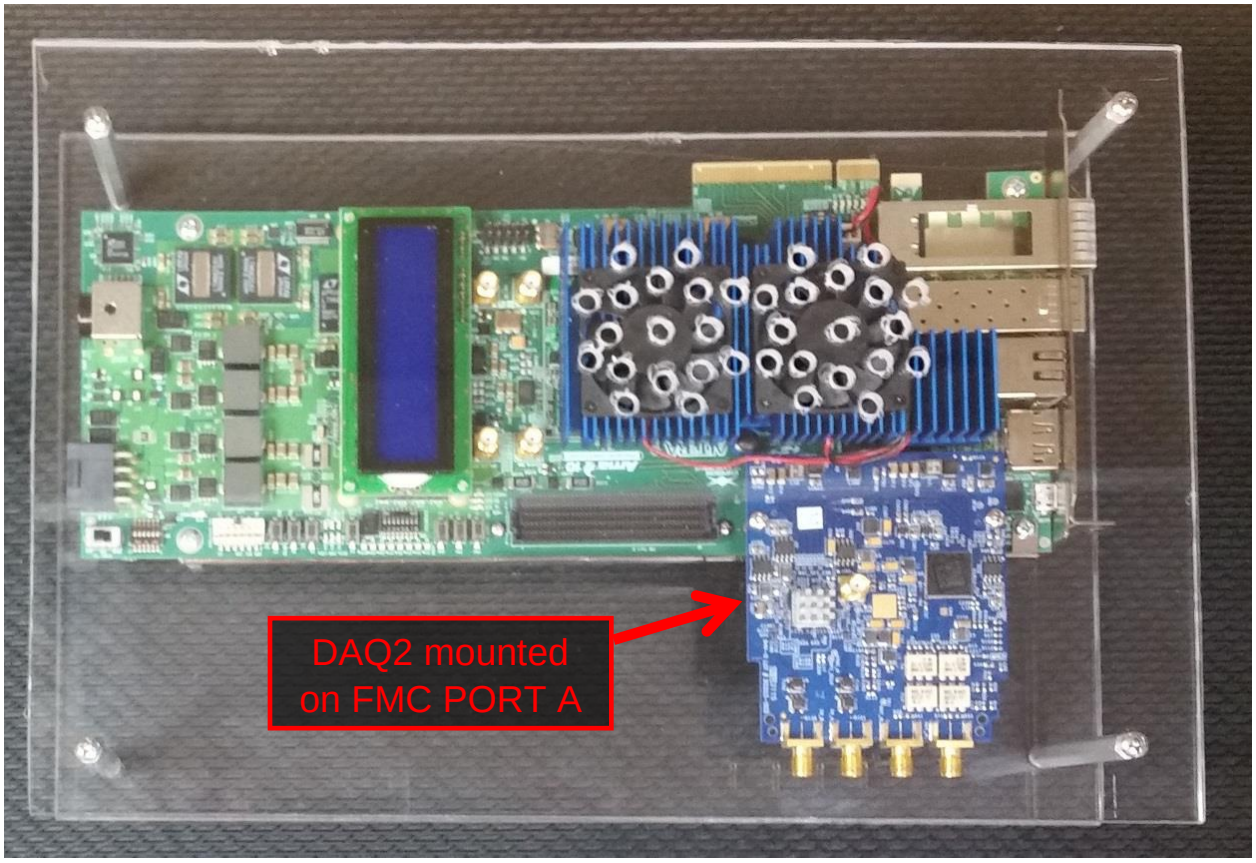


Figure 9: AD-FMCDAQ2-EBZ connected via FMC connector to Port A on Arria 10 GX board

2. On the AD-FMCDAQ2-EBZ hook up the two provided RG316 RF cables:
   a) Connect one cable from the SMA connector labeled **OUT_A** to the **IN_A** SMA connector.
   b) Connect the second cable between the **OUT_B** and **IN_B** SMA connectors as shown.

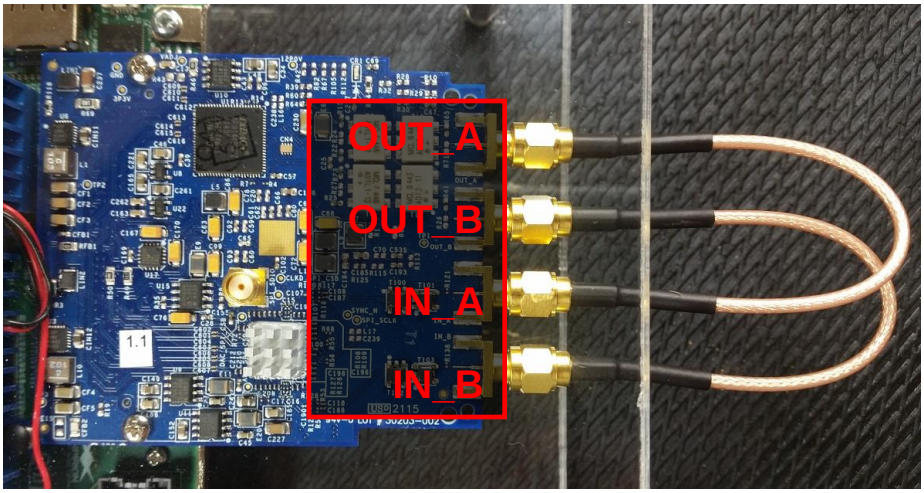


Figure 10: RF cable connections

3. Using the Cat-5e gigabit Ethernet cable connect the Arria 10 GX kit directly to the host PC via the RJ45 Ethernet port on each. Important: the use of a gigabit capable Ethernet patch cable is required due to the high data rates of the JESD204B interface.

   Note: This demonstration does not require access to the Internet to function. However, the PC's WiFi connection may stay active with Internet access without negatively impacting this demonstration.

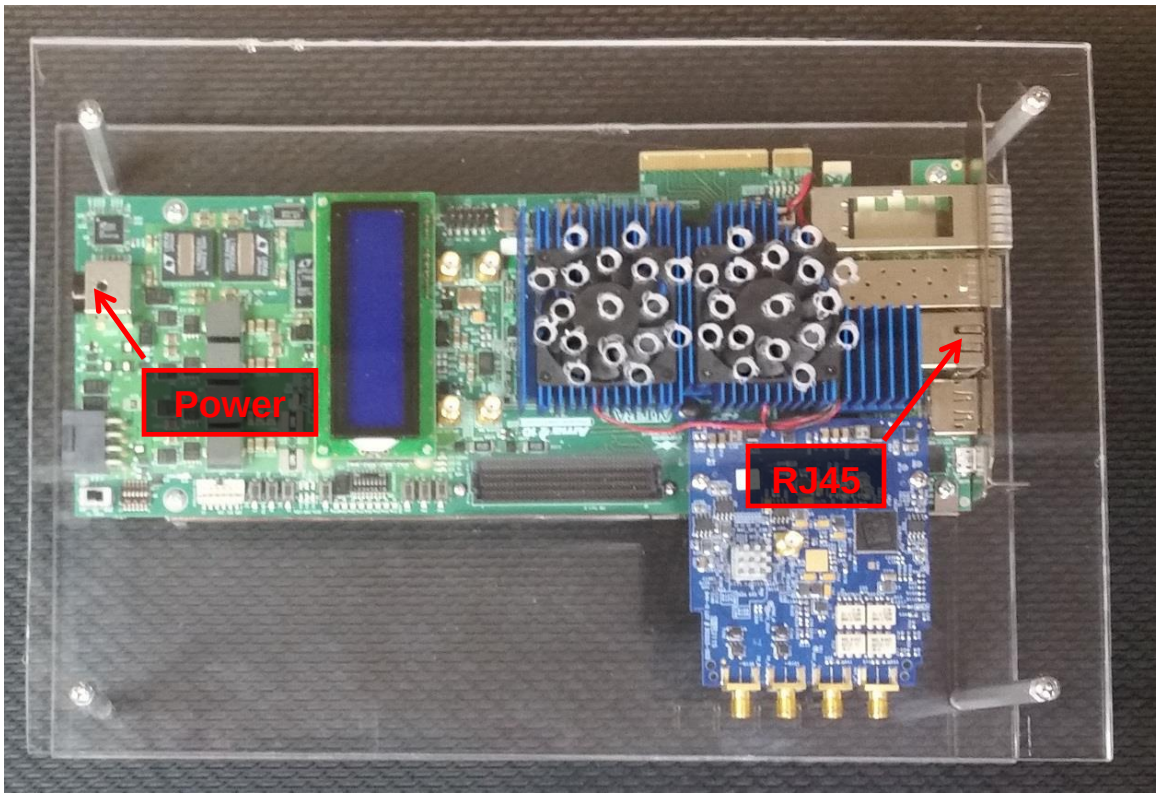


Figure 11: Power and Ethernet connections on Arria 10 GX Development Kit

4. Plug the included power supply into the Arria 10 GX board's 4-pin connector and into a 110V outlet.

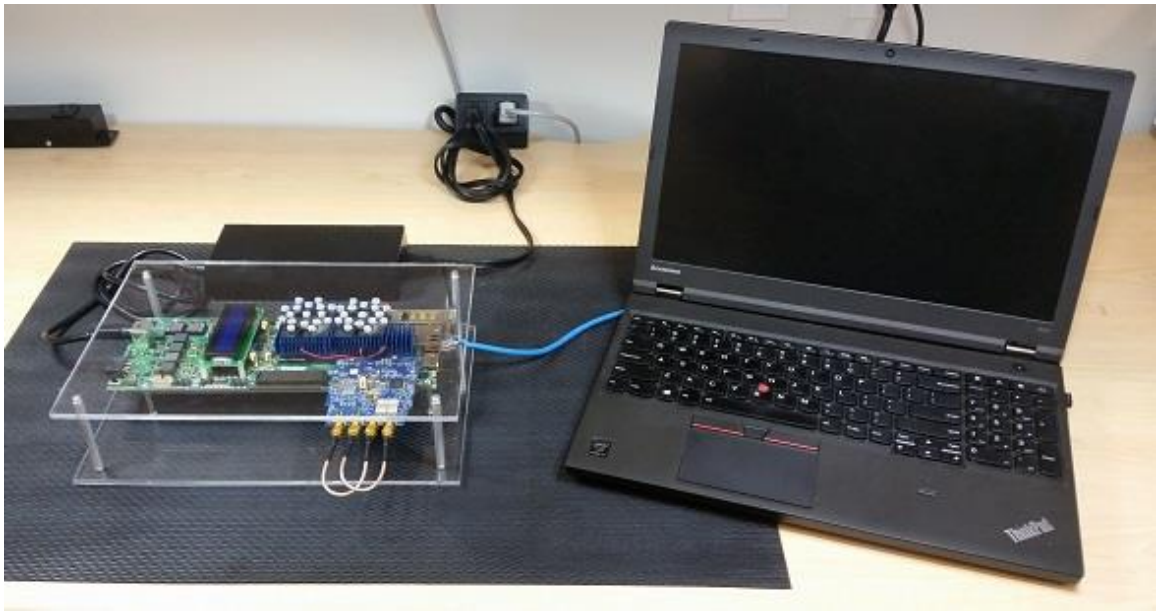


Figure 12: Complete Demo Setup

6. Software Setup

The instructions in this section will guide you through the software setup of the JESD204B demonstration.

1. Extract all files from the **JESD204B_Demo.zip** file on the provided USB Flash drive to the host PC into any directory.

After extracting the zip archive there will be 4 items.

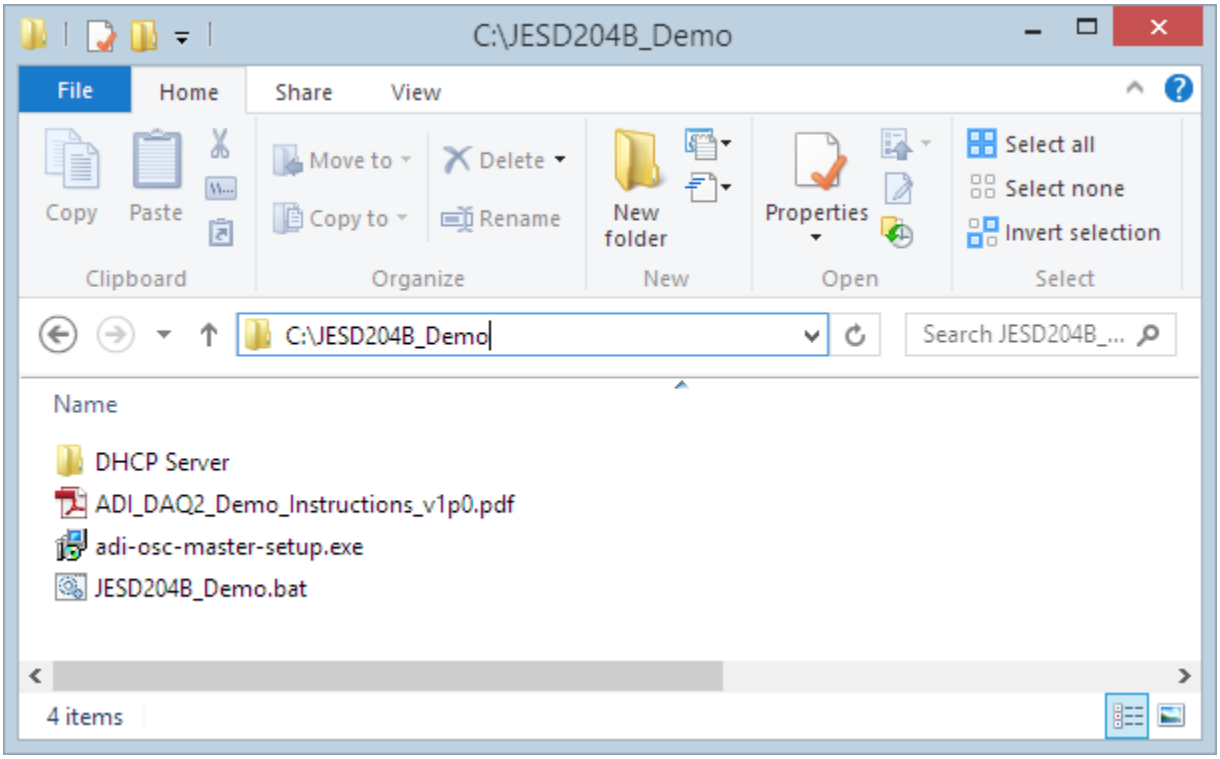
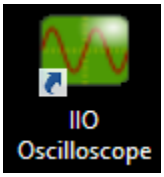


Figure 13: Extracted JESD204B Archive

2. Install the Analog Devices IIO Oscilloscope application by double-clicking the **adi-osc-master-setup.exe** installer. Accept **ALL** the defaults and accept the License Agreement. Also check the box labeled 'Create a desktop icon'.

After installing the IIO Oscilloscope there will be a new **IIO Oscilloscope** Desktop icon.

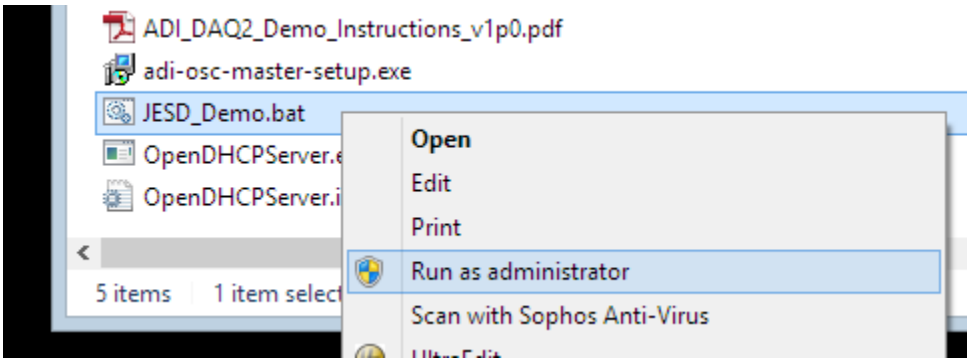


7. Running the Demonstration

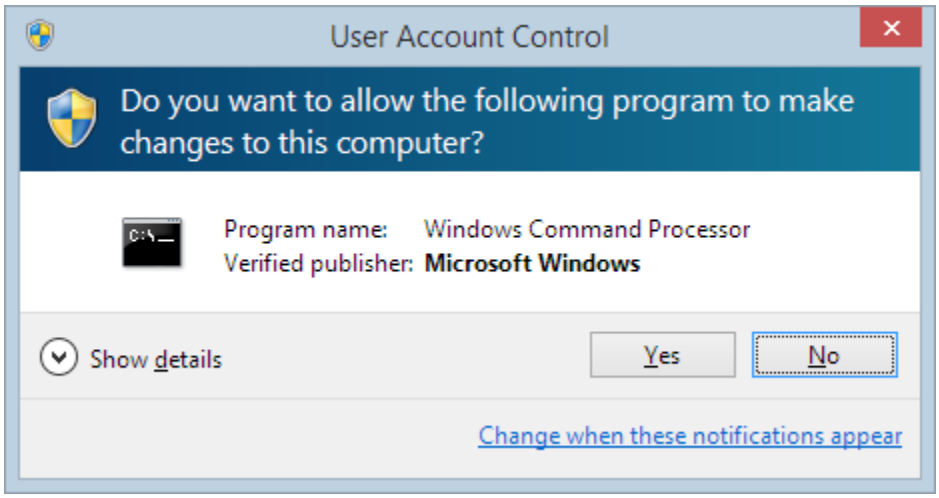
This section describes how to run the JESD204B demonstration including powering up the hardware and making a connection to the system with the IIO Oscilloscope application. An initial configuration of the transmitters is described and details on creating plots of the received data are covered.

7.1 Start the DHCP Server

1. Launch the **JESD204B_Demo.bat** batch file as **administrator** by right-clicking the file and selecting **Run as administrator**.

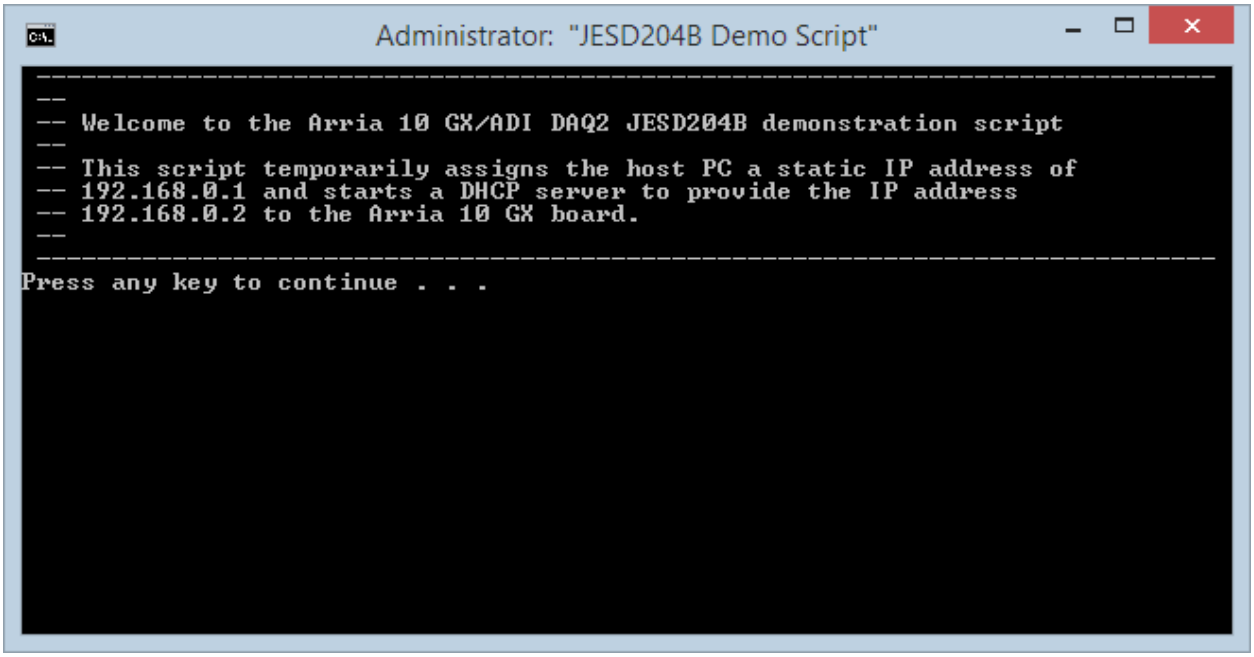


2. Select **Yes** on the **User Account Control** dialog allowing the script to execute.

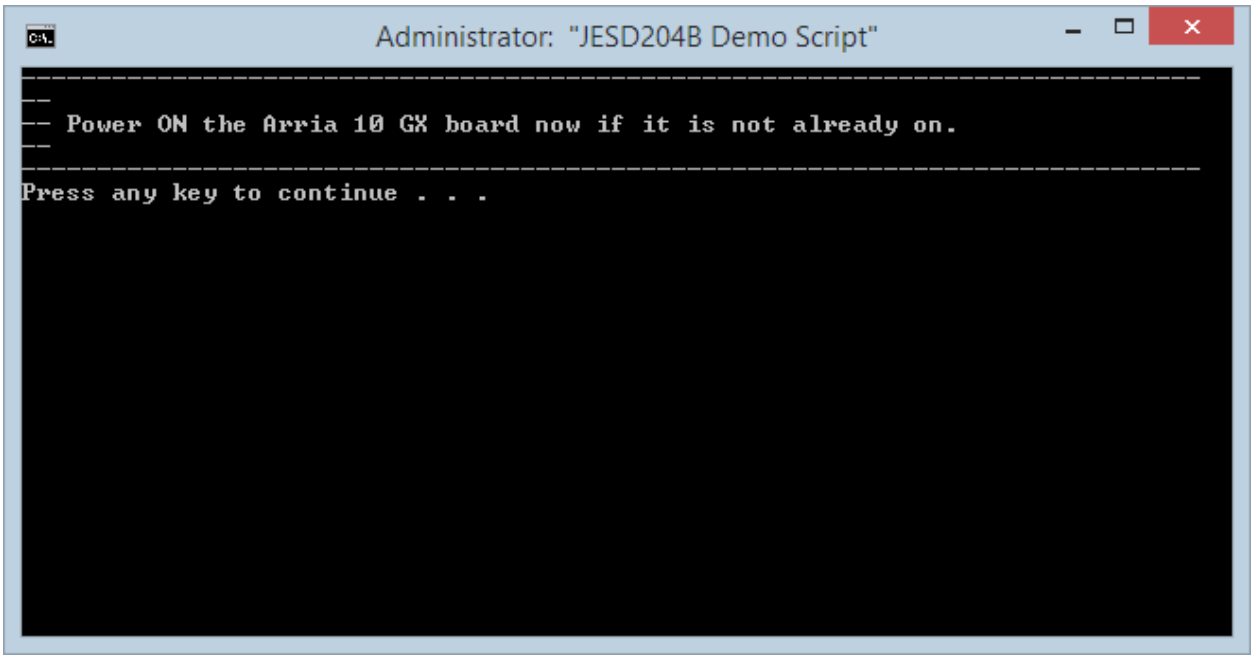


The "**JESD204B Demo Script**" window will open providing information about the script.

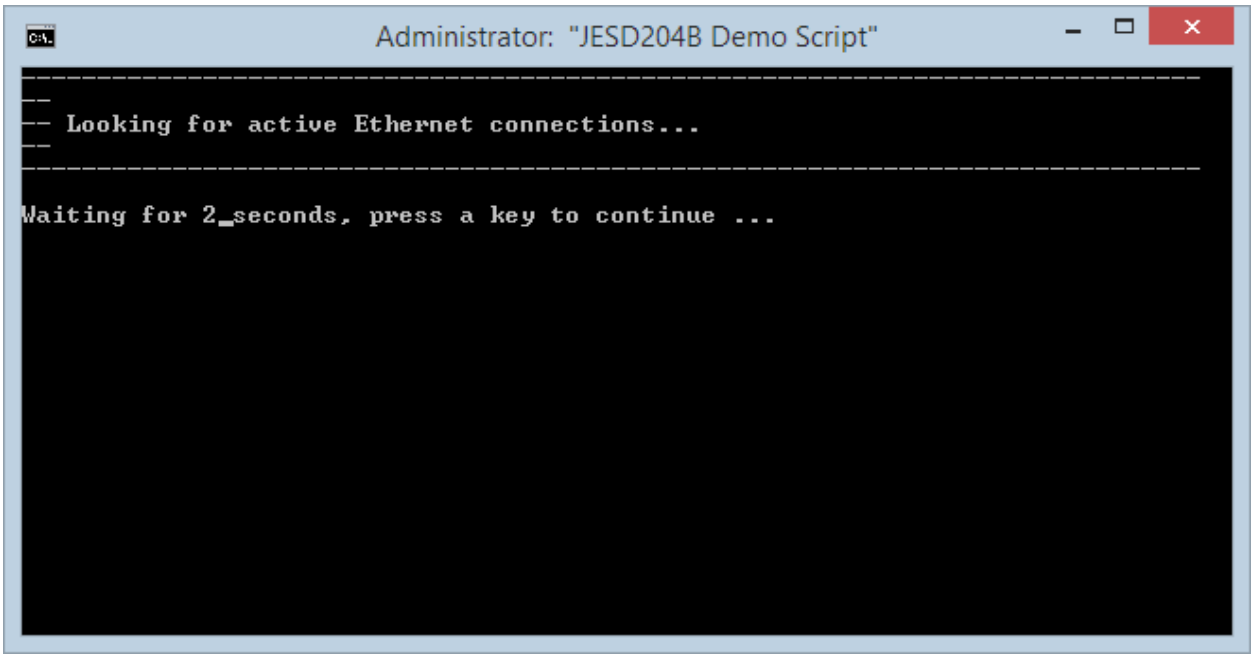
3. **Press any key** on the PC keyboard to continue.



4. Move the power switch, **SW1,** on the Arria 10 GX kit to the **ON** position and **press any key** on the keyboard. Upon power-up, the FPGA will be programmed from the preconfigured CFI flash on the Arria 10 GX kit. The 8 red LEDs will be illuminated upon successful FPGA configuration.

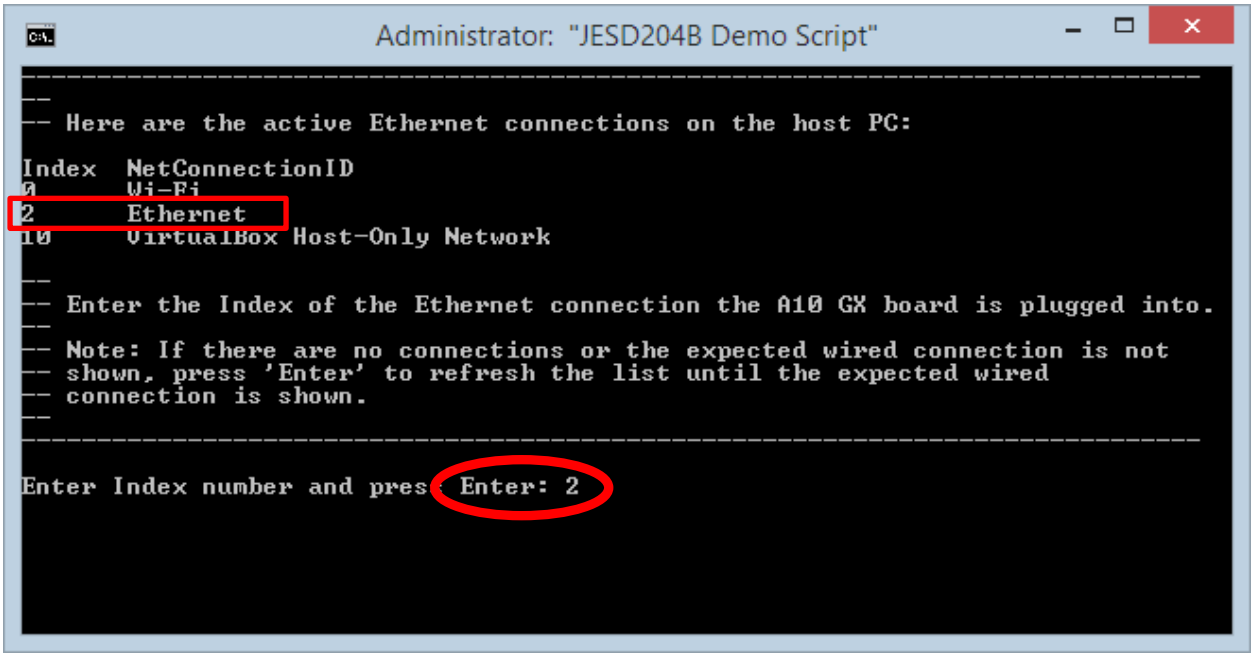


The script will query the PC Ethernet connections for 5 seconds and automatically report back the active interfaces.

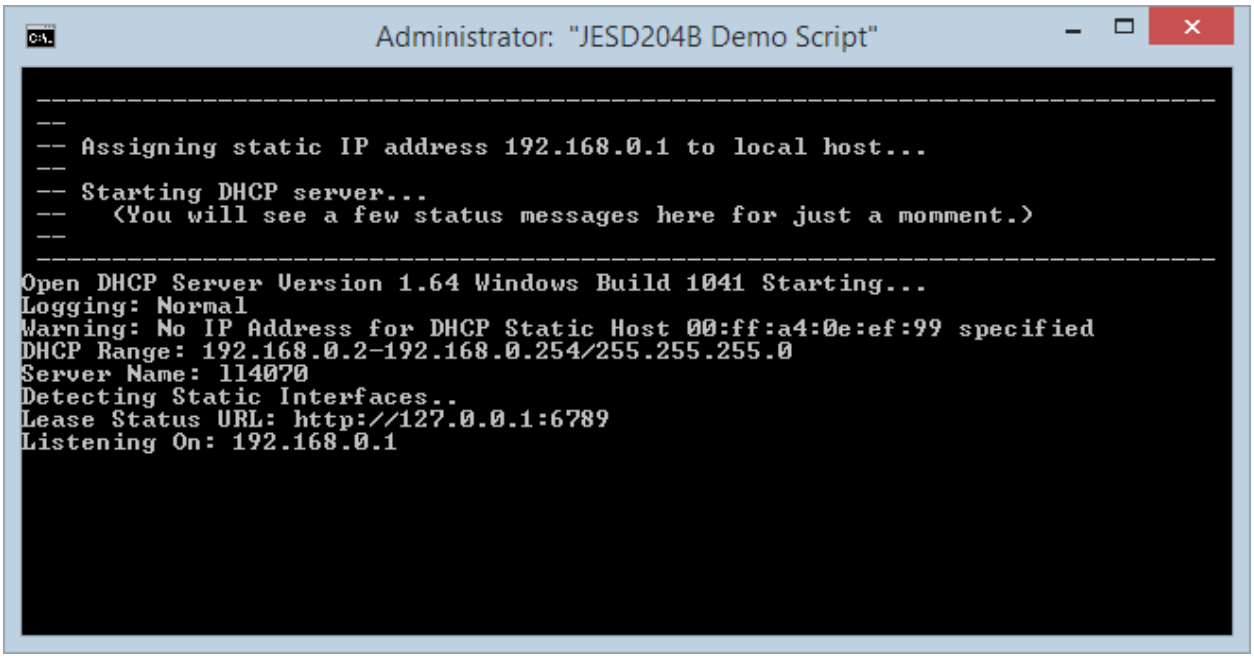


Note: The name of the connections may vary. ('Local Area Connection' or 'Ethernet' are common.)

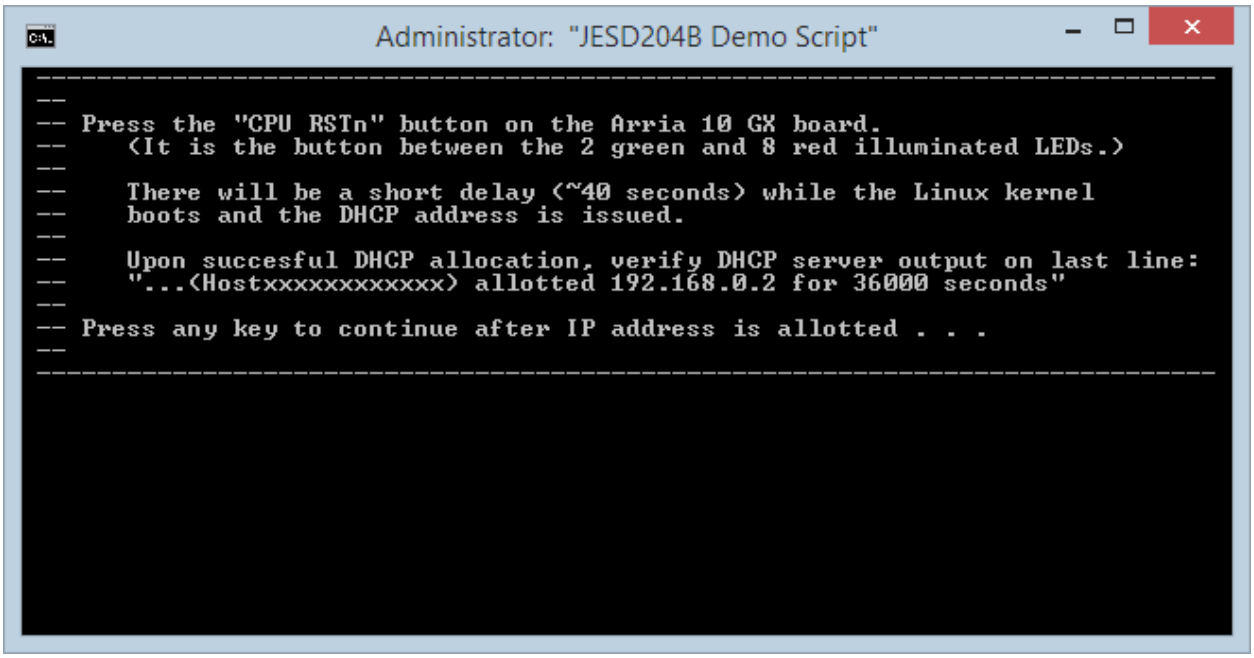
5. Enter the **Index** number of the Ethernet connection which the A10 GX board is plugged into and press **Enter**. (Index = 2 for "Ethernet" in the below example.)



Status messages will appear with information concerning assigning the static IP address to the host and starting the DHCP server. These messages will only appear for a few seconds and then disappear.

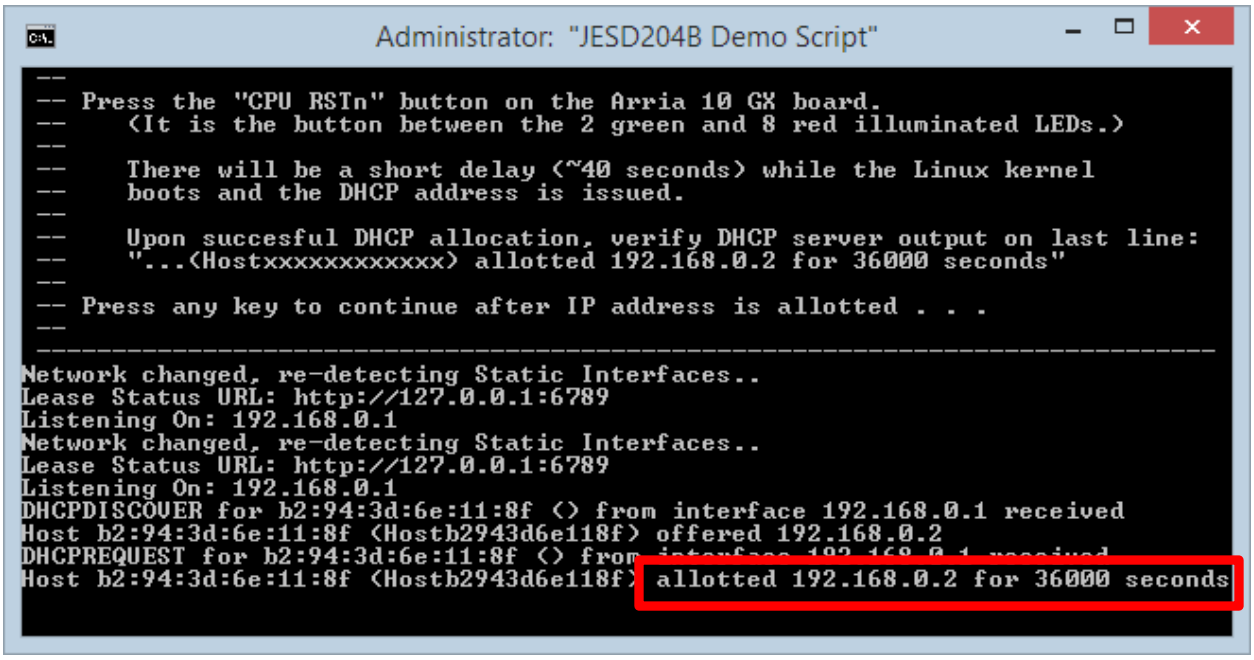


6. Press the **"CPU RSTn"** button on the Arria 10 GX board forcing the NIOS processor into reset and reloading of the Linux kernel. The button is located between the 2 green and 8 red illuminated LEDS.



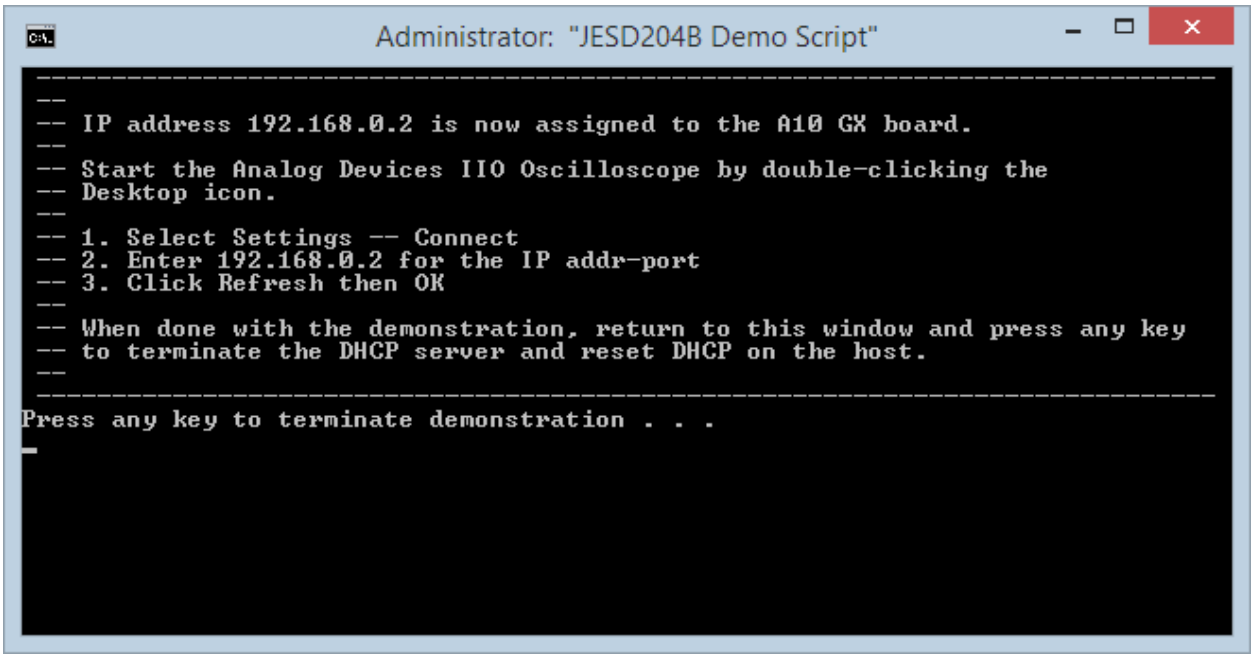
Additional DHCP server status messages will appear with information concerning assigning the static IP address to the Arria 10 GX. Upon successful DHCP allocation, verify the static IP address 192.168.0.2 was assigned to the Arria 10 GX.

7. **Press any key** once the status message "**Host xx:xx:xx:xx:xx:xx (Hostxxxxxxxxxxxx) allotted 192.168.0.2 for 3600 seconds**" appears. (Note: The "xx" values will vary depending on the host PC MAC address.)



The script output now provides additional information about running the demonstration.

Note: **DO NOT** press any additional keys while in this window or close this window until the demonstration is completed as it will terminate the DHCP server and sever the connection between the PC and the Arria 10 GX FPGA. See section 7.4.



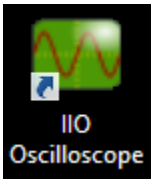
7.2 Connect the IIO Oscilloscope

There are two components to IIO Oscilloscope application that is run on the host PC: configuration and plotting.

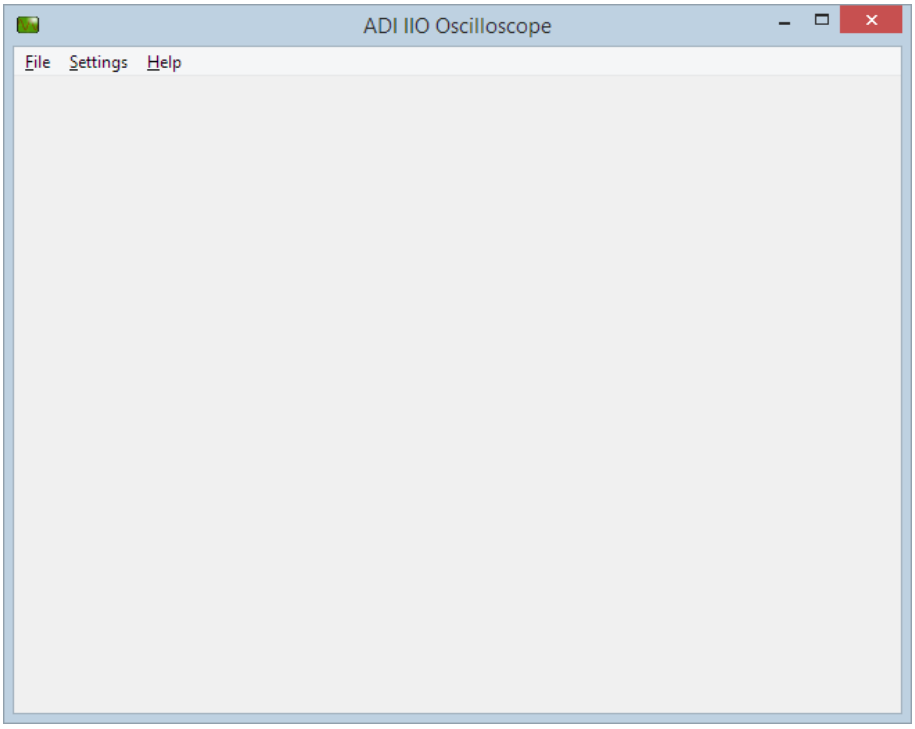
The configuration dialogs provide for choosing the digital signal data that is to be sent to the AD9144 DAC as well as putting the AD9380 ADC into test modes. The AD9144 data is either "tones" that are the output generated by the Arria 10 DDS frequency synthesizer blocks or data files containing digital represntations of a signal.

The plotting component of the IIO Oscilloscope application allows the user to view the data received by the Arria 10 after the signal has made a complete loop from the FPGA, through the JESD204B interface to the DAC, through the RF cable back into the ADC, again through a JESD204B interface and back into the FPGA. The plots can display data in the time or frequency domain as well as constealation and cross correleation plots.

1. Launch the **IIO Oscilloscope** application by double-clicking the icon on the Desktop.

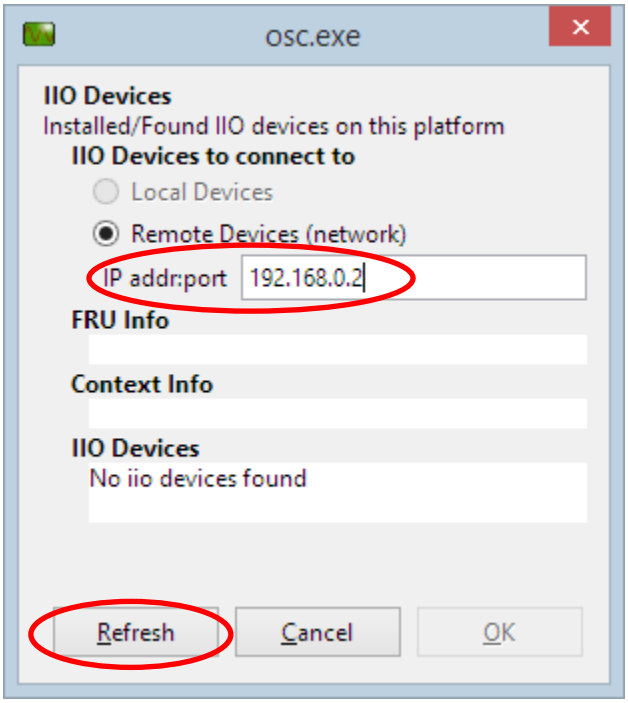


2. The IIO Oscilloscope application will start with a blank window.

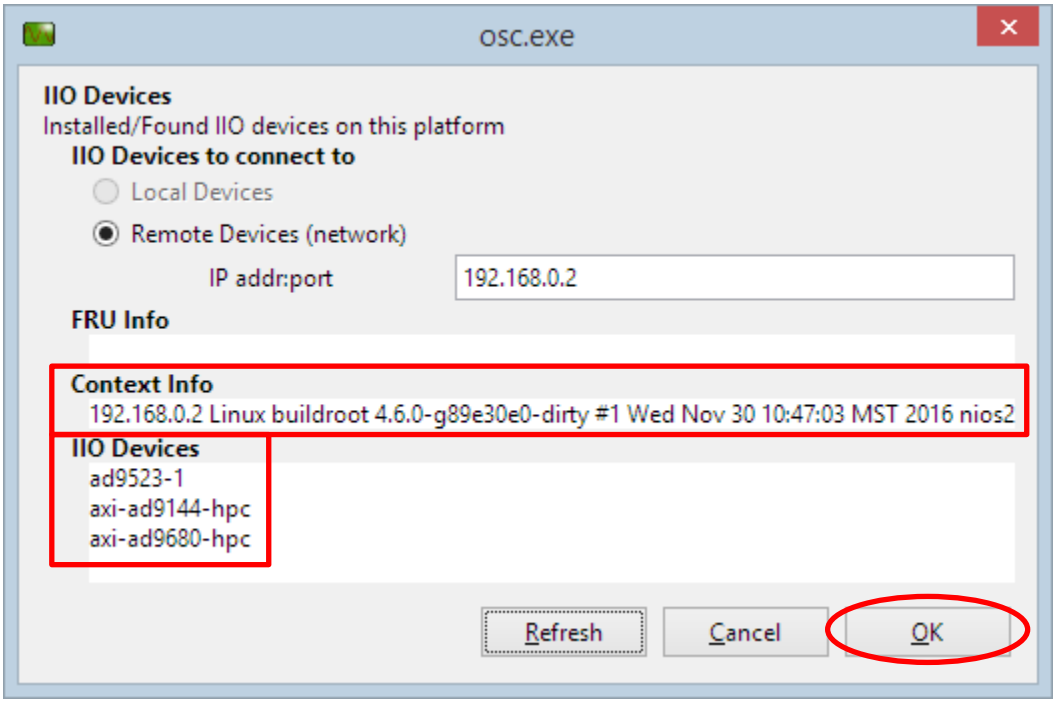


3. Establish a network connection from the IIO Oscilloscope application by selecting **Settings -> Connect**

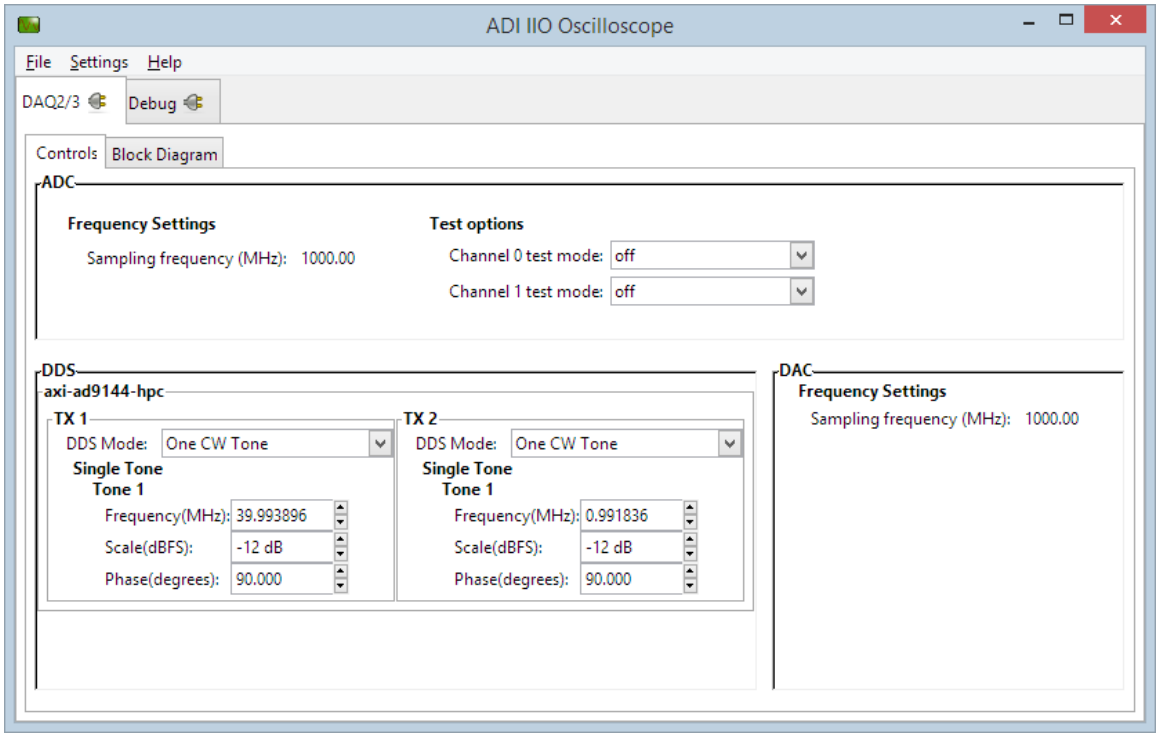
4. Enter the IP address **192.168.0.2** into the **IP addr:port** field and click **Refresh.**



5. A successful connection is verified by observing the **Context Info** and **IIO Devices** fields as shown here. Click **OK.**



The ADI IIO Oscilloscope window will now be populated as shown (some values may differ):

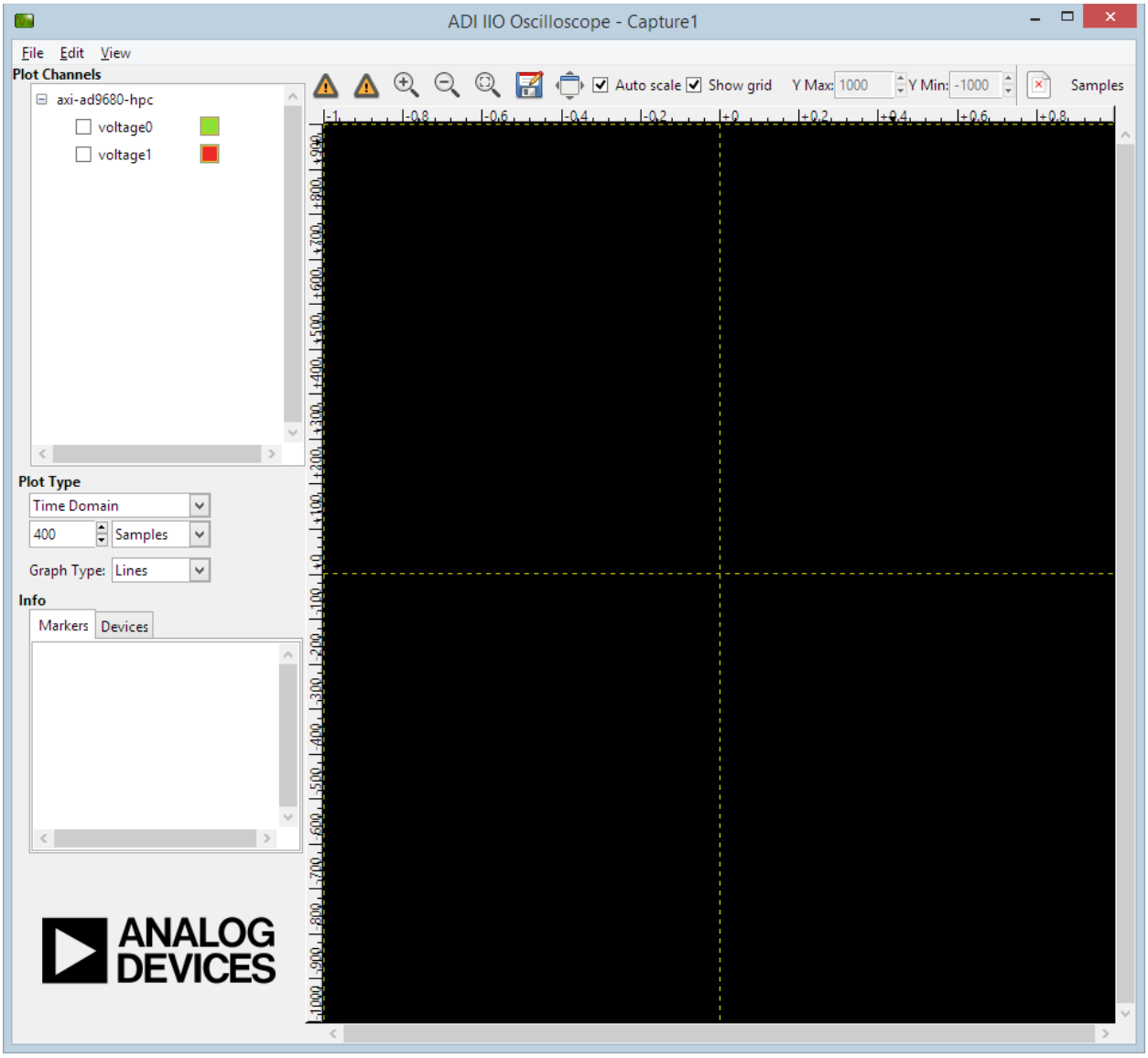


6. Enable the FPGA IP to generate a 40 MHz sine wave for the AD9144 **TX 1** channel by highlighting the **Frequency(Mhz)** field and typing in '**40**'. Set amplitude by typing '**-12**' in **Scale(dBFS)** window then press **Enter**. Note: The frequency requested will be adjsted to closest match possible that the FPGA DDS IP blocks can synthesize.

Note: TX 2 is not enabled for this demo setup. Set 'DDS Mode' to 'Disable' just as a reminder.

7.3 Create Plots

1. In the **ADI IIO Oscilloscope** window, using the pull-down menu select **File -> New Plot.**
   A new **ADI IIO Oscilloscope – Capture 1** window will open:



2. Check the selection boxes next to **voltage0** and **voltage1** in the **Plot Channels** panel. These equate to the I & Q channels respectively for the Analog Devices AD9144 DAC.

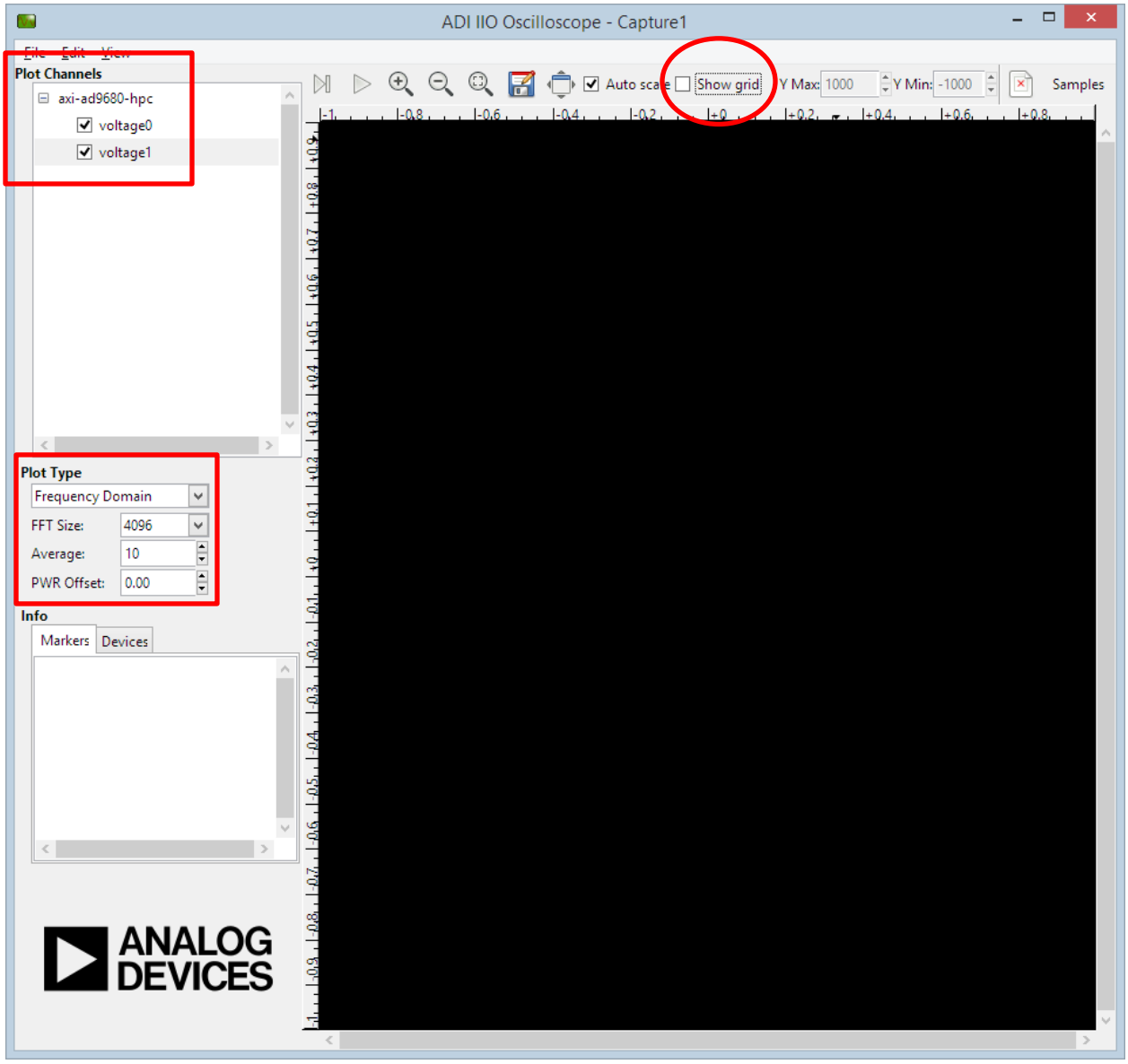
3. Change the **Plot Type** to **Frequency Domain** via the drop-down list.

4. Change the **FFT Size** to **4096**

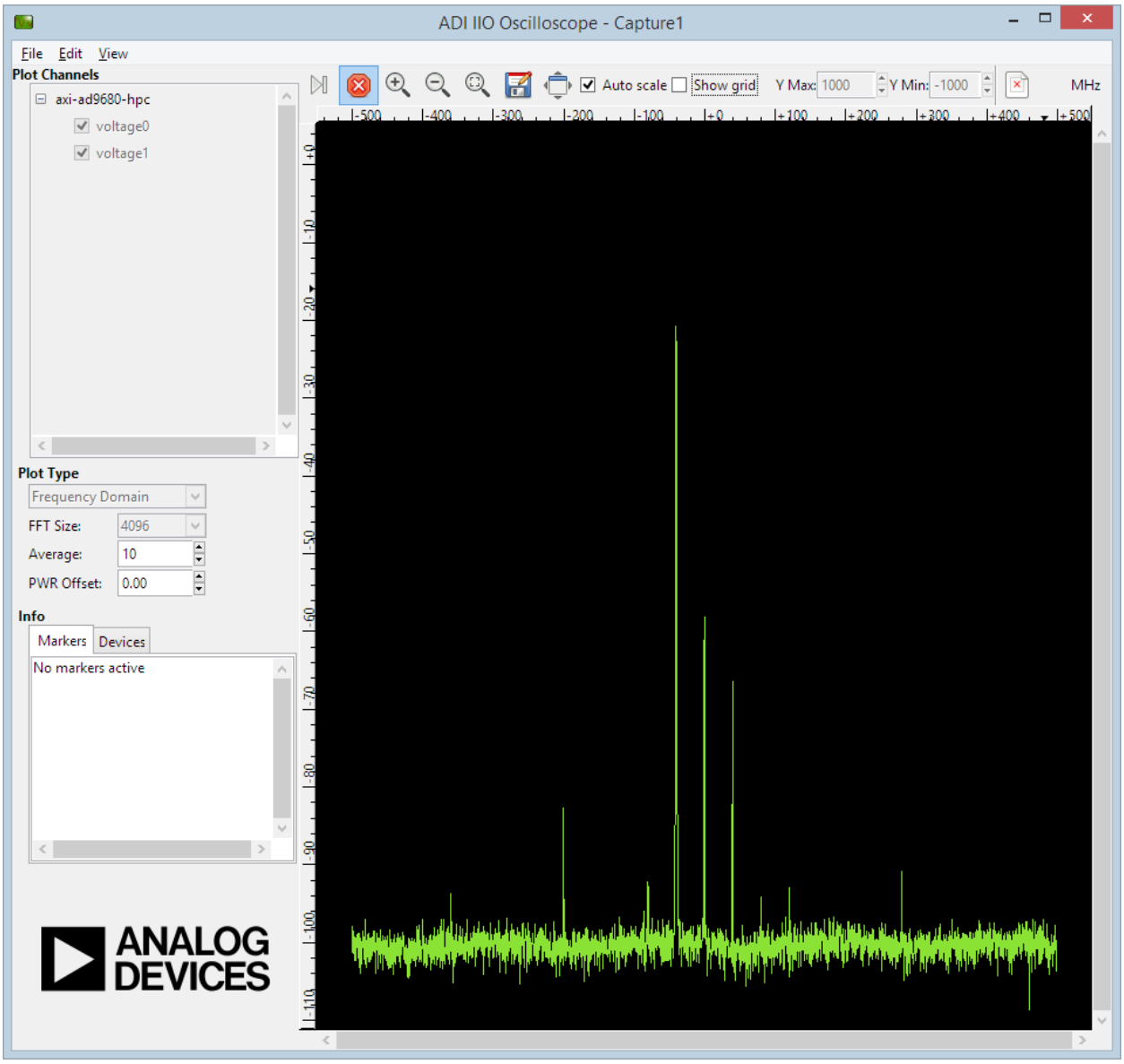
5. Set the **Average** to **10**

6. Uncheck the **Show Grid** selection box near the top of the window.

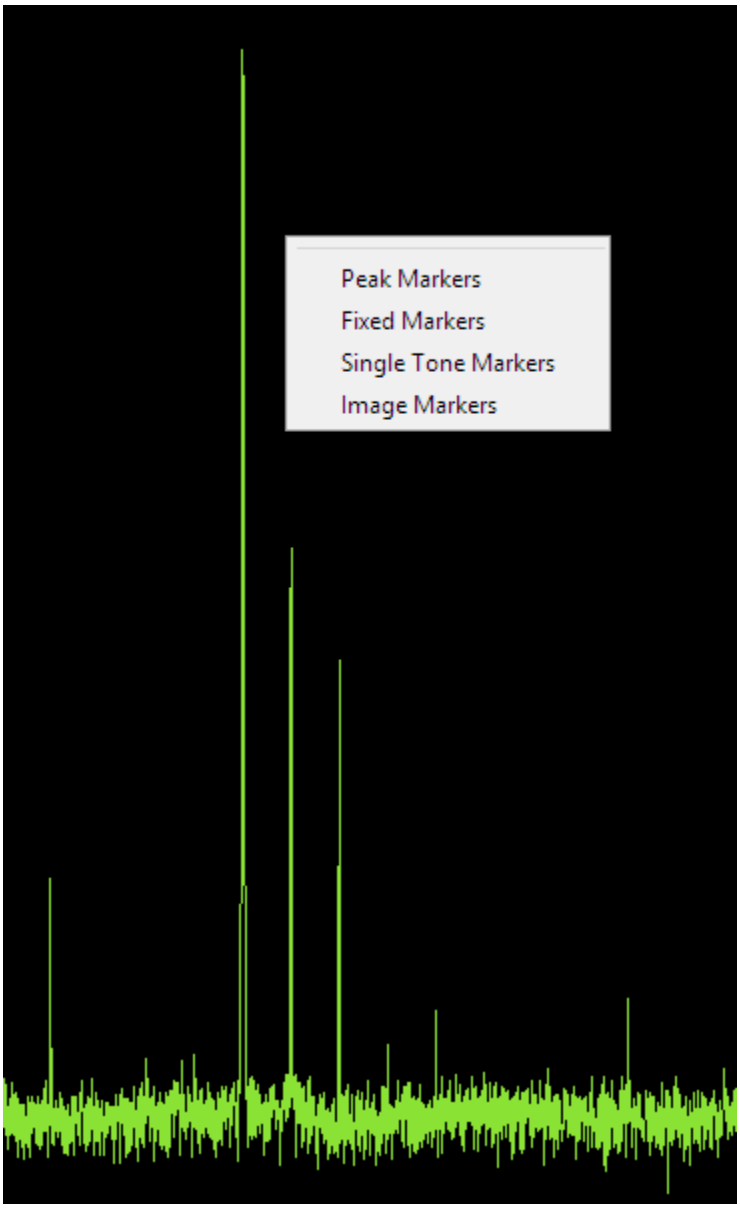
The ADI IIO Oscilloscope – Capture 1 window should now look like this:



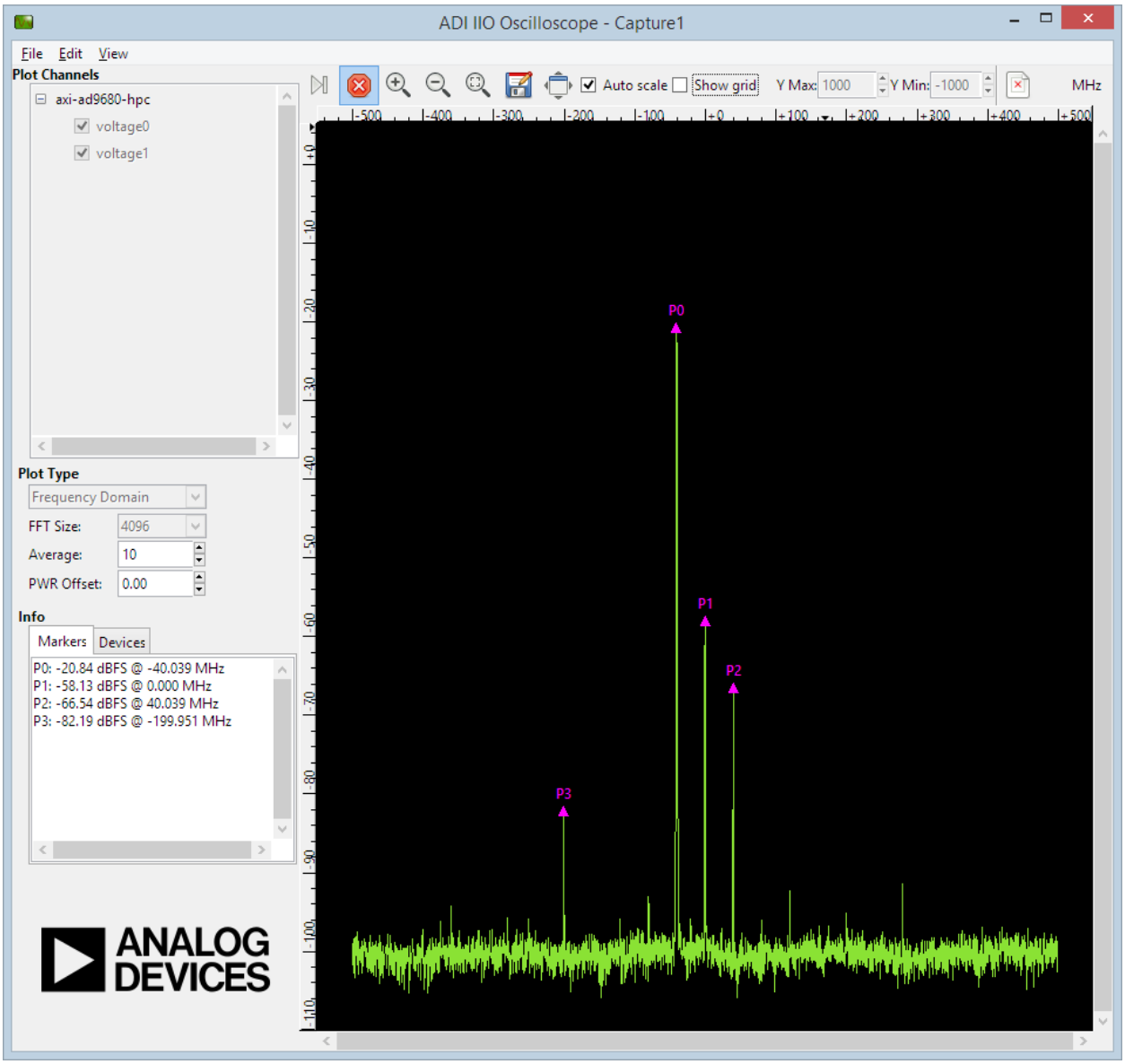
7. Click on the "**play**" button  near the top of the window to start the oscilloscope capture.



8. Set markers on the plot by right-clicking in the middle of the plot and selecting the marker of choice. (**Peak Markers** is a good choice…)

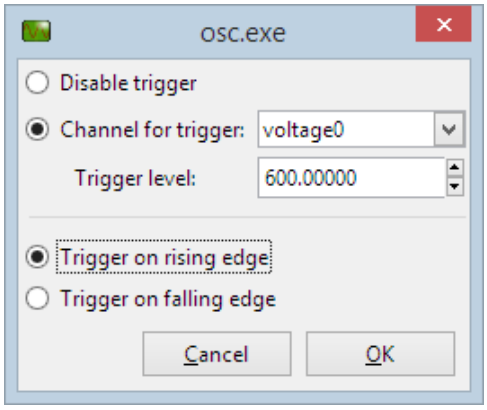


Once markers are set, they will persist on the plot and the details of each marker are displayed in the **Info** panel.

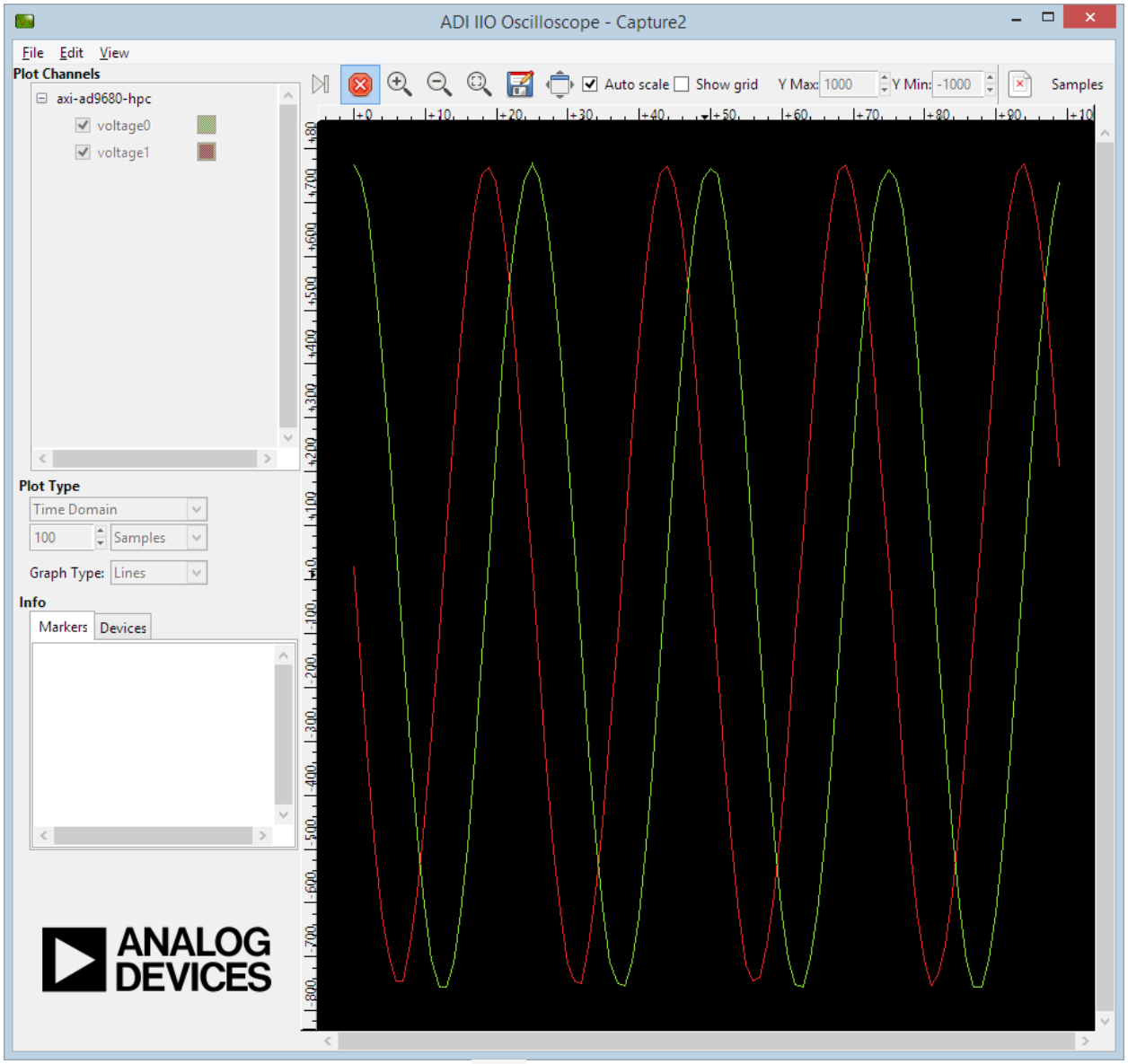


9. Add a second plot by clicking the  icon in the upper-right corner of the Capture 1 window. Set up the new **ADI IIO Oscilloscope – Capture 2** window to plot in the **Time Domain** with **100** Samples on both voltage channels.
10. Right-click on the **axi-ad9680-hpc** in the **Plot Channels** panel and select **Trigger settings**.

11. Select the radio button for **Channel for trigger: voltage0** and set the **Trigger level** to **600**. Click **OK**.



12. Click "**play**" to observe the new time domain plot.

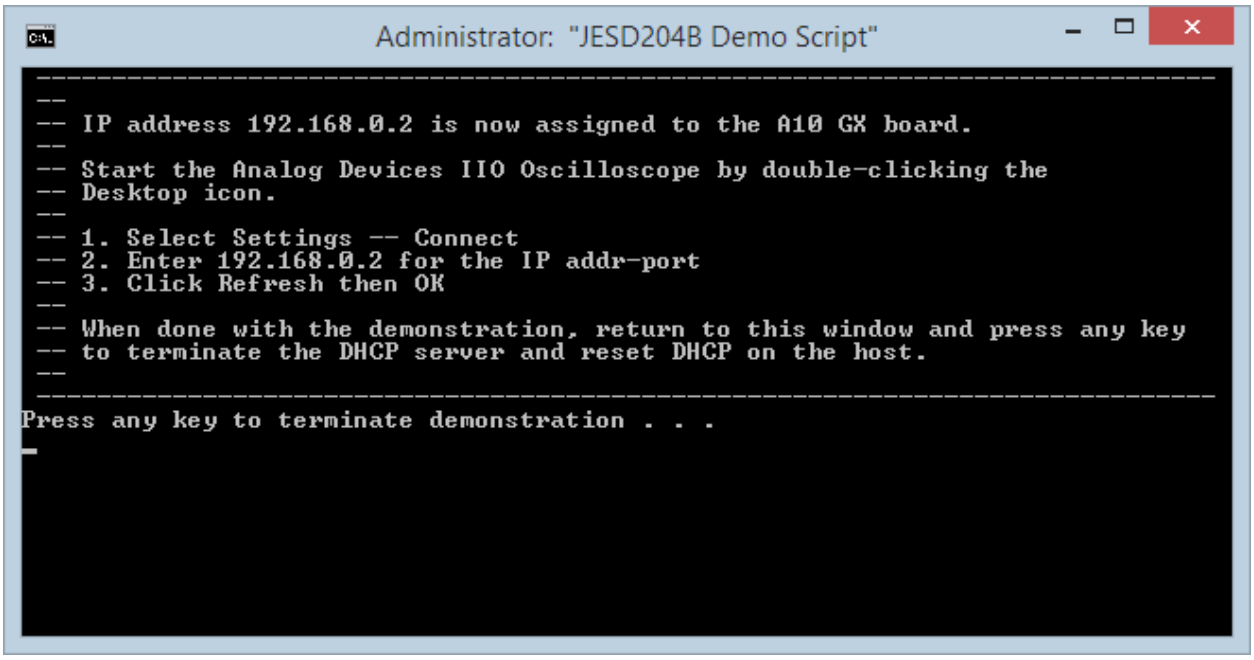


13. Stop the capture by clicking the "stop" icon  in each of the capture windows as desired**.** (A plot must be stopped in order to make changes to its capture settings.)
14. From here, play around with different settings in the ADI IIO Oscilloscope ADC/DAC control window and change the **DDS Single Tone: Tone 1 Frequency (MHz)** and observe the changes in the plots.
15. Change the **DDS Mode** to **TWO CW Tones** and observe 2 frequencies in the plots.

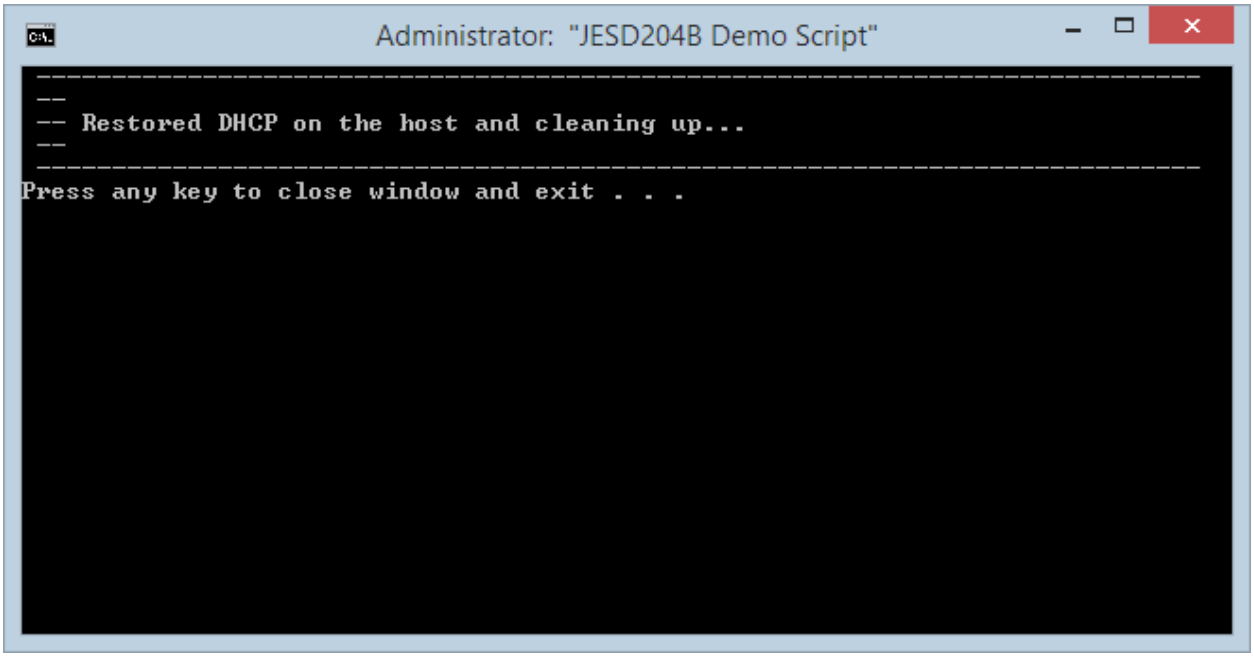
Feel free to poke around and play with any of the settings and plotting options. Note that due to the large amount of high speed data being received by the FPGA and plotted, sometimes the plots momentarily hang. They do return to functioning once you stop and restart the plot(s).

7.4 Shutdown

1. When done with the demo, **close** the **Capture** windows and **close** the **ADI IIO Oscilloscope** window.
2. **IMPORTANT** – To properly reset the host PC Ethernet network interface to DHCP, in the **JESD204B Demo Script** window running the DHCP server, **press any key** to properly terminate the script. This will force the DHCP server to stop and the batch file will restore the DHCP settings on the host.



3. **Press any key** to close the final window completing the demonstration script.



8. APPENDIX

8.1 More Information

Intel Arria 10 GX FPGA

https://www.altera.com/products/fpga/arria-series/arria-10/overview.html

Intel Arria 10 GX FPGA Development Kit

https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-a10-gx-fpga.html

Analog Devices AD9144 Quad 16-bit 2.8GSPS DAC

http://www.analog.com/en/products/digital-to-analog-converters/da-converters/AD9144.html

Analog Devices 9680 Dual 14-bit 1.25GSPS ADC

http://www.analog.com/en/products/analog-to-digital-converters/high-speed-ad-10msps/ad9680.html

Analog Devices AD-FMCDAQ2-EBZ Evaluation Board

http://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad-fmcdaq2-ebz.html