Arrow High Speed

Data Acquisition Kit

User Guide

Featuring the
Analog Devices DAQ2 Evaluation Board
and
Intel Arria 10 GX Development Kit

Version 4.0 **11/09/2017**

Table of Contents

1. Introduction

The Arrow High-Speed Data Acquisition Kit is a complete development platform for creating solutions with the space-saving high-speed GSPS JESD204B serial interface.

Featuring Analog Devices' GSPS data converters and Intel's Arria 10 FPGA, the kit allows them to communicate across 4 serial lanes in each direction at speeds up to 40GSPS. Also provided are all the timing and power components required to both develop solutions and demonstrate the capabilities of JESD204B. With sampling speeds of up to 1GSPS, this is the ideal platform for applications requiring the capture and transportation of large amounts of data.

A one-year license for all IP and tools is included so that the user can begin development immediately.

The built-in demo mode allows for a rapid out of box (OOB) demonstration without the need for installing the Intel Quartus toolset.

1.1 Theory of Operation

The kit is configured to allow the user to send data from the Intel Arria 10 GX FPGA to the Analog Devices AD9144 DAC using the JESD204B serial interface and FMC (FPGA Mezzanine Card) connectors. It is setup to send data from the Analog Devices AD9680 ADC back to the Arria 10 by the same method. By attaching two RF cables, the analog outputs from the AD9144 can be looped back to the inputs of the AD9680 forming a complete closed system. Using Analog Devices' IIO Oscilloscope application on a host PC, the user can set the inputs generated by the Arria 10 and view the outputs on the return path.

The FPGA provides many capabilities in this kit. The primary means of configuring the DAC outputs and receiving the ADC inputs happens via dedicated IP blocks in the FPGA fabric. This also provides the gigabit transceivers necessary to communicate to the JESD204B capable DAC and ADC.

A wired Ethernet connection between the FPGA and the host PC is used to transfer the data to and from the host IIO Oscilloscope application and the Linux OS running on the NIOS processor in the FPGA.

The data sent out from the FPGA to the DAC is supplied from one of two sources: the FPGA can either create a digital sine wave internally via its Direct Digital Synthesizer block (DDS), or read in an externally supplied data file. From here the digital data is packaged and sent to the JESD204B IP block inside the FPGA, where it is configured per the JESD204B standard. The serialized data is then transmitted to the DAC over an FPGA Mezzanine Card (FMC) connection on four 10Gbps channels. Once the data has been received and decoded by the JESD204B DAC, the analog signals are sent to a pair of RF SMA connectors; this is defined as the transmit path.

For a closed loop system the signals from the DAC's SMA connectors are transmitted over RF cables to SMA connectors connected to the inputs of the ADC. The ADC takes the analog signals and converts to the serialized digital JESD204B format, then sends this to the FPGA over the FMC connection on four additional 10Gbps channels; the receive path.

Once the data is captured in the FPGA it is sent over the gigabit Ethernet connection to the host PC running the IIO Oscilloscope application, where the results can be viewed in the time and frequency domains or as a constellation plot.

2. Data Flow/Signal Path

Here is a brief description of the signal as it flows from the FPGA across the JESD204B interface to the data converters and back. Refer to Figure 1.

2.1 Transmit Path

1. Using the IIO Oscilloscope application running on a host PC, along with a gigabit Ethernet cable connected from the PC to the Arria 10 FPGA, either a digital sine wave in the 0-500MHz range is generated from the FPGA's internal DDS frequency synthesizer blocks, or a data file with a digital signal representation is selected.
2. Inside the Arria 10 the digital signal is converted into the JESD204B format using Analog Devices' IP. It is then sent out across 4 lanes to an FMC connector on the Arria 10 development kit at a rate of 40Gbps (4 lanes @ 10Gbps each).
3. The data flows through the corresponding FMC connector on the AD-FMCDAQ2-EBZ board and into the AD9144 multichannel high-speed DAC where it is converted from the JESD204B standard to the proper digital format prior to being converted to analog. The AD9144 DAC generates both I and Q signals used for quadrature amplitude modulation (QAM) of the RF signal, converts it to analog and sends each signal out via SMA RF connectors connected to RG316 RF coaxial cables.

2.2 Receive Path

4. The analog RF signals flow through the two coaxial cables and back into the AD-FMCDAQ2-EBZ board through two additional SMA RF connectors routed to the AD9680 2-channel ADC. The signal is sampled and digitized and converted back into the JESD204B standard.
5. The data is sent back along 4 lanes also at a rate of 10Gbps per lane (40Gbps total) across the FMC connector to the Arria 10 GX kit where it is decoded by Arria 10 FPGA IP blocks.
6. The received data is sent to the host PC over the gigabit Ethernet connection. Using the ADI IIO Oscilloscope graphical user interface application on the host, the received data can be viewed in the time domain, frequency domain or as a polar plot.

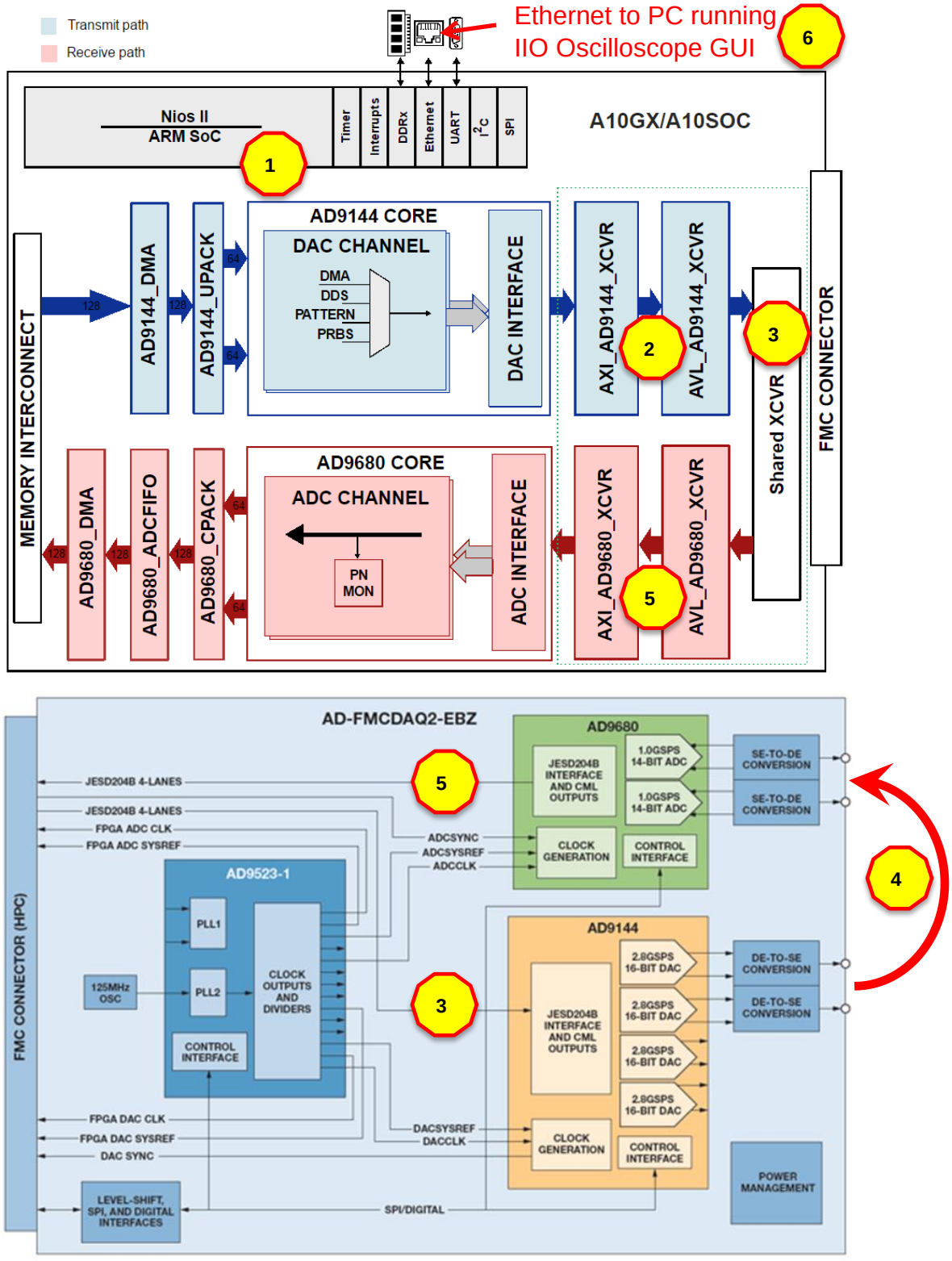


Figure 1: JESD204B Demonstration Platform Block Diagram

3. Kit Contents

The Arrow High-Speed Data Acquisition Kit comes with the following components:

- Intel Arria 10 GX Development Kit p/n DK-DEV-10AX115S-A including power supply
- Analog Devices AD-FMCDAQ2-EBZ 'DAQ2' Evaluation Board
- (2) RG316 SMA RF cables
- (1) 5' CAT-6A 1000BASE-T GigE Ethernet cable

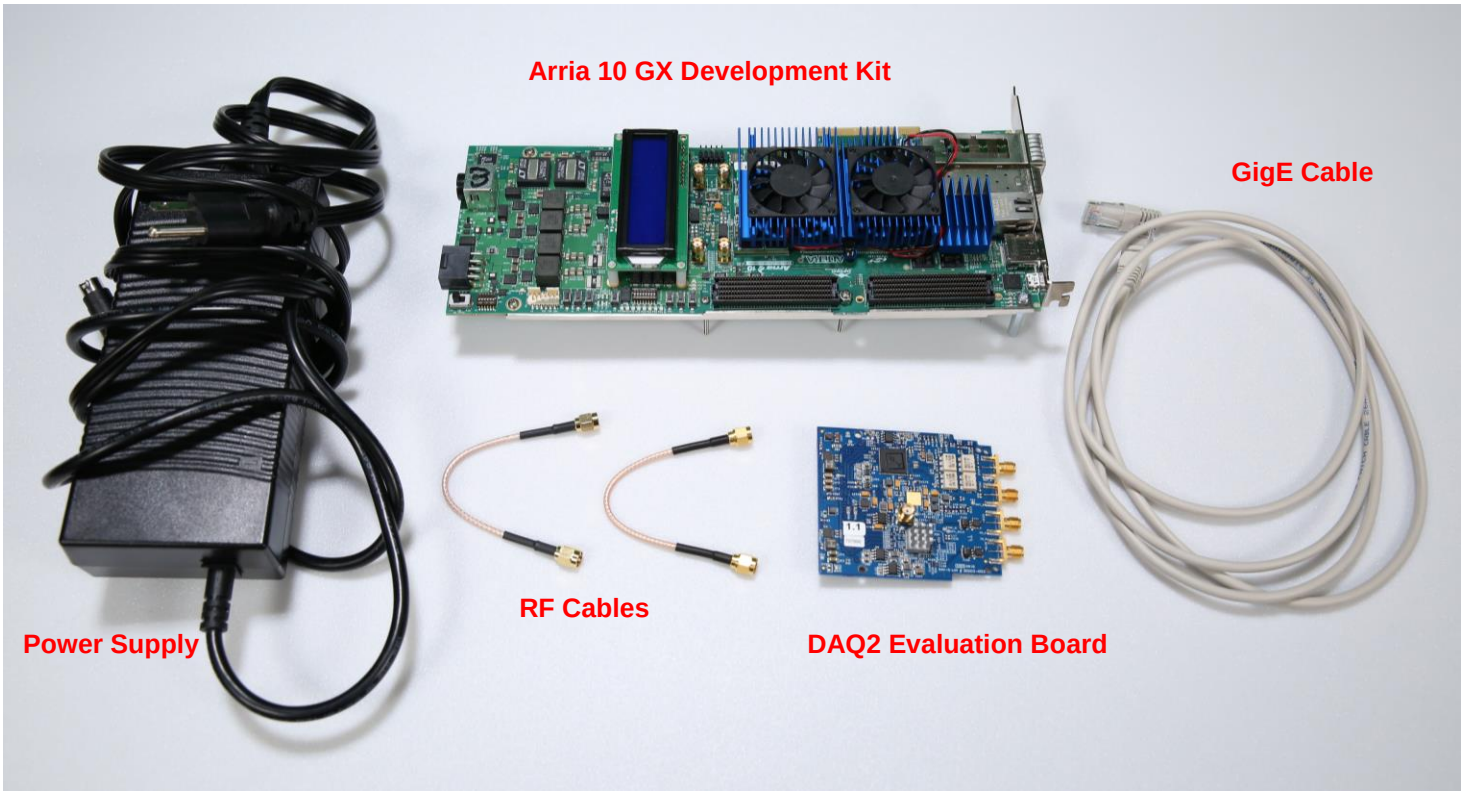


Figure 2: Arrow High-Speed Data Acquisition Kit Contents

3.1 Intel Arria 10 GX Development Kit

Figure 3: Arria 10 GX FPGA Development Kit (Power Supply not shown)

- https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-a10-gx-fpga.html

User guide: https://www.altera.com/content/dam/altera-www/global/en_US/support/boards-kits/arria10/FPGA/A10-FPGA-ES3-DK-UG_1.pdf

The Arria 10 GX FPGA Development Kit includes the following hardware.

- Arria 10 GX 10AX115S2F45I1SG2 FPGA
- 1 GB DDR4 SDRAM, 2GB DDR3 SDRAM, or RLDRAM3 (16 Meg x 36) (daughter cards)
- Two FMC loopback interfaces supporting gigabit transceivers, LVDS and single-ended I/Os
- One quad small-form-factor pluggable (QSFP) and one SFP+ port
- PCIe x8 edge connector
- Serial digital interface (SDI) channel
- Character LCD
- AC adapter power cables
- Ethernet and USB cables

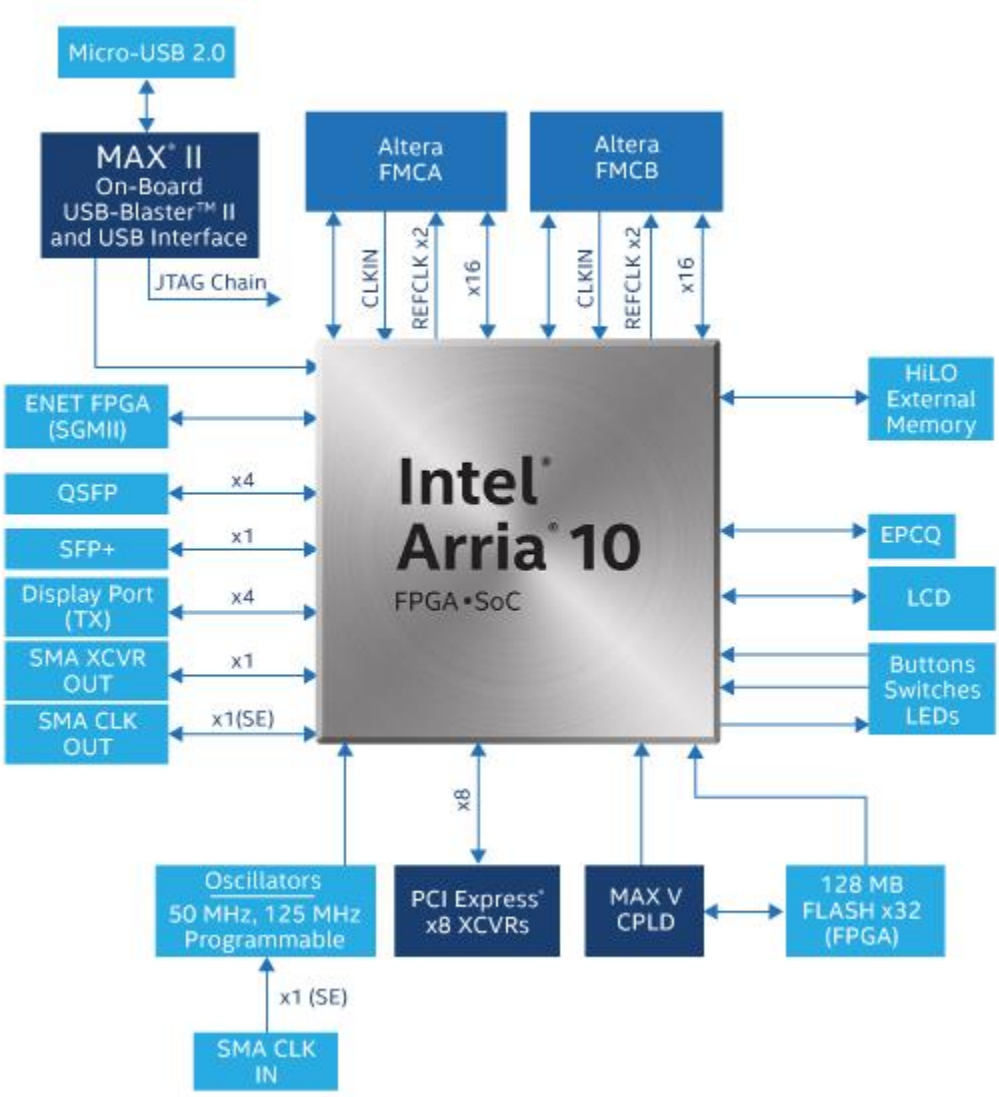


Figure 4: Arria 10 GX Development Board Block Diagram

3.2 Analog Devices DAQ2 Evaluation Board

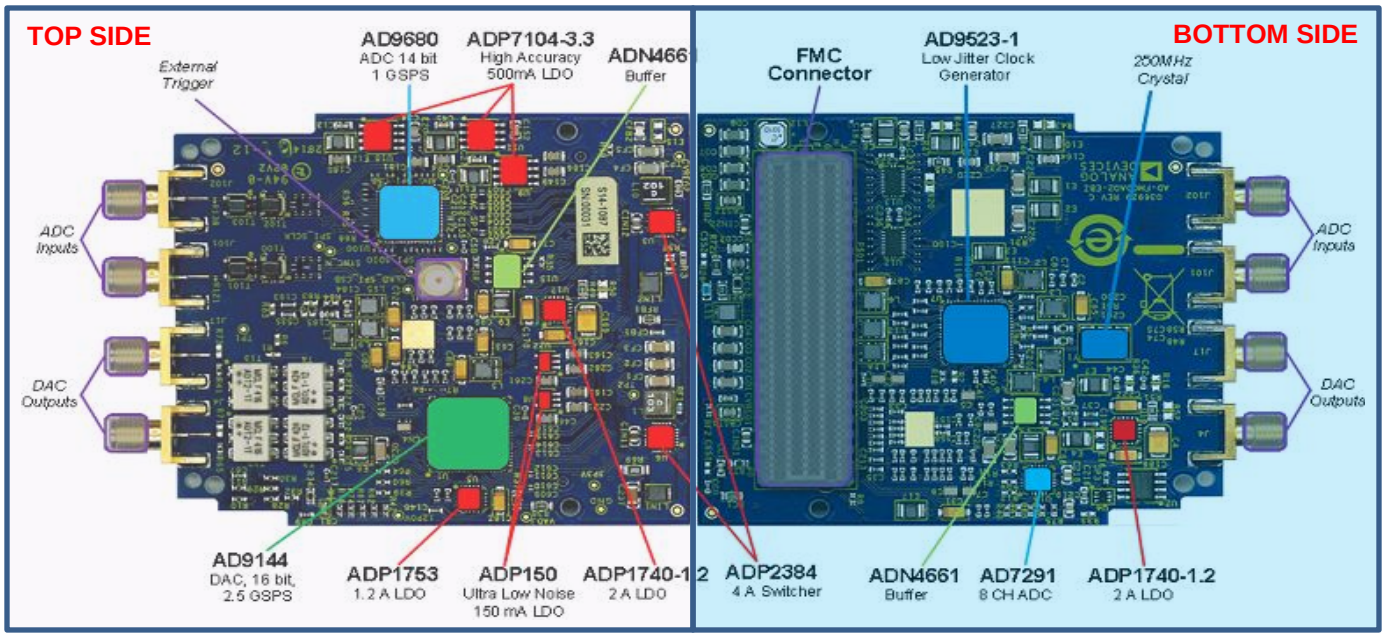


Figure 5: Analog Devices AD-FMCDAQ2-EBZ Evaluation Board Top (Left) and Bottom (Right)

- http://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad-fmcdaq2-ebz.html

The AD-FMCDAQ2-EBZ Evaluation Board contains the following.

- AD9680 2-channel 14-Bit 1.0GSPS JESD204B ADC
- AD9144 4-Channel 16-Bit 2.8GSPS JESD204B DAC
- AD9523-1 14-Output 1GHz Clock Generator
- FPGA Mezzanine Card (FMC) High-Speed Connector

Also:

- AD7291 8-Channel 12-Bit ADC
- Miscellaneous Power and Timing components

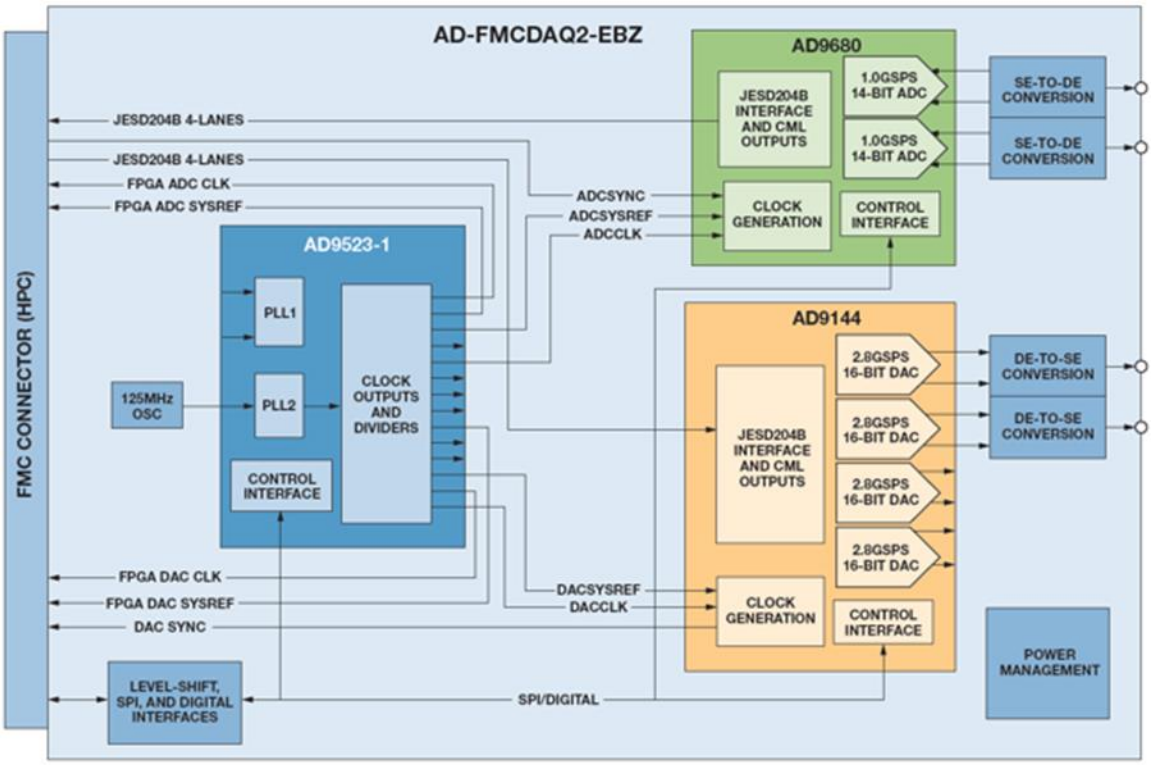


Figure 6: AD-FMCDAQ2-EBZ Evaluation Board Block Diagram

4. Downloading the Github Content

All necessary software applications and files listed below are provided in the arrow-socfpga github site. There is no need to install the Intel Quartus Prime Design Software to run the built-in demo.

- Files necessary for the demonstration can be found on the **Arrow** github pages. Follow the instructions listed below to download this content

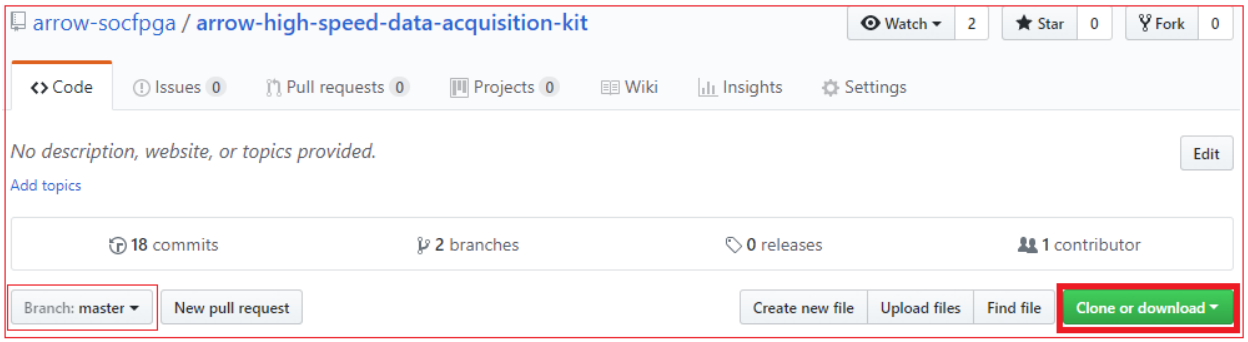


Figure 7- Github site for Arrow High-Speed Development Kit

1. Open a browser to https://github.com/arrow-socfpga/arrow-high-speed-data-acquisition-kit
2. Select the **2017_r1 branch.**
3. Download the repository as a zip file. Extract the zip file to a directory.
4. cd to the **arrow-high-speed-data-acquisition-kit/arria10gx_intel_PSG** sub-directory.

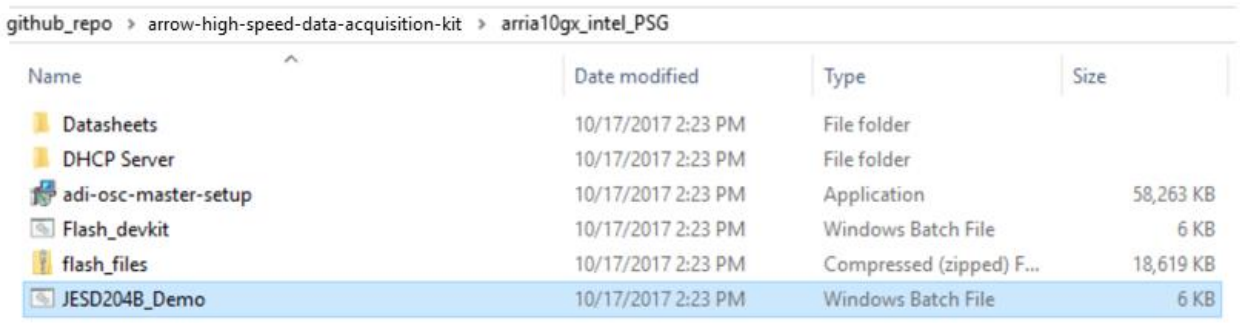


Figure 8- Software and Firmware for Kit

4.1 Applications

- Analog Devices IIO Oscilloscope – **OSC.exe**
    - The ADI IIO Oscilloscope is an example application, which demonstrates how to interface different evaluation boards from within a Linux system. The application supports plotting of the captured data in four different modes (time domain, frequency domain, constellation and cross-correlation). The application also allows a user to view and modify several settings of the evaluation board's devices.
    - The IIO Oscilloscope application installer is provided in the downloaded content.
    - Optional web link: https://github.com/analogdevicesinc/iio-oscilloscope/releases/download/v0.5-master/adi-osc-master-setup.exe
- DHCP Server – **OpenDHCPServer.exe**
    - A simple DHCP server is required so that the network interface of the Arria 10 FPGA is assigned an IP address within the same subnet as the host PC.
    - The DHCP server application is provided in the downloaded content.
    - Optional web link: https://sourceforge.net/projects/dhcpserver/

4.2 Files

- Arria 10 Development kit firmware flash batch file – **Flash_devkit.bat**
    - The **Flash_devkit.bat** batch file temporarily assigns a static IP address to the host PC. It also dynamically assigns an IP address to the Arria 10 development kit. This will be used in Section 6 to flash the demo firmware into the kit.
- Firmware flash files – **flash_files.zip**
    - Contains the FPGA hardware image flash file
    - Contains the Nios II processor Linux flash file.
- Arria 10 JESD204B Demonstration batch file – **JESD204B_Demo.bat**
    - The JESD204B_Demo.bat batch file temporarily assigns a static IP address to the host PC. It also dynamically assigns an IP address to the Arria 10 development kit.
- DHCP Server configuration settings – **OpenDHCPServer.ini**
    - Required by the OpenDHCPServer application.
    - The configuration settings file is provided in the JESD204B_Demo.zip file.

5. Hardware Configuration

The instructions in this section will guide you through the hardware setup of the JESD204B demonstration platform using the Arria 10 GX FPGA Development Kit and the Analog Devices DAQ2 JESD204B Evaluation Board.

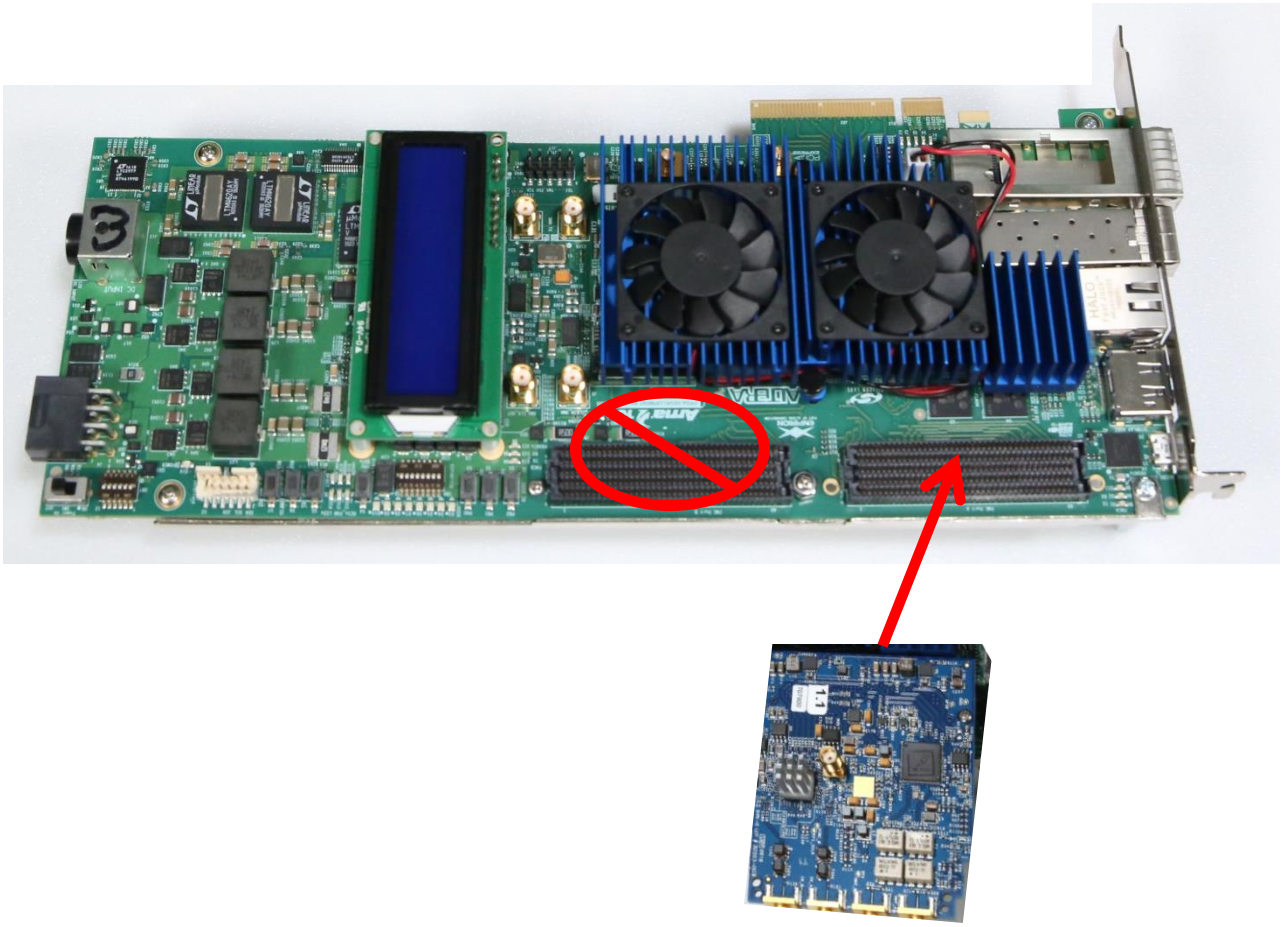


Figure 9: Connect AD-FMCDAQ2-EBZ board to FMC 'A' connector on Arria 10 GX board

On the AD-FMCDAQ2-EBZ hook up the two provided RG316 RF cables as shown

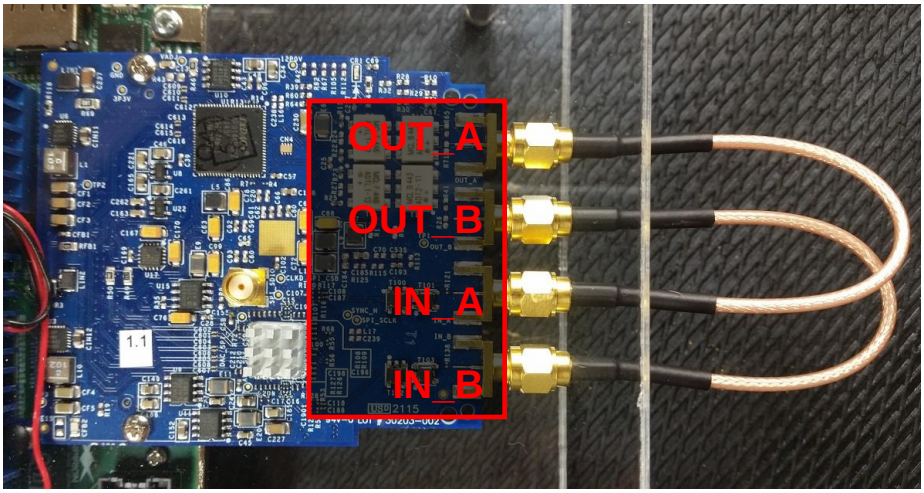


Figure 10: RF cable connections

2. Using the Cat-5e gigabit Ethernet cable connect the Arria 10 GX kit directly to the host PC via the RJ45 Ethernet port on each. Important: the use of a gigabit capable Ethernet patch cable is required due to the high data rates of the JESD204B interface.

3. Plug the included power supply into the Arria 10 GX board's 4-pin connector and into a 110V outlet.

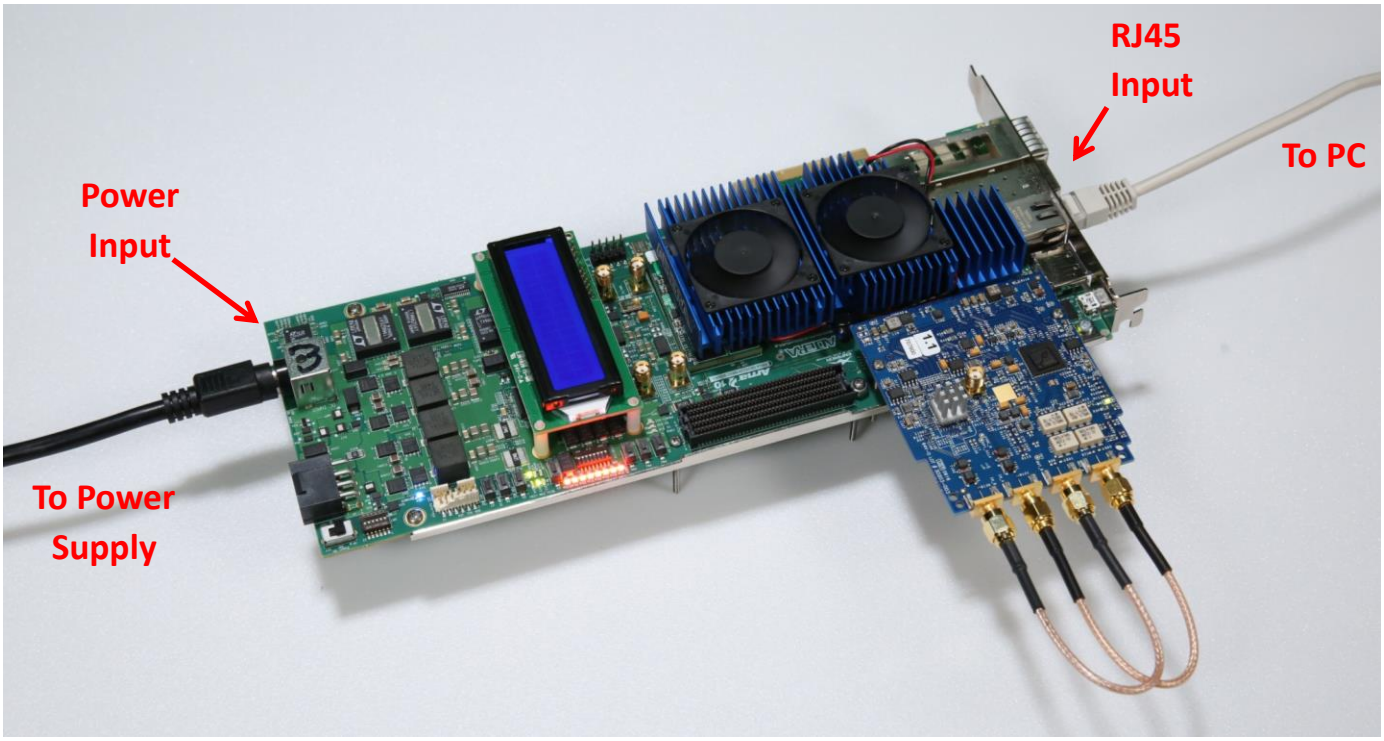


Figure 11: Power and Ethernet connections on Arria 10 GX Development Kit

4. Here is the complete setup

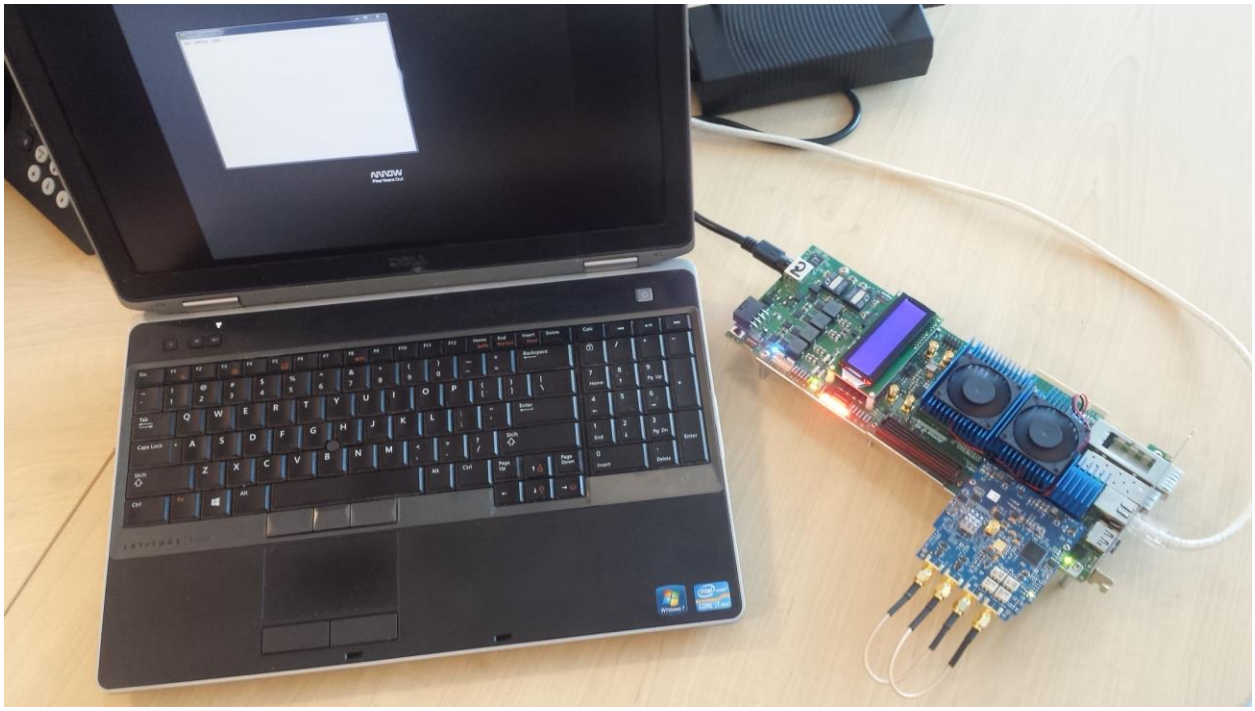


Figure 12: Complete Demo Setup

6. Software Installation

The instructions in this section will guide you through the software installation of the JESD204B demonstration.

Open the folder previously downloaded in section 4.1

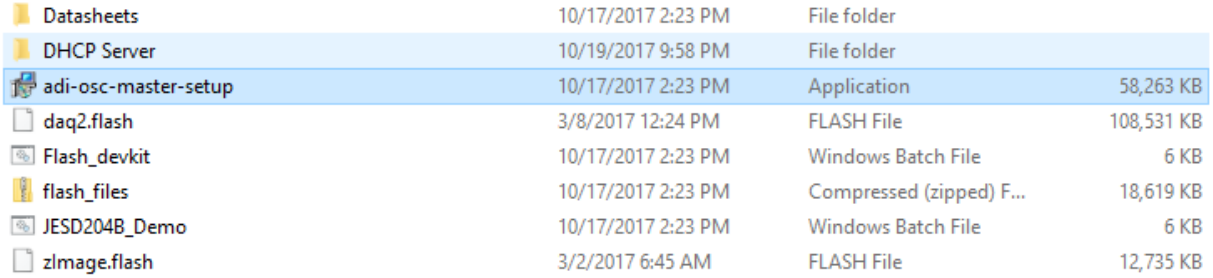
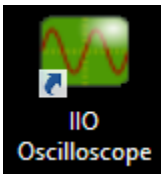


Figure 13: Extracted JESD204B Archive

1. Install the Analog Devices IIO Oscilloscope application by double-clicking the **adi-osc-master-setup.exe** installer. Accept **ALL** the defaults and accept the License Agreement. Also check the box labeled 'Create a desktop icon'.

After installing the IIO Oscilloscope there will be a new **IIO Oscilloscope** Desktop icon.

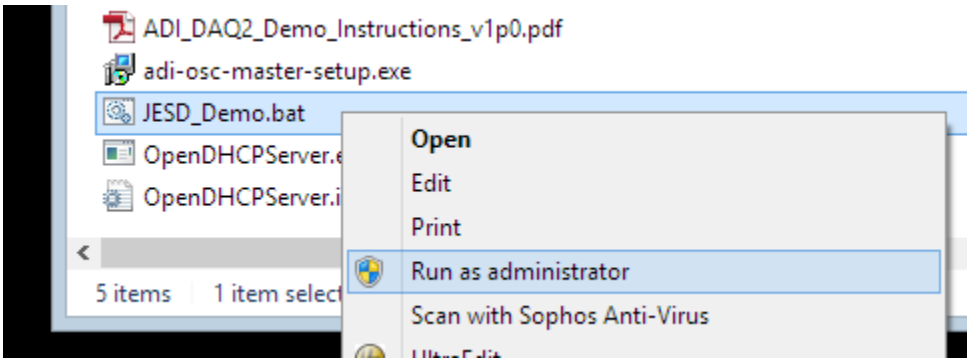


7. Running the Demonstration

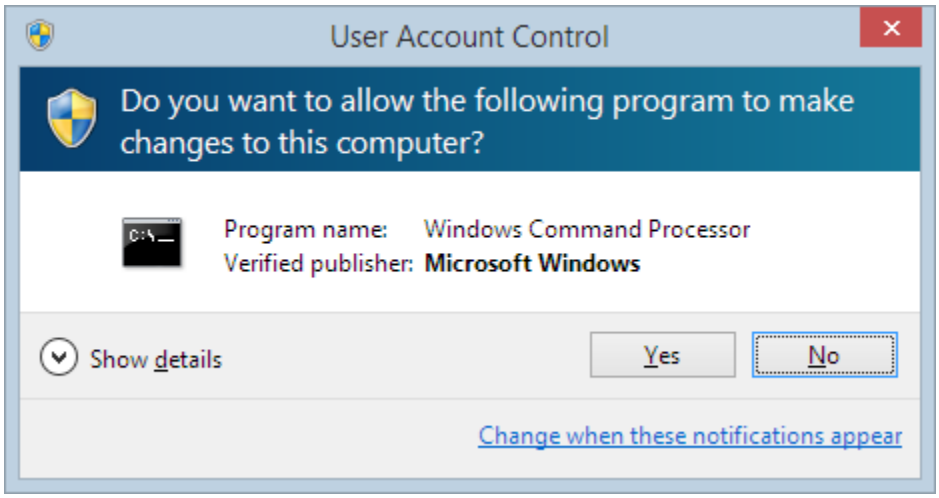
As mentioned previously the kit comes with a built-in demonstration of the JESD204B interface. This section describes how to run this including powering up the hardware and making a connection to the system with the IIO Oscilloscope application. An initial configuration of the transmitters is described and details on creating plots of the received data are covered.

7.1 Start the DHCP Server

1. Launch the **JESD204B_Demo.bat** batch file as **administrator** by right-clicking the file and selecting **Run as administrator**.

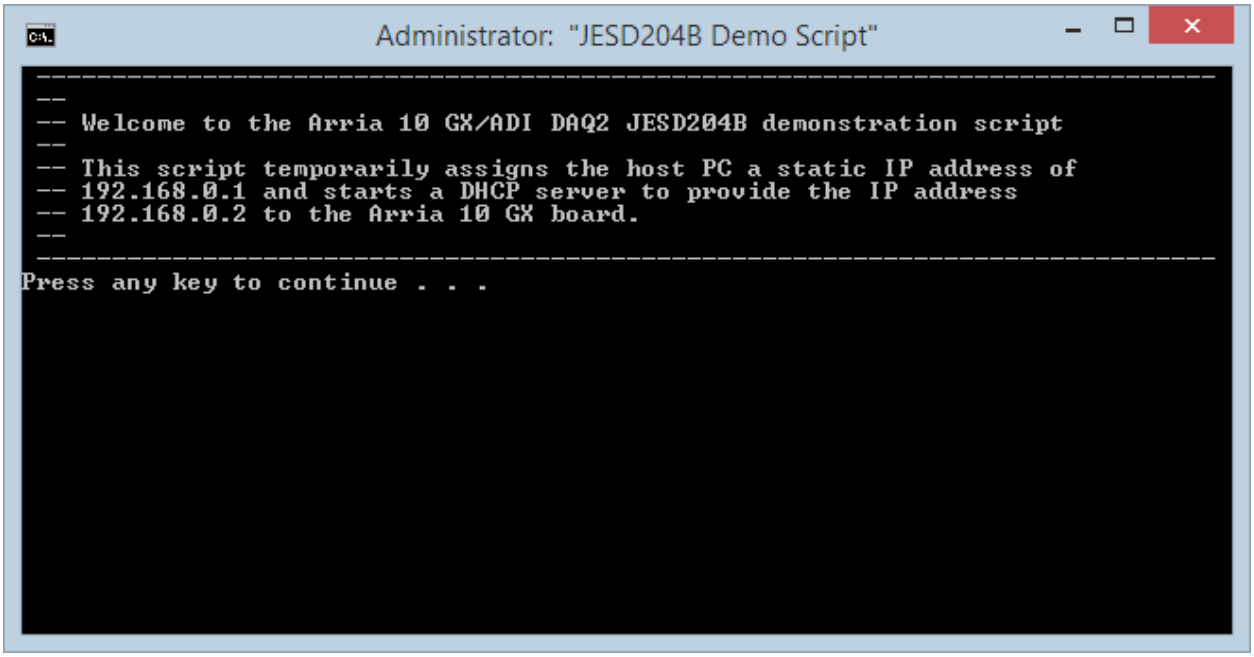


2. Select **Yes** on the **User Account Control** dialog allowing the script to execute.

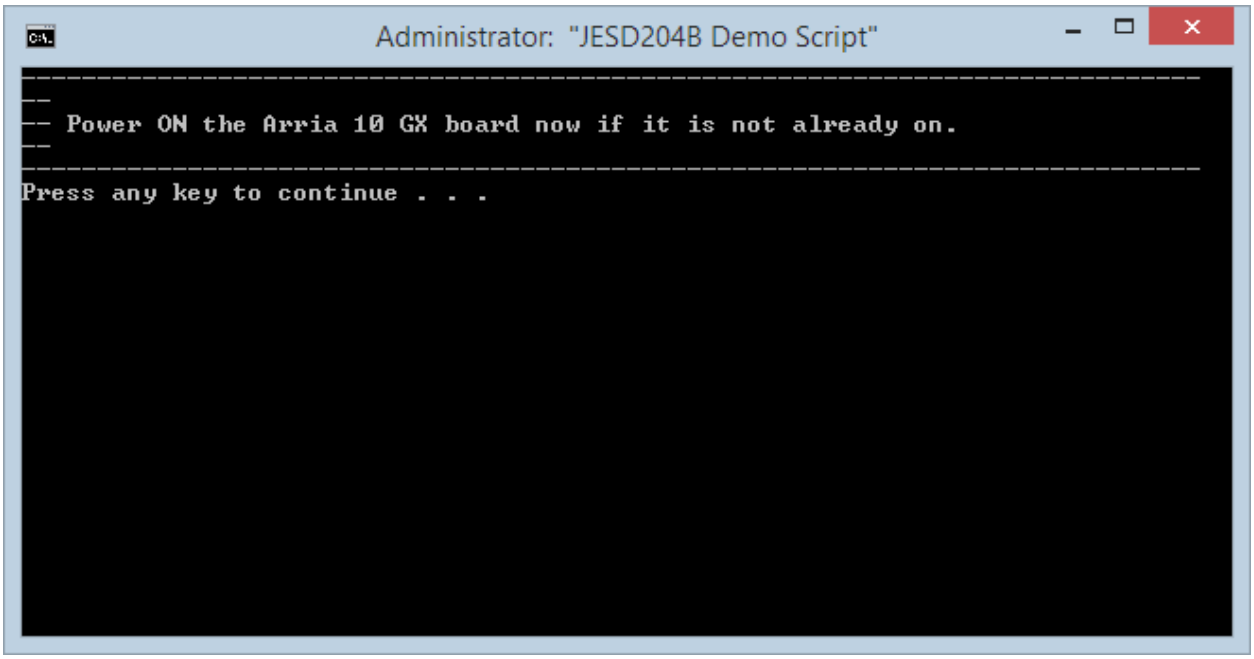


The "**JESD204B Demo Script**" window will open providing information about the script.

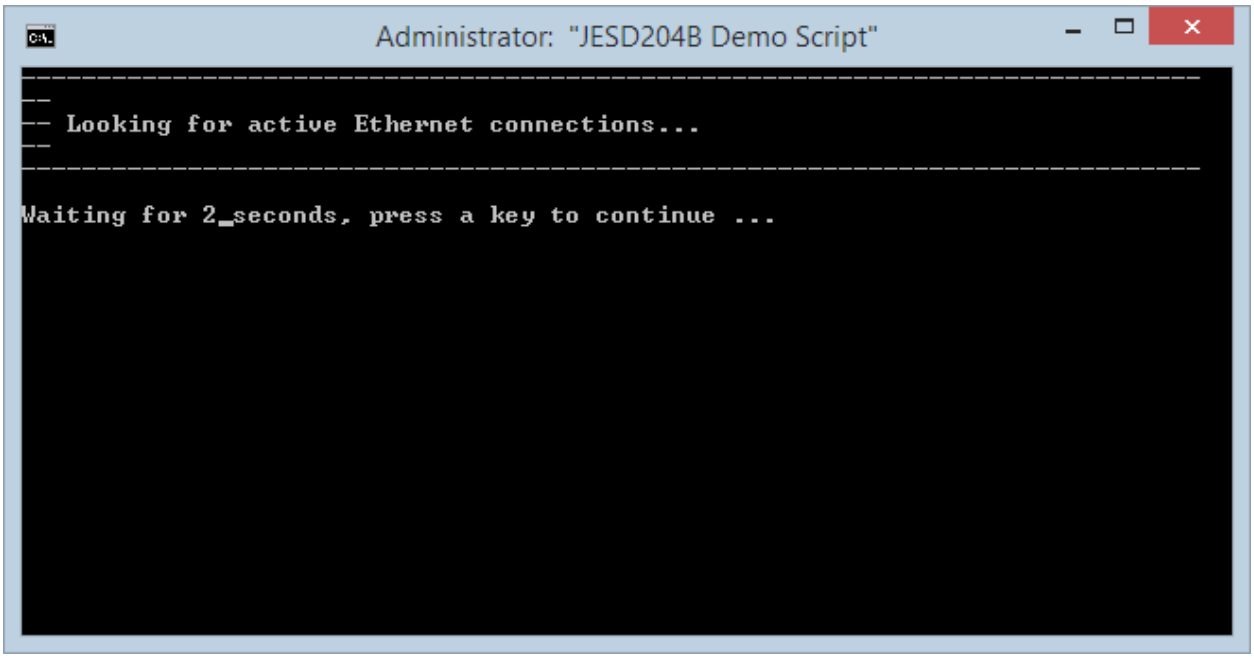
3. **Press any key** on the PC keyboard to continue.



4. Move the power switch, **SW1,** on the Arria 10 GX kit to the **ON** position and **press any key** on the keyboard. Upon power-up, the FPGA will be programmed from the preconfigured CFI flash on the Arria 10 GX kit. The 8 red LEDs will be illuminated upon successful FPGA configuration.

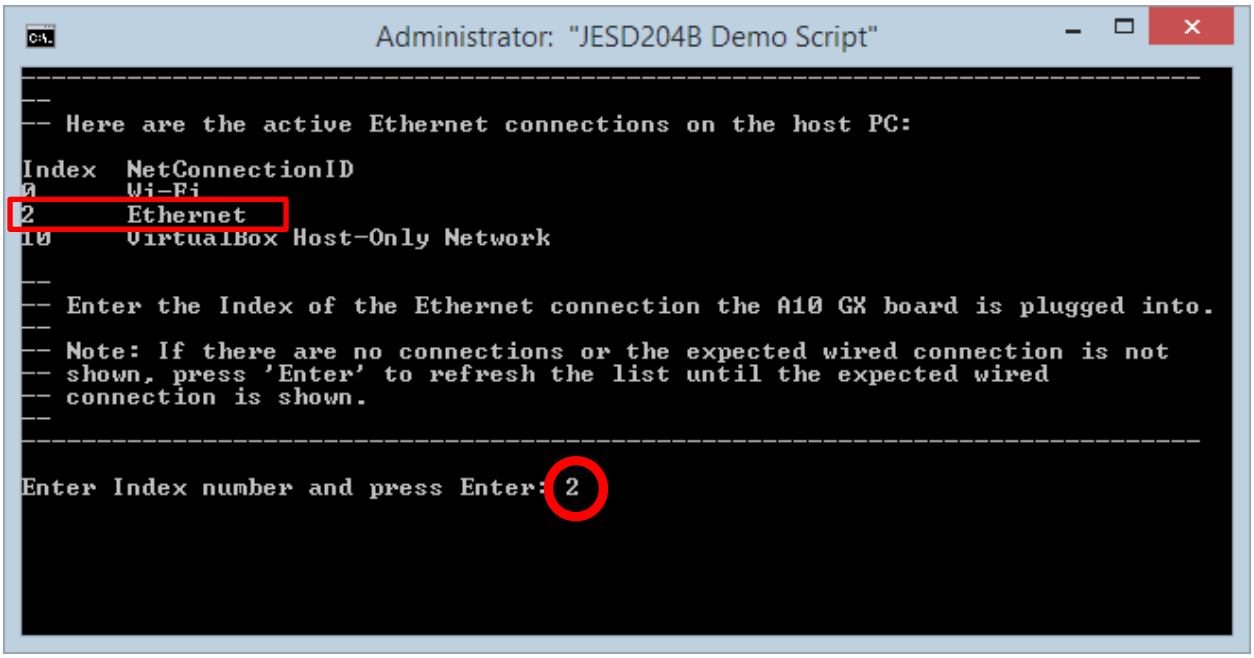


The script will query the PC Ethernet connections for 5 seconds and automatically report back the active interfaces.

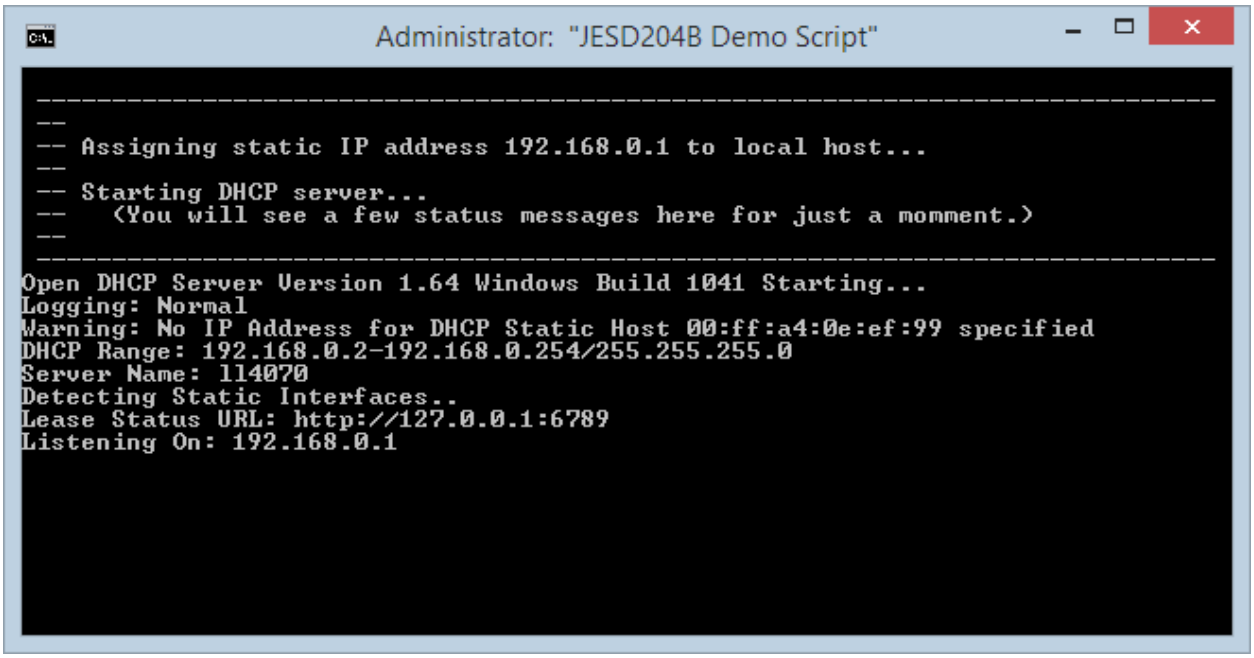


Note: The name of the connections may vary. ('Local Area Connection' or 'Ethernet' are common.)

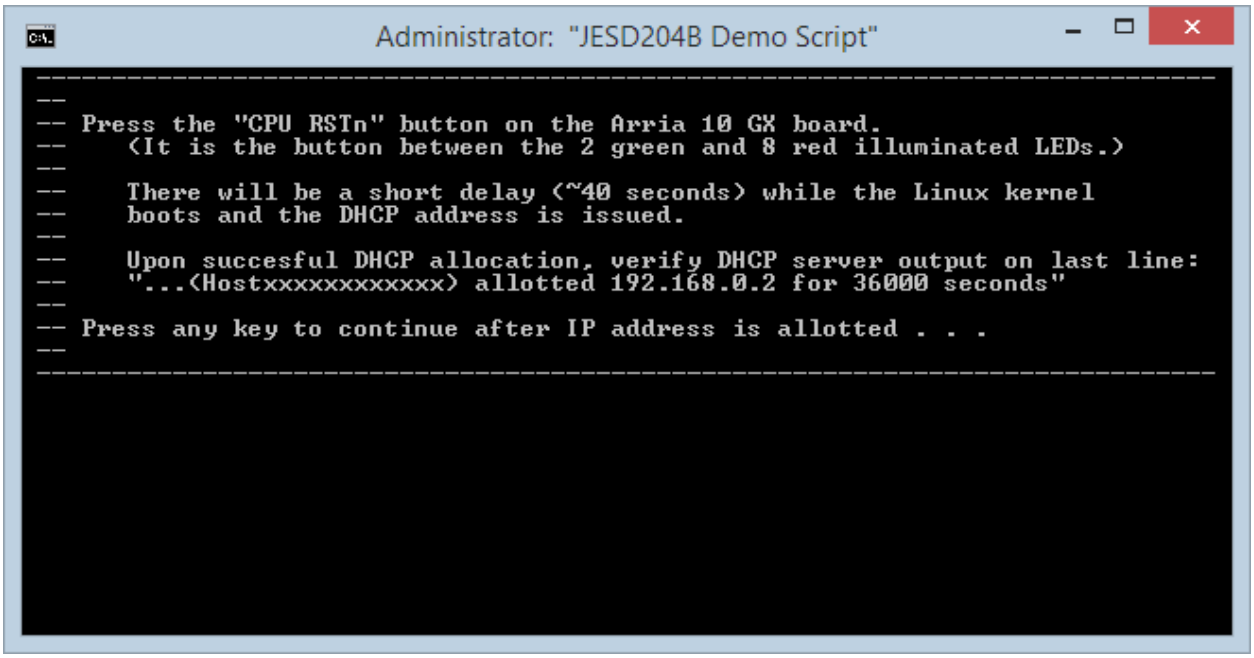
5. Enter the **Index** number of the Ethernet connection which the A10 GX board is plugged into and press **Enter**. (Index = 2 for "Ethernet" in the below example.)



Status messages will appear with information concerning assigning the static IP address to the host and starting the DHCP server. These messages will only appear for a few seconds and then disappear.

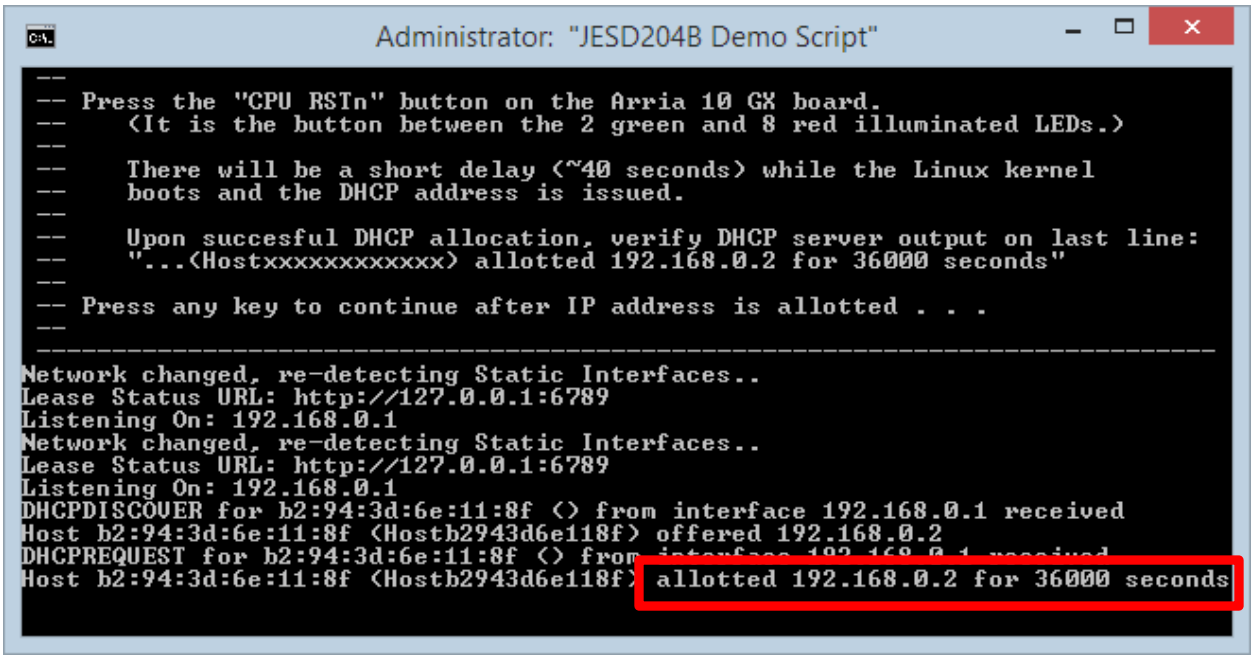


6. Press the **"CPU RSTn"** button on the Arria 10 GX board forcing the NIOS processor into reset and reloading of the Linux kernel. The button is located between the 2 green and 8 red illuminated LEDS.



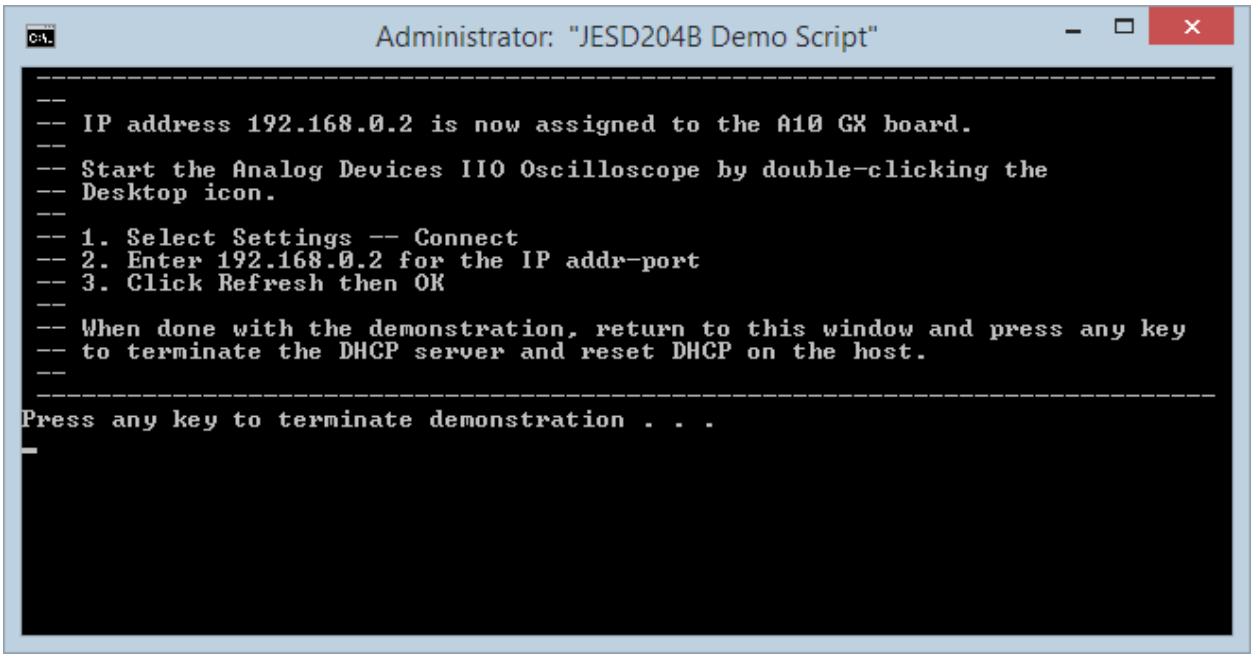
Additional DHCP server status messages will appear with information concerning assigning the static IP address to the Arria 10 GX. Upon successful DHCP allocation, verify the static IP address 192.168.0.2 was assigned to the Arria 10 GX.

7. **Press any key** once the status message "**Host xx:xx:xx:xx:xx:xx (Hostxxxxxxxxxxxx) allotted 192.168.0.2 for 3600 seconds**" appears. (Note: The "xx" values will vary depending on the host PC MAC address.)



The script output now provides additional information about running the demonstration.

Note: **DO NOT** press any additional keys while in this window or close this window until the demonstration is completed as it will terminate the DHCP server and sever the connection between the PC and the Arria 10 GX FPGA. See section 7.4.



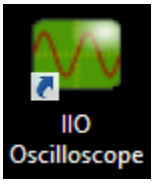
7.2 Connect the IIO Oscilloscope

There are two components to IIO Oscilloscope application that is run on the host PC: configuration and plotting.

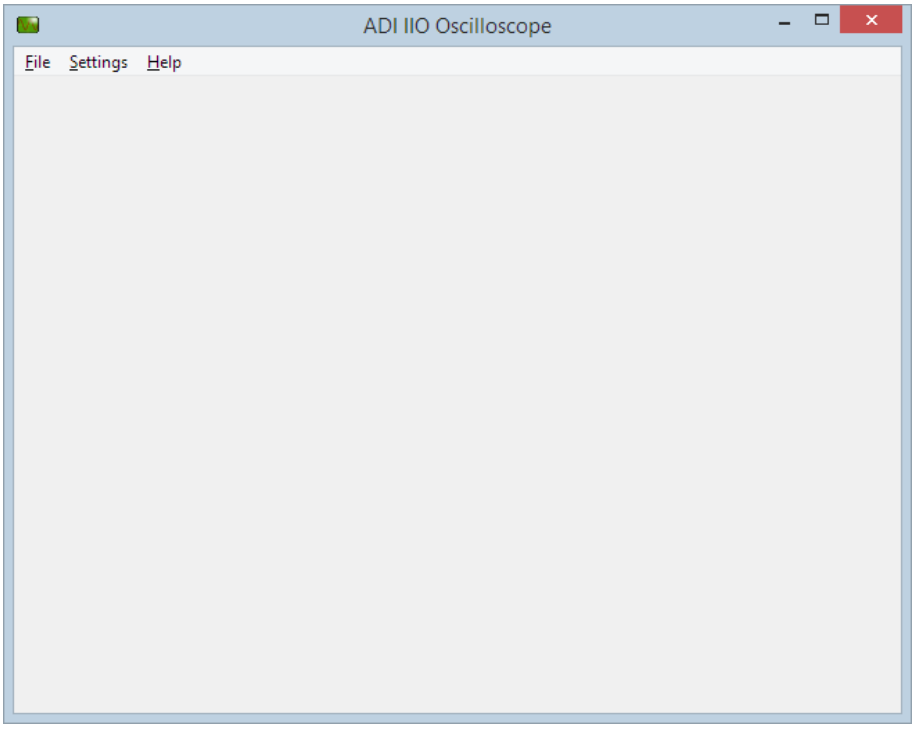
The configuration dialogs provide for choosing the digital signal data that is to be sent to the AD9144 DAC as well as putting the AD9380 ADC into test modes. The AD9144 data is either "tones" that are the output generated by the Arria 10 DDS frequency synthesizer blocks or data files containing digital representations of a signal.

The plotting component of the IIO Oscilloscope application allows the user to view the data received by the Arria 10 after the signal has made a complete loop from the FPGA, through the JESD204B interface to the DAC, through the RF cable back into the ADC, again through a JESD204B interface and back into the FPGA. The plots can display data in the time or frequency domain as well as constellation and cross correlation plots.

1. Launch the **IIO Oscilloscope** application by double-clicking the icon on the Desktop.

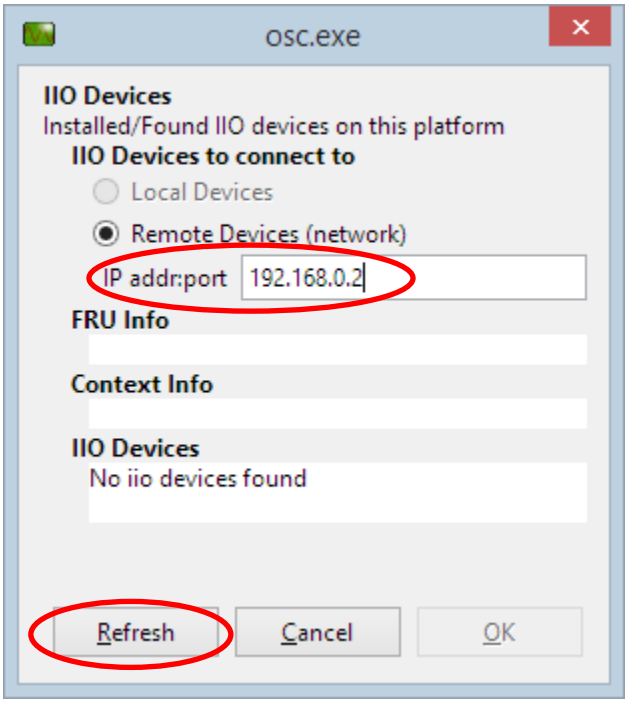


2. The IIO Oscilloscope application will start with a blank window.

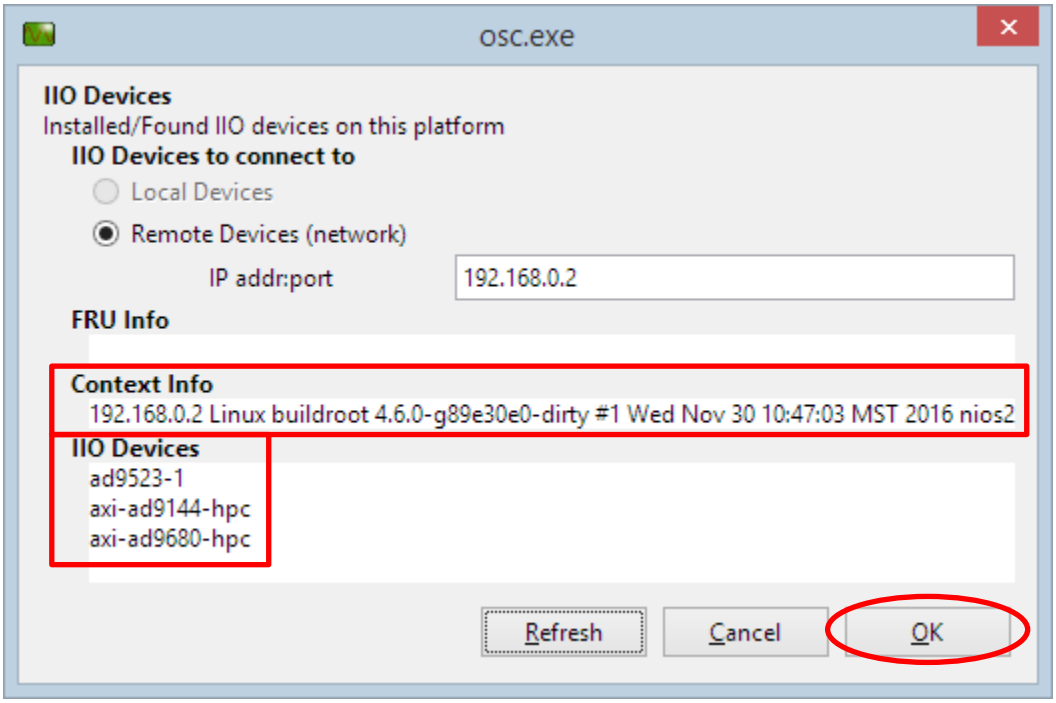


3. Establish a network connection from the IIO Oscilloscope application by selecting **Settings -> Connect**

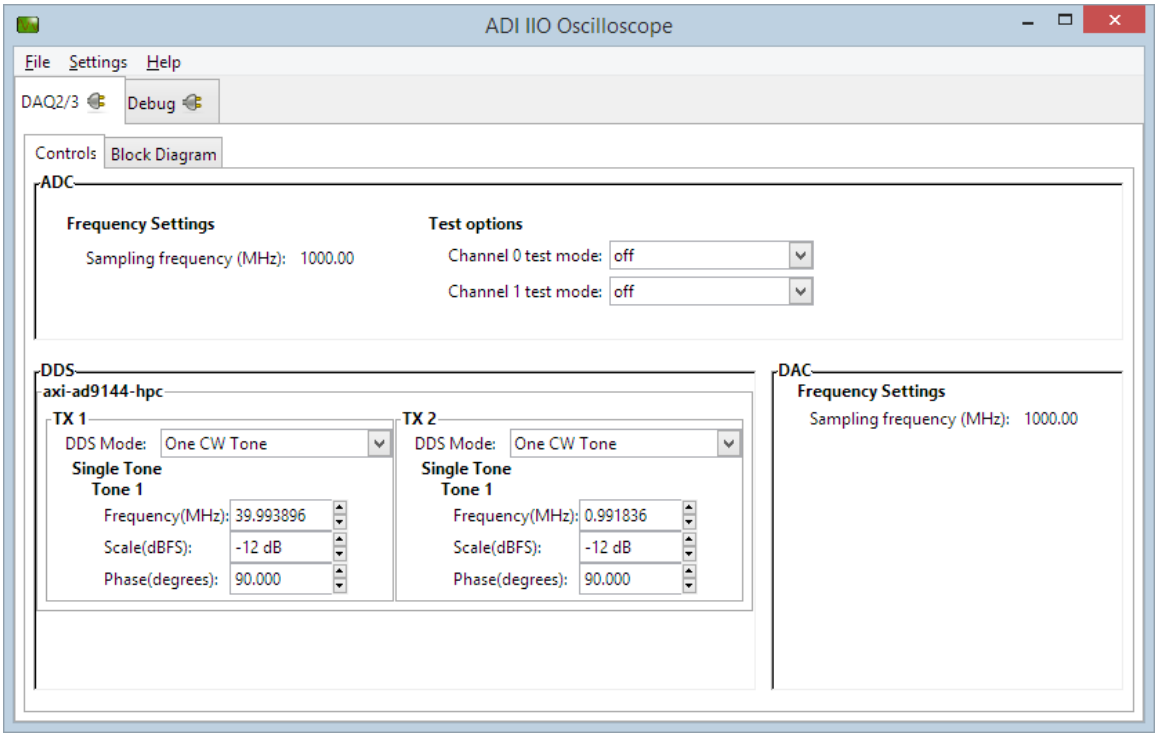
4. Enter the IP address **192.168.0.2** into the **IP addr:port** field and click **Refresh.**



5. A successful connection is verified by observing the **Context Info** and **IIO Devices** fields as shown here. Click **OK.**



The ADI IIO Oscilloscope window will now be populated as shown (some values may differ):

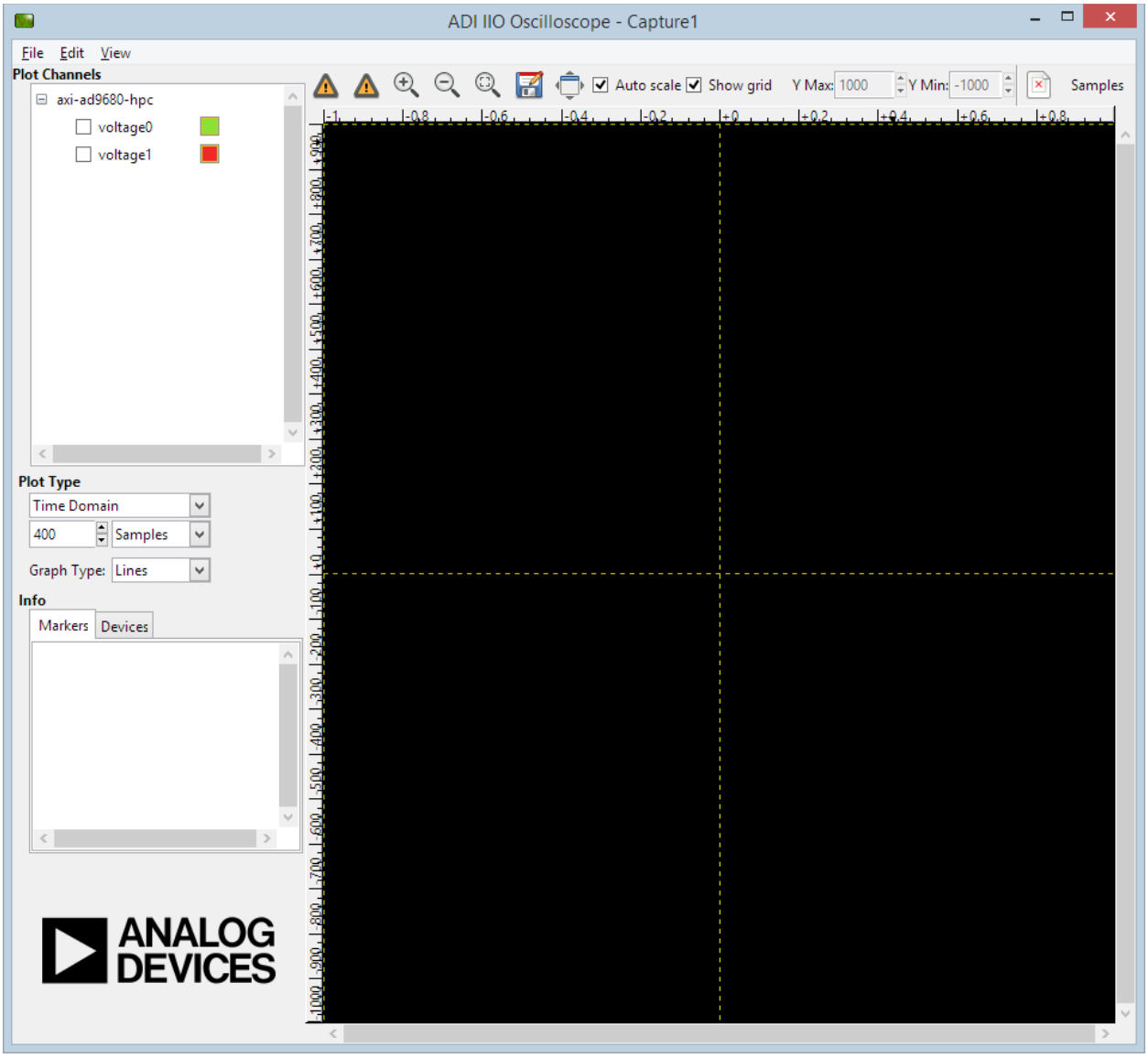


6. Enable the FPGA IP to generate a 40 MHz sine wave for the AD9144 **TX 1** channel by highlighting the **Frequency(Mhz)** field and typing in '**40**'. Set amplitude by typing '**-12**' in **Scale(dBFS)** window then press **Enter**. Note: The frequency requested will be adjsted to closest match possible that the FPGA DDS IP blocks can synthesize.

Note: TX 2 is not enabled for this demo setup. Set 'DDS Mode' to 'Disable' just as a reminder.

7.3 Create Plots

1. In the **ADI IIO Oscilloscope** window, using the pull-down menu select **File -> New Plot.**
   A new **ADI IIO Oscilloscope – Capture 1** window will open:



2. Check the selection boxes next to **voltage0** and **voltage1** in the **Plot Channels** panel. These equate to the I & Q channels respectively for the Analog Devices AD9144 DAC.

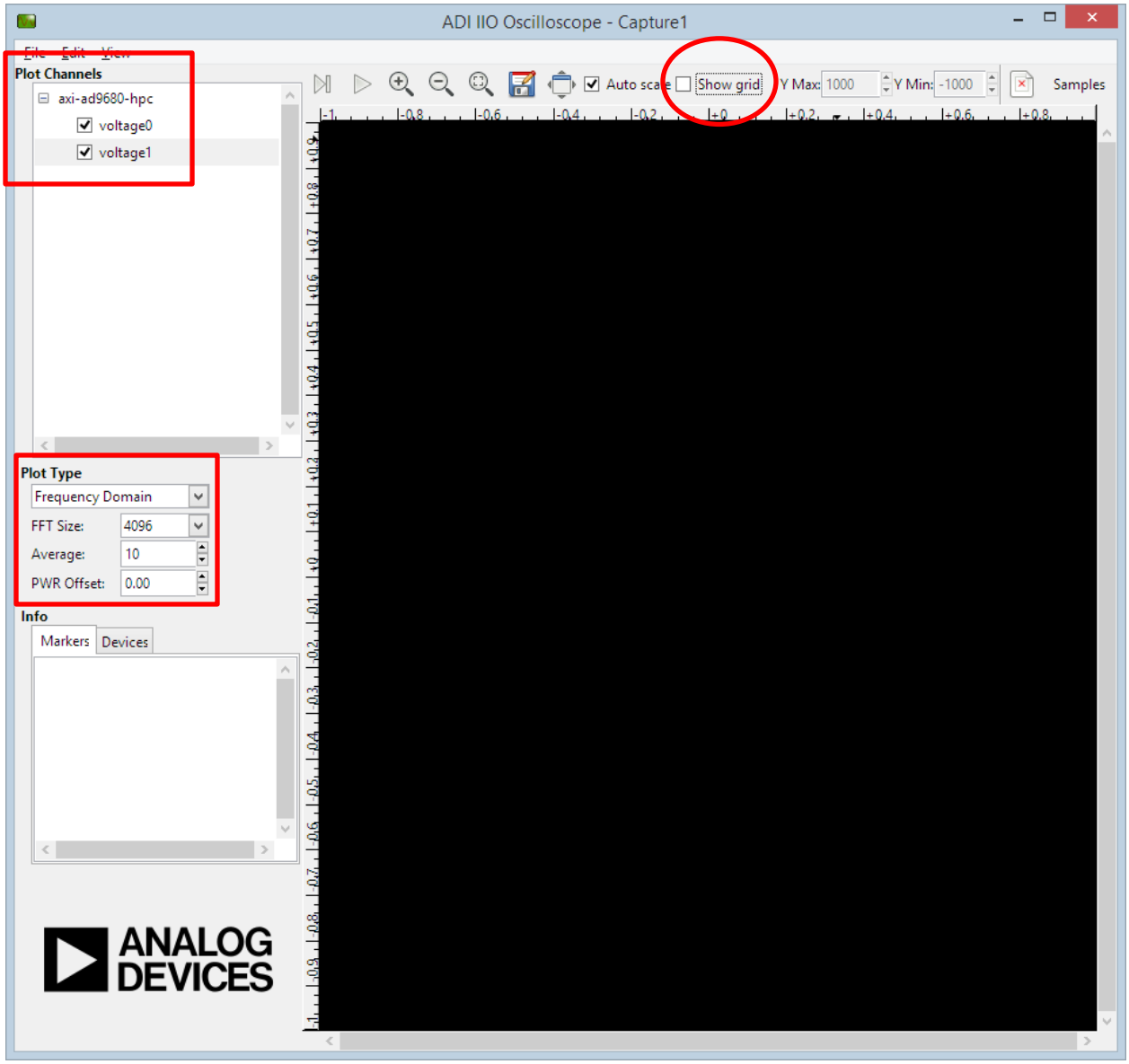
3. Change the **Plot Type** to **Frequency Domain** via the drop-down list.

4. Change the **FFT Size** to **4096**

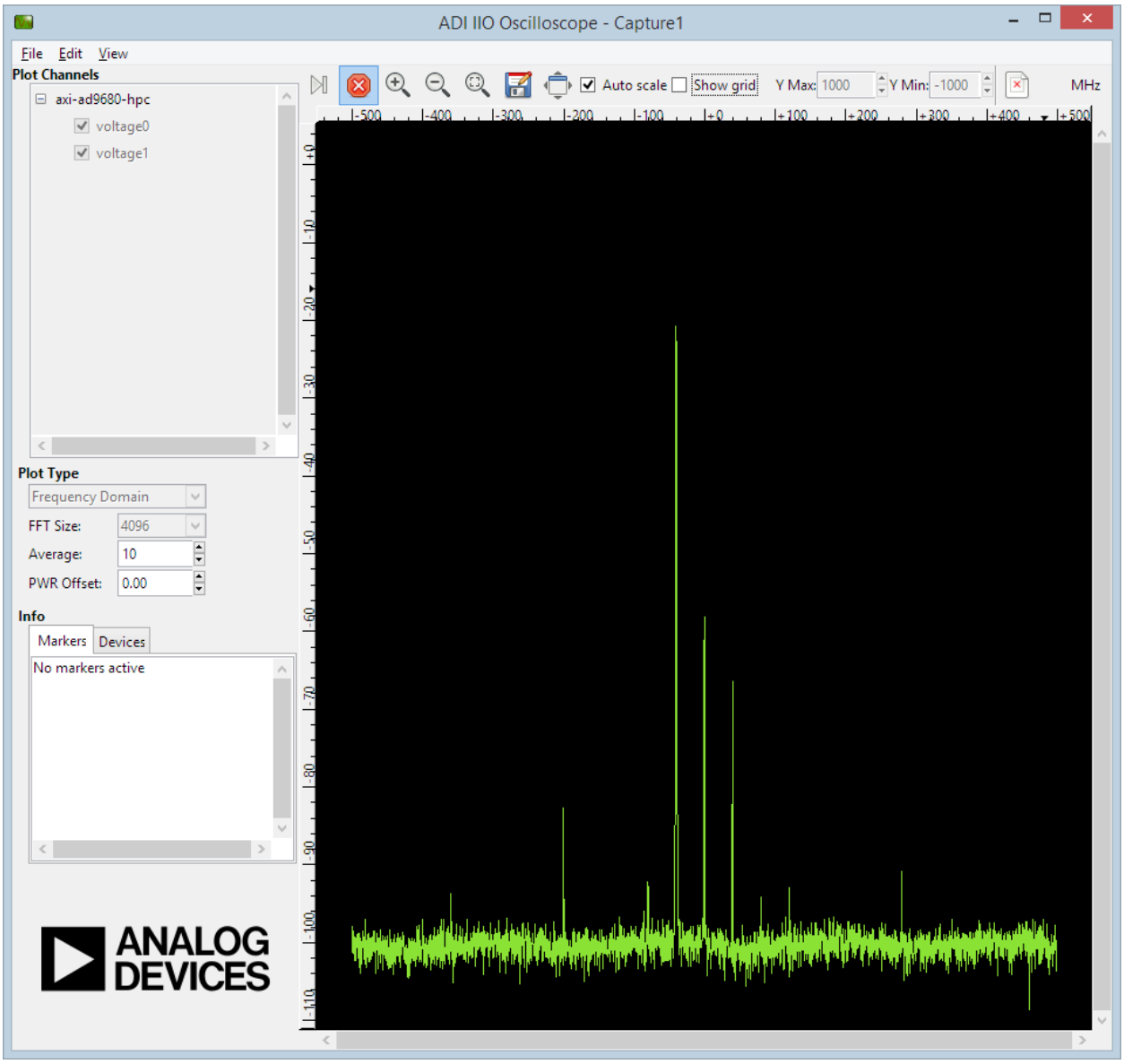
5. Set the **Average** to **10**

6. Uncheck the **Show Grid** selection box near the top of the window.

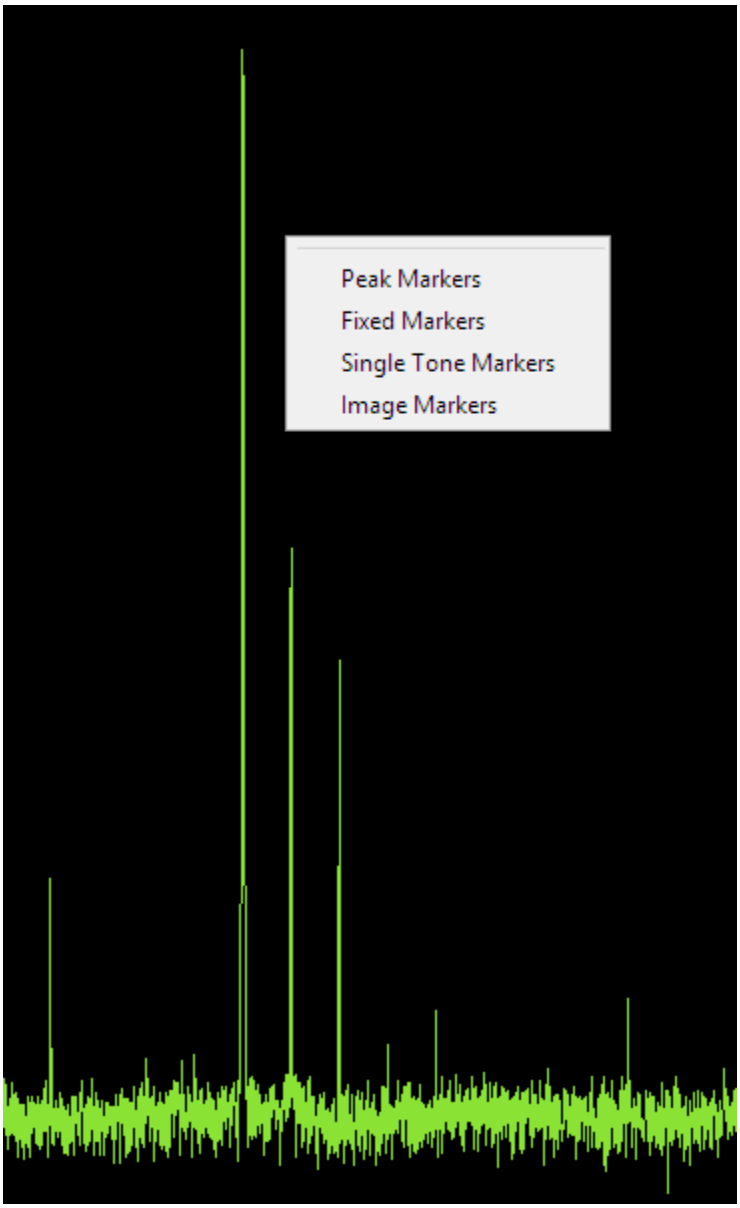
The ADI IIO Oscilloscope – Capture 1 window should now look like this:



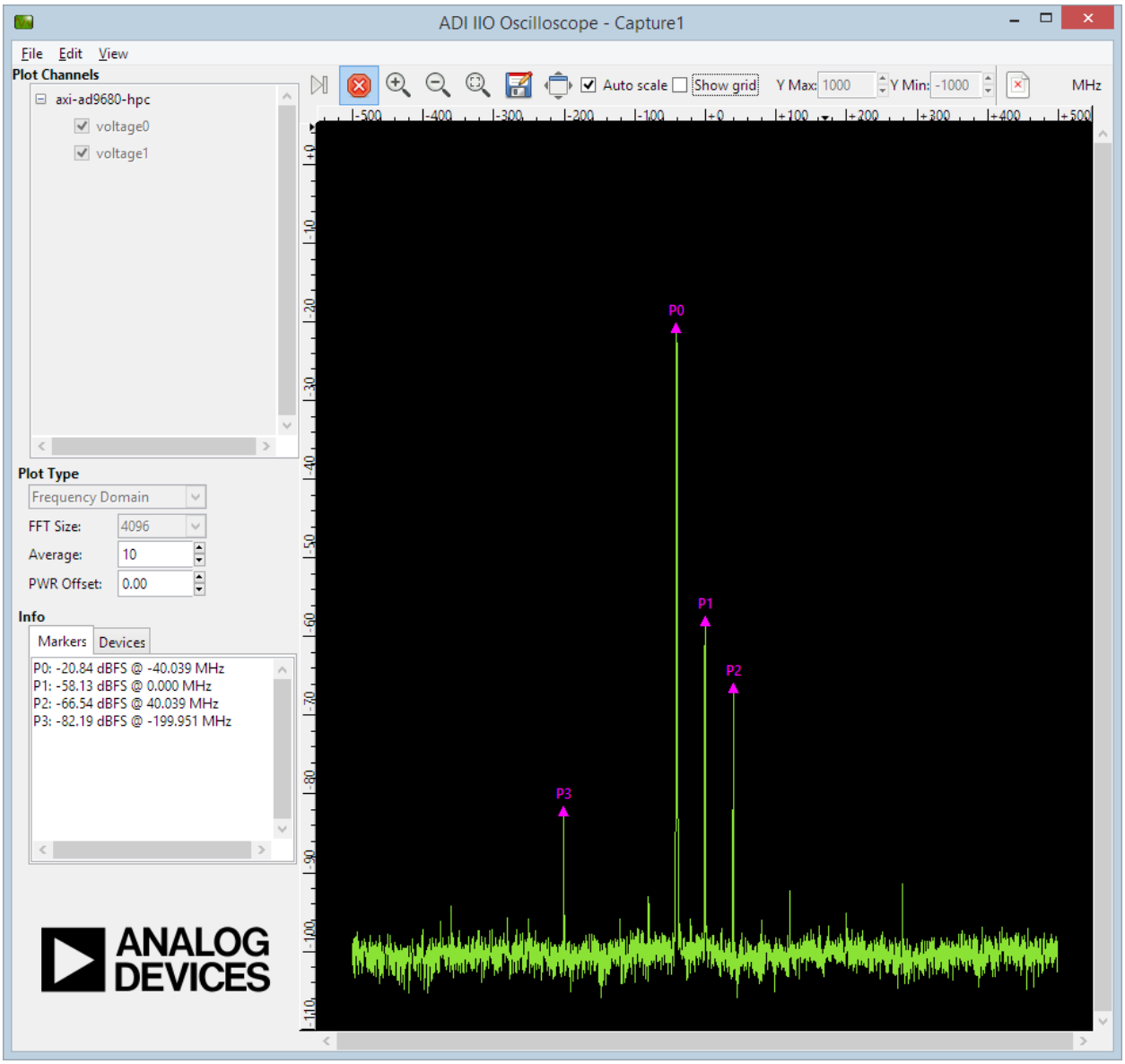
7. Click on the "**play**" button  near the top of the window to start the oscilloscope capture.



8. Set markers on the plot by right-clicking in the middle of the plot and selecting the marker of choice. (**Peak Markers** is a good choice…)

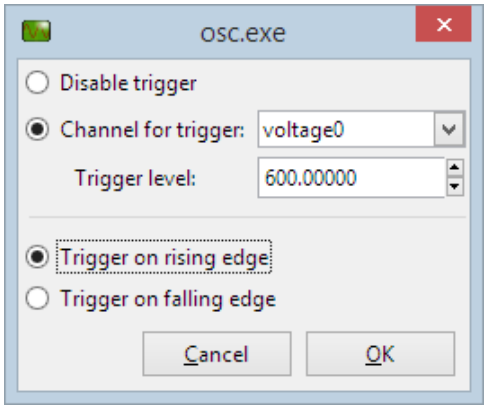


Once markers are set, they will persist on the plot and the details of each marker are displayed in the **Info** panel.

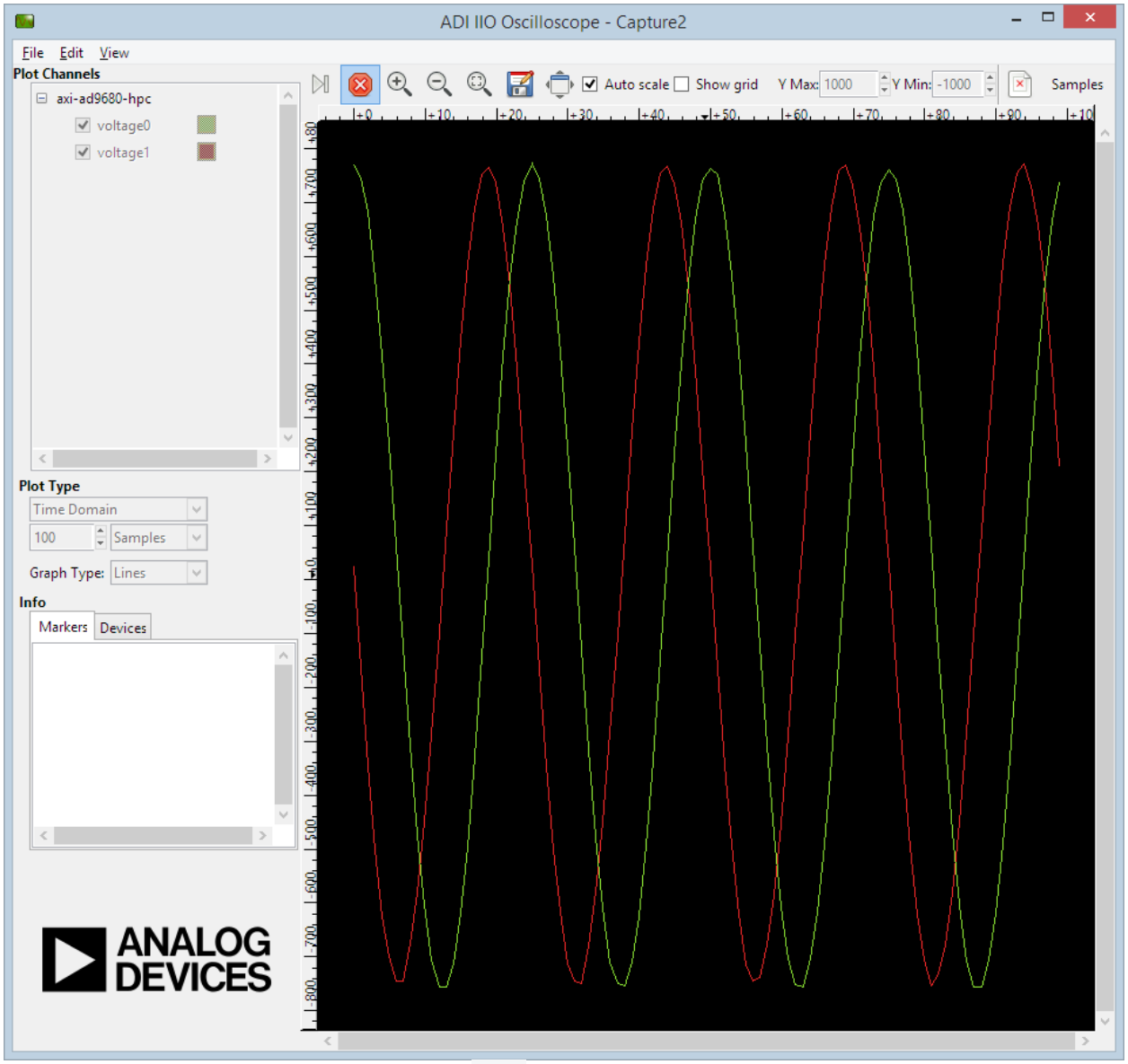


9. Add a second plot by clicking the  icon in the upper-right corner of the Capture 1 window. Set up the new **ADI IIO Oscilloscope – Capture 2** window to plot in the **Time Domain** with **100** Samples on both voltage channels.
10. Right-click on the **axi-ad9680-hpc** in the **Plot Channels** panel and select **Trigger settings**.

11. Select the radio button for **Channel for trigger: voltage0** and set the **Trigger level** to **600**. Click **OK**.



12. Click "**play**" to observe the new time domain plot.

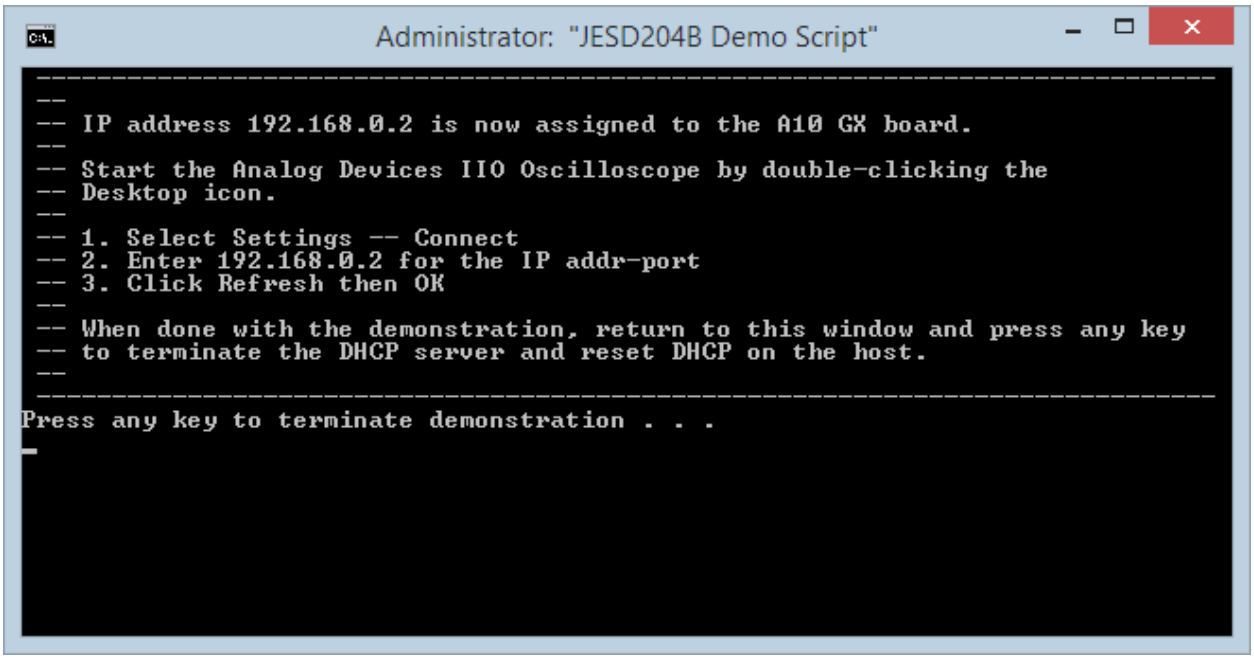


13. Stop the capture by clicking the "stop" icon  in each of the capture windows as desired**.** (A plot must be stopped in order to make changes to its capture settings.)
14. From here, play around with different settings in the ADI IIO Oscilloscope ADC/DAC control window and change the **DDS Single Tone: Tone 1 Frequency (MHz)** and observe the changes in the plots.
15. Change the **DDS Mode** to **TWO CW Tones** and observe 2 frequencies in the plots.

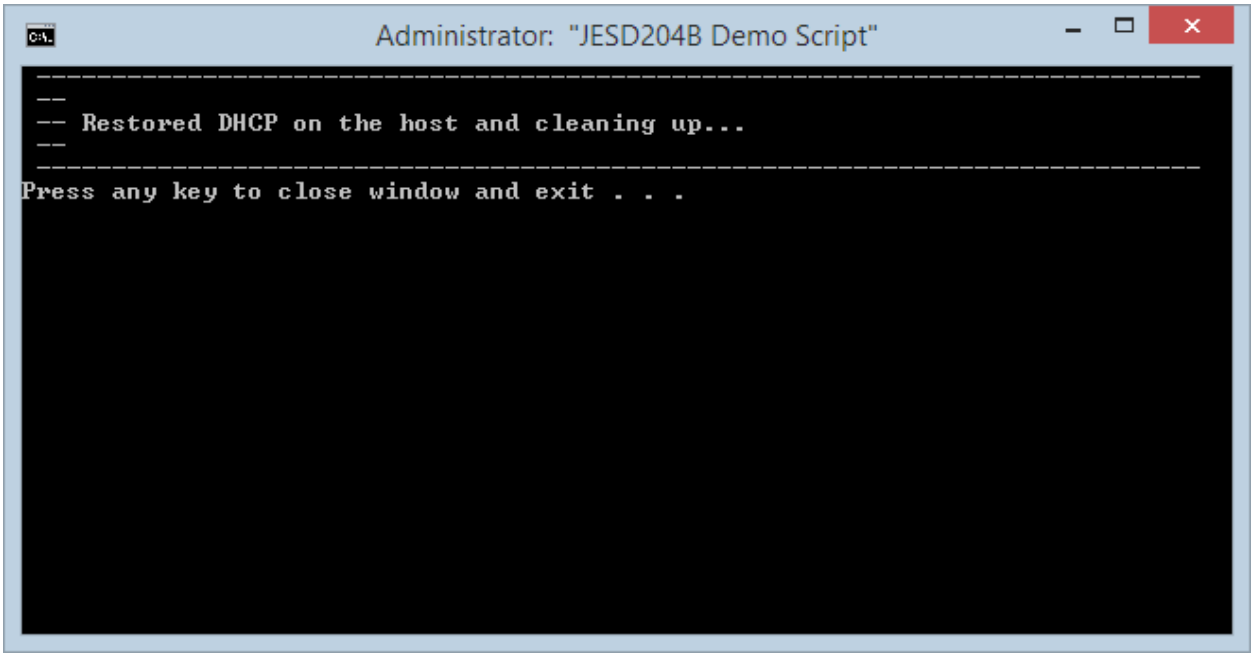
Feel free to poke around and play with any of the settings and plotting options. Note that due to the large amount of high speed data being received by the FPGA and plotted, sometimes the plots momentarily hang. They do return to functioning once you stop and restart the plot(s).

7.4 Shutdown

1. When done with the demo, **close** the **Capture** windows and **close** the **ADI IIO Oscilloscope** window.
2. **IMPORTANT** – To properly reset the host PC Ethernet network interface to DHCP, in the **JESD204B Demo Script** window running the DHCP server, **press any key** to properly terminate the script. This will force the DHCP server to stop and the batch file will restore the DHCP settings on the host.



3. **Press any key** to close the final window completing the demonstration script.



8. Building the Hardware and Software Reference Designs

This section describes how to obtain the source code and build the hardware and software portions of the reference design. The reference design provides a starting point for the user to create their own custom designs.

The reference designs were created and are maintained by Analog Devices Inc.

8.1 Hardware reference design resources

The following Analog Devices Inc. resources are available

- HDL User Guide - https://wiki.analog.com/resources/fpga/docs/hdl
- Latest Release Notes - https://github.com/analogdevicesinc/hdl/releases
- HDL Help & Support - https://ez.analog.com/community/fpga

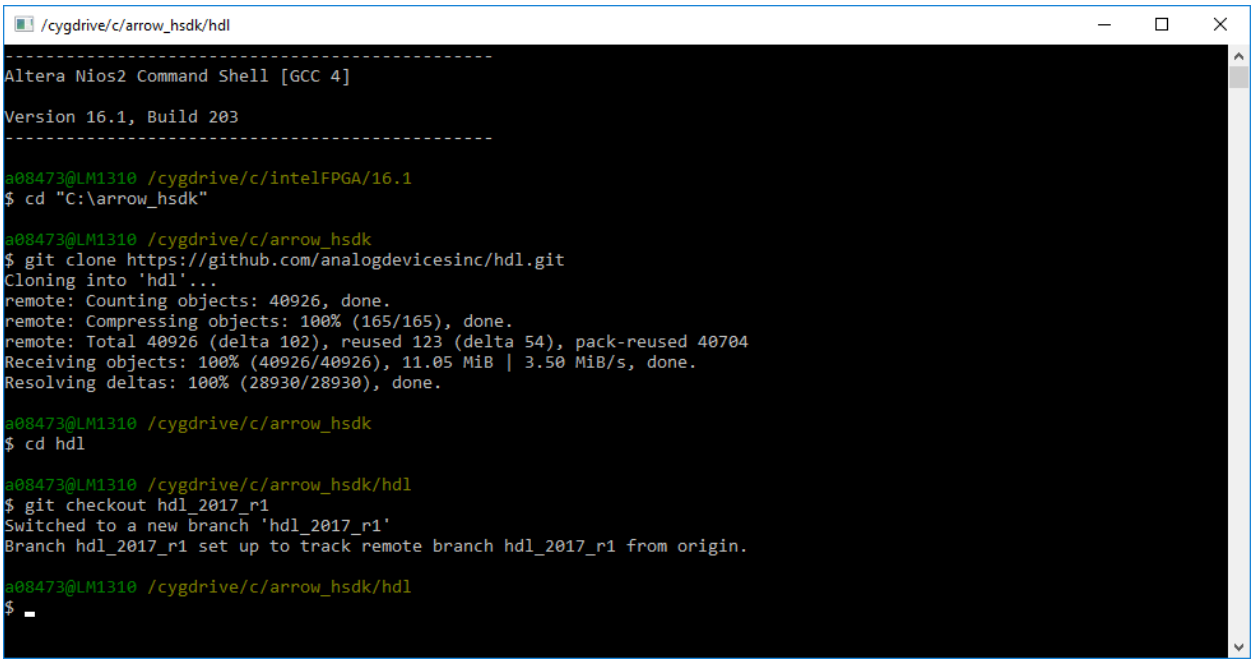
8.2 Install the Intel PSG development tools

The Quartus II Prime 16.1 Standard or Pro tools are required to build the hardware reference design

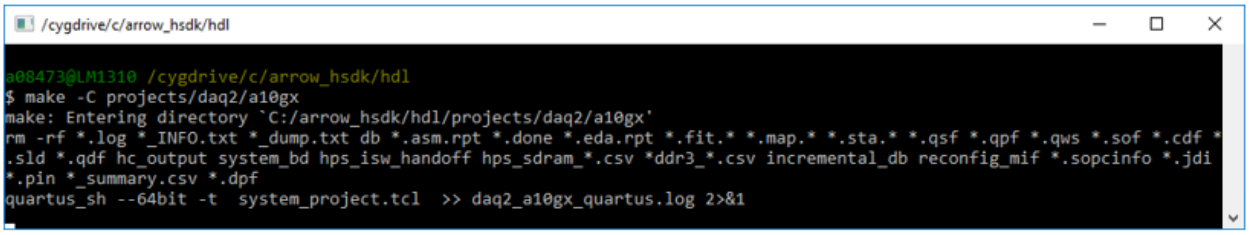
- Download the tools from https://www.altera.com/downloads/download-center.html and install
- Obtain licenses for Quartus and the Intellectual Property cores included in the reference design.

8.3 Build the hardware reference design

- open a **nios2 16.1 command shell**
- navigate to a selected directory
- git clone https://github.com/analogdevicesinc/hdl.git
- cd hdl
- git checkout **hdl_2017_r1**

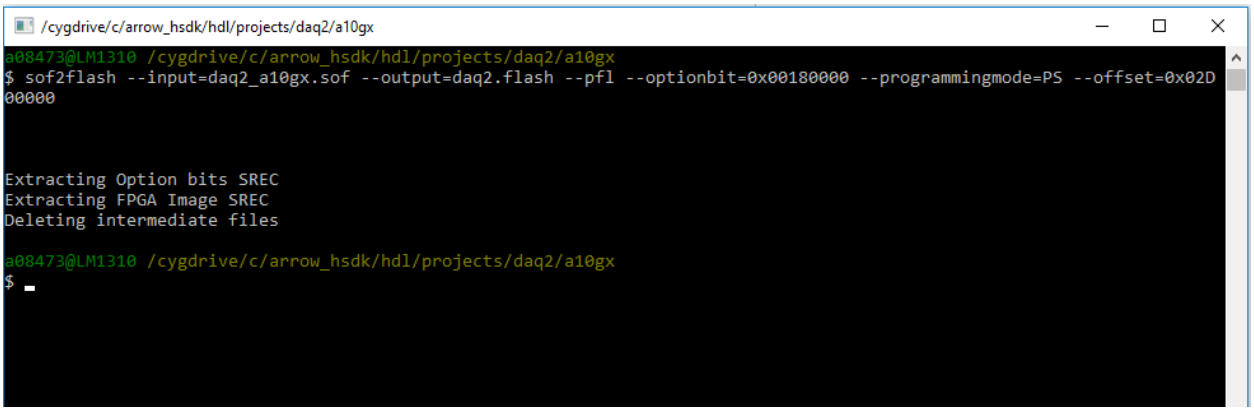


- **make -C projects/daq2/a10gx**
- The project can take up to an hour to build. All build information is saved to the **daq2_a10gx_quartus.log** test file



8.4 Create the hardware flash image

- From the current hdl directory cd to projects/daq2/a10gx
- sof2flash --input=daq2_a10gx.sof --output=daq2.flash --pfl --optionbit=0x00180000 --programmingmode=PS --offset=0x02D00000



Use the Board Update Portal to upload the image to flash as described in chapter 9

8.5 Software reference design resources

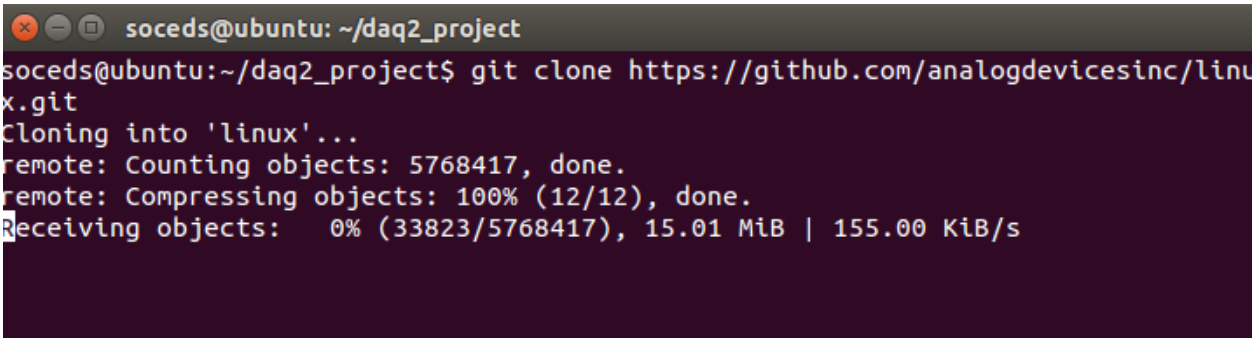
The following Analog Devices Inc. resources are available

- Nios II Linux https://wiki.analog.com/resources/tools-software/linux-drivers/platforms/nios2

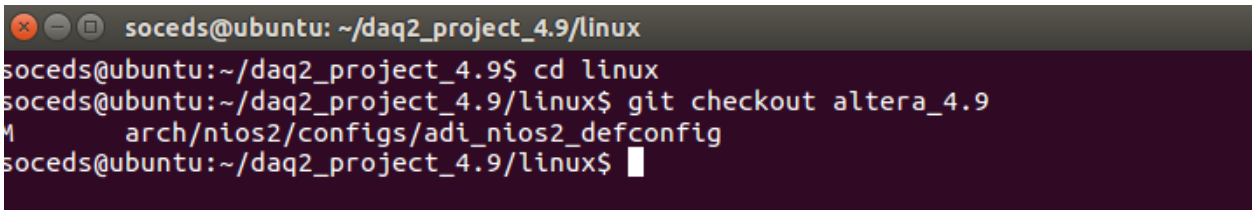
8.6 Build Linux for the Nios II processor

The following instructions assume that the user has a Linux host available. The build for the Arrow High Speed Development kit was tested using a host with Ubuntu 14.04 LTS

- open shell on the Linux host. cd to a <project_directory>
- git clone https://github.com/analogdevicesinc/linux.git



- cd linux/
- git checkout altera_4.9

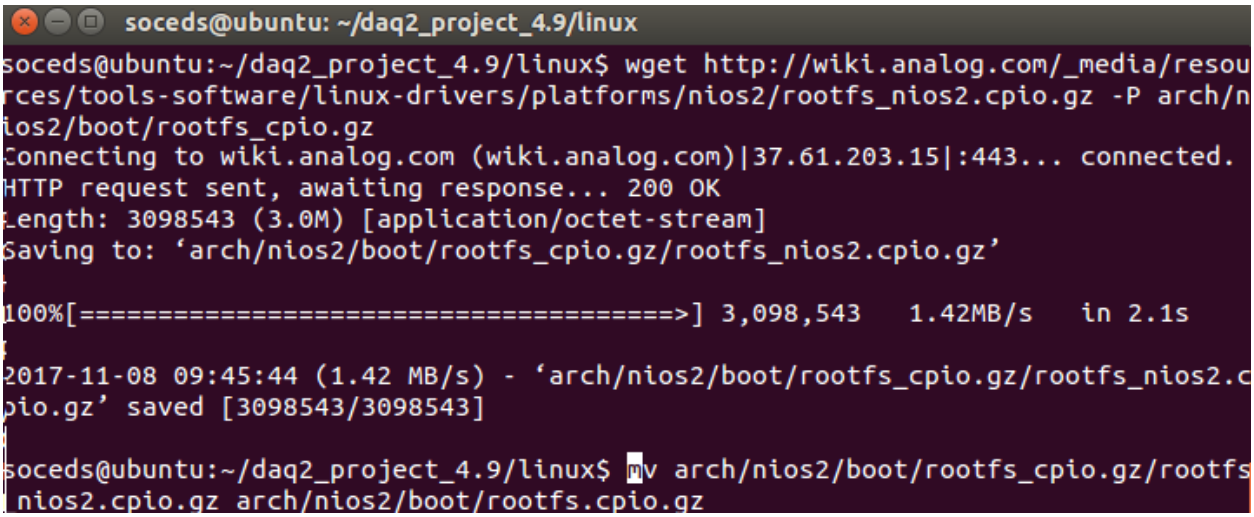


get the nios2 root file system

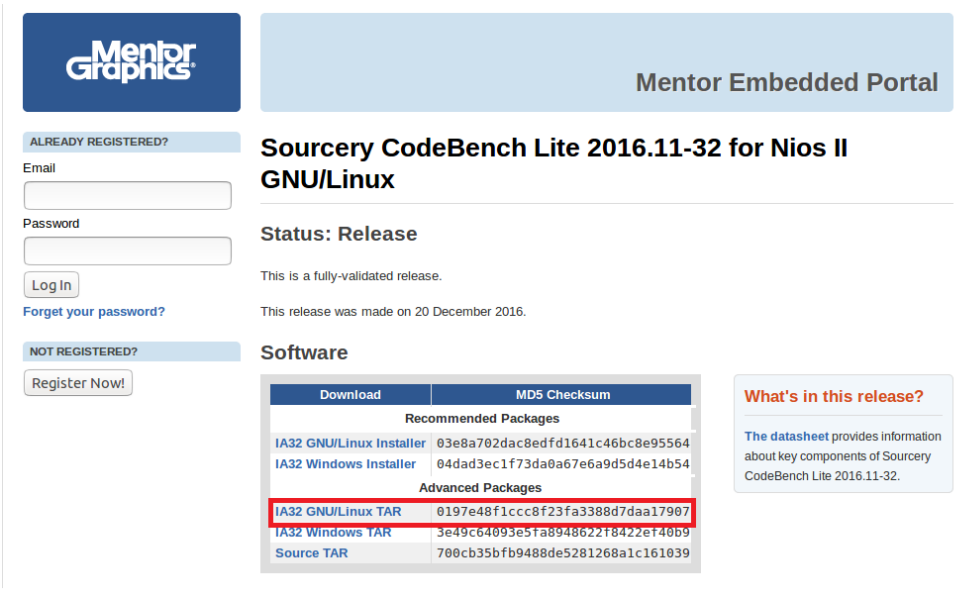
- wget http://wiki.analog.com/_media/resources/tools-software/linux-drivers/platforms/nios2/rootfs_nios2.cpio.gz -P arch/nios2/boot/rootfs_cpio.gz

move the rootfs to the appropriate folder

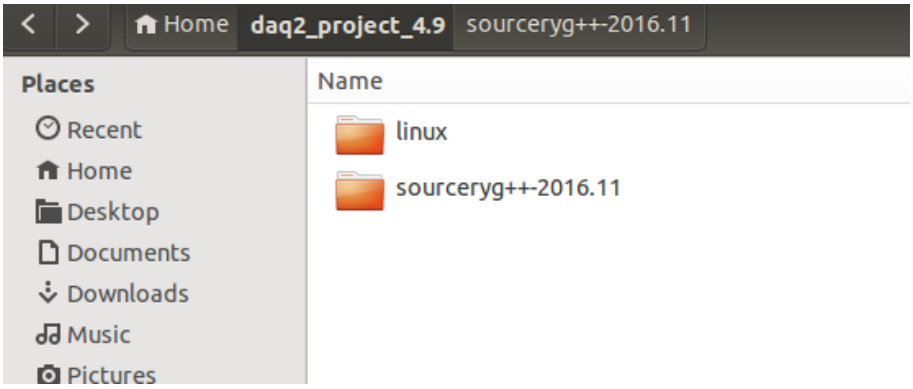
- mv arch/nios2/boot/rootfs_cpio.gz/rootfs_nios2.cpio.gz **arch/nios2/boot/rootfs.cpio.gz**



- **get nios toolchain from codesourcery**. download **advanced package IA32 GNU/Linux**
- https://sourcery.mentor.com/GNUToolchain/release3275



- untar into the <project directory>



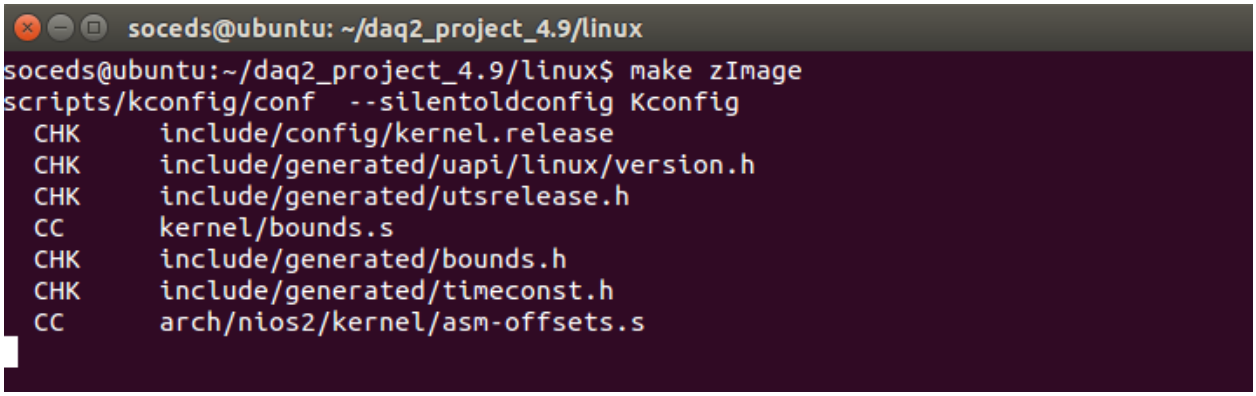
- export ARCH=nios2
- export CROSS_COMPILE=<project directory>/sourceryg++2016.11/bin/**nios2-linux-gnu-**

```
soceds@ubuntu: ~/daq2_project_4.9/linux
soceds@ubuntu:~/daq2_project_4.9/linux$ export ARCH=nios2
soceds@ubuntu:~/daq2_project_4.9/linux$
soceds@ubuntu:~/daq2_project_4.9/linux$
soceds@ubuntu:~/daq2_project_4.9/linux$ export CROSS_COMPILE=../sourceryg++-2016
.11/bin/nios2-linux-gnu-
soceds@ubuntu:~/daq2_project_4.9/linux$
```

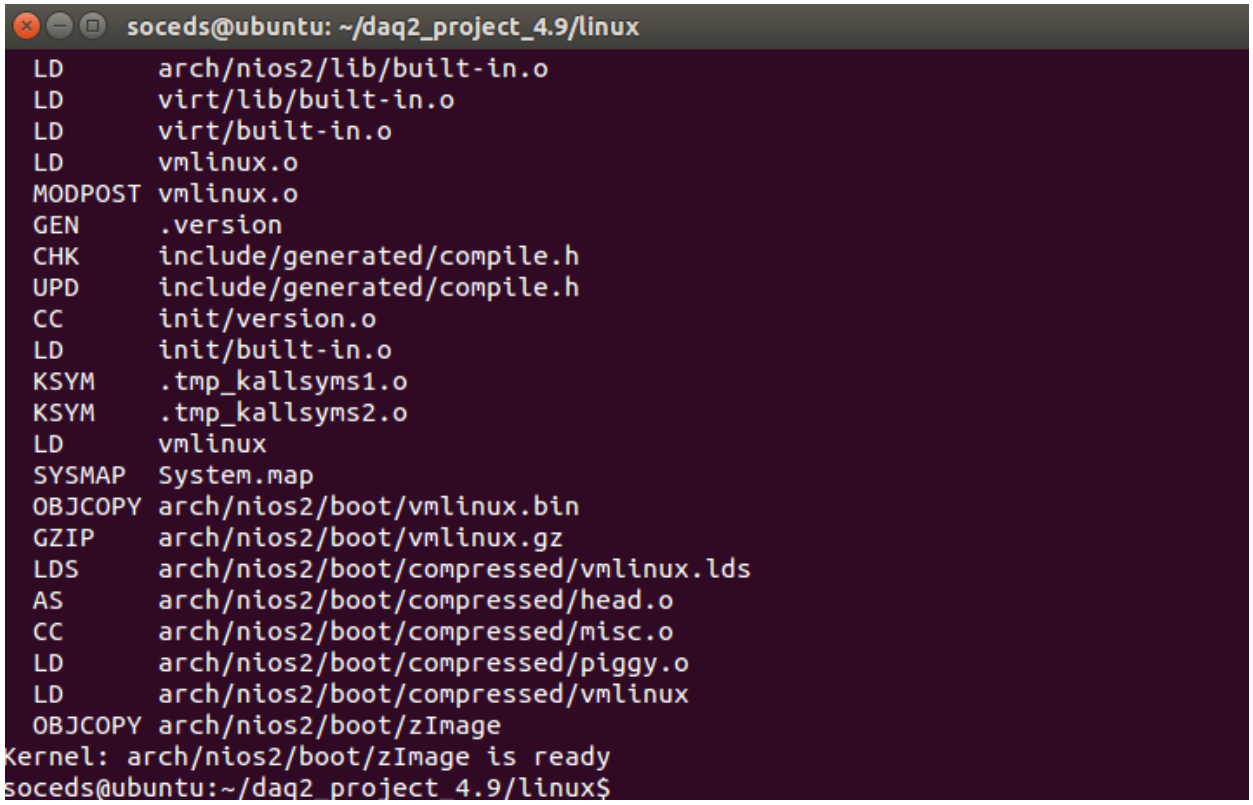
- make **adi_nios2_defconfig**
- cp arch/nios2/boot/dts/a10gx_daq2.dts arch/nios2/boot/devicetree.dts

```
soceds@ubuntu: ~/daq2_project_4.9/linux
soceds@ubuntu:~/daq2_project_4.9/linux$ make adi_nios2_defconfig
#
# configuration written to .config
#
soceds@ubuntu:~/daq2_project_4.9/linux$ cp arch/nios2/boot/dts/a10gx_daq2.dts ar
ch/nios2/boot/devicetree.dts
soceds@ubuntu:~/daq2_project_4.9/linux$
```

- make zImage

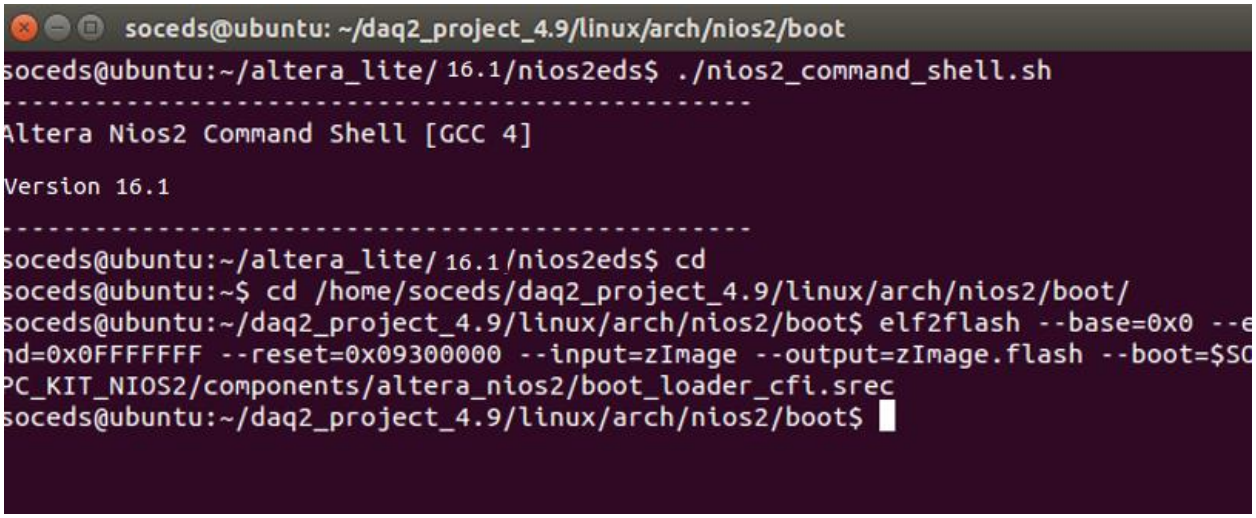


- the zImage file is located in arch/nios2/boot



8.7 Create the software flash image

- open a nios2 16.1 command shell
- cd <project_directory>/linux/arch/nios2/boot
- elf2flash --base=0x0 --end=0x0FFFFFFF --reset=0x09300000 --input=zImage --output=zImage.flash --boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srec



Use the Board Update Portal to upload the image to flash as described in chapter 9.

9. Flashing the Arria 10 GX Development Kit

The instructions in this section will guide you through flashing the demonstration firmware into the Arria 10 GX development kit.

9.1 Navigate to the content folder

- Open the folder previously downloaded in section 4.1
- Unzip **flash_files**.zip
- **daq2.flash** is the **FPGA** image flash file
- **zImage.flash** is the Nios II processor **Linux** image flash file

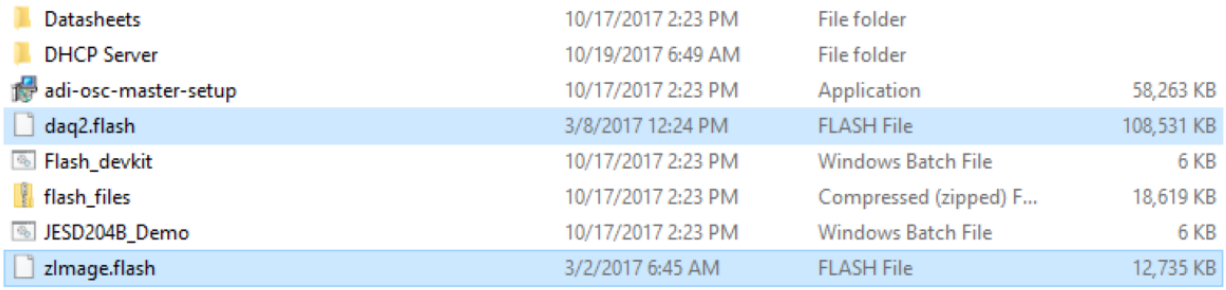
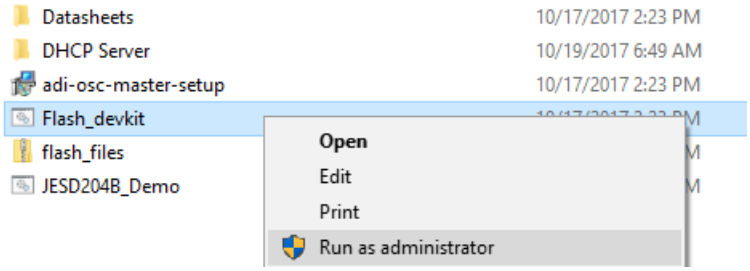


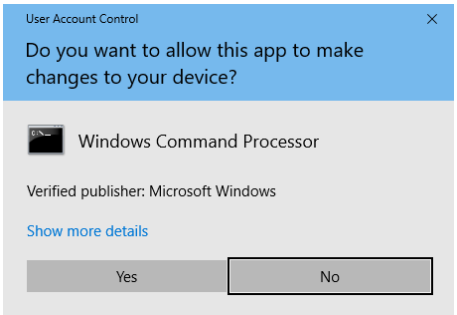
Figure 14- FPGA and Linux files

9.2 Start the DHCP Server

8. Flash_devkit**.bat** batch file as **administrator** by right-clicking the file and selecting **Run as administrator**.



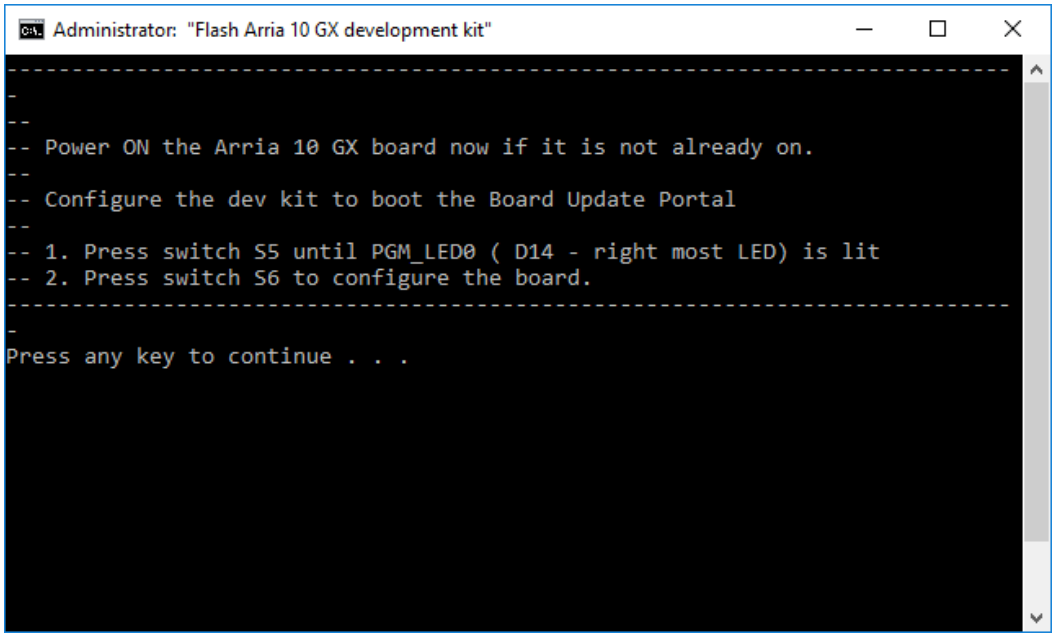
9. Select **Yes** on the **User Account Control** dialog allowing the script to execute.



The "**Flash_devkit**" **Script**" window will open providing information about the script.

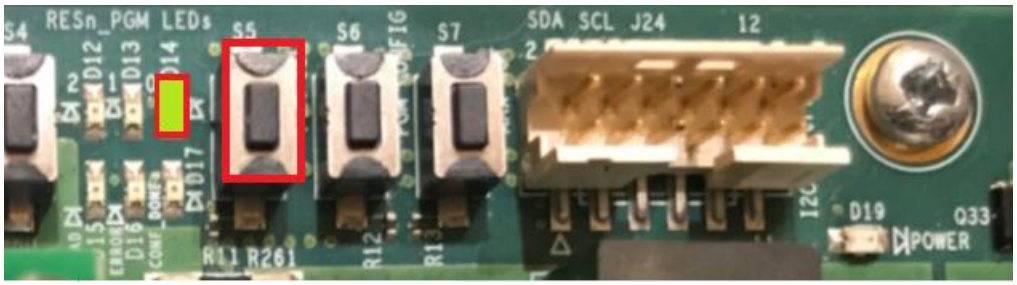
10. **Press any key** on the PC keyboard to continue.

11. Move the power switch, **SW1,** on the Arria 10 GX kit to the **ON** position.

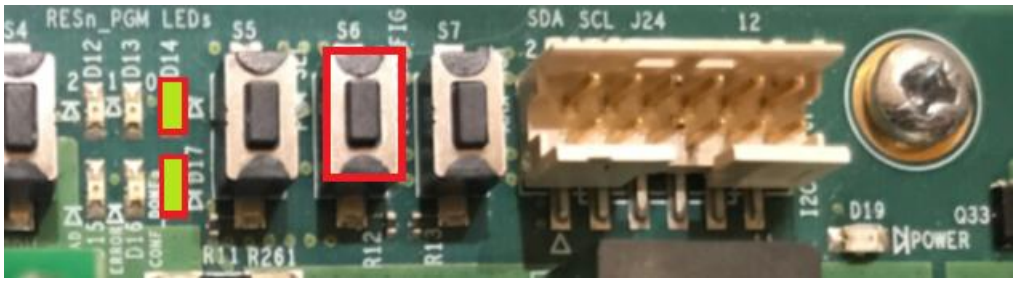


12. Configure the Arria 10 GX development kit to boot the **Board Update Portal** (BUP)

    - Press switch S5 until PGM_LED0 (D14 - right most LED) is lit



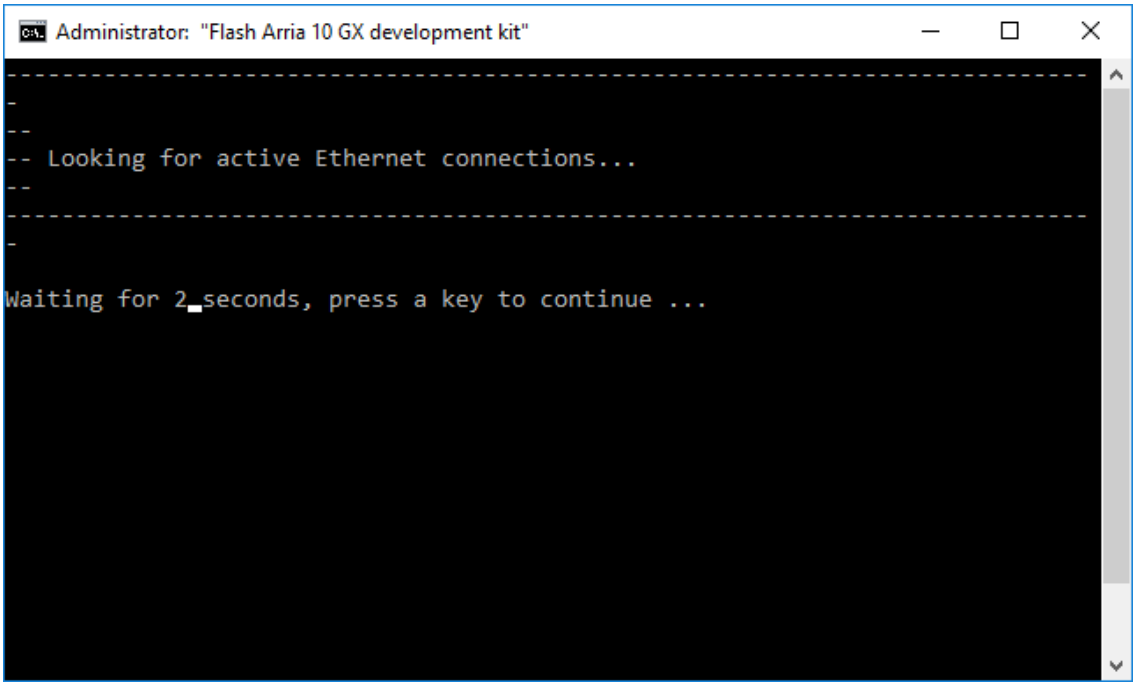
    - Press switch S6 to configure the board. The CONF_DONE LED (D17 – bottom right) will be lit to indicate the BUP image has been loaded into the FPGA



The text below will appear on the display to indicate that the BUP has been successfully loaded into the FPGA.

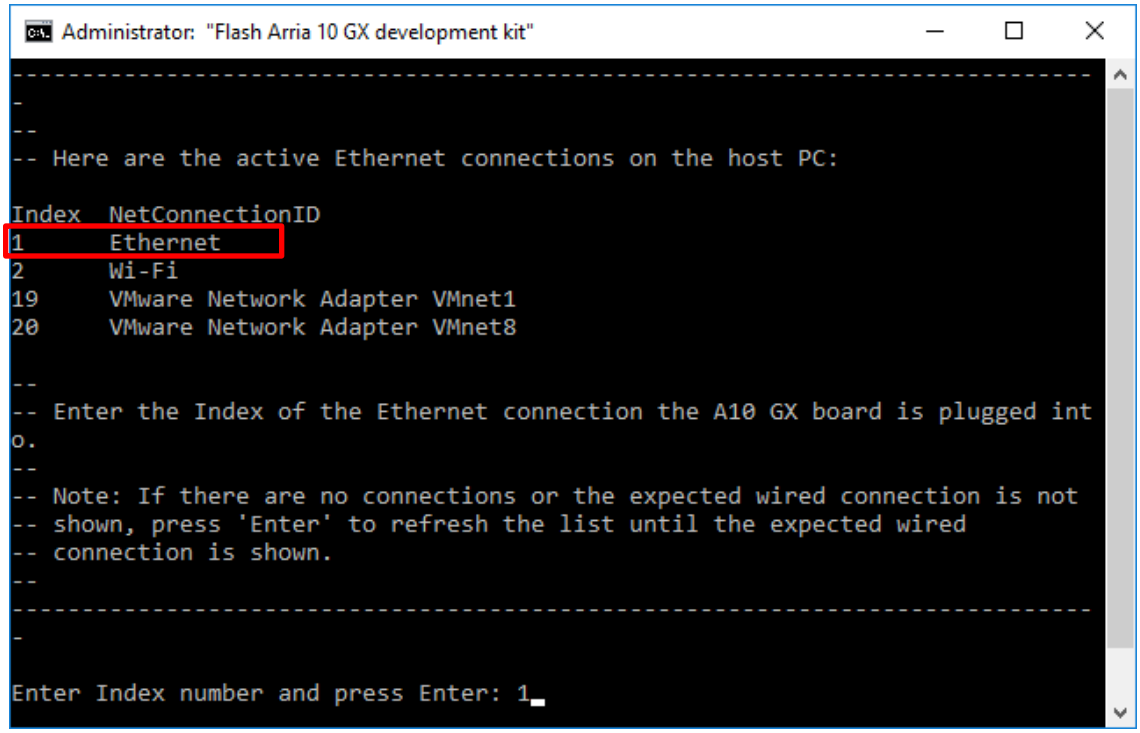
- Press any key on the keyboard to continue.

The script will query the PC Ethernet connections for 5 seconds and automatically report back the active interfaces.

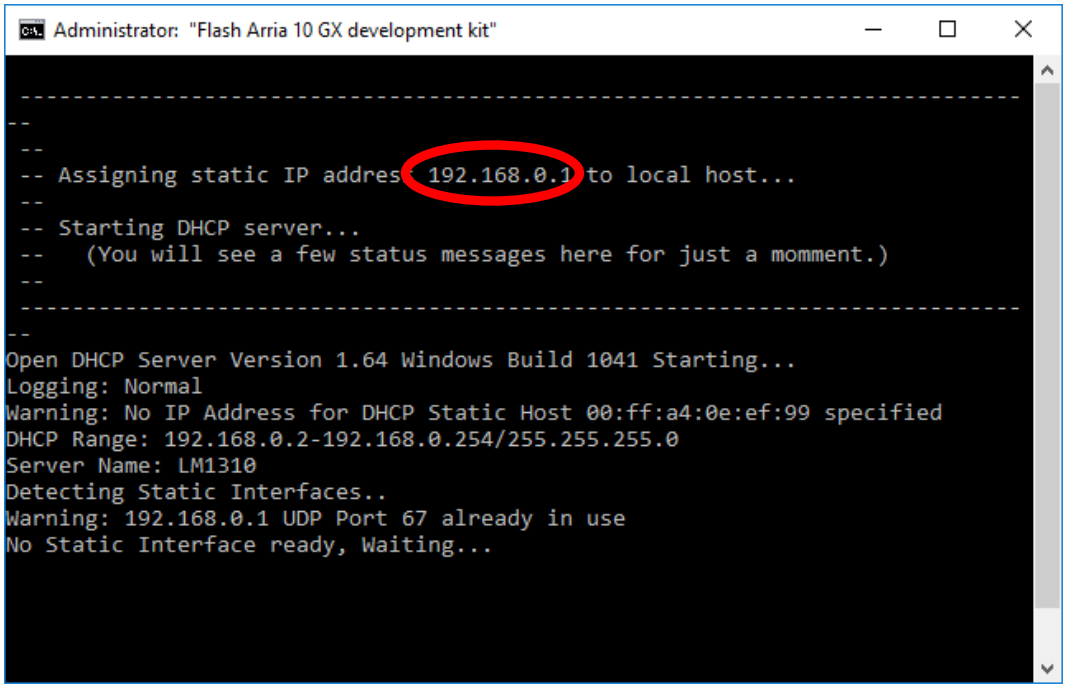


Note: The name of the connections may vary. ('Local Area Connection' or 'Ethernet' are common.)

13. Enter the **Index** number of the Ethernet connection which the A10 GX board is plugged into and press **Enter**. (Index = 1 for "Ethernet" in the below example.)

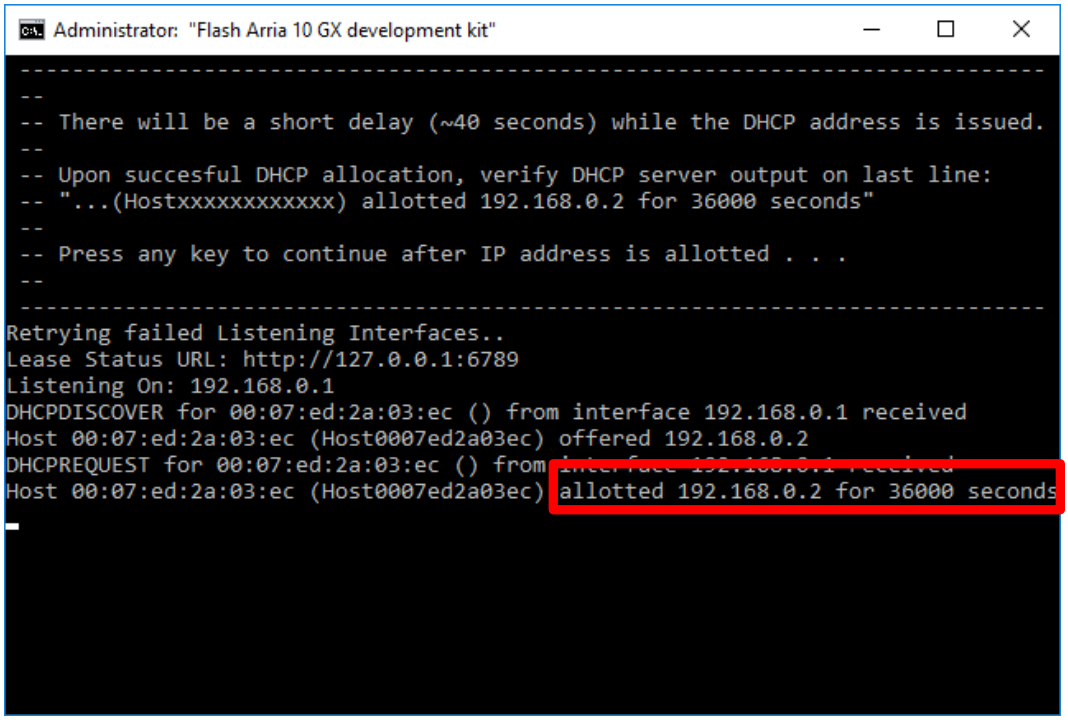


Status messages will appear with information concerning assigning the static IP address to the host and starting the DHCP server. These messages will only appear for a few seconds and then disappear. The entire process can take up to a minute to assign an IP address.



Additional DHCP server status messages will appear with information concerning assigning the static IP address to the Arria 10 GX. Upon successful DHCP allocation, verify the static IP address 192.168.0.2 was assigned to the Arria 10 GX.

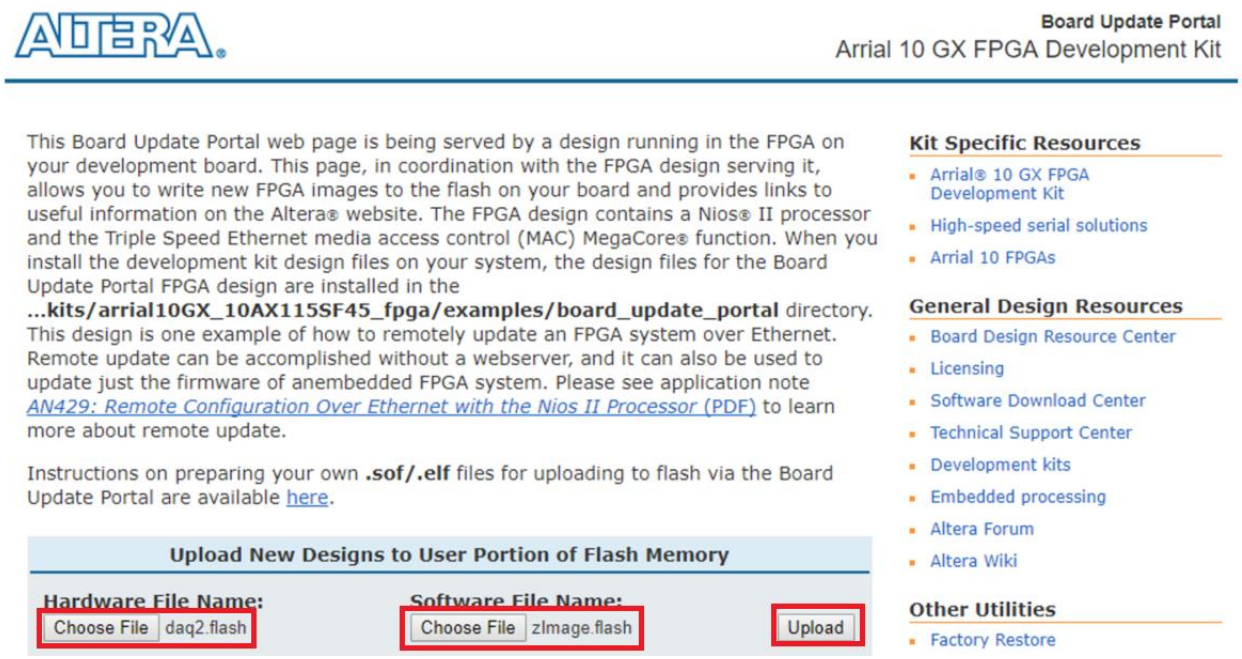
14. **Press any key** once the status message "**Host xx:xx:xx:xx:xx:xx (Hostxxxxxxxxxxxx) allotted 192.168.0.2 for 3600 seconds**" appears. (Note: The "xx" values will vary depending on the host PC MAC address.)



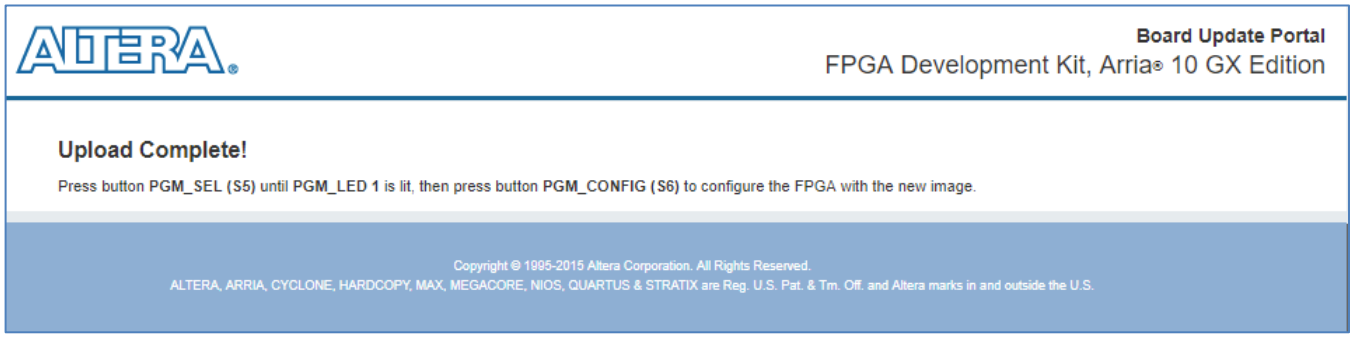
15. Open a web browser to connect to the Board Update Portal

- Open a web browser with the URL set to 192.168.0.2
- Select daq2.flash for the Hardware File Name
- Select zImage.flash for the Software File Name
- Press the Upload button to begin the Upload

The files are large and the upload process can take up to 30 minutes to complete.



The following message will appear when uploading is complete



10. APPENDIX

10.1 More Information

Intel Arria 10 GX FPGA

https://www.altera.com/products/fpga/arria-series/arria-10/overview.html

Intel Arria 10 GX FPGA Development Kit

https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-a10-gx-fpga.html

Analog Devices AD9144 Quad 16-bit 2.8GSPS DAC

http://www.analog.com/en/products/digital-to-analog-converters/da-converters/AD9144.html

Analog Devices 9680 Dual 14-bit 1.25GSPS ADC

http://www.analog.com/en/products/analog-to-digital-converters/high-speed-ad-10msps/ad9680.html

Analog Devices AD-FMCDAQ2-EBZ Evaluation Board

Product page
http://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad-fmcdaq2-ebz.html

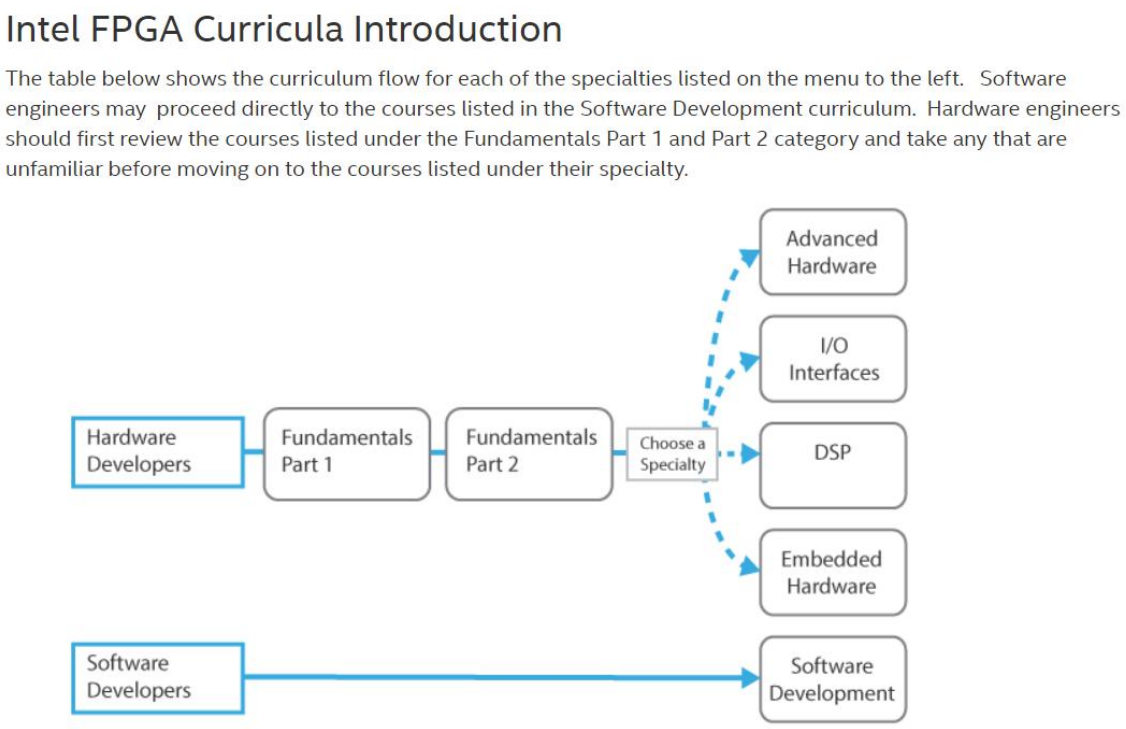
User Guide
https://wiki.analog.com/resources/eval/user-guides/ad-fmcdaq2-ebz

10.2 Online resources

10.2.1 Intel FPGAs

Intel PSG Training Curricula

https://www.altera.com/support/training/curricula.html



Intel PSG DSP Overview

https://www.altera.com/solutions/technology/dsp/overview.html

Intel HLS Compiler Overview

https://www.altera.com/products/design-software/high-level-design/intel-hls-compiler/overview.html

Intel FPGA SDK for OPENCL

https://www.altera.com/products/design-software/embedded-software-developers/opencl/overview.html

10.2.2 Analog Devices

Wiki
https://wiki.analog.com/start

FPGA Reference Designs
https://wiki.analog.com/resources/alliances/altera

Engineer Zone
https://ez.analog.com/community/fpga

Education

http://www.analog.com/en/education.html

10.2.3 Arrow Electronics

Product site:

https://www.arrow.com/

Github site:

https://github.com/arrow-socfpga/arrow-high-speed-data-acquisition-kit

11. REVISION HISTORY

Revision	Changes	Date
1.0	Pre-release	2/8/2017
2.0	Initial release	6/7/2017
3.0	Added instructions on downloading and flashing image from Github	10/17/2017
4.0	Modified to include instructions on productized version	11/9/2017