# FINAL PROJECT

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# CMPEN 331- Section 2

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## Abstract:

For the honors component of Lab 5, I extended the basic pipelined MIPS CPU by implementing a forwarding unit to handle data hazards without introducing stalls. This module detects dependencies between instructions across pipeline stages and dynamically selects the correct data source—whether from the EXE, MEM, or WB stage—to forward into the ALU inputs. I also integrated this functionality into the main datapath using two muxes (forwardA and forwardB), ensuring that the ALU always receives the most recent values. This enhancement allows the CPU to execute dependent instructions in consecutive cycles without delay, making the pipeline more efficient and closer to how real-world processors operate. The design was verified through simulation using a custom testbench that displayed the correct execution and resolution of data hazards in real time.

**Device: Zyboboard (XC7Z010- -1CLG400C)**

A screenshot of a computer code

AI-generated content may be incorrect. A screenshot of a computer program

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## Schematic Design

A diagram of a computer network

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## Waveform

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## Floorplanning

A screenshot of a computer

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## IO Planning A screenshot of a computer game AI-generated content may be incorrect.

Bitstream:

I tried changing the device and tried a lot of implementations, but it doesn't seem to adapt to the requirements. I am unsure whether it is a hardware issue with the computer I was working on in the W136 Lab. I have discussed the matter with TA Wasih.