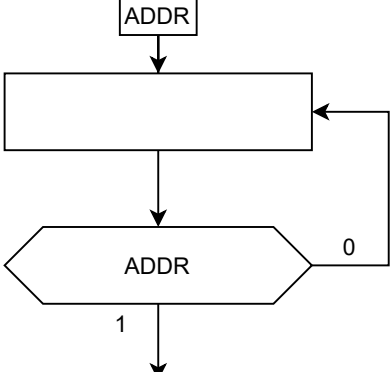
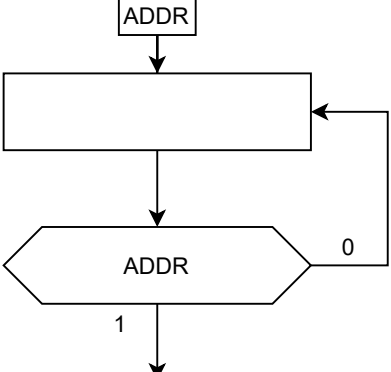
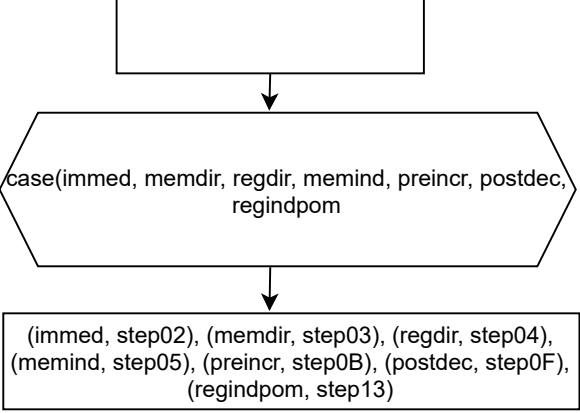
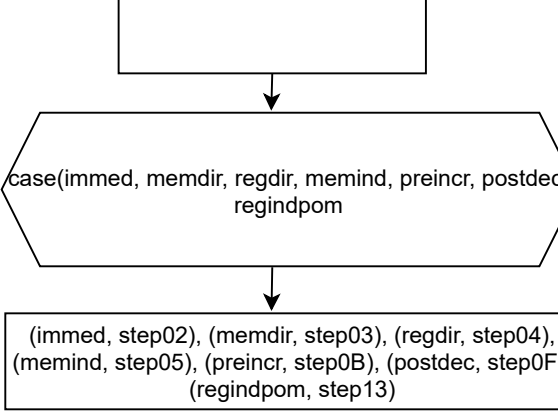
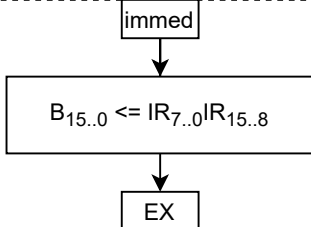
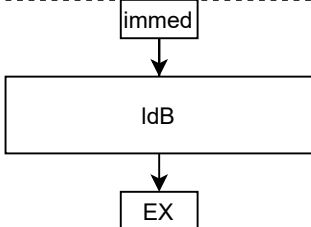
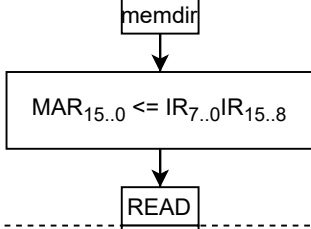
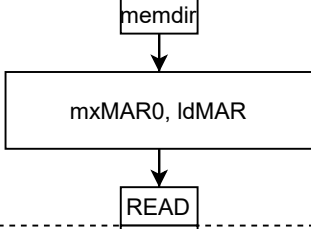
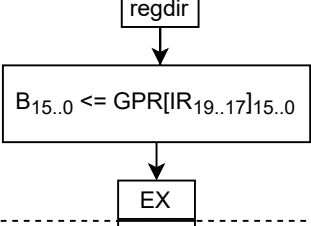
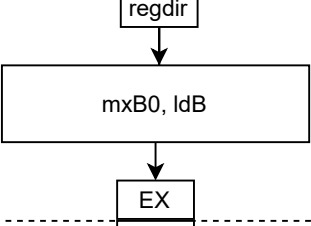
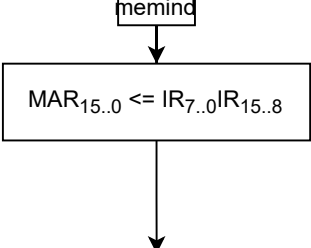
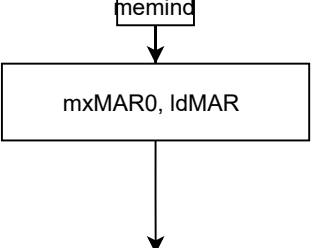


Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
 <pre> graph TD     ADDR[ADDR] --&gt; Box1[ ]     Box1 --&gt; ADDR_hex{{ADDR}}     ADDR_hex -- 0 --&gt; Box1     ADDR_hex -- 1 --&gt; Box2[ ] </pre>	 <pre> graph TD     ADDR[ADDR] --&gt; Box1[ ]     Box1 --&gt; ADDR_hex{{ADDR}}     ADDR_hex -- 0 --&gt; Box1     ADDR_hex -- 1 --&gt; Box2[ ] </pre>	step00 br(if notADDR then step00)
 <pre> graph TD     Box1[ ] --&gt; Case{{case(immed, memdir, regdir, memind, preincr, postdec, regindpom)}}     Case --&gt; Box2["(immed, step02), (memdir, step03), (regdir, step04), (memind, step05), (preincr, step0B), (postdec, step0F), (regindpom, step13)"] </pre>	 <pre> graph TD     Box1[ ] --&gt; Case{{case(immed, memdir, regdir, memind, preincr, postdec, regindpom)}}     Case --&gt; Box2["(immed, step02), (memdir, step03), (regdir, step04), (memind, step05), (preincr, step0B), (postdec, step0F), (regindpom, step13)"] </pre>	step01 br(case(immed, memdir, regdir, memind, preincr, postdec, regindpom) then (immed, step02), (memdir, step03), (regdir, step04), (memind, step05), (preincr, step0B), (postdec, step0F), (regindpom, step13))
 <pre> graph TD     immed[immed] --&gt; Box1["B15..0 &lt;= IR7..0IR15..8"]     Box1 --&gt; EX1[EX]     EX1 -- memdir --&gt; Box2["MAR15..0 &lt;= IR7..0IR15..8"] </pre>	 <pre> graph TD     immed[immed] --&gt; IdB[ldB]     IdB --&gt; EX1[EX]     EX1 -- memdir --&gt; Box2["mxMAR0, ldMAR"] </pre>	step02 ldB, br step1A
 <pre> graph TD     EX1[EX] -- memdir --&gt; Box1["MAR15..0 &lt;= IR7..0IR15..8"]     Box1 --&gt; READ1[READ]     READ1 -- regdir --&gt; Box2["B15..0 &lt;= GPR[IR19..17]15..0"] </pre>	 <pre> graph TD     EX1[EX] -- memdir --&gt; Box1["mxMAR0, ldMAR"]     Box1 --&gt; READ1[READ]     READ1 -- regdir --&gt; Box2["mxB0, ldB"] </pre>	step03 mxMAR0, ldMAR, br step14
 <pre> graph TD     READ1[READ] -- regdir --&gt; Box1["B15..0 &lt;= GPR[IR19..17]15..0"]     Box1 --&gt; EX2[EX]     EX2 -- memind --&gt; Box2["MAR15..0 &lt;= IR7..0IR15..8"] </pre>	 <pre> graph TD     READ1[READ] -- regdir --&gt; Box1["mxB0, ldB"]     Box1 --&gt; EX2[EX]     EX2 -- memind --&gt; Box2["mxMAR0, ldMAR"] </pre>	step04 mxB0, ldB, br step1A
 <pre> graph TD     EX2[EX] -- memind --&gt; Box1["MAR15..0 &lt;= IR7..0IR15..8"]     Box1 --&gt; Exit[ ] </pre>	 <pre> graph TD     EX2[EX] -- memind --&gt; Box1["mxMAR0, ldMAR"]     Box1 --&gt; Exit[ ] </pre>	step05 mxMAR0, ldMAR

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Име и презиме

Арсеније Симоновић

Индекс

2019/0471

Потпис

Пројекат

Задатак 76

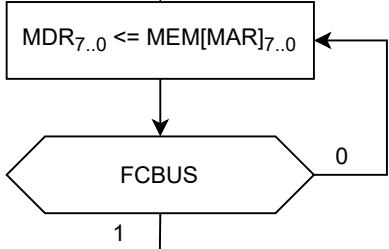
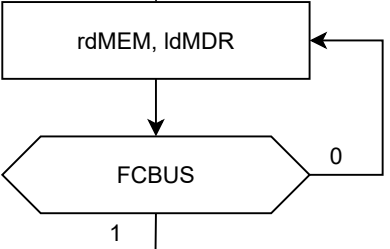
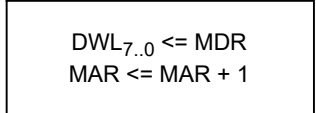
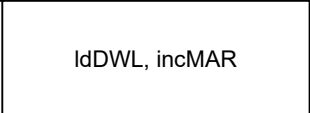
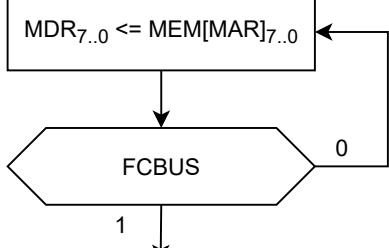
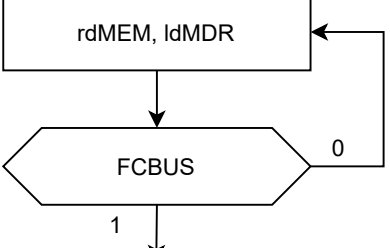
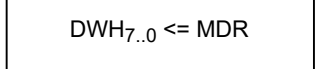
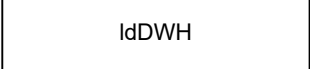
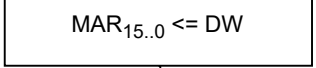
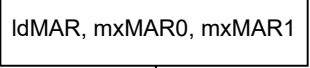


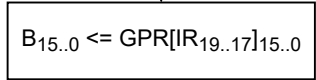
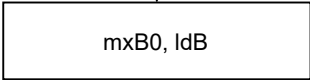
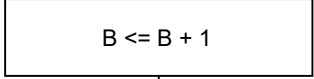
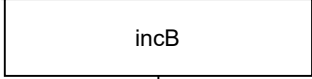
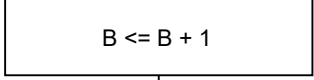
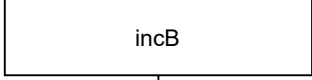
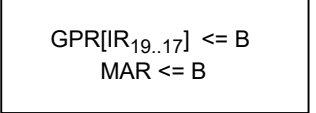
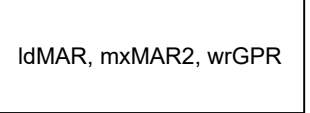


Назив

Основи рачунарске технике 2


Датум

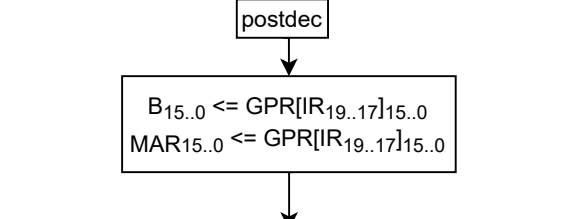
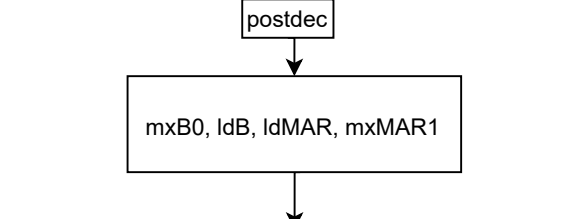
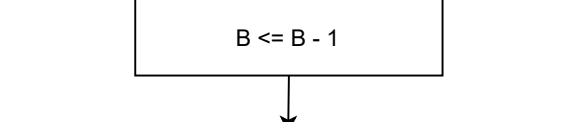
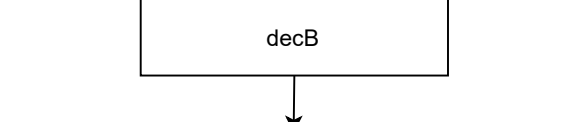
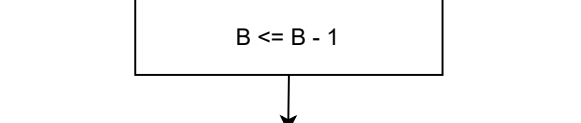
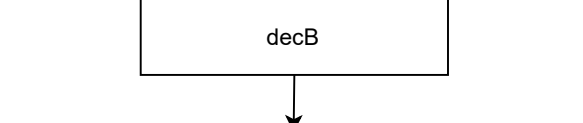
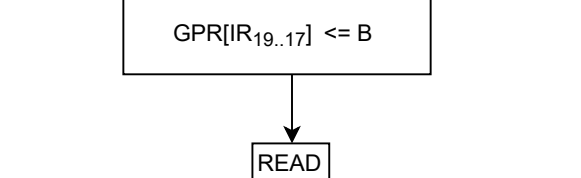
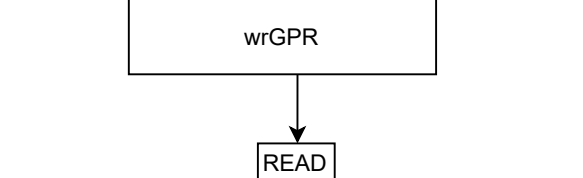
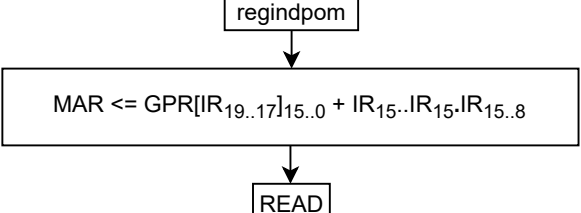
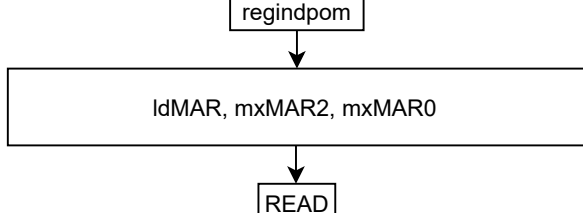
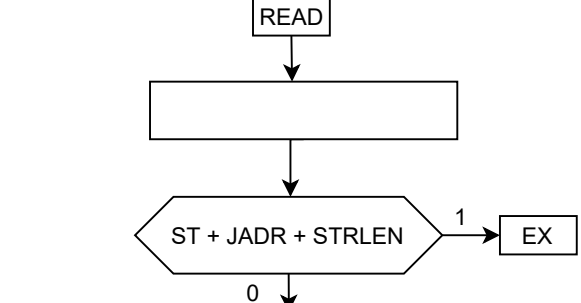
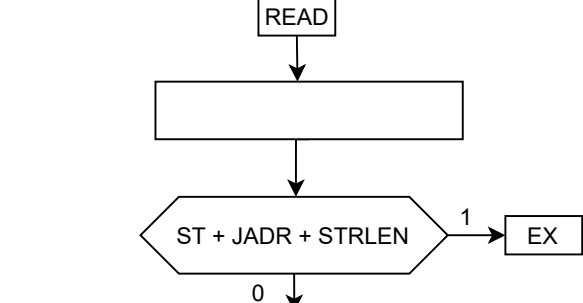
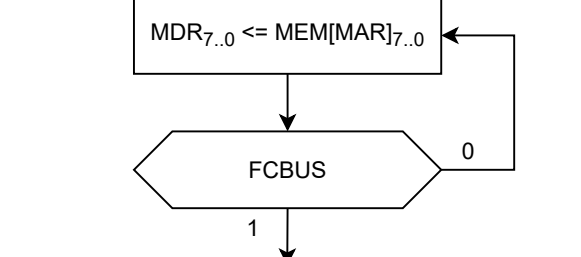
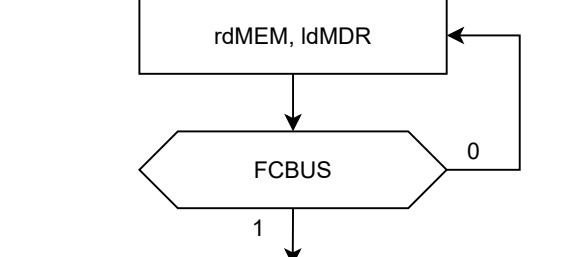
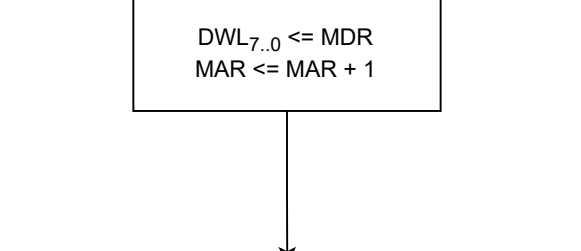
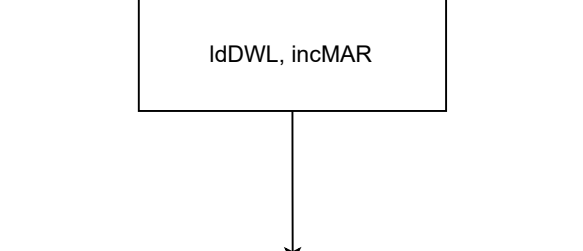
Страна

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Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
		step06 rdMEM, ldMDR, br(if notFCBUS then step06)
		step07 ldDWL, incMAR
		step08 rdMEM, ldMDR, br(if notFCBUS then step08)
		step09 ldDWH
		step0A ldMAR, mxMAR0, mxMAR1, br step14
		step0B mxB0, ldB
		
		step0C incB
		step0D incB
		step0E ldMAR, mxMAR2, wrGPR, br step14
		

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Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
		step0F mxB0, ldB, ldMAR, mxMAR1
		step10 decB
		step11 decB
		step12 wrGPR, br step14
		step13 ldMAR, mxMAR2, mxMAR0
		step14 br(if NoRead then step1A)
		step15 rdMEM, ldMDR, br(if notFCBUS then step15)
		step16 ldDWL, incMAR

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Име и презиме

Арсеније Симоновић

Индекс

2019/0471

Потпис

Пројекат

Задатак 76


Назив

Основи рачунарске технике 2

Датум

Страна

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Дијаграм тока микрооперација		Дијаграм тока управљачких сигнала		Секвенца управљачких сигнала
<div><div>MDR<sub>7..0</sub> &lt;= MEM[MAR]<sub>7..0</sub></div><div>FCBUS</div><div>1</div><div>DWH<sub>7..0</sub> &lt;= MDR</div><div>B<sub>15..0</sub> &lt;= DW</div><div>EX</div><div>EX</div><div>ADDR &lt;= 0 EXEC &lt;= 1</div><div>ADDR</div></div>		<div><div>rdMEM, ldMDR</div><div>FCBUS</div><div>1</div><div>ldDWH</div><div>ldB, mxB1</div><div>EX</div><div>EX</div><div>clADDR, stEXEC</div><div>ADDR</div></div>		<div>step17 rdMEM, ldMDR, br(if notFCBUS then step17)</div> <div>step18 ldDWH</div> <div>step19 ldB, mxB1</div> <div>step1A clADDR, stEXEC, br step00</div>
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	Име и презиме	Индекс	Потпис	Пројекат
	Арсеније Симоновић	2019/0471		Задатак 76
Назив	Основи рачунарске технике 2		Датум	Страна 4/4