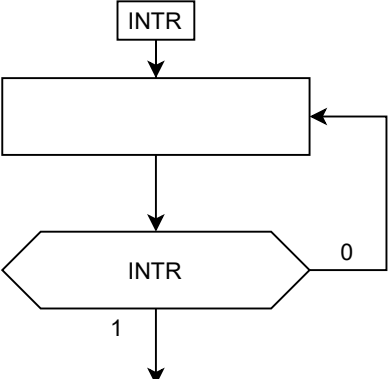
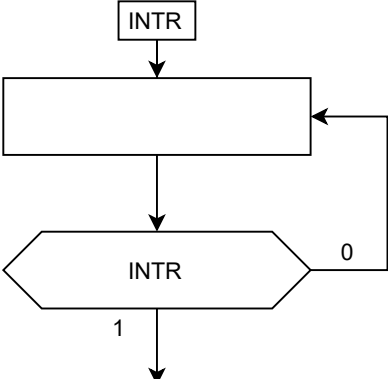
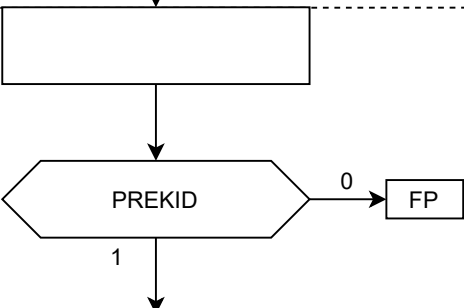
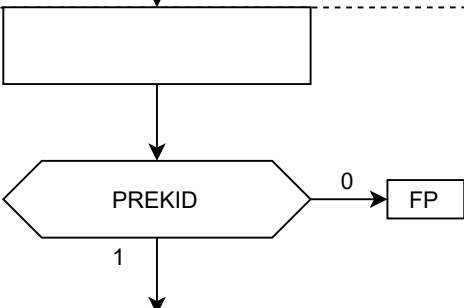
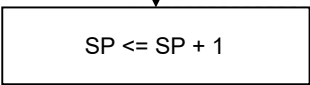

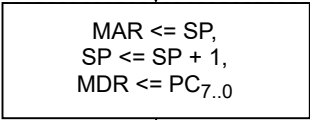
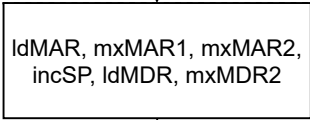
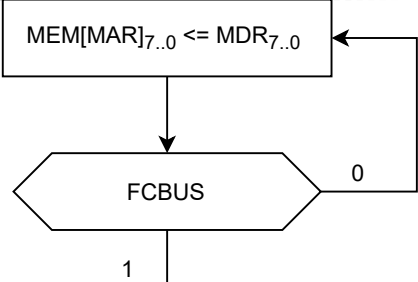
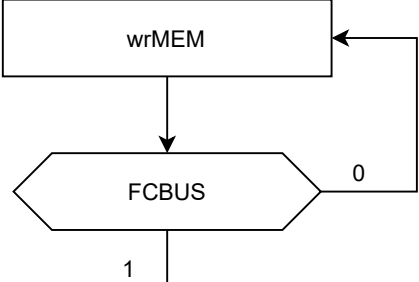
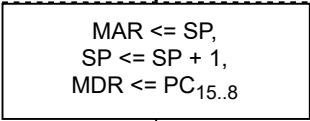
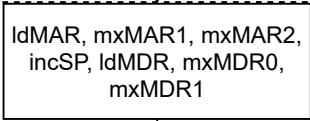


Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
		step00 br(if not!INTR then step00)
		step01 br(if not!PREKID then step16)
		step02 incSP
		step03 ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR2
		step04 wrMEM, br(if not!FCBUS then step04)
		step05 ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR0, mxMDR1

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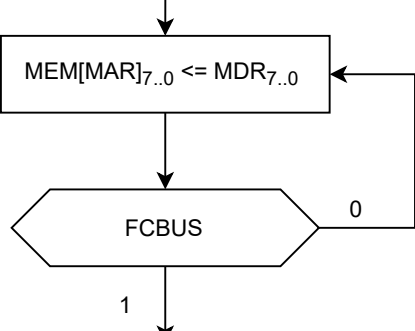
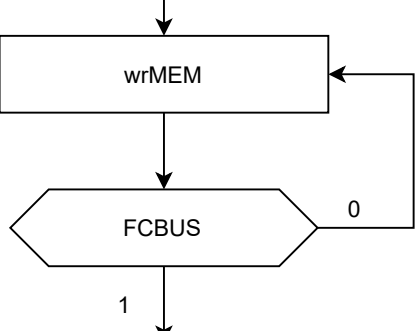
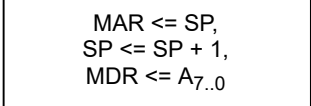
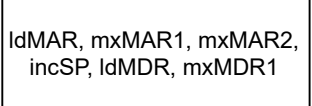
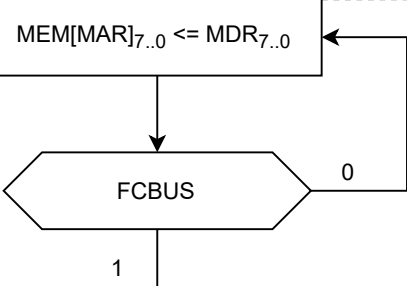
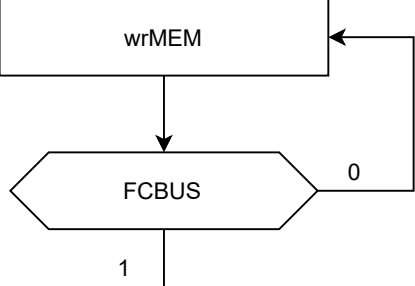
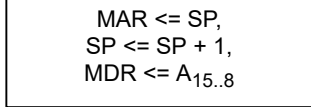
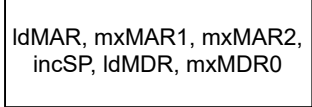
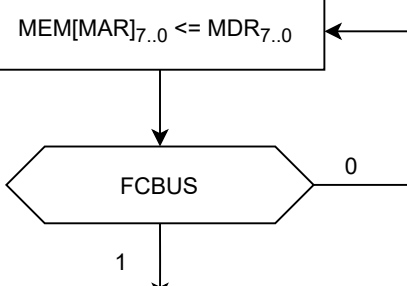
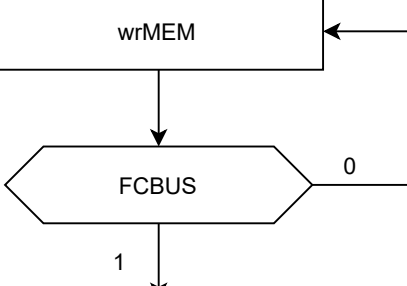
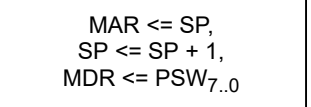
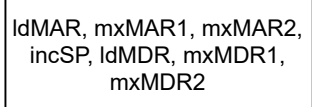
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Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
 <pre> graph TD Start(()) --> Step06[MEM[MAR]7..0 <= MDR7..0] Step06 --> FCBUS{FCBUS} FCBUS -- 0 --> Step06 FCBUS -- 1 --> Step07[MAR <= SP, SP <= SP + 1, MDR <= A7..0] </pre>	 <pre> graph TD Start(()) --> Step06[wrMEM] Step06 --> FCBUS{FCBUS} FCBUS -- 0 --> Step06 FCBUS -- 1 --> Step07[ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR1] </pre>	step06 wrMEM, br(if notFCBUS then step06)
 <pre> graph TD Step07[MAR <= SP, SP <= SP + 1, MDR <= A7..0] --> Step08[MEM[MAR]7..0 <= MDR7..0] </pre>	 <pre> graph TD Step07[ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR1] --> Step08[wrMEM] </pre>	step07 ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR1
 <pre> graph TD Step08[MEM[MAR]7..0 <= MDR7..0] --> FCBUS{FCBUS} FCBUS -- 0 --> Step08 FCBUS -- 1 --> Step09[MAR <= SP, SP <= SP + 1, MDR <= A15..8] </pre>	 <pre> graph TD Step08[wrMEM] --> FCBUS{FCBUS} FCBUS -- 0 --> Step08 FCBUS -- 1 --> Step09[ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR0] </pre>	step08 wrMEM, br(if notFCBUS then step08)
 <pre> graph TD Step09[MAR <= SP, SP <= SP + 1, MDR <= A15..8] --> Step0A[MEM[MAR]7..0 <= MDR7..0] </pre>	 <pre> graph TD Step09[ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR0] --> Step0A[wrMEM] </pre>	step09 ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR0
 <pre> graph TD Step0A[MEM[MAR]7..0 <= MDR7..0] --> FCBUS{FCBUS} FCBUS -- 0 --> Step0A FCBUS -- 1 --> Step0B[MAR <= SP, SP <= SP + 1, MDR <= PSW7..0] </pre>	 <pre> graph TD Step0A[wrMEM] --> FCBUS{FCBUS} FCBUS -- 0 --> Step0A FCBUS -- 1 --> Step0B[ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR1, mxMDR2] </pre>	step0A wrMEM, br(if notFCBUS then step0A)
 <pre> graph TD Step0B[MAR <= SP, SP <= SP + 1, MDR <= PSW7..0] --> End(()) </pre>	 <pre> graph TD Step0B[ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR1, mxMDR2] --> End(()) </pre>	step0B ldMAR, mxMAR1, mxMAR2, incSP, ldMDR, mxMDR1, mxMDR2

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Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
<pre> graph TD Start(()) --> Step0C[MEM[MAR]7..0 <= MDR7..0] Step0C --> FCBUS{FCBUS} FCBUS -- 0 --> Step0C FCBUS -- 1 --> Step0D[MAR <= SP, SP <= SP + 1, MDR <= PSW15..8] </pre>	<pre> graph TD Start(()) --> Step0C[wrMEM] Step0C --> FCBUS{FCBUS} FCBUS -- 0 --> Step0C FCBUS -- 1 --> Step0D[ldMAR, mxMAR1, mxMAR2, ldMDR, mxMDR0, mxMDR2] </pre>	step0C wrMEM, br(if notFCBUS then step0C)
<pre> graph TD Step0D[MAR <= SP, SP <= SP + 1, MDR <= PSW15..8] --> Step0E[MEM[MAR]7..0 <= MDR7..0] </pre>	<pre> graph TD Step0D[ldMAR, mxMAR1, mxMAR2, ldMDR, mxMDR0, mxMDR2] --> Step0E[wrMEM] </pre>	step0D ldMAR, mxMAR1, mxMAR2, ldMDR, mxMDR0, mxMDR2
<pre> graph TD Step0E[MEM[MAR]7..0 <= MDR7..0] --> FCBUS{FCBUS} FCBUS -- 0 --> Step0E FCBUS -- 1 --> Step0F[BRU2..0 <= UEXT2..0] </pre>	<pre> graph TD Step0E[wrMEM] --> FCBUS{FCBUS} FCBUS -- 0 --> Step0E FCBUS -- 1 --> Step0F[ldBR] </pre>	step0E wrMEM, br(if notFCBUS then step0E)
<pre> graph TD Step0F[BRU2..0 <= UEXT2..0] --> Step10[MAR15..0 <= IVTP15..0 + IVTDSP15..0] </pre>	<pre> graph TD Step0F[ldBR] --> Step10[ldMAR, mxMAR0, mxMAR1, mxMAR2] </pre>	step0F ldBR
<pre> graph TD Step10[MAR15..0 <= IVTP15..0 + IVTDSP15..0] --> Step11[MDR7..0 <= MEM[MAR]7..0] </pre>	<pre> graph TD Step10[ldMAR, mxMAR0, mxMAR1, mxMAR2] --> Step11[ldMDR, rdMEM] </pre>	step10 ldMAR, mxMAR0, mxMAR1, mxMAR2
<pre> graph TD Step11[MDR7..0 <= MEM[MAR]7..0] --> FCBUS{FCBUS} FCBUS -- 0 --> Step11 FCBUS -- 1 --> Step12[DWL <= MDR, MAR <= MAR + 1] </pre>	<pre> graph TD Step11[ldMDR, rdMEM] --> FCBUS{FCBUS} FCBUS -- 0 --> Step11 FCBUS -- 1 --> Step12[ldDWL, incMAR] </pre>	step11 ldMDR, rdMEM, br(if notFCBUS then step11)
<pre> graph TD Step12[DWL <= MDR, MAR <= MAR + 1] --> End(()) </pre>	<pre> graph TD Step12[ldDWL, incMAR] --> End(()) </pre>	step12 ldDWL, incMAR

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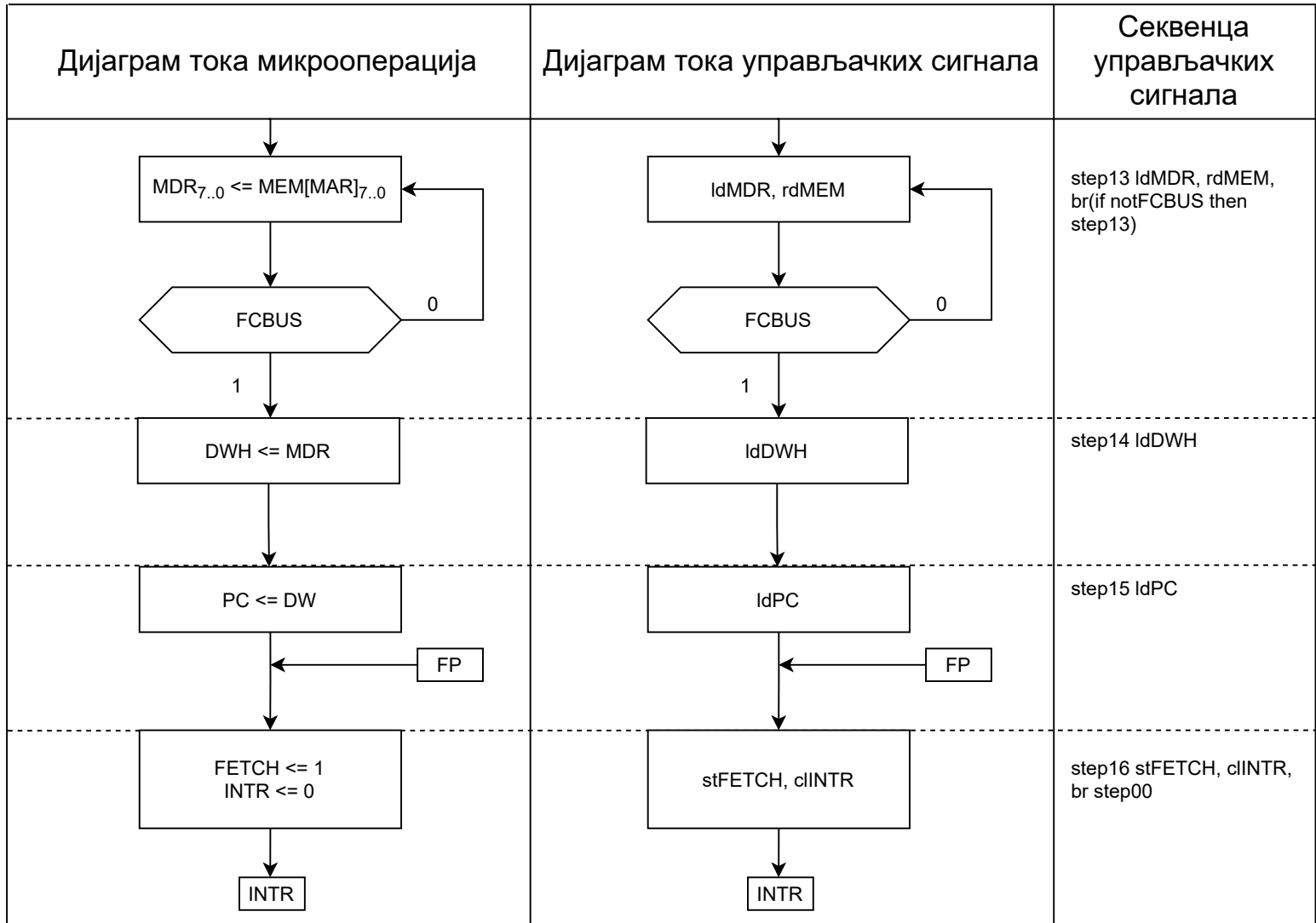
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