Alarm Clock

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Introduction

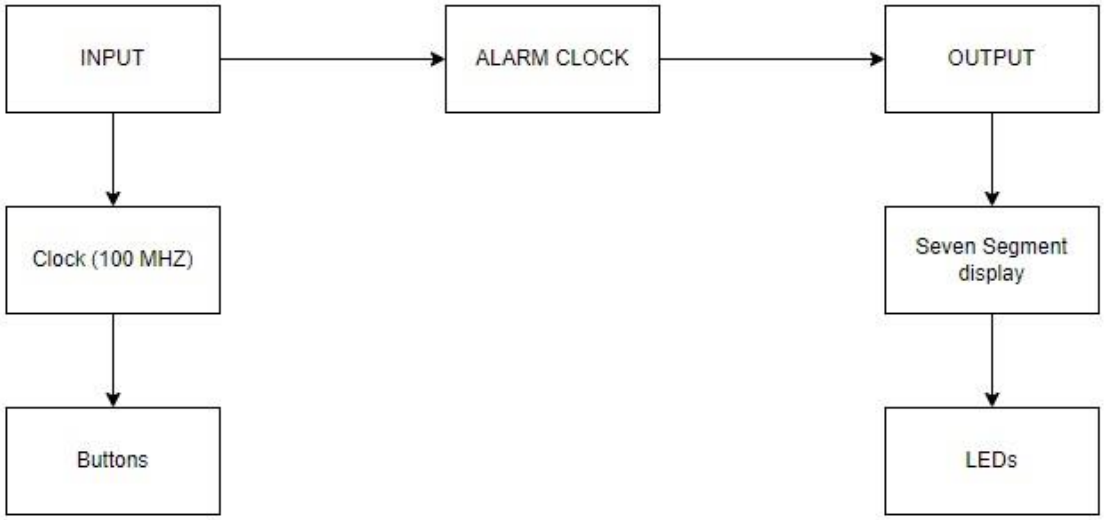
- Alarm clock

- **Implementation**
  - ModelSim VHDL implementation
  - FPGA Implementation Xilinx Vivado
  - Schematic and PCB Design using KiCAD

Concept Description

- 4 Segments for running clock
- 4 Segments for Alarm set clock
- Left, Right buttons to increase decrease alarm set time
- Up, Down buttons to increase decrease running clock time
- When running clock time reaches alarm set time, LEDs become HIGH

Block diagram

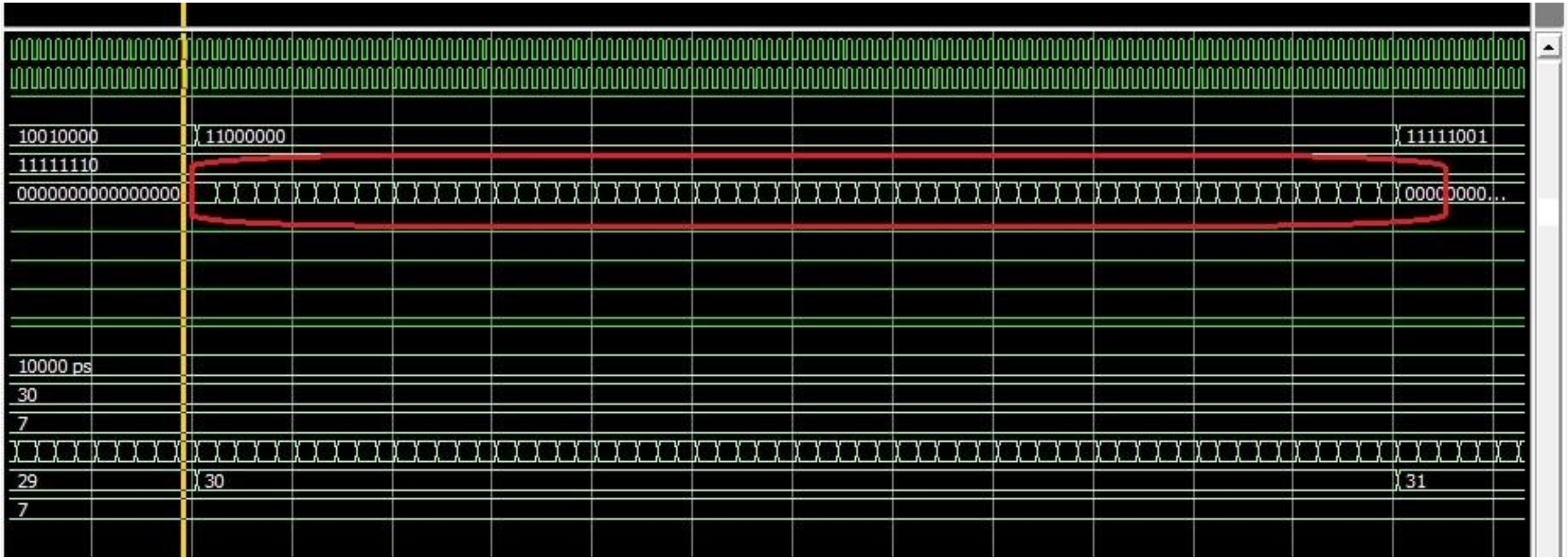


VHDL DESIGN

- Contains Seven_Segment, seg_decode, One_sec, Alarm_Time, Clock_Time components.
- Process flash_process is reponsible for checking alarm flashing LEDs
- Verified design using testbench

Testbench	The clock generation process generates a clock signal (clk_i) with a period specified by CLK_PERIOD. It alternates between '0' and '1' every half of the specified period.
	Initially, the reset signal (rstn_i) is set to '0' for a period of 10 clock cycles and then set to '1'
	The alarm is to 7:30.

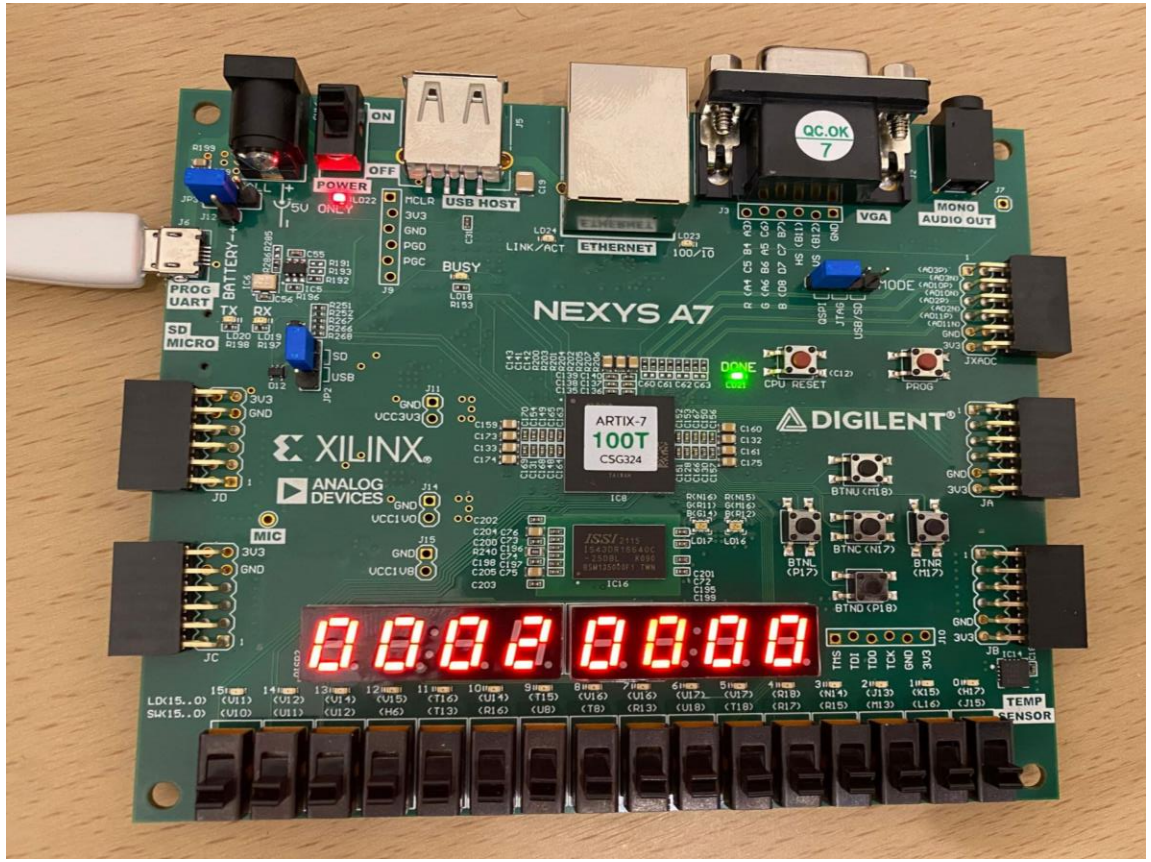
ModelSIM Simulation

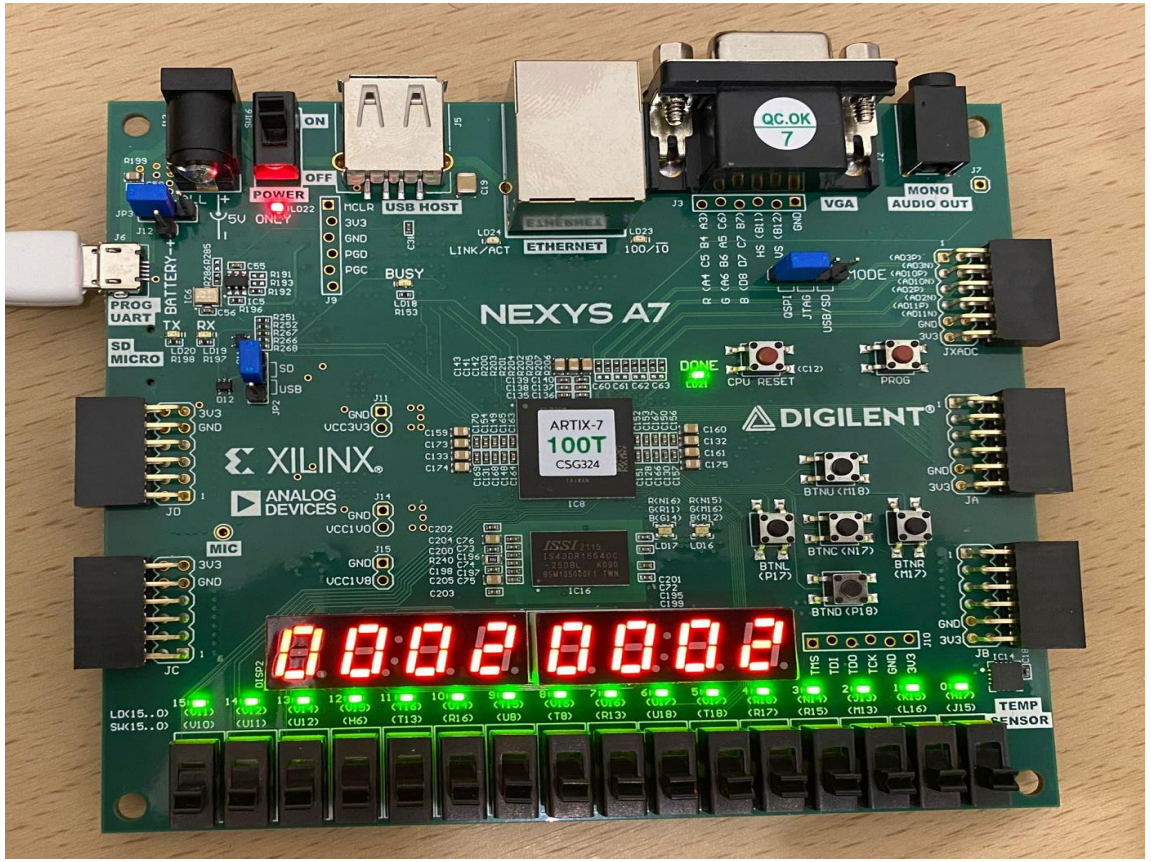


FPGA IMPLEMENTATION

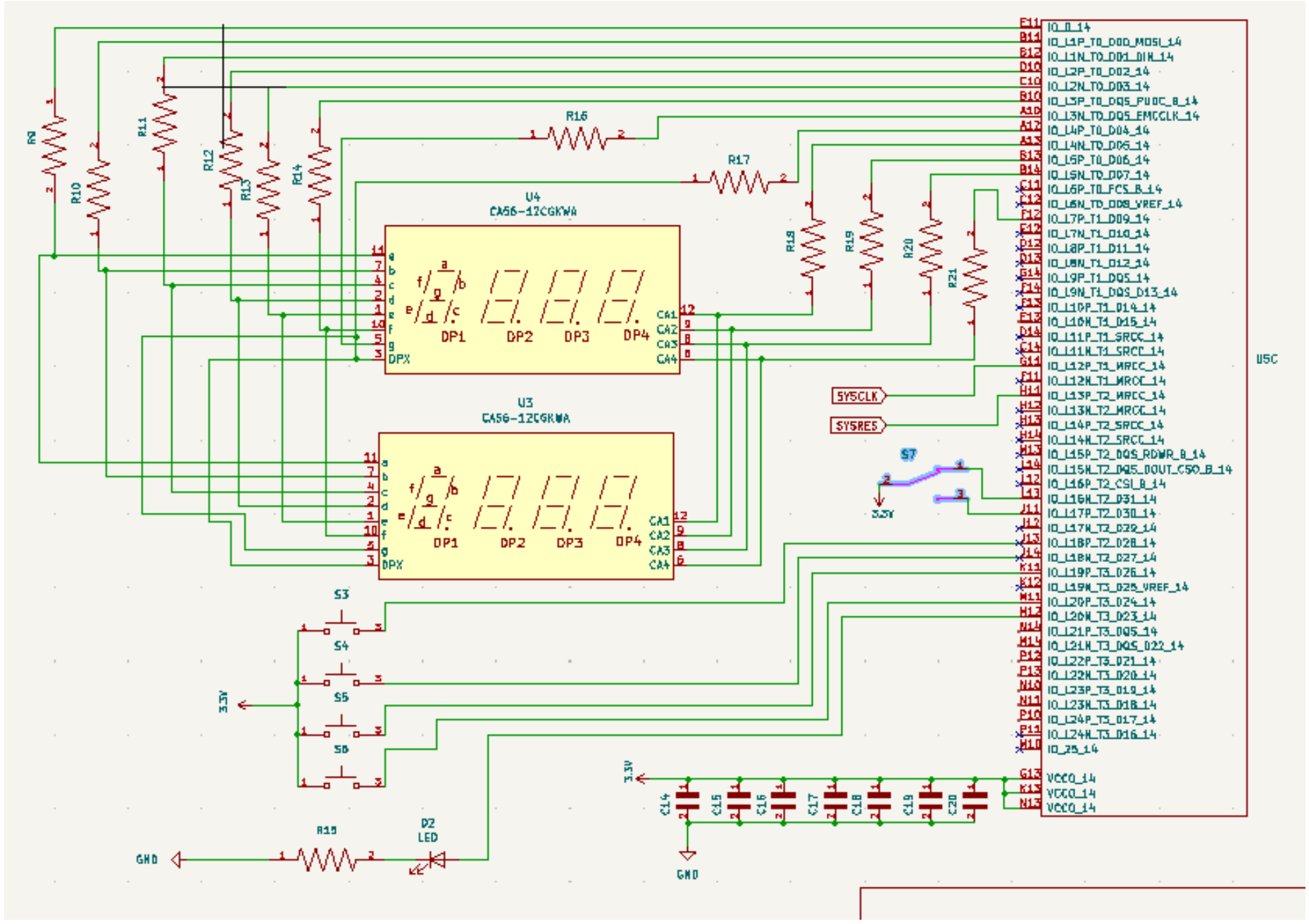
- **Temp_on_7seg** : responsible for driving a 7-segment display, controlling alarm and clock time, and flashing LEDs based on the alarm and clock settings
- **Seven_Segment** : provides the functionality to control a seven-segment display and display different values based on the input number vector and the timing provided by the clock signal.
- **One_Sec** : generates a pulse signal every second
- **Alarm_Time** : implements an alarm clock module that allows the adjustment of hours and minutes using control signals.
- **Clock_Time** : implements a clock module that allows the adjustment of hours and minutes using control signals.

FPGA IMPLEMENTATION RESULTS





PCB Schematic



PCB Layout