802.11 Wi-Fi Implementation Project

ASIC/FPGA Chip Design

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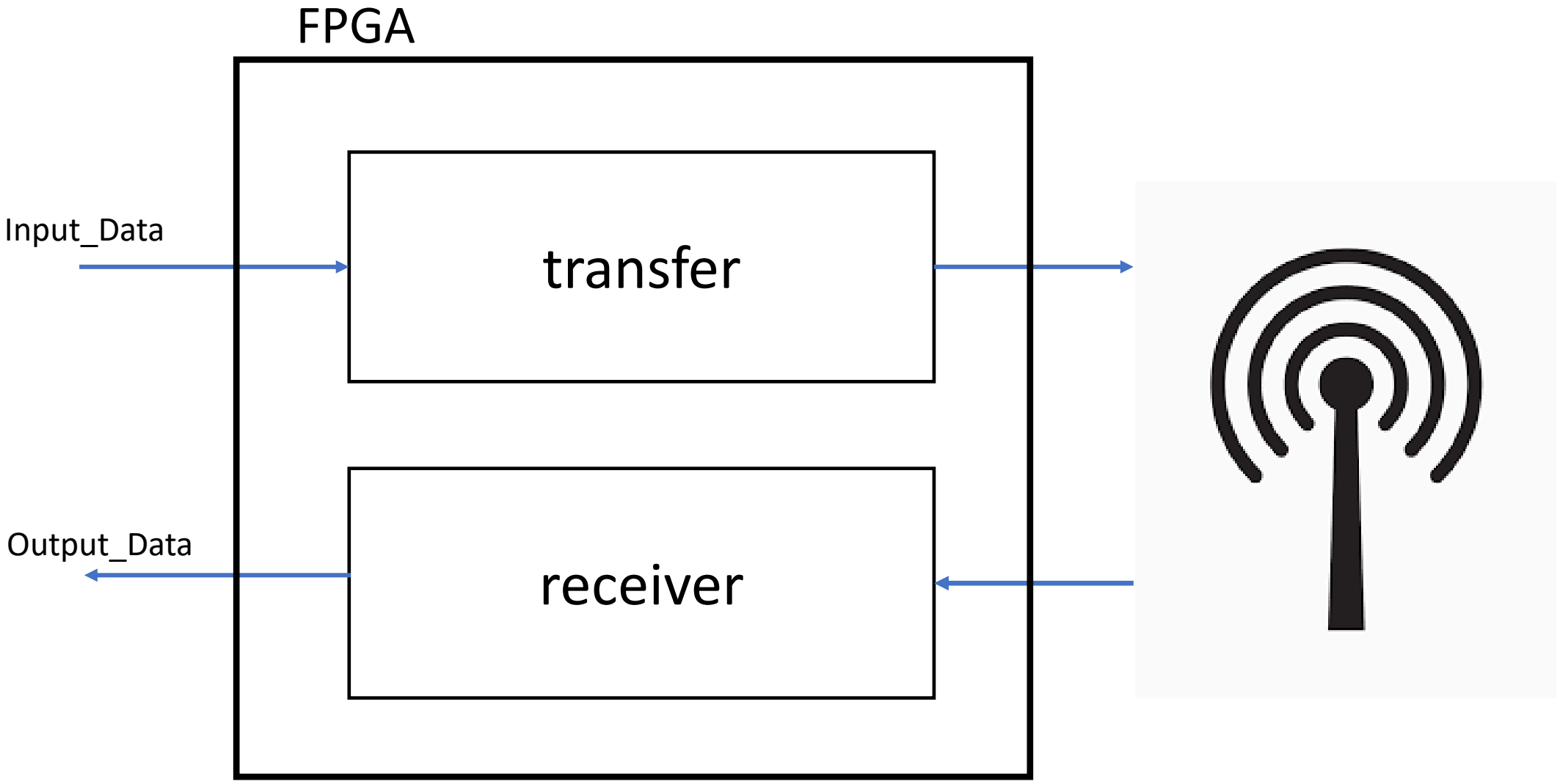
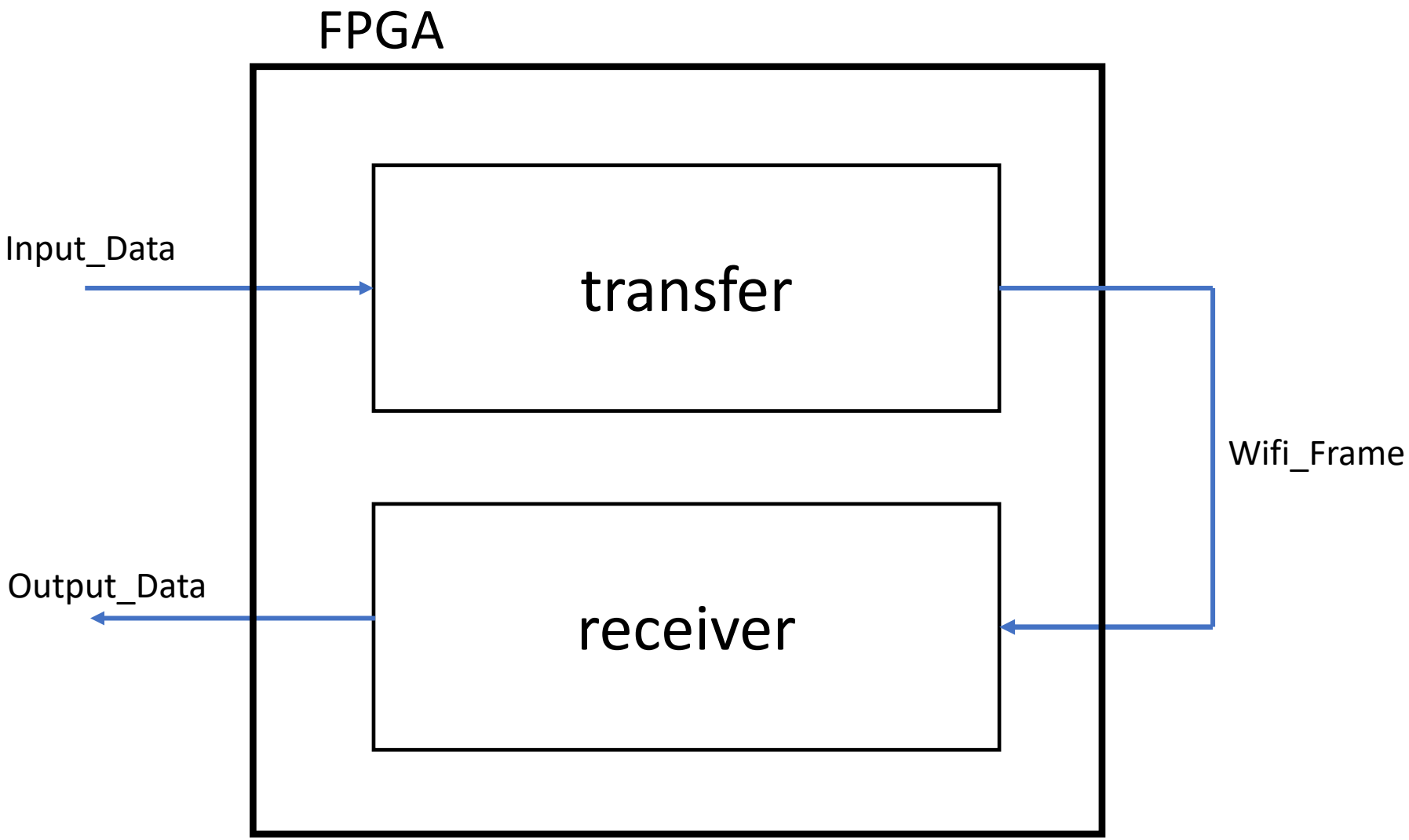

FPGA
Input_Data
transfer
Output_Data
receiver

What we want !



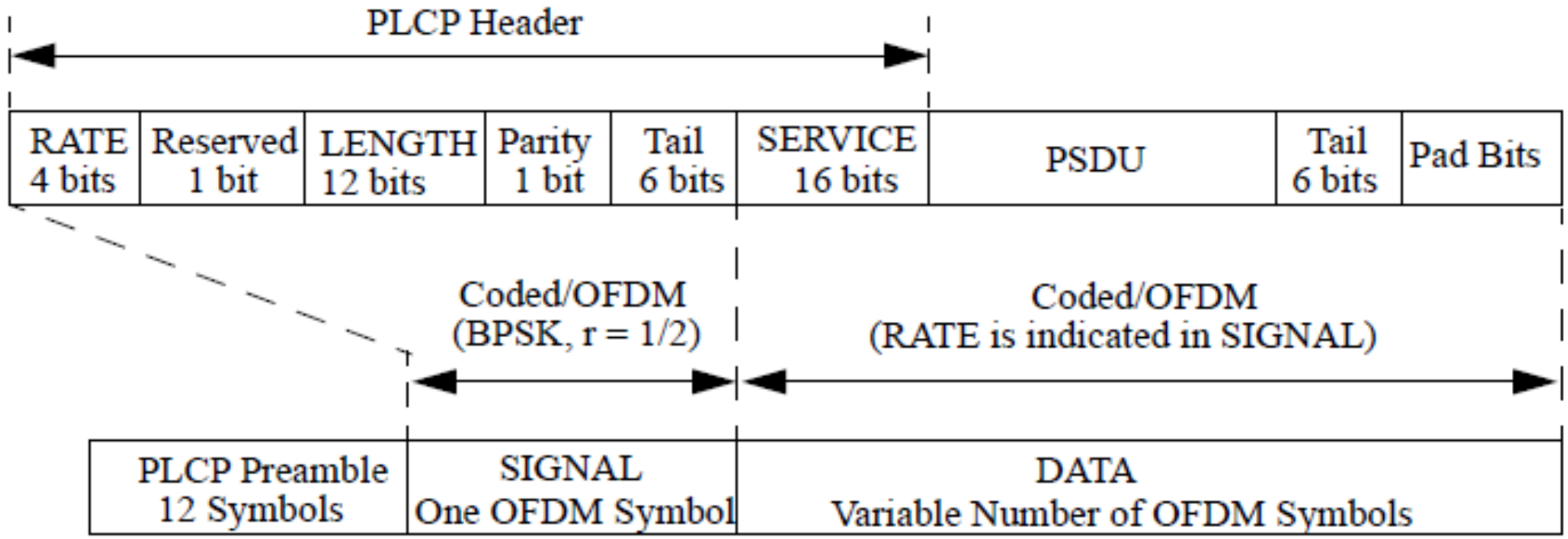
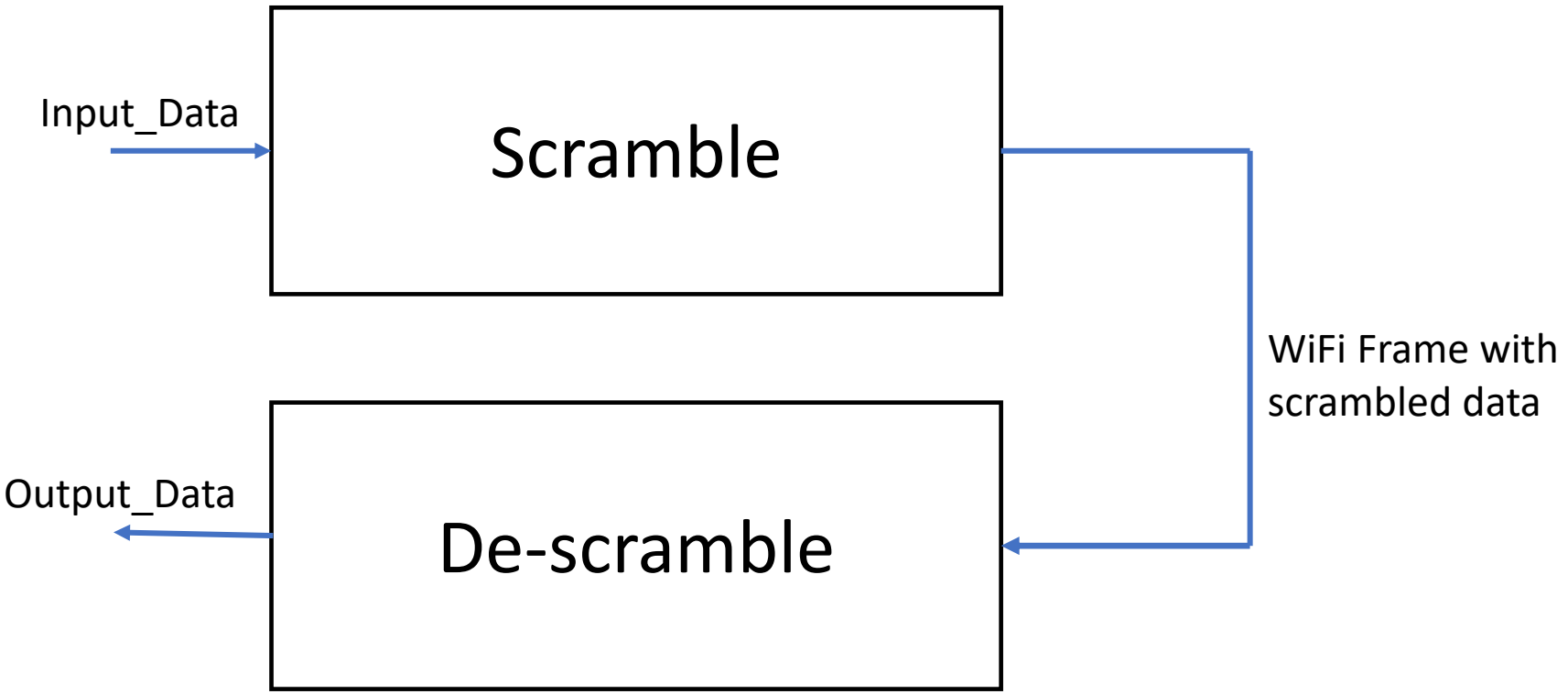


Figure 107—PPDU frame format

Read Page 7,8,9

Phase 1

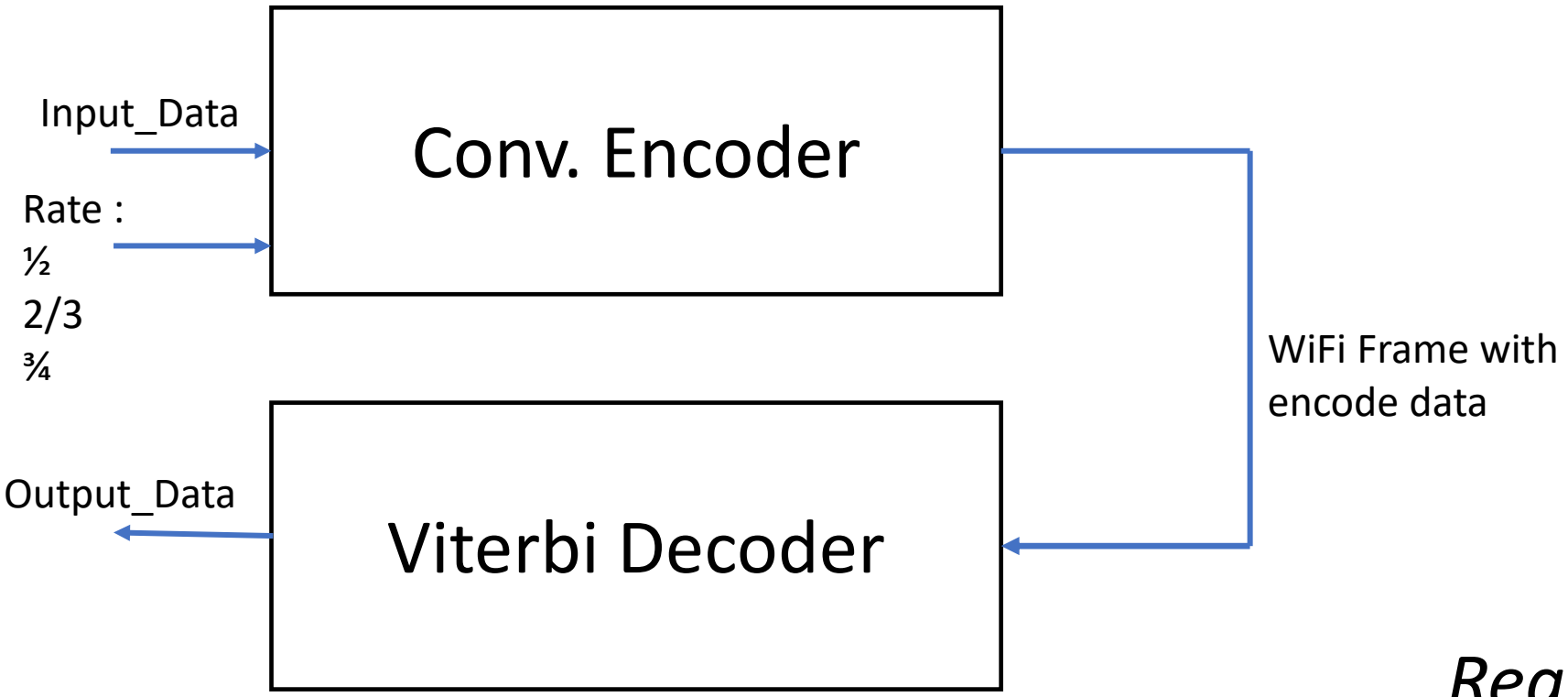
Matlab & Verilog Implementation and Verification



Read Page 16

Phase 2

Matlab & Verilog Implementation and Verification



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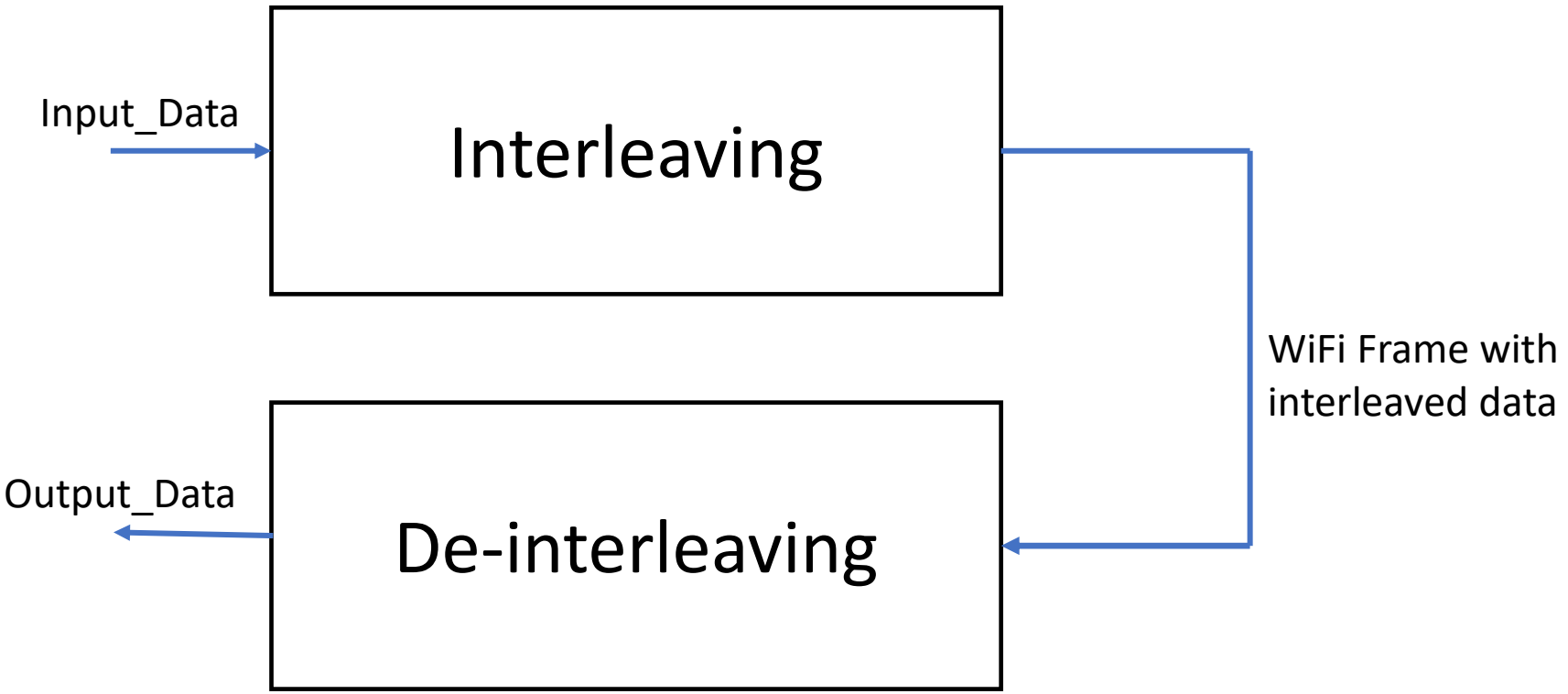
Phase 3

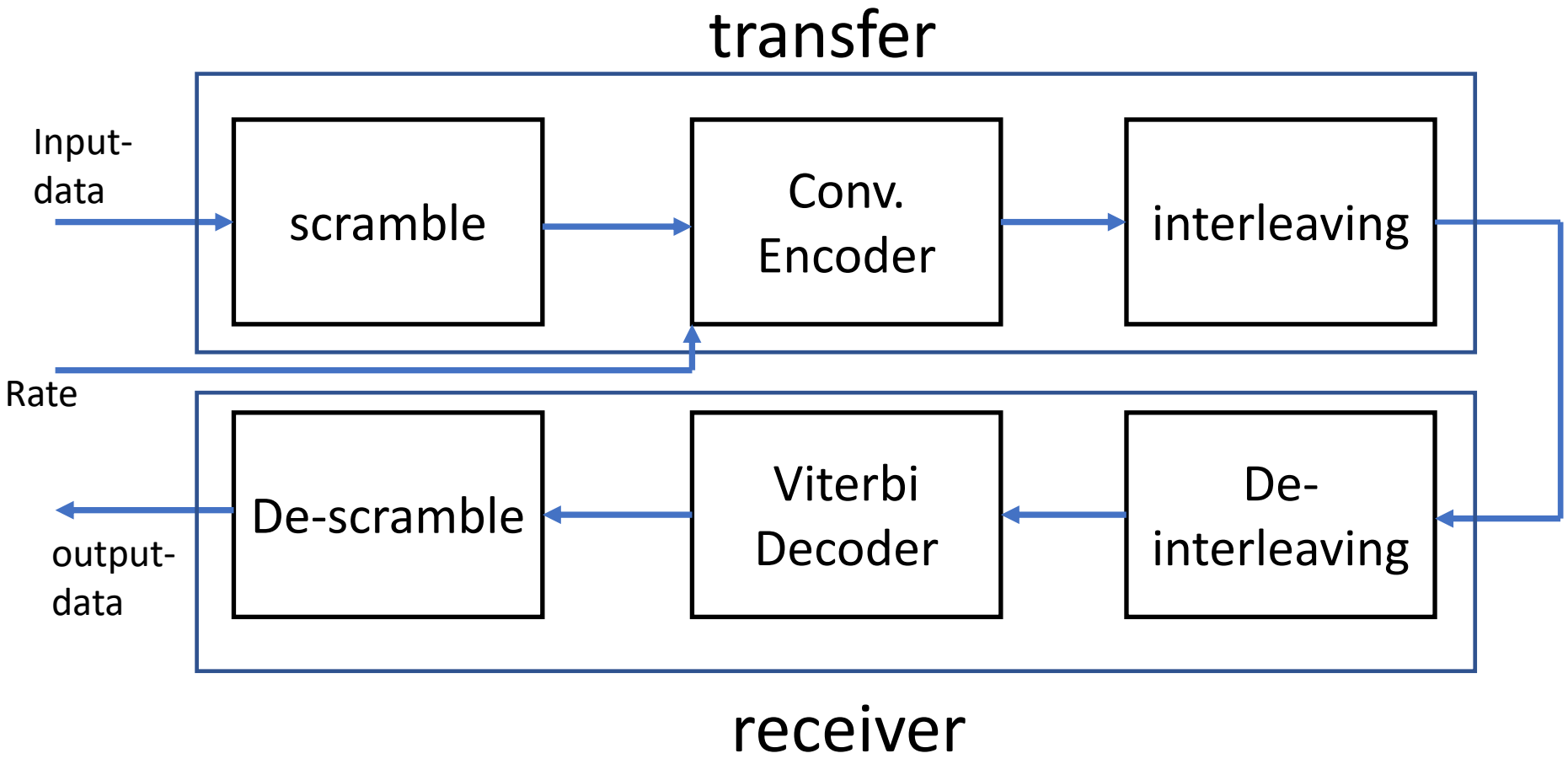
Matlab & Verilog Implementation and Verification



Read Page 17,19

Phase 4

- Check Matlab output of transfer with HDL output of transfer
- Check Input data with Output data
- Only 1 bit difference wont be accepted



How to deliver

- You should have a clean and understandable directories in your deliver files. Dirty folders and files wont be accepted.
- You should have also a report that should have :
  - Directory Description (likes ReadMe files)
  - Algorithms brief description
  - Simulation Results
- You should send a .zip file consists : your files , report