Phase 1

Fibonacci Sequence Number Identifier Circuit

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OVERVIEW

The project's core objective is to develop a digital circuit that calculates the nth term in the Fibonacci sequence, where the value of n is inputted in binary format. This circuit is designed to assist in computational tasks where quick retrieval of Fibonacci numbers is essential.

GOALS

A. General

1. **Professional Presentation:**

   The document is concise, clearly structured, and adheres to professional standards in presenting the project requirements.

2. **Timeliness:**

   The document is prepared and submitted as per the timeline provided.

3. **Grammar & Spelling:**

   The text is reviewed and ensured to be free of grammatical and spelling errors.

B. Content

1. **Background:**

   The project is tailored to create a circuit that, when provided with a binary input, calculates the corresponding number in the Fibonacci sequence.

2. **Inputs (a0 to a2):**

   The circuit will be designed to accept a 3-bit binary input (ranging from 0 to 7), representing the position in the Fibonacci sequence.

3. **Outputs (b0 to b3):**

   Four output lines, presenting the corresponding Fibonacci number in binary format.

4. **Error Conditions and Responses:**

   Specific error handling for inputs requesting Fibonacci terms outside the pre-defined range, resulting in an error output pattern.

5. **Eliminate Ambiguities:**

   A well-defined algorithm for calculating Fibonacci numbers ensures consistent and accurate outputs.

PROBLEM STATEMENT

The designed circuit aims to swiftly and accurately provide the nth Fibonacci number, corresponding to a 3-bit binary input, ensuring precision and consistency in outputs and error handling.

SPECIFICATIONS

Inputs:

a0 to a2: Three binary inputs capable of representing numbers from 0 to 7, indicating the position in the Fibonacci sequence.

Outputs:

b0 to b3: Four binary outputs showcasing the Fibonacci number corresponding to the provided input.

Error Conditions & Responses:

Specific error outputs for inputs that are not within the acceptable range or those that do not correspond to a Fibonacci term within the sequence's limit set for this circuit.

1. Out-of-Range Inputs:

Scenario: The circuit is designed to handle inputs corresponding to specific positions in the Fibonacci sequence. If an input represents a position beyond this limit, it should be treated as an error.

Error Response: A specific binary pattern, distinct from valid Fibonacci numbers, is outputted to signal this error.

2. Hardware Limitation:

Scenario: The circuit might have hardware limitations, like a maximum calculable Fibonacci number due to the bit width of the output or other hardware constraints.

Error Response: A unique error pattern in the output to indicate that the requested Fibonacci number exceeds the hardware's calculation capability.

3. Invalid Input Patterns:

Scenario: If the circuit receives an input pattern that doesn't correspond to any valid request (although this is mitigated by the 3-bit input width which inherently restricts the input to 0-7).

Error Response: The circuit could generate a unique error pattern distinct from valid outputs.

Ambiguous Cases:

1. Starting Index:

Alternative Interpretation: The sequence starts at the first term as 0 (0, 1, 1, 2, 3...).

Terms Generated: When input is ‘001’ (representing 1), output could potentially be ‘0000’ (representing 0 as the first term).

Standard to be Used: The project will adopt the convention that the sequence starts with the first term as 1 (1, 1, 2, 3...). Therefore, an input of ‘001’ will yield an output of ‘0001’, representing 1 as the first term.

2. Error Handling for Zero:

Alternative Interpretation: Input of ‘000’ could be treated as an error since there's no "zeroth" term in the sequence, or it could be assigned to a default value.

Output: The circuit could potentially yield an error signal or a default value, leading to an inconsistency in interpretation.

Standard to be Used: The project will treat an input of ‘000’ as an error, and a specific error output pattern will be generated. This ensures consistency and avoids the ambiguity of assigning a value to the "zeroth" term.

APPENDIX – TABLES/SUPPORTING DIAGRAMS

Appendix A:

Binary Input (a2 a1 a0)	Decimal Input	Fibonacci Sequence Number (Decimal)	Binary Output (b3 b2 b1 b0)
0	0	Error - Zeroth Term	0
1	1	1	1
10	2	1	1
11	3	2	10
100	4	3	11
101	5	5	101
110	6	8	1000
111	7	13	1101
1000	8	Error - Out of Range	1110
1001	9	Error - Out of Range	1110
1010	10	Error - Hardware Limitation	1111

CHECKLIST FOR SUBMISSION

- ☑ Professionally presented
- ☑ Properly identified
- ☑ Submitted on time
- ☑ Good grammar
- ☑ Correct spelling
- ☑ Sufficient background information
- ☑ Inputs are specified
- ☑ Outputs are specified
- ☑ Error conditions and responses specified
- ☑ Ambiguous possibilities eliminated