Peerzada Arsalan Masoodi

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Education

Shri Mata Vaishno Devi University — Katra, J&K
B.Tech. Electronics and Communication Engineering — *Nov 2022 – June 2026*

- **CGPA: 8.3 / 10**

Experience

Undergraduate Research Intern — June 2024 – July 2024
National Institute of Technology — *Srinagar, J&K*

- Assisted in semiconductor device research under Dr. Sheikh Amir Ahsan with focus on MOSFET physics and microelectronics.
- Analyzed I–V characteristics, small-signal models, and transient behavior using **LTspice**.
- Connected device-level insights to CMOS VLSI design, strengthening understanding of leakage control, threshold tuning, and layout implications.

Projects

TinyODIN-inspired SNN ASIC Flow | *QuestaSim, OpenSpike, OpenLane* — December 2025

- Designed and implemented an RTL-level LIF neuron module following the TinyODIN neuromorphic architecture.
- Verified neuron dynamics (leak, threshold crossing, spike generation, reset) using QuestaSim waveform analysis
- Integrated the neuron model into an open-source ASIC flow using OpenLane, targeting low-power neuromorphic inference.

Digital Soldering Station | *LTspice, KiCad, OnShape* — July 2025

- Designed and simulated a PID-based temperature control system to maintain stable soldering tip temperature.
- Implemented the complete system on a custom PCB using Arduino Nano and developed a 3D-modeled enclosure for the final product.

Ripple Carry Adder | *Cadence Virtuoso, Spectre, Linux* — April 2025

- Designed a transistor-level ripple carry adder in Cadence Virtuoso, verifying logic correctness.
- Implemented a full-custom GDSII layout applying duality mirror principles for optimized performance.

Audio Amplifier | *LTspice, KiCad* — November 2024

- Designed and simulated an audio amplifier in LTspice, analyzing gain frequency response, and output impedance.
- Implemented the design on a custom PCB in KiCad and validated performance by driving a speaker load.

Alarm Clock | *Proteus, Keil 5* — October 2024

- Built a simple digital alarm clock system using the 8085 microcontroller architecture.
- Programmed and deployed the firmware onto a microcontroller trainer kit for real-time functional testing.

Technical Skills

Languages: Python · C++ · C · MATLAB · LaTeX · HTML
HDL / Embedded: Verilog · Embedded C · Assembly
Tools: LTspice · Vivado · QuestaSim · Cadence Virtuoso · OpenLANE · Yosys · KiCad · EagleCAD · Proteus
NPTEL Certifications: Digital IC Design (Top 5%), Computer Networks and Internet Protocol (Top 5%), Computer Architecture and Organization, VLSI RTL to GDS (Top 5%)
Memberships: IEEE Computer Society · IEEE Solid-State Circuits Society

Leadership / Extracurricular

Tarang — December 2024 – Present
Core Member — *Shri Mata Vaishno Devi University*

- Co-managed technical events for the university technical fest EKATVA–2025, including organizing a boat race and designing circuits for a PCB design competition.

Vikalp — April 2023 – Present
Member — *Shri Mata Vaishno Devi University*

- Volunteered in a student-led initiative providing academic support to underprivileged children from nearby communities.