R. Bharanish

DIGITAL LOGIC DESIGN PRACTICAL

(SUBJECT CODE 1052233320)

(For III Semester Computer Engineering)

(As per Regulation 2023)

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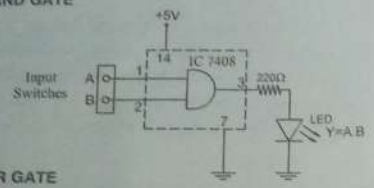
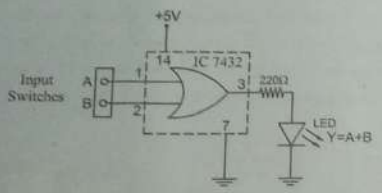
LOGIC DIAGRAM

a) AND GATE



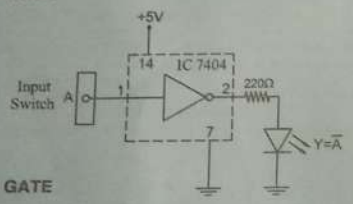
INPUT		OUTPUT
A	B	Y = A . B
LOW	LOW	
LOW	HIGH	
HIGH	LOW	
HIGH	HIGH	

B) OR GATE



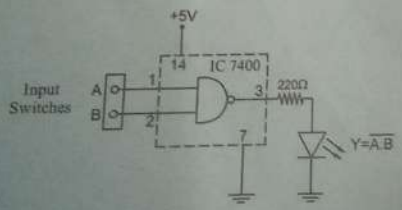
INPUT		OUTPUT
A	B	Y = A + B
LOW	LOW	
LOW	HIGH	
HIGH	LOW	
HIGH	HIGH	

C) NOT GATE



INPUT	OUTPUT
A	Y = $\overline{A}$
LOW	
HIGH	

D) NAND GATE



INPUT		OUTPUT
A	B	Y = $\overline{A . B}$
LOW	LOW	
LOW	HIGH	
HIGH	LOW	
HIGH	HIGH	

LOGIC GATES

Ex. No. : 1

Date :

Aim :

To verify the truth tables of AND, OR, NOT, NAND, NOR and Ex-OR gates by using 74XX ICs.

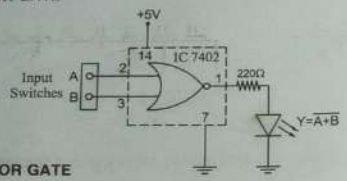
Apparatus required

S.No.	Description	Range	Quantity
1	AND gate	IC 7408	1
2	OR gate	IC 7432	1
3	NOT gate	IC 7404	1
4	NAND gate	IC 7400	1
5	NOR gate	IC 7402	1
6	Ex-OR gate	IC 7486	1
7	IC trainer board	Digital	1
8	Connecting Wires	-	-

Theory

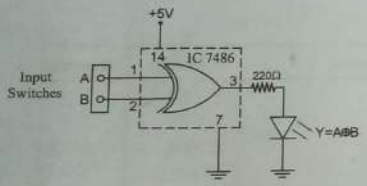
Gate is a logic circuit, with one or more inputs and only one output. The output occurs only for a well defined condition of its inputs. The A and B inputs produce the output of AND gate as A.B, the output of OR gate as A + B, the output of NOT gate as $\overline{A}$, the output of NAND gates as $\overline{A . B}$, the output of NOR gate as $\overline{A + B}$ and the output of EX-OR gate as $A \oplus B$. In the AND gate, the output is high only when all the inputs are in high level, otherwise its output is in low level. The NAND gate is the complement of AND gate. In the OR gate the output is high only when minimum any one of the input is in high level, otherwise its output is low. The NOR gate is the complement of OR gate. In a two input Ex-OR gate the output is high when both inputs are different. Conversely the output is low when both inputs are identical. A NOT gate simply invert its input.

E) NOR GATE



INPUT		OUTPUT
A	B	$Y = \overline{A + B}$
LOW	LOW	
LOW	HIGH	
HIGH	LOW	
HIGH	HIGH	

F) EX-OR GATE



INPUT		OUTPUT
A	B	$Y = A \oplus B$
LOW	LOW	
LOW	HIGH	
HIGH	LOW	
HIGH	HIGH	

TRUTH TABLES

AND gate

INPUT		OUTPUT
A	B	Y = A . B
0	0	0
0	1	0
1	0	0
1	1	1

OR gate

INPUT		OUTPUT
A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

NOT gate

INPUT	OUTPUT
A	$Y = \overline{A}$
0	1
1	0

NAND gate

INPUT		OUTPUT
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

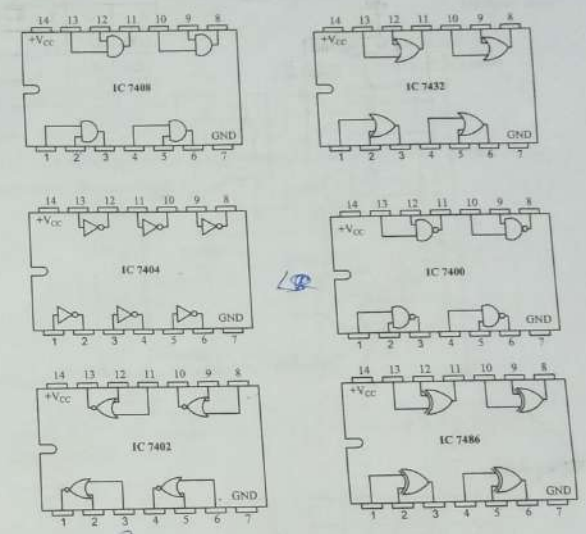
NOR gate

INPUT		OUTPUT
A	B	$Y = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

EX-OR gate

INPUT		OUTPUT
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAMS



Procedure

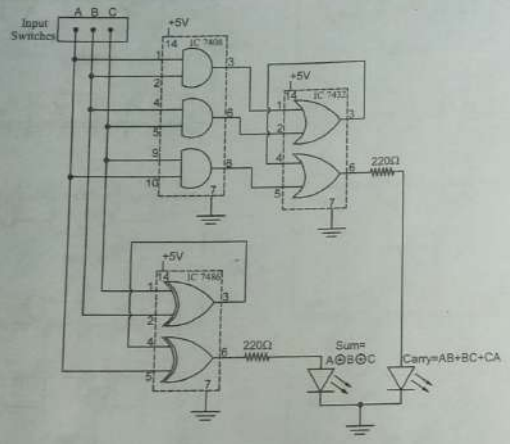
1. Make the connections as per the logic diagram.
2. Switch ON the IC trainer board.
3. Apply the combinations of input one by one as specified in the truth table.
4. Note its output level.
5. Repeat the above procedures for all mentioned gates.
6. Switch OFF the IC trainer board.
7. Disconnect the components.

Result

The truth tables of AND, OR, NOT, NAND, NOR and EX-OR gates are verified by using 74XX ICs.

FULL ADDER

Logic diagram



Tabular column

INPUTS			OUTPUT	
A	B	C	Sum	Carry
LOW	LOW	LOW		
LOW	LOW	HIGH		
LOW	HIGH	LOW		
LOW	HIGH	HIGH		
HIGH	LOW	LOW		
HIGH	LOW	HIGH		
HIGH	HIGH	LOW		
HIGH	HIGH	HIGH		

FULL ADDER

Ex. No. : 2

Date :

Aim :

To construct and test the performance full adder by using logic gates.

Apparatus Required :

S.No.	Description	Range	Quantity
1.	IC trainer Kit	Digital	1
2.	ICs	7408, 7486, 7432	each 1 No
3.	Connecting wires	-	-

Theory

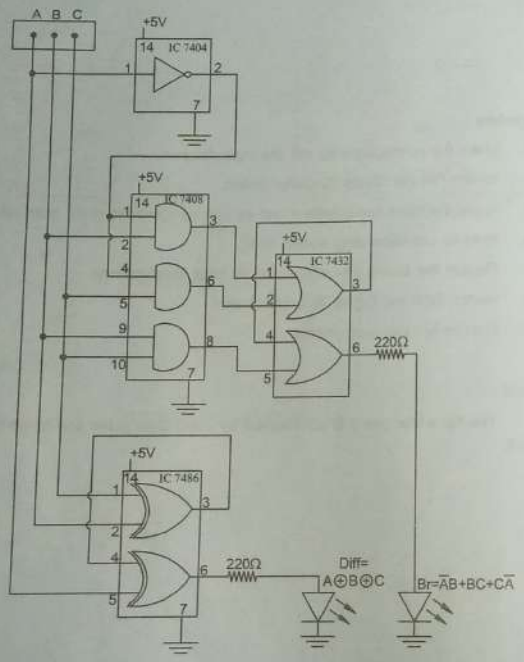
Full adder is a logic circuit used for adding three single bit binary numbers. The A, B and C of the three inputs, produce the output as, Sum = A ⊕ B ⊕ C, and Carry = AB + BC + CA.

Truth table

INPUT			OUTPUT	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

Logic diagram



FULL SUBTRACTOR

Ex. No. : 3

Date :

Aim :

To construct and test the performance of full subtractor by using logic gates.

Apparatus Required :

S.no.	Description	Range	Quantity
1.	IC trainer Kit	Digital	1
2.	ICs	7404, 7486, 7432, 7408	each 1 No
3.	Connecting wires	-	-

Theory :

Full subtractor is used for performing 3 bit binary subtraction. The A, B and C inputs produce the output as Diff = A ⊕ B ⊕ C and Br = $\bar{A}$C + $\bar{A}$B + BC.

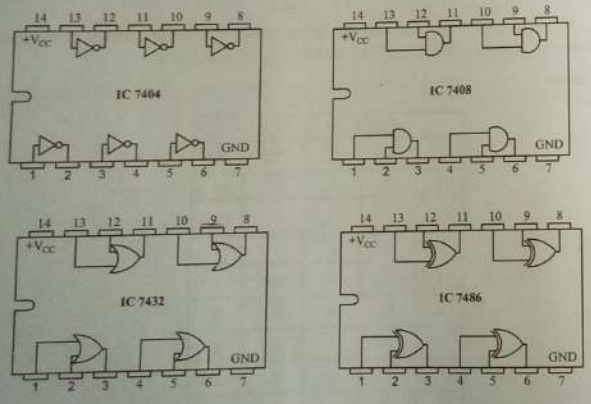
Truth table

INPUT			OUTPUT	
A	B	C	Diff	Br
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Tabular column

INPUT			OUTPUT	
A	B	C	Diff	Br
LOW	LOW	LOW		
LOW	LOW	HIGH		
LOW	HIGH	LOW		
LOW	HIGH	HIGH		
HIGH	LOW	LOW		
HIGH	LOW	HIGH		
HIGH	HIGH	LOW		
HIGH	HIGH	HIGH		

IC Pin diagrams



Procedure :

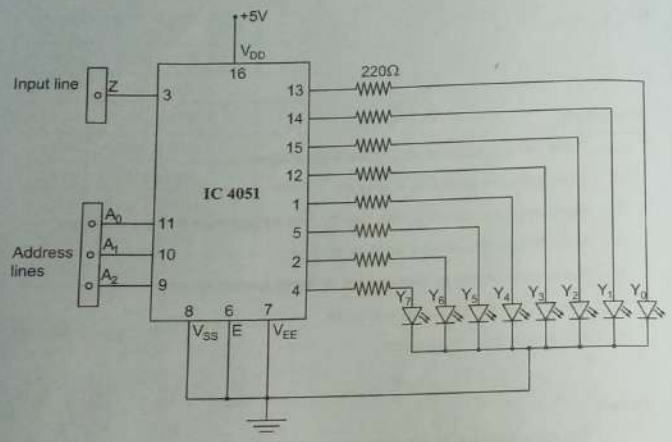
1. Make the connections as per the logic diagram.
2. Switch ON the Digital IC trainer kit.
3. Apply the input combinations one by one as specified in the truth table.
4. Note its corresponding output level.
5. Repeat the above procedures for all input combinations
6. Switch OFF the Digital IC trainer kit.
7. Disconnect the components.

Result :

The full subtractor circuit is constructed by using logic gates and its performance is also tested.

DE-MULTIPLEXER

Logic diagram



DE-MULTIPLEXER

Ex. No. : 4

Date :

Aim :

To construct and validate the truth table of de-multiplexer.

Apparatus Required :

S.No.	Description	Range	Quantity
1.	IC trainer kit	Digital	1
2.	IC (MUX/DEMUX)	4051	1
3.	Connecting wires	-	-

Theory :

IC 4051 is a 1 of 8 multiplexer / 1 to 8 Demultiplexer. In Demultiplexer operation, among the 8 output lines, any one output is selected according to the address applied to its address input lines. The input is transferred to that output line.

In multiplexer operation among the 8 input lines, any one input is transferred to its output, depends upon the address applied to its address input lines.

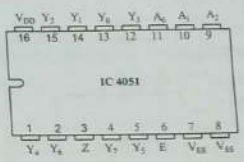
Truth Table

Address input			Enabled output
A_2	A_1	A_0	
0	0	0	Y_0
0	0	1	Y_1
0	1	0	Y_2
0	1	1	Y_3
1	0	0	Y_4
1	0	1	Y_5
1	1	0	Y_6
1	1	1	Y_7

Tabular column

Input D	Address input			Output							
	A_2	A_1	A_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
	0	0	0	0	0	0	0	0	0	0	
	0	0	1	0	0	0	0	0	0		0
	0	1	0	0	0	0	0	0		0	0
	0	1	1	0	0	0	0		0	0	0
	1	0	0	0	0	0		0	0	0	0
	1	0	1	0	0		0	0	0	0	0
	1	1	0	0		0	0	0	0	0	0
	1	1	1		0	0	0	0	0	0	0

Pin diagram



Procedure :

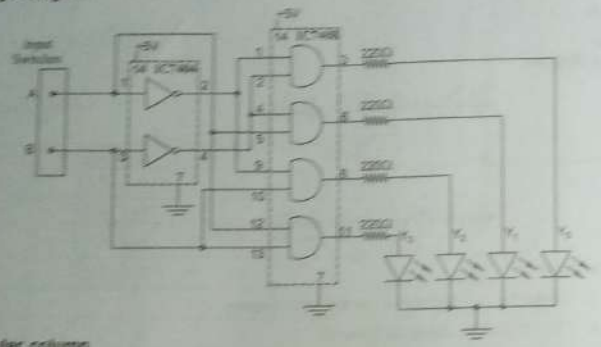
1. Make the connections as per the logic diagram.
2. Switch ON the Digital IC trainer Kit.
3. Apply the combinations of input one by one as specified in the truth table.
4. Note its corresponding output readings.
5. Switch OFF the Digital IC trainer Kit.
6. Disconnect the components.

Result :

The circuit of demultiplexer is constructed and its truth table is validated.

DECODER (2 TO 4 (OR) 1 OF 4 DECODER)

Logic diagram



Tabular column

INPUT		OUTPUT			
B	A	Y_3	Y_2	Y_1	Y_0
LOW	LOW				
LOW	HIGH				
HIGH	LOW				
HIGH	HIGH				

DECODER

Ex. No. : 5

Date :

Aim :

To construct and validate the performance of decoder circuit.

Apparatus Required :

S.No	Description	Range	Quantity
1.	IC trainer Kit	Digital	1
2.	ICs	7408, 7432 7404	each 1 No
3.	Connecting wires	-	-

Theory :

In Decoders, the number of output lines is more than the number of input lines. Among the output lines, any one of the output lines is selected at a time in accordance with the address applied to the input lines. In encoders the number of output lines is less than the number of input lines. An encoder converts an active input signal into a coded output signal.

Truth table

INPUT		OUTPUT			
B	A	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0