Documentation

Pi-Sense

26-05-2023

Important Notes:

- ***The descriptions in italics in this document (except for some section headings) are exemplary and explanatory and must be removed from the completed report.***
- ***Identify which section of this report was created by which team member***
- ***Your documentation should have ca. 8 pages (content! Without cover sheet, references, appendix etc.).***

1 Team members

1. Arsany Girgis
2. Emirkan Sali
3. Lochana Abhayawardana

2 Introduction

Introduction into your project
Why are FPGAs and VHDL important for your project domain?

3 Concept description

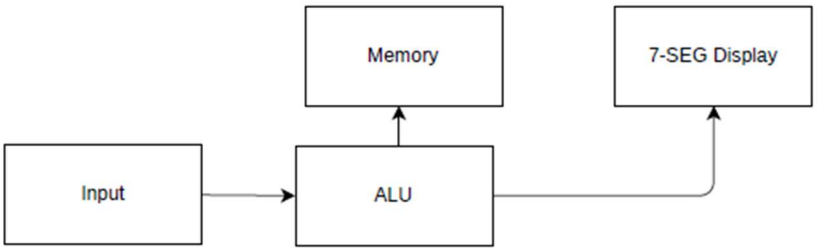

Figure 1

The concept of a 4-bit calculator on an FPGA (Field-Programmable Gate Array) involves designing and implementing a digital circuit that performs basic arithmetic operations on 4-bit binary numbers. The FPGA serves as a programmable hardware platform that allows us to create and configure custom digital circuits to perform specific functions.

- *Designing the Calculator:*

The calculator design starts with defining the input and output requirements. In this case, the inputs are two 4-bit binary numbers (a and b), an operation select signal (op), and the outputs are the result (result), carry-out (carry_out), and overflow (overflow) signals.
The desired operations (addition, subtraction, multiplication, and division) are implemented using appropriate arithmetic and logical circuits within the FPGA design.

- *VHDL Implementation:*

The calculator's functionality is described using a hardware description language like VHDL or Verilog.
The operations are typically implemented using standard arithmetic and logical operators provided by the language, such as addition (+), subtraction (-), multiplication (*), division (/), and remainder (rem).
Additional logic is implemented to handle special cases, such as division by zero.

- *Synthesis and Place & Route:*

Once the VHDL/Verilog code is written, it is synthesized using a synthesis tool that converts the code into a gate-level representation.
The synthesized design is then subjected to a place and route (P&R) process, where the FPGA resources (logic elements, flip-flops, interconnects, etc.) are allocated and connected to implement the desired functionality.

4 Project/Team management

We used agile as a project method where we had weekly sprints
All members participated in all tasks.