EE2026: DIGITAL DESIGN

Academic Year 2022-2023, Semester 2

LAB 2: Combinational Circuits in Verilog

OVERVIEW:

A combinational circuit is one where the outputs depend only on the current inputs. In this lab, we will be designing some combinational circuits that are able to perform addition.

The pre-requisite for this lab requires one to be able to:

- Create a Verilog project and design source in Vivado.
- Create a testbench to simulate the design source.
- Generate the RTL schematic and the synthesised circuit schematic of design source.
- Map and implement a design on the Basys 3 development board.
- Understand well the contents of Lectures 1, 2, and especially 3: Introduction to Verilog.

This lab will cover the following:

- Designing a one-bit full adder circuit using the dataflow modelling method.
- Designing a two-bit parallel adder circuit using the structural modelling method.

Tasks for this lab include:

- Designing the Verilog code of a one-bit full adder.
- Designing, simulating and implementing a four-bit parallel adder on the FPGA.
- Understanding a 1-bit two-to-one multiplexer.

GRADED ASSIGNMENT [CANVAS SUBMISSION: SUNDAY 5th FEBRUARY 2023, 10:00 P.M.]:

Further details are available at the end of this lab manual

ONE-BIT-FULL ADDER:

Consider the binary addition shown in ***Figure 2.1***. To design a circuit that would perform the addition of two one-bit values, the circuit would need to have three input bits and two output bits.

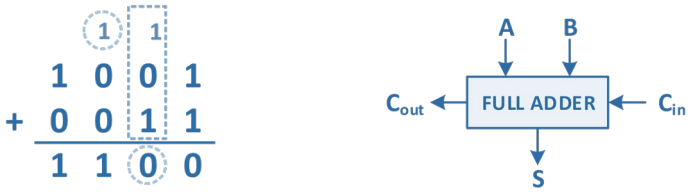


Figure 2.1: *Binary Addition and functional block diagram of the one-bit full adder*

Such a circuit is called a one-bit full adder. It adds two bits (**A**, **B**) and the carry ($\mathbf{C_{in}}$) from a previous stage of addition, and produces a sum (**S**) and a carry ($\mathbf{C_{out}}$), as illustrated through a truth table in ***Figure 2.2***. By simplifying the truth table, the Boolean expressions for **S** and $\mathbf{C_{out}}$ can be obtained.

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + C_{in}\,(A \oplus B)$$

Figure 2.2: *Truth table and boolean expressions of the one-bit full adder*

Note: A half adder, in contrast to a full adder, does not involve a carry input. Thus, for a half adder, $S = A \oplus B$, *and* $C_{out} = AB$

UNDERSTANDING | TASK 1

Using the dataflow method, complete the Verilog code for the one-bit full adder. Verify that the RTL schematic is as shown.

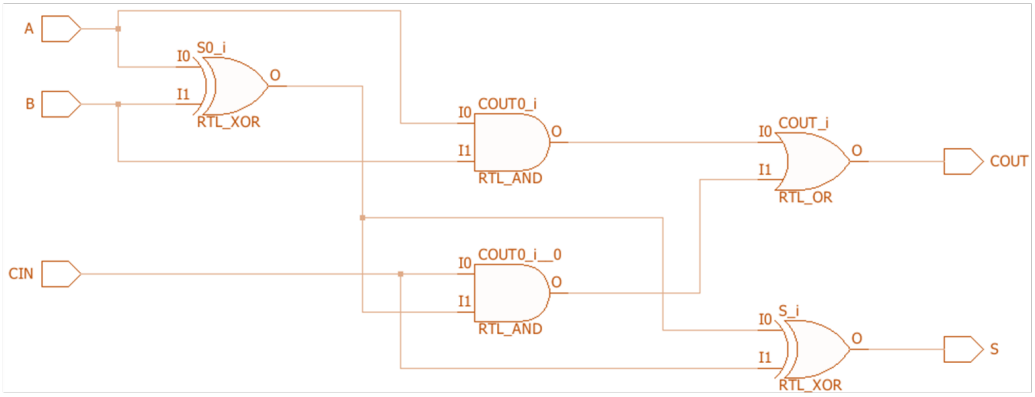
Verilog skeleton code for the one-bit-full adder:

```
module my_full_adder(input A, B, CIN, output S, COUT);

    assign S =
    assign COUT =

endmodule
```

RTL schematic for the one-bit full adder:



TWO-BIT FULL ADDER:

By cascading one-bit full adder blocks, the one-bit adder can be reused and parallel adders that add multiple bits can be created through the structural modelling method. A two-bit ripple-carry adder is illustrated in ***Figure 2.3***.

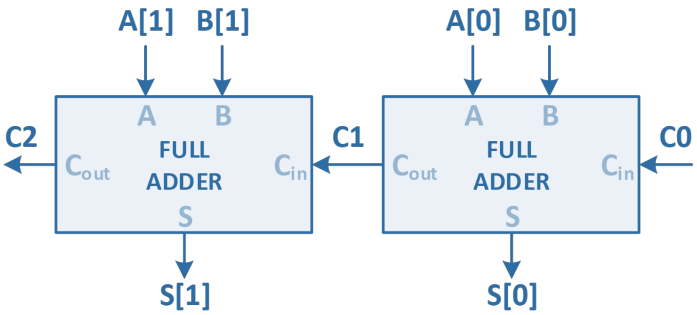


Figure 2.3: *Functional block diagram of the two-bit ripple-carry adder*

With the code for a one-bit full adder, a new module is created and two full adder blocks (fa0, fa1) are instantiated. By specifying the inputs and outputs to these blocks, the connection **C1** between them is made. Note that the order of signals during instantiation should respect the order in which they were declared in the one-bit full adder module **my_full_adder**.

This approach to hardware description is called structural modelling, whereby a more abstract module (for example, **my_2_bit_adder**) is built from simpler components describing gate-level hardware (such as **my_full_adder**).

Verilog code for two-bit ripple-carry adder, using structural modelling:

```
module my_2_bit_adder(input [1:0] A, input [1:0] B, input C0,
                      output [1:0] S, output C2);

    wire C1;

    my_full_adder fa0 (A[0], B[0], C0, S[0], C1);
    my_full_adder fa1 (A[1], B[1], C1, S[1], C2);

endmodule
```

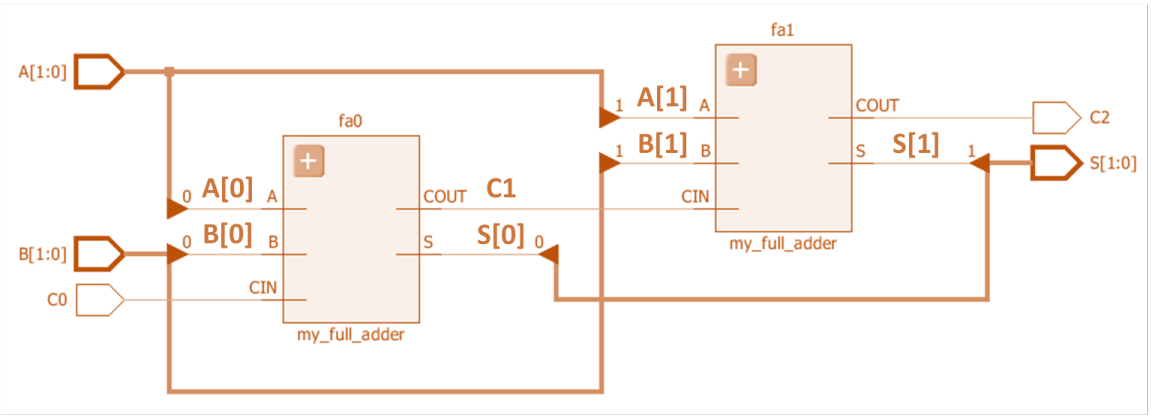
[Note] Two-bit port declaration for A, B, S:

Instead of having multiple input and output ports (A1, A0, B1, B0, S1, S0), multi-bit vector ports are defined.

Example: `input [5:0] apple`

Input port name is **apple**, with size of 6 bits. apple[5] refers to the MSB, apple[0] refers to the LSB.

RTL schematic for the two-bit ripple-carry adder:



FOUR-BIT FULL ADDER:

The functional block diagram of a four-bit ripple-carry adder is shown in ***Figure 2.4***.

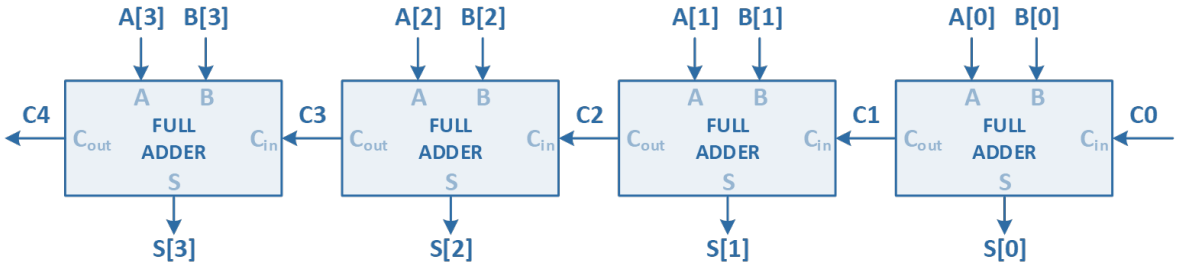


Figure 2.4: *Functional block diagram of a four-bit ripple-carry adder*

UNDERSTANDING | TASK 2

Start by adding a new design source for the four-bit full adder.

1. By using the structural modelling method, design a four-bit ripple-carry adder.
2. Generate the RTL schematic and check that connections between the blocks are correct.
3. Simulate your code with the following three sets of input values, and check that the simulation outputs are correct:

A:		0	0	1	1	A:		1	0	1	1	A:		1	1	1	1
B:	+	0	0	1	1	B:	+	0	1	1	1	B:	+	1	1	1	1
		□	□	□	□			□	□	□	□			□	□	□	□

[Note] Brief guidelines for multi-bit vector ports in the testbench:

- The port size should be indicated when declaring the signals. Inputs to the module being tested are declared using **reg**, whereas outputs from the module being tested are declared using **wire**:
  `reg [3:0] A; wire [3:0] S;`
- The parameters for the module being tested do not need the port size of the signals:
  `my_4_bit_adder module_alias (A, B, CARRY_IN, S, CARRY_OUT);`
- The testbench stimuli for multi-bit vector ports can be written as:
  `A = 4'b0011; B = 4'b0011; CARRY_IN = 1'b0;`

4. Synthesise and implement your code on the FPGA, using appropriate switches and LEDs on the Basys 3 development board to represent the inputs and outputs.

This task is considered completed and understood if you have the following items related to the four-bit full adder:

- The RTL schematic of your design (item 2 of this task)
- The simulation waveform results of the three testbench stimuli (item 3 of this task)
- The four-bit ripple-carry adder on the Basys 3 development board (item 4 of this task)

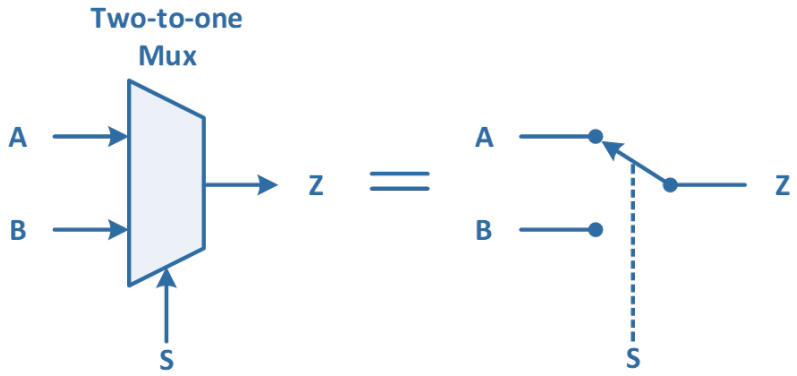
UNDERSTANDING | TASK 3

Instead of using four one-bit adder blocks, can you think of an alternative way (still using structural modelling) in creating the four-bit ripple-carry adder? Consider doing the same things as indicated in **UNDERSTANDING | TASK 2** by using such alternative way. This task is meant as practice for you to improve your Vivado skills and Verilog understanding, and will not be explained.

1-BIT TWO-TO-ONE MULTIPLEXER (POST-LAB NON-GRADED – NO SUBMISSION REQUIRED):

It is strongly encouraged to complete this practice task before working on the graded post-lab assignment!

A multiplexer (MUX) is a combinational circuit that connects one of its input signals to the output, based on the control signal. A simple 1-bit two-to-one mux, with inputs **A**, **B**, control signal **S**, and output **Z**, is illustrated as a functional block diagram, together with its simplified truth table, in **Figure 2.5.**



S	Z
0	A
1	B

Figure 2.5: *Functional block diagram and truth table of a 1-bit two-to-one multiplexer*

UNDERSTANDING | TASK 4

A quick way to implement the Verilog code for a 1-bit two-to-one multiplexer is using the conditional syntax:

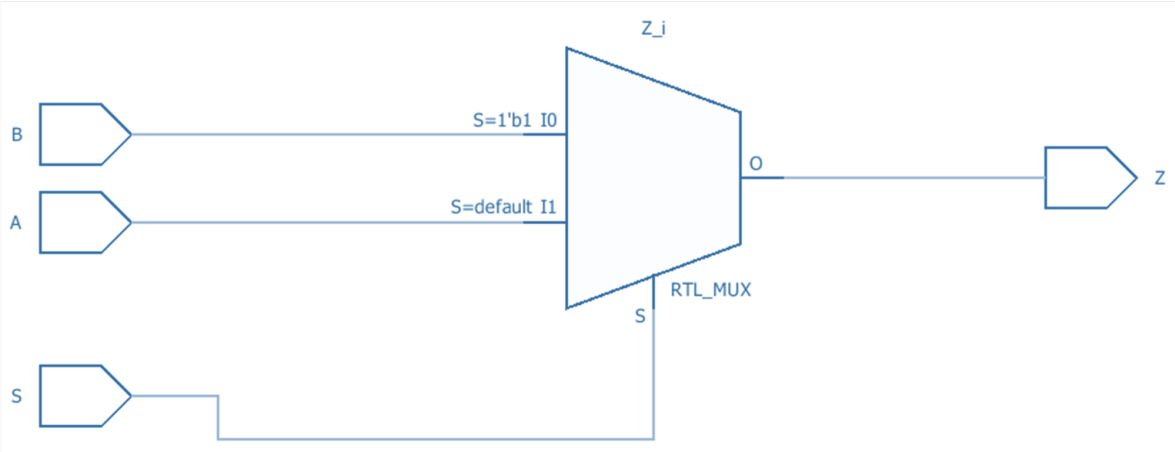
condition ? expression1 : expression2;

Notice in the schematic, how the code is automatically recognised as a MUX.

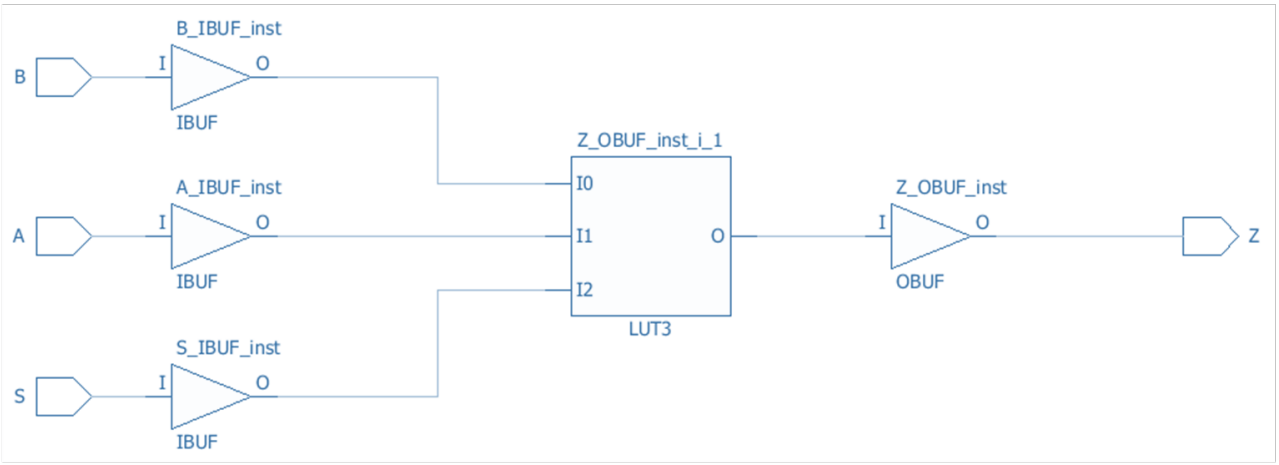
Verilog code for 1-bit two-to-one mux, using the dataflow method

```
module my_2_to_1_mux (input A, B, S, output Z);
    assign Z = S ? B : A; // assign B to Z if S = 1 or assign A to Z if S = 0;
endmodule
```

RTL schematic for the 1-bit two-to-one mux



Synthesised design schematic for the 1-bit two-to-one mux



Fill in the truth table for the **LUT3**, as extracted from the synthesised design schematic for the 1-bit two-to-one mux:

Explain how the truth table for the **LUT3** matches that of the truth table indicated in **Figure 2.5**:

GRADED POST-LAB ASSIGNMENT

Complete as much as possible, in **one working bitstream for this whole assignment**. It is much better to have a working program with some completed functionalities, instead of submitting a program without a working bitstream (No marks given).

IMPORTANT CHARACTERS

In this assignment, these are the important characters to note from your student matriculation number:

- The 2nd rightmost numerical value of your student matriculation number (Initialisation, subtask B and subtask C)
- The 3rd rightmost numerical value of your student matriculation number (Subtask A)

INITIALISATION

When the program starts, the seven segment displays must show the following patterns **exactly**, based on the **2nd rightmost numerical value of your student matriculation number**:

2nd Rightmost Numerical Value	0	1	2	3	4
Required 7-Segments Displays					

2nd Rightmost Numerical Value	5	6	7	8	9
Required 7-Segments Displays					

SUBTASK A

Based on the **3rd rightmost numerical value of your student matriculation number**, create two separate parallel adders as indicated in the table below:

3rd Rightmost Numerical Value	Required parallel adders. Each one of these parallel adders must be made up of multiple 1-bit adders	
0	2-bit parallel adder	3-bit parallel adder
1	3-bit parallel adder	2-bit parallel adder
2	2-bit parallel adder	4-bit parallel adder
3	4-bit parallel adder	2-bit parallel adder
4	3-bit parallel adder	4-bit parallel adder
5	4-bit parallel adder	3-bit parallel adder
6	3-bit parallel adder	5-bit parallel adder
7	5-bit parallel adder	3-bit parallel adder
8	2-bit parallel adder	5-bit parallel adder
9	5-bit parallel adder	2-bit parallel adder

Following that, make use of both parallel adders to create a single complete n-bit parallel adder with inputs A and B, and output S. The bits given to the single complete n-bit adder must be divided between the two parallel adders in the following manner:

3rd Rightmost Numerical Value	**Most significant bits** of the complete adder must use the following adder	**Least significant bits** of the complete adder must use the following adder	n-bit input A, or Input B, of the complete adder	n-bit output S of the complete adder
0	2-bit parallel adder	3-bit parallel adder	5 bits	5 bits
1	3-bit parallel adder	2-bit parallel adder	5 bits	5 bits
2	2-bit parallel adder	4-bit parallel adder	6 bits	6 bits
3	4-bit parallel adder	2-bit parallel adder	6 bits	6 bits
4	3-bit parallel adder	4-bit parallel adder	7 bits	7 bits
5	4-bit parallel adder	3-bit parallel adder	7 bits	7 bits
6	3-bit parallel adder	5-bit parallel adder	8 bits	8 bits
7	5-bit parallel adder	3-bit parallel adder	8 bits	8 bits
8	2-bit parallel adder	5-bit parallel adder	7 bits	7 bits
9	5-bit parallel adder	2-bit parallel adder	7 bits	7 bits

The single complete n-bit adder must not have any inputs or outputs for carry bits.

SUBTASK B

When a certain pushbutton, is pressed and held, certain LEDs on the Basys 3 development board must light up. The pushbutton and LEDs to light up are dependent on the **2nd rightmost numerical value of your student matriculation number**, as indicated in the table below:

2nd Rightmost Numerical Value	Pushbutton to use	LEDs to turn on
0	BTNU (Up)	LD15, LD14, LD13
1	BTNR (Right)	LD15, LD14
2	BTND (Down)	LD15, LD14, LD13, LD12, LD11, LD10
3	BTNL (Left)	LD15, LD14
4	BTNC (Centre)	LD15, LD14, LD13, LD12
5	BTNU (Up)	LD15, LD14
6	BTNR (Right)	LD15, LD14, LD13, LD12
7	BTND (Down)	LD15, LD14, LD13, LD12, LD11, LD10
8	BTNL (Left)	LD15, LD14, LD13, LD12
9	BTNC (Centre)	LD15, LD14, LD13

SUBTASK C

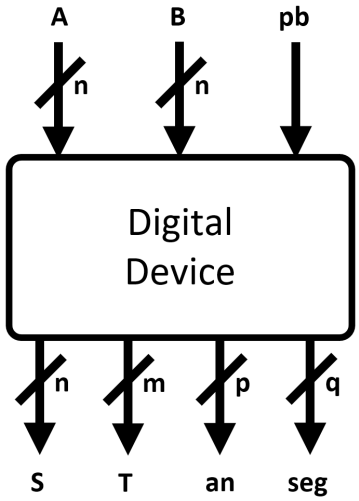
The result from the single complete n-bit adder of SUBTASK A is shown by default on the LEDs of the Basys 3 development board. However, when the user presses and hold the pushbutton that was indicated in SUBTASK B, it is required to have another alternate n-bit result (**AR**) shown on the LEDs of the Basys 3 development board, instead of the n-bit default result (**DR**). That alternate n-bit result is dependent on the **2nd rightmost numerical value of your student matriculation number**, as shown in the table below:

2nd Rightmost Numerical Value	Alternate result (AR)	Further details
0	3 least significant bits of DR inverted	
1	DR divided by 2	Ignore the decimal point of S (Round down)
2	DR multiplied by 8	Ignore bits that exceed the size of S
3	2 most significant bits of DR inverted	
4	DR divided by 4	Ignore the decimal point of S (Round down)
5	DR multiplied by 2	Ignore bits that exceed the size of S
6	4 least significant bits of DR inverted	
7	DR divided by 8	Ignore the decimal point of S (Round down)
8	DR multiplied by 4	Ignore bits that exceed the size of S
9	3 most significant bits of DR inverted	

Arithmetic operators for addition, subtraction, multiplication, and division are **NOT ALLOWED** anywhere inside this whole graded assignment. No marks will be given if arithmetic operators (**+** , **-** , ***** , **/**) are used

SUBTASK D (Implementation)

Combine the INITIALISATION, SUBTASK A, SUBTASK B and SUBTASK C together, such that the digital device implemented on the Basys 3 development board only have these ports:



INPUTS:
A : n number of switches (Subtasks A and C)
B : n number of switches (Subtasks A and C)
pb : one pushbutton (Subtask B)

OUTPUTS:
S : n number of LEDs (Subtasks A and C)
T : m number of LEDS (Subtask B)
an : p number of anodes (Initialisation)
seg : q number of segments (Initialisation)

It is compulsory to use the following switches to represent inputs A and B of the Digital Device:

- The input A must use consecutive switches on the Basys 3 development board, with the **least significant bit A[0] linked to SW0**. Similarly, A[1] should be linked to SW1, A[2] to SW2, and so on.
- The input B must use consecutive switches on the Basys 3 Development board, with the **least significant bit B[0] linked to SW8**. Similarly, B[1] should be linked to SW9, B[2] to SW10, and so on.
- **Switches not used by A or B must NOT be used or linked to any other signals under any circumstances.** For example, in a 4-bit Digital Device, SW4 to SW7, and SW12 and SW15, should not be linked to any signals, nor used in any circumstances.

It is compulsory to use the following LEDs to represent the output S of the Digital Device:

- The output S must use consecutive LEDs on the Basys 3 development board, with the **least significant bit S[0] linked to LD0**. Similarly, S[1] should be linked to LD1, S[2] should be linked to LD2, and so on.
- **LEDs not used by S or T must NOT be used or linked to any other signals under any circumstances.** For example, in a 4-bit Digital Device, with the 2nd rightmost numerical value of the student matriculation number being 3, LD4 to LD13, should not be linked to any signals, nor used in any circumstances.

SUBTASK E (Simulation)

You are also required to simulate and verify any **six unique** test cases in **one single simulation** for the digital device created in SUBTASK D, and which meets the following conditions:

- At least two of the test cases must have the pushbutton (pb) to be ON
- At least two of the test cases must have the pushbutton (pb) to be OFF
- The anode (an) value and segment (seg) value must match the requirement set out in the INITIALISATION

A screenshot (PrintScreen) of the simulation waveform pattern from the Vivado simulation window must be obtained, and then pasted on a 1-page landscape page. Marks are only given if the simulation waveforms are **clear and meet these number representations**:

- Input A, input B, input pb, output S, output T are all in **binary representation**
- Output an, output seg, are all in **hexadecimal representation**

SUBTASK F (RTL Schematics)

A screenshot (PrintScreen) of the RTL analysis schematic from Vivado must be obtained, and then pasted on a 1-page landscape page. You are not allowed to do any editing to the RTL analysis schematic screenshot.

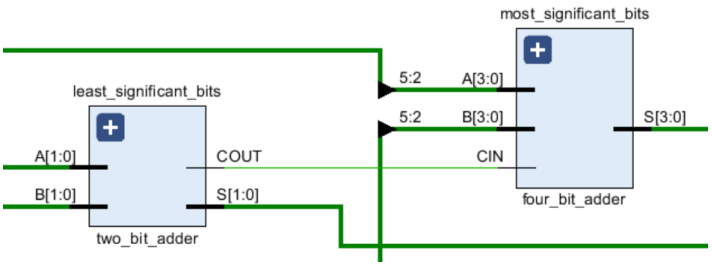
For marks to be awarded, the following conditions must be met for the RTL analysis schematics (The images being shown here is for a Digital Device with A, B and S being 6 bits. The 6 bits consist of a 2-bit parallel adder for the 2 least significant bits, and a 4-bit parallel adder for the 4 most significant bits in this example):

(1) None of the modules are expanded (That is, screenshot the top-level module clearly after clicking on RTL Analysis -> Schematics). Furthermore, **a minimum of two separate parallel adder modules** (As indicated in SUBTASK A) **must be seen without expanding any modules in the schematics.**

(2) All inputs of the Digital Device (SUBTASK D) must be clear, including the numerical values between the square brackets. For example:

(3) All outputs of the Digital Device (SUBTASK D) must be clear, including the numerical values between the square brackets. For example:

(4) All inputs to, and outputs from, the parallel adder modules must be clear, including the numerical values between the square brackets. For example, in this 6-bit Digital System example, there are two parallel adders (As indicated in SUBTASK A) being used:



DOCUMENT UPLOAD REQUIREMENTS:

(1) Your name and matriculation number on the top of the first page of the document.
(2) The screenshot (PrintScreen) of the simulation waveform pattern from the Vivado simulation window on the first page of the document.
(3) The screenshot (PrintScreen) of the RTL analysis schematic from Vivado on the second page of the document.

Print the two pages landscape document as a **single PDF** for CANVAS upload. The PDF file **must follow the naming template** indicated in the CANVAS submission instruction at the end of this lab manual.

SUGGESTIONS

- This assignment can be completed by using what you have learnt throughout lab session 2. It is not recommended to use advanced contents not taught in this lab session
- Complete the MUX task and understand the purpose of MUX before working on the assignment
- Use multi-bits to represent the anodes and segment displays
- Assume the pushbutton works like a switch when it is pressed and held
- The following will be taught in subsequent lectures / tutorials / labs, and are thus **not necessary** in lab 2:
    - if-else functions
    - always blocks
    - shift operators

EXAMPLE:

If your student matriculation number is A0159089Y, then:

2nd rightmost numerical value:	8
3rd rightmost numerical value:	0

INITIALISATION

SUBTASK A:

0	2-bit parallel adder	3-bit parallel adder	5 bits	5 bits

SUBTASK B:

8	BTNL (Left)	LD15, LD14, LD13, LD12

SUBTASK C:

8	DR multiplied by 4	Ignore bits that exceed the size of S

ADDITIONAL EXAMPLES FOR SUBTASK C:

Assuming 6 Bits System

SUPPOSE DEFAULT RESULT (DR) IS	LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0
DR divided by 2	
DR divided by 4	
DR divided by 8	
DR multiplied by 2	
DR multiplied by 4	
DR multiplied by 8	
3 least significant bits of DR inverted	
4 least significant bits of DR inverted	
2 most significant bits of DR inverted	
3 most significant bits of DR inverted	

LINK TO BASYS3 DEMONSTRATION EXAMPLE:

EE2026 - Assignment 2 Demonstration.m4v

CANVAS SUBMISSION INSTRUCTIONS

- Ensure that your bitstream has been successfully generated and tested on your Basys 3 development board **BEFORE** archiving your Vivado workspace for CANVAS upload

- It is compulsory to archive your project in a compressed form without any saved simulation waveforms. In the uploaded archive, the codes (.v files) are important, not the waveforms (.wdb files). **The archive size should not exceed 4 MB in size for any lab assignments.** Follow the instructions given in the pdf: "Archive Project in Vivado 2018.02"

- **After** following the instructions in "**Archive Project in Vivado 2018.02**", rename your project archive as indicated in the appendix of this lab manual

- **Separately** from the project archive, **the single PDF document** (Simulation waveform + RTL analysis schematic of the Digital Device) is to be named as indicated in the appendix of this lab manual.

- Upload to CANVAS EE2026 -> Assignments -> Lab 2 Graded Assignment -> Lab 2 Submission (On-Time)

- Download your CANVAS archive after uploading. **Click and drag the single folder within that archive to desktop**, and then open the Vivado project in that extracted folder to see if it can be opened. **Check if you can also run your bitstream correctly.** No project files and no working bitstream is equivalent to losing all marks

- The CANVAS upload must be completed by **Sunday 5th February 2023, 10:00 P.M.** Avoid uploading during the grace period of 2 hours

- A penalty of 25% applies for late submissions of up to 1 week.

- The late submission folder closes 1 week after the original deadline. **Late submissions are not accepted and not graded if a submission is found within the on-time folder, or if grading has already started on an earlier submitted file**. The late submission folder will be located at: CANVAS EE2026 -> Assignments -> Lab 2 Graded Assignment -> Lab 2 Submission (Late)

Plagiarism is penalised with a 100% penalty for all SOURCES and RECIPIENTS

All past and future submissions, and marks, will be reviewed in greater detail, for any person found to have plagiarised

ALL THE SUBMISSION INSTRUCTIONS LISTED ABOVE WILL AFFECT YOUR GRADES!

GRADING PROCESS

- During subsequent lab sessions, our graders will be providing you updates on the grading of your submission

- Submissions not following all the ***CANVAS SUBMISSION INSTRUCTIONS*** (listed above) will not be graded immediately, and they will instead be reviewed towards the end of the semester. **You will not be able to see your results during the lab sessions in such situations**

APPENDIX (COMPULSORY renaming just before CANVAS upload):

It is **compulsory to rename your project archive and PDF report**, just before the CANVAS upload, as listed in the table below.

Do not change any other part of the naming. Simply **copy** the naming from the table below and **paste** it while renaming your project archive and PDF report. Then upload these 2 items to CANVAS after the renaming.

Penalties will be incurred if your submission cannot be found according to the exact naming template below.

Archive Naming	PDF Report Naming
L2_Mon_AM_ARIF KHALID_983_Archive	L2_Mon_AM_ARIF KHALID_983_Report
L2_Wed_PM_ARTEMIS NGOH_342_Archive	L2_Wed_PM_ARTEMIS NGOH_342_Report
L2_Mon_AM_AUNG PHONE NAING_363_Archive	L2_Mon_AM_AUNG PHONE NAING_363_Report
L2_Wed_PM_BENJAMIN CHRISTOPHER TOH_702_Archive	L2_Wed_PM_BENJAMIN CHRISTOPHER TOH_702_Report
L2_Mon_AM_BENJAMIN LONG WEI MING_953_Archive	L2_Mon_AM_BENJAMIN LONG WEI MING_953_Report
L2_Wed_AM_BIAN RUI_671_Archive	L2_Wed_AM_BIAN RUI_671_Report
L2_Wed_PM_BRANDON OWEN SJARIF_179_Archive	L2_Wed_PM_BRANDON OWEN SJARIF_179_Report
L2_Wed_PM_BUI DUC THANH_820_Archive	L2_Wed_PM_BUI DUC THANH_820_Report
L2_Wed_AM_BUI PHUONG NAM_451_Archive	L2_Wed_AM_BUI PHUONG NAM_451_Report
L2_Wed_PM_CALEB CHAN JIA LE_569_Archive	L2_Wed_PM_CALEB CHAN JIA LE_569_Report
L2_Wed_PM_CHAO YIJU_863_Archive	L2_Wed_PM_CHAO YIJU_863_Report
L2_Wed_PM_CHEAH HAO YI_666_Archive	L2_Wed_PM_CHEAH HAO YI_666_Report
L2_Wed_AM_CHEN JUNHAN JERALD_262_Archive	L2_Wed_AM_CHEN JUNHAN JERALD_262_Report
L2_Mon_AM_CHENVISUWAT NITA_872_Archive	L2_Mon_AM_CHENVISUWAT NITA_872_Report
L2_Wed_AM_CHERAN LEE YENNING_991_Archive	L2_Wed_AM_CHERAN LEE YENNING_991_Report
L2_Wed_PM_CHEW JUN WEI MAX_381_Archive	L2_Wed_PM_CHEW JUN WEI MAX_381_Report
L2_Mon_AM_CHEW SI NING KACEY_433_Archive	L2_Mon_AM_CHEW SI NING KACEY_433_Report
L2_Wed_AM_CHIA YU XUAN_884_Archive	L2_Wed_AM_CHIA YU XUAN_884_Report
L2_Wed_PM_CHIEW YI XIANG_756_Archive	L2_Wed_PM_CHIEW YI XIANG_756_Report
L2_Wed_AM_CHONG YONG RUI_594_Archive	L2_Wed_AM_CHONG YONG RUI_594_Report
L2_Wed_PM_CHUA ZHONG HENG_908_Archive	L2_Wed_PM_CHUA ZHONG HENG_908_Report
L2_Mon_AM_CHUAH WAN JUIN_377_Archive	L2_Mon_AM_CHUAH WAN JUIN_377_Report
L2_Wed_PM_CLEON CHENG RUI FENG_796_Archive	L2_Wed_PM_CLEON CHENG RUI FENG_796_Report
L2_Mon_AM_CLEON LIEW GE WEI_788_Archive	L2_Mon_AM_CLEON LIEW GE WEI_788_Report
L2_Wed_PM_DEEPANJALI DHAWAN_498_Archive	L2_Wed_PM_DEEPANJALI DHAWAN_498_Report
L2_Wed_PM_DENNIS ONG QINKANG_605_Archive	L2_Wed_PM_DENNIS ONG QINKANG_605_Report
L2_Wed_PM_DEXTER HOON YONG EN_166_Archive	L2_Wed_PM_DEXTER HOON YONG EN_166_Report
L2_Wed_PM_DIVAKARAN MANUSHRI_824_Archive	L2_Wed_PM_DIVAKARAN MANUSHRI_824_Report
L2_Mon_AM_DYLAN CHIA TIAN_729_Archive	L2_Mon_AM_DYLAN CHIA TIAN_729_Report
L2_Wed_AM_DYLAN HO SHU JIE_536_Archive	L2_Wed_AM_DYLAN HO SHU JIE_536_Report
L2_Wed_AM_EE JIA EN JARED_035_Archive	L2_Wed_AM_EE JIA EN JARED_035_Report
L2_Wed_PM_ER JUN ZE_233_Archive	L2_Wed_PM_ER JUN ZE_233_Report
L2_Mon_AM_EU ZHENG XI_767_Archive	L2_Mon_AM_EU ZHENG XI_767_Report
L2_Wed_PM_EUGENE ANG JIA SHING_189_Archive	L2_Wed_PM_EUGENE ANG JIA SHING_189_Report
L2_Mon_AM_FARIS HAMID SIRRAJ_265_Archive	L2_Mon_AM_FARIS HAMID SIRRAJ_265_Report
L2_Wed_AM_FELICIA BEATRICE BUDIAWAN_855_Archive	L2_Wed_AM_FELICIA BEATRICE BUDIAWAN_855_Report
L2_Mon_AM_FOO YANG WEI JEROME_012_Archive	L2_Mon_AM_FOO YANG WEI JEROME_012_Report
L2_Mon_AM_GAO YUN FAN_187_Archive	L2_Mon_AM_GAO YUN FAN_187_Report
L2_Mon_AM_GARLAPATI SAI CHAITANYA_949_Archive	L2_Mon_AM_GARLAPATI SAI CHAITANYA_949_Report
L2_Mon_AM_GAU KIAT LOK JERALD_058_Archive	L2_Mon_AM_GAU KIAT LOK JERALD_058_Report
L2_Wed_PM_GOH JING HONG_722_Archive	L2_Wed_PM_GOH JING HONG_722_Report
L2_Mon_AM_GOH YI XUAN_250_Archive	L2_Mon_AM_GOH YI XUAN_250_Report

L2_Wed_PM_GRACE ZHU XING YU_936_Archive	L2_Wed_PM_GRACE ZHU XING YU_936_Report
L2_Mon_AM_GUAN XIAO_837_Archive	L2_Mon_AM_GUAN XIAO_837_Report
L2_Mon_AM_HAMADA MASAHIRO_120_Archive	L2_Mon_AM_HAMADA MASAHIRO_120_Report
L2_Wed_PM_HANG TIAN_725_Archive	L2_Wed_PM_HANG TIAN_725_Report
L2_Wed_PM_HO ZHAN RUI GLENN_662_Archive	L2_Wed_PM_HO ZHAN RUI GLENN_662_Report
L2_Wed_PM_HONG LIN SHANG_890_Archive	L2_Wed_PM_HONG LIN SHANG_890_Report
L2_Mon_AM_HOO TENG JUAN_494_Archive	L2_Mon_AM_HOO TENG JUAN_494_Report
L2_Mon_AM_HUI YU CONG_397_Archive	L2_Mon_AM_HUI YU CONG_397_Report
L2_Mon_AM_HUNG HIN WANG CLEMENT_615_Archive	L2_Mon_AM_HUNG HIN WANG CLEMENT_615_Report
L2_Wed_AM_JAVIENNE YEO MYN_441_Archive	L2_Wed_AM_JAVIENNE YEO MYN_441_Report
L2_Mon_AM_JOHN TOH JIA JUN_603_Archive	L2_Mon_AM_JOHN TOH JIA JUN_603_Report
L2_Wed_PM_KHAIRUL AIZAT B MD HALIM_315_Archive	L2_Wed_PM_KHAIRUL AIZAT B MD HALIM_315_Report
L2_Mon_AM_KHOO YOU RUN_353_Archive	L2_Mon_AM_KHOO YOU RUN_353_Report
L2_Wed_PM_KIM TAE WON_392_Archive	L2_Wed_PM_KIM TAE WON_392_Report
L2_Wed_PM_KISHORE SO ASOKAN_812_Archive	L2_Wed_PM_KISHORE SO ASOKAN_812_Report
L2_Wed_PM_KOH CHEE HENG_333_Archive	L2_Wed_PM_KOH CHEE HENG_333_Report
L2_Mon_AM_KOH JING JIE MARCUS_625_Archive	L2_Mon_AM_KOH JING JIE MARCUS_625_Report
L2_Mon_AM_KOH NGIAP HIN_229_Archive	L2_Mon_AM_KOH NGIAP HIN_229_Report
L2_Wed_AM_KWUA CHUN REN_262_Archive	L2_Wed_AM_KWUA CHUN REN_262_Report
L2_Wed_PM_LEE JUN HAO BRYAN_090_Archive	L2_Wed_PM_LEE JUN HAO BRYAN_090_Report
L2_Wed_PM_LEE JUN HUI ANSENN_865_Archive	L2_Wed_PM_LEE JUN HUI ANSENN_865_Report
L2_Wed_AM_LEE ZHI XUAN_363_Archive	L2_Wed_AM_LEE ZHI XUAN_363_Report
L2_Wed_PM_LEE ZHI ZHONG MOSES_669_Archive	L2_Wed_PM_LEE ZHI ZHONG MOSES_669_Report
L2_Wed_PM_LEI HAO_291_Archive	L2_Wed_PM_LEI HAO_291_Report
L2_Wed_PM_LEONARDO ONG DINGCHAO_944_Archive	L2_Wed_PM_LEONARDO ONG DINGCHAO_944_Report
L2_Wed_AM_LEONG HOI MING JOSHUA_256_Archive	L2_Wed_AM_LEONG HOI MING JOSHUA_256_Report
L2_Mon_AM_LEONG HUEN WENG_012_Archive	L2_Mon_AM_LEONG HUEN WENG_012_Report
L2_Wed_AM_LEONG HUNG REY_590_Archive	L2_Wed_AM_LEONG HUNG REY_590_Report
L2_Wed_PM_LEONG SONG ZHU OWEN_408_Archive	L2_Wed_PM_LEONG SONG ZHU OWEN_408_Report
L2_Wed_PM_LEONG YAT PANG_470_Archive	L2_Wed_PM_LEONG YAT PANG_470_Report
L2_Wed_PM_LI MINGYUAN_670_Archive	L2_Wed_PM_LI MINGYUAN_670_Report
L2_Mon_AM_LIM HONG YAO_619_Archive	L2_Mon_AM_LIM HONG YAO_619_Report
L2_Wed_AM_LIM ZHENG RONG_047_Archive	L2_Wed_AM_LIM ZHENG RONG_047_Report
L2_Mon_AM_LINUS PUAH JIA HE_811_Archive	L2_Mon_AM_LINUS PUAH JIA HE_811_Report
L2_Wed_AM_LIONG WEI YONG DEEN_930_Archive	L2_Wed_AM_LIONG WEI YONG DEEN_930_Report
L2_Mon_AM_LIU XIAOGE_254_Archive	L2_Mon_AM_LIU XIAOGE_254_Report
L2_Mon_AM_LOH JOO HOE_456_Archive	L2_Mon_AM_LOH JOO HOE_456_Report
L2_Mon_AM_LOH YUAN LONG KEDRIAN_084_Archive	L2_Mon_AM_LOH YUAN LONG KEDRIAN_084_Report
L2_Mon_AM_LU BINGYUAN_325_Archive	L2_Mon_AM_LU BINGYUAN_325_Report
L2_Mon_AM_MAN JUNCHENG_844_Archive	L2_Mon_AM_MAN JUNCHENG_844_Report
L2_Wed_PM_MANOJ DORAIRAJAN_508_Archive	L2_Wed_PM_MANOJ DORAIRAJAN_508_Report
L2_Wed_PM_MATTHEW LIU ZHEN JIE_439_Archive	L2_Wed_PM_MATTHEW LIU ZHEN JIE_439_Report
L2_Wed_PM_MITCH MALVIN_911_Archive	L2_Wed_PM_MITCH MALVIN_911_Report
L2_Wed_AM_MUSTAFA ANIS HUSSAIN_072_Archive	L2_Wed_AM_MUSTAFA ANIS HUSSAIN_072_Report
L2_Wed_PM_MUTHUKRISHNAN NAVYA_130_Archive	L2_Wed_PM_MUTHUKRISHNAN NAVYA_130_Report
L2_Mon_AM_MUTHYA NARAYANACHARY AKHI_509_Archive	L2_Mon_AM_MUTHYA NARAYANACHARY AKHI_509_Report
L2_Wed_PM_NAM SANGJUN_260_Archive	L2_Wed_PM_NAM SANGJUN_260_Report
L2_Wed_PM_NAZRUL SYAHMI BIN MURAD_711_Archive	L2_Wed_PM_NAZRUL SYAHMI BIN MURAD_711_Report
L2_Mon_AM_NG DE QI_171_Archive	L2_Mon_AM_NG DE QI_171_Report
L2_Mon_AM_NG KAI WEN_144_Archive	L2_Mon_AM_NG KAI WEN_144_Report
L2_Wed_PM_NG LIXUAN NIXON_667_Archive	L2_Wed_PM_NG LIXUAN NIXON_667_Report

L2_Mon_AM_NG YAN ZHEN_909_Archive	L2_Mon_AM_NG YAN ZHEN_909_Report
L2_Wed_PM_NGUYEN DUC THANG_361_Archive	L2_Wed_PM_NGUYEN DUC THANG_361_Report
L2_Wed_AM_NGUYEN QUANG ANH_912_Archive	L2_Wed_AM_NGUYEN QUANG ANH_912_Report
L2_Mon_AM_NICHOLAS H GOH MAOWEN_475_Archive	L2_Mon_AM_NICHOLAS H GOH MAOWEN_475_Report
L2_Mon_AM_NIKHIL SHASHIDHAR_992_Archive	L2_Mon_AM_NIKHIL SHASHIDHAR_992_Report
L2_Wed_PM_NING ZHI YAN_096_Archive	L2_Wed_PM_NING ZHI YAN_096_Report
L2_Wed_AM_OH YI XIU WILSON_510_Archive	L2_Wed_AM_OH YI XIU WILSON_510_Report
L2_Mon_AM_ONG CHUAN KAI_208_Archive	L2_Mon_AM_ONG CHUAN KAI_208_Report
L2_Mon_AM_ONG HEE JET_579_Archive	L2_Mon_AM_ONG HEE JET_579_Report
L2_Wed_AM_ONG JUN LIN JEREMIAH_679_Archive	L2_Wed_AM_ONG JUN LIN JEREMIAH_679_Report
L2_Mon_AM_ONG SHAO YONG_220_Archive	L2_Mon_AM_ONG SHAO YONG_220_Report
L2_Wed_PM_OONG JIN RONG JARED_178_Archive	L2_Wed_PM_OONG JIN RONG JARED_178_Report
L2_Wed_AM_OU NINGXIANG_191_Archive	L2_Wed_AM_OU NINGXIANG_191_Report
L2_Mon_AM_OW YONG JIN XUAN_649_Archive	L2_Mon_AM_OW YONG JIN XUAN_649_Report
L2_Wed_PM_PARANJAPE INDRANEEL RAJEE_412_Archive	L2_Wed_PM_PARANJAPE INDRANEEL RAJEE_412_Report
L2_Wed_PM_POOBALAN AATMIKA LAKSHMI_701_Archive	L2_Wed_PM_POOBALAN AATMIKA LAKSHMI_701_Report
L2_Mon_AM_RACHEL FONG RUI YUAN_567_Archive	L2_Mon_AM_RACHEL FONG RUI YUAN_567_Report
L2_Wed_PM_REYNOLD SAMEL LAM_216_Archive	L2_Wed_PM_REYNOLD SAMEL LAM_216_Report
L2_Mon_AM_RICHARD KURNIAWAN_030_Archive	L2_Mon_AM_RICHARD KURNIAWAN_030_Report
L2_Wed_PM_RICHARD LOONG CHENG JUN_496_Archive	L2_Wed_PM_RICHARD LOONG CHENG JUN_496_Report
L2_Wed_PM_RYAN TAN_565_Archive	L2_Wed_PM_RYAN TAN_565_Report
L2_Wed_PM_RYUJI KOW JIE SI_117_Archive	L2_Wed_PM_RYUJI KOW JIE SI_117_Report
L2_Wed_AM_SAMUEL TAN SZE WEE_575_Archive	L2_Wed_AM_SAMUEL TAN SZE WEE_575_Report
L2_Wed_AM_SAUNG NAYCHI MIN_779_Archive	L2_Wed_AM_SAUNG NAYCHI MIN_779_Report
L2_Wed_PM_SEBASTIAN SOEWANTO_268_Archive	L2_Wed_PM_SEBASTIAN SOEWANTO_268_Report
L2_Mon_AM_SEET SZE WEN_125_Archive	L2_Mon_AM_SEET SZE WEN_125_Report
L2_Mon_AM_SENTHILKUMAR SRIRAM_934_Archive	L2_Mon_AM_SENTHILKUMAR SRIRAM_934_Report
L2_Mon_AM_SEOW RUI SHENG_454_Archive	L2_Mon_AM_SEOW RUI SHENG_454_Report
L2_Wed_PM_SHAN YUXUAN_473_Archive	L2_Wed_PM_SHAN YUXUAN_473_Report
L2_Wed_AM_SHANNEN TAN_713_Archive	L2_Wed_AM_SHANNEN TAN_713_Report
L2_Mon_AM_SIM JUSTIN_898_Archive	L2_Mon_AM_SIM JUSTIN_898_Report
L2_Wed_AM_SIM QIAN HUI_289_Archive	L2_Wed_AM_SIM QIAN HUI_289_Report
L2_Mon_AM_SIUT WAI HONG CLEMENT_175_Archive	L2_Mon_AM_SIUT WAI HONG CLEMENT_175_Report
L2_Wed_PM_SONG ZIJIN_699_Archive	L2_Wed_PM_SONG ZIJIN_699_Report
L2_Mon_AM_STEVEN ANTYA ORVALA WASKI_459_Archive	L2_Mon_AM_STEVEN ANTYA ORVALA WASKI_459_Report
L2_Wed_PM_SURESH ABIJITH RAM_215_Archive	L2_Wed_PM_SURESH ABIJITH RAM_215_Report
L2_Wed_AM_SYED OMAR ZORAN_260_Archive	L2_Wed_AM_SYED OMAR ZORAN_260_Report
L2_Wed_AM_TAN HSIEN RONG_011_Archive	L2_Wed_AM_TAN HSIEN RONG_011_Report
L2_Wed_AM_TAN JIN SHENG BRIAN_260_Archive	L2_Wed_AM_TAN JIN SHENG BRIAN_260_Report
L2_Mon_AM_TAN JUN HAO KENNETH_519_Archive	L2_Mon_AM_TAN JUN HAO KENNETH_519_Report
L2_Wed_AM_TAN TZE LOONG_867_Archive	L2_Wed_AM_TAN TZE LOONG_867_Report
L2_Mon_AM_TAN WAN LIN_587_Archive	L2_Mon_AM_TAN WAN LIN_587_Report
L2_Wed_AM_TAN YI ZHE_674_Archive	L2_Wed_AM_TAN YI ZHE_674_Report
L2_Mon_AM_TAN YU XIANG GARETH_682_Archive	L2_Mon_AM_TAN YU XIANG GARETH_682_Report
L2_Wed_AM_TAN ZI XI_046_Archive	L2_Wed_AM_TAN ZI XI_046_Report
L2_Wed_AM_TANG JUN MEI SHANICE_739_Archive	L2_Wed_AM_TANG JUN MEI SHANICE_739_Report
L2_Wed_PM_TAY JIUN YUAN_398_Archive	L2_Wed_PM_TAY JIUN YUAN_398_Report
L2_Mon_AM_TAY YU YANG_039_Archive	L2_Mon_AM_TAY YU YANG_039_Report
L2_Wed_AM_TENG YUANKAI_862_Archive	L2_Wed_AM_TENG YUANKAI_862_Report
L2_Mon_AM_TEO JUN YONG ADEN_600_Archive	L2_Mon_AM_TEO JUN YONG ADEN_600_Report
L2_Mon_AM_TEOH JING YANG_566_Archive	L2_Mon_AM_TEOH JING YANG_566_Report

L2_Wed_AM_THANT AUNG HTET NYAN_654_Archive	L2_Wed_AM_THANT AUNG HTET NYAN_654_Report
L2_Wed_AM_TIAN SHIXING_830_Archive	L2_Wed_AM_TIAN SHIXING_830_Report
L2_Mon_AM_TOH HONG FENG_218_Archive	L2_Mon_AM_TOH HONG FENG_218_Report
L2_Mon_AM_TOH MING CHUN_573_Archive	L2_Mon_AM_TOH MING CHUN_573_Report
L2_Mon_AM_TONG ZHENG HONG_407_Archive	L2_Mon_AM_TONG ZHENG HONG_407_Report
L2_Mon_AM_TRICIA BOO KOH WEI PING_477_Archive	L2_Mon_AM_TRICIA BOO KOH WEI PING_477_Report
L2_Mon_AM_TU HUIYU_423_Archive	L2_Mon_AM_TU HUIYU_423_Report
L2_Wed_PM_UDAYAKUMAR NIVETHA_182_Archive	L2_Wed_PM_UDAYAKUMAR NIVETHA_182_Report
L2_Wed_PM_VARATHARAJU VIGNESH_677_Archive	L2_Wed_PM_VARATHARAJU VIGNESH_677_Report
L2_Wed_AM_VARNIKA SRIVASTAVA_513_Archive	L2_Wed_AM_VARNIKA SRIVASTAVA_513_Report
L2_Wed_PM_VISHNU_211_Archive	L2_Wed_PM_VISHNU_211_Report
L2_Wed_AM_VU VAN DUNG_825_Archive	L2_Wed_AM_VU VAN DUNG_825_Report
L2_Wed_AM_WANG HAOYANG_534_Archive	L2_Wed_AM_WANG HAOYANG_534_Report
L2_Wed_AM_WANG SILANG_130_Archive	L2_Wed_AM_WANG SILANG_130_Report
L2_Mon_AM_WANG TINGJIA_501_Archive	L2_Mon_AM_WANG TINGJIA_501_Report
L2_Wed_AM_WANG YONGBIN_968_Archive	L2_Wed_AM_WANG YONGBIN_968_Report
L2_Wed_PM_WILSON LEE JUN WEI_735_Archive	L2_Wed_PM_WILSON LEE JUN WEI_735_Report
L2_Wed_AM_WINSTON LIM CHER HONG_359_Archive	L2_Wed_AM_WINSTON LIM CHER HONG_359_Report
L2_Wed_AM_WONG ZHONG XIANG_929_Archive	L2_Wed_AM_WONG ZHONG XIANG_929_Report
L2_Mon_AM_WOO KAI NING_128_Archive	L2_Mon_AM_WOO KAI NING_128_Report
L2_Wed_PM_WOO WEN JUN_636_Archive	L2_Wed_PM_WOO WEN JUN_636_Report
L2_Wed_PM_WU ZHEN_039_Archive	L2_Wed_PM_WU ZHEN_039_Report
L2_Wed_PM_YAO HE_485_Archive	L2_Wed_PM_YAO HE_485_Report
L2_Mon_AM_YEO MENG HAN_360_Archive	L2_Mon_AM_YEO MENG HAN_360_Report
L2_Mon_AM_YONG SHAN LING_973_Archive	L2_Mon_AM_YONG SHAN LING_973_Report
L2_Wed_PM_ZENG ZIQIU_720_Archive	L2_Wed_PM_ZENG ZIQIU_720_Report
L2_Wed_PM_ZHAI YUXIN_744_Archive	L2_Wed_PM_ZHAI YUXIN_744_Report
L2_Wed_AM_ZHANG WENZE_047_Archive	L2_Wed_AM_ZHANG WENZE_047_Report
L2_Wed_AM_ZHANG ZHITONG_202_Archive	L2_Wed_AM_ZHANG ZHITONG_202_Report
L2_Wed_AM_ZHAO LIXIUQI_464_Archive	L2_Wed_AM_ZHAO LIXIUQI_464_Report
L2_Wed_AM_ZHOU HUIQI_364_Archive	L2_Wed_AM_ZHOU HUIQI_364_Report
L2_Mon_AM_ZHOU KAIWEN_651_Archive	L2_Mon_AM_ZHOU KAIWEN_651_Report