Abstraction, 6, 263 implementation paradigm, xi–xii	Application Program Interface (API) notation, 19
modules and, 2–3	Architecture, x, 79, 99–101
Adder gates, 29–39	bottom-up, 3–4
Addresses, 45, 104	chip set, 2
direct addressing, 60–61	CPU and, 82–83
indirect addressing, 61	Hack, 5–6, 85–98
machine language and, 60–61, 63	hardware, 2
mapping and, 84–91, 137–141	I/O and, 84–85
memory and, 81-82 (see also Memory)	Jack, 175–176 (see also Jack)
program size limits and, 106	machine language and, 106–107
registers and, 45, 83–86	memory and, 81–82
subroutines and, 153–159	modifications and, 277-279
symbol table and, 105	modules and, 2–3
VM-Hack mapping and, 139–143, 161–168	optimization and, 80
Addressing instruction (A-instruction), 64–	registers and, 83-84
65, 108–110, 115	sequential chip hierarchy and, 47-50
Algorithms	standards and, 84
efficiency and, 249, 272-273	stored program concept and, 80
graphics and, 257–263	top-down, 3
mathematics and, 248–252	VM and, 121–151 (see also Virtual
memory management and, 252-256	Machine)
operating systems and, 272-273 (see also	von Neumann, 62, 79-81, 85
Operating systems)	Aristotle, 6
runtime and, 249	Arithmetic addition, 37
syntax and, 250	Arithmetic Logic Unit (ALU), 2, 6, 39
ALU. See Arithmetic Logic Unit	Boolean arithmetic and, 29, 32, 35–38
Analysis-synthesis paradigm, 223	combinational chips and, 46-47
And function, 8–9, 20	CPU and, x, 82–83, 94
implementation of, 26	description of, 35–38
multi-bit versions of, 21-23	Hack and, 86

Arithmetic Logic Unit (ALU) (cont.) radix complement method, 31 operating systems and, 248–249 signed binary numbers, 31-32 visualized chip operations and, 292 stack processing and, 126-127 Boolean logic Arrays, 81 data translation and, 224-231 abstraction of, 11 Jack and, 175, 184–185, 191, 265, 269 algebra and, 8-10 operating systems and, 256, 265, 269 canonical representation, 9 stack processing and, 124-127 conditional execution, 62 variable-length, 256 gates and, 8, 11-13 Virtual Machine (VM) and, 137 hardware construction and, 13-14 ASCII code, 71, 89, 252 HDL and, 14-17 Assembler, x, 5, 71–72, 75–76, 118–120, 277 machine language and, 57-77 hash table, 115 repetition, 61–62 implementation of, 112-116 subroutine calling, 62 labels and, 105 truth tables, 8 machine language specification and, 107 two-input functions, 9-10 macros and, 117 Bootstrap code, 165 mnemonics and, 108, 114 Buses, 21-22, 286-287 program size limits and, 106 symbols and, 60, 104–106, 110–111, 114– C#, 4–5, 112, 121, 147, 169 116, 143, 164 Jack and, 174, 196 syntax and, 104, 107-110 C++, 112, 147, 253 test scripts and, 103-104 Canonical representation, 9 as translator program, 104-107, 163-164 Case conventions, 108 variables and, 105 Central Processing Unit (CPU), 6, 29, 59 ALU and, 82-83, 94 Best-fit, 254 architecture and, 82-83 Big-Oh notation (O(n)), 249 control unit and, 82-83 Binary code, 5, 108. See also Boolean logic description of, 82-83 code generation and, 223-246 emulators and, 306-309 graphics and, 257-263 Hack and, 62-63, 85-96 Jack and, 174 instruction memory and, 82 Binary search, 251 program counter and, 84 Bitmaps, 259–263, 269 registers and, 82 Bit shifting, 60 testing and, 306-309 Bit-wise negation, 60 von Neumann architecture and, 81 Character output, 259-263, 269 Boolean arithmetic, x addition, 30 Chips, 2. See also Gates algebra and, 8-10 adder, 29-39 ALU and, 29, 32, 35-38 API specification and, 19 binary numbers and, 30-32 Boolean logic and, 7–28 CPU and, 29 built-in, 287–288, 293, 296, 304–305 least significant bits (LSB), 30 buses and, 286-287 memory and, 42-47 clocks and, 289-291 most significant bits (MSB), 30 combinational, 41, 46-47

connections and, 285-286	mapping and, 137–141
cost and, 14–15	memory allocation and, 234
description of, 11	nested subroutine calling and, 153
efficiency and, 288	parsing and, 203–207
feedback loops and, 291–292	p-code and, 123, 146
Hack platform and, 85–91	semantics and, 199
hardware simulator and, 283–284	syntax analysis and, 199–221, 237–241
HDL and, 14–17, 281–296	VM and, 122–127, 161–168, 233–235 (see
incrementer, 33–39	also Virtual Machine)
maintaining state and, 41–42	XML and, 199–201, 211–218, 221
pins and, 284–286	Complex Instruction Set Computing (CISC),
RAM, 86	98
ROM, 85	Composite gates, 11–13
sequential, 41–55, 289–292	Compute instruction (<i>C</i> -instruction), 66–69,
simulators and, 299–306	86, 108–110, 115
testing and, 297–313	Computers. See also Architecture
visualized operations for, 288, 292–296	ALU and, 29 (see also Arithmetic Logic
Clocks, 41, 48, 289–290	Unit)
feedback loops and, 291–292	Boolean abstraction and, 11
memory and, 42, 52–54	bootstrap code and, 165
Code generation	CPU and, 29 (see also Central Processing
commands translation and, 231–232	Unit)
data translation and, 224–231	dedicated, 97
operating systems and, 272 (see also	emulators and, 121–122
Operating systems)	general-purpose, 97–98
registers and, 223–224	HDL and, 14–17 (see also Hardware
syntax analysis and, 237–241	Description Language)
virtual machines and, 224	machine language and, 57–77
Combinational logic. See Boolean arithmetic	memory and, 81–82
Commands translation, 231–232	program flow and, 153–159
Common Language Runtime (CLR), 123,	stored program concept and, 79–80
146–147	Conditional execution, 62
Communications, 279	Conditional jump, 62
Compare file, 18	Constants, 181–182
Compilers, ix–x, 2, 5–6, 17, 103, 112	Control logic, 94–95
abstraction and, 175–179	Control unit, 82–83
analysis-synthesis paradigm and, 223	Converters. See Not function
code generation and, 223-246	Counters, x, 45, 47–48, 50, 52, 84, 95
description of, 199–201	CPU. See Central Processing Unit
grammars and, 203, 206–207	Cycles, 42
Hack and, 133-134 (see also Hack)	
high-level language and, 146–147	Data flip-flop (DFF)
Jack and, 133-134, 174, 193-195 (see also	clocked chips and, 290-291
Jack)	implementation of, 50–51
lexical analysis and, 202, 208	sequential logic and, 42–48

Data races, 46 Debugging, 75 Decoding, 94-96 Defragmantation, 254–256 Demultiplexors, 21, 24–26 Design. See also Architecture alternative elements for, 277 Boolean logic and, 7–28 bottom-up, 3-4 cost and, 14–15 digital, 27 gate logic and, 11–13 HDL and, 14-17 (see also Hardware Description Language) modifications and, 277-279 standards and, 84 testing and, 297–313 top-down, 3 Device driver, 256-257 Direct addressing, 60-61 Division, 250–251 DOS, 272

Emulators, 121–122
Hack and, 76–77
testing and, 297, 306–313
Equivalence function, 10
Execute cycle, 86, 98
Expression evaluation, 187–188, 231–232

Feedback loops, 46, 52–53, 291–292 Fetching, 86, 95–96, 98 File formats, 107–110 First-fit, 254 Flip-flops, x, 41, 52–54, 287–288 clocked chips and, 290–291 data, 42–51, 290–291 implementation of, 50–51 memory and, 42 Flow control, 231–232 Formal languages, 201–202 Fragmentation, 254, 256 FreeList, 254, 256 Full-adder chip, 32–33, 38 Functions. See also Boolean logic And, 8-9, 20-23, 26 assembly language symbols and, 164 bootstrap code and, 165 calling commands and, 159–164 compilers and, 233-235 (see also Compilers) Jack and, 174–175, 190–193 (see also Jack) Nand, 2, 7, 10, 19, 27 Nor, 2, 10 Not, 8–9, 26 Or, 8-9, 20-26 subroutines, 62, 112, 153–161, 181–190, 195, 209, 234-235 symbolic names and, 160 testing and, 297-313 VM-Hack mapping and, 139–143, 161–168 Xor, 10, 20-23, 26

Gates, ix-x, xvi, 4, 6 adder, 29-39 And, 8-9, 20-23, 26 API specification and, 19 Boolean arithmetic and, 29–40 Boolean logic and, 7-28 built-in chips and, 287-288 buses and, 21-22, 286-287 composite, 11-13 construction of, 13-14 demultiplexors and, 21 flip-flops and, 41-54, 287-291 HDL and, 14–17 (see also Hardware Description Language) interfaces and, 12-13 memory and, 42-47 multi-bit versions of, 21–25 Nand, 2, 7, 10, 19, 27 Nor, 2, 10 Not, 8-9, 26 Or, 8–9, 20–26 primitive, 11-13, 25-26 sequential, 41–55 specification, 17–25 switching devices and, 2 Xor, 10, 20–23, 26

Goto operation, 95, 155	Boolean logic and, 8-28
Grammars	chips and, 85, 293-296 (see also Chips;
Jack and, 203, 207-215	Gates)
parsing and, 203–207	keyboard, 71
syntax analyzer and, 207-213	machine language and, 57-77
Graphical User Interface (GUI), 247, 283,	memory and, 81-82
288-290	modifications and, 278-279
testing and, 297–313	operating systems and, 247–276
visualized chip operations and, 292-296	RAM, 42–47
Graphics, 98	screen, 70
character output, 259–261	sequential chips and, 41–55
circle drawing, 259	simulators and, 299-306
keyboard handling and, 261-263	stored program concept and, 79-80
line drawing, 257–258	Hardware Description Language (HDL),
multiplication and, 258-259	x-xiii, 5-6, 93, 278
pixel drawing, 257	API notation and, 282
GUI. See Graphical User Interface	case sensitivity and, 283
	chip logic and, 17–25, 281–296
Hack, 5, 35, 79	compare file, 18
address instruction format and, 64-65, 85-	description of, 281
86	efficiency and, 288
assembler, 75–76, 103–120	hardware simulator and, 14, 17-25, 283-
built-in chips and, 293, 296	284
case conventions and, 108	header section, 15
case sensitivity, 75	identifier naming and, 283
C-instruction, 66–69	interfaces and, 15–16
CPU and, 62–63, 76–77, 85–96	logic building and, 39
destination specification and, 66-68	parts section, 15
file formats and, 71–72, 107–110	statement representation, 15
graphics card and, 98	technical references for, 281–296
input/output (I/O) handling and, 70–71,	testing and, 16–17
98	visualized chip operations and, 292–296
instructions and, 108–110	Hardware simulator, 14, 283–284
Internet and, 279	chip specifications and, 17–25
jump specification, 68–69	Hash tables, 115, 226
memory and, 63, 87–91, 96	HDL. See Hardware Description Language
modifications and, 278–279	Heap, 132–133
platform description, 62–64, 85–98	High-level language, 4–6
symbols, 69–70	Jack, 173 (see also Jack)
syntax, 71–73, 107–110	operating systems and, 248
VM mapping and, 139–143, 161–168	program flow and, 153–159
Half-adder chip, 32–33, 38	subroutines and, 62, 112, 153–161, 181–190,
Hardware, ix-x, 4-6. See also Input/output	195, 209, 234–235
architecture of, 2, 79–101	VM-Hack mapping and, 139–143, 161–168

If-goto destination, 155	array handling, 175, 184–185, 191, 265, 269
If-x-then-y function, 10	binary code and, 174
Immediate addressing, 61	classes and, 175-183, 187-193, 208, 248,
Incrementer chip, 33–39	263–273
Indirect addressing, 61	code generation and, 223-246
Inheritance, 195–196, 241–242	constants, 181-182
Input/output (I/O), x	constructor for, 234–235
characters and, 259–263	data types and, 183–185
device driver, 256–257	evaluation order, 188
graphics, 257–263	expression evaluation and, 187-188, 231-
Hack and, 62-77, 70-71, 98	232
keyboards, 261-263, 266	flow control and, 231-232
operating systems and, 256–270	generic statements, 187
screens, 265–266	grammar and, 203, 207-215
standards and, 84	identifiers, 181–182
Instructions, 116	inheritance and, 195-196, 241-242
addresses, 64-65, 108-110 (see also	I/O and, 191–193, 209–215, 265–266, 269–
Addresses)	270
assembler and, 103-120	Java and, 174, 183, 196
CISC, 98	keyboards and, 192-193, 266, 270
compilers and, 122-127 (see also Compilers)	lexical analysis and, 202, 208
compute, 66–69, 108–110	linked list implementation, 179–180
decoding, 94–96	Main.main function, 174–175
execution, 94–96	memory and, 193, 266-267, 270-271
fetching, 86, 95–96, 98	modifications and, 277-278
labels and, 105	as object-based language, 173, 195-196,
macros and, 117	199
memory and, 63, 82	object handling and, 189-190, 228-231
RISC, 98	operating system, 195, 197, 235, 253, 257-
stack processing and, 130 (see also Stack	273
processing)	operator priority, 188
subroutines and, 62, 112, 153-161, 181-190,	parsing and, 200, 217, 221
195, 209, 234–235	program elements in, 133-134
symbolic vs. binary, 104	rational numbers and, 175–179
variables and, 105	reserved words, 181–182
Interfaces, 282, 284	screens and, 192, 265-266, 269
HDL and, 15–16	simplicity of, 174
logic gates and, 12	standard library of, 174, 190-193, 196, 263
Intermediate language (IL), 123	strings and, 191, 264-265, 268-269
Internal pins, 15–16	subroutines and, 181–190, 195, 209, 234–235
	symbols and, 181-182, 238-239
Jack, 1, 4-5, 147, 165, 169, 197	syntax and, 181-182, 187, 207-221, 237-
abstract data types and, 175-179	241
API notation and, 175-176, 200, 215, 224	tokenizing and, 181, 202, 205, 208, 214-215,
applications writing, 193–195	219–221

type conversions, 183, 241 jumps, 61–62, 68–69, 96 variables and, 181–187 stack processing and, 130 (see also Stack VM code and, 174, 233-235, 240 processing) void methods and, 235 stored program concept and, 79–80 white space, 181–182 XML and, 199-201, 211-218, 221 Machine language, x Java, 17, 247, 253, 277 abstraction and, 81 assembler and, 112 addressing and, 60-61, 63 built-in chips and, 293, 296 assembler and, 103-120 Jack and, 174, 183, 196 binary codes and, 59–60 stack arithmetic and, 122, 134 commands and, 60-62 standard libraries, 147 compilers and, 122-127 (see also Compilers) VM and, 122, 134, 169 conditional execution, 62 Java Runtime Environment, 123, 146 Hack, 62-77 Java Virtual Machine (JVM), 121, 123, instruction memory and, 82 146 labels and, 105 Jump, 109–110, 114 memory and, 58-62 nested subroutine calling and, 153-159 mnemonic symbols, 59 specification, 61-62, 68-69, 96 processor and, 59 program size limits and, 106 Keyboard input, 71, 84, 86, 89, 96 registers and, 59 Jack and, 192–193, 266, 270 repetition and, 61–62 operating systems and, 266, 270 subroutine calling, 62 string reading and, 262-263 symbolic vs. binary, 104 text handling and, 261-263 syntax and, 60-62, 71-73, 104 visualized chip operations and, 292-293 testing and, 306–309 unconditional jump, 62 Labels, 70, 105, 110, 116, 155, 159 variables and, 105 Last-in-first-out (LIFO) storage model, 124, VM and, 122-127 (see also Virtual 157 Machine) Least significant bits (LSB), 30 Macro commands, 117 Lexical analysis, 202, 208 Mapping XML and, 199–201, 211–218, 221 I/O operations and, 84–91 Lexical analysis (LEX) tool, 217 keyboard handling and, 262-263 Line drawing, 257–259 memory segments and, 142–143 Linked list, 179-180 VM-to-Hack, 139-143, 161-168 VM-to-Jack, 233-235 Linux, xiii, 277 Load command, 60 Memory, 2 Logic addresses and, 45, 91 (see also Addresses) Boolean, 7-28 (see also Boolean logic) allocation and, 253-254 control logic and, 94-95 arrays and, 227-228 decoding, 94-96 clocks and, 42, 52-54 fetching, 95–96 compilers and, 234 HDL and, 281-296 dynamic allocation and, 252–253 instruction execution, 94–96 flip-flops and, 42–54

Memory (cont.) arrays and, 256, 265, 269 fragmentation and, 254, 256 classes and, 264-271 graphics and, 257–263 description of, 247 Hack and, 63, 87–91, 96 graphics and, 257–263 implementation and, 50-52 hardware/software gaps and, 247 improved allocation and, 254-256 initialization and, 267 instruction, 63, 82 input/output (I/O) management, 256–266, Jack and, 193, 266-267, 270-271 269 - 270machine language and, 58-62 Jack and, 195, 235, 263-273 (see also Jack) mapped input/output (I/O) and, 84–91 mathematical operations and, 248–252, 264, object handling and, 228-231 268 operating systems and, 247, 252-256, 266memory and, 247, 252-256, 266-267, 270-267, 270-271 271 RAM, 42-45, 49-50 (see also Random program size limits and, 106 access memory) screens and, 265-266, 269-270 registers and, 42-49 strings and, 252, 256, 264-265, 268-269 stored program concept and, 79–80 Sys and, 267, 271 subroutines and, 62, 112, 153–161, 181–190, Operator priority, 188 195, 209, 234–235 Or function, 8–9, 20 testing and, 310-311 implementation of, 26 variable locations and, 106 multi-bit versions of, 21-23 virtual segment mapping and, 142–143 multi-way versions and, 23–25 Overflow, 30 visualized chip operations and, 292 VM and, 127–133 von Neumann architecture and, 81 Parsing, 2, 17, 60, 116 Mnemonics, 59, 108, 114 assembler and, 112-114 Multi-bit bus, 286-287 compilers and, 217 (see also Compilers) Multiplexors, x, 20-26 expression evaluation and, 187–188, 231– Multiplication, 249-250, 258-259 232 Multitasking, 247 grammar and, 203-207 Jack and, 200, 203-207, 217, 221 Nand function, 2, 7, 10, 19, 27 programming and, 107 recursive descent, 204-206 Negative numbers, 31–32 Nested subroutine calling, 153–159 symbol-less, 114-115 .NET infrastructure, 122, 123, 146–147 VM and, 144–146, 168 Network interface cards, 84 Pascal, 123, 146 P-code, 123, 146 Newton-Raphson method, 251 Pins, 11, 15-16, 284-286, 290, 300 Non-terminals, 203, 211 Nor function, 2, 10 Pixel drawing, 257 Not function, 8-9, 26 Pointers, 69-70, 124, 131, 142, 161 Number base, 30 Pop operation, 124, 130–132 Positive numbers, 31–32 Object types, 183–184 Postfix notation, 231-232 Operating systems, ix-x, 4 Primitive gates, 11–13, 25–26 API notation and, 263, 267 Program counter, 45, 84, 95

Program flow virtual, 69 assembly language symbols and, 164 visualized chip operations and, 292 bootstrap code and, 165 Reserved words, 181-182 calling protocol and, 160-161 Return address, 158 Right Polish Notation (RPN), 231-232 LIFO model and, 157 nested subroutine calling and, 153-159 Rogers, Carl, 1 VM, 129–130, 133–134, 153–168 RPN. See Right Polish Notation Push operation, 124, 130–132 Screen output, 70, 84, 86, 89, 96 Radix complement method, 31 characters and, 259-263 RAM. See Random access memory graphics and, 257-263 Jack and, 192, 265-266, 269 Random access memory (RAM), x, 6, 278– 279 operating systems and, 265-266, 269-270 clocked chips and, 290-291 resolution and, 257-258 Hack platform and, 86, 96, 139-143, 161visualized chip operations and, 292-296 Segment index, 131-132, 135 implementation of, 52 Selectors, 20 memory management and, 253 Semantics, 199. See also Symbols; Syntax operating systems and, 270-271 data translation and, 224-231 registers and, 49-50 Sequential logic, 6 chip hierarchy and, 47–50 sequential logic and, 42–47 testing and, 304-308, 311-312 clocks and, 289-291 VM and, 137–143, 161–168 feedback loops and, 291–292 Rational numbers, 175–179 flip-flops and, 41–54 Read-only memory (ROM) chips, 6, 85–86, memory and, 42-47 91, 278–279 time and, 45–47 Read/write operations Signed binary numbers, 31–32 memory and, 42-47 Simulators, 101 registers and, 48-49 testing and, 297, 299-306 Recursive descent parsing, 204–206 Square root function, 251 Reduced Instruction Set Computing (RISC), Stack pointer, 124, 131, 142, 161 98 Stack processing, 122 Registers, x, 2 arithmetic and, 126–130 addresses and, 45, 83-86 bootstrap code and, 165 API specification and, 48–49 heap structure and, 132–133 architecture of, 83-84 LIFO model and, 124, 157 CPU and, 82 memory and, 130-133 Hack and, 63-64, 69 model of, 124-127 implementation of, 52 nested subroutine calling and, 153–159 machine language and, 59 pop operation, 124, 130–132 memory and, 42-49 push operation, 124, 130-132 RAM and, 49–50 subroutines and, 153–159 read-write operations and, 48-49 VM-Hack mapping and, 139–143, 161–168 testing and, 304-305 Standard language library, 4

Standard mapping, 141	GUI and, 297-298
Store command, 60	machine language and, 306–309
Stored program concept, 79–80	script commands and, 301-304
Strings, 184	simulators and, 297, 299-306
Jack and, 191, 264–265, 268–269	test scripts, 16-17, 103-104
keyboard handling and, 262-263	VM and, 310-313
operating systems and, 252, 256, 264-265,	Text files, 2
268–269	Time
Subroutines, 62, 112	clocks, 41-54, 289-292
calling protocol and, 160-161	counters, x, 45, 47–48, 50, 52, 84
code generation and, 234–235	sequential logic, 6, 42-54, 289-292
functional commands and, 153-159	testing and, 297–313
Jack and, 181-190, 195, 209, 234-235	Tokens, 181
LIFO model and, 157	Jack tokenizing, 202, 205, 208, 214-215,
void, 235	219–221, 237–241
Switching technology, 2, 11	syntax analyzer and, 207-213
Symbols	Transistors, 2, 11
assembler and, 60, 104-106, 110-111, 114-	Translator program, 163–164
116, 143, 164	Truth tables, 8–9
function calling and, 160	Turing, Alan, 122
Jack and, 181–182	Turing machine, 80–81
labels, 70, 105, 110, 116, 155, 159	Two-input Boolean functions, 9–10
machine language and, 59-60, 69-70, 104	2's complement method, 30
mnemomic, 59	
resolution and, 105–106	Unconditional jump, 62
variables and, 105	Unix, 272
Symbol tables, 103, 105, 115–116, 243	
data translation and, 225–226	Variables, 105, 116
Jack and, 238–239	argument, 234
Syntax, 5, 104	fields, 183, 185, 226, 227
expression evaluation and, 187–188, 231–	Jack and, 181–187
232	local, 183, 185–186, 227, 234, 253
formal languages and, 201–202	parameter, 183, 185–186
non-terminals and, 203, 211	scope and, 1, 225–226
RPN, 231–232	static, 183, 185, 226–227, 234, 253
semantics and, 199	Virtual Hardware Description Language
terminals and, 203, 211	(VHDL), 14
testing and, 301–304	Virtual Machine (VM)
XML and, 199–201, 211–218, 221	advantages of, 121, 123–124
T. 1	arithmetic and, 126–130, 135
Taylor series, 251	array handling and, 137
Terminals, 203, 211	bootstrap code and, 165
Testing	class and, 129
chips, 299–306	compilers and, 122–127
emulators and, 297, 306–313	design suggestions for, 143

emulators and, 121-122, 150-151 examples of, 135-139 functions and, 127, 129–130, 133, 135–139 Hack mapping and, 139-143, 161-168 heap structure and, 132–133 high-level language and, 146–147, 153– implementation, 55, 103, 112 Jack and, 174, 233-235, 240 language for, 122 memory and, 127, 129-133 modifications and, 277-279 modularity and, 123-124 nested subroutine calling and, 153-159 object handling and, 137-139 program flow and, 129-130, 133-134, 153-168 stack processing and, 124–127 subroutines and, 154-159 symbols and, 143 syntax and, 123 testing and, 310–313 translator, 121 Virtual memory segments, 131 Visual Basic, 147 VM. See Virtual Machine Void methods, 235 von Neumann architecture, 62, 79-81, 85 White space, 108, 113, 181-182

White space, 108, 113, 181–182 Windows, xiii, 277 Working stack, 161

XML, 199–201, 211–218, 221 Xor function, 10, 20 implementation of, 26 multi-bit versions of, 21–23

Yet Another Compiler Compiler (YACC), 217