

BITS-Pilani Dubai Campus
I Sem 2021-22
Digital Design Laboratory / ECE/INSTR/CS F215
Submission Report
Experiment No.- 6 (Multiplexer and Demultiplexer)

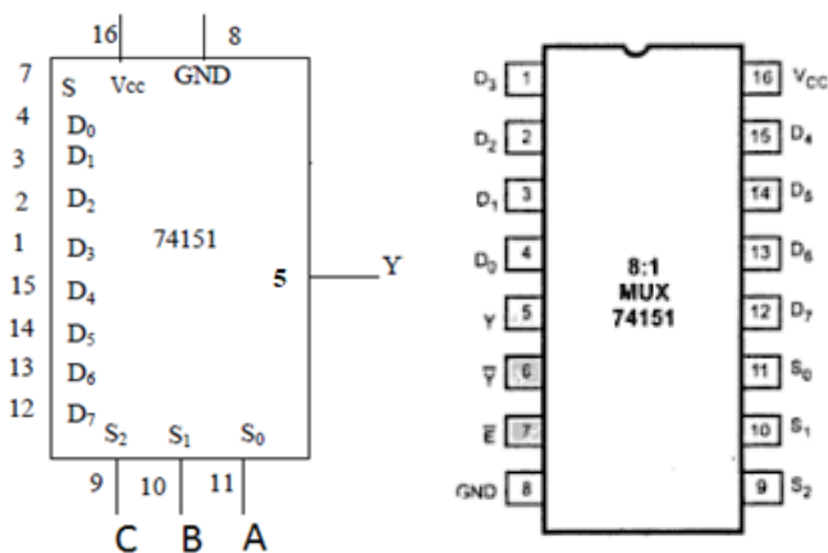
NameARSHDEEP SINGH.....

ID Number...2020A7PS0144U....

Hardware runs

Run 1: Multiplexer

Diagram



Truth Table

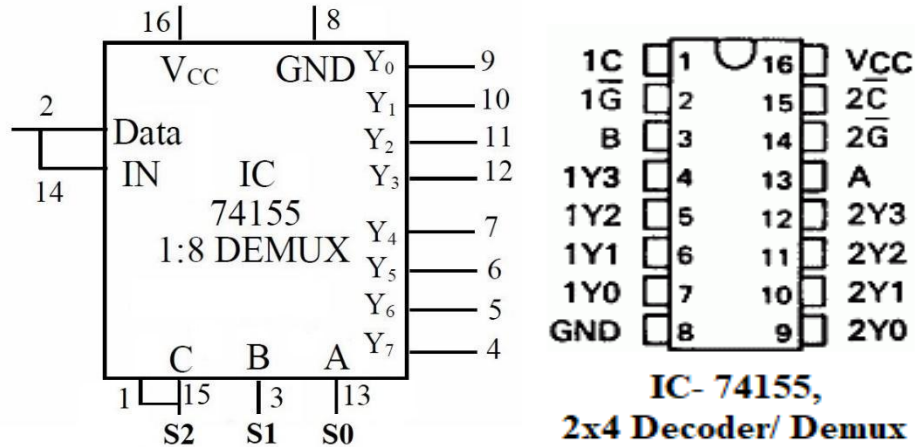
S	C	B	A	Y	Y'
1	x	x	x	x	x
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	0

Experiment No.- 6 (Multiplexer and Demultiplexer)

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Run 2: Demultiplexer

Diagram



Truth Table

Data	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
1	0	0	0	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0		1
1	1	1	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0

Software runs

Run 3: Multiplexer

1. Write the Verilog code and testbench for 2:1 Multiplexer using data flow modeling

A: Verilog Code and testbench-

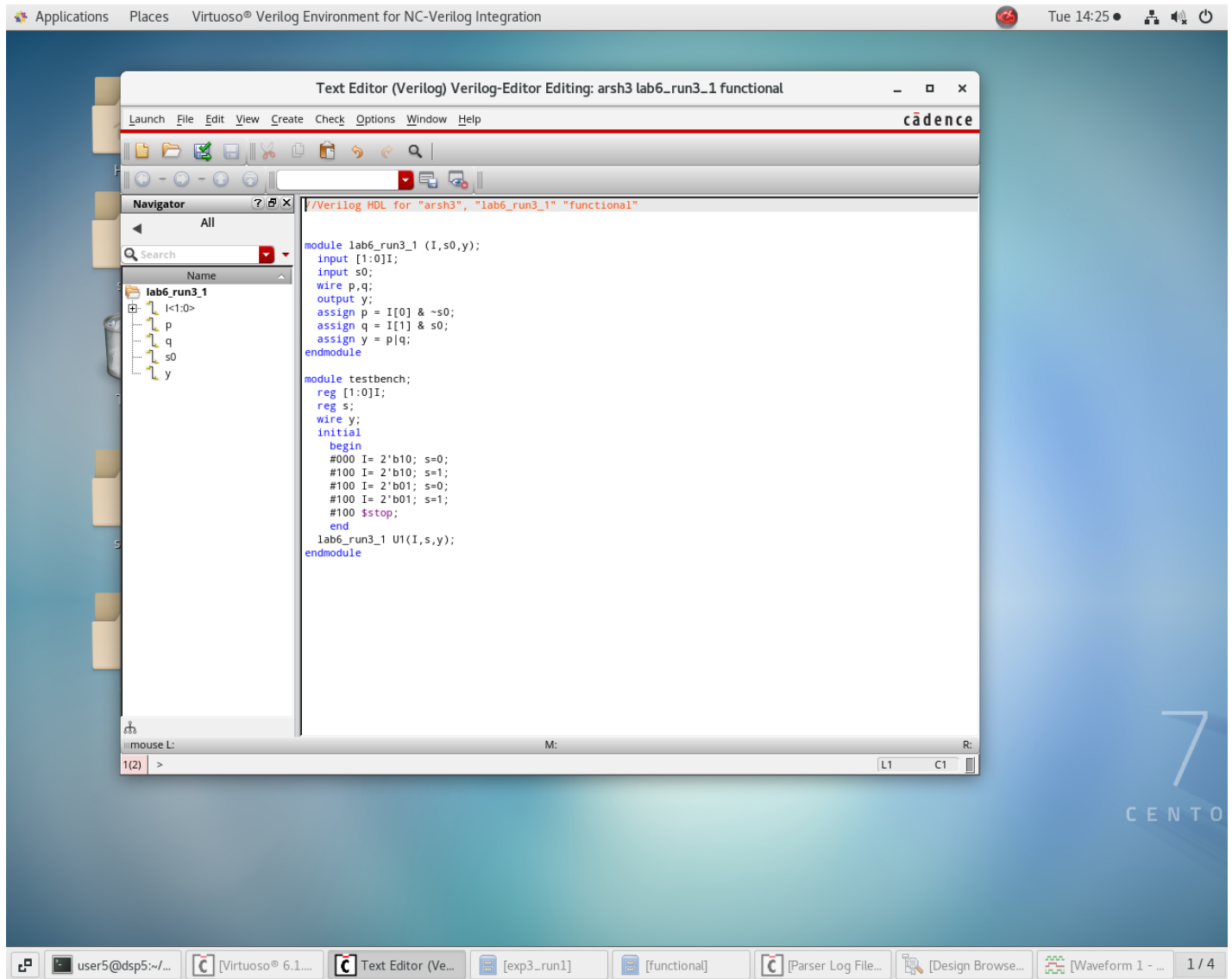
Experiment No.- 6 (Multiplexer and Demultiplexer)

Name **ID Number.....**

Experiment No.- 6 (Multiplexer and Demultiplexer)

Name

ID Number.....



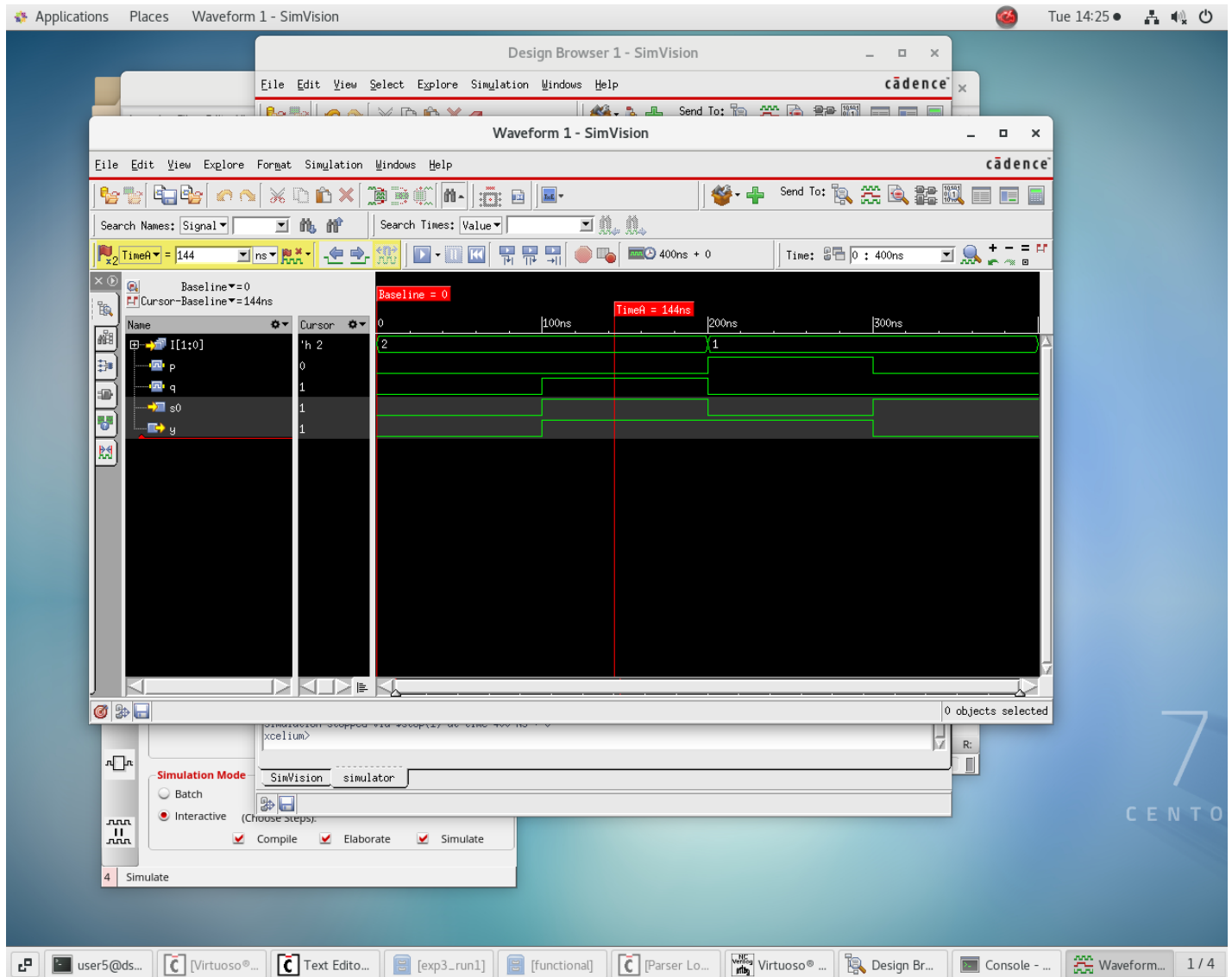
Q: Paste the screenshot of waveform window where you get the waveforms for the above code.

A:

Experiment No.- 6 (Multiplexer and Demultiplexer)

Name

ID Number.....



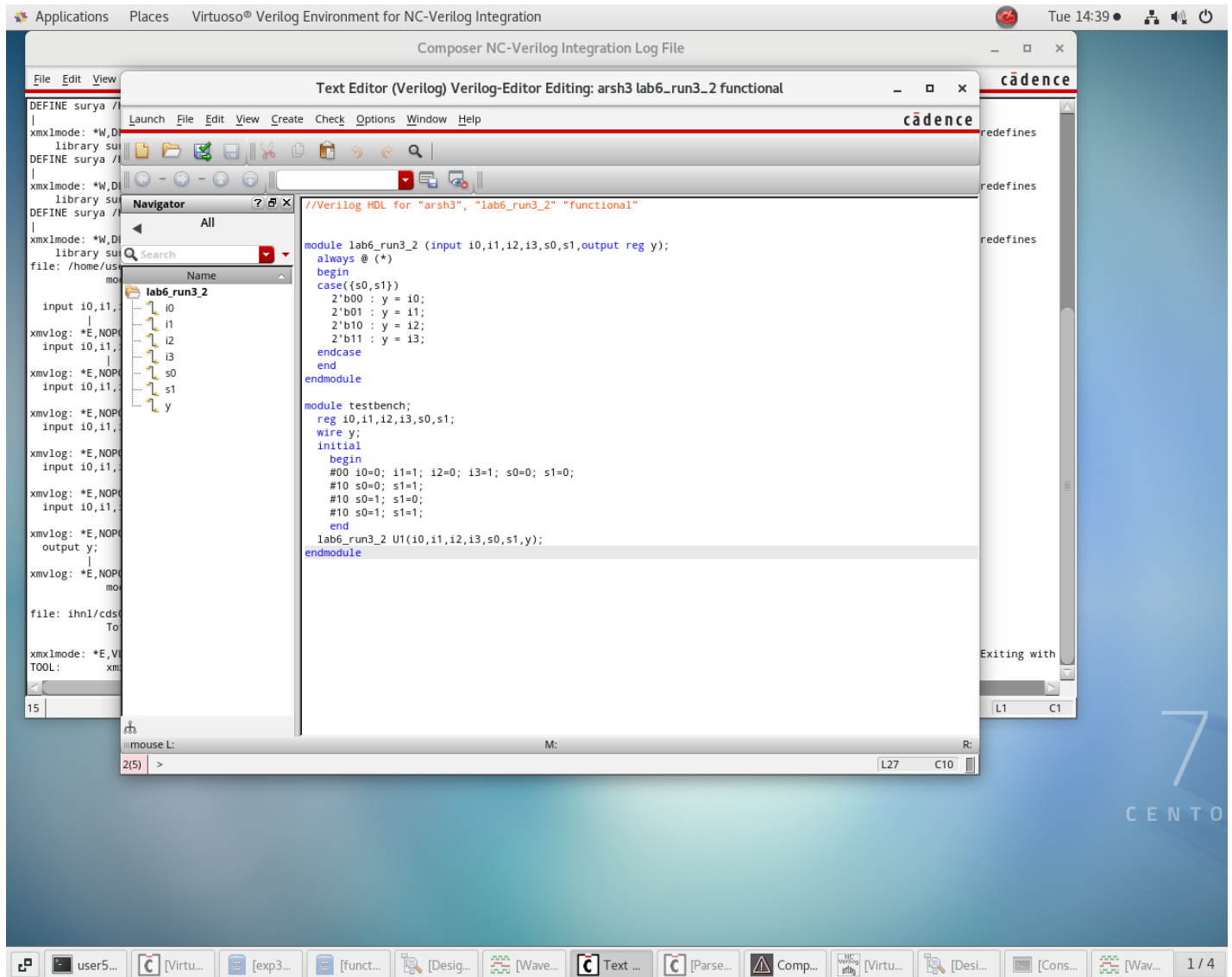
2. Write the Verilog code and testbench for 4:1 Multiplexer using behavioral modeling.

Experiment No.- 6 (Multiplexer and Demultiplexer)

Name

ID Number.....

A: Verilog Code and testbench -

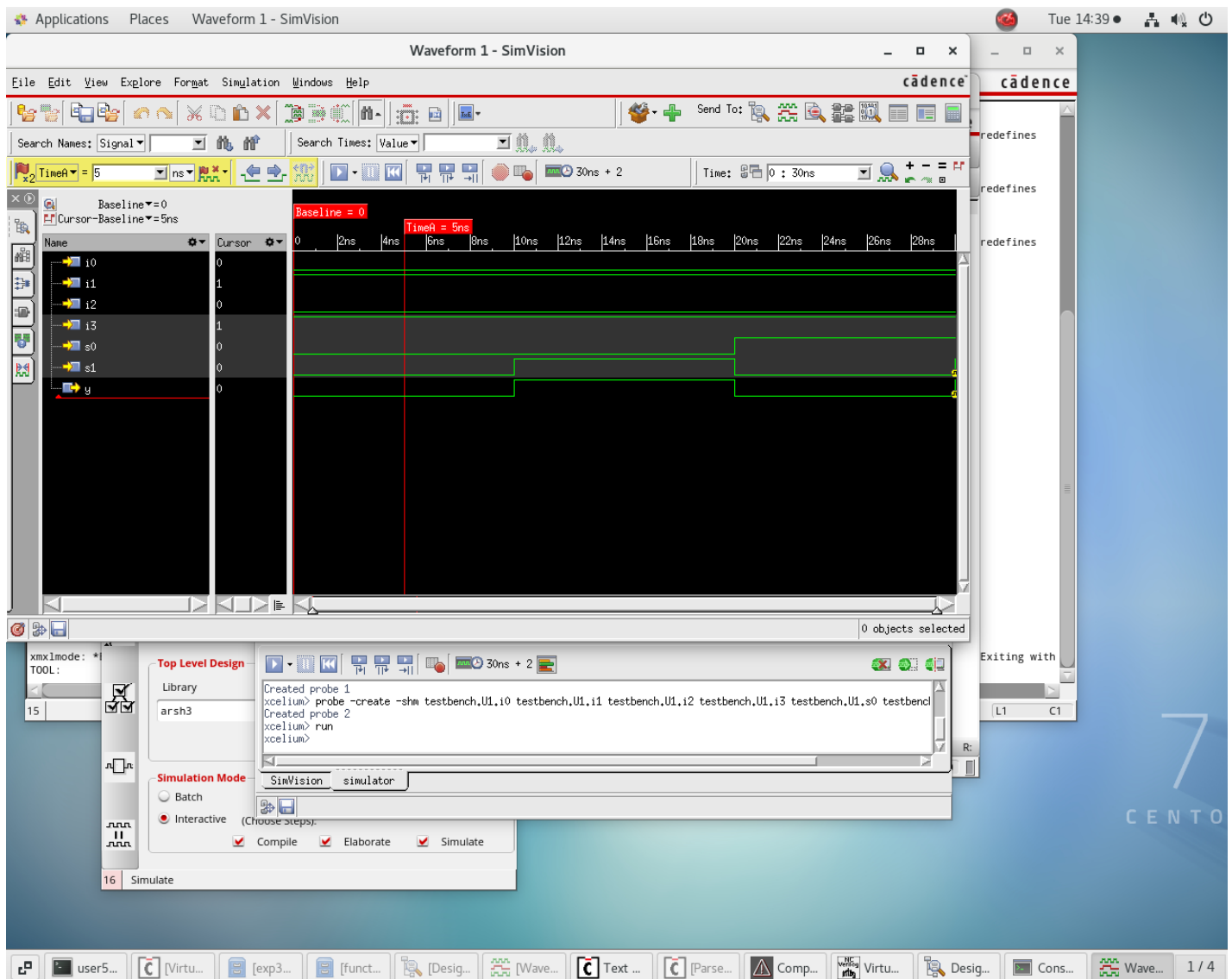


Experiment No.- 6 (Multiplexer and Demultiplexer)

Name ID Number.....

Q: Paste the screenshot of waveform window where you get the waveforms for the above code.

A:



Experiment No.- 6 (Multiplexer and Demultiplexer)

Name **ID Number.....**

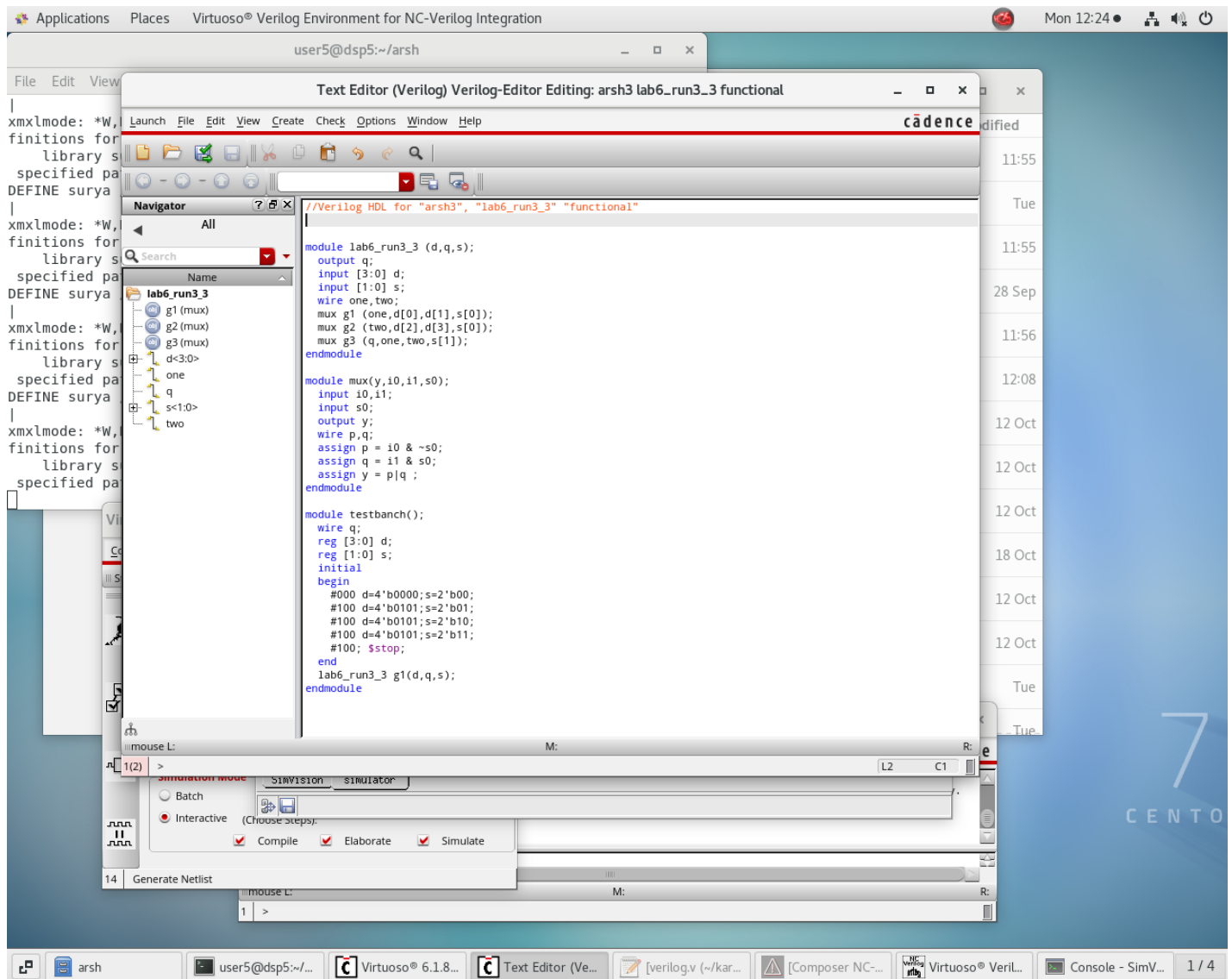
3. Write the Verilog code and testbench for 4:1 Multiplexer using structural modeling.

A: Verilog Code and testbench -

Experiment No.- 6 (Multiplexer and Demultiplexer)

Name

ID Number.....

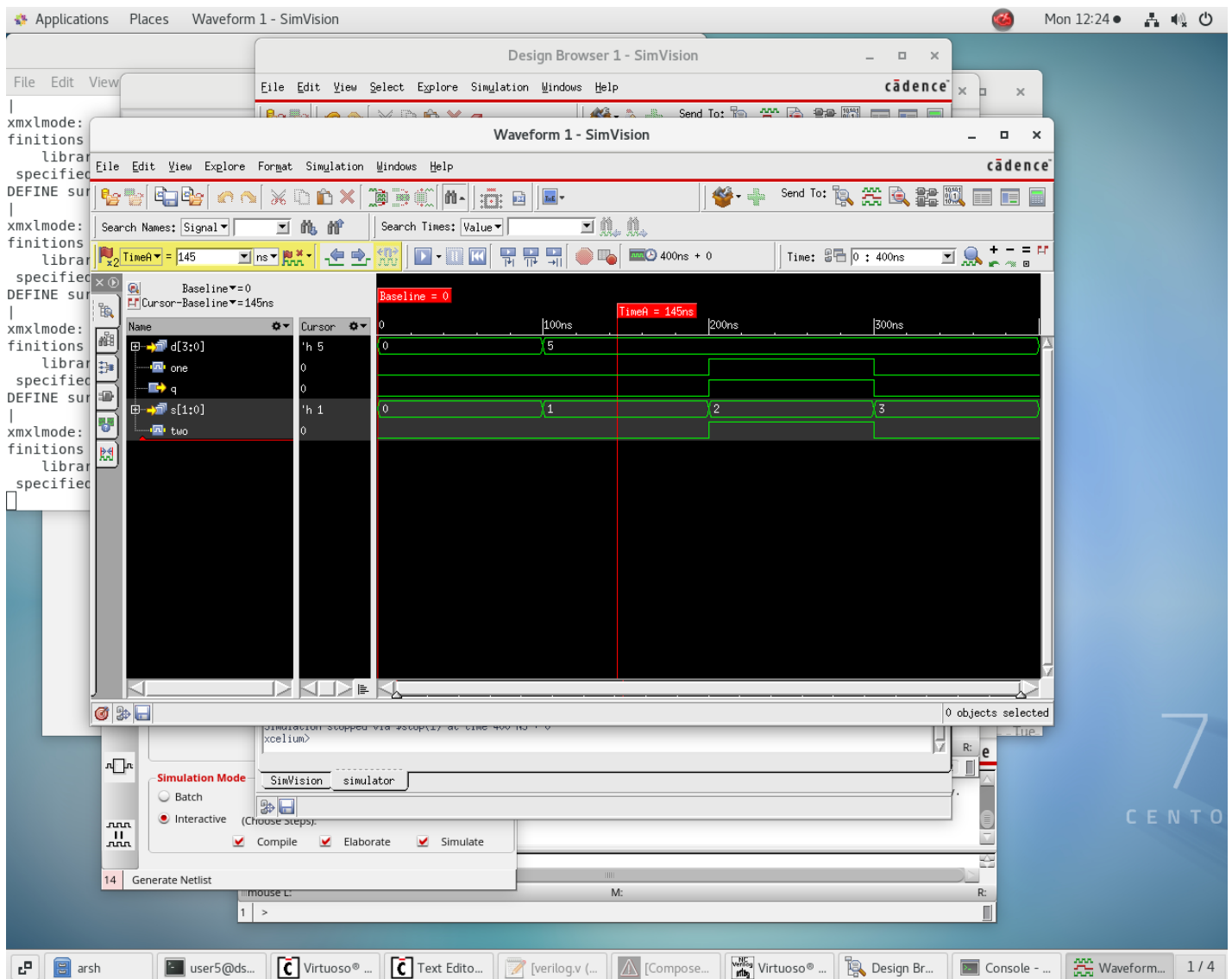


Experiment No.- 6 (Multiplexer and Demultiplexer)

Name ID Number.....

Q: Paste the screenshot of waveform window where you get the waveforms for the above code.

A:



Experiment No.- 6 (Multiplexer and Demultiplexer)

Name ID Number.....

Run 4: Demultiplexer

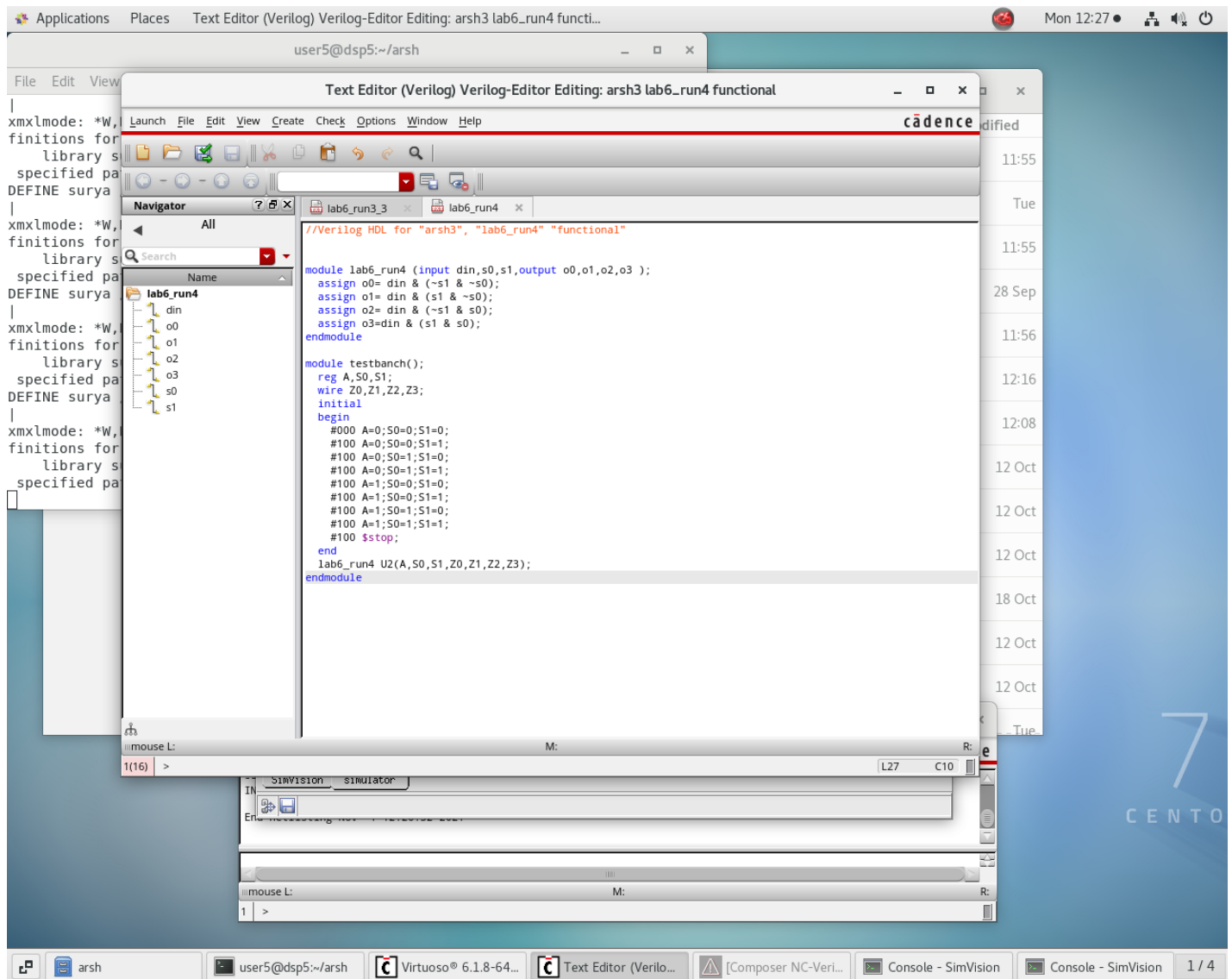
1. Write the Verilog code and testbench for 1:4 demultiplexer using behavioral modeling.

A: Verilog Code and testbench -

Experiment No.- 6 (Multiplexer and Demultiplexer)

Name

ID Number.....

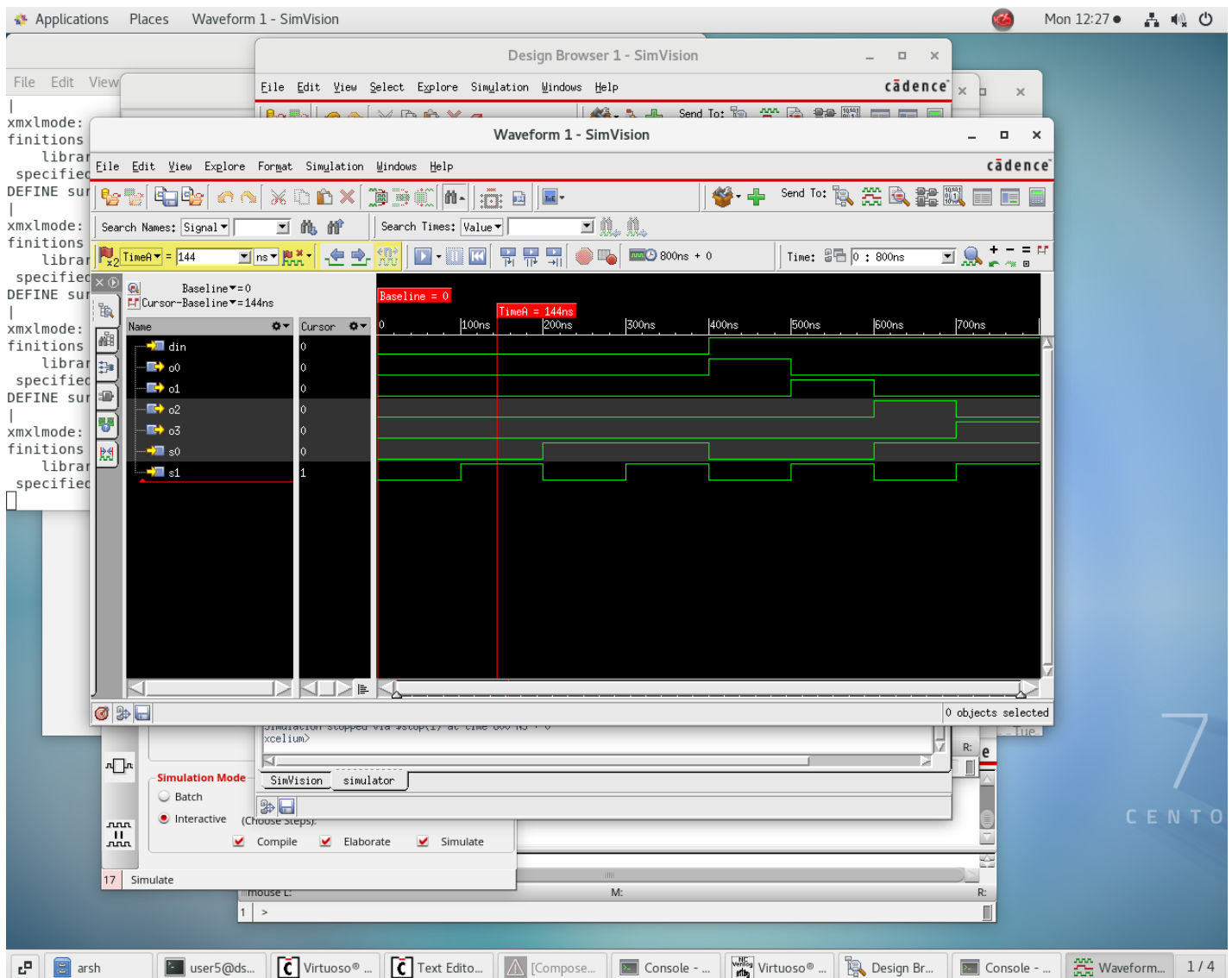


Experiment No.- 6 (Multiplexer and Demultiplexer)

Name ID Number.....

Q: Paste the screenshot of waveform window where you get the waveforms for the above code

A:



Experiment No.- 6 (Multiplexer and Demultiplexer)

Name ID Number.....

Assignment All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded '0' marks.

1. Write the Verilog code and testbench for 4:1 Multiplexer using data flow modeling.

Ans: Link1: <https://www.edaplayground.com/x/idu8>

2. Verilog code and testbench for implementing 2-input XOR gate using 2x1 multiplexer in structural modeling.

Ans: Link2: <https://www.edaplayground.com/x/q3fz>