BITS-Pilani Dubai Campus

I Sem 2021-22

Digital Design Laboratory / ECE/INSTR/CS F215

Submission Report

Experiment No.- 3 (Implementation of Boolean Function)

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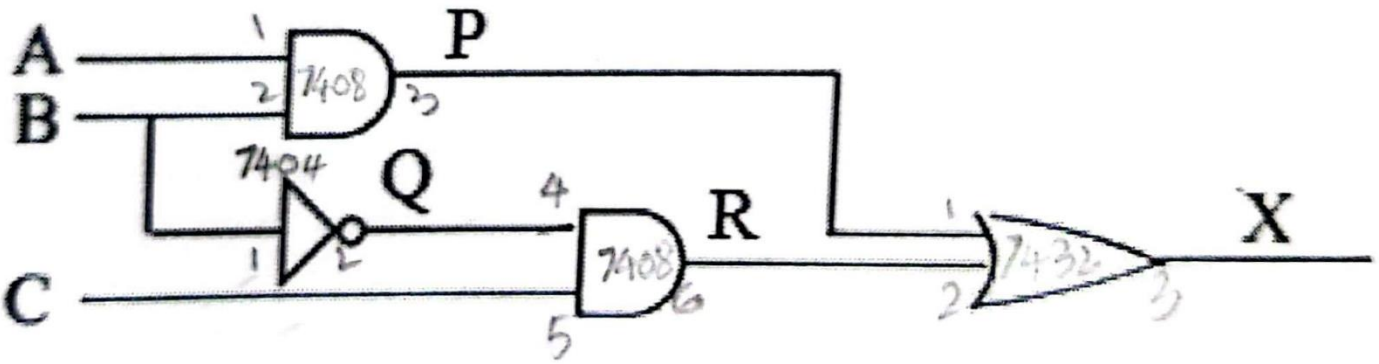
Hardware runs

Run 1: AND-OR implementation

Diagram

55



Truth Table

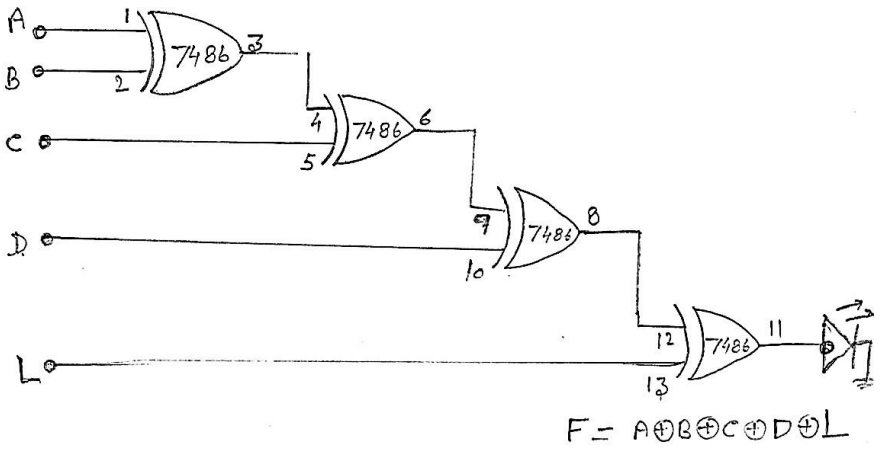
A	B	C	P	Q	R	X
0	0	0	0	1	0	0
0	0	1	0	1	1	1
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	1	0	0
1	0	1	0	1	1	1
1	1	0	1	0	0	1
1	1	1	1	0	0	1

Q: For the above circuit diagram fill in the following details

A: **No. of AND gates used:** 2
No. of NOT gates used: 1
No. of OR gates used: 1
Total No. of ICs used: 3

No. of AND gate IC used: 1
No. of NOT gate IC used: 1
No. of OR gate IC used: 1

Run 2: Parity generator
Diagram



Q: How many XOR gates are used?
A: 4

Q: How many 7486 IC are used? Can the circuit be implemented using only **one** 7486 IC?
A: 1 . yes .

Q: Take any six-input combinations of your choice and complete the below table.

Truth Table

A	B	C	D	L	P
0	1	1	0	0	0
0	1	1	0	1	1
1	1	1	1	0	0
1	1	1	1	1	1
1	0	1	0	0	0
1	0	1	0	1	1
1	0	0	1	0	0
1	0	0	1	1	1
1	1	0	0	0	0
1	1	0	0	1	1

Software runs

Run 3: Circuit implementation

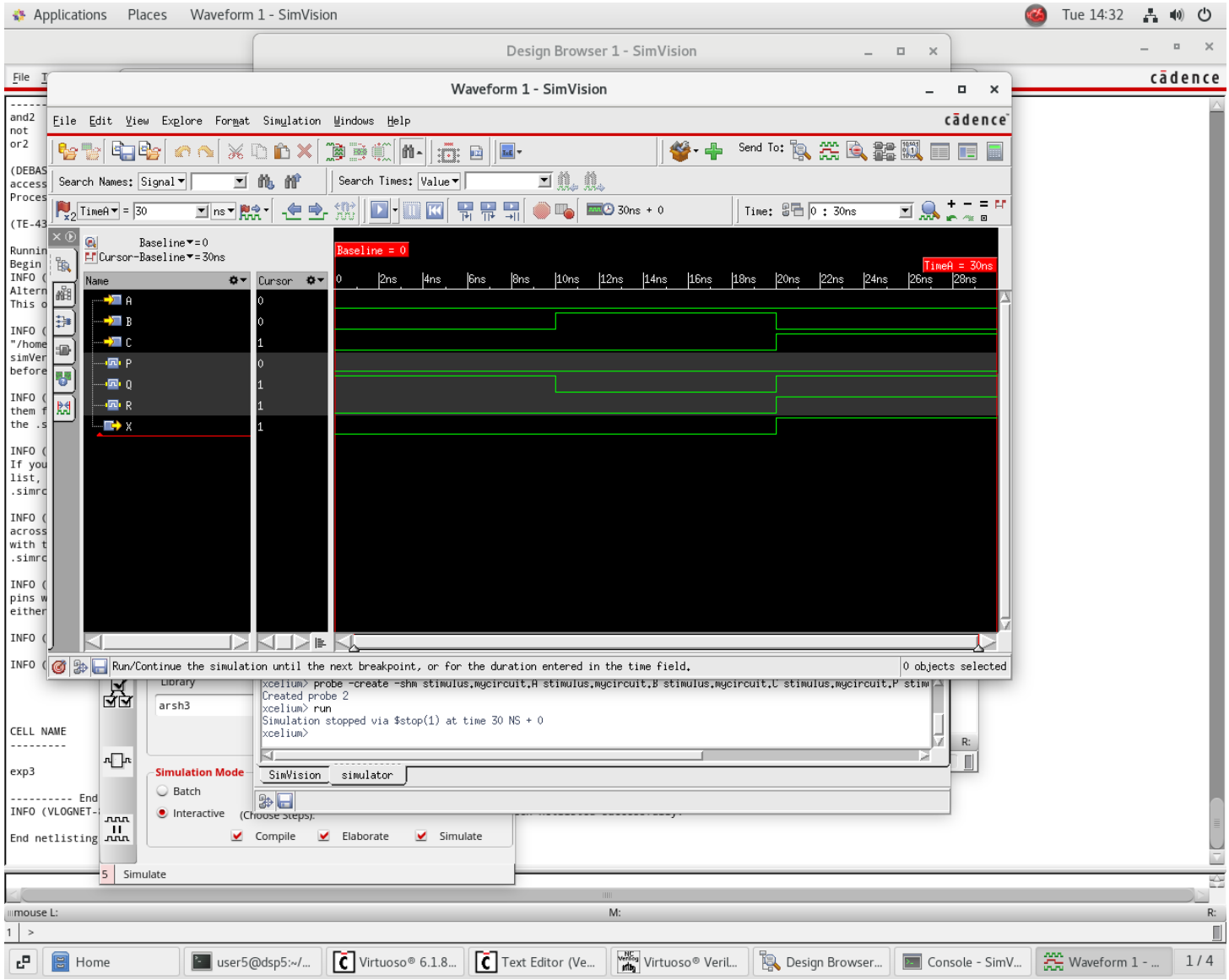
```
module exp3_Arshdeep (x,a,b,c);
input a,b,c;
output x;
wire p,q,r;
and g1(p,a,b);
not(q,b);
and(r,q,c);
or(x,r,p);
endmodule

module stimulus;
reg a,b,c;
wire x;
initial begin
a=0; b=0; c=0;
#10 a=0; b=1; c=0;
#10 a=0; b=1; c=1;
#10 $stop;
end
exp3_Arshdeep U1(x,a,b,c);
endmodule
```

(a) Implement the below circuit using Gate level modeling, write the code as well as its testbench.

Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.

A:



Run 4: Error detection and error correction codes

Q: Write Verilog code and testbench for generating even parity Hamming code for 4-bit data. (Hint: P0 = D2^D1^D0, P1 = D3^D1^D0, P2 = D3^D2^D0)

A: Verilog Code-

SV/Verilog Testbench

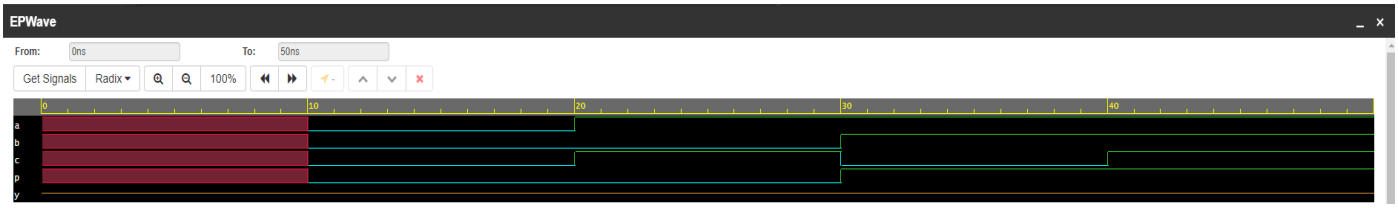
```
module even_parity_HCode_tb ;
  reg p,a,b,c;
  wire y;
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1 , even_parity_HCode_tb);
    #10 p=0 ; a=0 ; b=0 ; c=0 ;
    #10 p=0 ; a=1 ; b=0 ; c=1 ;
    #10 p=1 ; a=1 ; b=1 ; c=0 ;
    #10 p=1 ; a=1 ; b=1 ; c=1 ;
    #10 $stop ;
  end
  even_parity_HCode P1(y,p,a,b,c);
endmodule
```

SV/Verilog Design

```
module even_parity_HCode (y , p , a , b , c ) ;
  input p,a,b,c;
  output y;
  wire w1 , w2 ;
  assign w1 = p^a ;
  assign w2 = b^c ;
  assign w3 = w1^w2 ;
endmodule
```

Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.

A:



Assignment All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded '0' marks.
Copy-paste or type the unique URL of your assignment solution from website www.edaplayground.com for assignment questions. Please note that do not copy someone else's link as any kind of unfair means will result in academic misconduct and will be treated accordingly. All links for each user and each code are unique.

Q1: Implement a NOT gate using one 2-input NAND gate only. Write its verilog code also.
Ans: Link1: https://www.edaplayground.com/x/kAQX

Q2: Write Verilog code and testbench using data flow modeling for Y = ABC + AB +AC.
Ans: Link2: https://www.edaplayground.com/x/Bq5M

Q3: Write Verilog code and testbench for detecting even parity error in 4 bit (3+1) binary number.
Ans: Link3: https://www.edaplayground.com/x/HDsD

Q4: Write Verilog code and testbench for generating even parity bit for 4-bit binary number. (Hint: you can use the structure of run-2 of this experiment also or y = A^B^C^D).

Ans: Link4: https://www.edaplayground.com/x/ZRDn