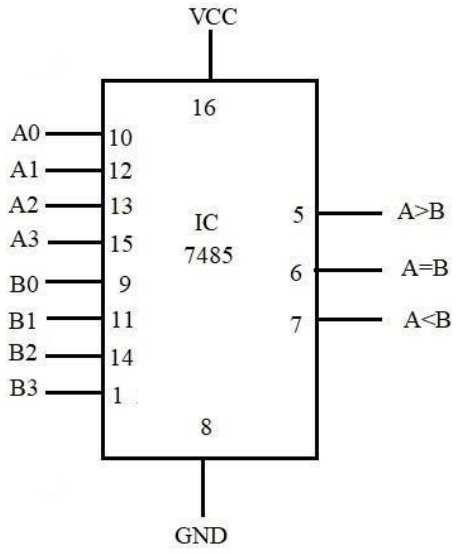
Experiment No.- 5 (Comparators and Decoders)

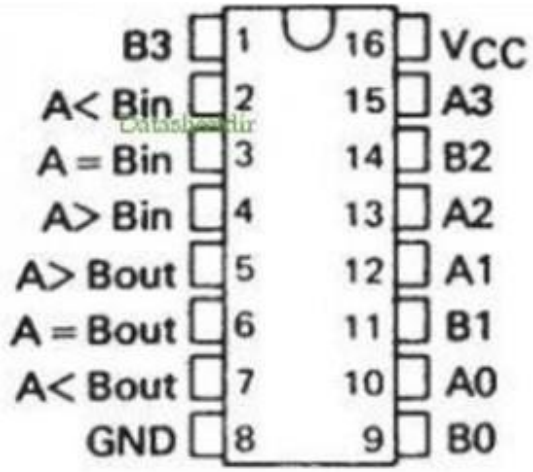
Name : Arshdeep Singh **ID Number :** 2020A7PS0144

Hardware runs

Run 1: Comparator

Diagram





IC 7485 4-bit Comparator

Truth Table

A (A3A2A1A0)	B (B3B2B1Bo)	A>B	A=B	A<B
0000	1111	0	0	1
1111	0000	1	0	0
0000	0000	0	1	0
1111	1111	0	1	0
0101	1000	0	0	1
1010	0011	1	0	0
1001	1001	0	1	0

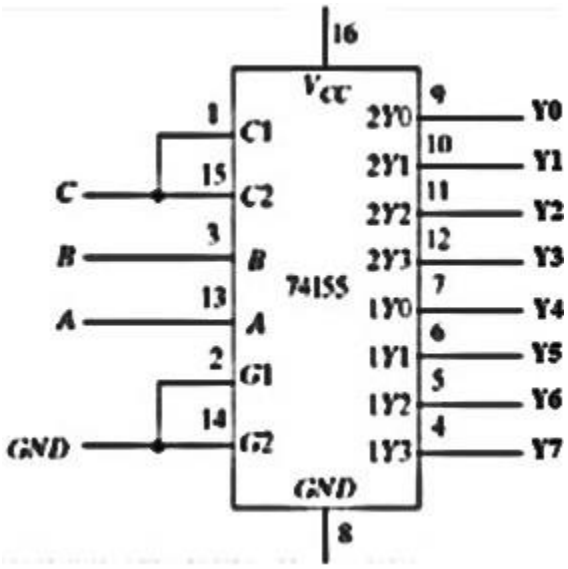
Experiment No.- 5 (Comparators and Decoders)

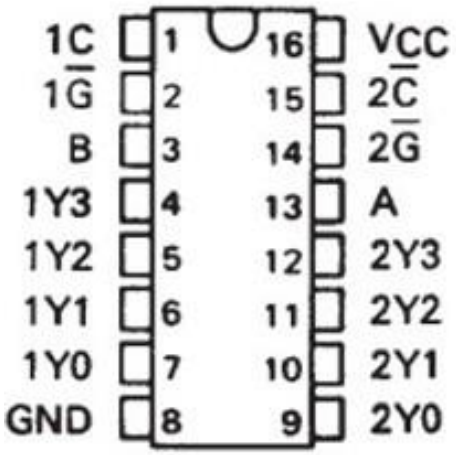
Name : Arshdeep Singh **ID Number :** 2020A7PS0144

Q: Name the gates that can be used as one-bit comparators.
A: XNOR gate.

Run 2: Decoder

Diagram





IC 74155 2-to-8 line decoder

Truth Table

C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Experiment No.- 5 (Comparators and Decoders)

Name : Arshdeep Singh **ID Number :** 2020A7PS0144

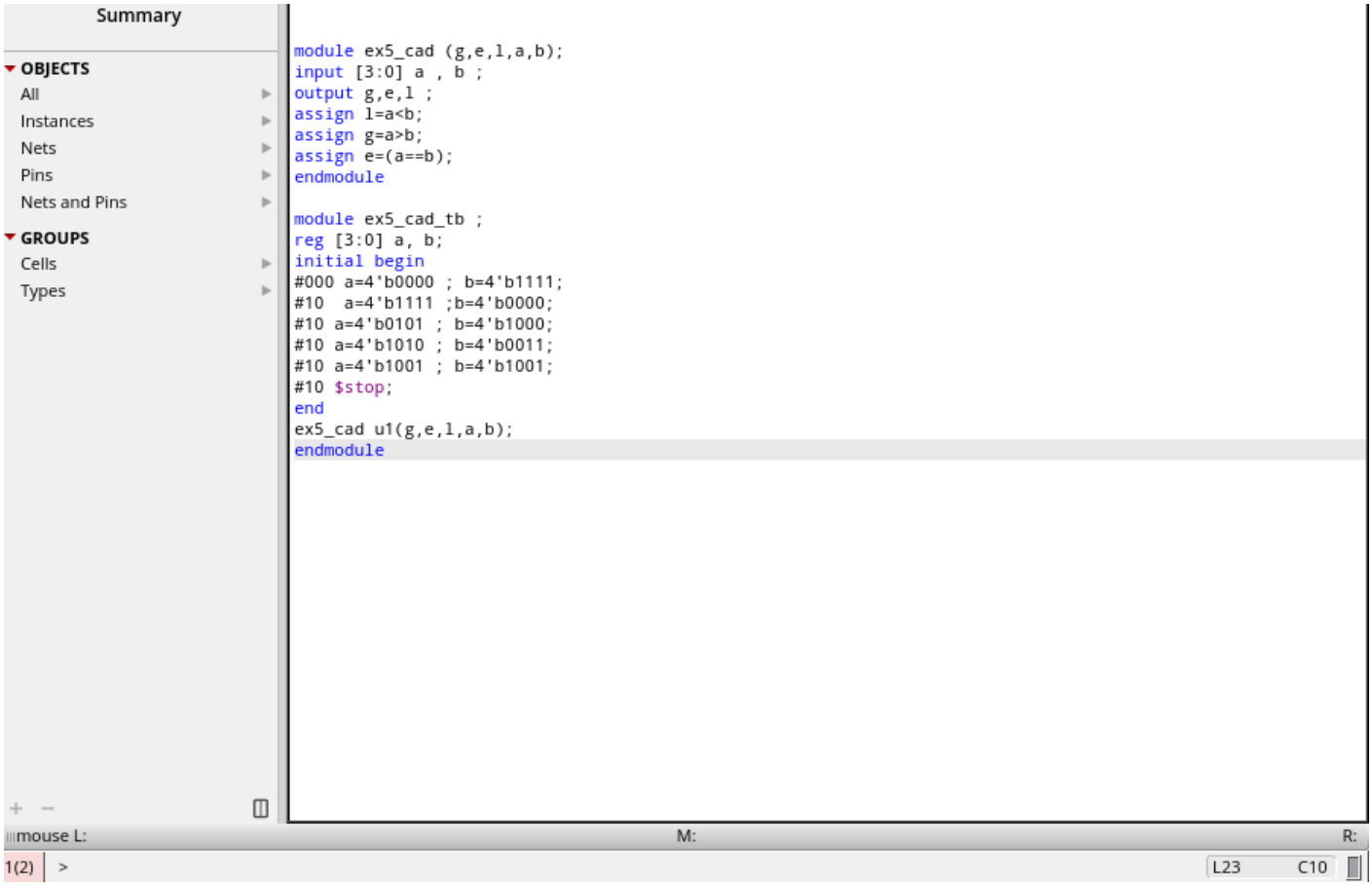
Q: Are the outputs of the decoder active low or active high?
A: Active low .
Q: What external gate would have been used if the IC were to be active high?
A: NAND gate .

Software runs

Run 3: Comparator

1. Write the Verilog code and testbench for 4-bit comparator using data flow modeling. (Hint: Use >, < and = = to compare the two numbers). Complete the truth table.

A: Verilog Code and testbench-



Experiment No.- 5 (Comparators and Decoders)

Name : Arshdeep Singh **ID Number :** 2020A7PS0144

Truth Table

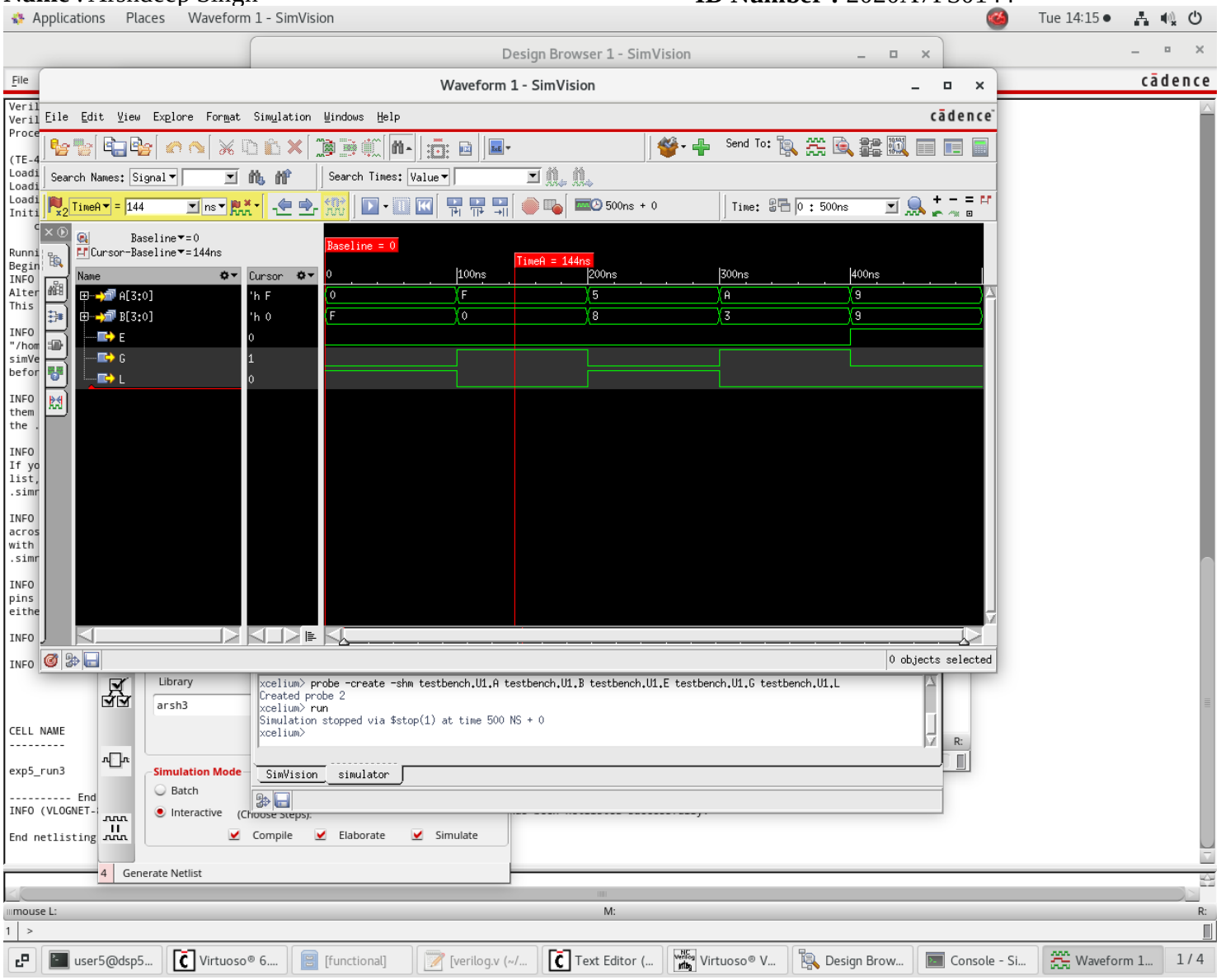
A (A3A2A1A0)	B (B3B2B1Bo)	A>B G	A=B E	A<B L
0000	1111	0	0	1
1111	0000	1	0	0
0101	1000	0	0	1
1010	0011	1	0	0
1001	1001	0	1	0

Q: Paste the screenshot of waveform window where you get the waveforms for the above code

A:

Experiment No.- 5 (Comparators and Decoders)

Name : Arshdeep Singh **ID Number :** 2020A7PS0144



Experiment No.- 5 (Comparators and Decoders)

Name : Arshdeep Singh **ID Number :** 2020A7PS0144

Run 4: Encoders and Decoders

1. Write the verilog code and testbench for 2:4 decoder using data flow modeling, with active high output. (Hint: part of code is written below; A is input and D is output.). Complete the truth table.

A: Verilog Code and testbench-

PLEASE CHECK LAST PAGE

Experiment No.- 5 (Comparators and Decoders)

Name : Arshdeep Singh **ID Number :** 2020A7PS0144

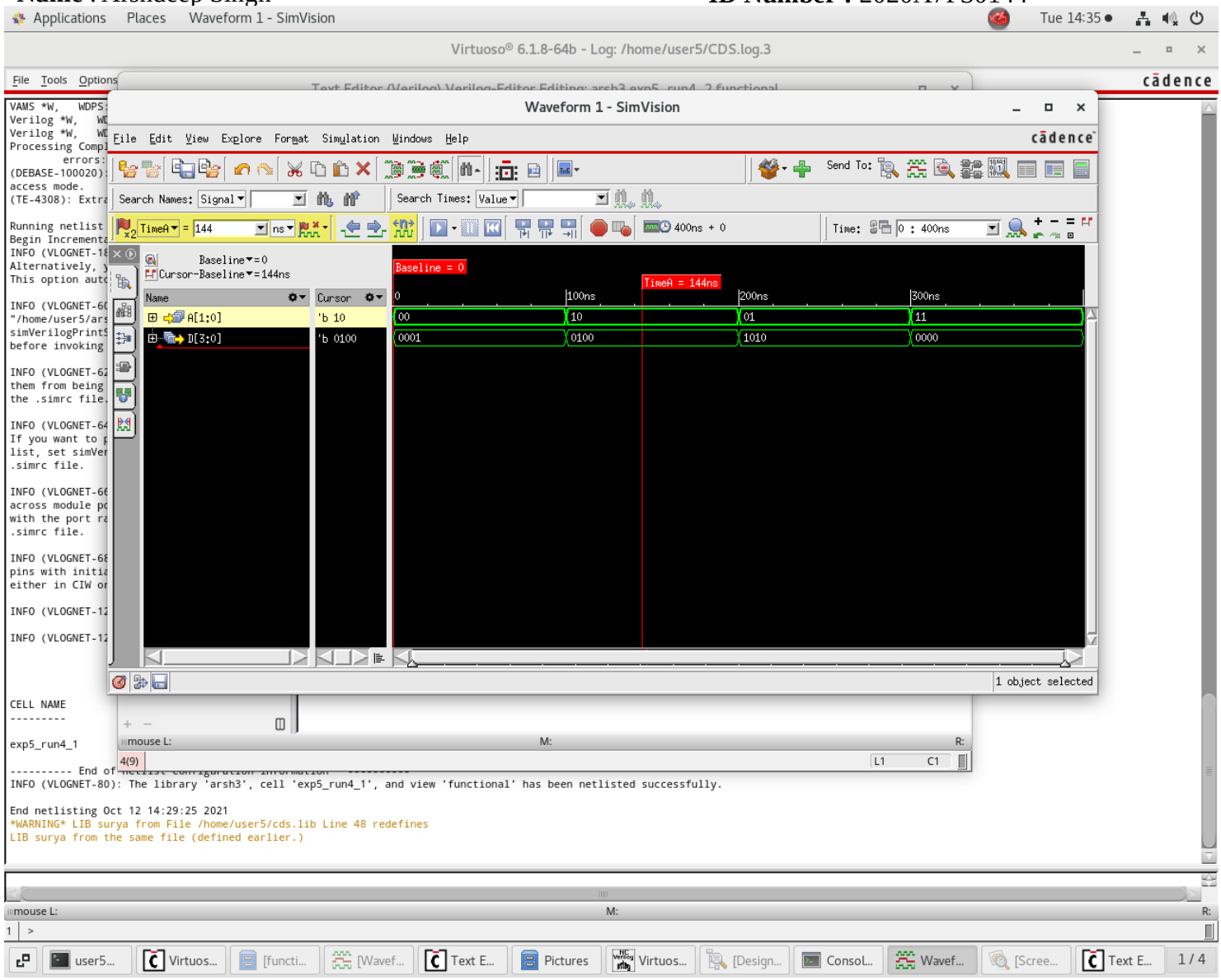
Truth Table

A1	A0	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Q: Paste the screenshot of waveform window where you get the waveforms for the above code.
A:

Experiment No.- 5 (Comparators and Decoders)

Name : Arshdeep Singh **ID Number :** 2020A7PS0144



Experiment No.- 5 (Comparators and Decoders)

Name : Arshdeep Singh **ID Number :** 2020A7PS0144

2. Write the verilog code and testbench for 8-bit priority encoder using behavioral modeling. (Hint: Use **if**, **else** and **else if** statements). Complete the truth table

A: Verilog Code and testbench-

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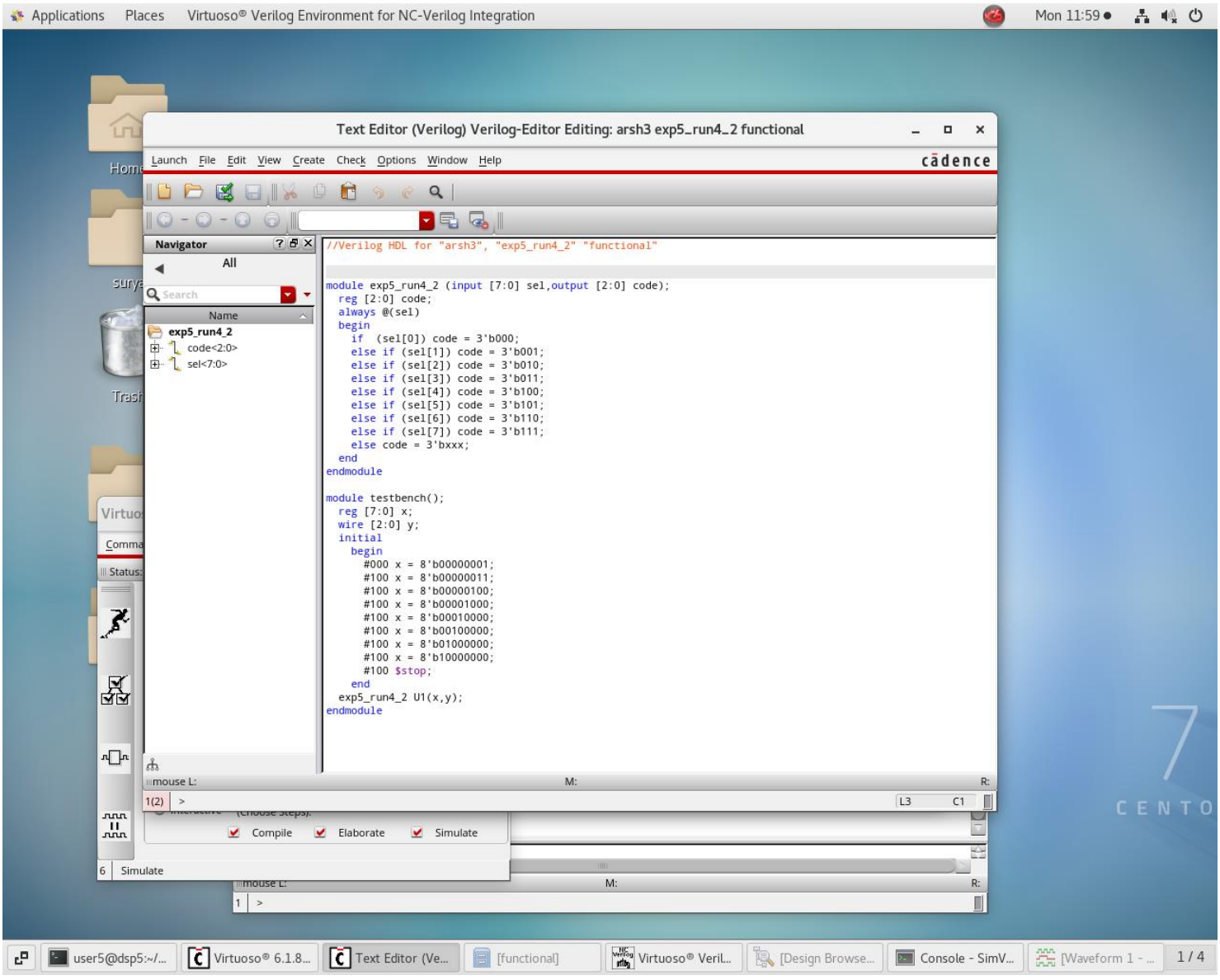


Experiment No.- 5 (Comparators and Decoders)

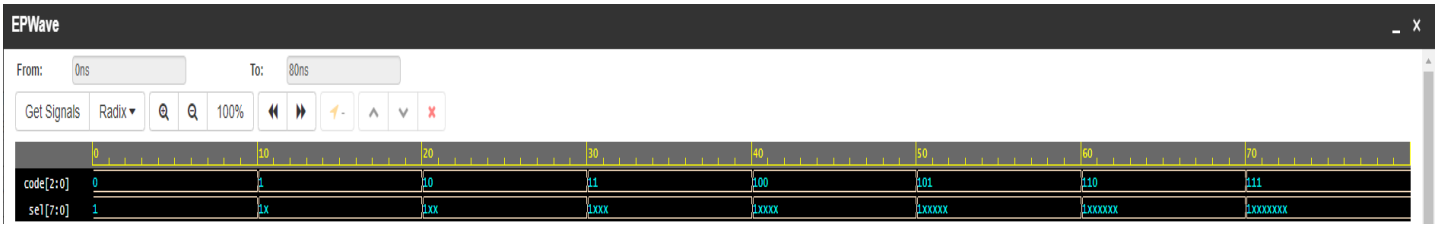
Name : Arshdeep Singh **ID Number :** 2020A7PS0144

Truth Table

D7	D6	D5	D4	D3	D2	D1	D0	Y2	Y1	Y0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	X	0	0	1
0	0	0	0	0	1	X	X	0	1	0
0	0	0	0	1	X	X	X	0	1	1
0	0	0	1	X	X	X	X	1	0	0
0	0	1	x	X	X	X	X	1	0	1
0	1	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	1	1	1

Q: Paste the screenshot of waveform window where you get the waveforms for the above code

A:



Assignment

1. Verilog code and testbench for 3-to-8 decoder using structural modeling (use 2-to-4 decoders as blocks).
Ans: Link1:

2. Write the Verilog code and testbench for 8:3 encoder using behavioral modeling. (Hint: use **case** statements)
Ans: Link2: www.edaplayground.com/x/Prz2

3. Write the verilog code and testbench for 2:4 decoder using data flow modeling, with active high output and active low enable pin. (Hint: use 1-bit enable input pin in all the assign statements like *D[3] = (A&B&~En)*).
Ans: Link3: www.edaplayground.com/x/BS45

4. Write the verilog code and testbench for 4-bit (4-to-2) encoder using behavioral modeling.
Ans: Link4: www.edaplayground.com/x/DbBg

Experiment No.- 5 (Comparators and Decoders)

Name : Arshdeep Singh **ID Number :** 2020A7PS0144