Experiment No. 4

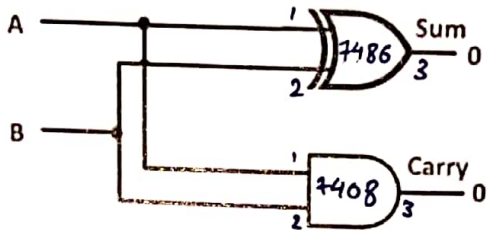
Adders and Subtractors

Hardware runs

Run 1: Half adder (30 mins)

A half adder is a circuit capable of adding two 1-bit numbers to produce a 1-bit sum and a 1-bit carry. Write down th truth table of a half adder and draw its diagram

Diagram



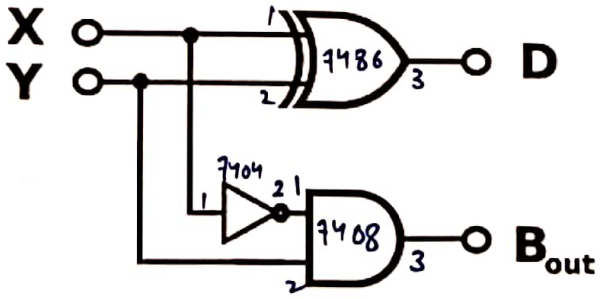
Truth Table

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Run 2: Half subtractor (20 mins)

Analogous to adders, a half subtractor performs subtraction on 2-bits while a full subtractor operates on 3-bits. Write the truth table of a Half subtractor below and Draw the circuit diagram

Diagram



Truth Table

A	B	DIFFERENCE	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Software runs

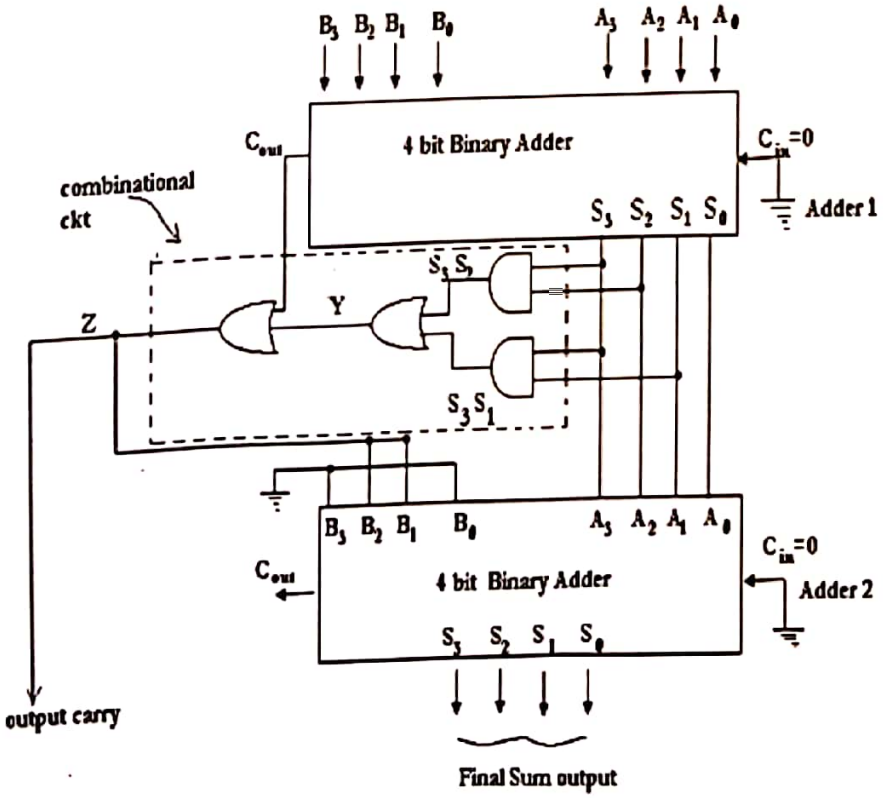
Run 3: Full adder and 4-bit adder (20 Mins)

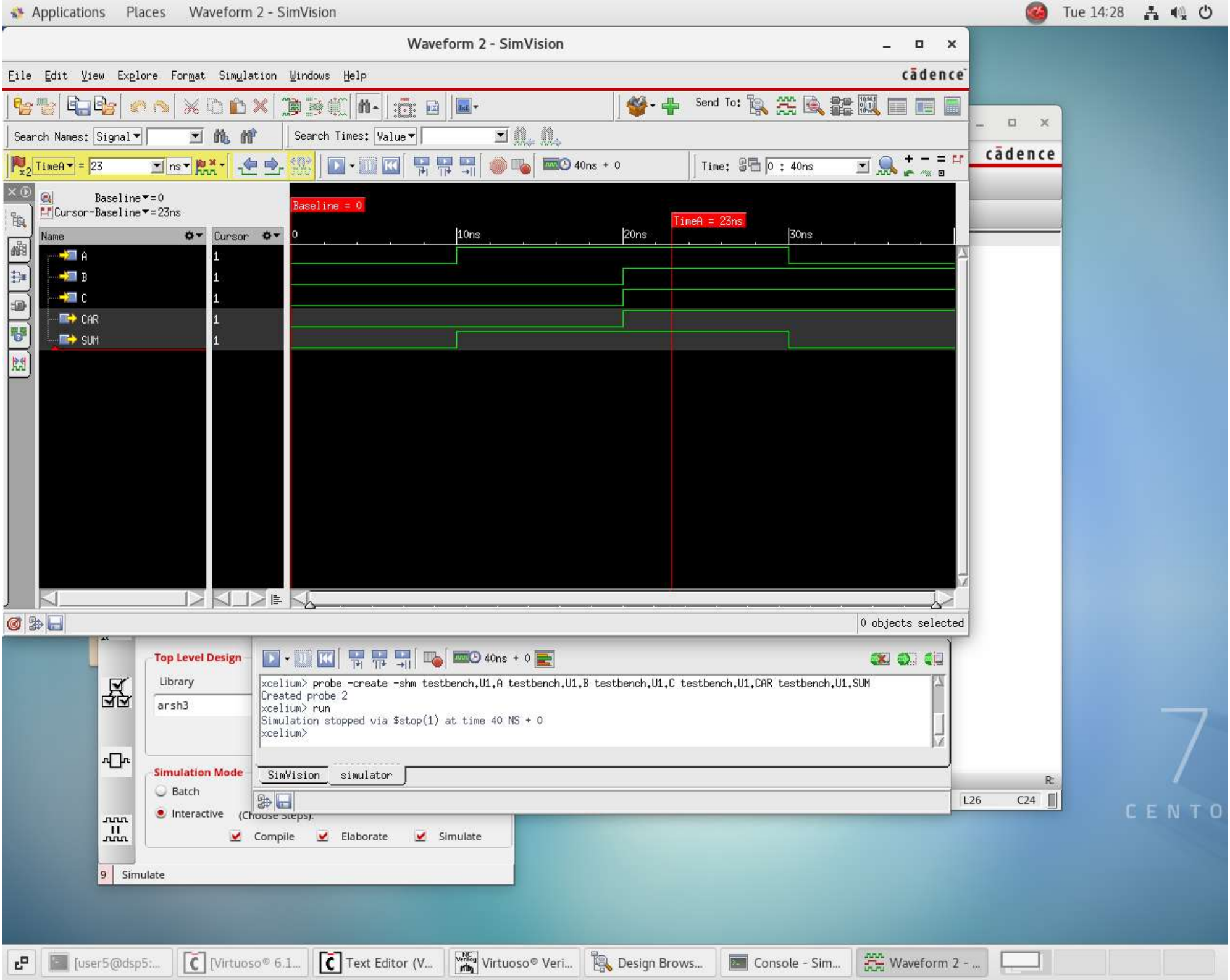
- Write the Verilog code and testbench of Full adder using data flow modeling. (Hint: Sum = A^B^C, Carry = C(A^B) + AB)
- Write the Verilog code and testbench for 4- bit parallel adder using structural modeling, use full adder as a building block defined in above code file.

(This is using or calling module from another file)

Run 4: BCD adder (25 Mins)

- Write the verilog code and testbench for BCD adder using structural modeling, use 4-bit parallel adder and other gates as building blocks. Use parallel adder code from above file)(Hint refer the image below)




Applications
Places
Waveform 2 - SimVision
Tue 14:28
Waveform 2 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Send To:
Search Names: Signal
Search Times: Value
TimeA = 23 ns
40ns + 0
Time: 0 : 40ns
Baseline=0
Cursor-Baseline=23ns
Name
Cursor
A
B
C
CAR
SUM
Baseline = 0
TimeA = 23ns
0
10ns
20ns
30ns
0 objects selected
Top Level Design
Library
arsh3
Simulation Mode
Batch
Interactive
(Choose steps):
Compile
Elaborate
Simulate
9 Simulate
xcelium> probe -create -shm testbench.U1.A testbench.U1.B testbench.U1.C testbench.U1.CAR testbench.U1.SUM
Created probe 2
xcelium> run
Simulation stopped via $stop(1) at time 40 NS + 0
xcelium>
SimVision
simulator
L26
C24
[user5@dsp5:...
[Virtuoso® 6.1...
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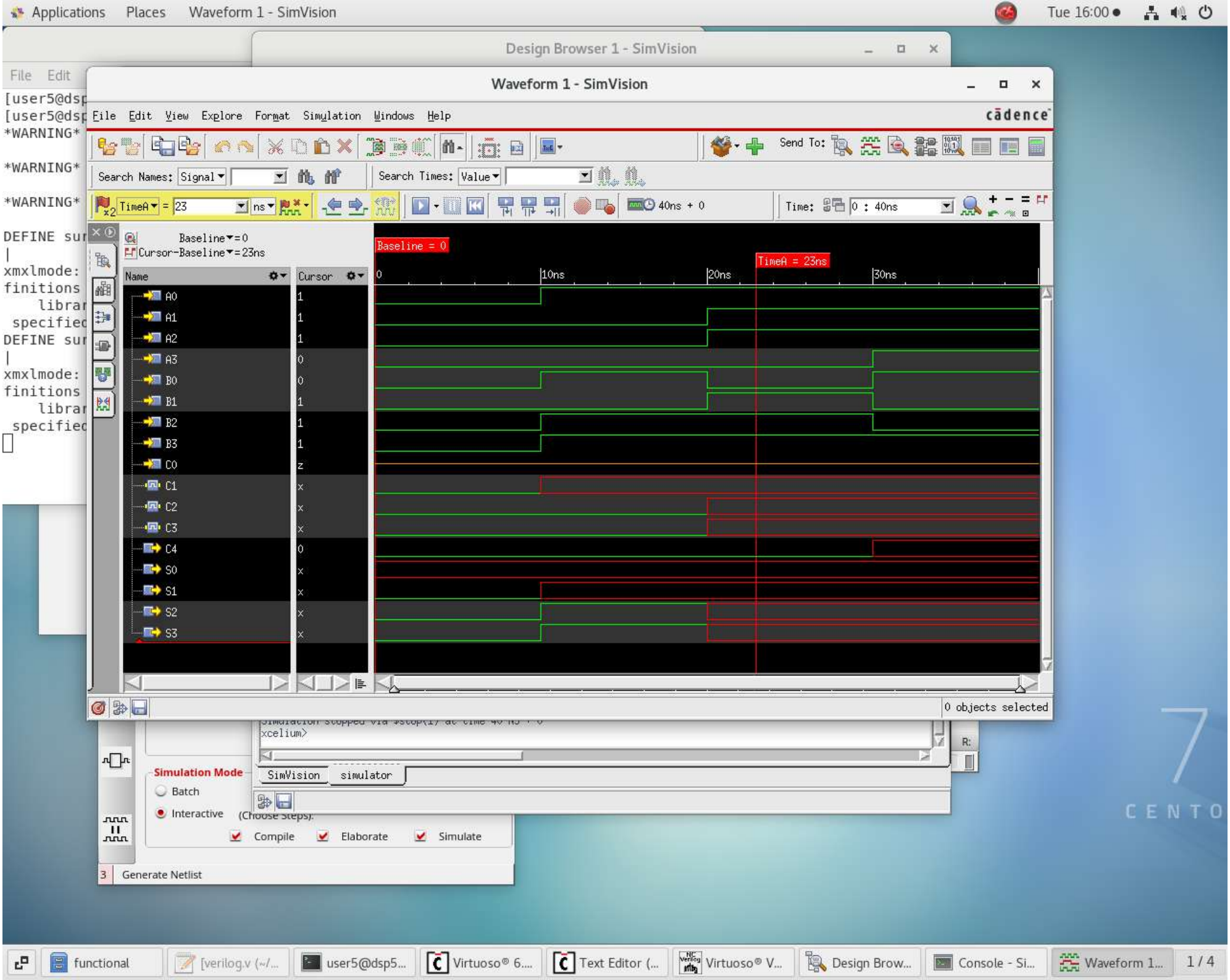
Console - Sim...
Waveform 2 - ...
CENTO


Applications
Places
Waveform 1 - SimVision
Tue 16:00
Design Browser 1 - SimVision
Waveform 1 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Send To:
Search Names: Signal
Search Times: Value
TimeA = 23
ns
40ns + 0
Time: 0 : 40ns
Baseline=0
Cursor-Baseline=23ns
Name
Cursor
A0 1
A1 1
A2 1
A3 0
B0 0
B1 1
B2 1
B3 1
C0 z
C1 x
C2 x
C3 x
C4 0
S0 x
S1 x
S2 x
S3 x
Baseline = 0
TimeA = 23ns
0
10ns
20ns
30ns
0 objects selected
xcelium>
SimVision
simulator
Simulation Mode
Batch
Interactive
Compile
Elaborate
Simulate
3 Generate Netlist
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user5@dsp5...
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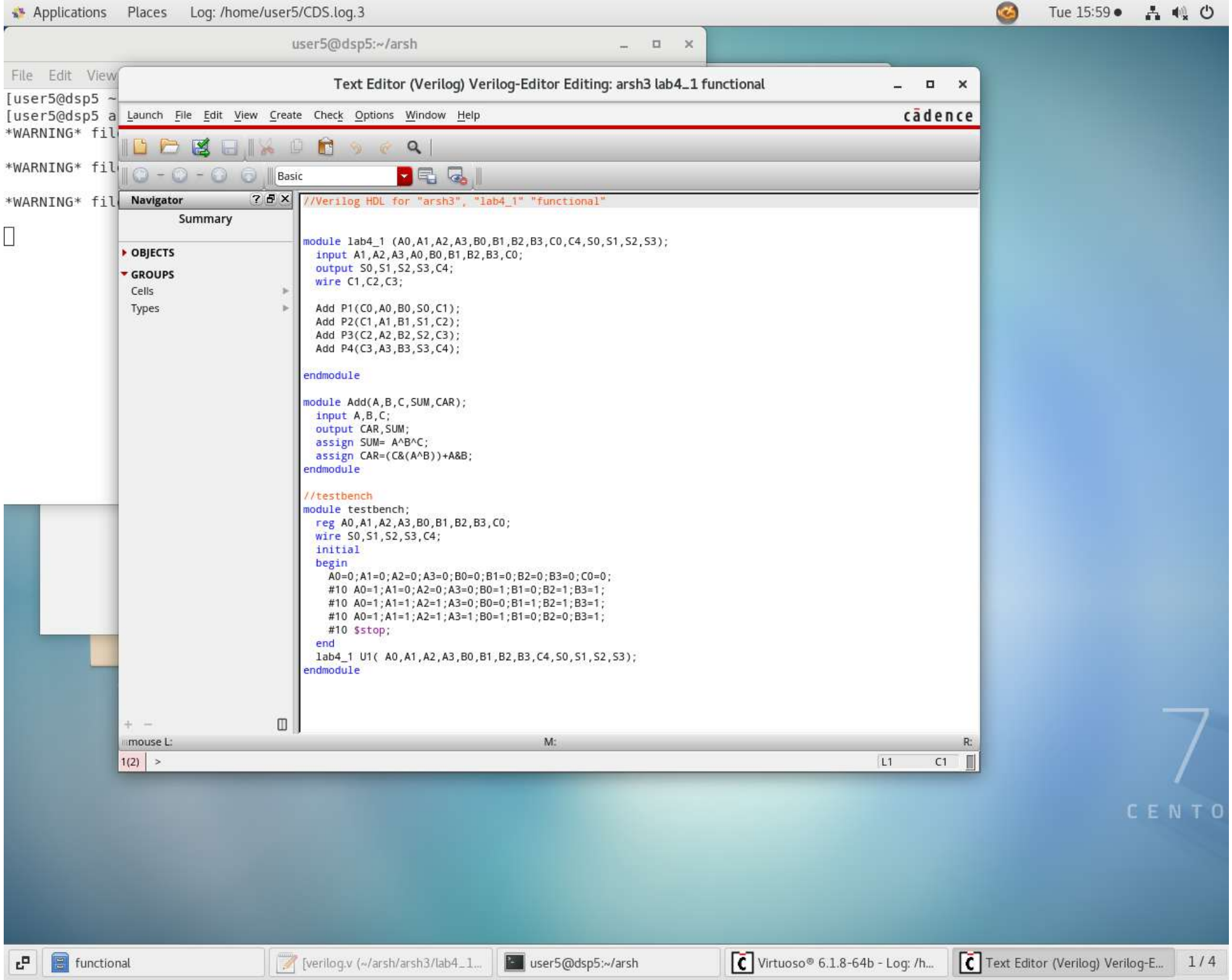
Text Editor (...
Virtuoso® V...
Design Brow...
Console - Si...
Waveform 1...
1 / 4


Applications Places Log: /home/user5/CDS.log.3
Tue 15:59
user5@dsp5:~/arsh
File Edit View
[user5@dsp5 ~
[user5@dsp5 a
WARNING fil
WARNING fil
WARNING fil
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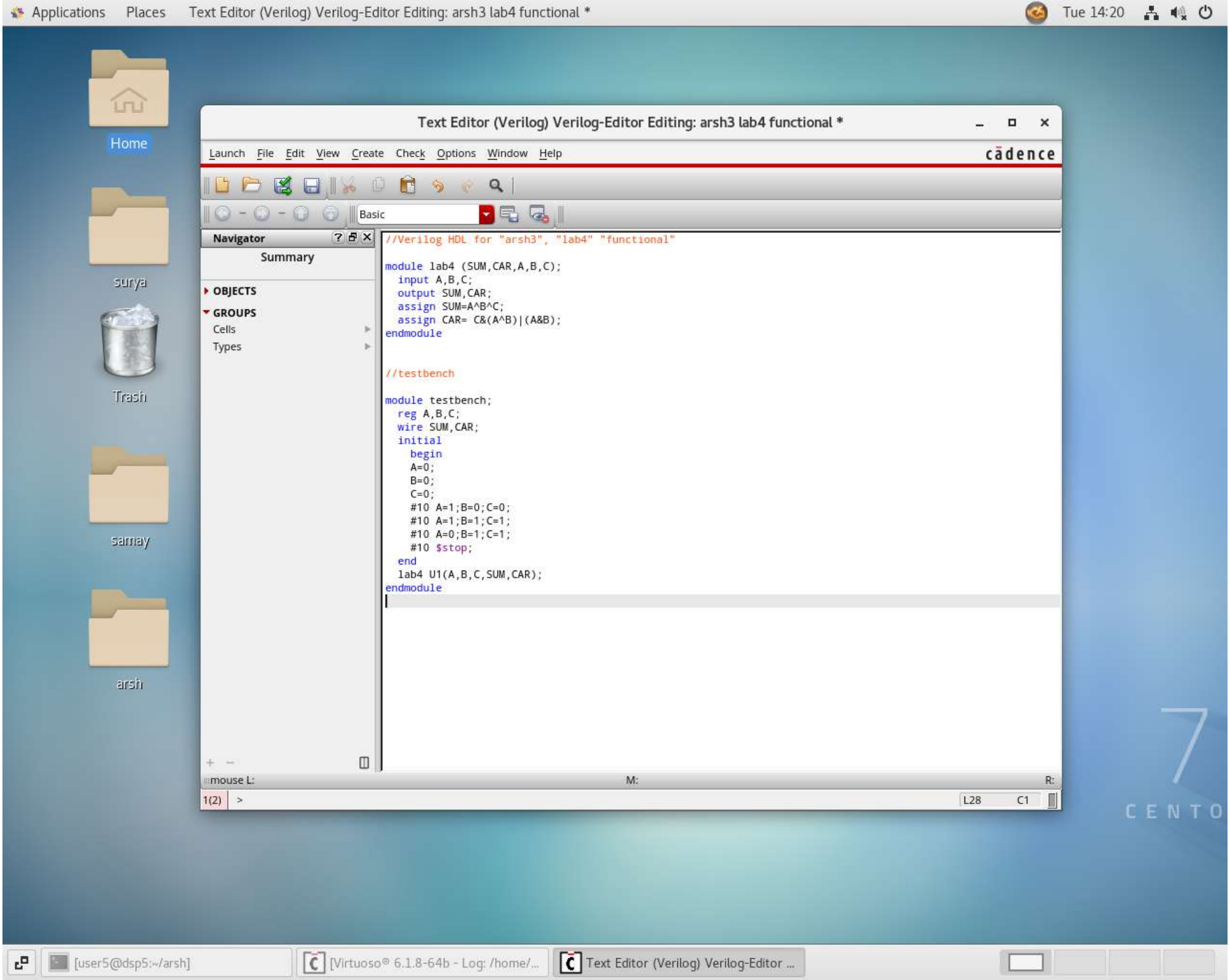
Launch File Edit View Create Check Options Window Help
cadence
Basic
Navigator
Summary
OBJECTS
GROUPS
Cells
Types
//Verilog HDL for "arsh3", "lab4_1" "functional"
module lab4_1 (A0,A1,A2,A3,B0,B1,B2,B3,C0,C4,S0,S1,S2,S3);
input A1,A2,A3,A0,B0,B1,B2,B3,C0;
output S0,S1,S2,S3,C4;
wire C1,C2,C3;
Add P1(C0,A0,B0,S0,C1);
Add P2(C1,A1,B1,S1,C2);
Add P3(C2,A2,B2,S2,C3);
Add P4(C3,A3,B3,S3,C4);
endmodule
module Add(A,B,C,SUM,CAR);
input A,B,C;
output CAR,SUM;
assign SUM= A^B^C;
assign CAR=(C&(A^B))+A&B;
endmodule
//testbench
module testbench;
reg A0,A1,A2,A3,B0,B1,B2,B3,C0;
wire S0,S1,S2,S3,C4;
initial
begin
A0=0;A1=0;A2=0;A3=0;B0=0;B1=0;B2=0;B3=0;C0=0;
#10 A0=1;A1=0;A2=0;A3=0;B0=1;B1=0;B2=1;B3=1;
#10 A0=1;A1=1;A2=1;A3=0;B0=0;B1=1;B2=1;B3=1;
#10 A0=1;A1=1;A2=1;A3=1;B0=1;B1=0;B2=0;B3=1;
#10 $stop;
end
lab4_1 U1(A0,A1,A2,A3,B0,B1,B2,B3,C4,S0,S1,S2,S3);
endmodule
mouse L:
M:
R:
1(2)
L1 C1
CENTO
functional
[verilog.v (~/arsh/arsh3/lab4_1...
user5@dsp5:~/arsh
Virtuoso® 6.1.8-64b - Log: /h...
Text Editor (Verilog) Verilog-E...
1 / 4


Applications
Places
Text Editor (Verilog) Verilog-Editor Editing: arsh3 lab4 functional *
Tue 14:20
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Text Editor (Verilog) Verilog-Editor Editing: arsh3 lab4 functional *
Launch File Edit View Create Check Options Window Help
cadence
Basic
Navigator
Summary
OBJECTS
GROUPS
Cells
Types
//Verilog HDL for "arsh3", "lab4" "functional"
module lab4 (SUM,CAR,A,B,C);
input A,B,C;
output SUM,CAR;
assign SUM=A^B^C;
assign CAR= C&(A^B)|(A&B);
endmodule
//testbench
module testbench;
reg A,B,C;
wire SUM,CAR;
initial
begin
A=0;
B=0;
C=0;
#10 A=1;B=0;C=0;
#10 A=1;B=1;C=1;
#10 A=0;B=1;C=1;
#10 $stop;
end
lab4 U1(A,B,C,SUM,CAR);
endmodule
mouse L:
M:
R:
1(2)
L28 C1
[user5@dsp5:~/arsh]
[Virtuoso® 6.1.8-64b - Log: /home/...
Text Editor (Verilog) Verilog-Editor ...

1. https://www.edaplayground.com/x/BMaW

2. https://www.edaplayground.com/x/axR9

3. https://www.edaplayground.com/x/gMD