BITS-Pilani Dubai Campus
I Sem 2021-22
Digital Design Laboratory / ECE/INSTR/CS F215
Submission Report
Experiment No.- 7 (Latches and Flipflops)

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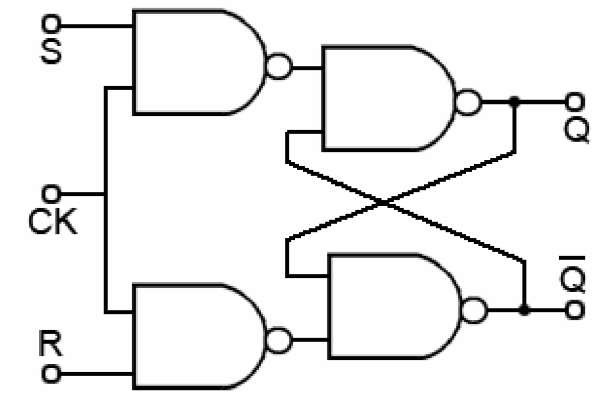
Hardware runs

Run 1: Clocked SR Latch using NAND gates

Diagram



Truth Table

Clock	S	R	Q(t)	Q(t+1)	Operation
0	x	x	x	Q(t)	no change
1	0	0	0	0	no change
1	0	0	1	1	no change
1	0	1	0	0	reset
1	0	1	1	0	reset
1	1	0	0	1	set
1	1	0	1	1	set
1	1	1	0	1	invalid
1	1	1	1	1	invalid

Q: What is the disadvantage with an SR latch?

It is invalid when the input is 1,1. Outputs have to be complement of each other but both nor gates show 1 for this input, so its wastage of one combination

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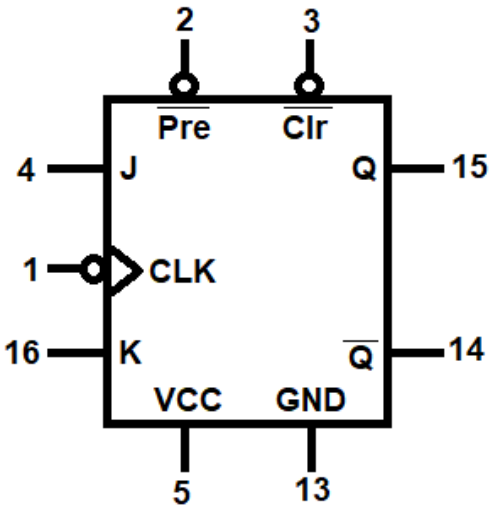
Run 2: JK Flip Flop

Diagram



Truth Table

J	K	Pre	Clr	Clock	Q(t)	Q(t+1)	Operation
x	x	0	0	x	1	1	Invalid
x	x	0	1	x	x	1	Preset
x	x	1	0	x	x	0	Clear
0	0	1	1	Neg trigger	x	Q(t)	No Change
0	1	1	1	Neg trigger	x	0	Reset
1	0	1	1	Neg trigger	x	1	Set
1	1	1	1	Neg trigger	x	Q'(t)	Toggle

Q: Are the preset and clear inputs synchronous or asynchronous.

Asynchronous inputs on a flip flop have control over the outputs (Q and Q') regardless of clock input status. Preset and Clear do not depend upon the clock signals and are thus Asynchronous in nature

Run 3: T Flip Flop (Using JK Flip Flop)

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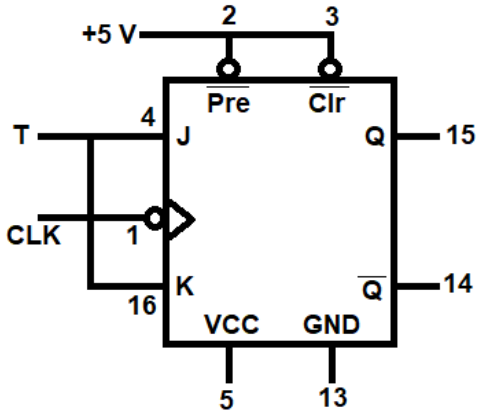
Diagram



Truth Table

T	Clock	Q(t)	Q(t+1)
0	0	x	Q(t)
1	0	x	Q(t)
0	Neg Trigger	x	Q(t)
1	Neg Trigger	x	Q(t)

Software runs

Run 4: SR Latch and Flip-flop

1. Write the Verilog code for clocked SR latch as shown in run-1 of this experiment using four NAND gates (Gate level modeling). Write the testbench also for all possible scenarios and also check for undefined case in waveforms when both S = R = '1'.

A: Verilog Code and testbench-

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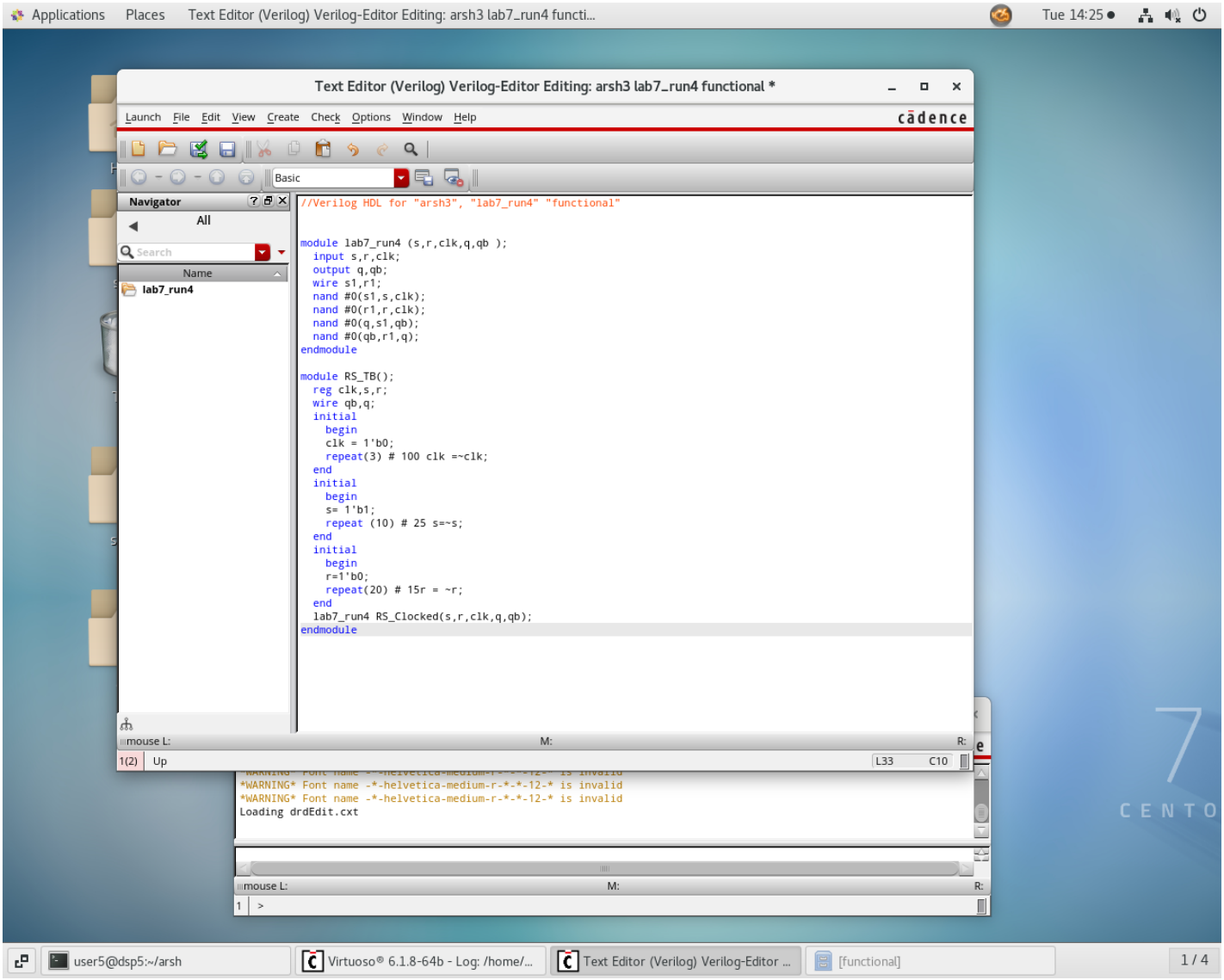
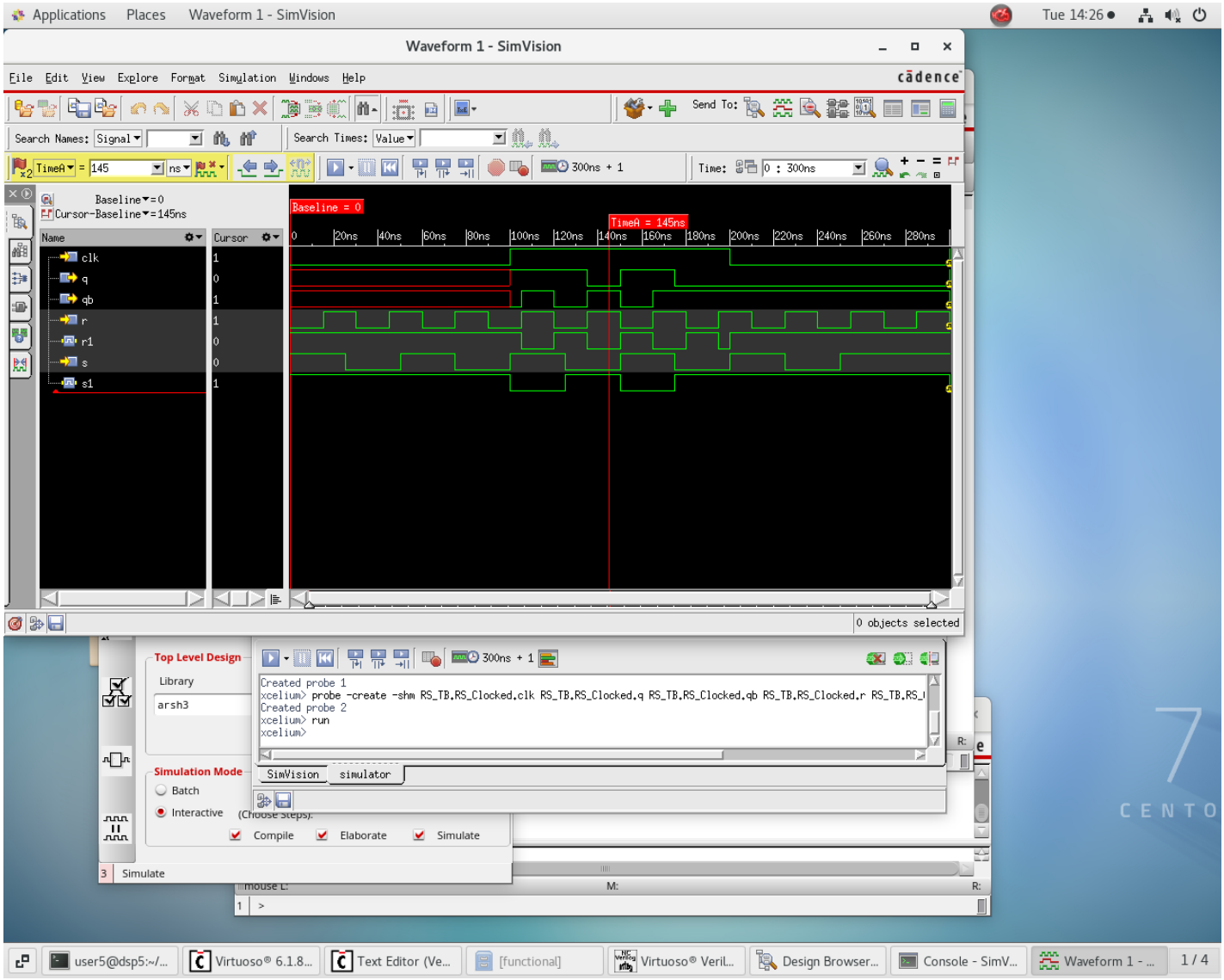


Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.
A:

Experiment No.- 7 (Latches and Flipflops)

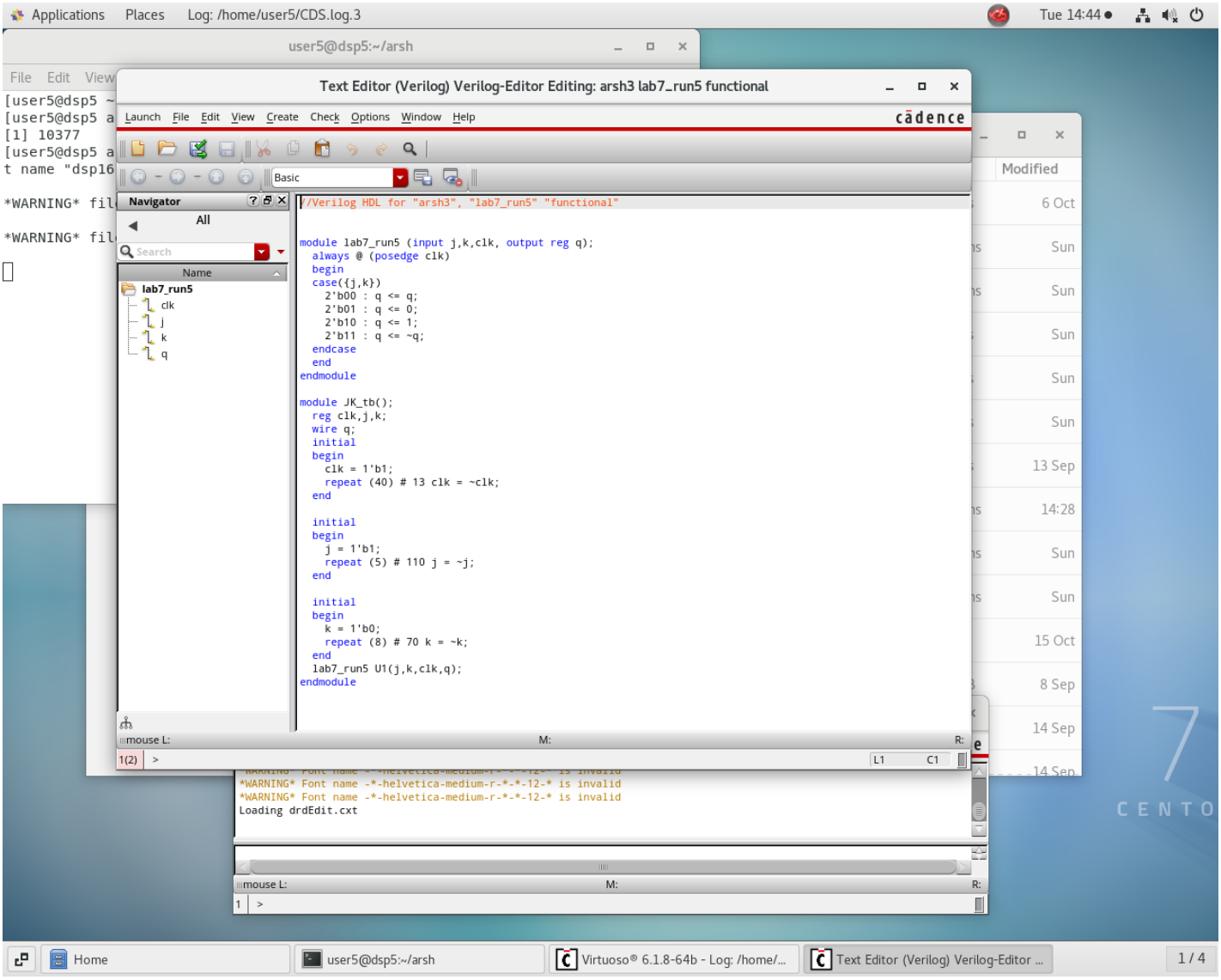


Experiment No.- 7 (Latches and Flipflops)

2. Write Verilog code and testbench for clocked JK flip-flop and compare their response in waveforms. (please use exhaustive testbench).

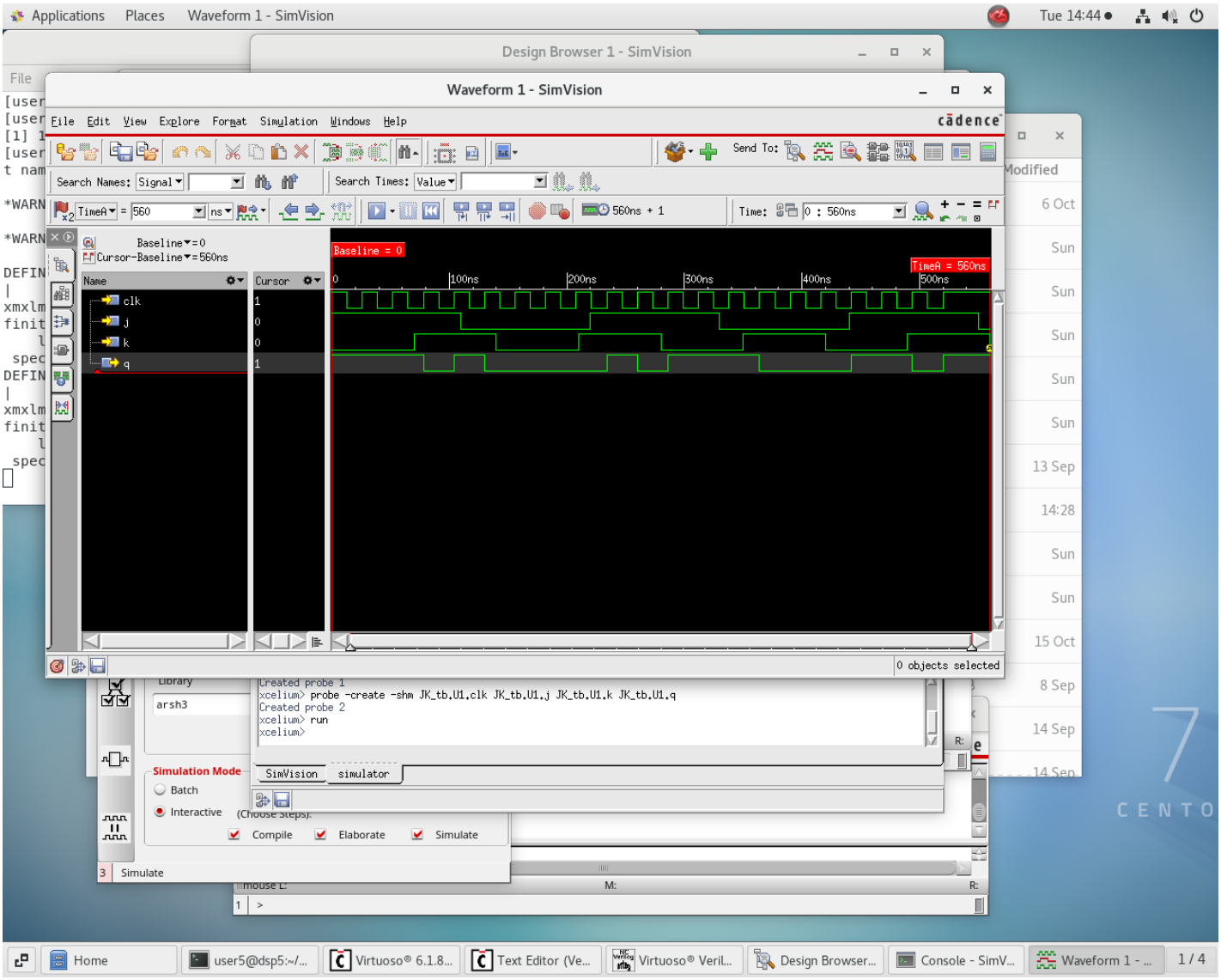
A: Verilog Code and testbench-

Experiment No.- 7 (Latches and Flipflops)



Experiment No.- 7 (Latches and Flipflops)

Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.
A:



Experiment No.- 7 (Latches and Flipflops)

Run 5: D-Flipflop

1. Write Verilog code and testbench for positive edge triggered D-Flip-flop with asynchronous set and reset.

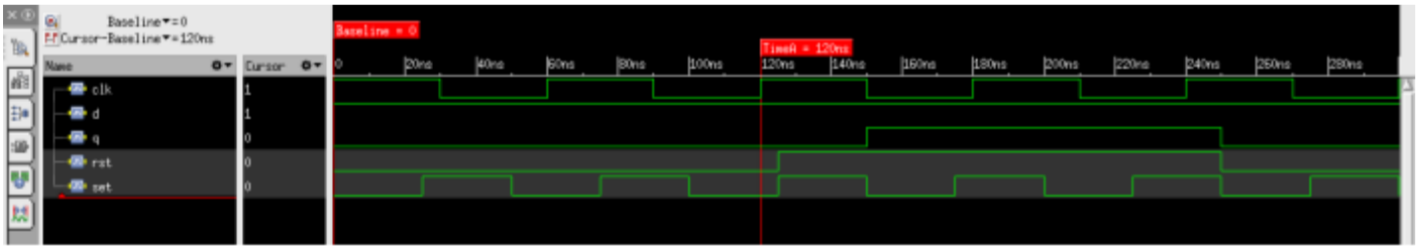
A: Verilog Code and testbench-

```
module run55 ( input d, set_b, rst_b, clk, output reg q);
always @ (posedge clk, negedge set_b, negedge rst_b)
begin
if (rst_b == 1'b0)
q <= 0;
else if (set_b == 1'b0)
q <=1;
else q <= d;
end
endmodule

module testbench();
reg d,set,rst,clk;
wire q;
initial
begin
clk = 1'b1;
repeat(40) #30 clk = ~clk;
end initial begin set = 1'b0;
repeat(20) #25 set = ~set;
end initial begin rst = 1'b0;
repeat(4) #125 rst = ~rst;
end
initial
begin
d = 1'b1;
repeat(20) #25 d = d;
end
run55 g1(d,set,rst,clk,q);
endmodule
```

Experiment No.- 7 (Latches and Flipflops)

Q: Paste the Image of your **Simvision** window where you get the waveforms for the above code.
A:



Assignment All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded '0' marks.

1. Verilog code and testbench for T Flip-Flop for positive edge triggered.
Ans: Link1: https://www.edaplayground.com/x/f4Gy

2. Identify the logic from the Verilog code below. (hint: Create testbench to identify).

```
module circuit_1 (input A,B, output C);
assign C = A ? B : C;
// ? : is the conditional operator (e.g. w=x ? y : z ; if x=true, then w=y if x =false then w=z)
endmodule
```

Ans: Link2: https://www.edaplayground.com/x/7CLC
It is a D Latch Logic

Experiment No.- 7 (Latches and Flipflops)

Self-Practice and self-evaluation

1. Verilog code and testbench for D Flip-Flop for negative edge triggered.
2. Identify the logic for the code below by writing the testbench

```
module circuit_2 (input D_in, en, rst, output q);
    assign q = !(rst ==1'b0) ? 0 : en ? D_in : q;
endmodule
```

3. Identify the logic for the code below by writing the testbench

```
module circuit_2 (output reg q, input d, en);
    always @ (en, d)
    if (en ==1'b1) q &lt;= d;
endmodule
```

4. Identify the logic for the code below by writing the testbench

```
module circuit_3 (q, q_bar, d, set, rst, clk);
    input d, set, rst, clk;
    output reg q;
    output q_bar;
    assign q_bar = !q;
    always @ (posedge clk) // code enters here only at rising edge or positive edge of clock
    // this also makes set and reset signals synchronous to clock edge only
    if (rst == 1'b0) q &lt;= 0; // operator '&lt;=' is the non-blocking assignment operator
    else if (set == 1'b0) q&lt;=1;
    else q &lt;= d;
endmodule
```