CAPITAL UNIVERSITY - KODERMA

VLSI DESIGN - ASSIGNMENT

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1. What is the need for demarcation line?

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All pMOS must lie ononе side of the line and all nMOS will have to be on the other side.

2. Compare NMOS and PMOS transistor.

NMOS and PMOS transistor has the following differences in

common.Fabrication:

In NMOS, the source and the drain are made of n-type semiconductors while the bulk is made ofa p-type semiconductor.
In PMOS, the source and the drain are made of p-type semiconductors while the bulk is made ofan n-type semiconductor.

Majority Carriers:

In NMOS, the majority carriers are
electrons.In PMOS, the majority
carriers are holes.

Size:
NMOS devices are comparatively smaller compared with PMOS devices with complimentaryconducting properties.

Operating Speed:
NMOS devices can be switched faster compared to PMOS devices.

3. Define propagation delay of CMOS inverter.

The propagation delay times are defined as the time delay between the 50% crossing of the input and the corresponding 50% crossing of the output. The rise time and the fall time of the output signal are defined as the time required for the voltage to change from its 10% level to its 90% level(or vice versa).

4. Mention the different types of scaling technique.

Device scaling is an important part of the very large scale integration (VLSI) design to boost up thesuccess path of VLSI industry, which results in denser and faster integration of the devices. As technology node moves towards the very deep submicron region, leakage current and circuit reliability become the key issues. Both are increasing with the new technology generation and affecting the performance of the overall logic circuit. The VLSI designers must keep the balance in power dissipation and the circuit's performance with scaling of the devices. In this paper, differentscaling methods are studied first. These scaling methods are used to identify the effects of those scaling methods on the power dissipation and propagation delay of the CMOS buffer circuit. For mitigating the power dissipation in scaled devices, we have proposed a reliable leakage reduction low power transmission gate (LPTG) approach and tested it on complementary metal oxide semiconductor (CMOS) buffer circuit. All simulation results are taken on HSPICE tool with Berkeleypredictive technology model (BPTM) BSIM4 bulk CMOS files. The LPTG CMOS buffer reduces 95.16% power dissipation with 84.20% improvement in figure of merit at 32 nm technology node. Various process, voltage and temperature variations are analyzed for proving the robustness of the proposed approach. Leakage current uncertainty decreases from 0.91 to 0.43 in the CMOS buffer circuit that causes large circuit reliability.

5. Why NMOS transistor is selected as pull down transistor?

Pull down means bring output to Zero from One too. If input is One for an inverter in CMOS, N transistor will be drive the output to Zero as pull down. If PMOS is used to pull down with source as VSS output will be at By and similarly, NMOS gives VDD minus one threshold as output if sourceconnected to VDD.

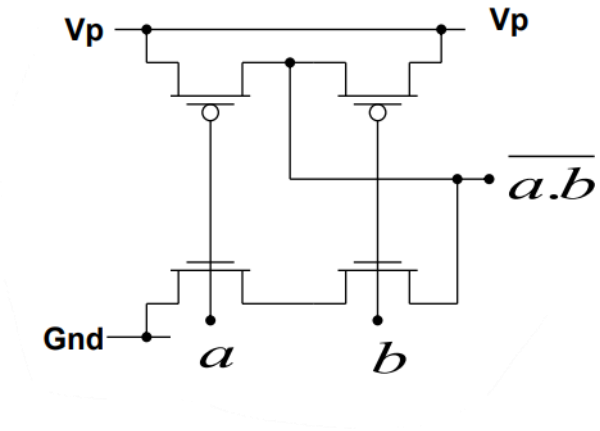
6. Describe the lambda based design rules used for layout.

Lambda-based rules: Allow first order scaling by linearizing the resolution of the

complete waferimplementation.
To move a design from 4 micron to 2 micron, simply reduce the value of lambda.Worked well for 4 micron processes down to 1.2 micron processes.
However, in general, processes rarely shrink uniformly.Probably not sufficient for submicron processes

7. What is stick diagram? Sketch the stick diagram for 2 input NAND gate.

A stick diagram is a kind of diagram which is used to plan the layout of a transistor cell.The stick diagrams uses "sticks" or lines to represent the devices and conductors.



8.Explain the hot carrier effect.

If a MOS transistor is operated under pinch-off condition, also known as ``saturated case'', hot carriers traveling with saturation velocity can cause parasitic effects at the drain side of the channel known as ``Hot Carrier Effects'' (HCE). These carriers have sufficient energy to generate electron-hole pairs by Impact Ionization.The generated bulk minority carriers can either be collected by the drain or injected into the gate oxide. The generated majority carriers create a bulkcurrent which can be used as a measurable quantity to determine the level of impact ionization

9.Draw the DC transfer characteristics of CMOS inverter.

The general arrangement and characteristics are illustrated in Fig.1.1 The current/voltagerelationships for the MOS transistor may be written as,

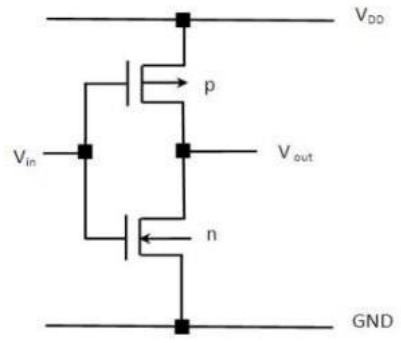


Figure 1.1 CMOS inverter

Where W_n and L_n, W_p and L_p are the n- and p- transistor dimensions respectively. The CMOSinverter has five regions of operation is shown in Fig.1.2 and in Fig. 1.3.

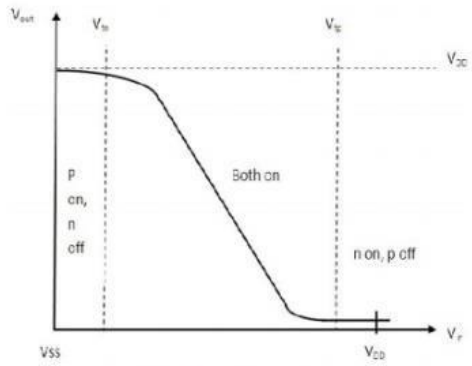


Figure 1.2 Transfer characteristics

Considering the static condition first, in region 1 for which Vin = logic 0, the p-transistor fully turned on while the n-transistor is fully turned off. Thus no current flows through the inverter andthe output is directly connected to VDD through the p-transistor.

In region 5 Vin = logic 1, the n-transistor is fully on while the p-transistor is fully off. Again, nocurrent flows and a good logic 0 appears at the output.

In region 2 the input voltage has increased to a level which just exceeds the threshold voltage of the n-transistor. The n-transistor conducts and has a large voltage between source and drain. Thep- transistor also conducting but with

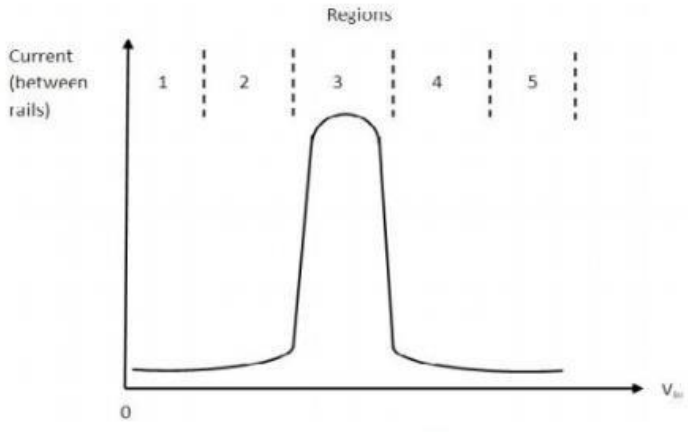


Figure 1.3 CMOS inverter current versus V_{in}

only a small voltage across it, it operates in the unsaturatedresistive region.

In region 4 is similar to region 2 but with the roles of the p- and n- transistors reversed.

The current magnitudes in region 2 and 4 are small and most of the energy consumed in switchingfrom one state to the other is due to the large current which flows in region 3.

In region 3 is the region in which the inverter exhibits gain and in which both transistors are insaturation.

Write

The currents in each device must be the same since the transistors are in

series. So we mayI dsp = - Idsn

Vin in terms of the β ratio and the other circuit voltages

and currentsVin = VDD + Vtp +Vtn $(\beta n + \beta p)^{1/2}$ / 1+ (βn +

$\beta p)^{1/2}$

Since both transistors are in saturation, they act as current sources so that the equivalent circuit inthis region is two current sources so that the equivalent circuit in this region is two current sourcesin series between VDD and VSS with the output voltage coming from their common point.

The region is inherently unstable in consequence and the change over from one logic level to theother is rapid.

Since only at this point will the two β factors be equal. But for βn= βp the device geometries mustbe such that

μ pWp/Lp = μ n Wn/Ln

The motilities are inherently unequal and thus it is necessary for the width to length ratio of the p-device to be three times that of the n-device, namely

Wp/Lp = 2.5 Wn/Ln

The mobility μ is affected by the transverse electric field in the channel and is thus independentonVgs.

It has been shown empirically that the actual mobility is

$\mu = \mu_z (1 - \emptyset (Vgs - Vt)^{-1}$

Ø is a constant approximately equal to 0.05 Vt includes anybody effect, and μ z is the mobilitywith zero transverse field.

10. Name the different operating modes of transistor?

They have four distinct modes of operation, which describe the current flowing through them. (When we talk about current flow through a transistor, we usually mean current flowing fromcollector to emitter of an NPN.)

The four transistor operation modes are:

Saturation -- The transistor acts like a short circuit. Current freely flows from collector to emitter.Cut-off -- The transistor acts like an open circuit. No current flows from collector to emitter.
Active -- The current from collector to emitter is proportional to the current flowing into the base.Reverse-Active -- Like active mode, the current is proportional to the base current, but it flows in reverse. Current flows from emitter to collector (not, exactly, the purpose transistors were designed for).

11. Classify SPICE models for MOS transistor.

SPICE has three built-in MOSFET models, selected by the LEVEL parameter in the model card.

Unfortunately, all these models have been rendered obsolete by the progres- sion to short-channel devices. They should only be used for first-order analysis, and we therefore limit ourselves

• The LEVEL 1 SPICE model implements the Shichman-Hodges model, which is based on the square law long-channel expressions, derived earlier in this chapter. It does not handle short-channel effects.

• The LEVEL 2 model is a geometry-based model, which uses detailed device physics to define its equations. It handles effects such as velocity saturation, mobility degra- dation, and drain-induced barrier lowering. Unfortunately, including all 3D-effects of an advanced submicron process in a pure physics-based model becomes complex and inaccurate.

• LEVEL 3 is a semi-empirical model. It relies on a mixture of analytical and empiri- cal expressions, and uses measured device data to determine its main parameters. It works quite well for channel lengths down to 1 µm.

In response to the inadequacy of the built-in models, SPICE vendors and semi-con- ductor

description of all those would take the remainder of this book, which is, obvi- ously, not the goal. We refer the interested reader to the extensive literature on this topic

12. What are the steps involved in IC fabrication?

Basic steps of IC fabrication The manufacturing of Integrated Circuits (IC) consists of followingsteps

- 1.Wafer production
- 2.Expitaxial growth
- 3. Etching
- 4. Masking
- 5.Doping
- 6.Atomic diffusion
- 7.Ion implantation
- 8.Metallization
- 9.Assambely and packaging

13. Discuss the limitations of the constant voltage scaling.

The disadvantage of constant voltage scaling is that the electric field increases as the minimumfeature length is reduced. This leads to velocity saturation, mobility degradation, increased leakage currents and lower breakdown voltages.

14. Define body effect and write the threshold equation including the body effect.

As we know that the threshold voltage is a function of the total charge in the depletion region (i.e.Qdep). Thus as the body voltage V B drops then depletion charge (Qdep) increases which increasesthe threshold voltage (VTH). This effect is called as the body effect or back gate effect.

15. Design a 3 input NAND gate.

The 3-input NAND Gate
Unlike the 2-input NAND gate, the 3-input NAND gate has three inputs. The Boolean expression ofthe logic NAND gate is defined as the binary operation dot(.). The NAND gate can be cascaded together to form any number of individual inputs. There are 23=8 possible combinations of inputs.

16. List out second order effects of MOS transistor.

The main second order effects are: Velocity Saturation, Threshold Voltage Variations and HotCarrier Effects.

17. Determine whether an NMOS transistor with a threshold voltage of 0.7v isoperating in thesaturation region if GSV=2v and DSV=3v.

18. Summarize the equation for describing the channel length modulation effect in NMOStransistor.

Channel length modulation can be defined as the change or reduction in length of the channel (L)due to increase in the drain to source voltage (VDS) in the saturation region. In large devices, thiseffect is negligible but for shorter devices ΔL/L becomes important.

19. Why the tunneling current is higher for NMOS transistors than PMOS transistors with silicagate?

A key point is that for a pMOS device is typically one order of magnitude smaller than an nMOSdevice with identical and when using SiO [4]. This is due to the much higher energy required forhole tunneling in SiO and the fact that there are very few electrons associated with a pMOS device.

20. Consider the NMOS transistor in 180nm process with a nominal threshold voltage of 0.4vand dopinglevel of 8x1017cm-3 . Propose the body voltage.

21. Describe path logical effort.

The path effort is expressed in terms of the path logical effort G (the product of the individual logical efforts of the gates), and the path electrical effort H (the ratio of the load of the path to itsinput capacitance).

22. List the methods to reduce dynamic power dissipation.

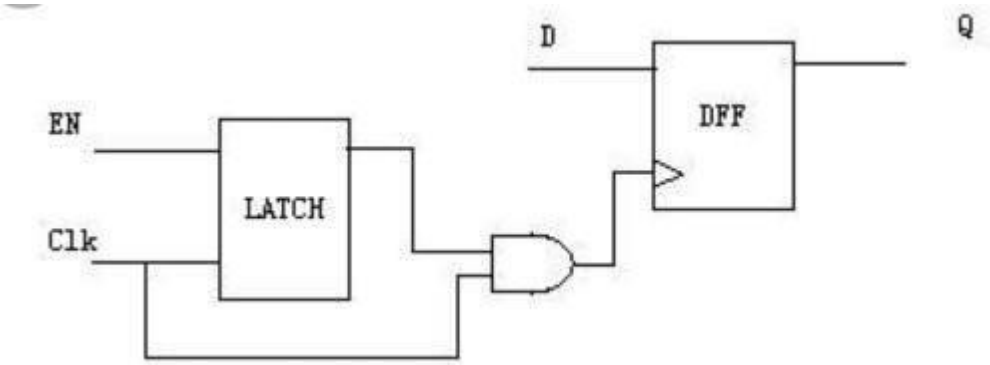
Due to increase of rate in frequency,the power dissipation of circuit will increase which will resultin increase in leakage,increase of cost,larger space area within a

given chip and due to that the overall quality of chip will decrease.

Hence due to that reduction in power is a important factor and for that number of low powertechniques has been adopted.

The following are some of the methods to reduce power

dissipation:-1] Clock gating:-



In general two kinds of power dissipation occured,one is static and the other is dynamic innature.Static power can be negelcted.

In the above circuit,due to switching of states increase of dynamic power dissipationoccurs.Dynamic power is the sum of transient power consumption and capacitive
load power consumption.This can be reduced using clock gating technique which increases theoverall capacitance of the clock tree.

One thing to take care is that clock gating circuits is often prone to glitches and that is whya latch has been introduced in the circuit which will take care of it.

2] Encoding Techniques:-

There are different encoding techniques which should be employed in order to reduce power.

- Proper use of don't care encoding helps in reducing state transitions which ultimately savespower.
- If the number of flip flops are more,number of states will also increase and hence Grayencoding should be used instead of binary encoding wherever applicable.
- LFSR should be used wherever needed in order to reduce power.

3] Frequency Application:-

In a larger subsystem or SOC,there are various components and blocks which should not berequired to be run with same frequency.

Components like Processors or interface agents like AXI or AHB can run with higher frequency butlower frequency blocks like APB,SPI can run with low frequency.

So by normalising the frequency and providing different frequencies to different frequency cansave a lot of power.

4] Operand Isolation:-

This is one of the most useful technique to reduce power dissipation.

If a circuit states are changing continuously depending on its input but as a designer we need to beconcerned with the output once in some clock cycle then we can hold the input by inserting some combinational logic when the output is not being used.This process is known as operand Isolation.

4] SOI:-

SOI stands for Silicon on Insulator which has been used in CMOS circuits and consists of two types of insulators.One is SiO_2 and the other one is sapphire and the advantage of these is the reductionof capacitance between source to body and drain to body region.

Another advantage is the reduction in diffusion capacitance which results in lower subthresholdleakage in circuits which in turn saves more power.

There are two kinds of SOI techniques available,one is PDSOI(partially depleted) and the other oneis FDSOI(Fully depleted).Although FDSOI helps in reduction of tunnelling currents in CMOS but dueto technology constraints PDSOI technique is widely being used.

5] Supply Voltage:-

By controlling the supply voltage (VDD) or by minimising the requirement of supply voltage to adesired extent,the power dissipation within a CMOS Circuit can be minimised.

6] Lowering DIBL:-

In short channel CMOS devices,the source and Drain comes very close to channel region and sharethe charge among themselves.

As the region near the Drain depletion region tend to increase,it reduces the potential barrier.

This problem is known as Drain Induced Barrier lowering and hence by reducing this,powerdissipation within a CMOS Circuit can be reduced.

23.Calculate logical effort and parasitic delay of n input NOR gate.

The delay of a simple logic gate as represented in equation d = gh + p is a simple linear relationship. The fig 22.8 shows this relationship graphically. Delay appears as a function of electrical effort for an inverter and for a two-input NAND gate. The slope of each line is the logicaleffort of the gate.

24. Distinguish between static and dynamic CMOS design.

Static CMOS circuits use or utilise complementary nMOS pulldown. And pMOS pull-up networks to implement logic gates or logic functions in integrated circuits. Dynamic gates use a clocked pMOS

pullup.

25. Explain pass transistor logic.

Pass transistor logic (PTL) describes several logic families used in the design of integrated circuits.It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages.

26. Design an AND gate using pass transistor.

27. Justify why the interconnect increase the circuit delay.

Interconnect delay becomes a more dominating component of circuit delay as feature size continues to decrease, performance-driven placement is increasingly important. However, the delay of a net heavily depends on other factors like routing, buffering, driver size, wire width, andwire spacing.

28. Define critical path

The critical path is the longest path in the circuit and limits the clock speed. When describing a digital circuit there are two other important factors: latency and throughput. Latency is the time needed for an input change to produce an output change; latency can be expressed as a length oftime or, in synchronous circuits, as a certain number of clock cycles. Throughput refers to the rateat which data can be processed.

29. What is Elmore constant?

Time constant for the Elmore delay for an RC interconnect can be calculated by the formula (3) τ Di = $\sum$ i = 1 N R i k C i where is the total number of nodes in the RC equivalent circuit, R i k is the resistance of the portion of the path to the and is the capacitance at node .

30. State the advantages of transmission gates.

The combination of both an PMOS and NMOS in Transmission Gate

arrangement avoids theproblem of reduced noise margin, increase switching resistance and increased static power dissipation (caused by increased Threshold Voltage), but requires that the control and its complement be available.

31. Justify the reasons for the speed advantage of CVSL family.

32. Implement a 2:1 MUX using pass transistor.

A 2:1 multiplexer is shown in Figure below. This gate selects either input A or B on the basis of thevalue of the control signal 'C'.When control signal C is logic low the output is equal to the input A and when control signal C is logic high the output is equal to the input B.

33. Narrate about logical effort.

Logical effort is the ratio of the input capacitance of a given gate to that of an inverter capable of delivering the same output current (and hence is a constant for a particular class of gate and can be described as capturing the intrinsic properties of the gate), and an electrical effort, h, which is the ratio of the input capacitance of the load to that of the gate. Note that "logical effort" does not take the load into account and hence we have the term "electrical effort" which takes the load into account.

34. Summarize the expression for electrical effort of logic circuits.

The electrical effort along a path. through a network is simply the ratio of the capacitance that loads the last. logic gate in the path to the input capacitance of the first gate in the path. We usean upper-case symbol, H, to indicate the path electrical effort.

35. Illustrate the method for reducing energy consumption of a logic circuit.

36. Discuss the advantages of power reduction in CMOS circuits.

Power reduction in CMOS platforms is essential for any application technology. This is a direct result of both lateral scaling—smaller features at higher density, and vertical scaling—shallowerjunctions and thinner layers.

37.Point out the factors that cause static power dissipation in CMOS circuits.

38. Mention the sources of power dissipation.

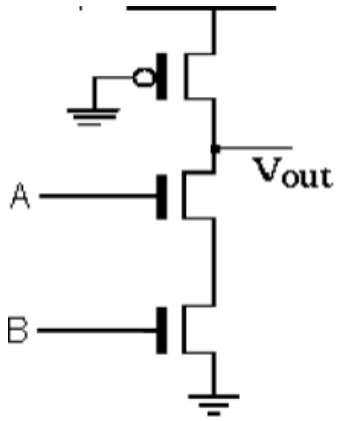
Sources of Power Dissipation Power dissipation in CMOS circuits comes from two components:Dynamic dissipation due to charging and discharging load

capacitances as gates switch “short- circuit” current while both pMOS and nMOS stacks are partially ON Static dissipation due to subthreshold leakage through OFF transistors

39. Draw the pseudo NMOS logic gate.

This logic structure consists of the pull up circuit being replaced by a single pull up pmos whose gate is permanently grounded. This actually means that pmos is all the time on and that now for a n input logic we have only n+1 gates. This technology is equivalent to the depletion mode type and

preceded the CMOS technology and hence the name pseudo. The two sections of the device are now called as load and driver. The Gn/Gp (Gdriver/Gload) has to be selected such that sufficient gain is achieved to get consistent pull up and pull down levels. This involes having ratioed transistor sizes so that correct operation is obtained. However if minimum size drivers are being used then the gain of the load has to be reduced to get adequate noise margin. There are certaindrawbacks of the design which is highlighted next 1. The gate capacitance of CMOS logic is two unit gates but for pseudo logic it is only one gate unit. 2. Since number of transistors per input is reduced area is reduced drastically. The disadvantage is that since the pMOS is always on, static power dissipation occurs whenever the nmos is on. Hence the conclusion is that in order to use pseudo logic a tradeoff between size & load or power dissipation has to be made.



40. If load capacitance increases, what will happen to CMOS power dissipation?

If in cmos circuit you increase the load capacitance assuming you kept other parameters constant.As you increase the load capacitance output current will take more time to charge the capacitor, this will increase the delay transition in logic.

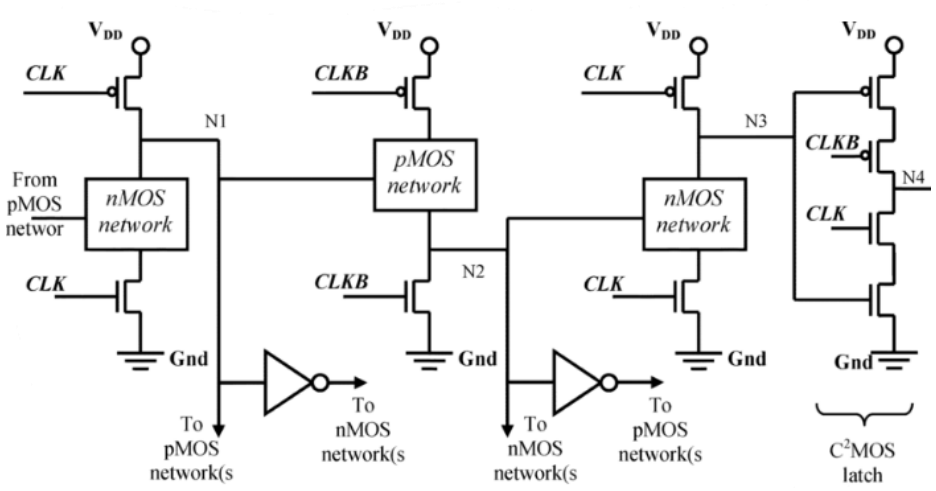
41. List the advantages of differential flip flops.

The advantage of D flip-flops is their simplicity and the fact that the output and input are essentially identical, except displaced in time by one clock period. A

delay flip flop in a circuitincreases the circuit's size, often to about twice the normal. Additionally, they also make thecircuits more complex.

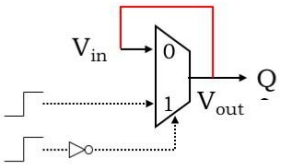
42. Enumerate about NORA CMOS in brief?

NORA or np-CMOS design style has been proposed as a race-free dynamic CMOS technique forpipelined circuits. NORA logic is constructed of cascaded nMOS and pMOS dy- namic logic networks that end on latches.



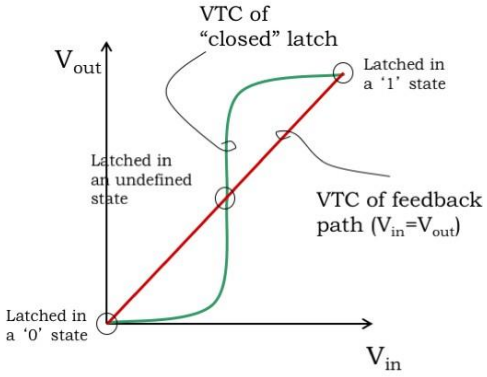
43. Sketch the characteristic curve of meta stable state in static latch.

The Mysterious Metastable State



Recall that the latch output is the solution to two simultaneous constraints:

1. The VTC of path thru MUX; and
2. $V_{in} = V_{out}$



In addition to our expected stable solutions, we find an unstable equilibrium in the forbidden zone called the "Metastable State"

44. Distinguish between a latches and flip flop.

Flip Flop	Latch
Flip-flop is a bistable device i.e., it has two stable states that are represented as 0 and 1.	Latch is also a bistable device whose states are also represented as 0 and 1.

It checks the inputs but changes the output only at times defined by the clock signal orany other control signal.	It checks the inputs continuously and responds to the changes in inputsimmediately.

It is a edge triggered device.	It is a level triggered device.
Gates like NOR, NOT, AND, NAND arebuilding blocks of flip flops.	These are also made up of gates.
They are classified into asynchronous or synchronous flipflops.	There is no such classification in latches.
It forms the building blocks of manysequential circuits like counters.	These can be used for the designing of sequential circuits but are not generallypreferred.
Flip-flop always have a clock signal	Latches doesn't have a clock signal
Flip-flop can be build from Latches	Latches can be build from gates
ex:D Flip-flop, JK Flip-flop	ex:SR Latch, D Latch

45. Classify the sequential elements in reducing the overhead and skew.

46. Define Clock Jitter.

Clock jitter is the deviation of a clock edge from its ideal position in time. Simply speaking, it is theinability of a clock source to produce a clock with clean edges. As the clock edge can arrive within a range, the difference between two successive clock edges will determine the instantaneous period for that cycle. So, clock jitter is of importance while talking about timing analysis. There aremany causes of jitter including PLL loop noise, power supply ripples, thermal noise, crosstalk between signals etc.

47. Summarize the operation modes of NORA logic.

A clock signal CLK and its complement CLKB are uti- lized for the circuit operation which is dividedin two phases, the precharge and the evaluation. In the precharge phase the latch is in the hold mode of operation while in the evaluation phase it is in the transparent mode of operation.

48. Determine the property of clock overlap in the registers.

49. What is Klass semi dynamic flip flop?

Edge-Triggered Semi-dynamic Flip flop (Klass 1998) The primary requirements of a flip-flop inhighspeed digital design are short latency and a simple & robust clocking scheme. These TSPC latches can be combined in various different ways to implement edgetriggered flip-flops.

50. Recall the methods of sequencing static circuit.

50.Recall the methods of sequencing
static circuit.q Combinational logic
– output depends on current
inputsq Sequential logic
– output depends on current and previous inputs
– Requires separating previous, current, future
– Called state or tokens
– Ex: FSM, pipeline
  - If tokens moved through pipeline at constant speed, no sequencing elements would benecessary
  - Ex: fiber-optic cable
  - Light pulses (tokens) are sent down cable
  - Next pulse sent before first reaches end of cable
  - No need for hardware to separate pulses
  - But dispersion sets min time between pulses
  - This is called wave pipelining in circuits
  - In most circuits, dispersion is high
  - Delay fast tokens so they don't catch slow ones.
  - Use flip-flops to delay fast tokens so they move through exactly one stage each cycle.
  - Inevitably adds some delay to the slow tokens
  - Makes circuit slower than just the logic delay
  - Called sequencing overhead
  - Some people call this clocking overhead
  - But it applies to asynchronous circuits too
  - Inevitable side effect of maintaining sequence

51. Write about pipelining?

52.Compare and Contrast Synchronous and Asynchronous Design?

53. Explain simple synchronizer circuit.

54. Formulate hold-time problem which would occur, If a data path circuits uses pulsed latchesin placeof flip flops.

55. Justify the advantages and applications of self-time pipelined circuits.

56. Design a 1-transistor DRAM cell.

57. Illustrate the concept of clock skew in transparent latches.

58. Give the properties of TSPC.

59. Why pipelining is need for of sequential circuits?

60. Draw the schematic of dynamic edge-triggered register.

61. Derive the expression for critical path of an array multiplier

62. Summarize the characteristics of Manchester carry chain adder.

63. List out the components of Data path

64. Why is barrel Shifters very useful in the designing of arithmetic circuits?

65. Interpret a partial product selection table using modified 3-bit booth's recoding multiplication.

66. What is latency?

67. Compare constant throughput/latency and variable throughput latency in active & leakagemode.

68. List the advantages and disadvantages of full adder design using static CMOS.

69. Analyze the concept of Dynamic voltage scaling and list its advantages.

70. Define Clock gating.

71. Creating a schematic for Sleep transistors used on both supply and ground.

72. Examine the need of VTCMOS

73. Give the applications of high speed adder

74. Analyze the inverting property of full adder.

75. How to design a high speed adder?

76. Write about logical and architectural optimization?

77. Classify Power optimization techniques for latency and throughput constrained

design.

78. Write the principle of any one fast multiplier?

79. Sketch a Manchester carry gate.

80. Elaborate the Concept of Transmission gate full adder

81. What is antifuse? State its merits and demerits.

82. Classify the implementation approaches for digital integrated circuits.

83. List out the advantages and disadvantages of cell based design methodology.

84. Narrate about feed-through cells and state their uses.

85. Classify the types of Macro cells.

86. Give a note on Tape out of chip.

87. State the features of full-custom design.

88. Compare semi-custom and full custom design.

89. Describe about standard cell based ASIC design?

90. Define Fuse based FPGA.

91. Name the elements in a configuration logic Block.

92. Develop an array based architecture used in Altera MAX series.

93. Design a primitive gate array cell.

94. Explain configurable logic block.

95. Summarize the functions of Programmable Interconnect Points in FPGA.

96. Identify the issues in implementing Boolean functions on array of cells.

97. Summarize the design steps of Semicustom design flow.

98. Illustrate Composition of generic digital processor.

99. Outline the steps for ASIC design flow.

100. Write the various ways of routing procedure

PART IA

UNIVERSITY EXAM QUESTION PATTERN – 30 MARK (EACH QUESTION CARRIES 6 MARKS)

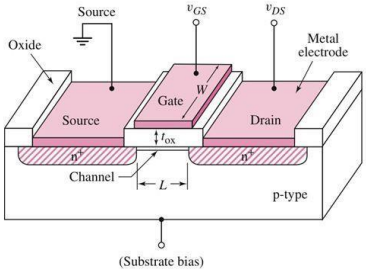
ANSWER ANY 10 QUESTION

1. Illustrate with necessary diagrams Electrical properties of MOS transistor in detail.

It has three terminals, named source, drain and gate. Just like other transistors, such as the BJT, a MOSFET is made of a semiconductor material, most commonly silicon. A semiconductor has very low electrical conductivity (in its pure form),

MOSFET	n-channel Enhancement-Type
Structure	

- p-type substrate : a single crystal silicon wafer that provides physical support of the device.
- Two heavily-doped (n^+) regions created in the substrate to form the **drain** and the **source**.



- A thin (0.02 to 0.1 μm) layer of silicon dioxide (SiO_2) is grown on the surface of the substrate covoring the area between the source and the drain.

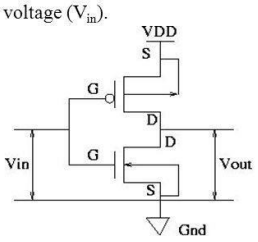
but when you introduce an impurity, the conductivityincreases dramatically.

2. Describe the CMOS inverter and Derive the DC characteristics.

A complementary CMOS inverter consists of a p-type and an n-type device connected in series.The DC transfer characteristics of the inverter are a function of the output voltage (Vout) with respect to the input voltage (Vin).

DC Characteristics of a CMOS Inverter

- A complementary CMOS inverter consists of a p-type and an n-type device connected in series.
- The DC transfer characteristics of the inverter are a function of the output voltage (V_{out}) with respect to the input voltage (V_{in}).



- The MOS device first order Shockley equations describing the transistors in cut-off, linear and saturation modes can be used to generate the transfer characteristics of a CMOS inverter.
- Plotting these equations for both the n- and p-type devices produces voltage-current characteristics shown below.

3. Narrate in detail about ideal I-V characteristics and non-ideal I-V characteristics of NMOSand PMOSdevices.

1. MOS I-V characteristics

- If Vgd < Vt, channel pinches off near drain
- When Vds > Vdsat = Vgs – Vt
- Now drain voltage no longer increases current

$$Ids = \beta\left(\frac{V_{gs} - V_t - V_{dsat}}{2}\right)V_{dsat}$$

$$= \frac{\beta}{2}(V_{gs} - V_t)^2$$

Shockley 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \text{ Cutoff} \\ \beta\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \text{ Linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} < V_{dsat} \text{ Saturation} \end{cases}$$

4. i) Derive the drain current of MOS device in different operating regions.

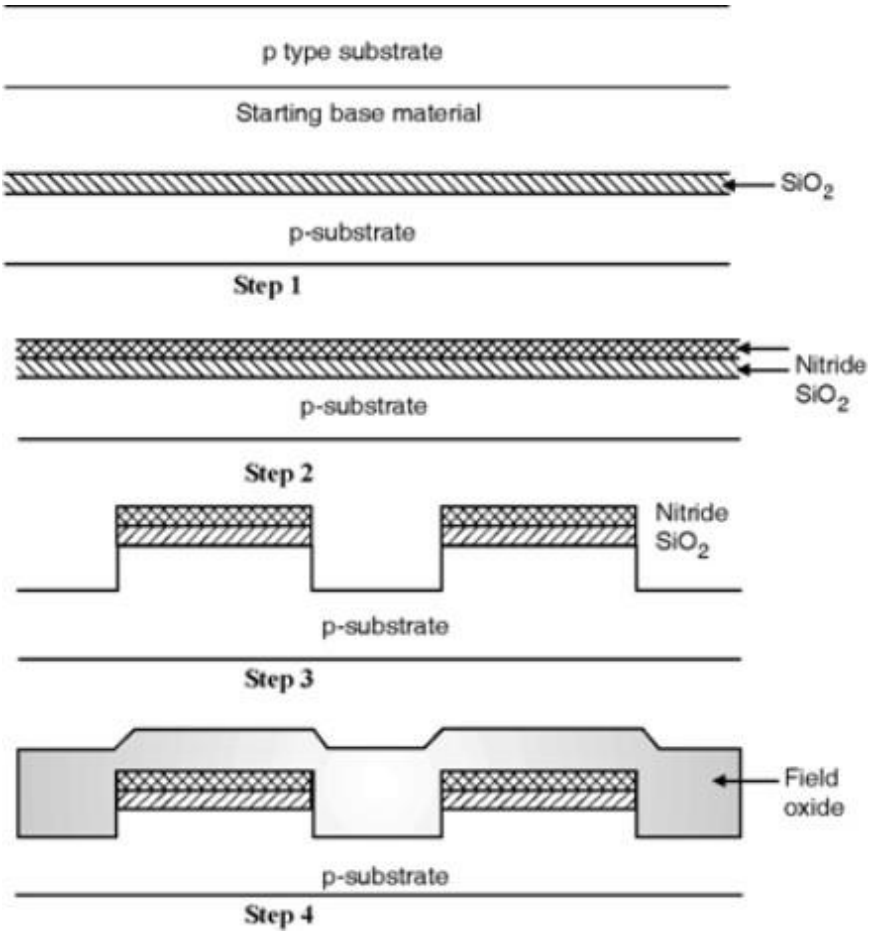
ii) With neat diagram formulate the n-well and channel formation in CMOS process.

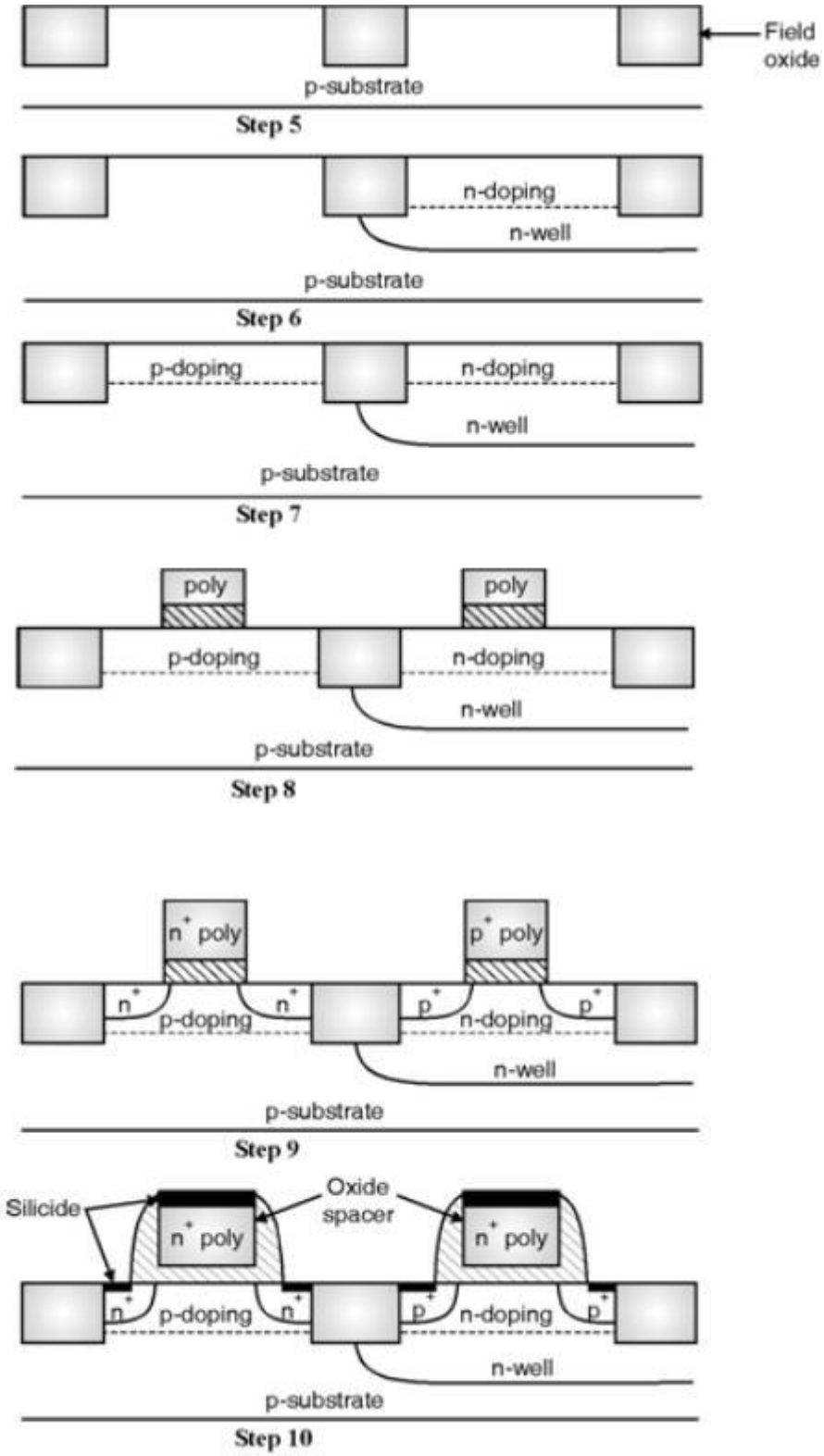
Step 1: First we choose a substrate as a base for fabrication. For N- well, a P-type silicon substrateis selected.
Step 2 – Oxidation: The selective diffusion of n-type impurities is accomplished using SiO_2 as a barrier which protects portions of the wafer against contamination of the substrate. SiO_2 is laid outby oxidation process done exposing the substrate to high-quality oxygen and hydrogen in an oxidation chamber at approximately 1000^0c
Step 3 – Growing of Photoresist: At this stage to permit the selective etching, the SiO_2 layer is subjected to the photolithography process. In this process, the wafer is coated with a uniform filmof a photosensitive emulsion.
Step 4 – Masking: This step is the continuation of the photolithography process. In this step, a desired pattern of openness is made using a stencil. This stencil is used as a mask over the photoresist. The substrate is now exposed to UV rays the photoresist present under the exposedregions of mask gets polymerized.
Step 5 – Removal of Unexposed Photoresist: The mask is removed and the unexposed region ofphotoresist is dissolved by developing wafer using a chemical

such as Trichloroethylene.
Step 6 – Etching: The wafer is immersed in an etching solution of hydrofluoric acid, which removesthe oxide from the areas through which dopants are to be diffused.
Step 7 – Removal of Whole Photoresist Layer: During the etching process, those portions of SiO_2which are protected by the photoresist layer are not affected. The photoresist mask is now stripped off with a chemical solvent (hot H_2SO_4).
Step 8 – Formation of N-well: The n-type impurities are diffused into the p-type substrate throughthe exposed region thus forming an N- well.

Step 9 – Removal of SiO_2: The layer of SiO_2 is now removed by using hydrofluoric acid.
Step 10 – Deposition of Polysilicon: The misalignment of the gate of a CMOS transistor would leadto the unwanted capacitance which could harm circuit. So to prevent this "Self-aligned gate
process" is preferred where gate regions are formed before the formation of source and drainusing ion implantation.
Polysilicon is used for formation of the gate because it can withstand the high temperature greaterthan 8000°c when a wafer is subjected to annealing methods for formation of source and drain.
Polysilicon is deposited by using Chemical Deposition Process over a thin layer of gate oxide. Thisthin gate oxide under the Polysilicon layer prevents further doping under the gate region.
Step 11 – Formation of Gate Region: Except the two regions required for formation of the gatefor NMOS and PMOS transistors the remaining portion of Polysilicon is stripped off.
Step 12 – Oxidation Process: An oxidation layer is deposited over the wafer which acts as a shieldfor further diffusion and metallization processes.
Step 13 – Masking and Diffusion: For making regions for diffusion of n-type impurities usingmasking process small gaps are made.
Using diffusion process three n+ regions are developed for the formation of terminals of NMOS.

Step 14 – Removal of Oxide: The oxide layer is stripped off.
Step 15 – P-type Diffusion: Similar to the n-type diffusion for forming the terminals of PMOS p-type diffusion are carried out.
Step 16 – Laying of Thick Field oxide: Before forming the metal terminals a thick field oxide is laidout to form a protective layer for the regions of the wafer where no terminals are required.
Step 17 – Metallization: This step is used for the formation of metal terminals which can provideinterconnections. Aluminum is spread on the whole wafer.
Step 18 – Removal of Excess Metal: The excess metal is removed from the wafer.
Step 19 – Formation of Terminals: In the gaps formed after removal of excess metal terminals areformed for the interconnections.
Step 20 – Assigning the Terminal Names: Names are assigned to the terminals of NMOS and PMOStransistors.


p type substrate
Starting base material
SiO_2
p-substrate
Step 1
Nitride
SiO_2
p-substrate
Step 2
Nitride
SiO_2
p-substrate
Step 3
Field
oxide
p-substrate
Step 4



5. Mention in detail about second order effects in MOS transistor.

The Second order effects are:-

1) Channel Length Modulation:

There are some subtleties to the operation of the transistor in the saturation region. The length ofthe channel changes with changing values of VDS. As the value of VDS is increased, it causes the depletion region of the Drain junction to grow. This reduces the length of the channel which impacts current. The model current equation must be modified to

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$$

In general, lambda is proportional to channel length. The effects of channel length modulation become more pronounced for smaller feature sizes. Thus, when a high impedance current sourceis required, longer channel transistors are used.

2) Velocity Saturation:

For high VDS, carriers experience higher lateral electric fields. Carrier velocity increases with increasing lateral electric fields. However, once the critical lateral electric field is reached, the velocity of the carriers does not increase any further. This is caused by an increased rate of collision and carrier scattering. The current does not increase at the expected rate. Rather, thecurrent increases very little, if at all.

3) Mobility Degradation:

With increasing VGS, vertical electric fields increase. This increase causes a rise in the number ofcarrier collisions, which degrades carrier mobility. The current flowing through the transistor is therefore than that expected by the ideal models. Mobility decreases with increasing temperature.

4) Threshold Voltage:

The threshold voltage is the value of gate voltage (VGS) at which strong inversion occurs. In other words, this is the voltage at which the transistor begins to conduct current. The Threshold Voltagedepends on:

1.Thickness of the oxide layer: 2.Charge of the impurities trapped between the silicon and theoxide 3.Dosage of ions implanted for threshold adjustment 4.Source to Bulk Voltage

The channel strength and the threshold voltage can be changed through application of appropriate voltage to the body terminal of the MOSFET. This is

known as the body effect.

$$V_t = V_{t0} + \gamma\left(\sqrt{V_{SB} - 2\phi_F} - \sqrt{|2\phi_F|}\right)$$

For gate voltages less than threshold voltage, current drops off exponentially and as feature sizesdecrease the way MOSFETs behave in this region becomes important. The transistor conducts some current before VGS = Vt. This is called sub-threshold conduction.

5) Temperature Dependence:

1. Carrier Mobility: Decreases with temperature
2. Threshold Voltage: Decreases with temperature

3. Junction Leakage: Increases with temperature
4. Velocity Saturation: Occurs sooner with higher temperature
5. Sub-threshold conduction: Increases exponentially with temperature. This means that atlow temperatures, lower threshold voltages can be used.

Most wear out mechanisms are temperature dependent so transistors are more reliable at lowertemperatures.

6) Hot-Carrier Effects:

The hot carrier effect can cause the threshold voltage of a device to drift over time. Smaller devices mean that carriers experience higher electric fields. This is because while device sizes havescaled, power signal voltages have not scaled at the same rate. These high electric fields can causeelectrons to become hot. These electrons have very high energy, and can tunnel into the gate oxide. These electrons, trapped in the gate oxide, can cause a rise in the Vt of a device.

To avoid this, designers use specially engineered drain and source regions to ensure that thestrength of the electric fields are limited so as to avoid the generation of hot carriers.

6. Summarize the following: i) CMOS process enhancements

In the Analog, Digital or RF CMOS integrated circuits along with transistors other elements such asinterconnects, resistors, capacitors are to be integrated on chip. In order to achieve this, enhancements in CMOS process technology is required. The main goals of adding CMOS enhancements are :

(1) To provide on chip capacitors for analog circuits.

(2) To provide on chip resistors.

(3) To provide routing of interconnects.

The enhancements in CMOS technology are :

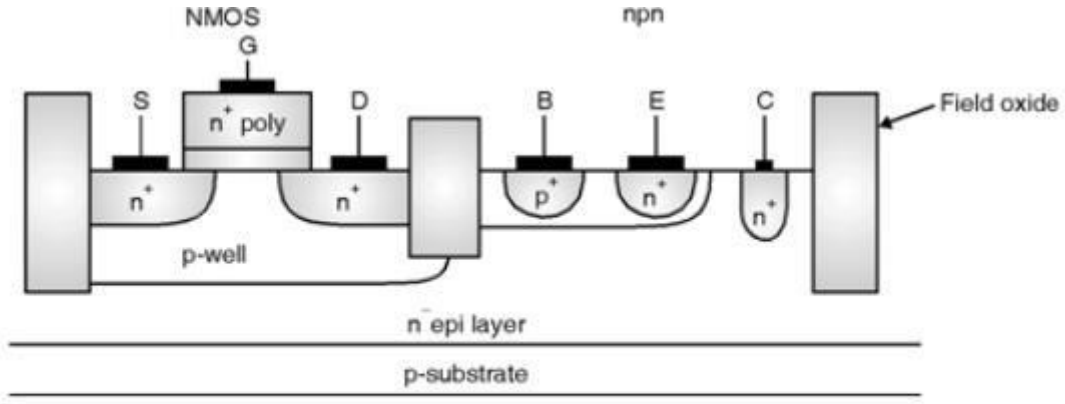
(1) Multilevel metal layers.

(2) Multilevel poly layers.

Transistors :

To enhance the CMOS technology the bipolar transistors can be integrated on chip in CMOStechnology and this forms the BiCMOS technology. Here we will discuss the processing requirements to make these devices on chip.

Figure below shows the cross-section of BiCMOS process in which NMOS and npn transistor arefabricated on the same substrate.



NMOS-npn transistors

The starting material is p substrate on which n type epitaxial layer is grown. To form the NMOS transistor a p well is diffused in selected area. And n^+ diffusions form the source and drain contacts. The nepilar is diffused with the p^+ diffusion which forms the base for the npn transistorboth the devices i.e. NMOS and npn transistors are isolated by field oxide.

Interconnect :

The most important enhancement in CMOS processes is the additions of signal and power supply routing layers. The advantage of this type of routing is it improves power and clock distribution tothe different modules inside the chip. The interconnect layers involved in process are :

(1) Metal interconnect

(2) Polysilicon interconnect

(3) Local interconnect.

The second layer of metal interconnect (Metal 2) is required for digital Integrated circuits. The connection between first metal layer (Metal 1) and second metal layer (Metal 2) is establishedwith the help of via. For high speed chips third metal layer (Metal 3) is also required.

Polysilicon Interconnect layers are used in ICs because of its high melting points

as compare to Al. But the major problem with polysilicon interconnect is it has high sheet resistance because of this for long distance interconnects this provides significant delay.

If silicide is used as a interconnect layer for connecting different cells then it is called as local interconnect. The important advantage of local interconnect is it allows direct connection between polysilicon and diffusion regions due to this metal contacts are eliminated which reducesthe chip area.

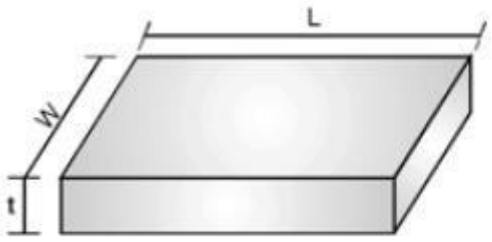
Circuit Elements :

Resistor :

In order to create the on chip resistors n-well or polysilicon materials can be used. The resistanceof a material is a function of the materials resistivity â€˜râ€™ and the dimensions of the material.Figure below shows the slab of the material. The resistance between the two leads A and B is given as,

R = Ã— = Rsheet

where Rsheet is the sheet resistance of material in W/square.

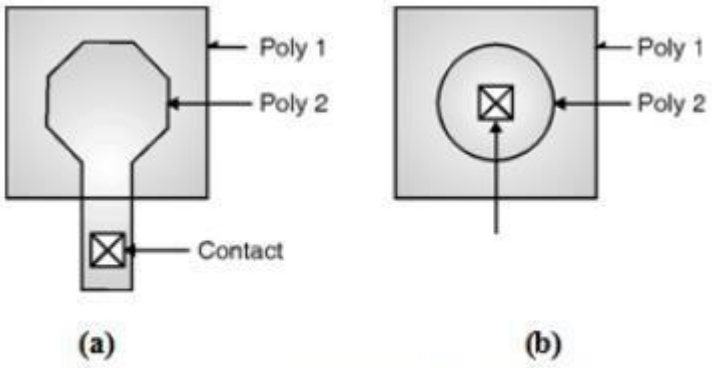


On chip resistance calculation for material slab

Capacitor :

Figure below shows the layout of capacitors used in integrated circuits.

As shown in Figure the capacitor can be formed by adding extra poly silicon layer. In Figure (b) allows contacts to poly to be placed directly on top of the thin oxide which is the isolation between two poly plates. The bottom plate of the capacitor is made using poly 1 while the top plate where area determines the capacitance is made using poly 2. A circular disc is used for poly 2. In Figure (a) the contact to poly is lying over the field region. In this, sharp corners are avoidedin the layout.



Layout of on chip capacitors

ii) Layout design rules.

The layout design rules provide a set of guidelines for constructing the various masks needed inthe fabrication of integrated circuits. Design rules are consisting of the minimum width and minimum spacing requirements between objects on the different layers.

The most important parameter used in design rules is the minimum line width. This parameter indicates the mask dimensions of the semiconductor material layers. Layout design rules are usedto translate a circuit concept into an actual geometry in silicon.

The design rules is the media between circuit engineer and the IC fabrication engineer. The Circuitdesigners requires smaller designs with high performance and high circuit density whereas the IC fabrication engineer requires high yield process.

Minimum line width (MLW) is the minimum MASK dimension that can be safely transferred to thesemiconductor material. For the minimum dimension design rules differ from company to company and from process to process.

To address this issue scalable design rule approach is used. In this approach rules are defined as afunction of single parameter called '□'. For an IC process '□' is set to a value and the design dimensions are converted in the form of numbers. Typically a minimum line width of a process is set to 2□ e.g. for a 0.25 □m process technology '□' equals 0.125 □m.

Layered Representation of Layout :

The layer representation of layout converts the masks used in CMOS into a simple layout levelsthat are easier to visualise by the designers. The CMOS design layouts are based on following components :

(1) Substrates or Wells : These wells are p type for NMOS devices and n type for PMOS devices.
(2) Diffusion regions : At these regions the transistors are formed and also called as active layer.These are defined by n+ for NMOS and p+ for PMOS transistors.
(3) Polysilicon layers : These are used to form the gate electrodes of the transistors.
(4) Metal interconnects layers : These are used to form the power supply and ground rails as wellas input and output rails.
(5) Contact and Via layers : These are used to form the inter layer connections.

7. i) Examine the equation for threshold voltage of a MOS transistor in terms of flat bandvoltage usingnecessary explanations and derivations.

ii) State the step by step derivation of threshold voltage equation of NMOS transistor with andwithoutbody effect.

8. Analyze the following combinational circuits using the CMOS logic:

i) Two input NOR gate. ii) Parity generator ii i) Two input NAND gate. iv) Multiplexers

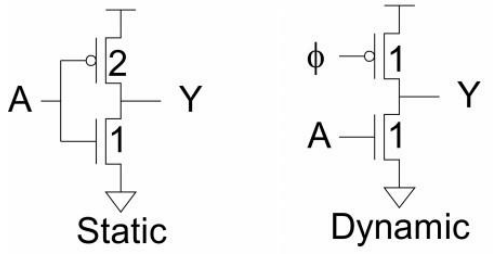
9. Describe in detail about

i) Delay estimation. ii) Logical effort. iii) Transistor sizing.

10. With supporting diagrams, give notes on :

i) Static CMOS ii) Bubble pushing iii) Compound gates.

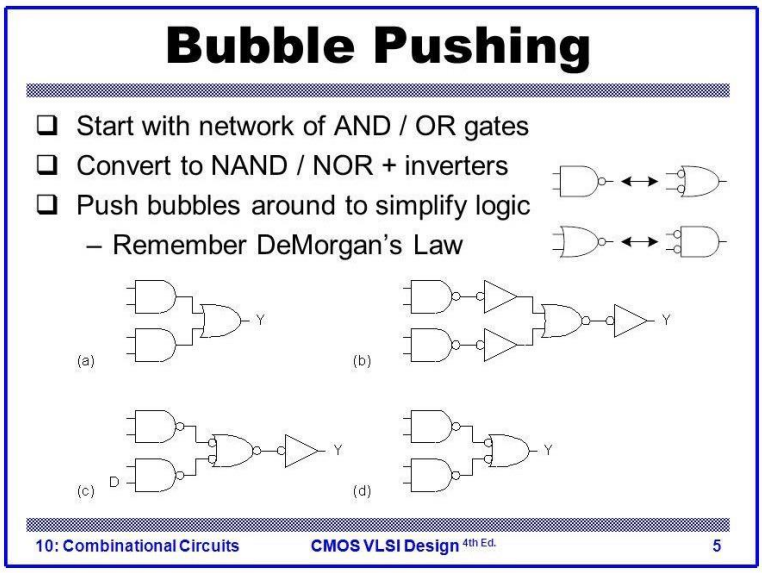
Static CMOS is a logic circuit design technique whereby the output is always strongly driven due toit always being connected to either VCC or GND (except when switching). This design is in contrastto Dynamic CMOS which relies on the temporary storage of signal using various load capacitances.



Bubble Pushing

Bubble pushing is a technique to apply De Morgan's theorem directly to the logic diagram.

Logic gates can be De Morganized so that bubbles appear on inputs or outputs in order to satisfysignal conditions rather than specific logic functions.



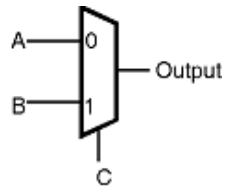
Compound logic gates (sometimes Complex logic gate) are simple devices that function like a fewbasic logic gates combined. Typically made from a few levels of logic, those gates can be used in optimizing various circuits in terms of area and transistors, yielding better performance.

11. Discuss briefly the principle and operation of the following along with its advantages.

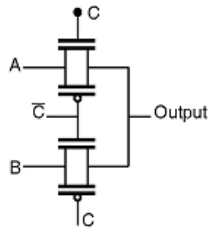
i) Pass Transistor logic ii) Complementary Pass Transistor Logic

12. Write the principle of transmission gate using the design of multiplexer.

MUX using transmission gate :
A 2:1 multiplexer is shown in Figure below. This gate selects either input A or B on the basis of thevalue of the control signal 'C'.When control signal C is logic low the output is equal to the input A and when control signal C is logic high the output is equal to the input B.
A 2 : 1 multiplexer can be implemented using transmission gates. Figure below shows the connection diagram of the 2 : 1 multiplexer using transmission gates. The 2 : 1 MUX selects eitherA or B depending upon the control signal C. This is equivalent to implementing the Boolean function,
F = (A C + B ––C)
When the control signal C is high then the upper transmission gate is ON and it passes A through itso that output = A.



2 : 1 MUX



2 : 1 MUX using transmission gate

When the control signal C is low then the upper transmission gate turns OFF and it will not allow Ato pass through it, at the same time the lower transmission gate is 'ON' and it allows B to pass through it so the output = B.

13. i) Relate with Necessary Diagrams the principle of Zipper CMOS Logic.

ii) Implement AND/NAND gates using Dual-
Rail DominoLogic.

13. Write short notes on:

i) Ratioed Circuits ii) Dynamic CMOS Circuits iii) Keepers iv) Multiple Ouput

Dynamic Logic

Ratioed circuits use weak pull-up devices and stronger pull- down devices. They reduce the inputcapacitance and hence improve logical effort by eliminating large pMOS transistors loading the inputs, but depend on the correct ratio of pull-up to pull-down strength.
Dynamic CMOS logic circuits are mostly used in VLSI chips. It provides highest performance compared to different logic families like TTL, ECL. The noise tolerance of dynamic CMOS logic gatescan be improved because of its faster speed and compact area than the static logic gates.
Keeper circuits are designed to assist in "keeping" the evaluate node charged High if it is suppose

to evaluate High. Therefore, they need to be strong enough to resist noise, leakage, etc. thatwould otherwise cause the node to errantly discharge to a Low value.

Multiple-output domino logic (MODL) is a recently introduced dynamic CMOS logic in which complex gates can have multiple outputs for producing multiple functions. Depending on thedegree of recurrence present in the circuit, this can result in a large reduction in the chip area required for implementing the circuit.

14. Examine with necessary diagrams and expressions:

i) Static power dissipation in CMOS circuits ii) Dynamic power dissipation in CMOS circuits

15. i) Write the expression for minimum possible delay of multistage logic networks.

ii) Design and estimate the frequency of n-stage ring oscillator and construct the ringoscillator froman odd number of inverter.

16. Explain the sequencing methods of sequential staticcircuits.

17. Discuss in detail : i) Synchronous pipelining in sequential circuits.

ii) Asynchronous pipelining in sequential circuits.

18. Write about the latches and flip-flops in design methodology of sequential circuit design

19. i) State and explain the Klass semi dynamic flip flops and differential Flip flops.

ii) Illustrate the enabled latches and flip flops.

20. i) Design a D-latch using transmission gate.

ii) Evaluate a 1-bit dynamic inverting and no inverting register using pass transistor