VLSI DESIGN

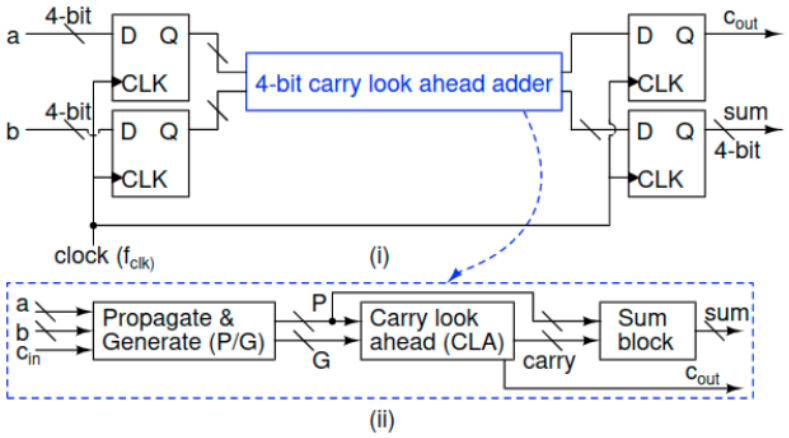
PROJECT

4-BIT CARRY LOOK-AHEAD ADDER

ARSHINI GOVINDU

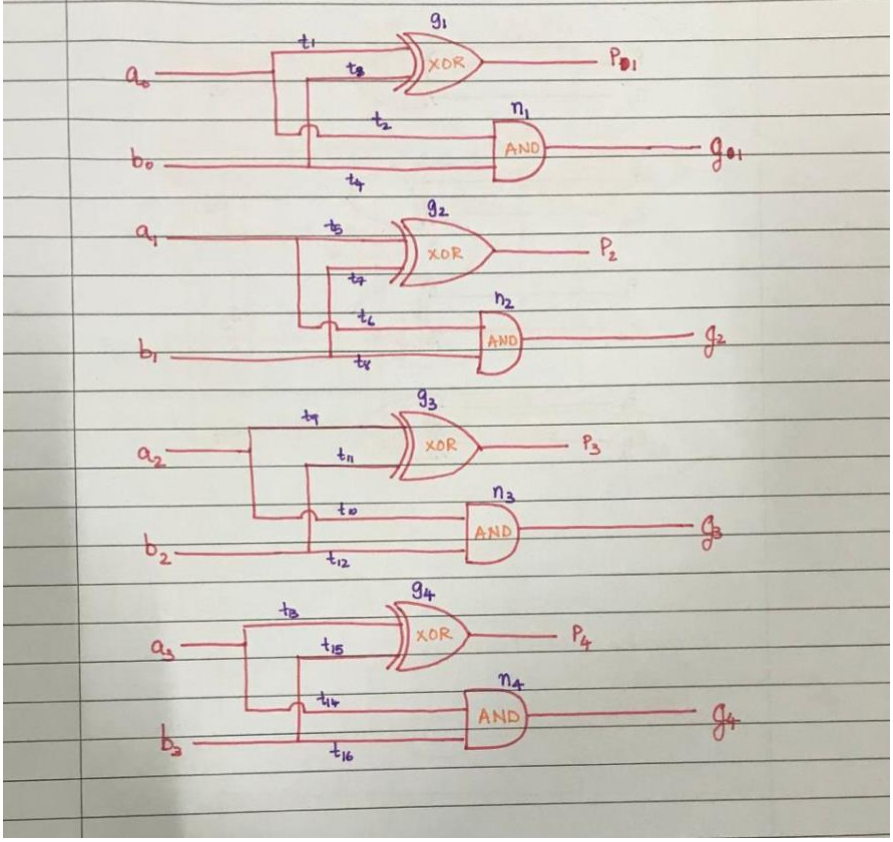
2020102009

Block Structure

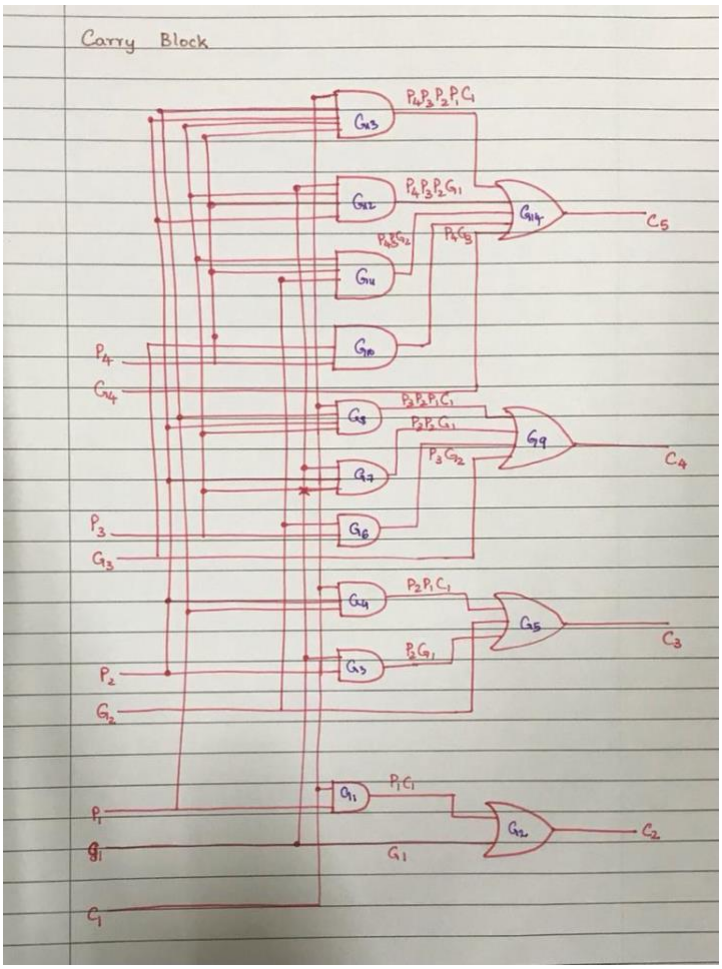


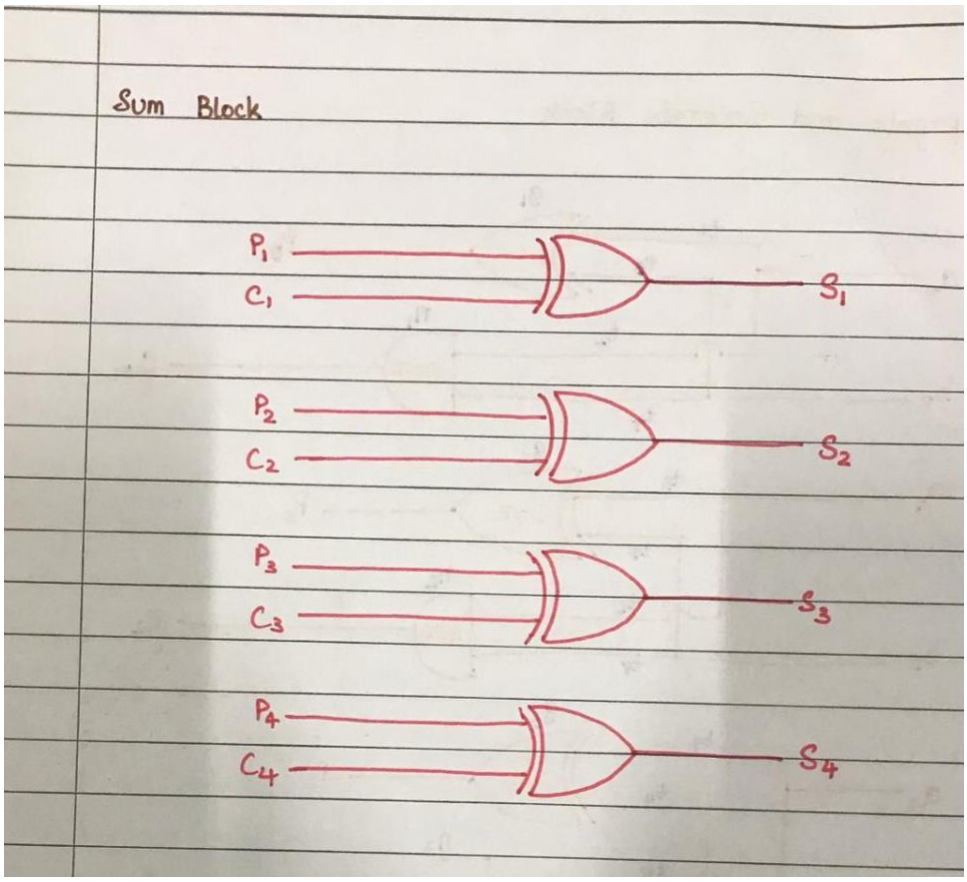
Design Details

Propagate and Generate Block

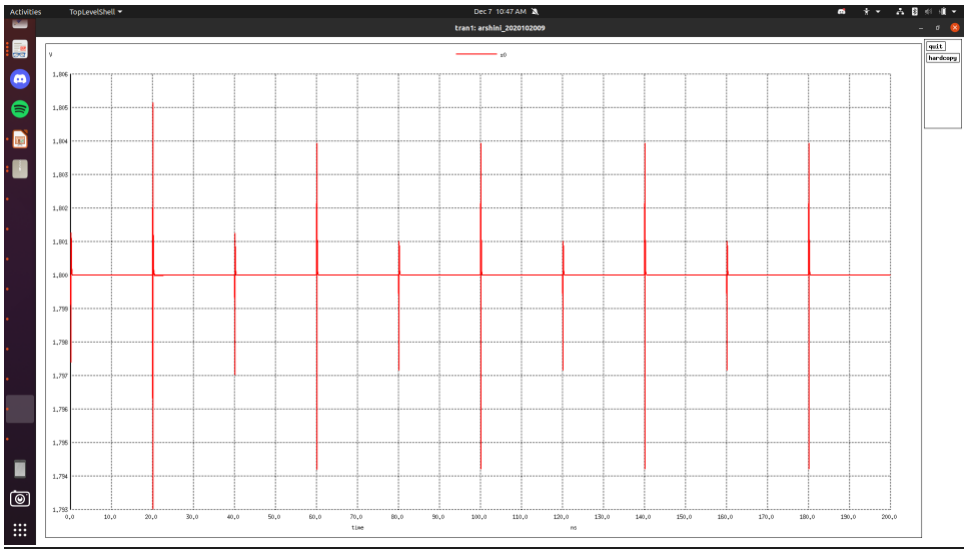


Carry Block


$P_4P_3P_2P_1C_1$
G_{13}
$P_4P_3P_2G_1$
G_{12}
G_{14}
C_5
$P_4P_3G_2$
P_4G_3
G_{11}
G_{10}
P_4
G_4
$P_3P_2P_1C_1$
G_8
$P_3P_2G_1$
G_9
C_4
P_3G_2
G_7
G_6
P_3
G_3
$P_2P_1C_1$
G_4
G_5
C_3
P_2G_1
P_2
G_2
P_1C_1
G_1
G_{15}
C_2
P_1
G_1
G_1



NGspice


Activities
TopLevelShell
Dec 7 10:47 AM
tran1: arshini_2020102009
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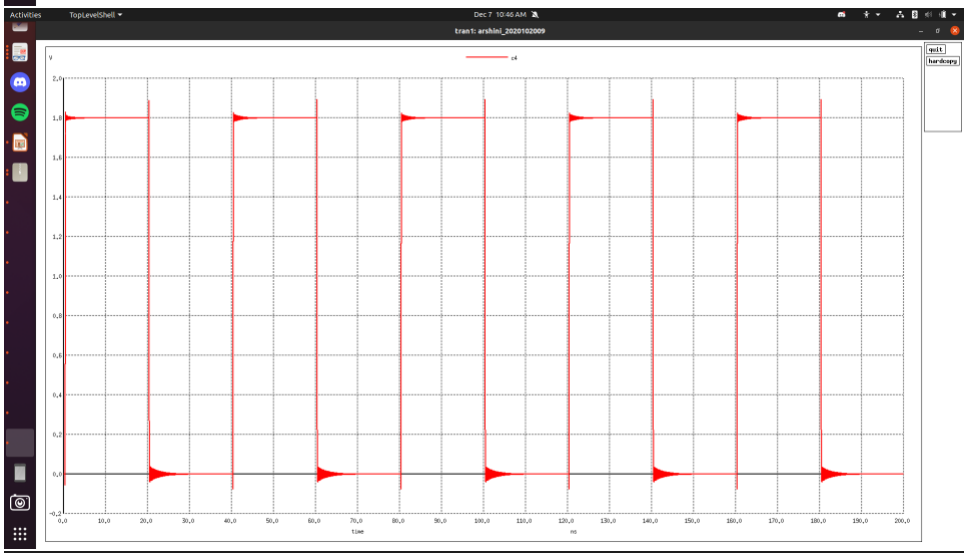
hardcopy
v
s0
time
ns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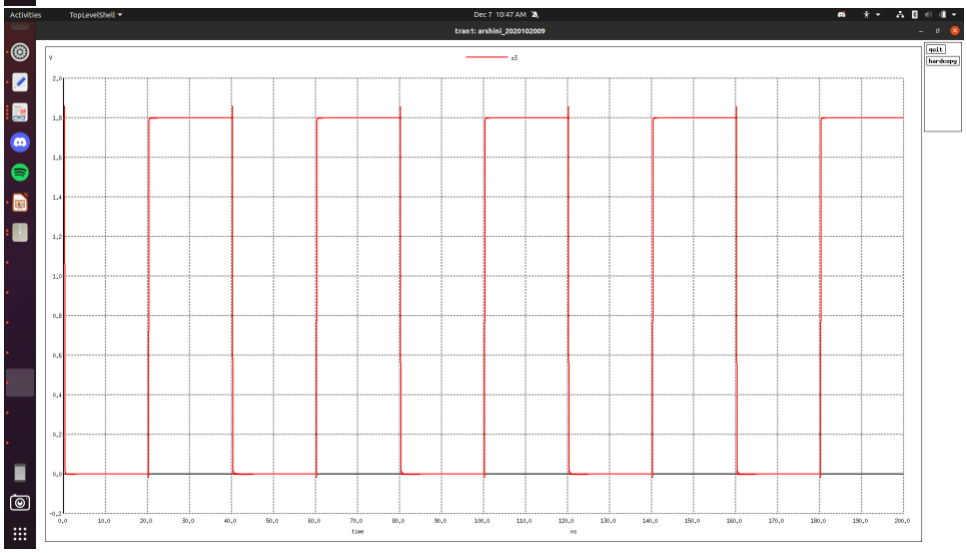
Activities
TopLevelShell
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quit
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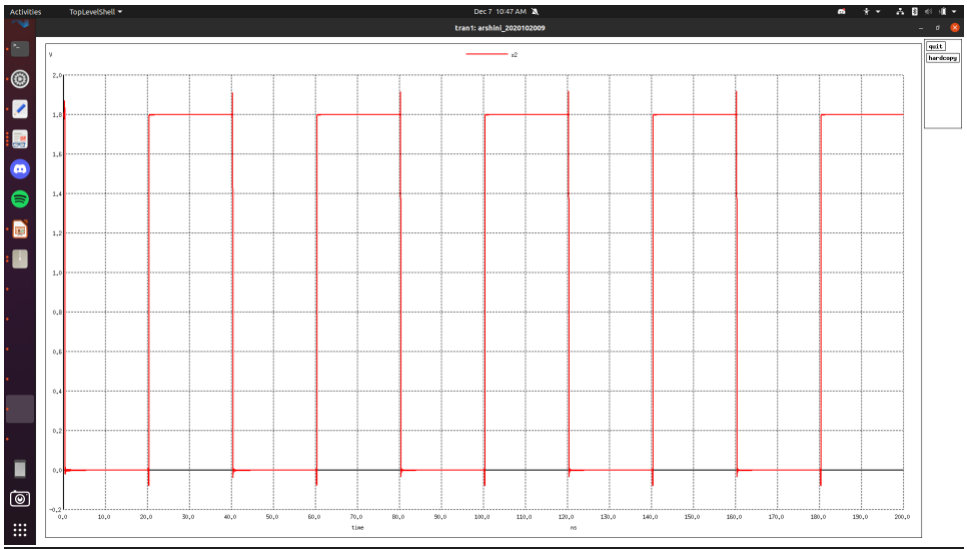
v
s3
time
ns


Activities
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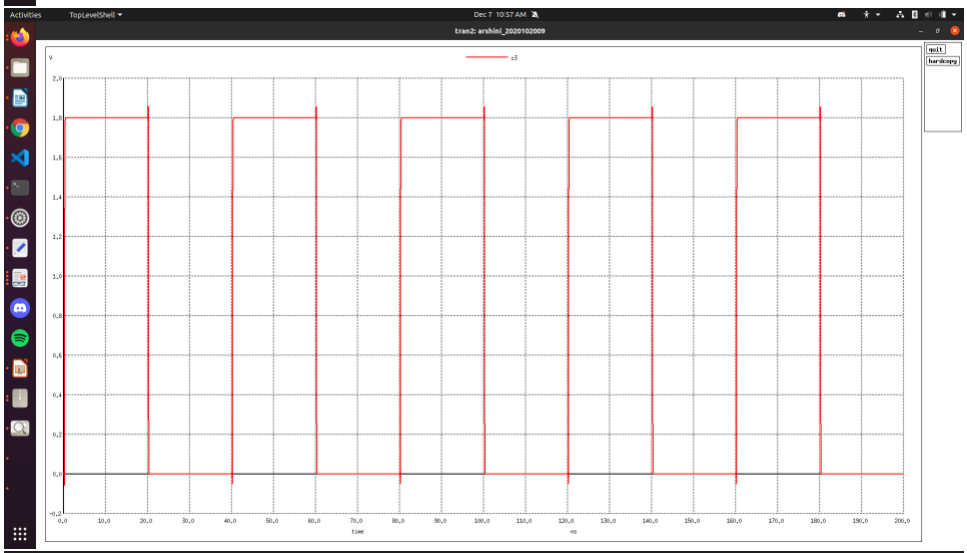
v
v2
time
ns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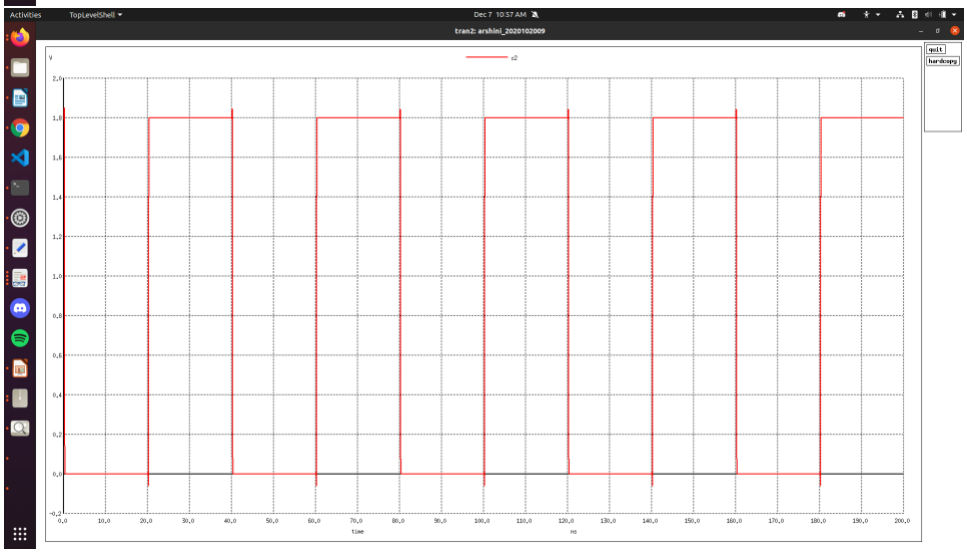
v
v3
time
ns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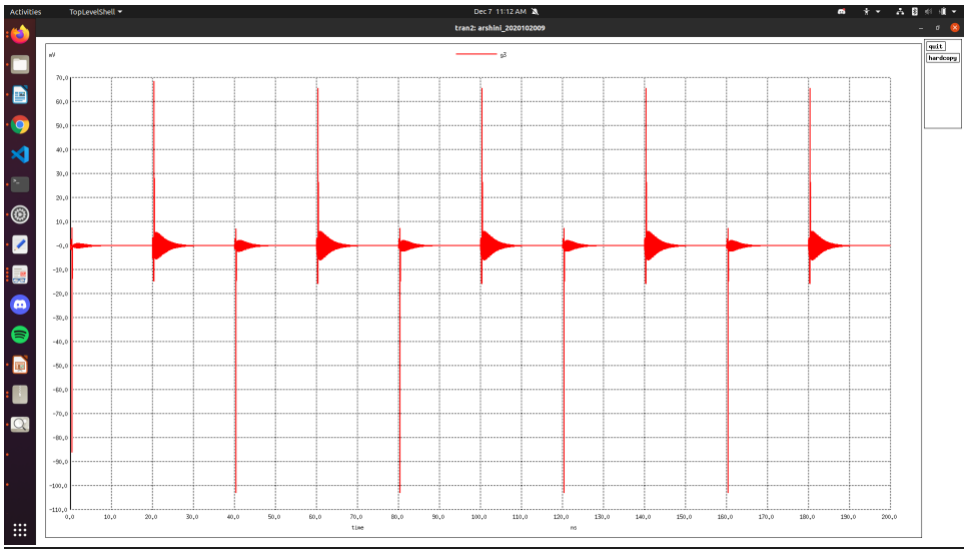
hardcopy
v
v2
time
ns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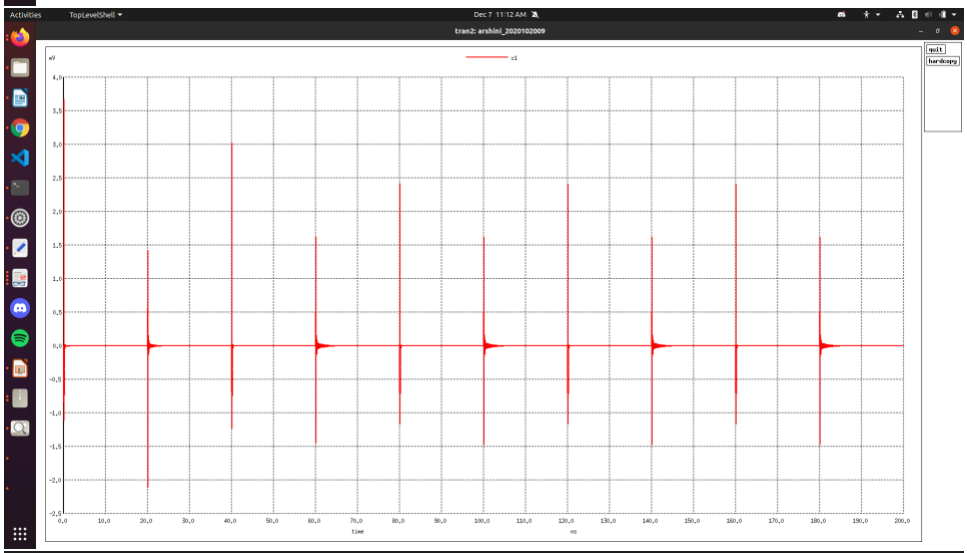
ns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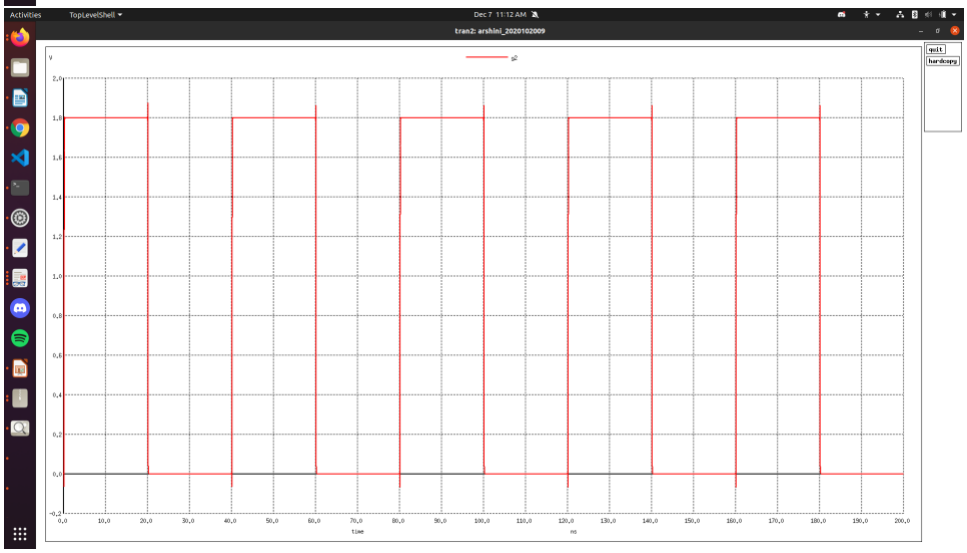
time
ns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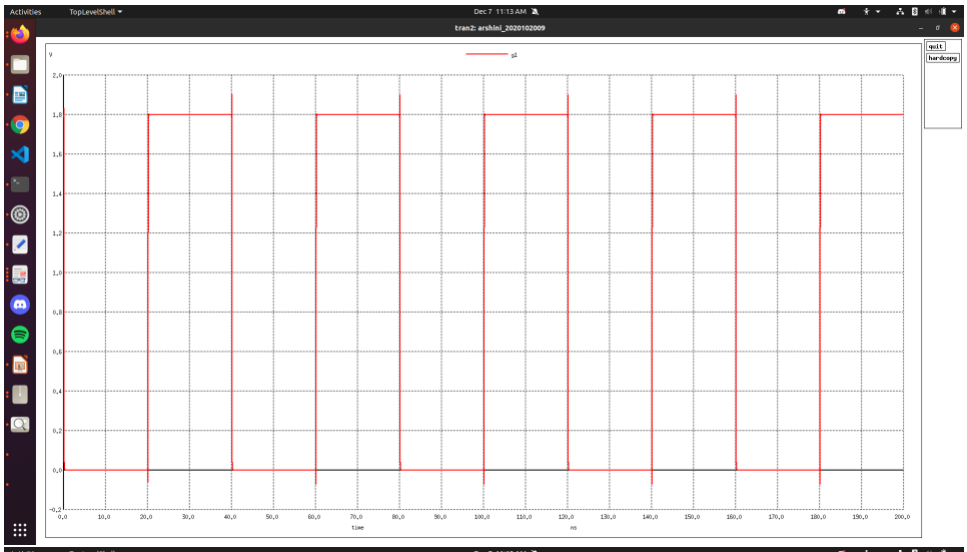
time
ns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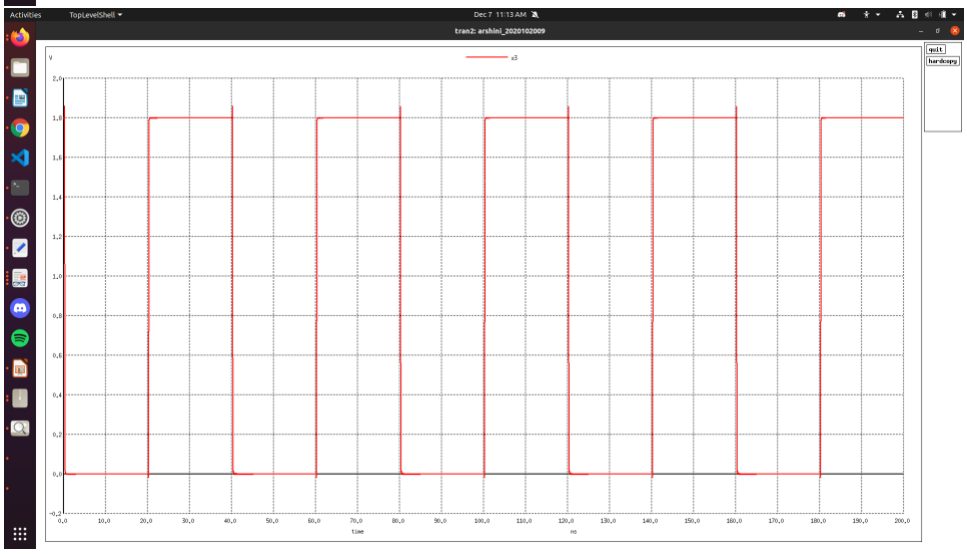
time
ns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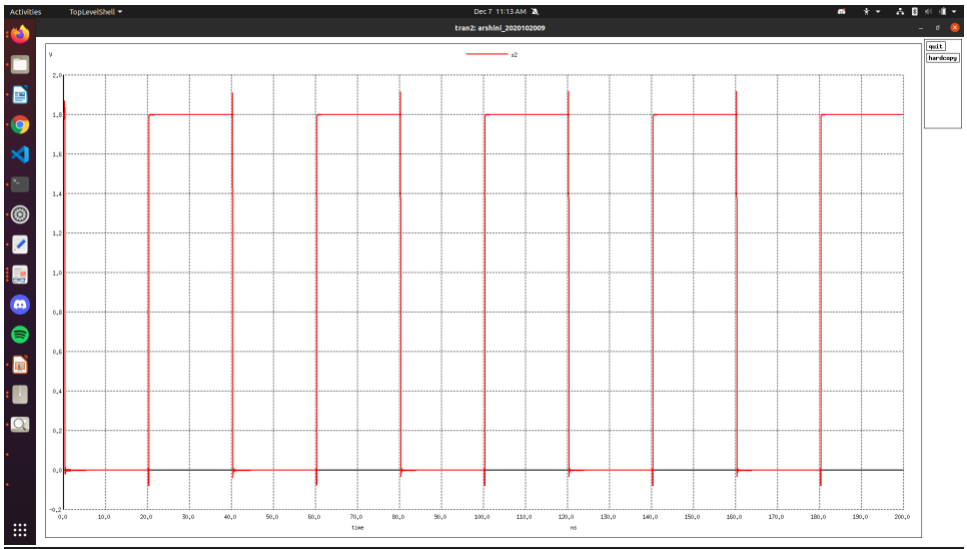
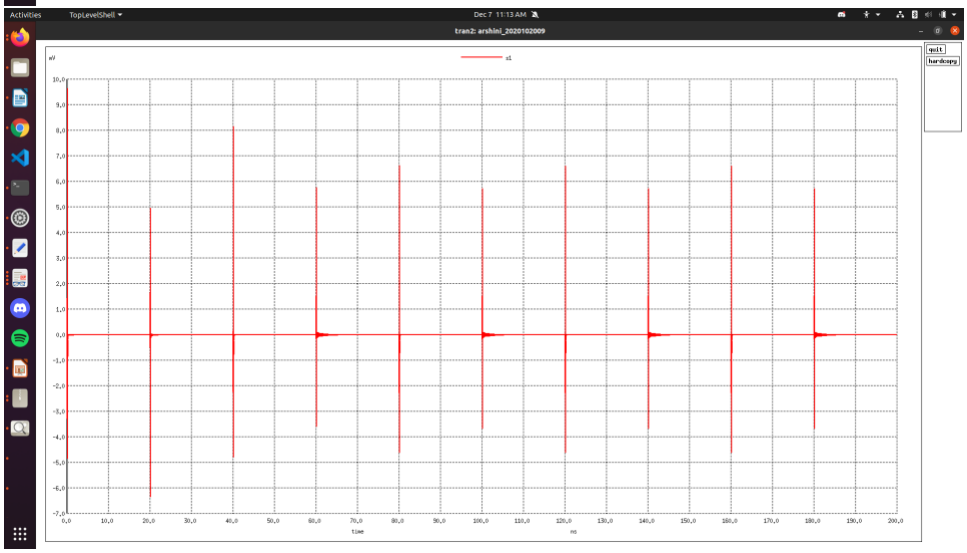

Activities
TopLevelShell
Dec 7 11:13 AM
tran2: arshini_2020102009
quit
hardcopy
v
v2
time
ns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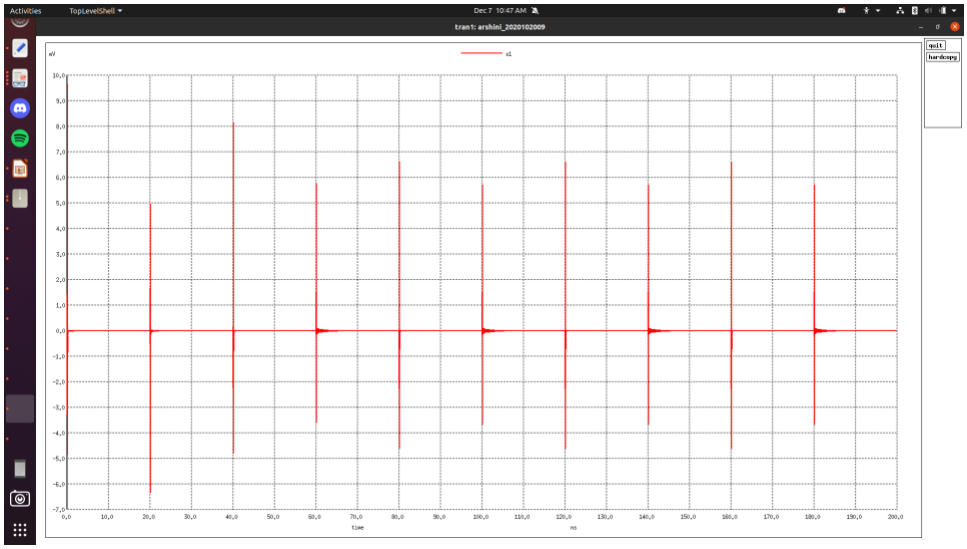
tran2: arshini_2020102009
quit
hardcopy
v
v1
time
ns


Activities
TopLevelShell
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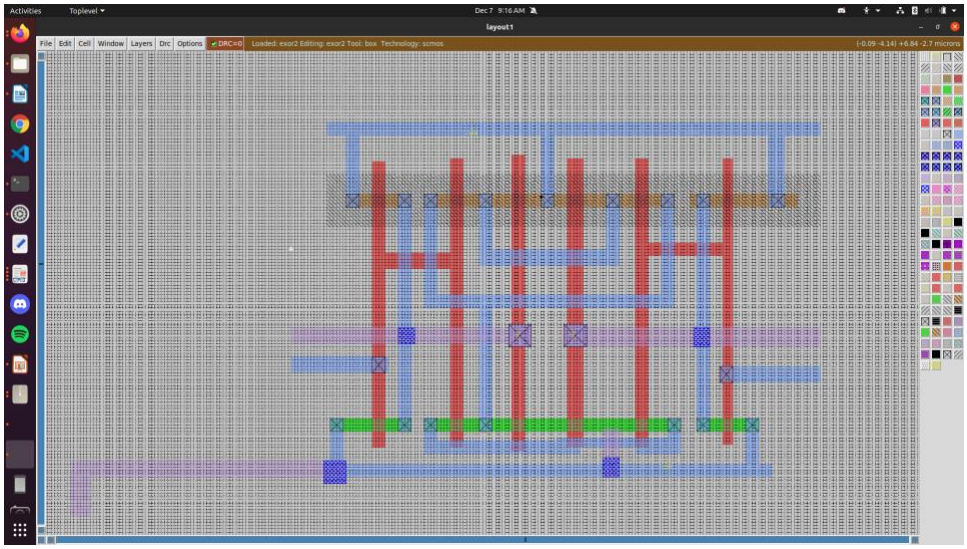
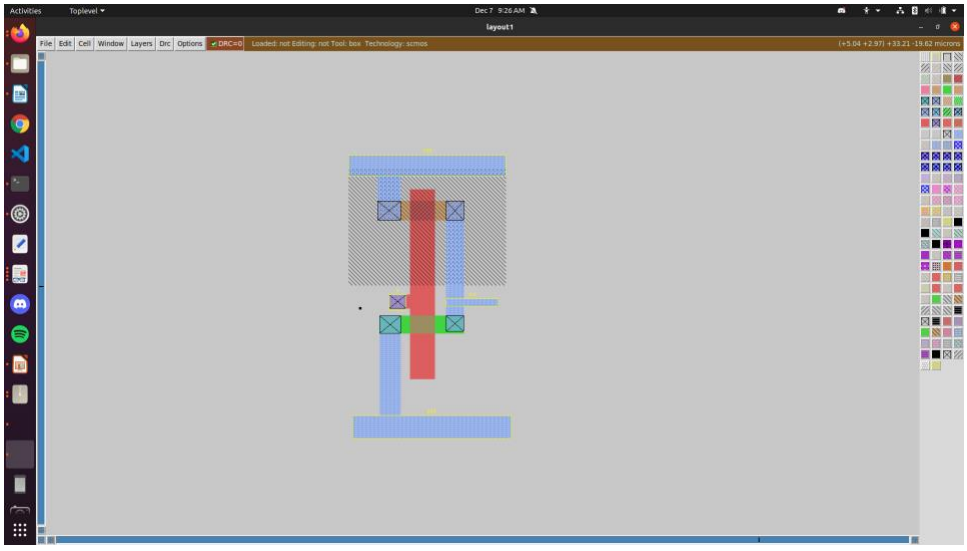
tran1: arshini_2020102009
quit
hardcopy
v
v1
time
ns

MAGIC Layout

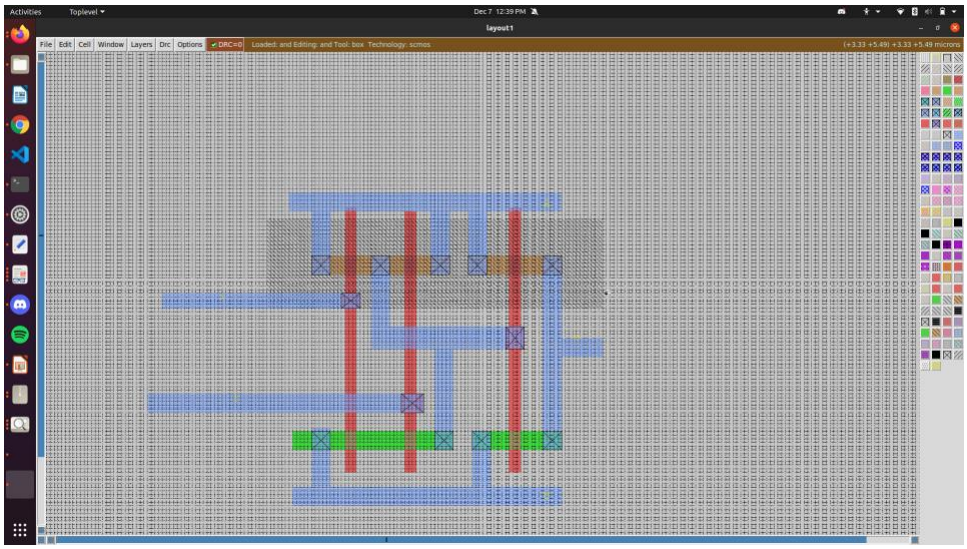
XOR Gate



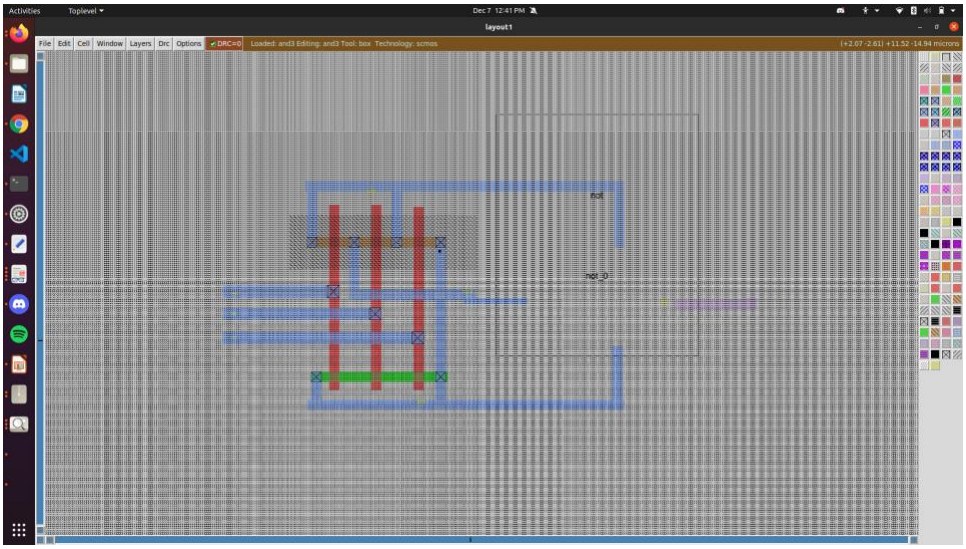
NOT Gate



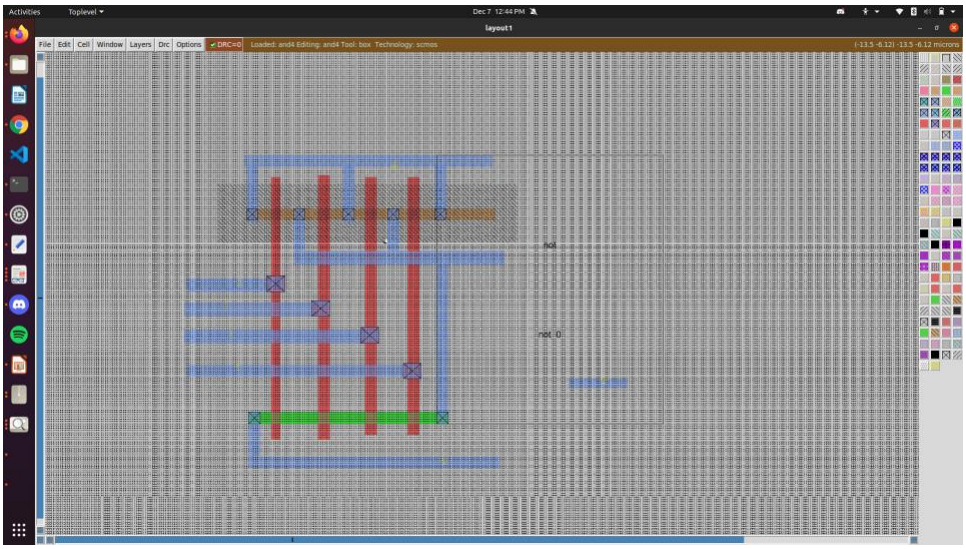
AND Gate



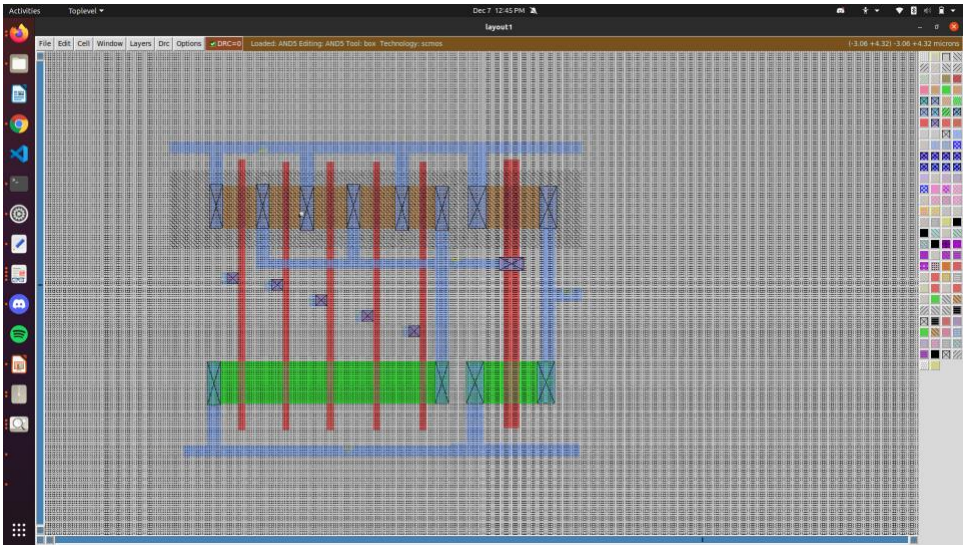
3-input AND Gate



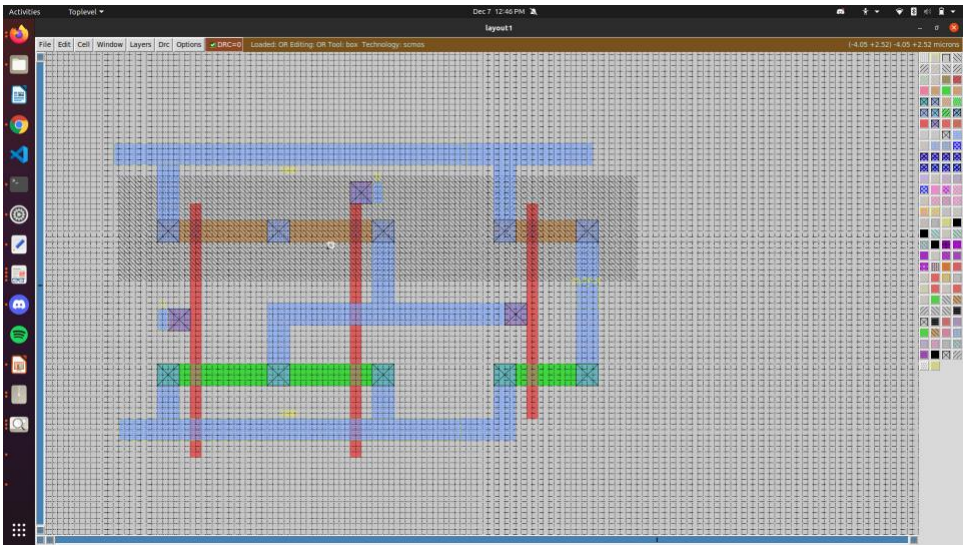
4-input AND Gate



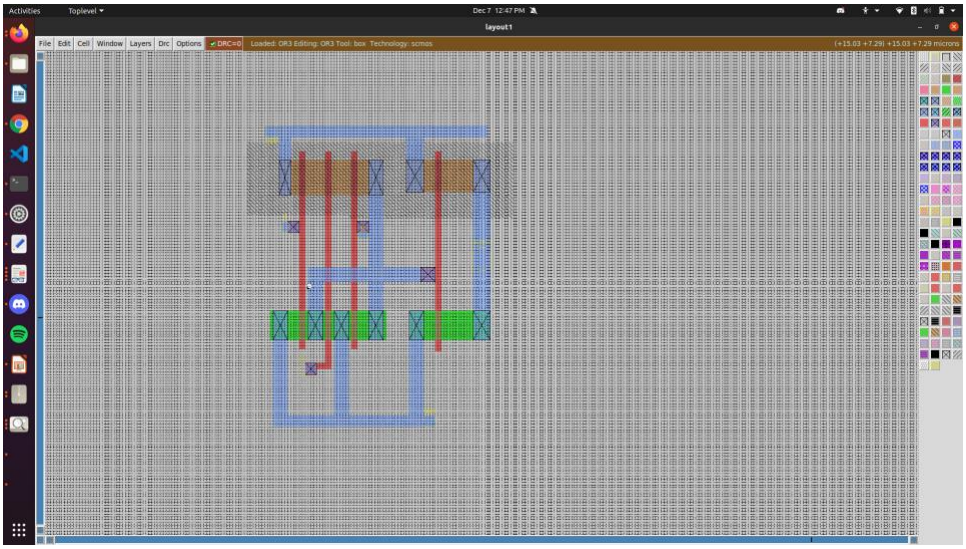
5-input AND Gate



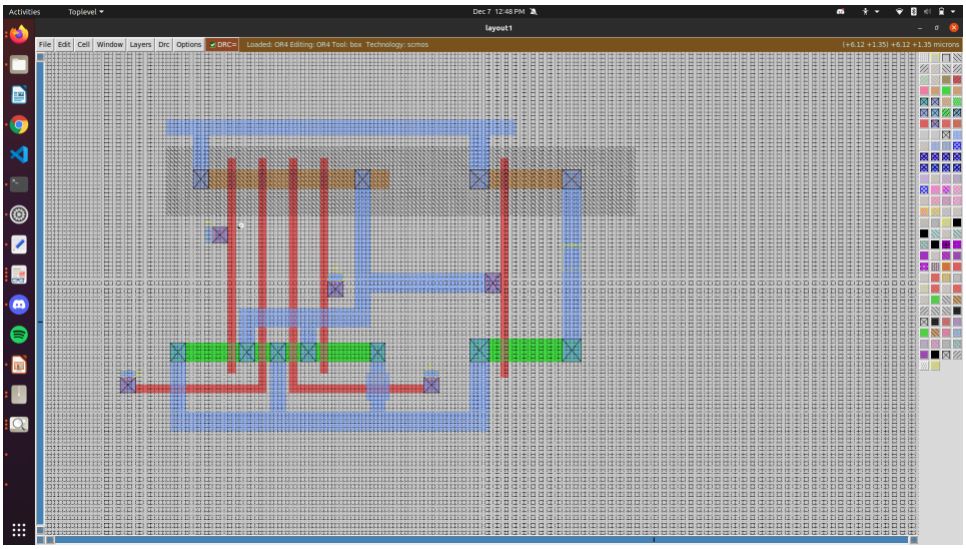
OR Gate



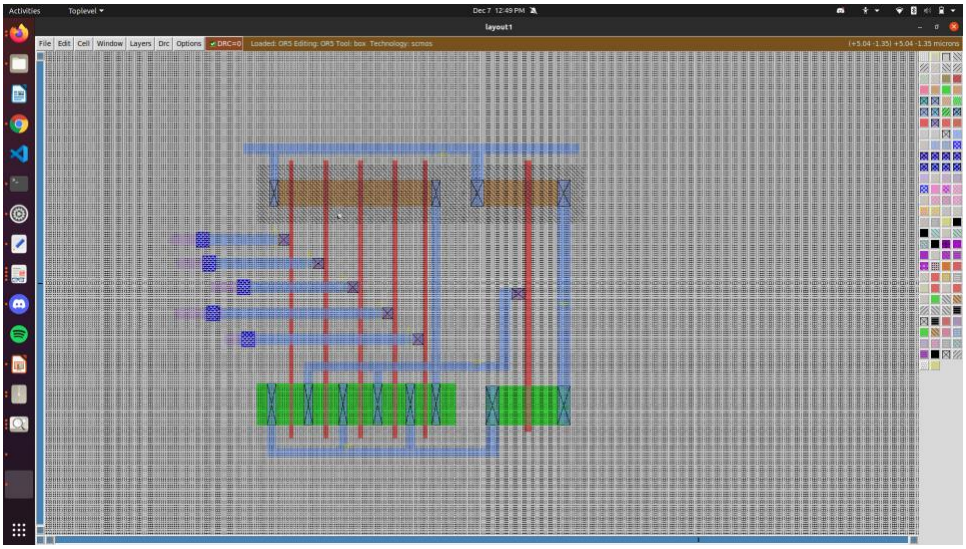
3-input OR Gate



4-input OR Gate



5-input OR Gate



Pre-layout Netlist(Ngspice)

```
.include TSMC_180nm.txt
.global Gnd Vdd
.subckt exor 7 2 4 1 0
M001 3 2 1 1 CMOSP W = 3.6u L = 0.18u
M001 3 2 0 0 CMOSN W = 1.8u L = 0.18u
M002 5 4 1 1 CMOSP W = 3.6u L = 0.18u
M002 5 4 0 0 CMOSN W = 1.8u L = 0.18u
```

```
M003 6 2 1 1 CMOSP W = 3.6u L = 0.18u
M004 6 4 1 1 CMOSP W = 3.6u L = 0.18u
M005 7 3 6 1 CMOSP W = 3.6u L = 0.18u
M006 7 5 6 1 CMOSP W = 3.6u L = 0.18u
M003 7 2 8 0 CMOSN W = 1.8u L = 0.18u
M004 8 4 0 0 CMOSN W = 1.8u L = 0.18u
M005 7 3 9 0 CMOSN W = 1.8u L = 0.18u
M006 9 5 0 0 CMOSN W = 1.8u L = 0.18u
.ends exor

.subckt and 1 4 5 6 0
M000 2 4 6 6 CMOSP W=3.6u L=0.18u
M001 2 5 6 6 CMOSP W=3.6u L=0.18u
M002 1 2 6 6 CMOSP W=3.6u L=0.18u
M000 2 5 3 0 CMOSN W=1.8u L=0.18u
M001 3 4 0 0 CMOSN W=1.8u L=0.18u
M002 1 2 0 0 CMOSN W=1.8u L=0.18u
.ends and

.subckt or 1 2 3 6 0
M000 6 2 4 6 CMOSP W=3.6u L=0.18u
M001 4 3 5 6 CMOSP W=3.6u L=0.18u
M002 6 5 1 6 CMOSP W=3.6u L=0.18u
M000 0 3 5 0 CMOSN W=1.8u L=0.18u
M001 0 2 5 0 CMOSN W=1.8u L=0.18u
M002 0 5 1 0 CMOSN W=1.8u L=0.18u
.ends or

.subckt cla K P C G Vdd Gnd
```

```
xtemp t C P Vdd Gnd and
xfinal K t G Vdd Gnd or
.ends cla

Vdd Vdd Gnd 1.8V
*a = 1100
vin1 a0 0 pulse 1.8 0 0ns 100ps 100ps 19.9ns 40ns
vin2 a1 0 pulse 1.8 0 0ns 100ps 100ps 19.9ns 40ns
vin3 a2 0 pulse 0 1.8 0ns 100ps 100ps 19.9ns 40ns
vin4 a3 0 pulse 0 1.8 0ns 100ps 100ps 19.9ns 40ns
*b = 0101
vin5 b0 0 pulse 0 1.8 0ns 100ps 100ps 19.9ns 40ns
vin6 b1 0 pulse 1.8 0 0ns 100ps 100ps 19.9ns 40ns
vin7 b2 0 pulse 0 1.8 0ns 100ps 100ps 19.9ns 40ns
vin8 b3 0 pulse 1.8 0 0ns 100ps 100ps 19.9ns 40ns

xp0 P0 a0 b0 Vdd Gnd exor
xp1 P1 a1 b1 Vdd Gnd exor
xp2 P2 a2 b2 Vdd Gnd exor
xp3 P3 a3 b3 Vdd Gnd exor

xg0 G0 a0 b0 Vdd Gnd and
xg1 G1 a1 b1 Vdd Gnd and
xg2 G2 a2 b2 Vdd Gnd and
xg3 G3 a3 b3 Vdd Gnd and

xc1 c1 P0 0 G0 Vdd Gnd cla
xc2 c2 P1 C1 G1 Vdd Gnd cla
xc3 c3 P2 C2 G2 Vdd Gnd cla
```

```
xc4 c4 P3 C3 G3 Vdd Gnd cla

xs0 s0 P0 0 Vdd Gnd exor
xs1 s1 P1 C1 Vdd Gnd exor
xs2 s2 P2 C2 Vdd Gnd exor
xs3 s3 P3 C3 Vdd Gnd exor

.tran 0.1n 200n
.control
run
set color0=white
set color1=red
set xbrushwidth=3.5
set curplottitle="Arshini_2020102009"
plot G1
plot G2
plot G3
plot G4
plot C1
plot C2
plot C3
plot C4
plot s0
plot s1
plot s2
plot s3
.endc
```

Pre-layout Netlist(Ngspice)

```
* SPICE3 file created from Magic.ext - technology: scmos

 .include ./TSMC_180nm.txt

.option scale=0.09u

 Vpower vdd gnd 1.8

M1000 cla4_0/OR5_0/B cla4_0/and4_0/not_0/a_n19_n11# cla4_0/OR5_0/vdd
cla4_0/and4_0/not_0/w_n33_n4# pfet w=4 l=3

+  ad=32 pd=24 as=3653 ps=1674

M1001 cla4_0/OR5_0/B cla4_0/and4_0/not_0/a_n19_n11# cla2_0/and3_0/c
Gnd nfet w=4 l=3

+  ad=32 pd=24 as=4201 ps=1958

M1002 cla4_0/and4_0/a_n47_n81# cla4_0/and_0/a cla4_0/and4_0/gnd Gnd
nfet w=5 l=4

+  ad=85 pd=44 as=50 ps=30

M1003 cla4_0/and4_0/a_n25_n81# cla4_0/and4_0/b
cla4_0/and4_0/a_n47_n81# Gnd nfet w=5 l=5

+  ad=80 pd=42 as=0 ps=0

M1004 cla4_0/OR5_0/vdd cla4_0/and4_0/b cla4_0/and4_0/a_n47_10#
cla4_0/and4_0/w_n75_0# pfet w=5 l=5

+  ad=0 pd=0 as=155 ps=82

M1005 cla4_0/OR5_0/vdd cla4_0/and4_0/d cla4_0/and4_0/a_n47_10#
cla4_0/and4_0/w_n75_0# pfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1006 cla4_0/and4_0/a_n47_10# cla4_0/and4_0/d cla4_0/and4_0/a_n4_n81#
Gnd nfet w=5 l=5

+  ad=65 pd=36 as=70 ps=38

M1007 cla4_0/and4_0/a_n4_n81# cla4_0/and4_0/c cla4_0/and4_0/a_n25_n81#
Gnd nfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0
```

```
M1008 cla4_0/and4_0/a_n47_10# cla4_0/and_0/a cla4_0/OR5_0/vdd
cla4_0/and4_0/w_n75_0# pfet w=5 l=4

+  ad=0 pd=0 as=0 ps=0

M1009 cla4_0/and4_0/a_n47_10# cla4_0/and4_0/c cla4_0/OR5_0/vdd
cla4_0/and4_0/w_n75_0# pfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1010 cla4_0/OR5_0/C cla2_0/and3_0/c cla4_0/OR5_0/vdd
cla4_0/and3_0/not_0/w_n33_n4# pfet w=4 l=3

+  ad=32 pd=24 as=0 ps=0

M1011 cla4_0/OR5_0/C cla2_0/and3_0/c cla2_0/and3_0/c Gnd nfet w=4 l=3

+  ad=32 pd=24 as=0 ps=0

M1012 cla2_0/and3_0/c cla3_0/and_0/b cla4_0/OR5_0/vdd
cla4_0/and3_0/w_n75_n9# pfet w=5 l=5

+  ad=405 pd=222 as=0 ps=0

M1013 cla4_0/OR5_0/vdd cla4_0/and3_0/b cla2_0/and3_0/c
cla4_0/and3_0/w_n75_n9# pfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1014 cla2_0/and3_0/c cla4_0/and_0/a cla4_0/OR5_0/vdd
cla4_0/and3_0/w_n75_n9# pfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1015 cla4_0/and3_0/a_n29_n65# cla4_0/and3_0/b
cla4_0/and3_0/a_n50_n65# Gnd nfet w=5 l=5

+  ad=80 pd=42 as=80 ps=42

M1016 cla2_0/and3_0/c cla3_0/and_0/b cla4_0/and3_0/a_n29_n65# Gnd nfet
w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1017 cla4_0/and3_0/a_n50_n65# cla4_0/and_0/a cla2_0/and3_0/c Gnd nfet
w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1018 cla4_0/OR5_0/D cla4_0/and_0/a_n67_5# cla4_0/OR5_0/vdd
cla4_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=55 pd=32 as=0 ps=0
```

```
M1019 cla4_0/and_0/a_n67_5# cla4_0/and_0/a cla4_0/OR5_0/vdd
cla4_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1020 cla4_0/and_0/a_n67_n42# cla4_0/and_0/a cla2_0/and3_0/c Gnd nfet
w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1021 cla4_0/and_0/a_n67_5# cla4_0/and_0/b cla4_0/and_0/a_n67_n42# Gnd
nfet w=5 l=3

+  ad=50 pd=30 as=0 ps=0

M1022 cla4_0/OR5_0/D cla4_0/and_0/a_n67_5# cla2_0/and3_0/c Gnd nfet
w=5 l=3

+  ad=55 pd=32 as=0 ps=0

M1023 cla4_0/OR5_0/vdd cla4_0/and_0/b cla4_0/and_0/a_n67_5#
cla4_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=0 pd=0 as=0 ps=0

M1024 cla4_0/OR5_0/a_n21_5# cla4_0/OR5_0/A cla4_0/OR5_0/vdd
cla4_0/OR5_0/w_n38_n3# pfet w=12 l=2

+  ad=168 pd=52 as=0 ps=0

M1025 cla4_0/OR5_0/a_11_5# cla4_0/OR5_0/C cla4_0/OR5_0/a_n5_5#
cla4_0/OR5_0/w_n38_n3# pfet w=12 l=2

+  ad=168 pd=52 as=168 ps=52

M1026 cla2_0/and3_0/c cla4_0/OR5_0/B cla4_0/OR5_0/nout Gnd nfet w=19
l=2

+  ad=0 pd=0 as=779 ps=196

M1027 cla4_0/OR5_0/nout cla4_0/OR5_0/E cla4_0/OR5_0/a_27_5#
cla4_0/OR5_0/w_n38_n3# pfet w=12 l=2

+  ad=72 pd=36 as=144 ps=48

M1028 cla4_0/OR5_0/a_n5_5# cla4_0/OR5_0/B cla4_0/OR5_0/a_n21_5#
cla4_0/OR5_0/w_n38_n3# pfet w=12 l=2

+  ad=0 pd=0 as=0 ps=0

M1029 cla4_0/OR5_0/nout cla4_0/OR5_0/C cla2_0/and3_0/c Gnd nfet w=19
l=2

+  ad=0 pd=0 as=0 ps=0
```

```
M1030 cla4_0/OR5_0/a_27_5# cla4_0/OR5_0/D cla4_0/OR5_0/a_11_5#
cla4_0/OR5_0/w_n38_n3# pfet w=12 l=2

+  ad=0 pd=0 as=0 ps=0

M1031 cla4_0/OR5_0/nout cla4_0/OR5_0/A cla2_0/and3_0/c Gnd nfet w=19
l=2

+  ad=0 pd=0 as=0 ps=0

M1032 cout cla4_0/OR5_0/nout cla2_0/and3_0/c Gnd nfet w=18 l=3

+  ad=324 pd=72 as=0 ps=0

M1033 cout cla4_0/OR5_0/nout cla4_0/OR5_0/vdd cla4_0/OR5_0/w_n38_n3#
pfet w=12 l=3

+  ad=216 pd=60 as=0 ps=0

M1034 cla2_0/and3_0/c cla4_0/OR5_0/D cla4_0/OR5_0/nout Gnd nfet w=19
l=2

+  ad=0 pd=0 as=0 ps=0

M1035 cla4_0/OR5_0/nout cla4_0/OR5_0/E cla2_0/and3_0/c Gnd nfet w=19
l=2

+  ad=0 pd=0 as=0 ps=0

M1036 cla4_0/OR5_0/vdd cla2_0/and_0/b cla4_0/AND5_0/out
cla4_0/AND5_0/w_n59_n15# pfet w=19 l=3

+  ad=0 pd=0 as=873 ps=210

M1037 cla4_0/OR5_0/A cla4_0/AND5_0/out cla4_0/OR5_0/vdd
cla4_0/AND5_0/w_n59_n15# pfet w=19 l=7

+  ad=323 pd=72 as=0 ps=0

M1038 cla4_0/AND5_0/a_n5_n85# cla4_0/AND5_0/b cla4_0/AND5_0/a_n25_n85#
Gnd nfet w=19 l=3

+  ad=323 pd=72 as=323 ps=72

M1039 cla4_0/AND5_0/out cla2_0/and3_0/c cla4_0/OR5_0/vdd
cla4_0/AND5_0/w_n59_n15# pfet w=19 l=3

+  ad=0 pd=0 as=0 ps=0

M1040 cla4_0/AND5_0/a_n25_n85# cla4_0/and_0/a cla2_0/and3_0/c Gnd nfet
w=19 l=3

+  ad=0 pd=0 as=0 ps=0
```

```
M1041 cla4_0/AND5_0/out cla4_0/AND5_0/c cla4_0/OR5_0/vdd
cla4_0/AND5_0/w_n59_n15# pfet w=19 l=3

+  ad=0 pd=0 as=0 ps=0

M1042 cla4_0/AND5_0/out cla4_0/and_0/a cla4_0/OR5_0/vdd
cla4_0/AND5_0/w_n59_n15# pfet w=19 l=3

+  ad=0 pd=0 as=0 ps=0

M1043 cla4_0/OR5_0/A cla4_0/AND5_0/out cla2_0/and3_0/c Gnd nfet w=19
l=7

+  ad=304 pd=70 as=0 ps=0

M1044 cla4_0/OR5_0/vdd cla4_0/AND5_0/b cla4_0/AND5_0/out
cla4_0/AND5_0/w_n59_n15# pfet w=19 l=3

+  ad=0 pd=0 as=0 ps=0

M1045 cla4_0/AND5_0/a_15_n85# cla4_0/AND5_0/c cla4_0/AND5_0/a_n5_n85#
Gnd nfet w=19 l=3

+  ad=342 pd=74 as=0 ps=0

M1046 cla4_0/AND5_0/a_36_n85# cla2_0/and_0/b cla4_0/AND5_0/a_15_n85#
Gnd nfet w=19 l=3

+  ad=342 pd=74 as=0 ps=0

M1047 cla4_0/AND5_0/out cla2_0/and3_0/c cla4_0/AND5_0/a_36_n85# Gnd
nfet w=19 l=3

+  ad=190 pd=58 as=0 ps=0

M1048 cla3_0/and4_0/vout cla3_0/and4_0/not_0/a_n19_n11#
cla3_0/and_0/vdd cla3_0/and4_0/not_0/w_n33_n4# pfet w=4 l=3

+  ad=32 pd=24 as=487 ps=288

M1049 cla3_0/and4_0/vout cla3_0/and4_0/not_0/a_n19_n11#
cla2_0/and3_0/c Gnd nfet w=4 l=3

+  ad=32 pd=24 as=0 ps=0

M1050 cla3_0/and4_0/a_n47_n81# cla3_0/and_0/a cla3_0/and4_0/d Gnd nfet
w=5 l=4

+  ad=85 pd=44 as=50 ps=30

M1051 cla3_0/and4_0/a_n25_n81# cla3_0/and4_0/b
cla3_0/and4_0/a_n47_n81# Gnd nfet w=5 l=5

+  ad=80 pd=42 as=0 ps=0
```

```
M1052 cla3_0/and_0/vdd cla3_0/and4_0/b cla3_0/and4_0/a_n47_10#
cla3_0/and4_0/w_n75_0# pfet w=5 l=5

+  ad=0 pd=0 as=155 ps=82

M1053 cla3_0/and_0/vdd cla3_0/and4_0/d cla3_0/and4_0/a_n47_10#
cla3_0/and4_0/w_n75_0# pfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1054 cla3_0/and4_0/a_n47_10# cla3_0/and4_0/d cla3_0/and4_0/a_n4_n81#
Gnd nfet w=5 l=5

+  ad=65 pd=36 as=70 ps=38

M1055 cla3_0/and4_0/a_n4_n81# cla3_0/and4_0/c cla3_0/and4_0/a_n25_n81#
Gnd nfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1056 cla3_0/and4_0/a_n47_10# cla3_0/and_0/a cla3_0/and_0/vdd
cla3_0/and4_0/w_n75_0# pfet w=5 l=4

+  ad=0 pd=0 as=0 ps=0

M1057 cla3_0/and4_0/a_n47_10# cla3_0/and4_0/c cla3_0/and_0/vdd
cla3_0/and4_0/w_n75_0# pfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1058 cla3_0/and3_0/not_0/vout cla2_0/and3_0/c cla3_0/and_0/vdd
cla3_0/and3_0/not_0/w_n33_n4# pfet w=4 l=3

+  ad=32 pd=24 as=0 ps=0

M1059 cla3_0/and3_0/not_0/vout cla2_0/and3_0/c cla2_0/and3_0/c Gnd
nfet w=4 l=3

+  ad=32 pd=24 as=0 ps=0

M1060 cla2_0/and3_0/c cla3_0/and_0/b cla3_0/and_0/vdd
cla3_0/and3_0/w_n75_n9# pfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1061 cla3_0/and_0/vdd cla3_0/and4_0/b cla2_0/and3_0/c
cla3_0/and3_0/w_n75_n9# pfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1062 cla2_0/and3_0/c cla3_0/and_0/a cla3_0/and_0/vdd
cla3_0/and3_0/w_n75_n9# pfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0
```

```
M1063 cla3_0/and3_0/a_n29_n65# cla3_0/and4_0/b
cla3_0/and3_0/a_n50_n65# Gnd nfet w=5 l=5

+  ad=80 pd=42 as=80 ps=42

M1064 cla2_0/and3_0/c cla3_0/and_0/b cla3_0/and3_0/a_n29_n65# Gnd nfet
w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1065 cla3_0/and3_0/a_n50_n65# cla3_0/and_0/a cla2_0/and3_0/c Gnd nfet
w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1066 cla3_0/and_0/out cla3_0/and_0/a_n67_5# cla3_0/and_0/vdd
cla3_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=55 pd=32 as=0 ps=0

M1067 cla3_0/and_0/a_n67_5# cla3_0/and_0/a cla3_0/and_0/vdd
cla3_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1068 cla3_0/and_0/a_n67_n42# cla3_0/and_0/a cla2_0/and3_0/c Gnd nfet
w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1069 cla3_0/and_0/a_n67_5# cla3_0/and_0/b cla3_0/and_0/a_n67_n42# Gnd
nfet w=5 l=3

+  ad=50 pd=30 as=0 ps=0

M1070 cla3_0/and_0/out cla3_0/and_0/a_n67_5# cla2_0/and3_0/c Gnd nfet
w=5 l=3

+  ad=55 pd=32 as=0 ps=0

M1071 cla3_0/and_0/vdd cla3_0/and_0/b cla3_0/and_0/a_n67_5#
cla3_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=0 pd=0 as=0 ps=0

M1072 s1 m1_n610_n2977# pblock_0/exor2_0/a_n24_n3#
pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=124 ps=78

M1073 pblock_0/not_0/vout pblock_0/not_0/vdd cla2_0/and3_0/c Gnd nfet
w=4 l=4

+  ad=64 pd=48 as=0 ps=0
```

```
M1074 pblock_0/exor2_0/a_n5_n72# pblock_0/exor2_0/a_n10_n46# s1 Gnd
nfet w=4 l=4

+  ad=52 pd=34 as=60 ps=38

M1075 pblock_0/not_0/vout pblock_0/not_0/vdd VDD
pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=693 ps=392

M1076 s1 pblock_0/not_0/vdd pblock_0/exor2_0/a_n36_n72# Gnd nfet w=4
l=4

+  ad=0 pd=0 as=72 ps=52

M1077 cla2_0/and3_0/c m1_n610_n2977# pblock_0/not_1/vout Gnd nfet w=4
l=3

+  ad=0 pd=0 as=64 ps=48

M1078 pblock_0/exor2_0/a_13_n72# pblock_0/exor2_0/a_7_n46#
pblock_0/exor2_0/a_n5_n72# Gnd nfet w=4 l=5

+  ad=64 pd=40 as=0 ps=0

M1079 pblock_0/exor2_0/a_n36_n72# m1_n610_n2977#
pblock_0/exor2_0/a_13_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1080 VDD pblock_0/exor2_0/a_n10_n46# pblock_0/exor2_0/a_n24_n3#
pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1081 pblock_0/exor2_0/a_n24_n3# pblock_0/not_0/vdd s1
pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1082 VDD m1_n610_n2977# pblock_0/not_1/vout
pblock_0/exor2_0/w_n66_n9# pfet w=4 l=3

+  ad=0 pd=0 as=72 ps=52

M1083 pblock_0/exor2_0/a_n24_n3# pblock_0/exor2_0/a_7_n46# VDD
pblock_0/exor2_0/w_n66_n9# pfet w=4 l=5

+  ad=0 pd=0 as=0 ps=0

M1084 pblock_0/not_0/vout pblock_0/not_0/vdd pblock_0/not_0/vdd
pblock_0/not_0/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=36 ps=26
```

```
M1085 pblock_0/not_0/vout pblock_0/not_0/vdd pblock_0/not_0/gnd Gnd
nfet w=4 l=3

+  ad=0 pd=0 as=32 ps=24

M1086 pblock_0/not_1/vout m1_n610_n2977# pblock_0/not_1/vdd
pblock_0/not_1/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=36 ps=26

M1087 pblock_0/not_1/vout m1_n610_n2977# pblock_0/not_1/gnd Gnd nfet
w=4 l=3

+  ad=0 pd=0 as=32 ps=24

M1088 s2 cla3_0/and4_0/b pblock_1/exor2_0/a_n24_n3#
pblock_1/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=124 ps=78

M1089 pblock_1/not_0/vout cla2_0/and_0/b cla2_0/and3_0/c Gnd nfet w=4
l=4

+  ad=64 pd=48 as=0 ps=0

M1090 pblock_1/exor2_0/a_n5_n72# pblock_1/exor2_0/a_n10_n46# s2 Gnd
nfet w=4 l=4

+  ad=52 pd=34 as=60 ps=38

M1091 pblock_1/not_0/vout cla2_0/and_0/b VDD
pblock_1/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=0 ps=0

M1092 s2 cla2_0/and_0/b pblock_1/exor2_0/a_n36_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=72 ps=52

M1093 cla2_0/and3_0/c cla3_0/and4_0/b pblock_1/not_1/vout Gnd nfet w=4
l=3

+  ad=0 pd=0 as=64 ps=48

M1094 pblock_1/exor2_0/a_13_n72# pblock_1/exor2_0/a_7_n46#
pblock_1/exor2_0/a_n5_n72# Gnd nfet w=4 l=5

+  ad=64 pd=40 as=0 ps=0

M1095 pblock_1/exor2_0/a_n36_n72# cla3_0/and4_0/b
pblock_1/exor2_0/a_13_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0
```

```
M1096 VDD pblock_1/exor2_0/a_n10_n46# pblock_1/exor2_0/a_n24_n3#
pblock_1/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1097 pblock_1/exor2_0/a_n24_n3# cla2_0/and_0/b s2
pblock_1/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1098 VDD cla3_0/and4_0/b pblock_1/not_1/vout
pblock_1/exor2_0/w_n66_n9# pfet w=4 l=3

+  ad=0 pd=0 as=72 ps=52

M1099 pblock_1/exor2_0/a_n24_n3# pblock_1/exor2_0/a_7_n46# VDD
pblock_1/exor2_0/w_n66_n9# pfet w=4 l=5

+  ad=0 pd=0 as=0 ps=0

M1100 pblock_1/not_0/vout cla2_0/and_0/b pblock_1/not_0/vdd
pblock_1/not_0/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=36 ps=26

M1101 pblock_1/not_0/vout cla2_0/and_0/b pblock_1/not_0/gnd Gnd nfet
w=4 l=3

+  ad=0 pd=0 as=32 ps=24

M1102 pblock_1/not_1/vout cla3_0/and4_0/b pblock_1/not_1/vdd
pblock_1/not_1/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=36 ps=26

M1103 pblock_1/not_1/vout cla3_0/and4_0/b pblock_1/not_1/gnd Gnd nfet
w=4 l=3

+  ad=0 pd=0 as=32 ps=24

M1104 s3 cla3_0/and_0/a pblock_2/exor2_0/a_n24_n3#
pblock_2/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=124 ps=78

M1105 pblock_2/not_0/vout cla2_0/NOR3_0/OUTPUT cla2_0/and3_0/c Gnd
nfet w=4 l=4

+  ad=64 pd=48 as=0 ps=0

M1106 pblock_2/exor2_0/a_n5_n72# pblock_2/exor2_0/a_n10_n46# s3 Gnd
nfet w=4 l=4

+  ad=52 pd=34 as=60 ps=38
```

```
M1107 pblock_2/not_0/vout cla2_0/NOR3_0/OUTPUT pblock_2/exor2_0/vdd
pblock_2/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=164 ps=106

M1108 s3 cla2_0/NOR3_0/OUTPUT pblock_2/exor2_0/a_n36_n72# Gnd nfet w=4
l=4

+  ad=0 pd=0 as=72 ps=52

M1109 cla2_0/and3_0/c cla3_0/and_0/a pblock_2/not_1/vout Gnd nfet w=4
l=3

+  ad=0 pd=0 as=64 ps=48

M1110 pblock_2/exor2_0/a_13_n72# pblock_2/exor2_0/a_7_n46#
pblock_2/exor2_0/a_n5_n72# Gnd nfet w=4 l=5

+  ad=64 pd=40 as=0 ps=0

M1111 pblock_2/exor2_0/a_n36_n72# cla3_0/and_0/a
pblock_2/exor2_0/a_13_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1112 pblock_2/exor2_0/vdd pblock_2/exor2_0/a_n10_n46#
pblock_2/exor2_0/a_n24_n3# pblock_2/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1113 pblock_2/exor2_0/a_n24_n3# cla2_0/NOR3_0/OUTPUT s3
pblock_2/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1114 pblock_2/exor2_0/vdd cla3_0/and_0/a pblock_2/not_1/vout
pblock_2/exor2_0/w_n66_n9# pfet w=4 l=3

+  ad=0 pd=0 as=72 ps=52

M1115 pblock_2/exor2_0/a_n24_n3# pblock_2/exor2_0/a_7_n46#
pblock_2/exor2_0/vdd pblock_2/exor2_0/w_n66_n9# pfet w=4 l=5

+  ad=0 pd=0 as=0 ps=0

M1116 pblock_2/not_0/vout cla2_0/NOR3_0/OUTPUT pblock_2/not_0/vdd
pblock_2/not_0/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=36 ps=26

M1117 pblock_2/not_0/vout cla2_0/NOR3_0/OUTPUT pblock_2/not_0/gnd Gnd
nfet w=4 l=3

+  ad=0 pd=0 as=32 ps=24
```

```
M1118 pblock_2/not_1/vout cla3_0/and_0/a pblock_2/not_1/vdd
pblock_2/not_1/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=36 ps=26

M1119 pblock_2/not_1/vout cla3_0/and_0/a pblock_2/not_1/gnd Gnd nfet
w=4 l=3

+  ad=0 pd=0 as=32 ps=24

M1120 cla2_0/and3_0/not_0/vout cla2_0/and3_0/c VDD
cla2_0/and3_0/not_0/w_n33_n4# pfet w=4 l=3

+  ad=32 pd=24 as=0 ps=0

M1121 cla2_0/and3_0/not_0/vout cla2_0/and3_0/c cla2_0/and3_0/c Gnd
nfet w=4 l=3

+  ad=32 pd=24 as=0 ps=0

M1122 cla2_0/and3_0/c cla2_0/and3_0/c VDD cla2_0/and3_0/w_n75_n9# pfet
w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1123 VDD cla2_0/and_0/a cla2_0/and3_0/c cla2_0/and3_0/w_n75_n9# pfet
w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1124 cla2_0/and3_0/c cla2_0/and3_0/a VDD cla2_0/and3_0/w_n75_n9# pfet
w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1125 cla2_0/and3_0/a_n29_n65# cla2_0/and_0/a cla2_0/and3_0/a_n50_n65#
Gnd nfet w=5 l=5

+  ad=80 pd=42 as=80 ps=42

M1126 cla2_0/and3_0/c cla2_0/and3_0/c cla2_0/and3_0/a_n29_n65# Gnd
nfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1127 cla2_0/and3_0/a_n50_n65# cla2_0/and3_0/a cla2_0/and3_0/c Gnd
nfet w=5 l=5

+  ad=0 pd=0 as=0 ps=0

M1128 cla2_0/NOR3_0/c cla2_0/and_0/a_n67_5# cla2_0/and_0/vdd
cla2_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=55 pd=32 as=145 ps=88
```

```
M1129 cla2_0/and_0/a_n67_5# cla2_0/and_0/a cla2_0/and_0/vdd
cla2_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1130 cla2_0/and_0/a_n67_n42# cla2_0/and_0/a cla2_0/and3_0/c Gnd nfet
w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1131 cla2_0/and_0/a_n67_5# cla2_0/and_0/b cla2_0/and_0/a_n67_n42# Gnd
nfet w=5 l=3

+  ad=50 pd=30 as=0 ps=0

M1132 cla2_0/NOR3_0/c cla2_0/and_0/a_n67_5# cla2_0/and3_0/c Gnd nfet
w=5 l=3

+  ad=55 pd=32 as=0 ps=0

M1133 cla2_0/and_0/vdd cla2_0/and_0/b cla2_0/and_0/a_n67_5#
cla2_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=0 pd=0 as=0 ps=0

M1134 cla2_0/NOR3_0/OUTPUT cla2_0/NOR3_0/a_n1_n18# cla2_0/and3_0/c Gnd
nfet w=10 l=2

+  ad=170 pd=54 as=0 ps=0

M1135 cla2_0/and3_0/c cla2_0/m2_n103_n35# cla2_0/NOR3_0/a_n1_n18# Gnd
nfet w=10 l=2

+  ad=0 pd=0 as=170 ps=74

M1136 cla2_0/NOR3_0/a_n1_n18# cla2_0/NOR3_0/c cla2_0/NOR3_0/a_8_32#
cla2_0/NOR3_0/w_n21_25# pfet w=12 l=2

+  ad=108 pd=42 as=84 ps=38

M1137 cla2_0/NOR3_0/OUTPUT cla2_0/NOR3_0/a_n1_n18# VDD
cla2_0/NOR3_0/w_n21_25# pfet w=11 l=2

+  ad=187 pd=56 as=0 ps=0

M1138 cla2_0/NOR3_0/a_n1_32# cla3_0/and_0/b VDD
cla2_0/NOR3_0/w_n21_25# pfet w=12 l=2

+  ad=84 pd=38 as=0 ps=0

M1139 cla2_0/NOR3_0/a_8_32# cla2_0/m2_n103_n35# cla2_0/NOR3_0/a_n1_32#
cla2_0/NOR3_0/w_n21_25# pfet w=12 l=2

+  ad=0 pd=0 as=0 ps=0
```

```
M1140 cla2_0/NOR3_0/a_n1_n18# cla3_0/and_0/b cla2_0/and3_0/c Gnd nfet
w=10 l=2

+  ad=0 pd=0 as=0 ps=0

M1141 cla2_0/NOR3_0/a_n1_n18# cla2_0/NOR3_0/c cla2_0/and3_0/c Gnd nfet
w=10 l=2

+  ad=0 pd=0 as=0 ps=0

M1142 s4 cla4_0/and_0/a pblock_3/exor2_0/a_n24_n3#
pblock_3/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=136 pd=100 as=124 ps=78

M1143 pblock_3/not_0/vout m1_981_n2115# cla2_0/and3_0/c Gnd nfet w=4
l=4

+  ad=64 pd=48 as=0 ps=0

M1144 pblock_3/exor2_0/a_n5_n72# pblock_3/exor2_0/a_n10_n46# s4 Gnd
nfet w=4 l=4

+  ad=52 pd=34 as=124 ps=86

M1145 pblock_3/not_0/vout m1_981_n2115# pblock_3/exor2_0/vdd
pblock_3/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=164 ps=106

M1146 s4 m1_981_n2115# pblock_3/exor2_0/a_n36_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=72 ps=52

M1147 cla2_0/and3_0/c cla4_0/and_0/a s4 Gnd nfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1148 pblock_3/exor2_0/a_13_n72# pblock_3/exor2_0/a_7_n46#
pblock_3/exor2_0/a_n5_n72# Gnd nfet w=4 l=5

+  ad=64 pd=40 as=0 ps=0

M1149 pblock_3/exor2_0/a_n36_n72# cla4_0/and_0/a
pblock_3/exor2_0/a_13_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1150 pblock_3/exor2_0/vdd pblock_3/exor2_0/a_n10_n46#
pblock_3/exor2_0/a_n24_n3# pblock_3/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1151 pblock_3/exor2_0/a_n24_n3# m1_981_n2115# s4
pblock_3/exor2_0/w_n66_n9# pfet w=4 l=4
```

```
+  ad=0 pd=0 as=0 ps=0

M1152 pblock_3/exor2_0/vdd cla4_0/and_0/a s4
pblock_3/exor2_0/w_n66_n9# pfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1153 pblock_3/exor2_0/a_n24_n3# pblock_3/exor2_0/a_7_n46#
pblock_3/exor2_0/vdd pblock_3/exor2_0/w_n66_n9# pfet w=4 l=5

+  ad=0 pd=0 as=0 ps=0

M1154 pblock_3/not_0/vout m1_981_n2115# pblock_3/not_0/vdd
pblock_3/not_0/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=36 ps=26

M1155 pblock_3/not_0/vout m1_981_n2115# pblock_3/not_0/gnd Gnd nfet
w=4 l=3

+  ad=0 pd=0 as=32 ps=24

M1156 s4 cla4_0/and_0/a pblock_3/not_1/vdd pblock_3/not_1/w_n33_n4#
pfet w=4 l=3

+  ad=0 pd=0 as=36 ps=26

M1157 s4 cla4_0/and_0/a pblock_3/not_1/gnd Gnd nfet w=4 l=3

+  ad=0 pd=0 as=32 ps=24

M1158 cla2_0/and_0/b pdblock_0/and_0/a_n67_5# cla4_0/OR5_0/vdd
pdblock_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=55 pd=32 as=0 ps=0

M1159 pdblock_0/and_0/a_n67_5# aa cla4_0/OR5_0/vdd
pdblock_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1160 pdblock_0/and_0/a_n67_n42# aa cla2_0/and3_0/c Gnd nfet w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1161 pdblock_0/and_0/a_n67_5# ba pdblock_0/and_0/a_n67_n42# Gnd nfet
w=5 l=3

+  ad=50 pd=30 as=0 ps=0

M1162 cla2_0/and_0/b pdblock_0/and_0/a_n67_5# cla2_0/and3_0/c Gnd nfet
w=5 l=3

+  ad=55 pd=32 as=0 ps=0
```

```
M1163 cla4_0/OR5_0/vdd ba pdblock_0/and_0/a_n67_5#
pdblock_0/and_0/w_n91_n4# pfet w=5 l=3

+  ad=0 pd=0 as=0 ps=0

M1164 pdblock_0/pblock_0/not_1/vout ba
pdblock_0/pblock_0/exor2_0/a_n24_n3#
pdblock_0/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=136 pd=100 as=124 ps=78

M1165 pdblock_0/pblock_0/not_0/vout aa cla2_0/and3_0/c Gnd nfet w=4
l=4

+  ad=64 pd=48 as=0 ps=0

M1166 pdblock_0/pblock_0/exor2_0/a_n5_n72#
pdblock_0/pblock_0/exor2_0/a_n10_n46# pdblock_0/pblock_0/not_1/vout
Gnd nfet w=4 l=4

+  ad=52 pd=34 as=124 ps=86

M1167 pdblock_0/pblock_0/not_0/vout aa cla4_0/OR5_0/vdd
pdblock_0/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=0 ps=0

M1168 pdblock_0/pblock_0/not_1/vout aa
pdblock_0/pblock_0/exor2_0/a_n36_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=72 ps=52

M1169 cla2_0/and3_0/c ba pdblock_0/pblock_0/not_1/vout Gnd nfet w=4
l=3

+  ad=0 pd=0 as=0 ps=0

M1170 pdblock_0/pblock_0/exor2_0/a_13_n72#
pdblock_0/pblock_0/exor2_0/a_7_n46#
pdblock_0/pblock_0/exor2_0/a_n5_n72# Gnd nfet w=4 l=5

+  ad=64 pd=40 as=0 ps=0

M1171 pdblock_0/pblock_0/exor2_0/a_n36_n72# ba
pdblock_0/pblock_0/exor2_0/a_13_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1172 cla4_0/OR5_0/vdd pdblock_0/pblock_0/exor2_0/a_n10_n46#
pdblock_0/pblock_0/exor2_0/a_n24_n3#
pdblock_0/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0
```

M1173 pdblock_0/pblock_0/exor2_0/a_n24_n3# aa pdblock_0/pblock_0/not_1/vout pdblock_0/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+ ad=0 pd=0 as=0 ps=0

M1174 cla4_0/OR5_0/vdd ba pdblock_0/pblock_0/not_1/vout pdblock_0/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=3

+ ad=0 pd=0 as=0 ps=0

M1175 pdblock_0/pblock_0/exor2_0/a_n24_n3# pdblock_0/pblock_0/exor2_0/a_7_n46# cla4_0/OR5_0/vdd pdblock_0/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=5

+ ad=0 pd=0 as=0 ps=0

M1176 pdblock_0/pblock_0/not_0/vout aa cla4_0/OR5_0/vdd pdblock_0/pblock_0/not_0/w_n33_n4# pfet w=4 l=3

+ ad=0 pd=0 as=0 ps=0

M1177 pdblock_0/pblock_0/not_0/vout aa cla2_0/and3_0/c Gnd nfet w=4 l=3

+ ad=0 pd=0 as=0 ps=0

M1178 pdblock_0/pblock_0/not_1/vout ba cla4_0/OR5_0/vdd pdblock_0/pblock_0/not_1/w_n33_n4# pfet w=4 l=3

+ ad=0 pd=0 as=0 ps=0

M1179 pdblock_0/pblock_0/not_1/vout ba cla2_0/and3_0/c Gnd nfet w=4 l=3

+ ad=0 pd=0 as=0 ps=0

M1180 cla3_0/and_0/b pdblock_1/and_0/a_n67_5# cla4_0/OR5_0/vdd pdblock_1/and_0/w_n91_n4# pfet w=5 l=3

+ ad=55 pd=32 as=0 ps=0

M1181 pdblock_1/and_0/a_n67_5# ab cla4_0/OR5_0/vdd pdblock_1/and_0/w_n91_n4# pfet w=5 l=3

+ ad=65 pd=36 as=0 ps=0

M1182 pdblock_1/and_0/a_n67_n42# ab cla2_0/and3_0/c Gnd nfet w=5 l=3

+ ad=65 pd=36 as=0 ps=0

M1183 pdblock_1/and_0/a_n67_5# bb pdblock_1/and_0/a_n67_n42# Gnd nfet w=5 l=3

+ ad=50 pd=30 as=0 ps=0

```
M1184 cla3_0/and_0/b pdblock_1/and_0/a_n67_5# cla2_0/and3_0/c Gnd nfet
w=5 l=3

+  ad=55 pd=32 as=0 ps=0

M1185 cla4_0/OR5_0/vdd bb pdblock_1/and_0/a_n67_5#
pdblock_1/and_0/w_n91_n4# pfet w=5 l=3

+  ad=0 pd=0 as=0 ps=0

M1186 pdblock_1/pblock_0/not_1/vout bb
pdblock_1/pblock_0/exor2_0/a_n24_n3#
pdblock_1/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=136 pd=100 as=124 ps=78

M1187 pdblock_1/pblock_0/not_0/vout ab cla2_0/and3_0/c Gnd nfet w=4
l=4

+  ad=64 pd=48 as=0 ps=0

M1188 pdblock_1/pblock_0/exor2_0/a_n5_n72#
pdblock_1/pblock_0/exor2_0/a_n10_n46# pdblock_1/pblock_0/not_1/vout
Gnd nfet w=4 l=4

+  ad=52 pd=34 as=124 ps=86

M1189 pdblock_1/pblock_0/not_0/vout ab cla4_0/OR5_0/vdd
pdblock_1/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=0 ps=0

M1190 pdblock_1/pblock_0/not_1/vout ab
pdblock_1/pblock_0/exor2_0/a_n36_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=72 ps=52

M1191 cla2_0/and3_0/c bb pdblock_1/pblock_0/not_1/vout Gnd nfet w=4
l=3

+  ad=0 pd=0 as=0 ps=0

M1192 pdblock_1/pblock_0/exor2_0/a_13_n72#
pdblock_1/pblock_0/exor2_0/a_7_n46#
pdblock_1/pblock_0/exor2_0/a_n5_n72# Gnd nfet w=4 l=5

+  ad=64 pd=40 as=0 ps=0

M1193 pdblock_1/pblock_0/exor2_0/a_n36_n72# bb
pdblock_1/pblock_0/exor2_0/a_13_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0
```

```
M1194 cla4_0/OR5_0/vdd pdblock_1/pblock_0/exor2_0/a_n10_n46#
pdblock_1/pblock_0/exor2_0/a_n24_n3#
pdblock_1/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1195 pdblock_1/pblock_0/exor2_0/a_n24_n3# ab
pdblock_1/pblock_0/not_1/vout pdblock_1/pblock_0/exor2_0/w_n66_n9#
pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1196 cla4_0/OR5_0/vdd bb pdblock_1/pblock_0/not_1/vout
pdblock_1/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1197 pdblock_1/pblock_0/exor2_0/a_n24_n3#
pdblock_1/pblock_0/exor2_0/a_7_n46# cla4_0/OR5_0/vdd
pdblock_1/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=5

+  ad=0 pd=0 as=0 ps=0

M1198 pdblock_1/pblock_0/not_0/vout ab cla4_0/OR5_0/vdd
pdblock_1/pblock_0/not_0/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1199 pdblock_1/pblock_0/not_0/vout ab cla2_0/and3_0/c Gnd nfet w=4
l=3

+  ad=0 pd=0 as=0 ps=0

M1200 pdblock_1/pblock_0/not_1/vout bb cla4_0/OR5_0/vdd
pdblock_1/pblock_0/not_1/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1201 pdblock_1/pblock_0/not_1/vout bb cla2_0/and3_0/c Gnd nfet w=4
l=3

+  ad=0 pd=0 as=0 ps=0

M1202 cla4_0/and_0/b pdblock_2/and_0/a_n67_5# cla4_0/OR5_0/vdd
pdblock_2/and_0/w_n91_n4# pfet w=5 l=3

+  ad=55 pd=32 as=0 ps=0

M1203 pdblock_2/and_0/a_n67_5# ac cla4_0/OR5_0/vdd
pdblock_2/and_0/w_n91_n4# pfet w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1204 pdblock_2/and_0/a_n67_n42# ac cla2_0/and3_0/c Gnd nfet w=5 l=3
```

```
+  ad=65 pd=36 as=0 ps=0

M1205 pdblock_2/and_0/a_n67_5# bc pdblock_2/and_0/a_n67_n42# Gnd nfet
w=5 l=3

+  ad=50 pd=30 as=0 ps=0

M1206 cla4_0/and_0/b pdblock_2/and_0/a_n67_5# cla2_0/and3_0/c Gnd nfet
w=5 l=3

+  ad=55 pd=32 as=0 ps=0

M1207 cla4_0/OR5_0/vdd bc pdblock_2/and_0/a_n67_5#
pdblock_2/and_0/w_n91_n4# pfet w=5 l=3

+  ad=0 pd=0 as=0 ps=0

M1208 pdblock_2/pblock_0/not_1/vout bc
pdblock_2/pblock_0/exor2_0/a_n24_n3#
pdblock_2/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=136 pd=100 as=124 ps=78

M1209 pdblock_2/pblock_0/not_0/vout ac cla2_0/and3_0/c Gnd nfet w=4
l=4

+  ad=64 pd=48 as=0 ps=0

M1210 pdblock_2/pblock_0/exor2_0/a_n5_n72#
pdblock_2/pblock_0/exor2_0/a_n10_n46# pdblock_2/pblock_0/not_1/vout
Gnd nfet w=4 l=4

+  ad=52 pd=34 as=124 ps=86

M1211 pdblock_2/pblock_0/not_0/vout ac cla4_0/OR5_0/vdd
pdblock_2/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=0 ps=0

M1212 pdblock_2/pblock_0/not_1/vout ac
pdblock_2/pblock_0/exor2_0/a_n36_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=72 ps=52

M1213 cla2_0/and3_0/c bc pdblock_2/pblock_0/not_1/vout Gnd nfet w=4
l=3

+  ad=0 pd=0 as=0 ps=0

M1214 pdblock_2/pblock_0/exor2_0/a_13_n72#
pdblock_2/pblock_0/exor2_0/a_7_n46#
pdblock_2/pblock_0/exor2_0/a_n5_n72# Gnd nfet w=4 l=5

+  ad=64 pd=40 as=0 ps=0
```

```
M1215 pdblock_2/pblock_0/exor2_0/a_n36_n72# bc
pdblock_2/pblock_0/exor2_0/a_13_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1216 cla4_0/OR5_0/vdd pdblock_2/pblock_0/exor2_0/a_n10_n46#
pdblock_2/pblock_0/exor2_0/a_n24_n3#
pdblock_2/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1217 pdblock_2/pblock_0/exor2_0/a_n24_n3# ac
pdblock_2/pblock_0/not_1/vout pdblock_2/pblock_0/exor2_0/w_n66_n9#
pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1218 cla4_0/OR5_0/vdd bc pdblock_2/pblock_0/not_1/vout
pdblock_2/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1219 pdblock_2/pblock_0/exor2_0/a_n24_n3#
pdblock_2/pblock_0/exor2_0/a_7_n46# cla4_0/OR5_0/vdd
pdblock_2/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=5

+  ad=0 pd=0 as=0 ps=0

M1220 pdblock_2/pblock_0/not_0/vout ac cla4_0/OR5_0/vdd
pdblock_2/pblock_0/not_0/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1221 pdblock_2/pblock_0/not_0/vout ac cla2_0/and3_0/c Gnd nfet w=4
l=3

+  ad=0 pd=0 as=0 ps=0

M1222 pdblock_2/pblock_0/not_1/vout bc cla4_0/OR5_0/vdd
pdblock_2/pblock_0/not_1/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1223 pdblock_2/pblock_0/not_1/vout bc cla2_0/and3_0/c Gnd nfet w=4
l=3

+  ad=0 pd=0 as=0 ps=0

M1224 cla4_0/OR5_0/E pdblock_3/and_0/a_n67_5# cla4_0/OR5_0/vdd
pdblock_3/and_0/w_n91_n4# pfet w=5 l=3

+  ad=55 pd=32 as=0 ps=0
```

```
M1225 pdblock_3/and_0/a_n67_5# ad cla4_0/OR5_0/vdd
pdblock_3/and_0/w_n91_n4# pfet w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1226 pdblock_3/and_0/a_n67_n42# ad cla2_0/and3_0/c Gnd nfet w=5 l=3

+  ad=65 pd=36 as=0 ps=0

M1227 pdblock_3/and_0/a_n67_5# bd pdblock_3/and_0/a_n67_n42# Gnd nfet
w=5 l=3

+  ad=50 pd=30 as=0 ps=0

M1228 cla4_0/OR5_0/E pdblock_3/and_0/a_n67_5# cla2_0/and3_0/c Gnd nfet
w=5 l=3

+  ad=55 pd=32 as=0 ps=0

M1229 cla4_0/OR5_0/vdd bd pdblock_3/and_0/a_n67_5#
pdblock_3/and_0/w_n91_n4# pfet w=5 l=3

+  ad=0 pd=0 as=0 ps=0

M1230 pdblock_3/pblock_0/not_1/vout bd
pdblock_3/pblock_0/exor2_0/a_n24_n3#
pdblock_3/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=136 pd=100 as=124 ps=78

M1231 pdblock_3/pblock_0/not_0/vout ad cla2_0/and3_0/c Gnd nfet w=4
l=4

+  ad=64 pd=48 as=0 ps=0

M1232 pdblock_3/pblock_0/exor2_0/a_n5_n72#
pdblock_3/pblock_0/exor2_0/a_n10_n46# pdblock_3/pblock_0/not_1/vout
Gnd nfet w=4 l=4

+  ad=52 pd=34 as=124 ps=86

M1233 pdblock_3/pblock_0/not_0/vout ad cla4_0/OR5_0/vdd
pdblock_3/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=64 pd=48 as=0 ps=0

M1234 pdblock_3/pblock_0/not_1/vout ad
pdblock_3/pblock_0/exor2_0/a_n36_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=72 ps=52

M1235 cla2_0/and3_0/c bd pdblock_3/pblock_0/not_1/vout Gnd nfet w=4
l=3

+  ad=0 pd=0 as=0 ps=0
```

```
M1236 pdblock_3/pblock_0/exor2_0/a_13_n72#
pdblock_3/pblock_0/exor2_0/a_7_n46#
pdblock_3/pblock_0/exor2_0/a_n5_n72# Gnd nfet w=4 l=5

+  ad=64 pd=40 as=0 ps=0

M1237 pdblock_3/pblock_0/exor2_0/a_n36_n72# bd
pdblock_3/pblock_0/exor2_0/a_13_n72# Gnd nfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1238 cla4_0/OR5_0/vdd pdblock_3/pblock_0/exor2_0/a_n10_n46#
pdblock_3/pblock_0/exor2_0/a_n24_n3#
pdblock_3/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1239 pdblock_3/pblock_0/exor2_0/a_n24_n3# ad
pdblock_3/pblock_0/not_1/vout pdblock_3/pblock_0/exor2_0/w_n66_n9#
pfet w=4 l=4

+  ad=0 pd=0 as=0 ps=0

M1240 cla4_0/OR5_0/vdd bd pdblock_3/pblock_0/not_1/vout
pdblock_3/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1241 pdblock_3/pblock_0/exor2_0/a_n24_n3#
pdblock_3/pblock_0/exor2_0/a_7_n46# cla4_0/OR5_0/vdd
pdblock_3/pblock_0/exor2_0/w_n66_n9# pfet w=4 l=5

+  ad=0 pd=0 as=0 ps=0

M1242 pdblock_3/pblock_0/not_0/vout ad cla4_0/OR5_0/vdd
pdblock_3/pblock_0/not_0/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1243 pdblock_3/pblock_0/not_0/vout ad cla2_0/and3_0/c Gnd nfet w=4
l=3

+  ad=0 pd=0 as=0 ps=0

M1244 pdblock_3/pblock_0/not_1/vout bd cla4_0/OR5_0/vdd
pdblock_3/pblock_0/not_1/w_n33_n4# pfet w=4 l=3

+  ad=0 pd=0 as=0 ps=0

M1245 pdblock_3/pblock_0/not_1/vout bd cla2_0/and3_0/c Gnd nfet w=4
l=3

+  ad=0 pd=0 as=0 ps=0
```

C0 cla3_0/and_0/b cla3_0/and4_0/b 3.01fF

C1 cla2_0/and3_0/c cla3_0/and_0/b 2.00fF

C2 cla2_0/and_0/b cla3_0/and4_0/b 3.16fF

C3 cla3_0/and_0/a cla2_0/and_0/b 2.34fF

C4 cla2_0/and_0/b cla2_0/and3_0/c 3.14fF

C5 cla4_0/OR5_0/vdd cla2_0/and3_0/c 3.22fF

C6 cla4_0/and4_0/b cla4_0/and4_0/c 3.71fF

C7 cla3_0/and_0/a cla3_0/and4_0/b 13.36fF

C8 cla2_0/and3_0/c cla3_0/and4_0/b 2.90fF

C9 cla2_0/and3_0/c cla4_0/and_0/b 5.10fF

C10 cla2_0/and_0/b cla4_0/and_0/a 3.08fF

C11 VDD m2_n610_n2977# 6.34fF

C12 cla4_0/and_0/a Gnd 5.54fF

C13 pdblock_3/pblock_0/not_1/vout Gnd 2.98fF

C14 bd Gnd 6.19fF

C15 pdblock_3/pblock_0/not_0/vout Gnd 3.22fF

C16 ad Gnd 3.04fF

C17 pdblock_3/pblock_0/exor2_0/w_n66_n9# Gnd 2.46fF

C18 pdblock_3/and_0/w_n91_n4# Gnd 2.17fF

C19 pdblock_2/pblock_0/not_1/vout Gnd 2.98fF

C20 bc Gnd 6.11fF

C21 pdblock_2/pblock_0/not_0/vout Gnd 3.22fF

C22 ac Gnd 3.04fF

C23 pdblock_2/pblock_0/exor2_0/w_n66_n9# Gnd 2.46fF

C24 cla4_0/and_0/b Gnd 53.04fF

C25 pdblock_2/and_0/w_n91_n4# Gnd 2.17fF

C26 cla3_0/and4_0/b Gnd 49.40fF

C27 pdblock_1/pblock_0/not_1/vout Gnd 2.98fF

C28 bb Gnd 6.21fF

C29 pdblock_1/pblock_0/not_0/vout Gnd 3.22fF

C30 ab Gnd 3.02fF

C31 pdblock_1/pblock_0/exor2_0/w_n66_n9# Gnd 2.46fF

C32 pdblock_1/and_0/w_n91_n4# Gnd 2.17fF

C33 cla2_0/and3_0/c Gnd 116.38fF

C34 pdblock_0/pblock_0/not_1/vout Gnd 2.98fF

C35 ba Gnd 6.20fF

C36 pdblock_0/pblock_0/not_0/vout Gnd 3.22fF

C37 aa Gnd 3.03fF

C38 pdblock_0/pblock_0/exor2_0/w_n66_n9# Gnd 2.46fF

C39 cla2_0/and_0/b Gnd 107.87fF

C40 pdblock_0/and_0/w_n91_n4# Gnd 2.17fF

C41 s4 Gnd 2.96fF

C42 pblock_3/not_0/vout Gnd 3.22fF

C43 m1_981_n2115# Gnd 22.32fF

C44 pblock_3/exor2_0/w_n66_n9# Gnd 2.46fF

C45 cla2_0/NOR3_0/OUTPUT Gnd 21.17fF

C46 cla2_0/NOR3_0/w_n21_25# Gnd 2.37fF

C47 cla2_0/and_0/w_n91_n4# Gnd 2.17fF

C48 cla2_0/and3_0/w_n75_n9# Gnd 2.55fF

C49 VDD Gnd 22.37fF

C50 pblock_2/not_1/vout Gnd 2.33fF

C51 pblock_2/not_0/vout Gnd 3.22fF

C52 pblock_2/exor2_0/vdd Gnd 5.39fF

C53 pblock_2/exor2_0/w_n66_n9# Gnd 2.46fF

C54 pblock_1/not_1/vout Gnd 2.33fF

C55 pblock_1/not_0/vout Gnd 3.22fF

C56 pblock_1/exor2_0/w_n66_n9# Gnd 2.46fF

C57 pblock_0/not_1/vout Gnd 2.33fF

```
C58 m1_n610_n2977# Gnd 2.50fF
C59 pblock_0/not_0/vout Gnd 3.22fF
C60 pblock_0/not_0/vdd Gnd 2.65fF
C61 pblock_0/exor2_0/w_n66_n9# Gnd 2.46fF
C62 cla3_0/and_0/w_n91_n4# Gnd 2.17fF
C63 cla3_0/and3_0/w_n75_n9# Gnd 2.55fF
C64 cla3_0/and4_0/w_n75_0# Gnd 3.50fF
C65 cla4_0/AND5_0/w_n59_n15# Gnd 6.54fF
C66 cla4_0/OR5_0/w_n38_n3# Gnd 4.09fF
C67 cla4_0/OR5_0/D Gnd 6.79fF
C68 cla4_0/and_0/w_n91_n4# Gnd 2.17fF
C69 cla4_0/and3_0/b Gnd 3.18fF
C70 cla4_0/and3_0/w_n75_n9# Gnd 2.55fF
C71 cla4_0/OR5_0/C Gnd 5.20fF
C72 cla4_0/and4_0/d Gnd 4.73fF
C73 cla4_0/and4_0/c Gnd 3.74fF
C74 cla4_0/and4_0/b Gnd 3.95fF
C75 cla4_0/and4_0/w_n75_0# Gnd 3.50fF
C76 cla4_0/OR5_0/B Gnd 2.04fF
.tran 10p 1000p
.end
```

The propagate and generate block has a vertical pitch as well as the CLA block. The sum block has a horizontal pitch.

Verilog HDL

Code:

```
module cla(a1,a2,a3,a4,b1,b2,b3,b4,s1,s2,s3,s4);
  input a0,a1,a2,a3,a4,b1,b2,b3,b4,c1;
```

```
  output s1,s2,s3,s4,c5;
  wire
p1,p2,p3,p4,c1,c2,c3,c4,t1,t2,t3,t4,t5,t6,t7,t8,t9,t10,t11,t12,t13,t14
,t15,t16;
  xor G1(p1,a1,b1);
  xor G2(p2,a2,b2);
  xor G3(p3,a3,b3);
  xor G4(p4,a4,b4);
  and n1(g1,a1,b1);
  and n2(g2,a2,b2);
  and n3(g3,a3,b3);
  and n4(g4,a4,b4);

  //C1
  assign c1=g1;

  //C2
  and G1(t1,p1,c1);
  or G2(c2,t1,g1);

  //C3
  and G3(t2,p2,g1);
  and G4(t3,c1,p2,p1);
  or G5(c3,t3,g2);

  //C4
  and G6(t4,p3,g2);
  and G7(t5,p3,p2,g1);
  and G8(t6,p3,p2,p1,c1);
  or G9(c4,t4,t5,t6,g3);
```

```
  //C5
  and G10(t7,p4,g3);
  and G11(t8,p4,p3,g2);
  and G12(t9,p4,p3,p2,g1);
  and G13(t10,p4,p3,p2,p1,c1);
  or G14(c5,t7,t8,t9,t10,g4);

  //sum
  xor W1(s1,p1,c2);
  xor W2(s2,p2,c3);
  xor W3(s3,p3,c4);
  xor W4(s4,p4,c5);

endmodule
```

Testbench:

```
module tb;
reg c1,a1,a2,a3,a4,b1,b2,b3,b4;
wire s1,s2,s3,s4,c5;
cla
uut(.c1(c1),.a1(a1),.a2(a2),.a3(a3),.a4(a4),.b1(b1),.b2(b2),.b3(b3),.b
4(b4),.s1(s1),.s2(s2),.s3(s3),.s4(s4),.c5(c5));

initial begin
$dumpfile("cla.vcd");
  $dumpvars(0,tb);

  $monitor($time," A=%b%b%b%b B=%b%b%b%b Cout=%b
S=%b%b%b%b",a4,a3,a2,a1,b4,b3,b2,b1,c1,s4,s3,s2,s1);
    c1 = 1'b1;
```

```
    a1 = 1'b1;
    b1 = 1'b1;
    a2 = 1'b1;
    b2 = 1'b1;
    a3 = 1'b1;
    b3 = 1'b1;
    a4 = 1'b1;
    b4 = 1'b1;
    #2560 $finish;
end

always #5 a1 = ~a1;
always #10 b1 = ~b1;
always #20 a2 = ~a2;
always #40 b2 = ~b2;
always #80 a3 = ~a3;
always #360 b3 = ~b3;
always #420 a4 = ~a4;
always #640 b4 = ~b4;
always #1280 c1 = ~c1;

endmodule
```