ECE463: Digital VLSI Design

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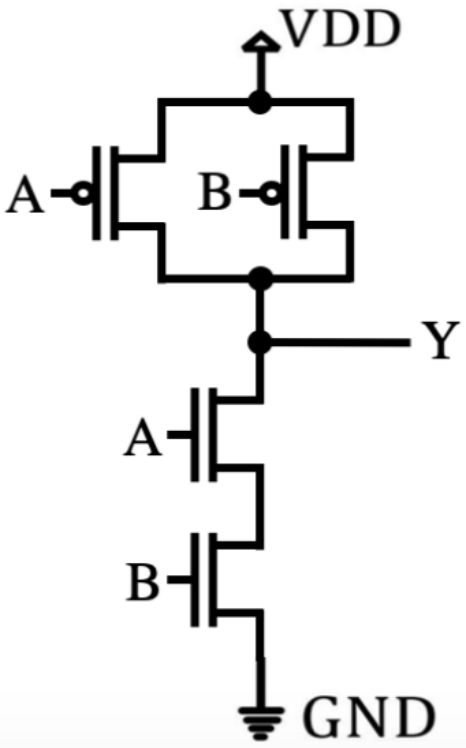
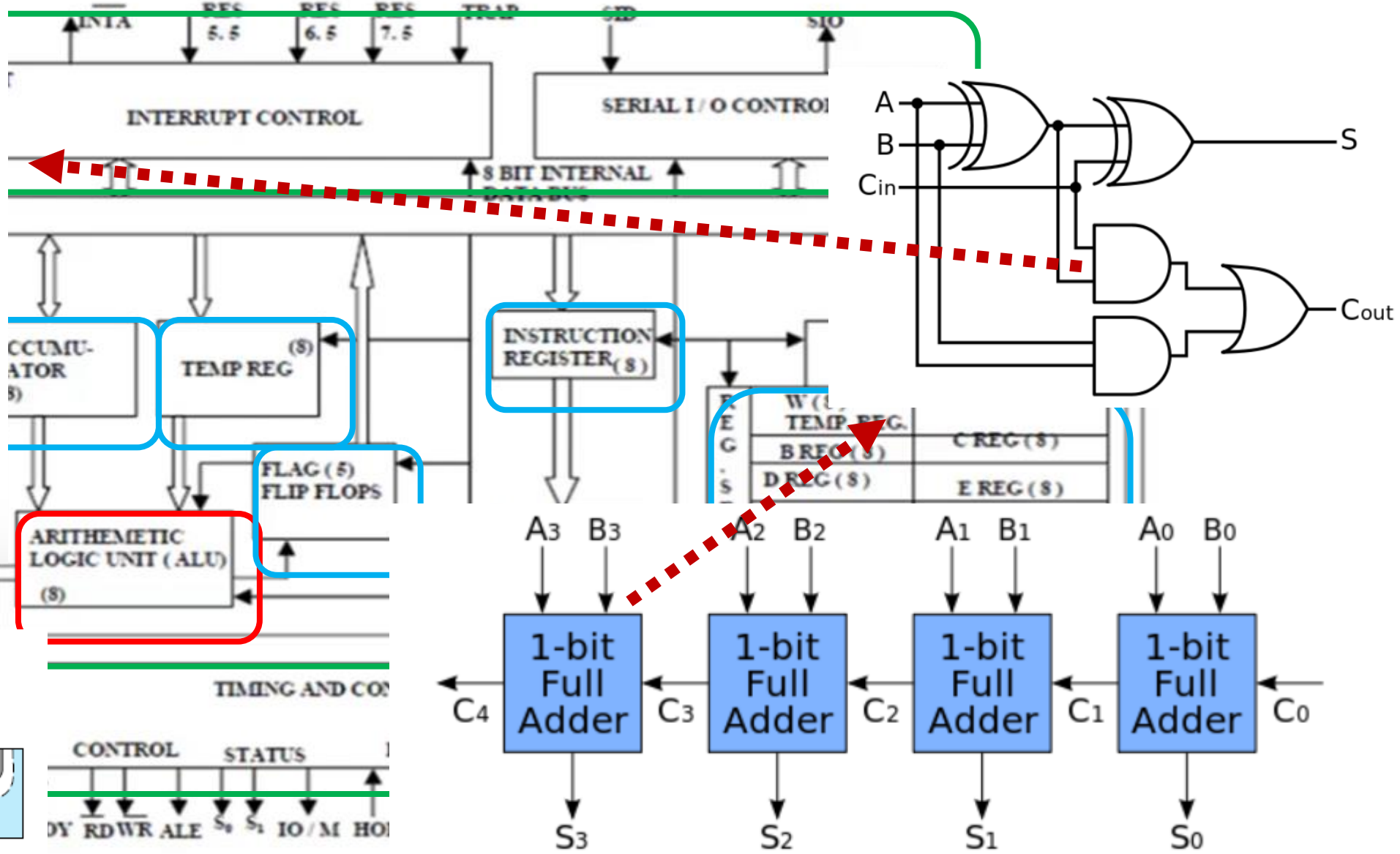
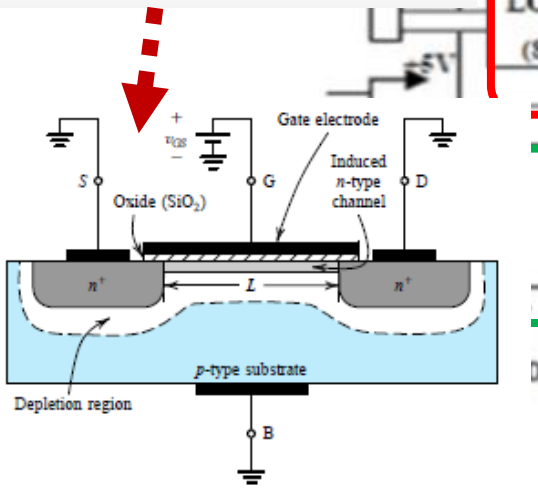
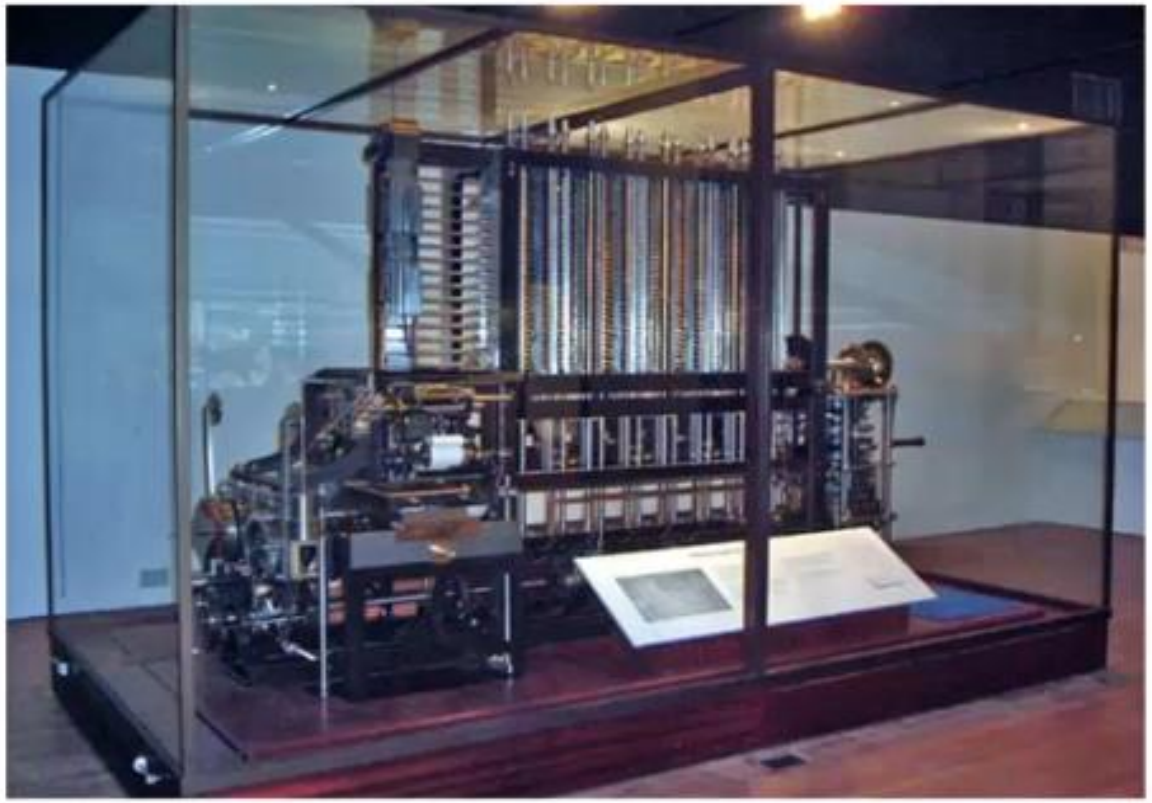
8085 microprocessor







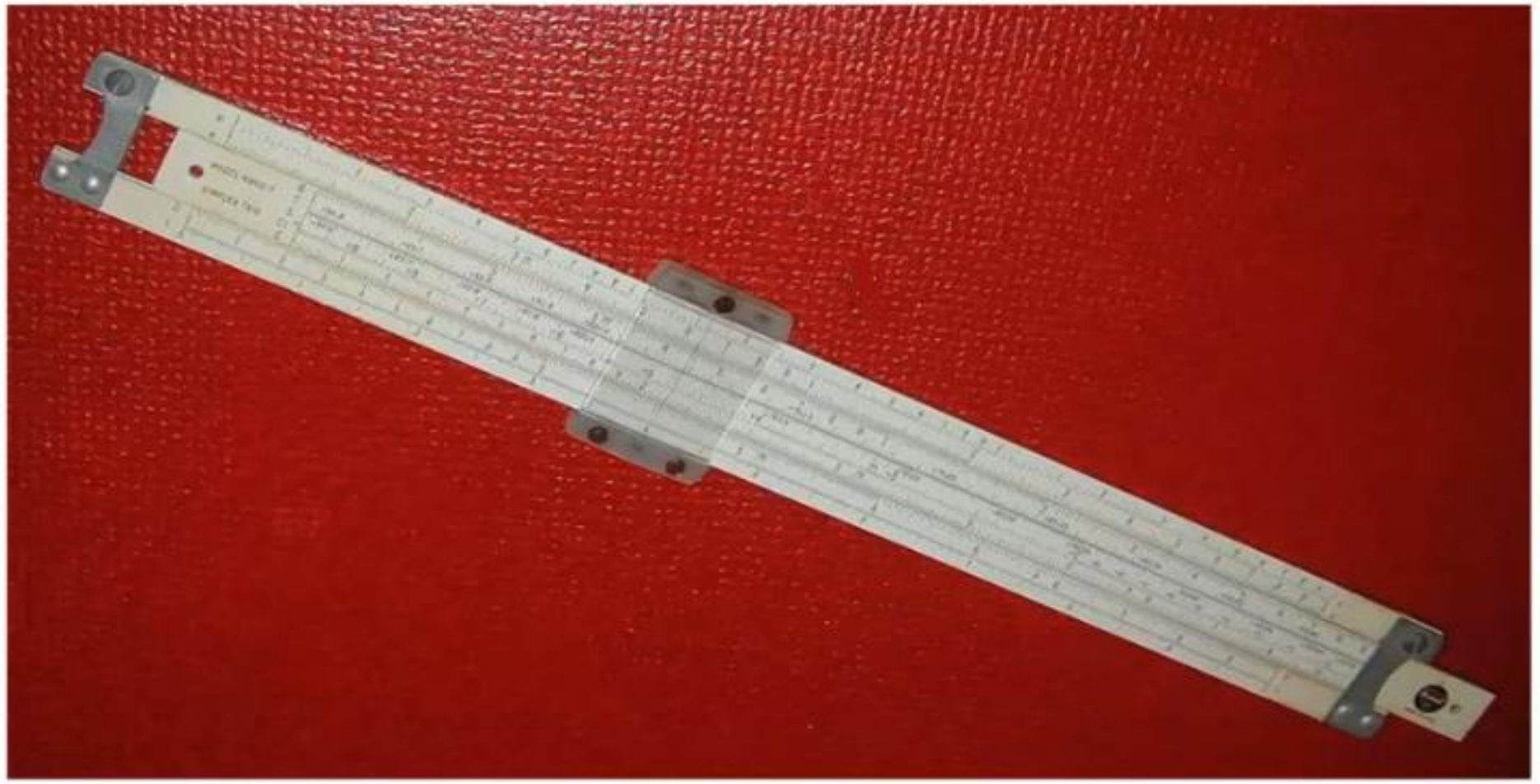
Before the advent of Electronics



The London Science Museum's working difference engine, built a century and a half after Charles Babbage's design….wikipedia

In 1822, Charles Babbage presented a small cogwheel assembly that demonstrated the operation of his difference engine, a mechanical calculator which would be capable of holding and manipulating seven numbers of 31 decimal digits each. It was the first time that a calculating machine could work automatically using as input results from its previous operations It was the first calculating machine to use a printer.

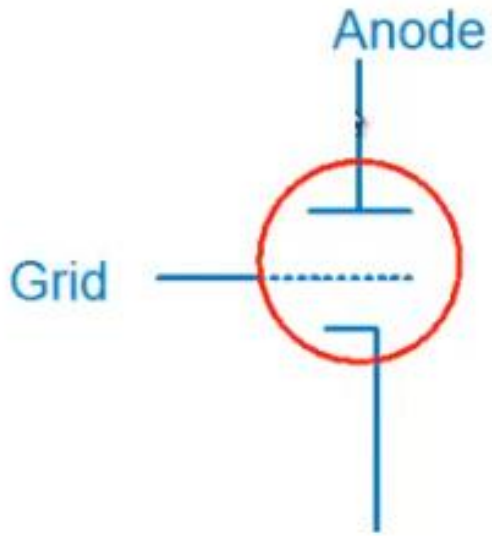
Slide Rule

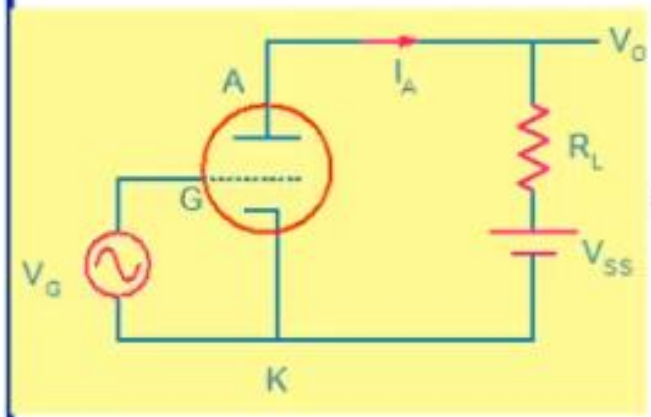


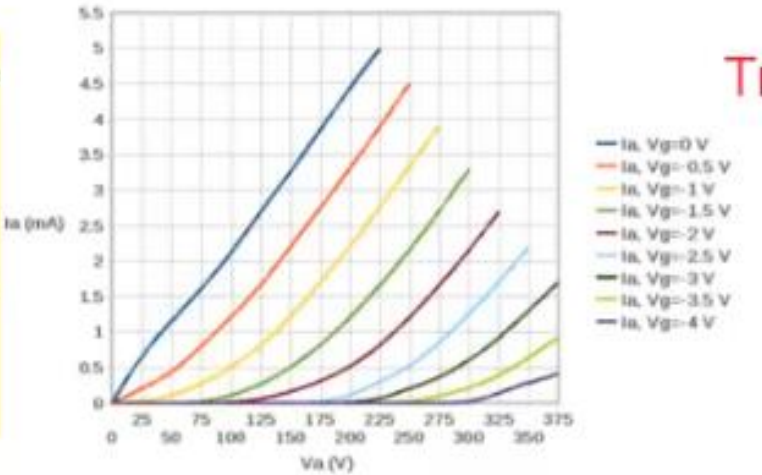
source ….wikipedia

The Electronics revolution started with the invention of the Triode (1906)

Lee De Forest : 1873-1961



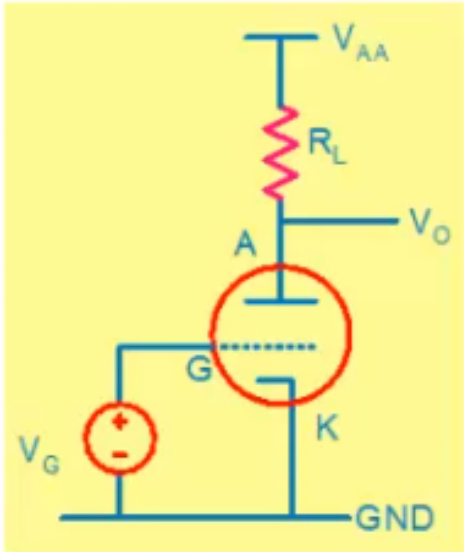




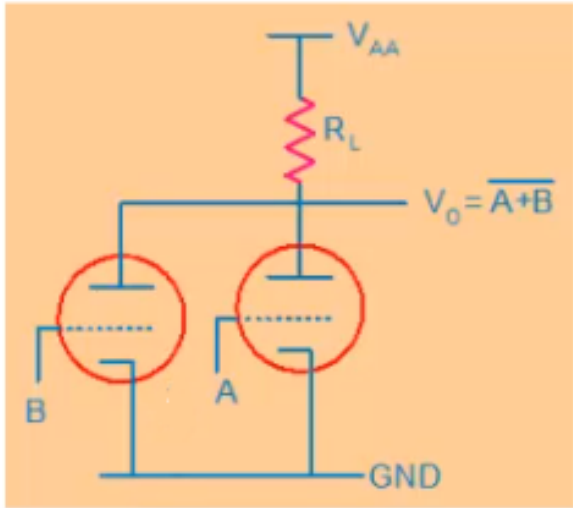
Transconductance

$$\frac{\partial I_A}{\partial V_G}$$

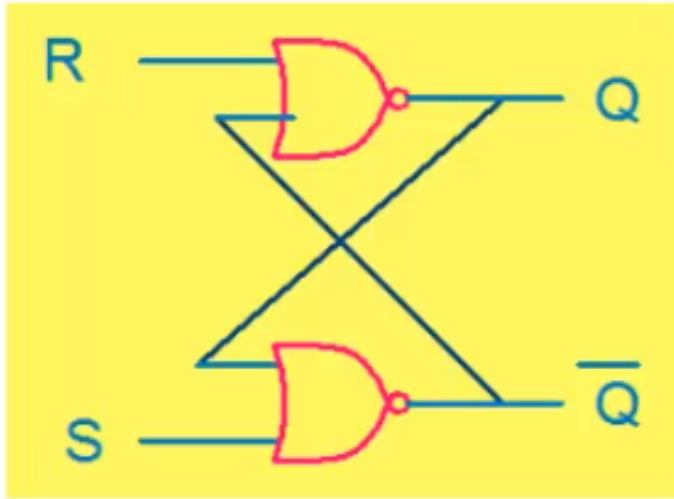
Triode revolutionized information processing



Inverter

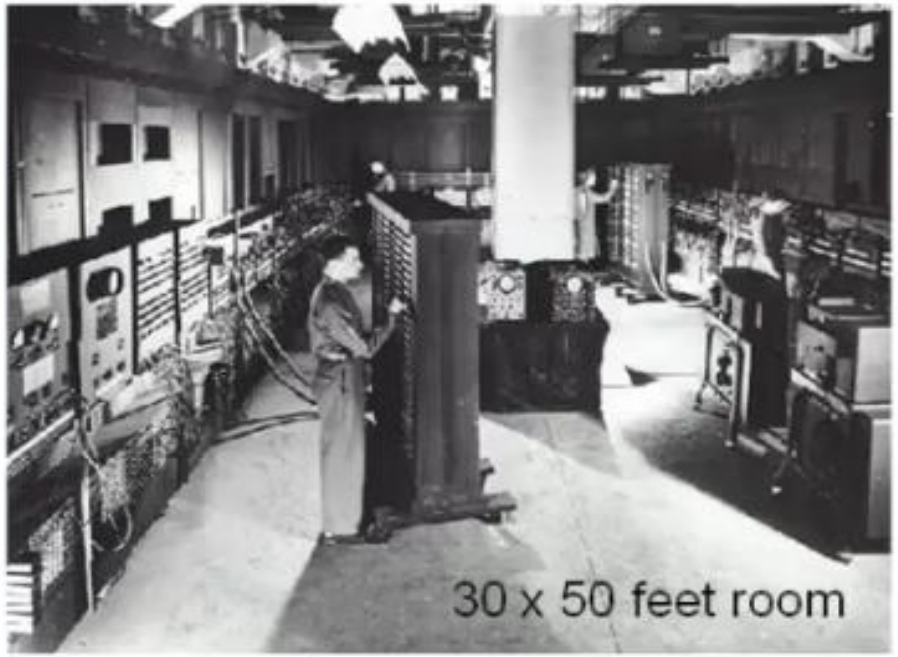


NOR



NOR Latch

Triode enabled Processing, Storage and Communication, of Information



ENIAC: Electronic numerical Integrator and computer: 1946

The ENIAC contained 17,468 vacuum tubes, along with 70,000 resistors, 10,000 capacitors, 1,500 relays, 6,000 manual switches and 5 million soldered joints

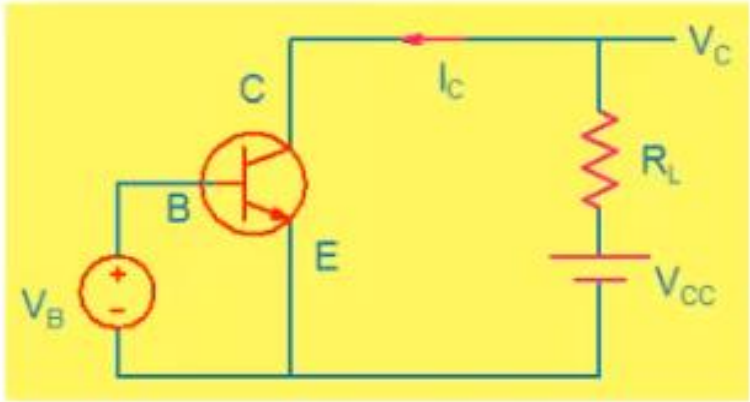
It weighed **30 tons**, consumed **160 kilowatts** of electrical power,

Records from 1952 show that approximately 19,000 vacuum tubes had to be replaced in that year alone, which averages out to about **50 tubes a day**!

- Although the seed of information revolution was there in Triode itself, it was difficult to harness it

Transistor: 1948

Two CK703 germanium crystal triodes shown with a 1U4 tube for size comparison.



$$\frac{\partial I_C}{\partial V_{BE}} >> \frac{\partial I_C}{\partial V_{CE}}$$

$$\Rightarrow \frac{\partial V_{CE}}{\partial V_{BE}} >> 1$$

A Transistor could do most of what a triode could do and it was smaller, consumed less power and was more reliable

What occupied a room earlier, now occupied a table top

-530 germanium transistors and 2300 diodes.

-Size 420 x 440 x 250 mm (16.5" x 17.3" x 9.8"), 25Kg

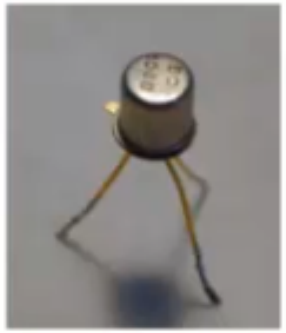
-Cost 535 thousand yen (about US$1,490)

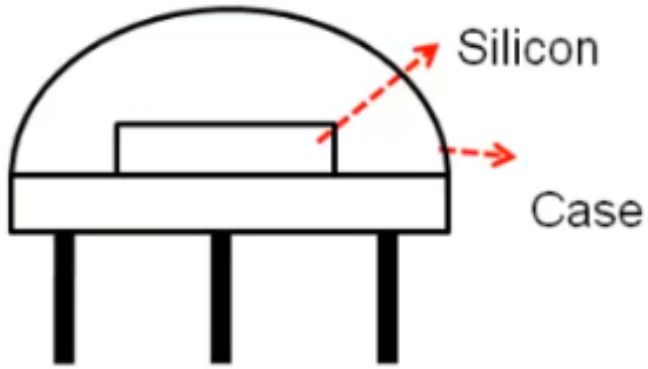
-90 Watts of power

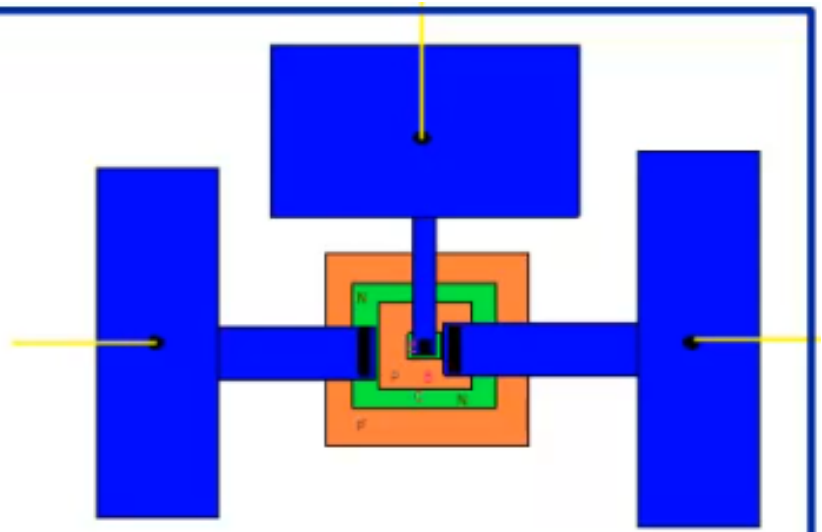
Sharp *CS-10A, 1964*

Integration level was better but still limited

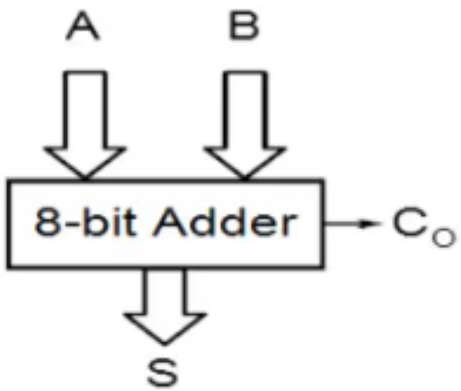
Discrete Circuit

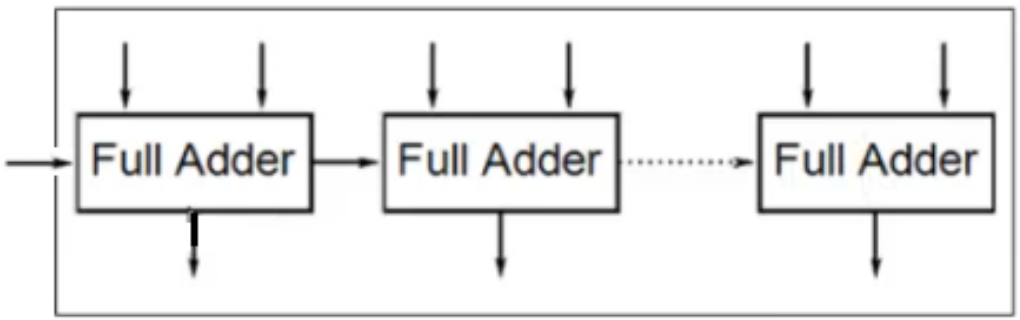






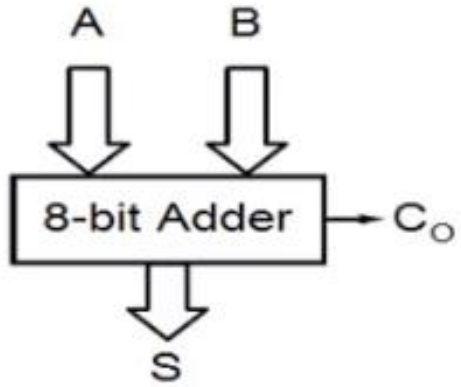
8-bit adder

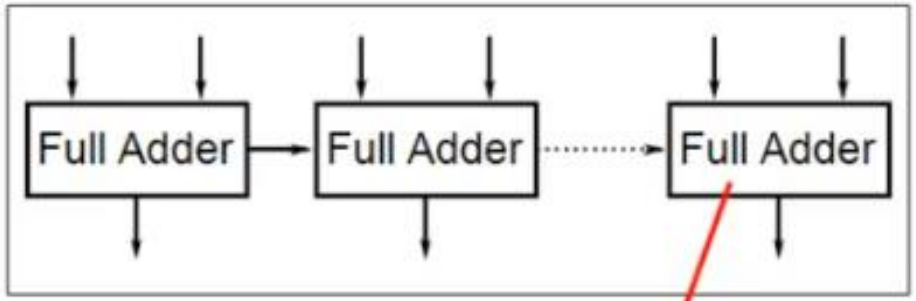


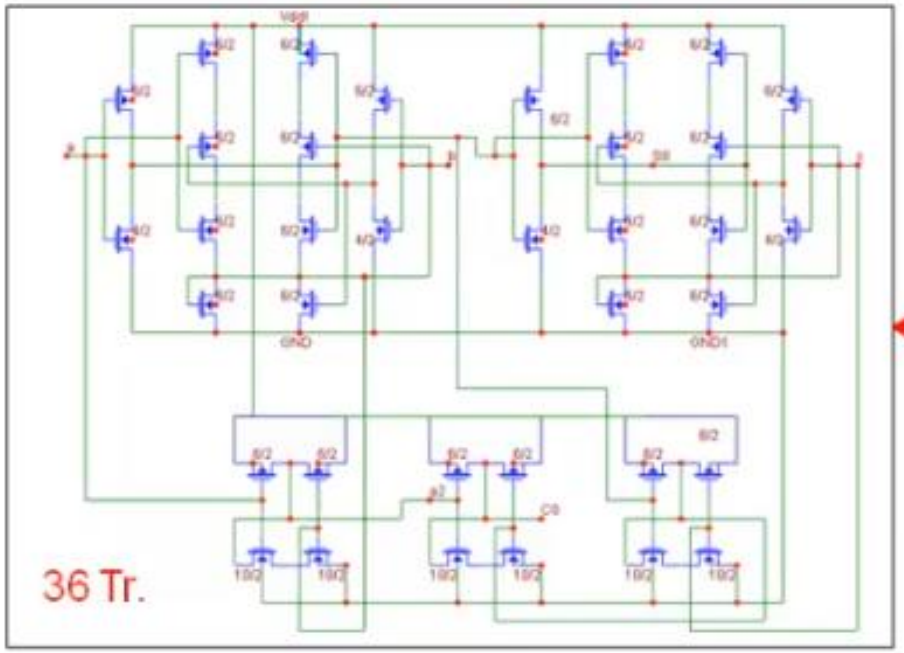


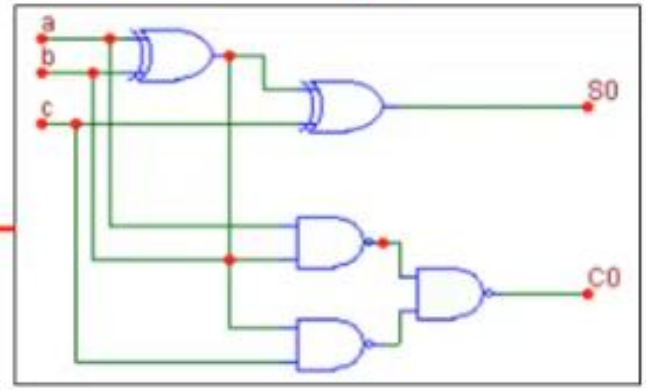
8-bit adder

288 Tr.

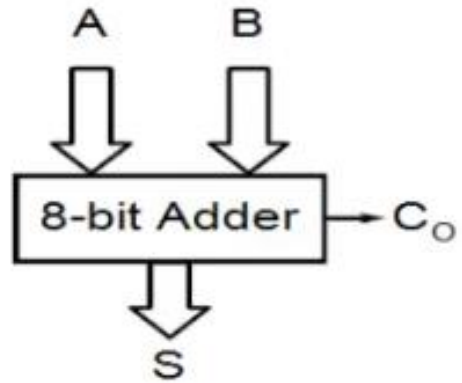




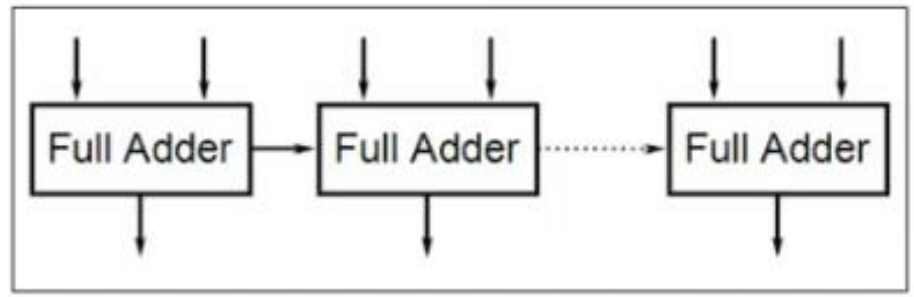




Discrete Transistor Circuit



288 Tr.



$$\sim 120\ \text{cm}^2 \sim 11\text{cm} \times 11\text{cm}$$

$$\sim \frac{24\ \text{Tr}}{10\ \text{cm}^2} \sim 2.4\ \text{Tr/cm}^2$$

24k would occupy 1m x 1m !

Integrated Circuit : 1958

Jack Kilby

Robert Noyce

Phase shift oscillator

March 24, 1959: Texas Ins. demonstrated an Integrated multivibrator with the discrete equivalent of two capacitors, eight resistors, and two diffused - base transistors; and a phase-shift oscillator, with the equivalent of three capacitors, five resistors, and one transistor.

In a press release, the company wrote that "they are considered to approach the ultimate in miniaturizing complex electronic circuitry and components."

- In October 1961, the company announced its Series 51, with five different digital-circuit logic modules—flip-flops, counters, NOR gates, NAND gates, and exclusive ORs. They cost $95 in sample quantities and $65 each in quantities of 100.

Nobel prize in Physics 2000

Monolithic Integration

Fig. 8b

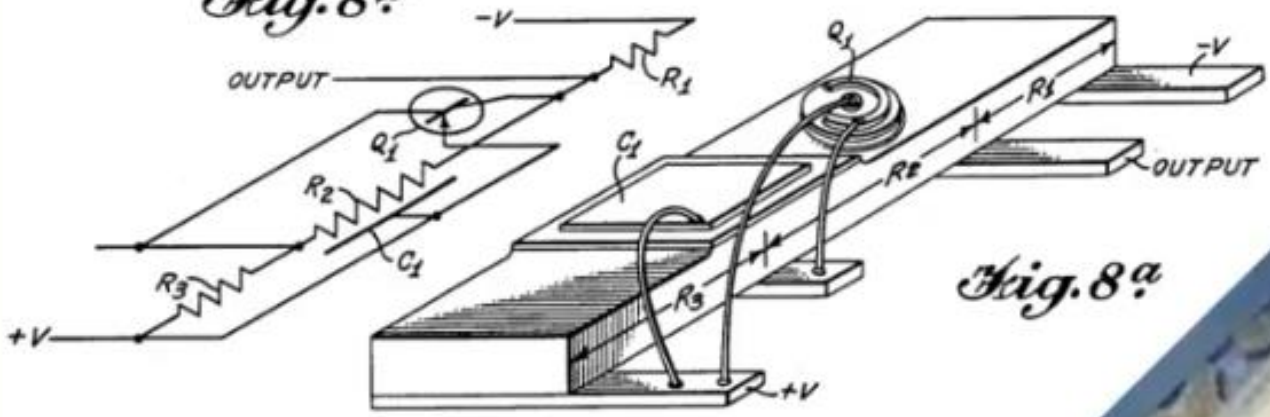


Fig. 8a

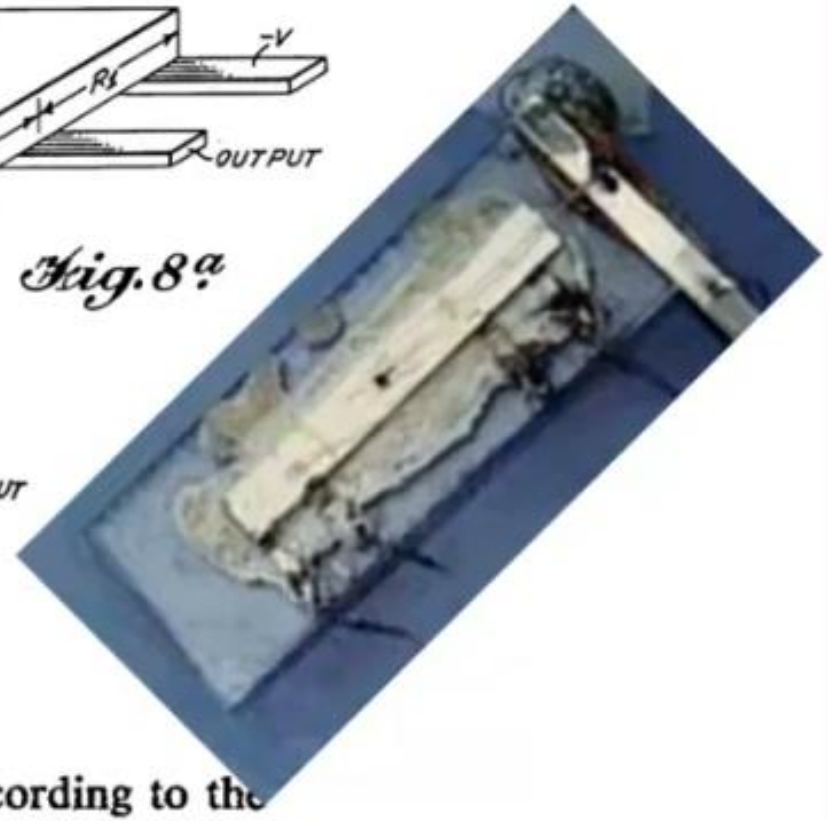
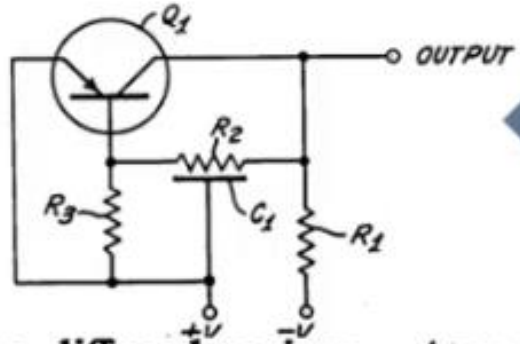
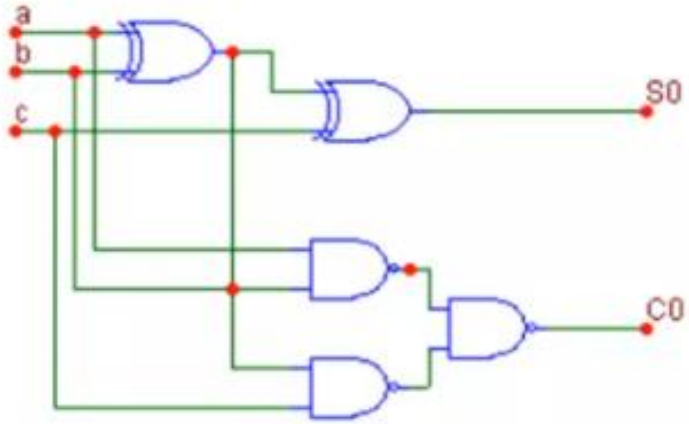


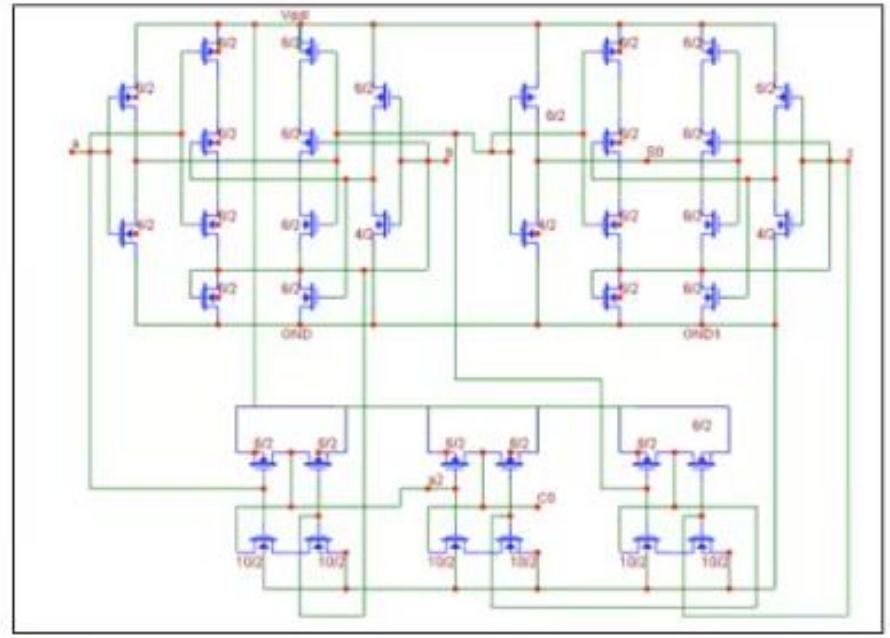
Fig. 8c

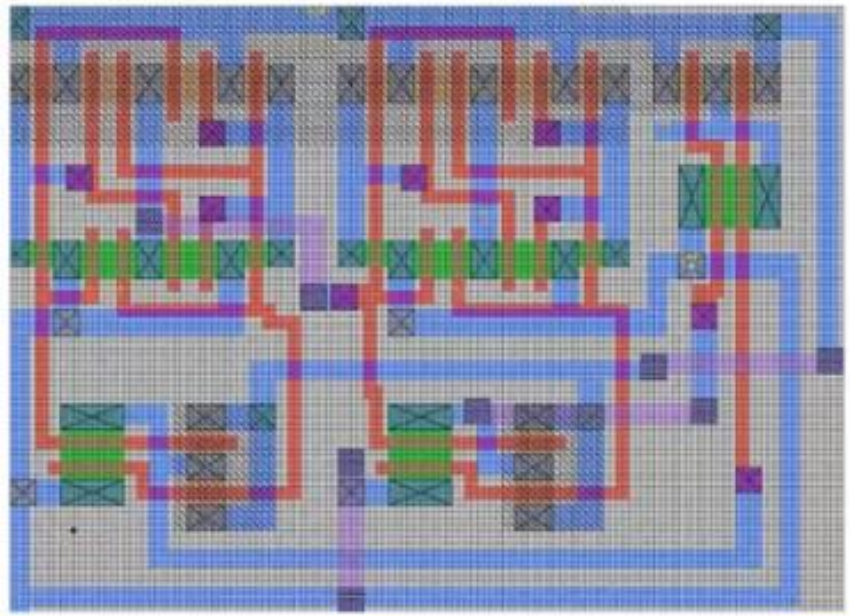


Jack S. Kilby
INVENTOR

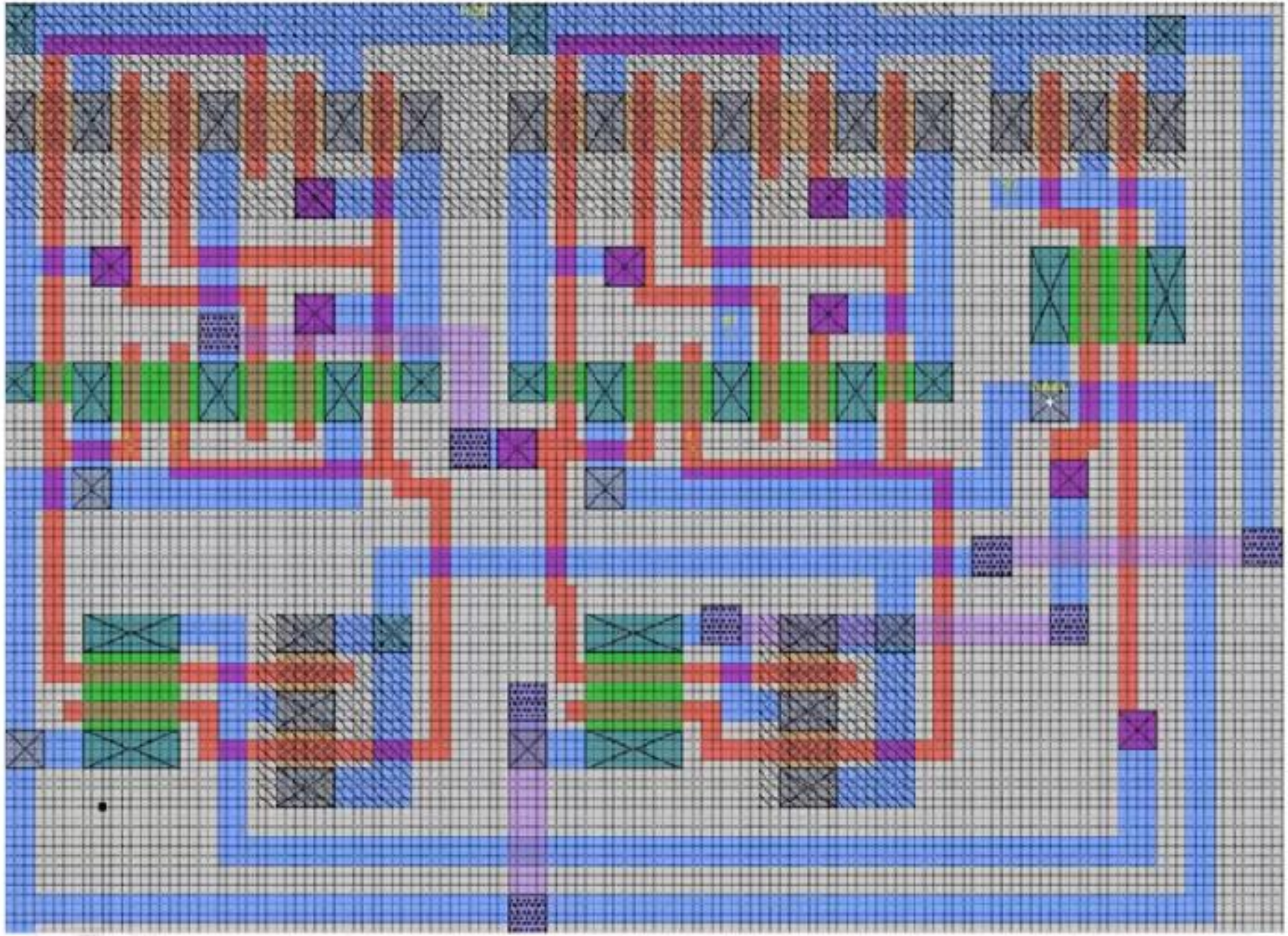
case may be, between diffused regions. According to the principles of this invention, all components of an entire electronic circuit are fabricated within the body so characterized by adapting the novel techniques to be described in detail hereinafter. It is to be noted that all components of the circuit are integrated into the body of semiconductor material and constitute portions thereof.





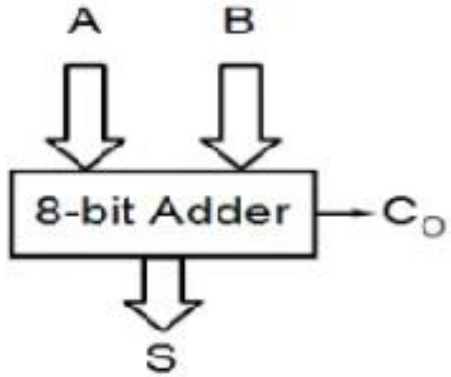


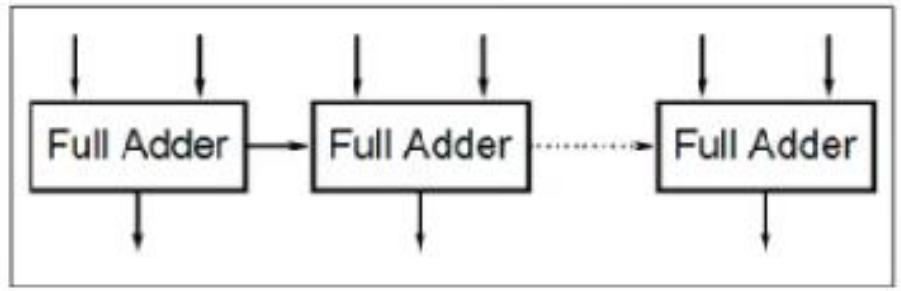
~66μm×48μm
for 1μm technology

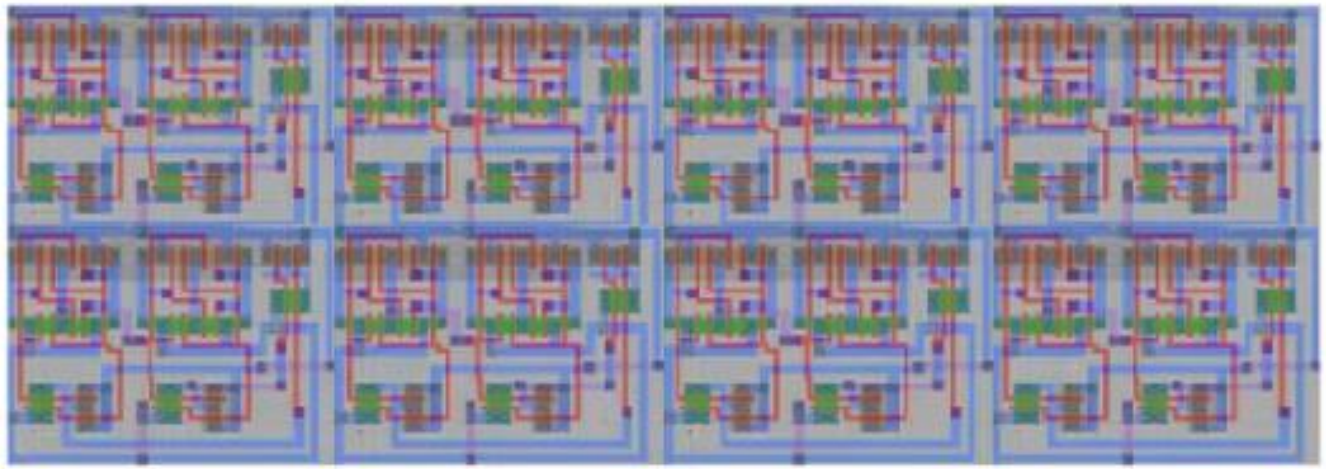


Monolithic implementation

288 Tr.

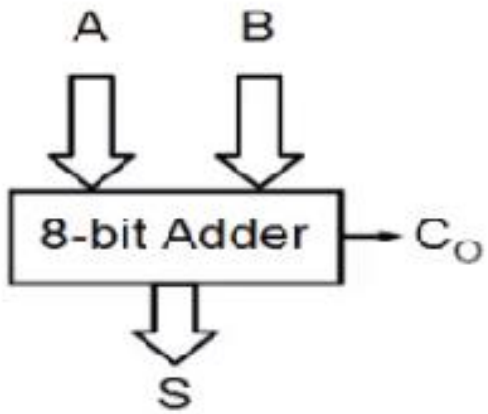


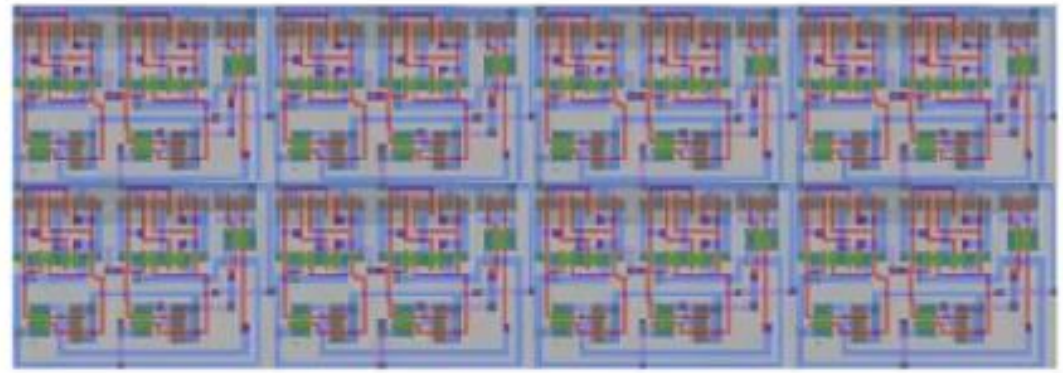




~270μm×100μm

Packaged IC



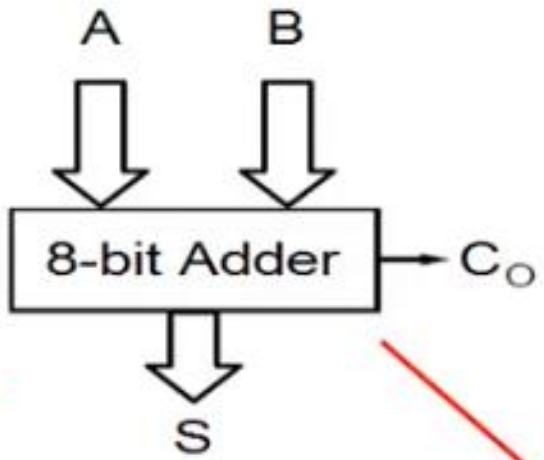


~270μm×100μm

Length ~2.5×14 = 35mm

Width~7.62mm

Discrete vs. Monolithic Circuit

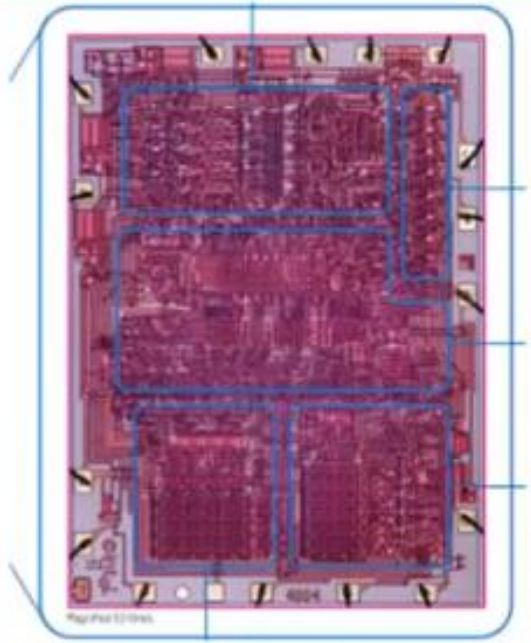


288 Tr circuit.

~120 cm^2 ~11cm×11cm

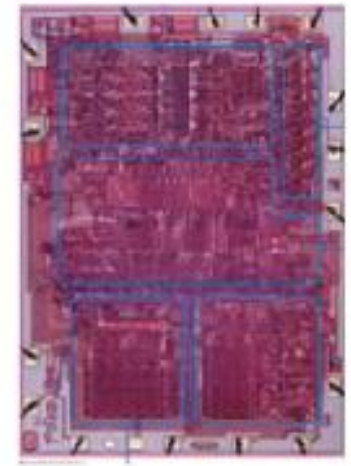
~ 35mm × 7.62mm

The first microprocessor sold by Intel was the four-bit 4004 in 1971. It was designed to work in conjunction with three other microchips, the 4001 ROM, 4002 RAM and the 4003 Shift Register. It had 2300 transistors designed using a 10um PMOS process. Maximum clock rate was 740kHz

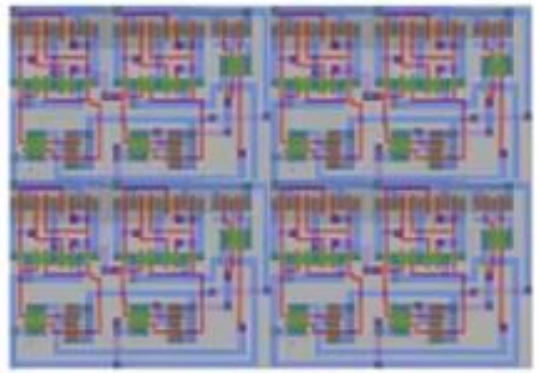


This revolutionary microprocessor, measuring 1/8th by 1/6th of an inch—the size of a fingernail—delivered the same computing power as the first electronic computer, the ENIAC*, built in 1946, which filled an entire room and used 18,000 vacuum tubes.

Key Issue: Integration



Increased levels of integration is still challenging



3.3 mm

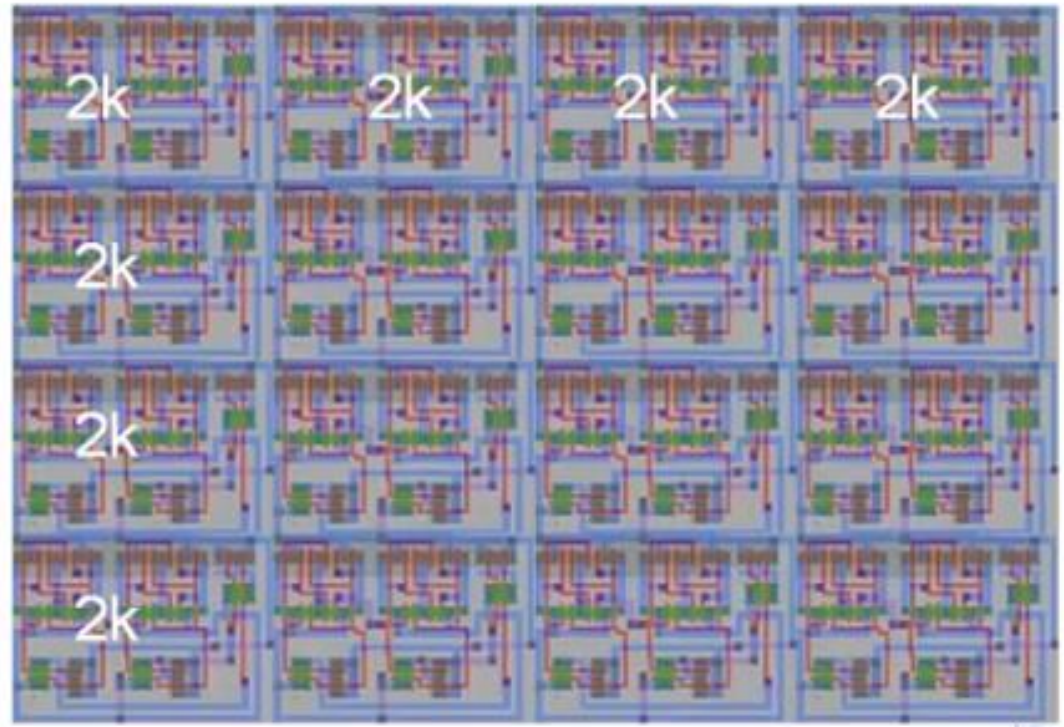
3.3 mm

~2k Tr and die size 10mm^2

~64k Tr

1.32 cm

1.32 cm

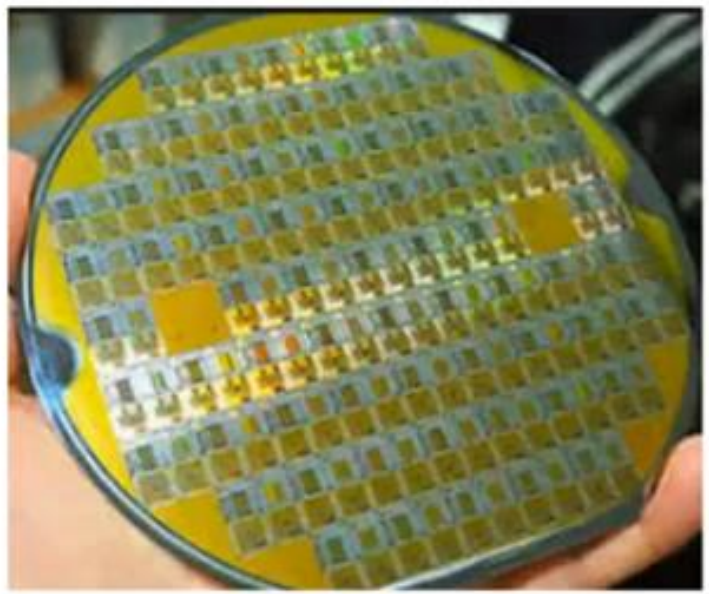


die size 174mm^2

IC Economics

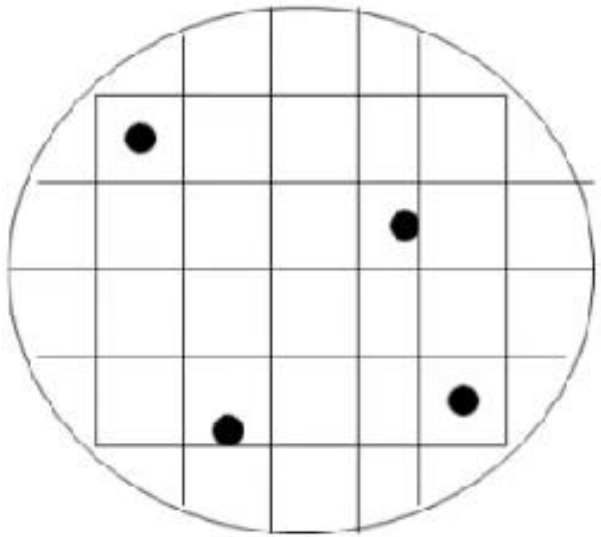
$$\text{IC Cost} = C = \frac{C_{\text{Dev.}}}{N} + C_{\text{Prod.}}$$

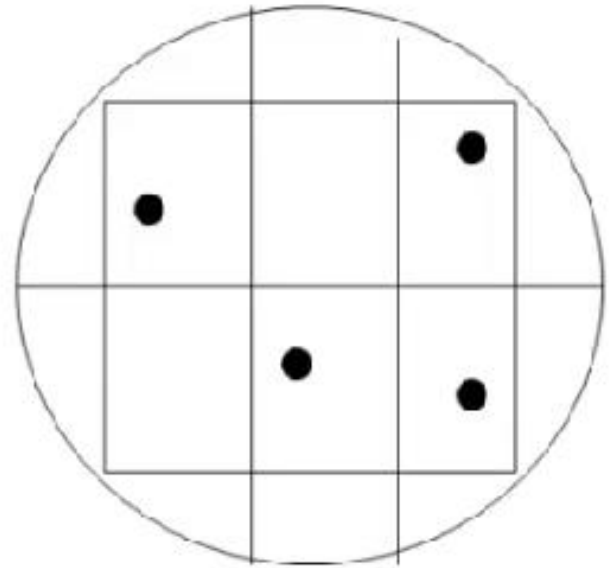
$$C_{\text{Prod.}} = C_{Die} + C_{Pack.} + C_{test}$$



$$C_{Die} \sim \frac{C_{wafer}/\gamma_w}{\left(0.85 A_{wafer}/A_{IC}\right) \times \gamma_d}$$

Yield generally decreases with die size





~16/20 = 80%

~2/6 = 33%

Yield depends on defect density die size

$$C_{Die} \propto A_{IC}^{4}$$

Source: INTEGRATED CIRCUIT ENGINEERING CORPORATION

	16M DRAM (0.35μ)	64M DRAM (0.35μ)
Tested Wafer Cost	$1,180 (200mm)	$1,485 (200mm)
Die Size	84,000 sq mils (54mm^2)	232,500 sq mils (150mm^2)
Total Dice Available	476	162
Probe Yield	80% (at 0.5 defects/cm^2)	40% (at 0.7 defects/cm^2)
Number Of Good Dice	380	65
Package Cost	$0.40	$0.50
Assembly Yield	99%	99%
Final Test Cost	$0.60	$1.20
Final Test Yield	95%	85%
Factory Cost	$4.36	$29.15
ASP	$7.75	$55.00
Approx. Revenue/Wafer Start	$2,770	$3,008
Revenue/Sq In. Started	$55	$60
Gross Margin	44%	47%

Source: ICE

16912G

$$476 / 581 = 0.82$$

$$C_{IC} \sim \frac{\frac{1180}{380} + 0.4 + 0.6}{0.95} = \frac{3.1 + 0.4 + 0.6}{0.95} = 4.3\$$$

	BiCMOS MPU (0.35µ)
Tested Wafer Cost	$1,890 (200mm epi wafer)
Die Size	135,000 sq mils (90mm^2)
Total Dice Available	292
Probe Yield	37% (at 1.2 defects/cm^2)
Number Of Good Dice	108
Package Cost	$25.75 (296-pin CPGA)
Assembly Yield	99%
Final Test Cost	$35.00
Final Test Yield	70%
Factory Cost	$112.41
ASP (1,000)	$350
Approx. Revenue/Wafer Start	$26,195
Revenue/Sq In. Started	$542
Gross Margin	68%

Source: ICE 14448G

Pentium (166MHz P54CS) Cost Analysis (3Q96)

$$C_{IC} \sim \frac{17.5 + 25.75 + 35}{0.7} = \$112$$

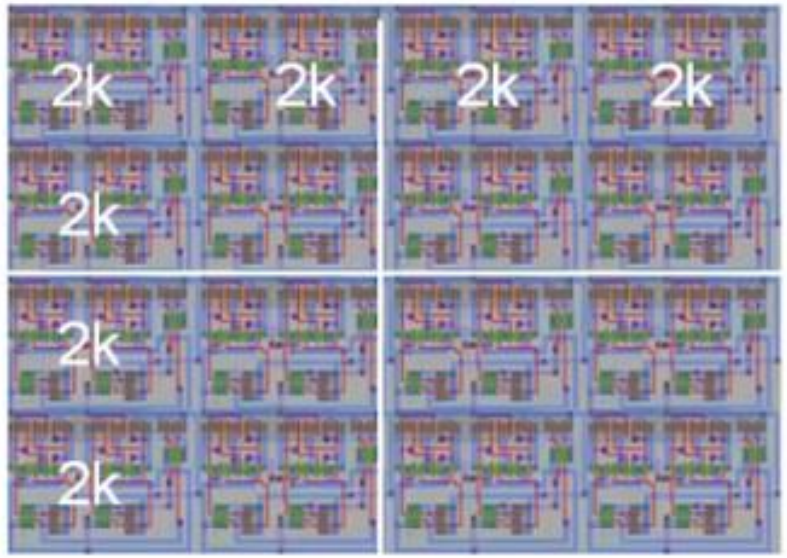
The Pentium FDIV bug was a computer bug that affected the floating point unit (FPU) of the early Intel Pentium processors. Because of the bug, the processor could return incorrect binary floating point results when dividing a number. Intel attributed the error to missing entries in the lookup table used by the floating-point division circuitry.

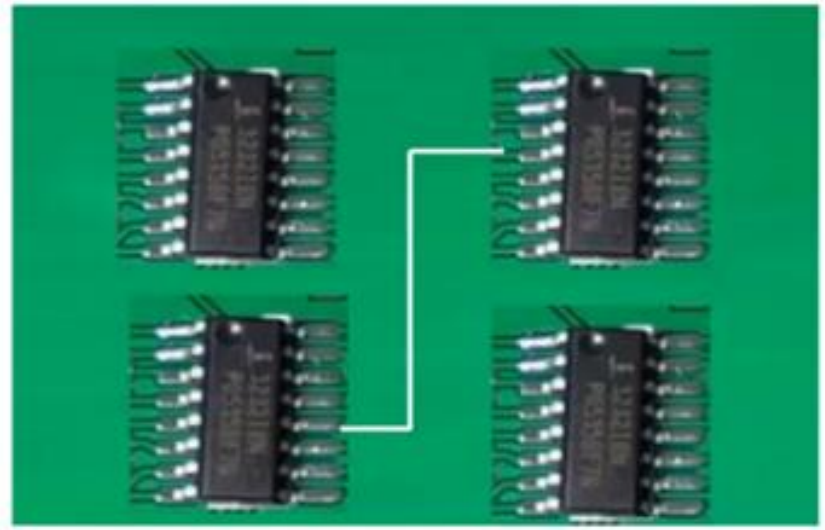
The severity of the FDIV bug is debated. Intel, producer of the affected chip, claims that the common user would experience it once every 27,000 years while IBM, manufacturer of a chip competing with Intel's Pentium, claims that the common user would experience it once every 24 days.

In December 1994, Intel recalled the defective processors. In January 1995, Intel announced "a pre-tax charge of $475 million against earnings, ostensibly the total cost associated with replacement of the flawed processors."....wikipedia

- One cannot simply increase circuit complexity as it result in increased die area, reduced yield and thus unacceptable cost

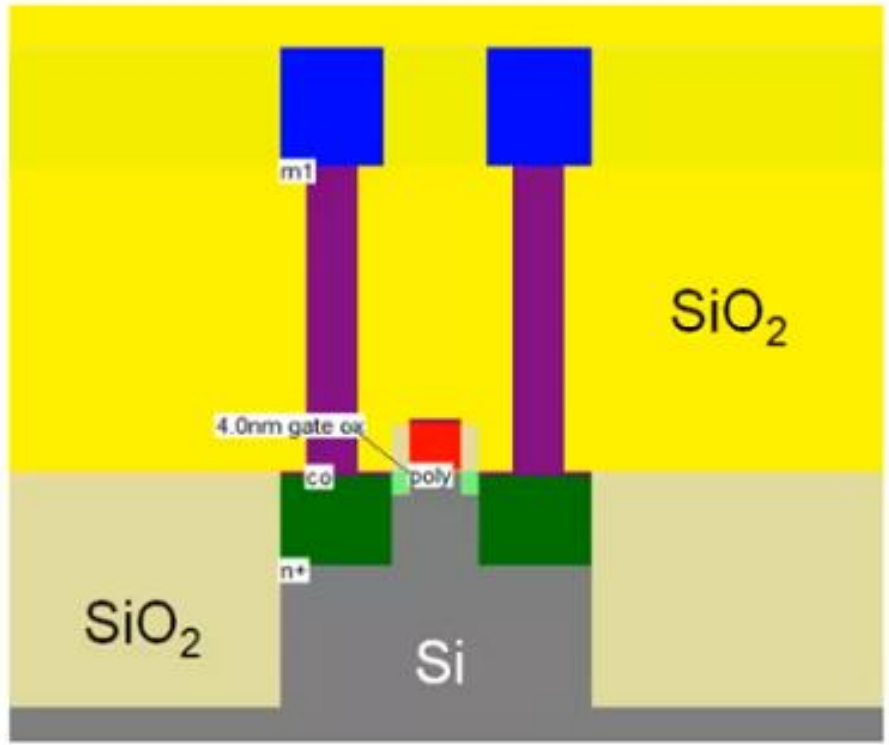
- Once could partition the circuit into a chipset and integrate them on a PCB

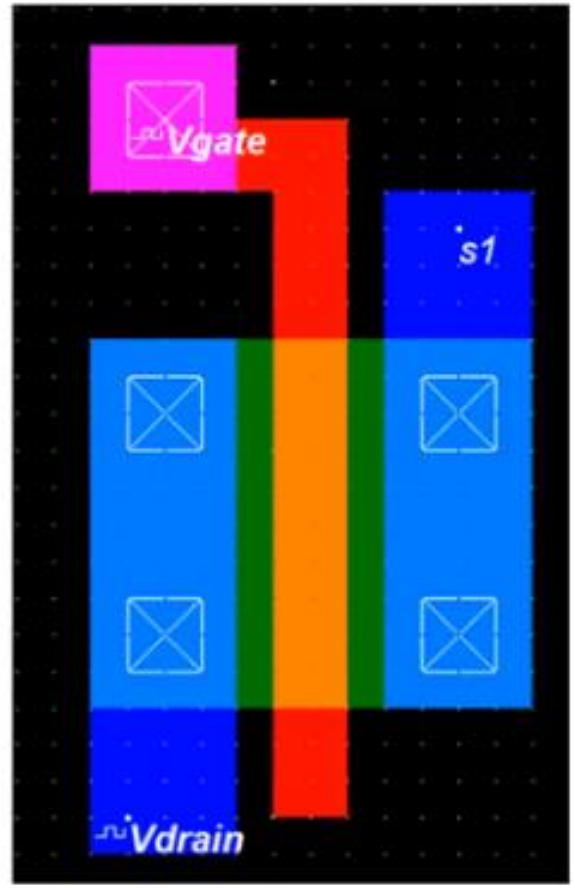




Off-chip interconnects are longer due to which they cause more delay and incur a power penalty as well.

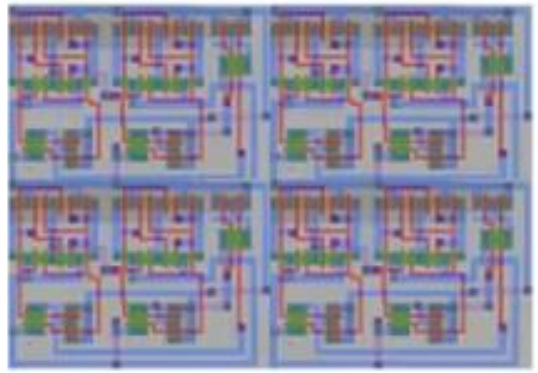
CMOS technology is Scalable





Both horizontal and vertical dimensions can be shrunk to not only reduce area but improve the speed of the transistor as well

CMOS technology is Scalable

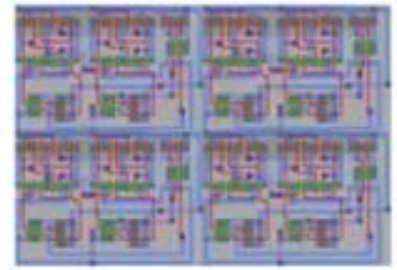


3.3 mm

3.3 mm

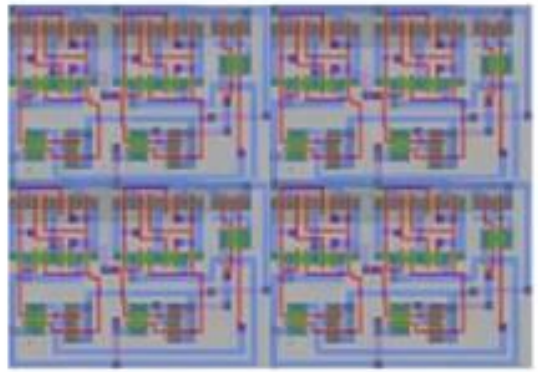
~2k Tr , die size ~10mm^2
For 10µm technology

2 mm



2 mm

~2k Tr , die size ~4mm^2
For 6µm technology



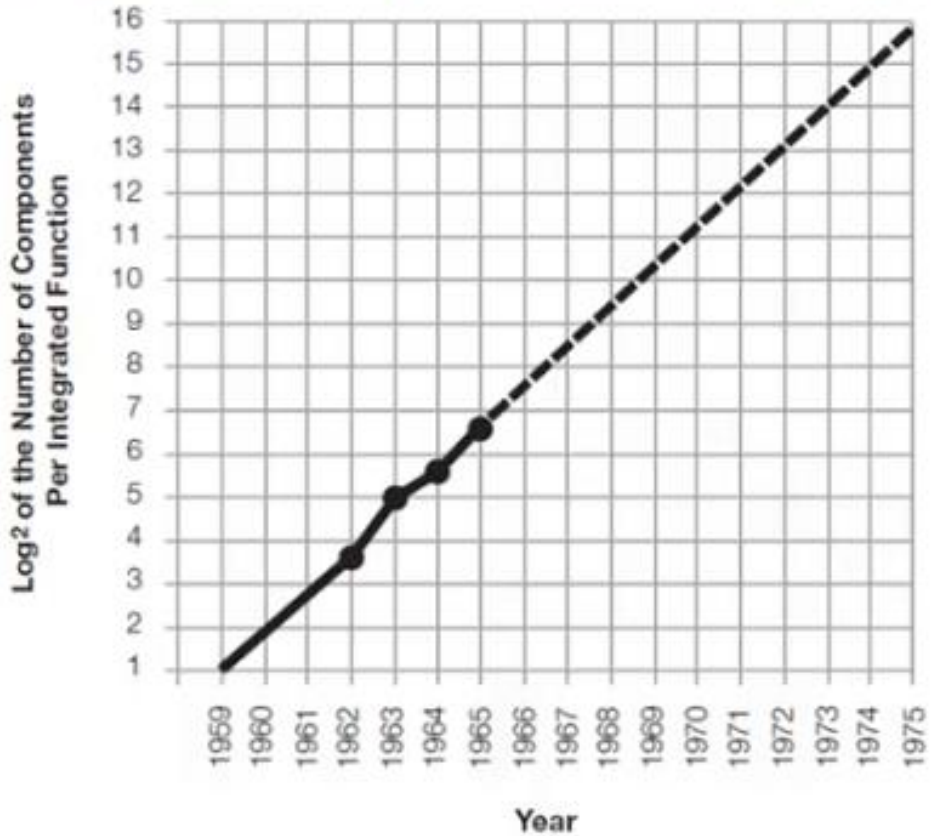
3.3 mm

3.3 mm

~5.5k Tr , die size ~10mm^2
For 6µm technology

Moore's law (1965)

"cramming more components onto integrated circuits"

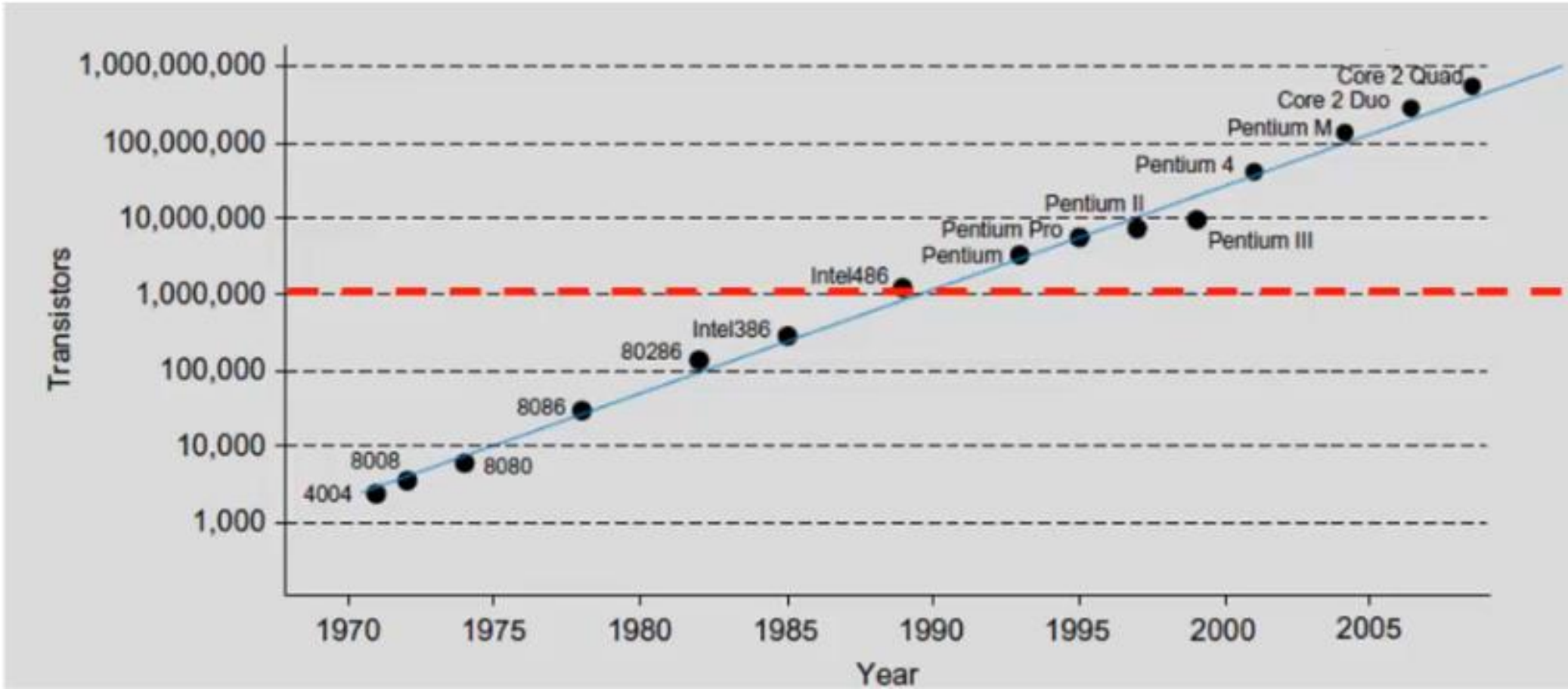


"Complexity of integrated circuits has approximately doubled every year since their introduction. Cost per function has decreased several thousand-fold, while system performance and reliability have been improved dramatically…1975"

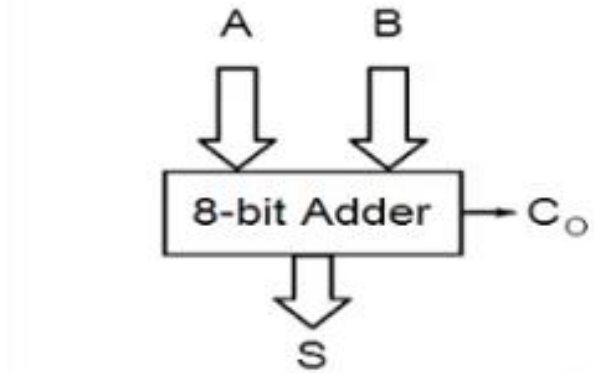
Intel Microprocessors

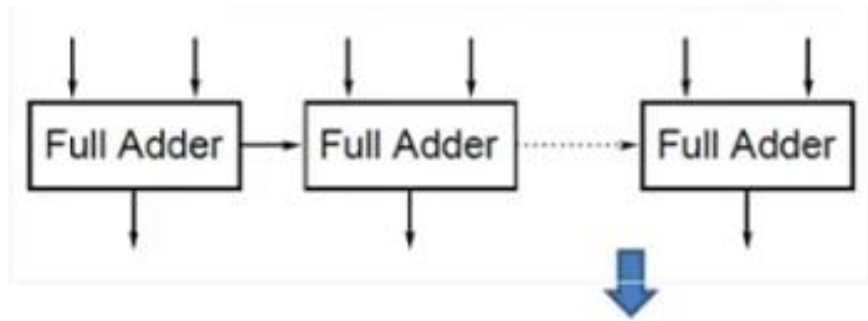
processor	Year	Technology	Transistors	Clock speed
4004	1971	10u	2.3k	740k
C8008	1972	10u	3.5k	500k
8080	1974	6u	4.5k	2M
P8085 (100 million sold)	1976	3u	6.5k	3M
8086 (16 bit)	1978	3u	29k	5M
80186	1982	3u	55k	6M
80286	1982	1.5u	134k	6M
80386 (32 bit)	1985	1.5u	275k	16M

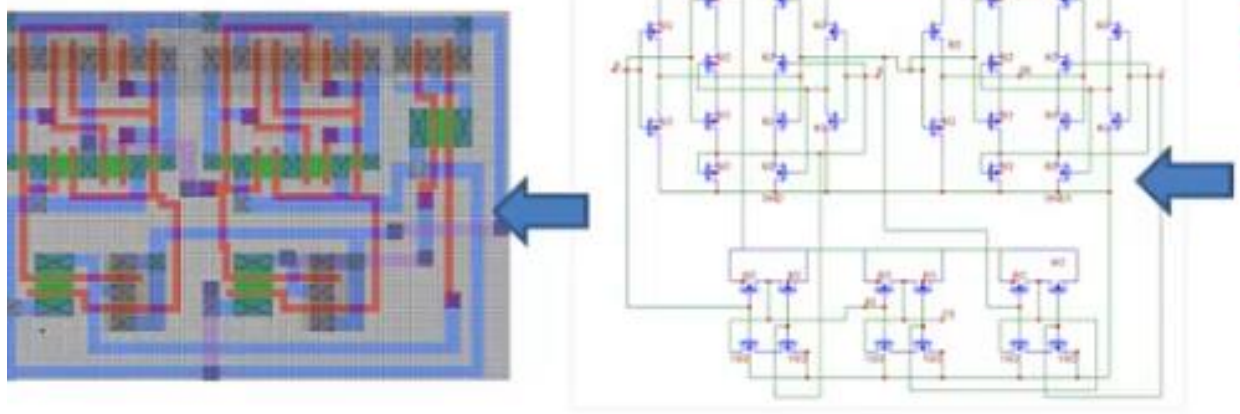
processor	year	technology	transistors	Clock speed
i486	1989	1um	1.2M	25M
pentium	1993	0.8u	3.1M	66M
Pentium pro	1995	0.6u	5.5M	200M
Pentium II	1997	0.25u	7.5M	300M
Pentium III	1999	180n	9.5M	500M
Pentium IV	2000	180nm	42M	1.5G
Pentium M	2002	90nm	55M	1.7G
itanium	2002	130nm	220	1G
Quad core 64 bit	2006	65nm	291M	2.93G

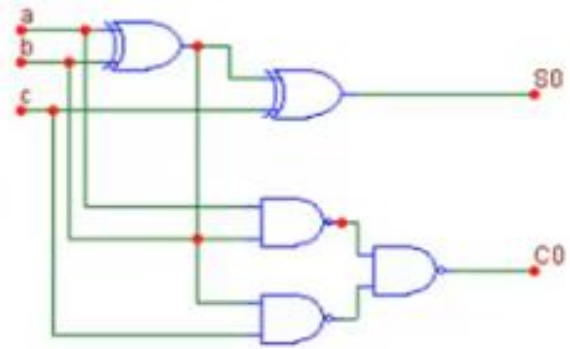

1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
Transistors
1970
1975
1980
1985
1990
1995
2000
2005
Year
4004
8008
8080
8086
80286
Intel386
Intel486
Pentium
Pentium Pro
Pentium II
Pentium III
Pentium 4
Pentium M
Core 2 Duo
Core 2 Quad

▪Digital IC design involves not only logic design but also its translation to transistor schematic and physical layout. It also involves developing test patterns that can be used to test the fabricated circuit



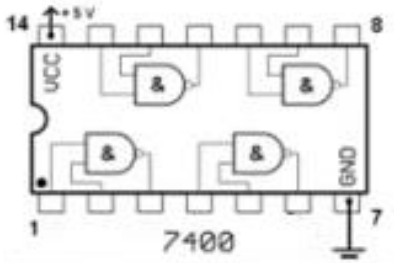






Design is complex requiring high skill, is expensive and time consuming and only justified for very high volume applications

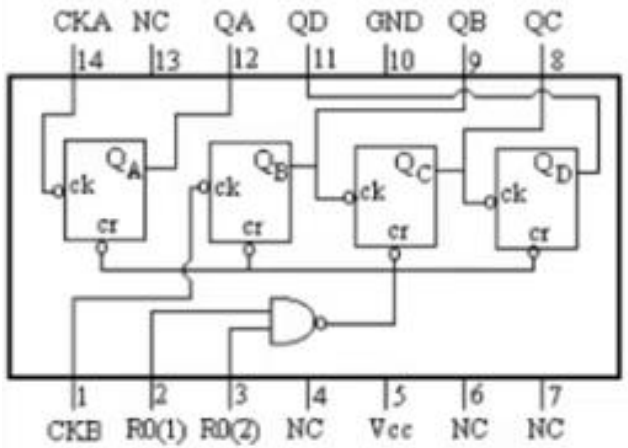
Traditionaly Custom Digital system design has been carried out using off-the-shellf general purpose digital ICs

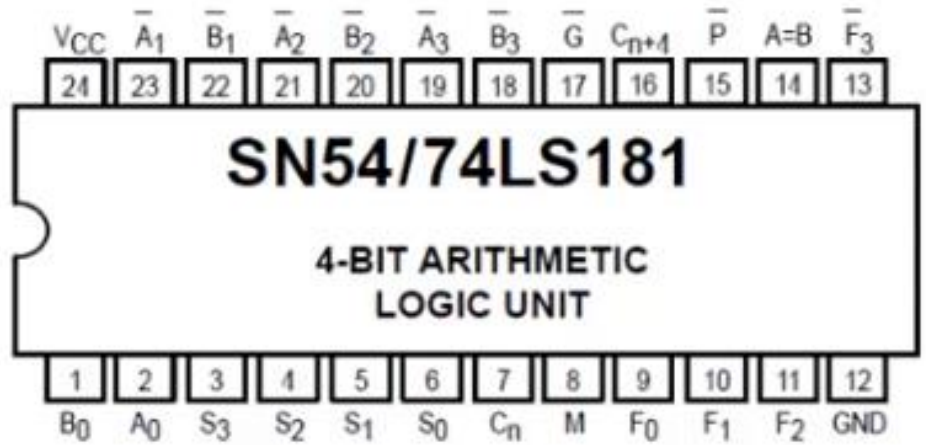


74LS83 - 74LS83 4-bit Binary Full Adder

Features

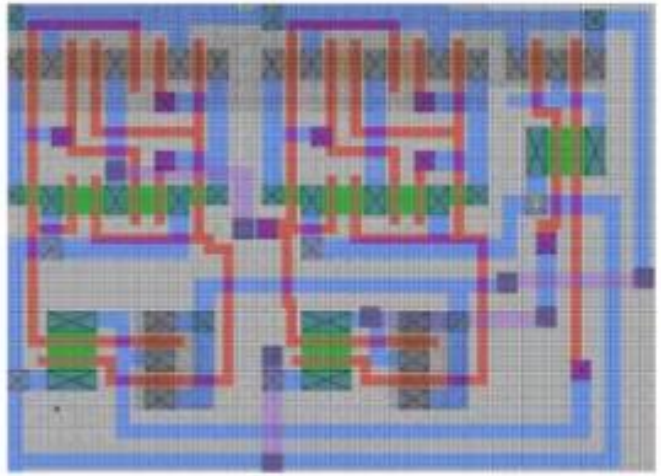
- Designed to add Two 4-bit Binary Numbers
- Full Carry Look Ahead across the Four bits
- Fast Add Times
- Operating Temperature up to 70oC
- Standard TTL Switching Voltages





7493: 4 bit binary counter

IC manufacturer



Can offer complex Ics but only if volume is high

System designer

Would like to offer a solution that uses as few Ics but due to custom design volume is low.

Solution : Programmable ICs

Microprocessors, microcontrollers, DSP processors etc

FPGA : field programmable gate arrays

Combinational Circuits

Combinational Circuit Design

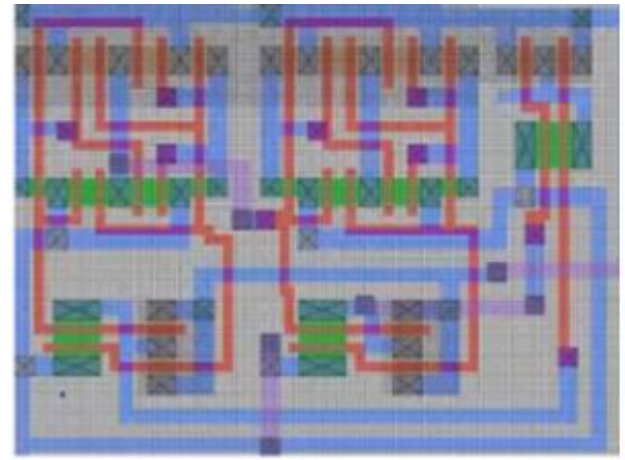
Function : $\overline{Y} = \overline{a}\,\overline{b}\,\overline{c} + \overline{a}\,b\,\overline{c} + a\,\overline{b}\,c$

a, b, and c are inputs and
y is the output.

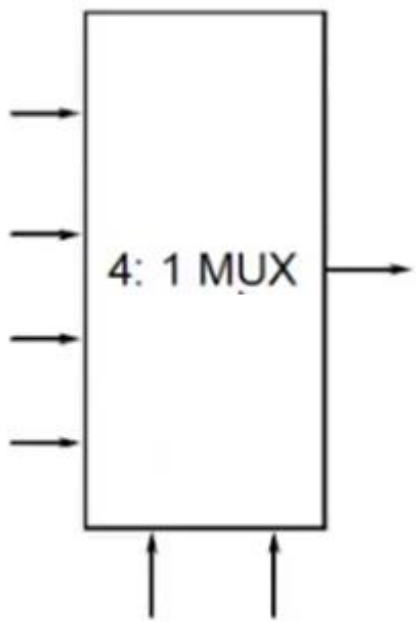
Performance: $\text{delay} \le \tau_d$

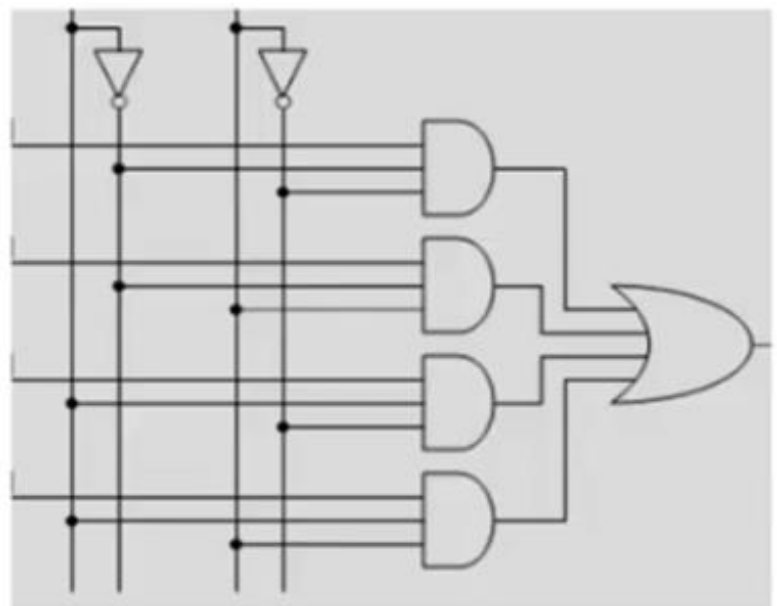
Area minimum $C_{Die} \sim \dfrac{C_{wafer}/\gamma_w}{\left(0.85 A_{wafer}/A_{IC}\right) \times \gamma_d}$

$$\overline{Y} = \overline{a}\,\overline{b}\,\overline{c} + \overline{a}\,b\,\overline{c} + a\,\overline{b}\,c$$



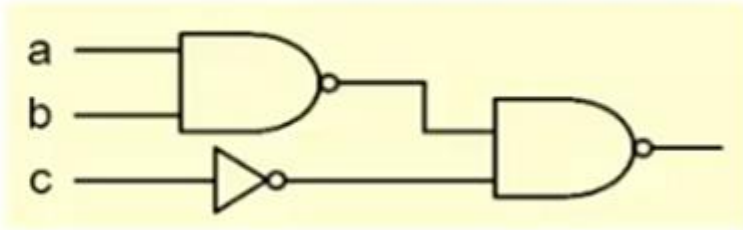
Decision: Full custom design or semicustom design

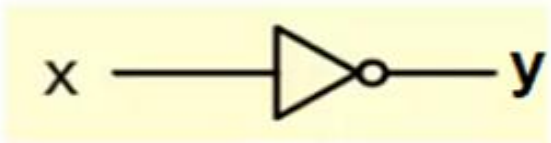




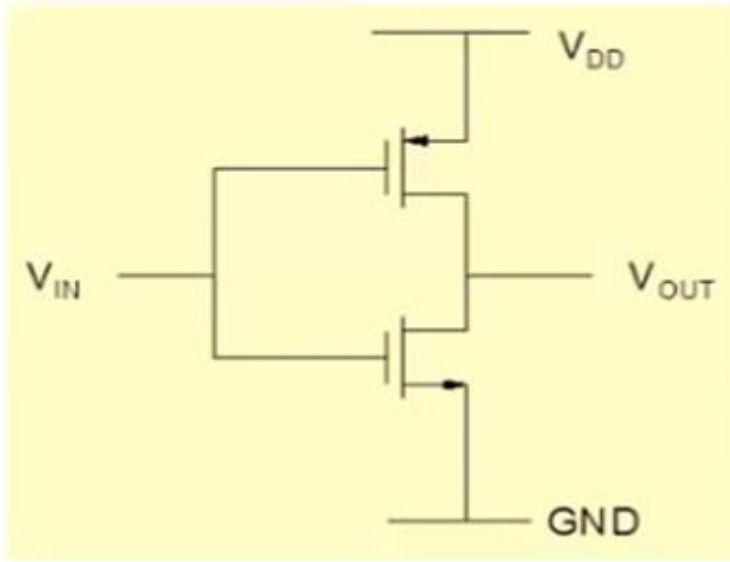
Design consists of several synthesis steps, each of which involves transformation of **behavioral** representation (functionality, performance) into a **structural** representation.

$$\overline{Y} = \overline{a}\,\overline{b}\,\overline{c} + \overline{a}\,b\,\overline{c} + a\,\overline{b}\,c$$



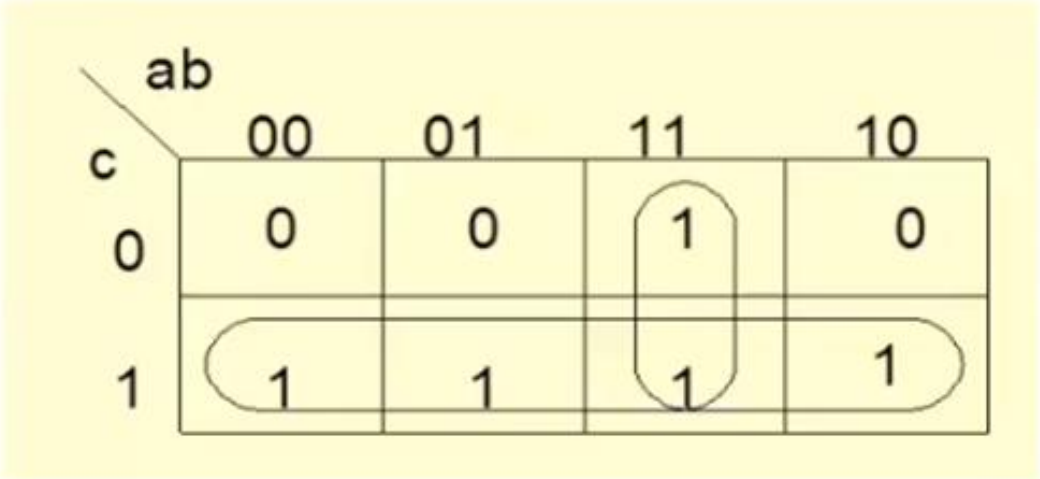


$$y = \overline{x}$$



Step-1: Logic Synthesis

1. Minimization
2. Technology mapping



$$x + \bar{x} = 1$$

$$Y = ab + c$$

-Algorithm is required whose complexity keeps pace with increasing circuit complexity.

-Manual minimization is tedious, sub-optimal and also error prone for complex designs.

A CAD tool is required

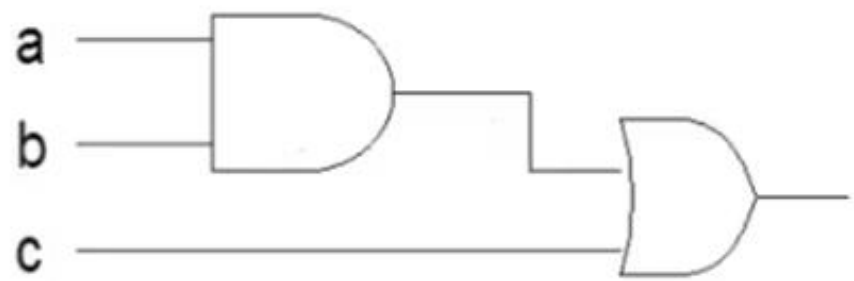
Logic Synthesis

-Minimization
-Technology mapping

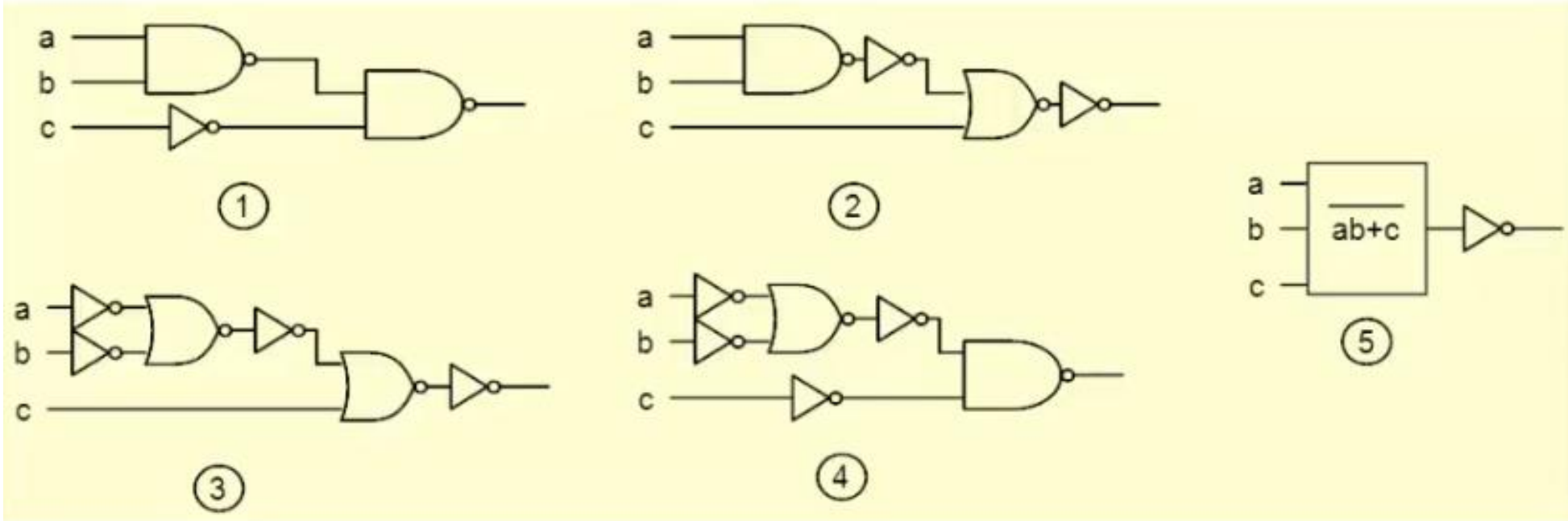
-map the minimized expression onto a network of gates available in the chosen technology.

$$Y = ab + c$$

$\Rightarrow$
?

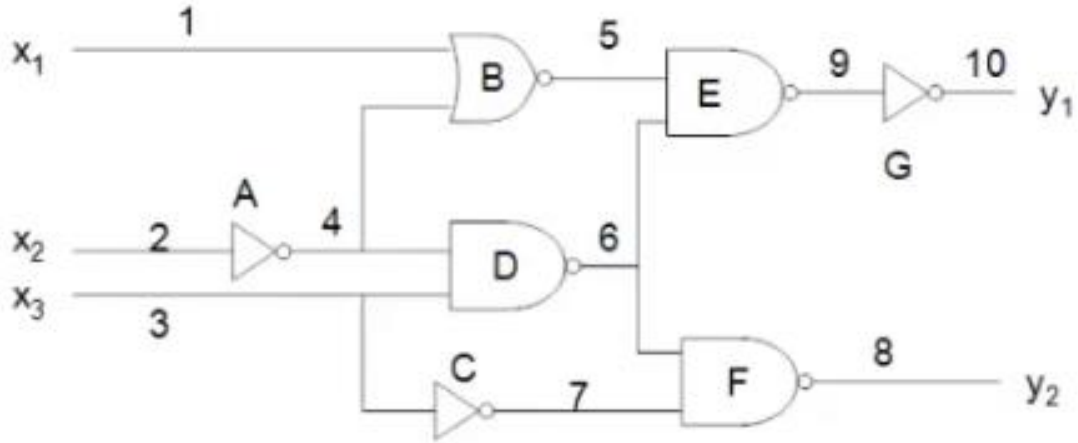


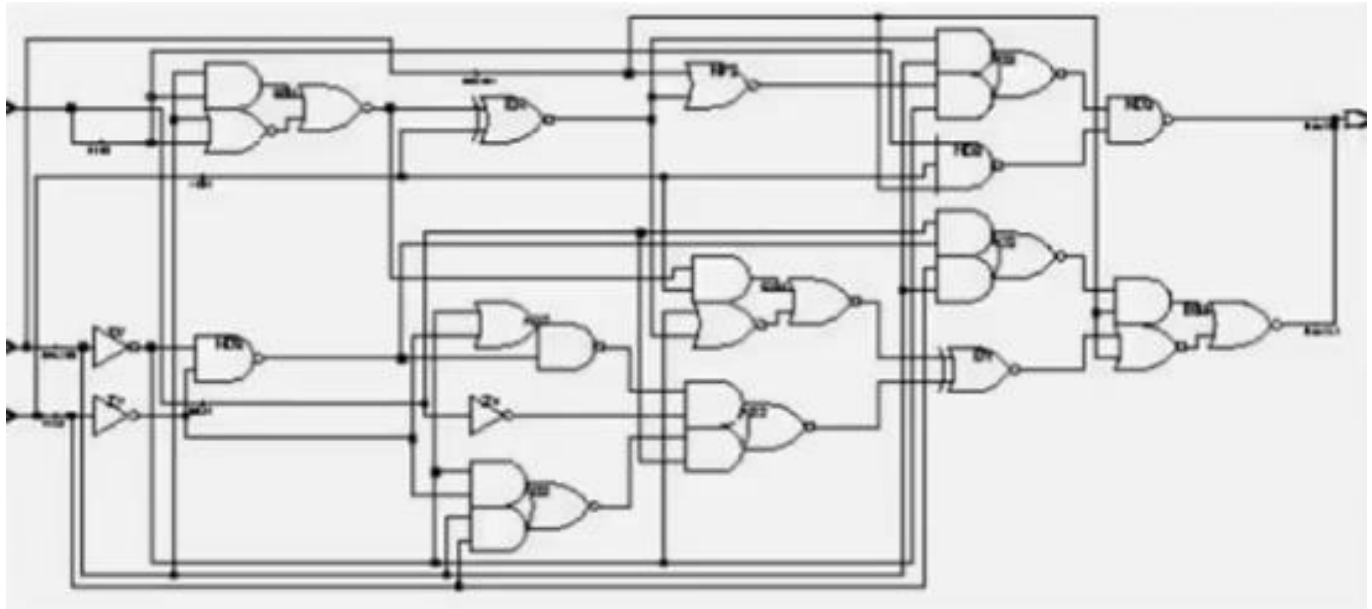
CMOS : elementary gates are NAND, NOR, NOT etc



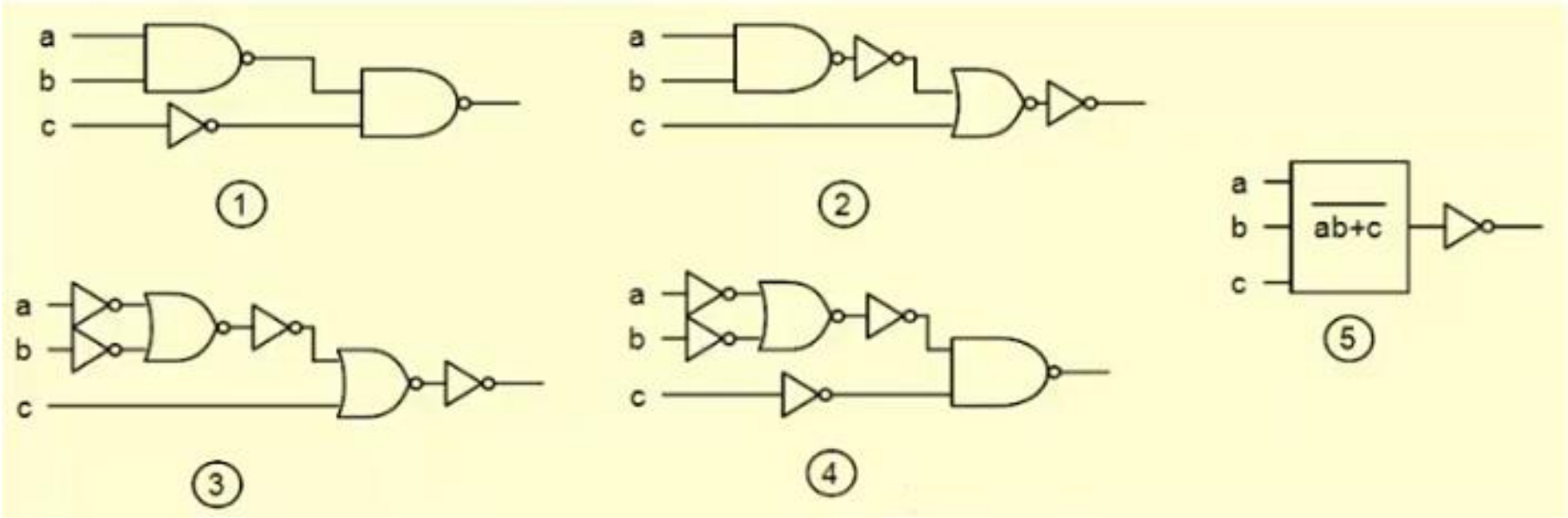
-All the above designs have the same functionality but they would differ in terms of area and delay

-It may be difficult to estimate these values at this stage





A CAD tool called static timing analysis tool is required to check if delay constraints are satisfied



-All the above designs have the same functionality but they would differ in terms of area and delay

-It may be difficult to estimate these values at this stage

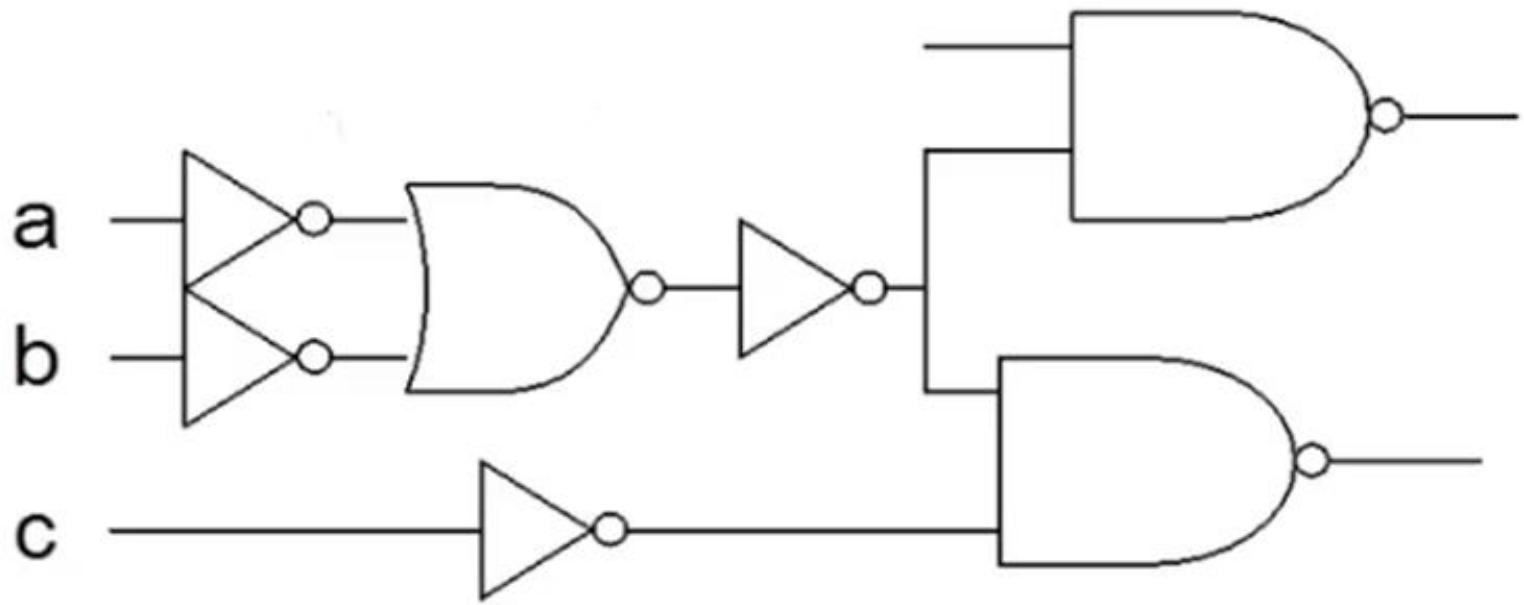
Two ways:

-take each one of the possible solutions and complete its design to the last detail.

-choose one possibility based on some estimate of performance and area and then carry out its detailed design.

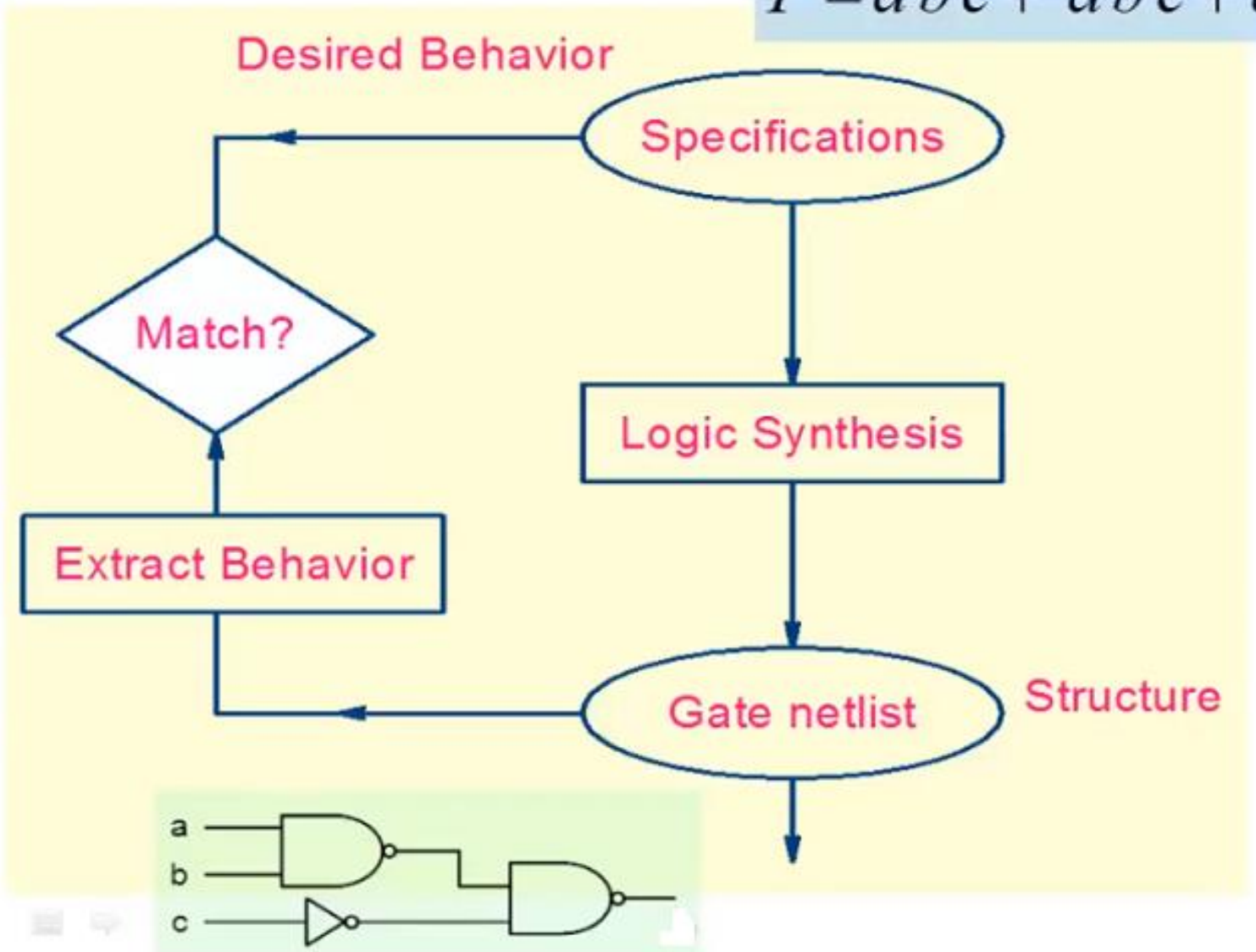
Logic Verification: Horizontal & Vertical

Horizontal : Check compliance with certain rules
Fan-in, Fan-out, floating inputs etc.

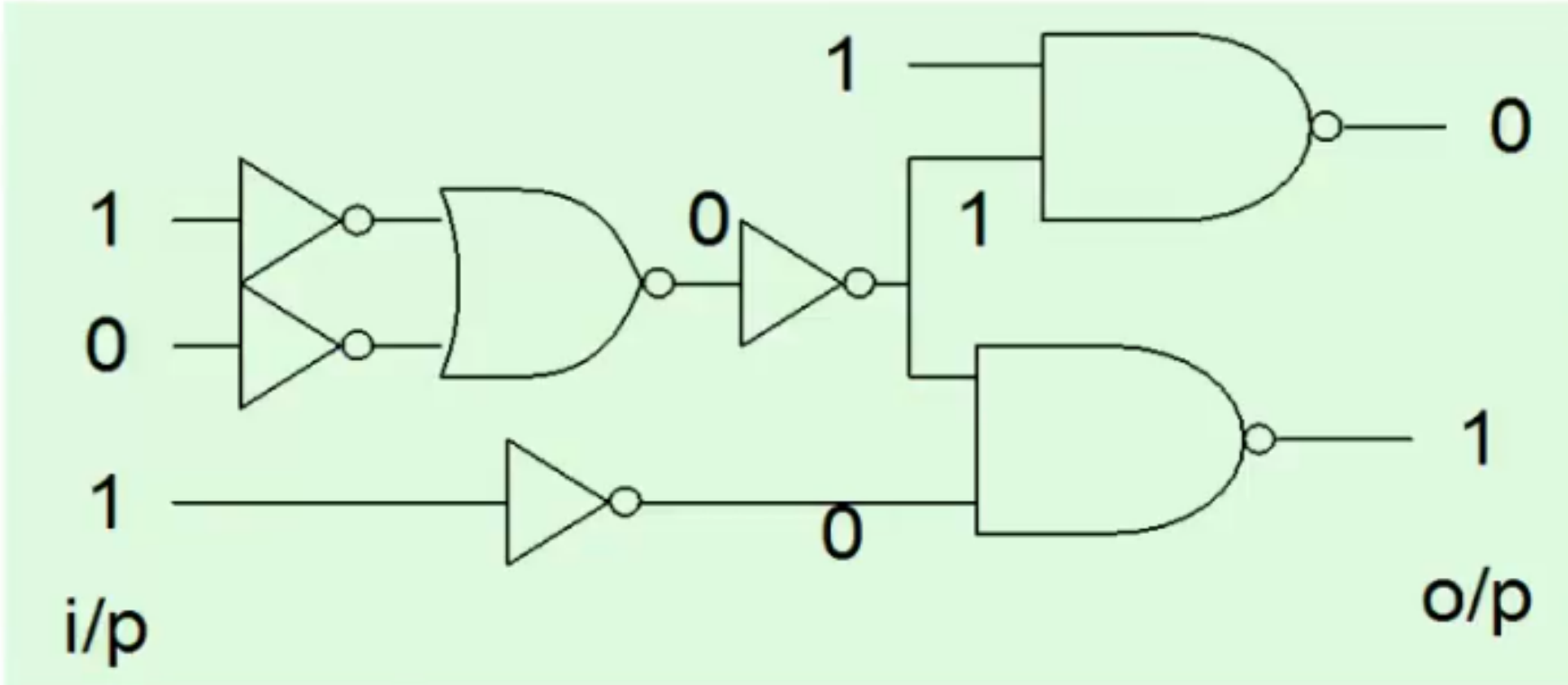


Logic Verification: Vertical

$$\bar{Y} = \bar{a}\bar{b}\bar{c} + \bar{a}b\bar{c} + a\bar{b}c$$

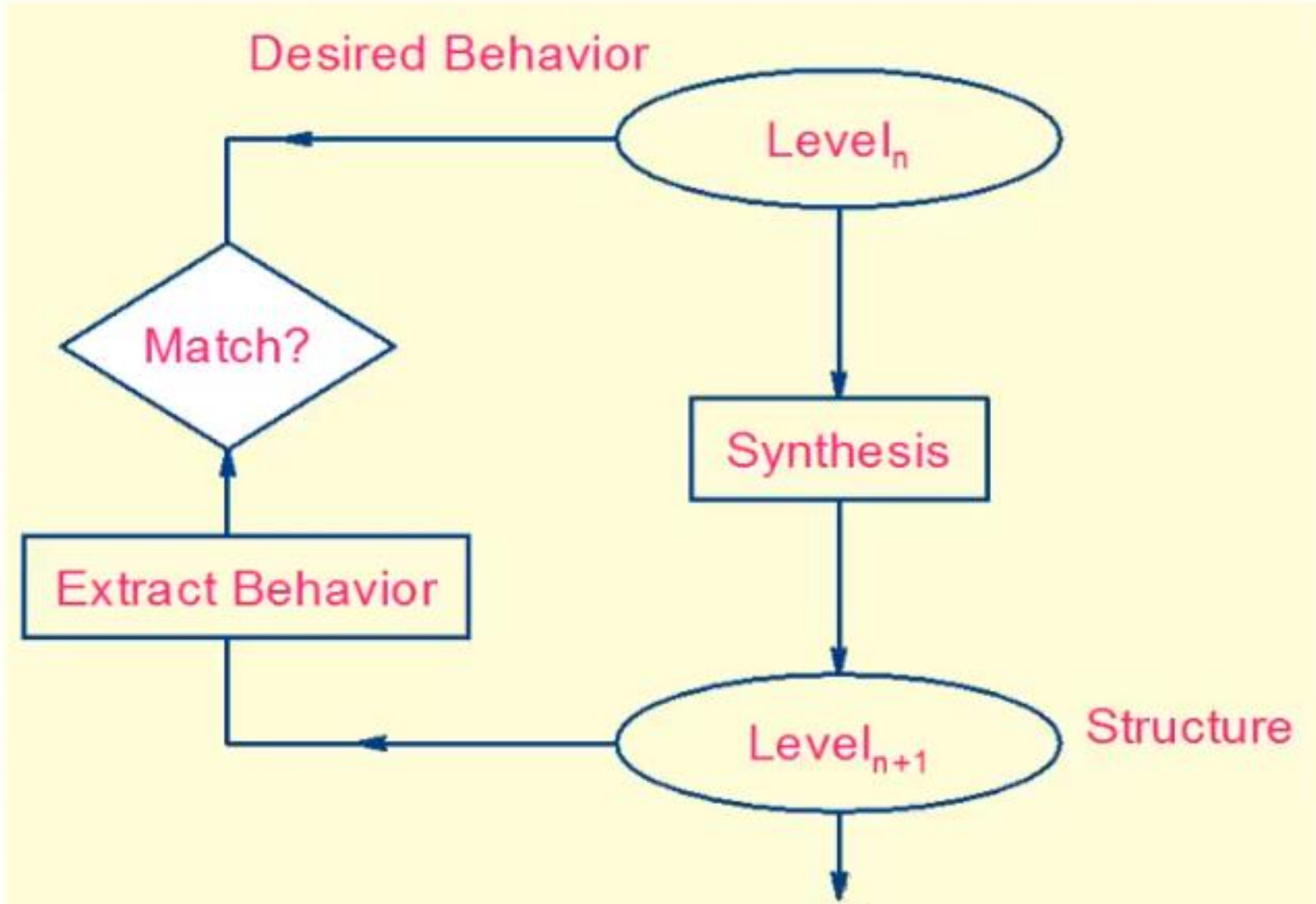


Logic Simulation

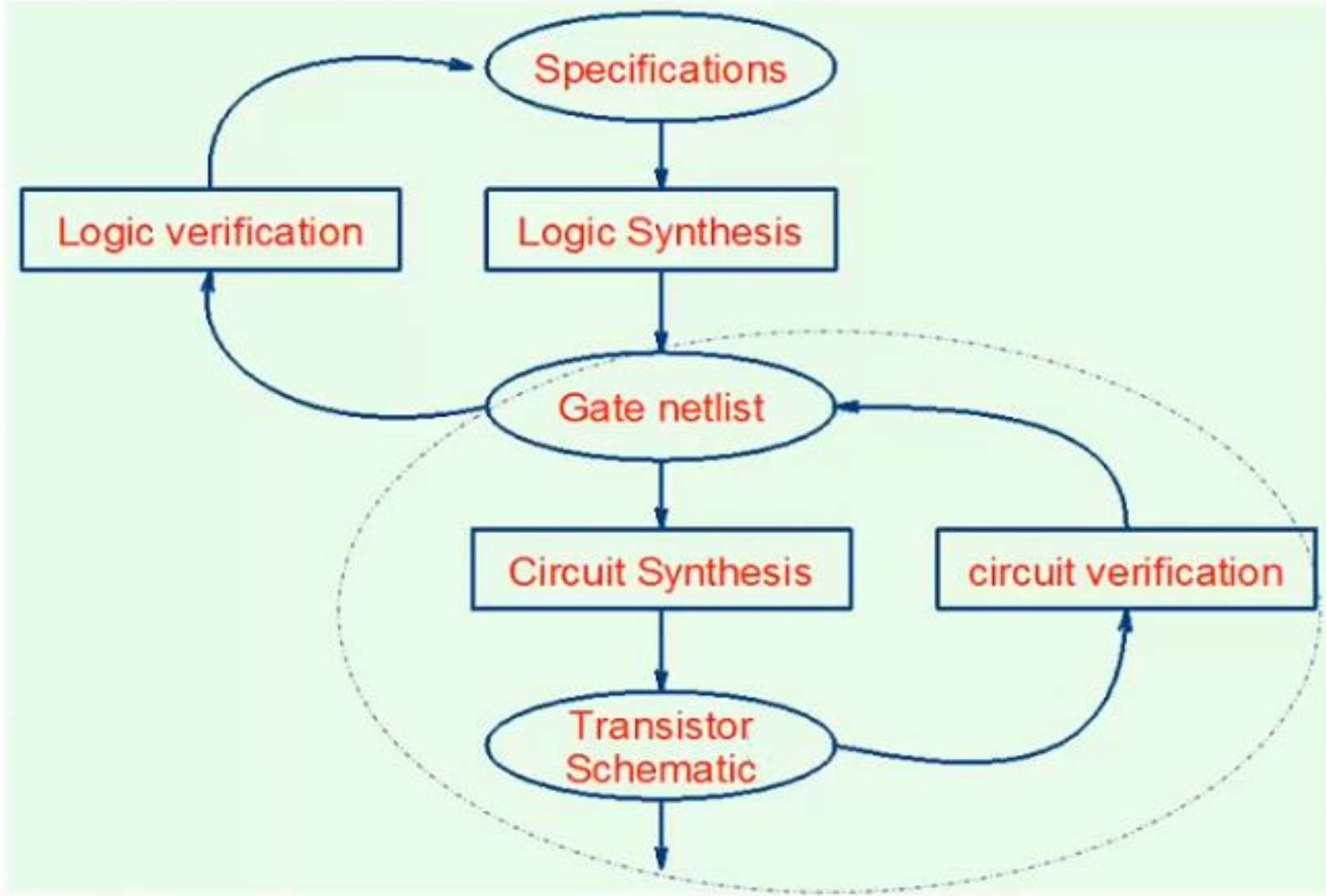


A CAD tool is required

Verification: Generic structure

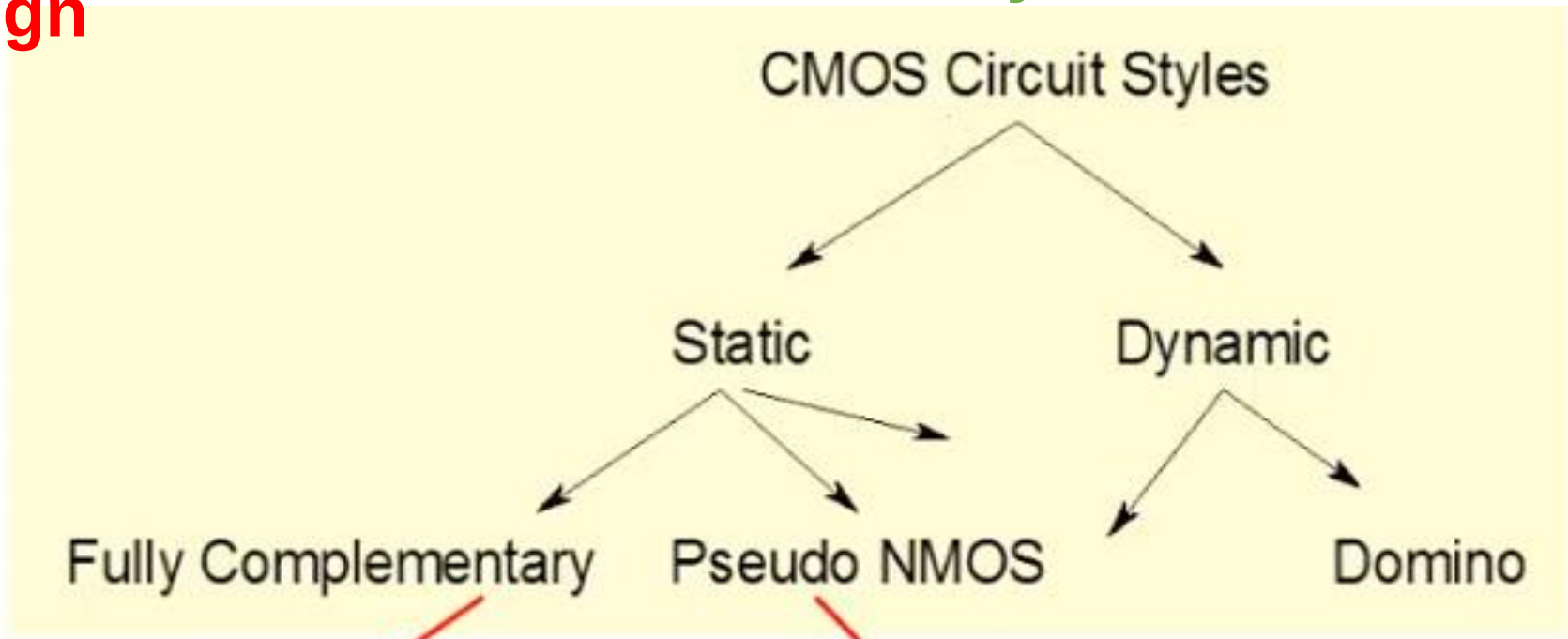


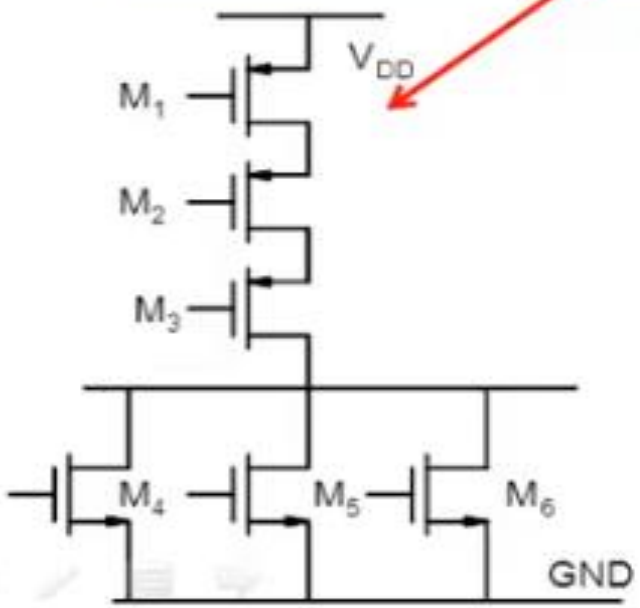
Next Phase : Circuit Design

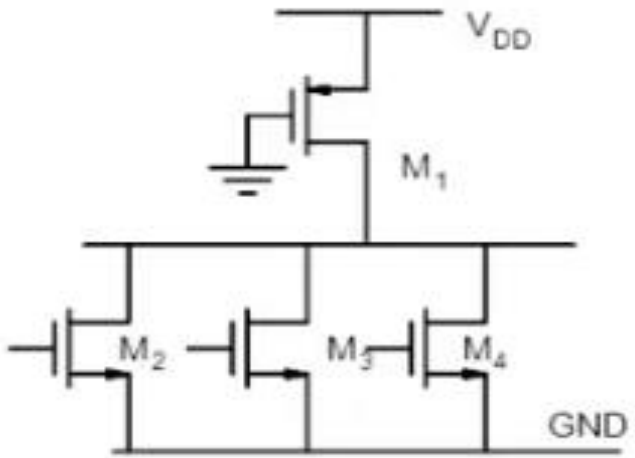


Circuit Design

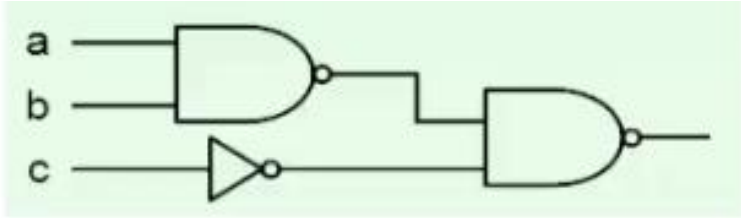
Choose a Circuit style

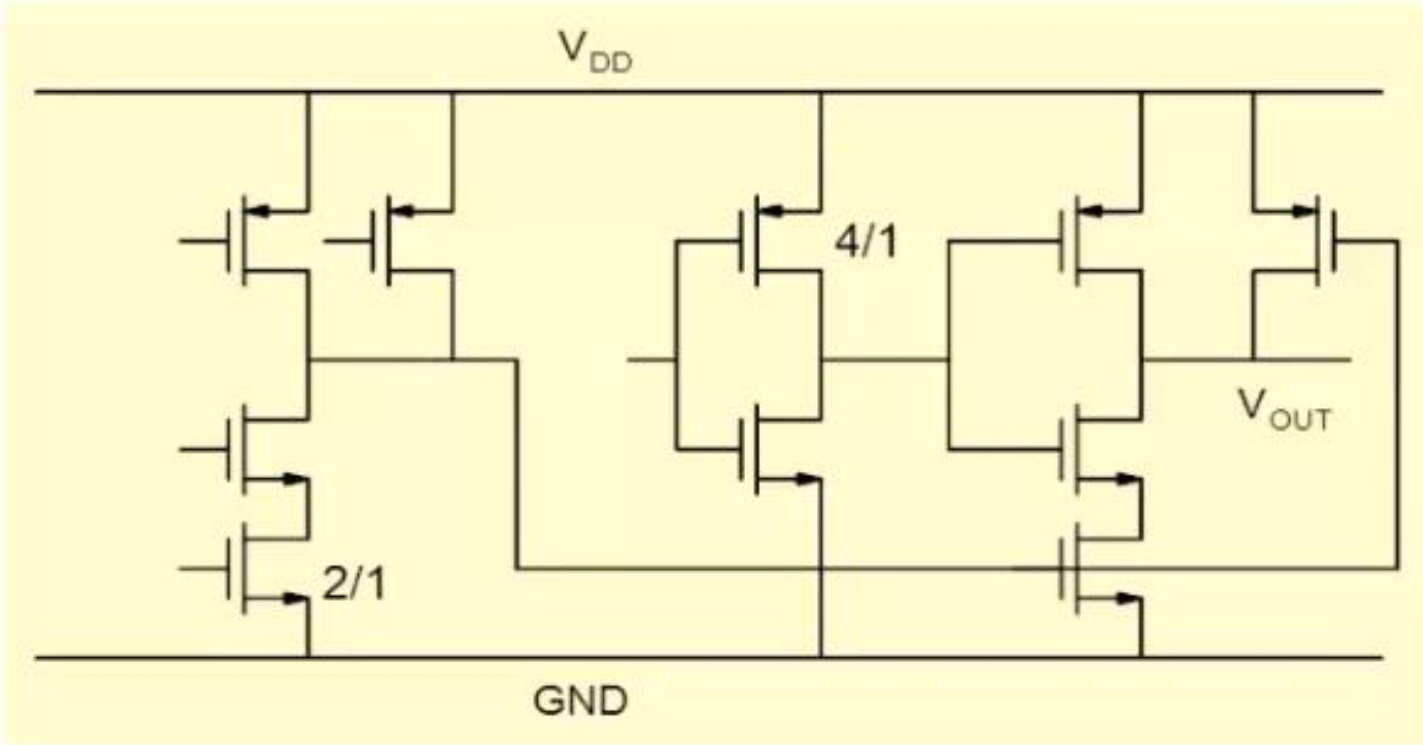






Circuit Design

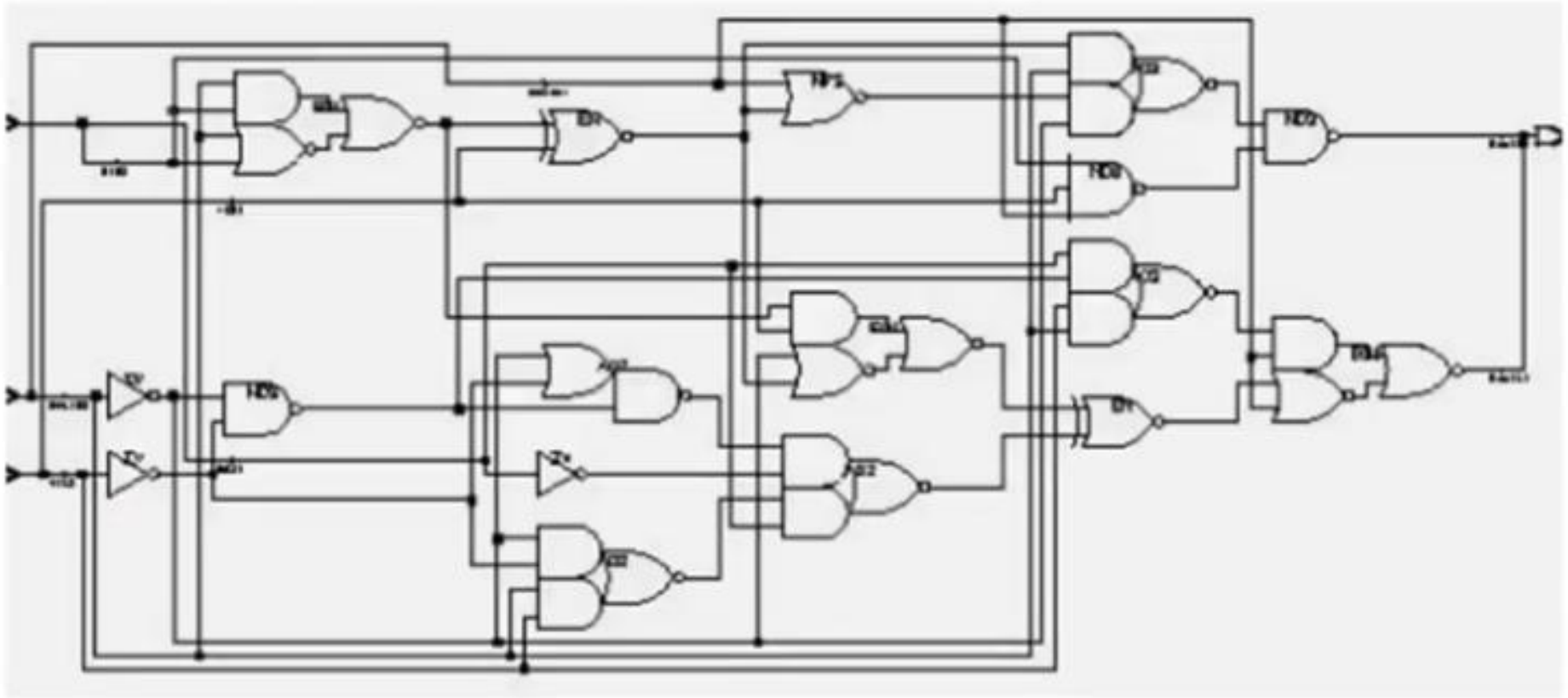




-Size Transistors to meet delay specs.and minimize area

Sizing has to be done under uncertainty

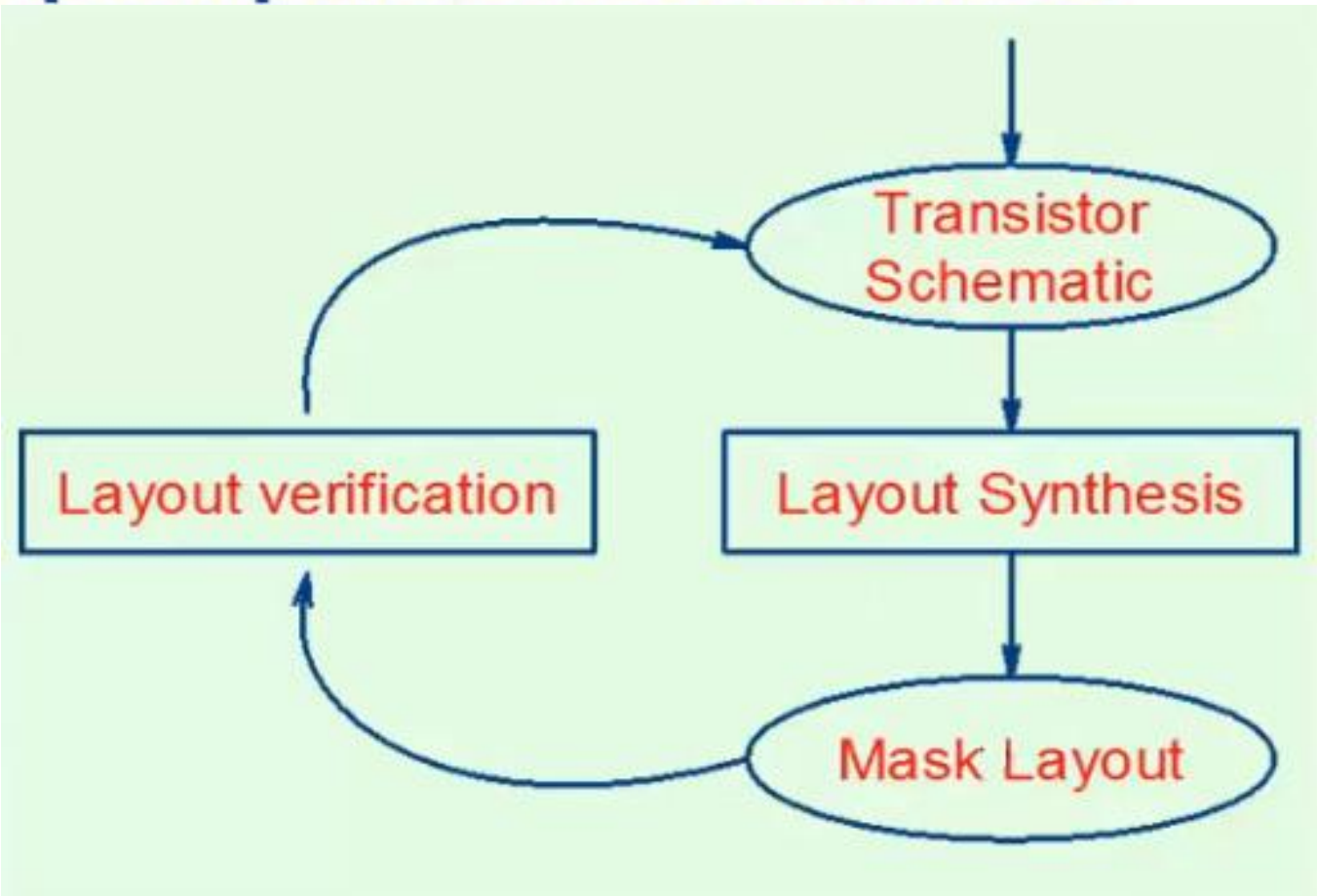
A CAD tool: circuit simulator is required to verify performance and functionality



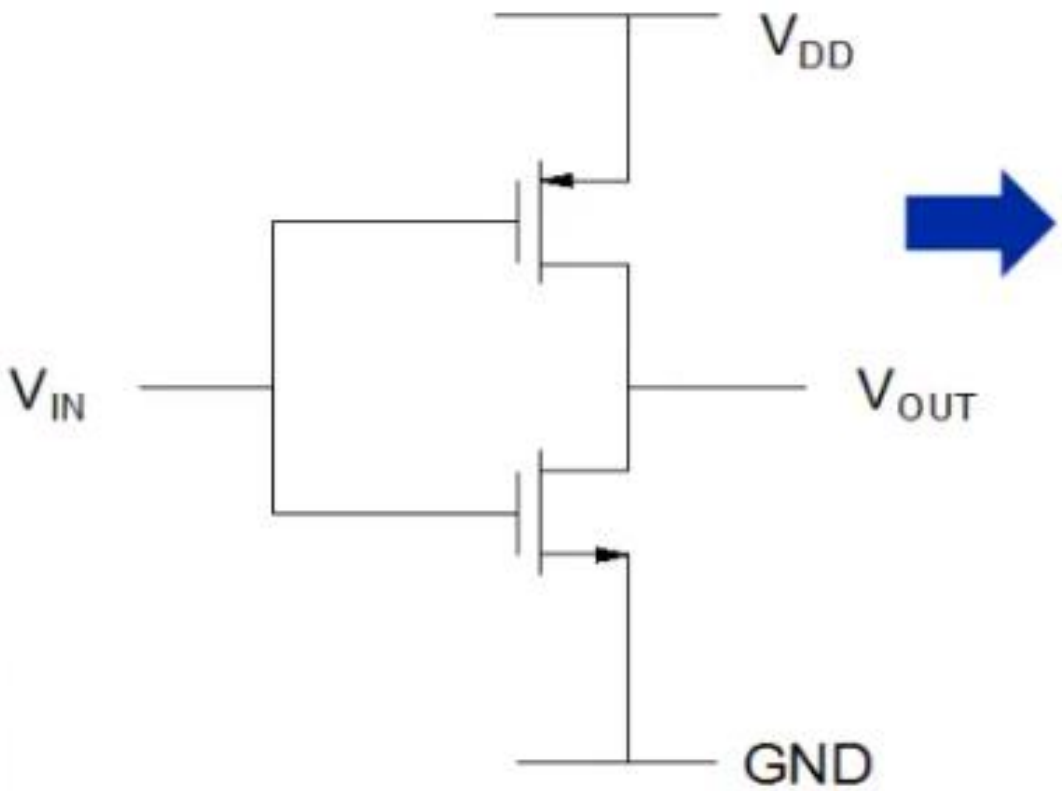
Circuit dependent custom sizing of transistors becomes impossible with increased complexity

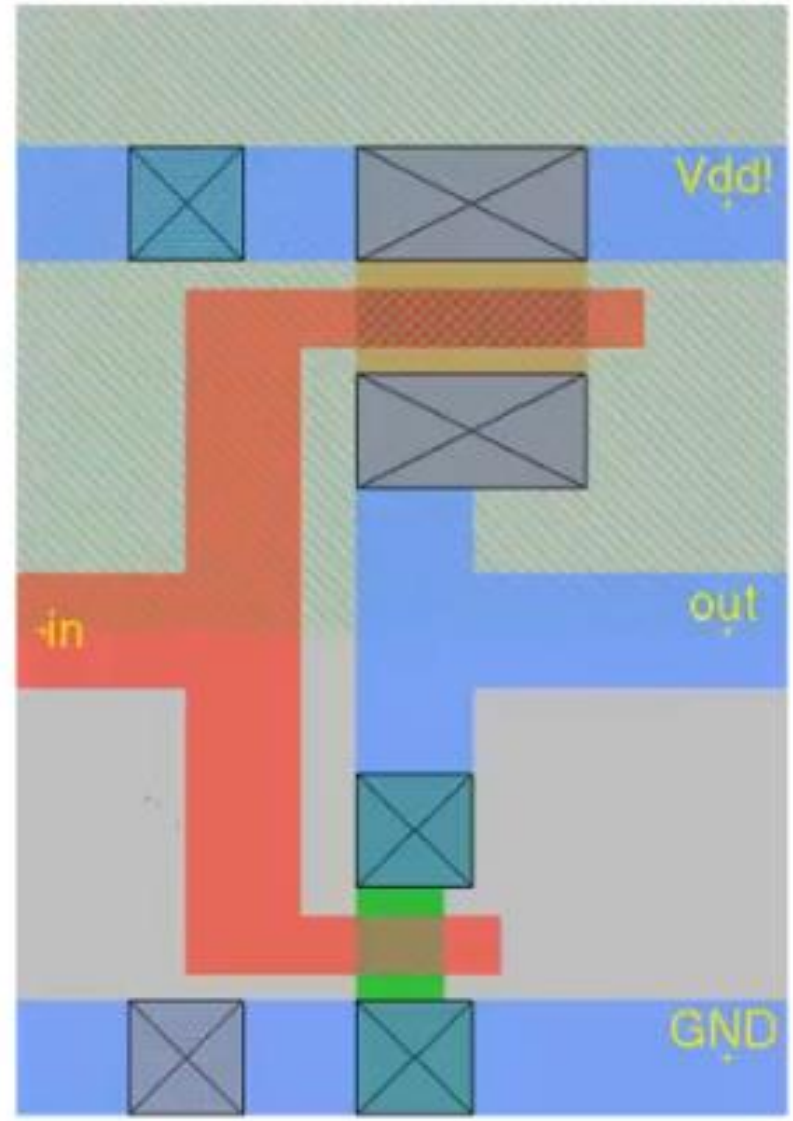
Next Phase : Physical or Layout Design

A design is complete only when we have a complete plan for its fabrication



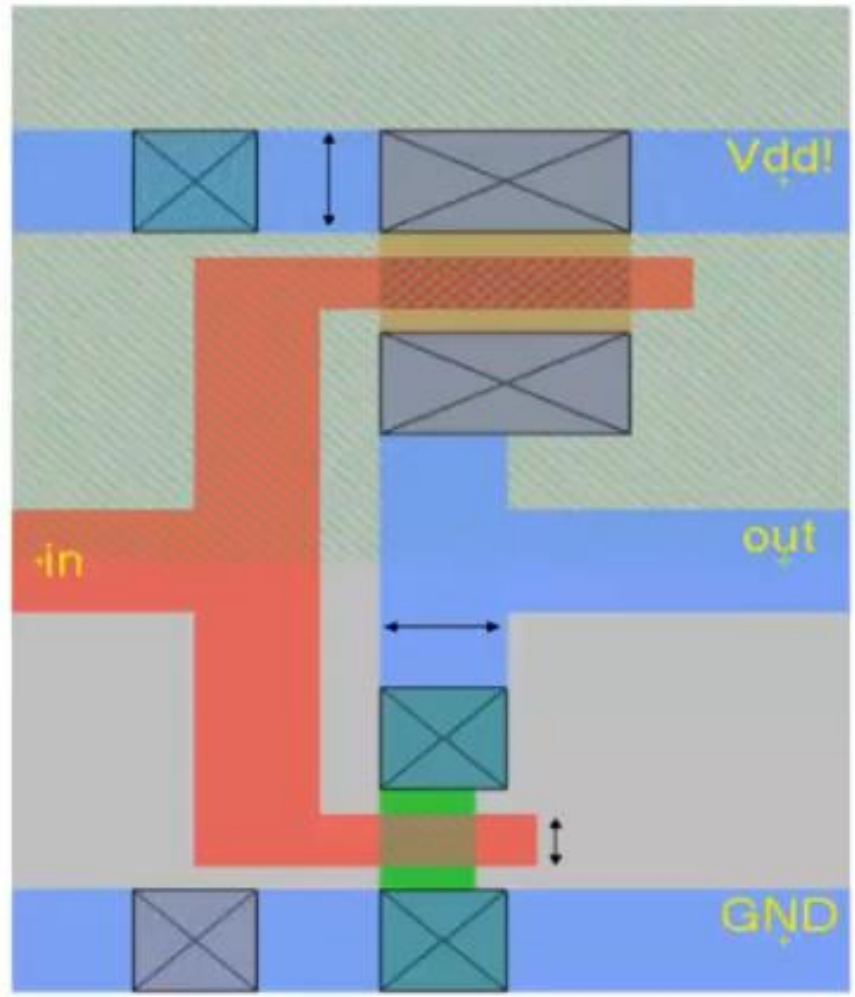
Layout Design





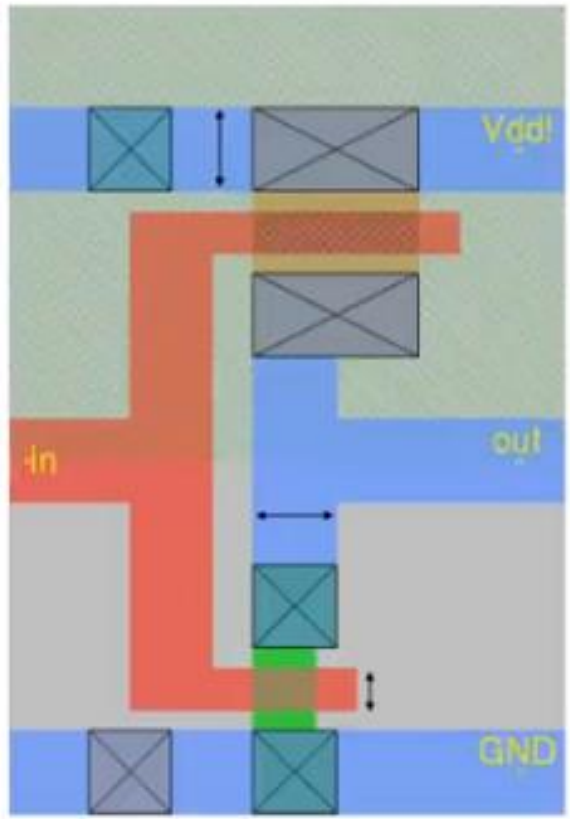
Verification

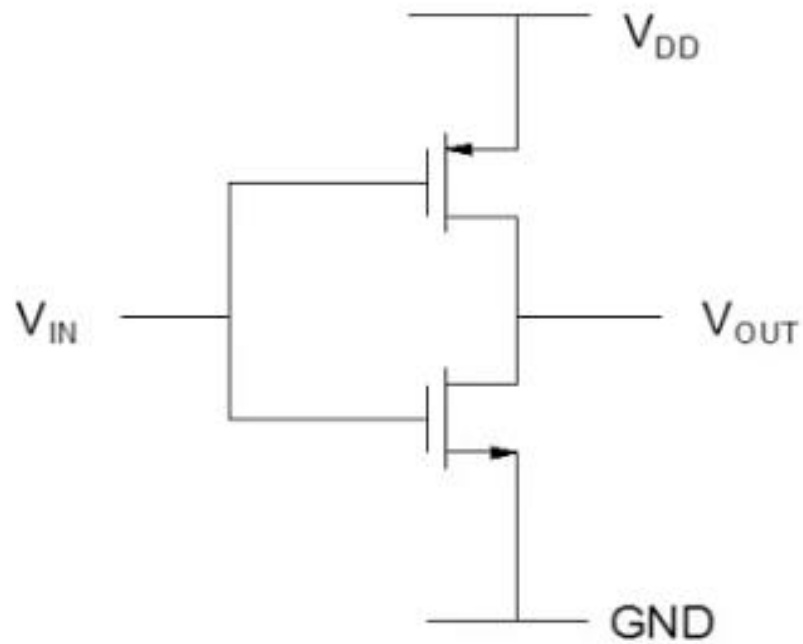
-Design Rule Check (DRC)



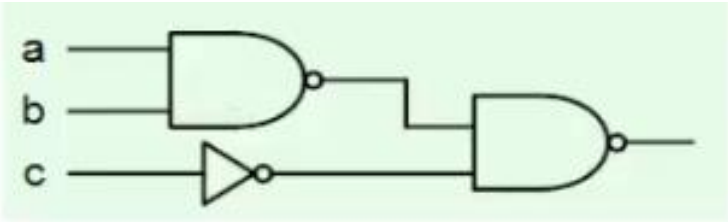
Verification

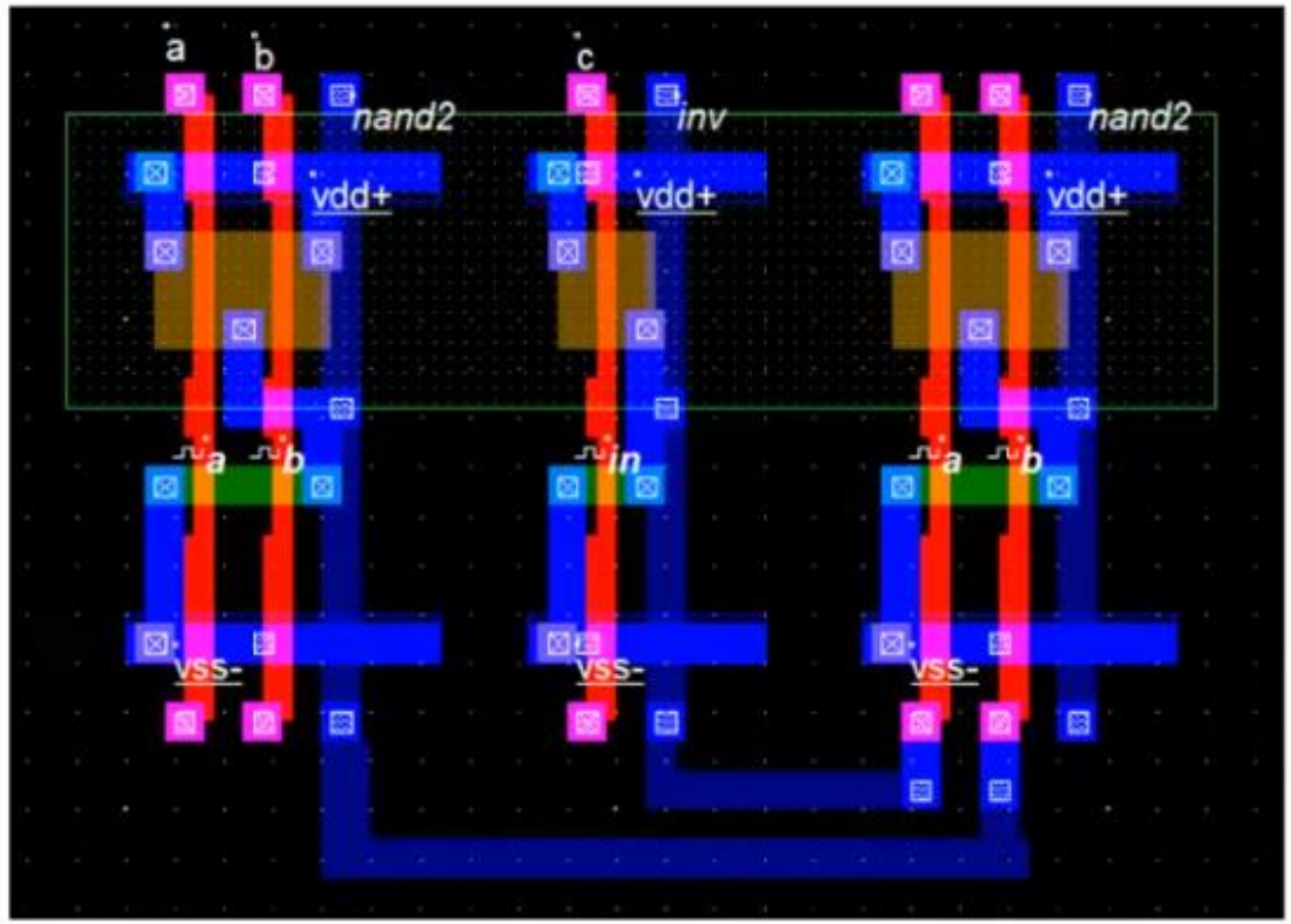
-Layout vs. Schematic check (LVS)



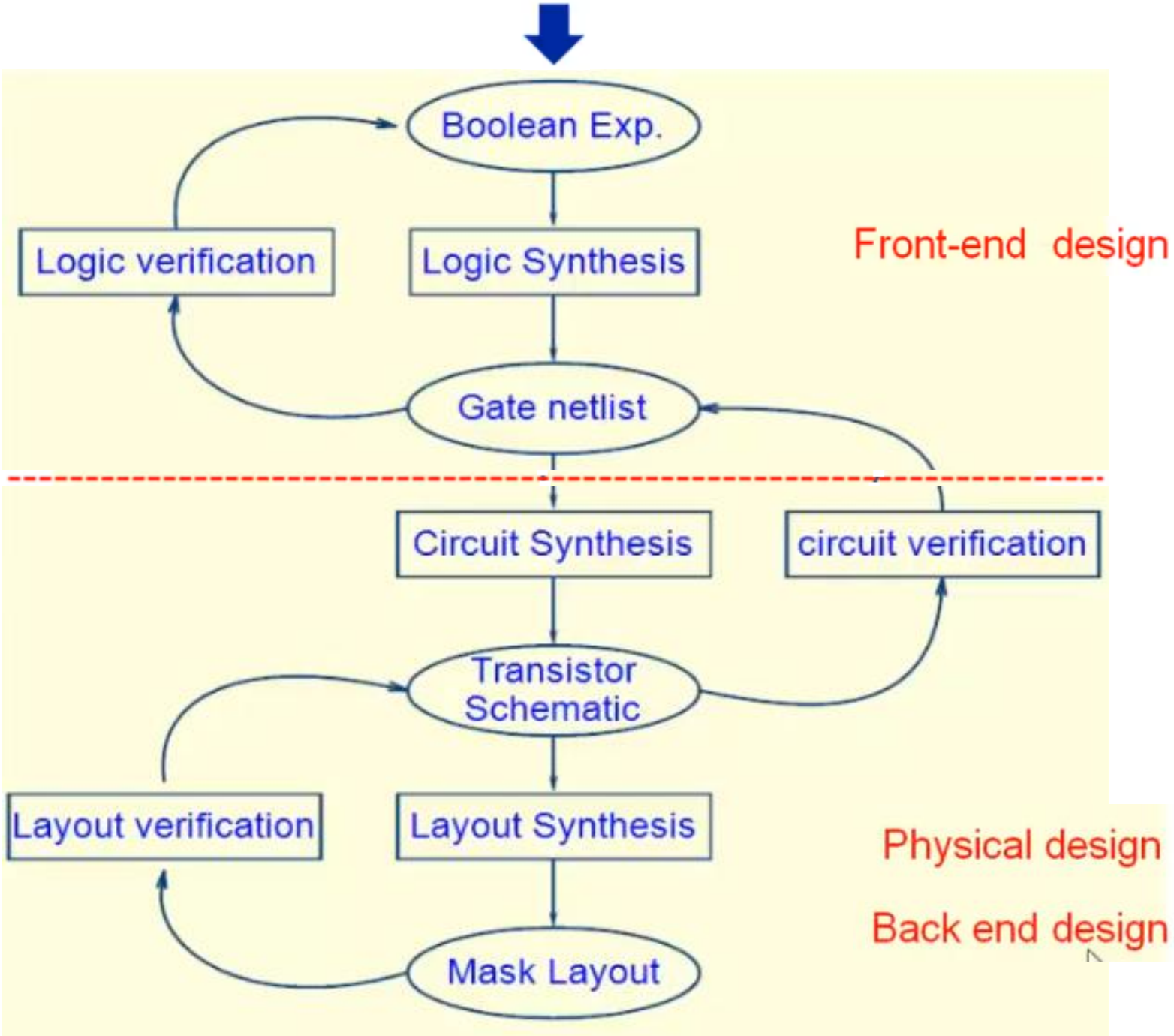


Circuit simulation on the extracted schematic gives
Correct prediction of performance





Placement and Routing


Boolean Exp.
Logic verification
Logic Synthesis
Front-end design
Gate netlist
Circuit Synthesis
circuit verification
Transistor Schematic
Layout verification
Layout Synthesis
Physical design
Back end design
Mask Layout