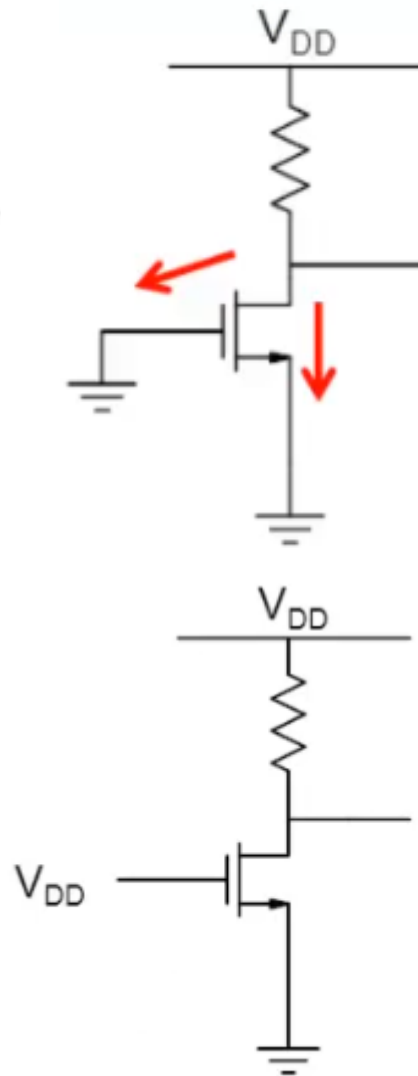
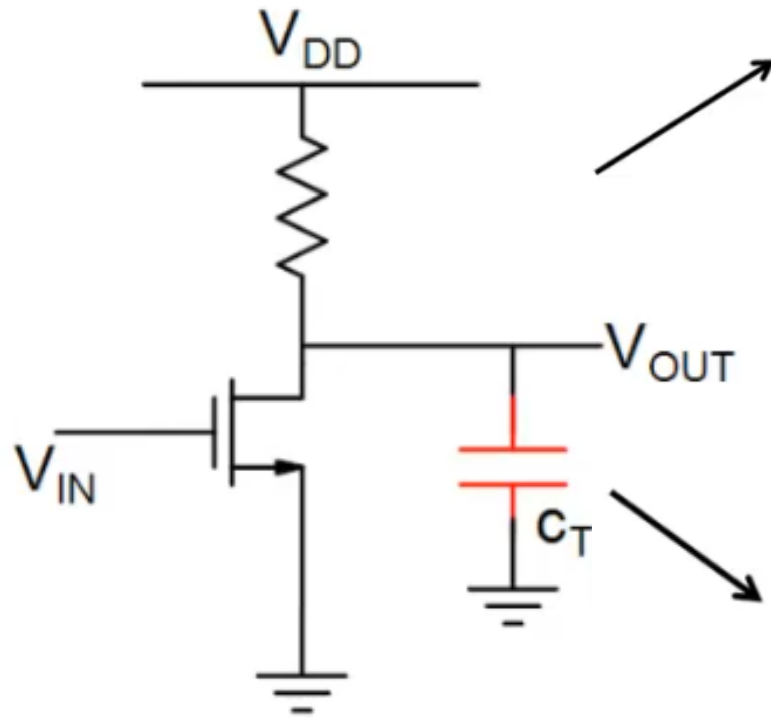
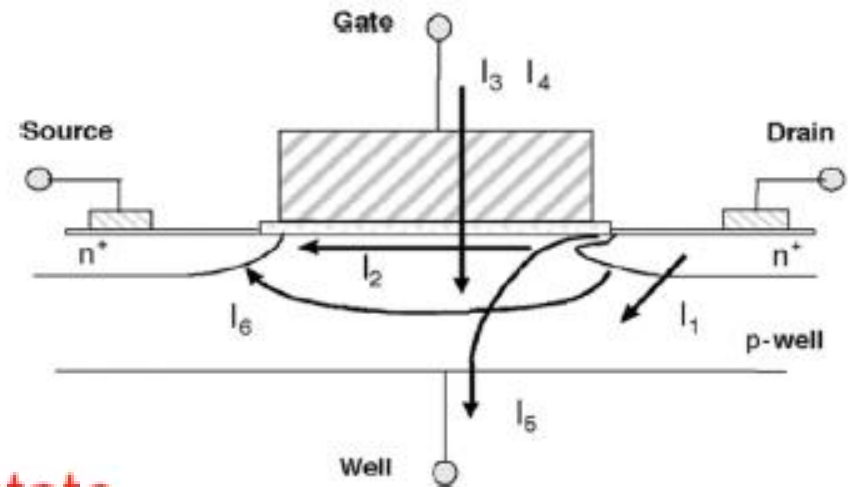
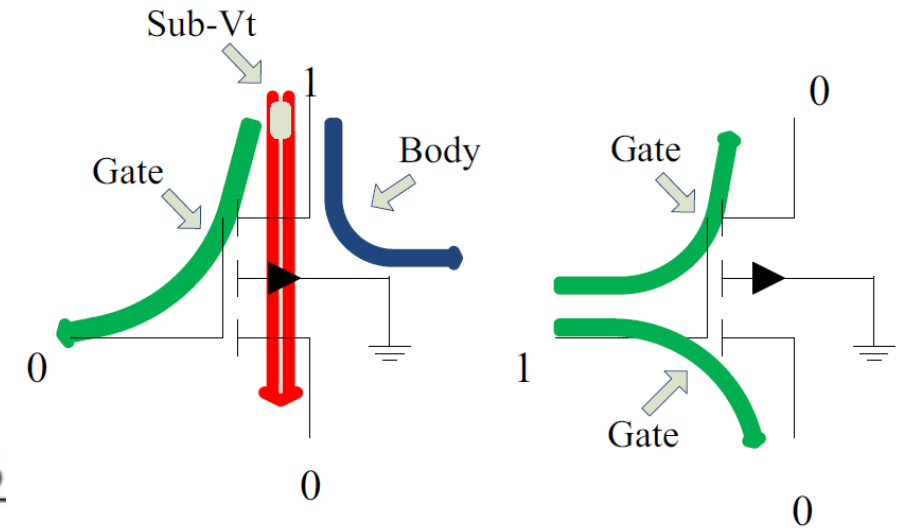


Power dissipation



$$P = V_{DD} \times I_{leakage}$$

$$P \sim \frac{V_{DD}^2}{R_D}$$



1. Static
2. Dynamic

Energy should be drawn only to change the state

- If channel is **locking**:

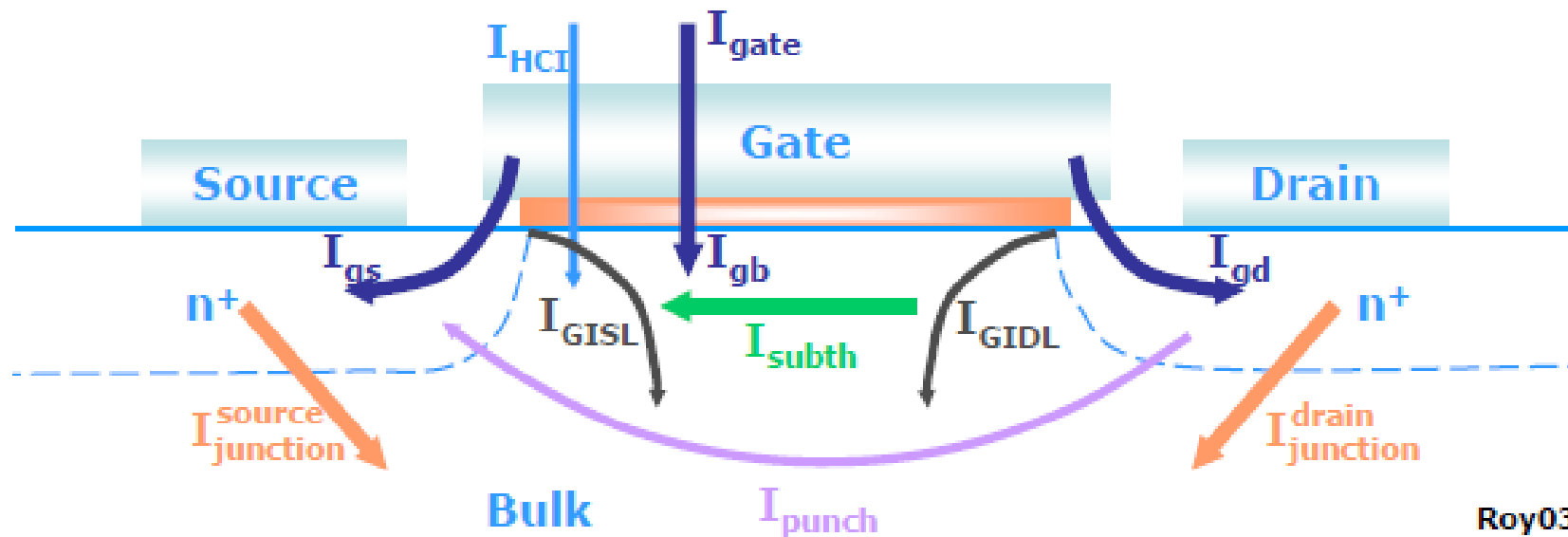
- subthreshold current (I_{subth})
- gate tunnelling to S/D (I_{gate})
- pn-junction leakage (I_{junction})
- gate induced drain leakage (I_{GIDL})
- depletion punchthrough (I_{punch})

- If channel is **conducting**:

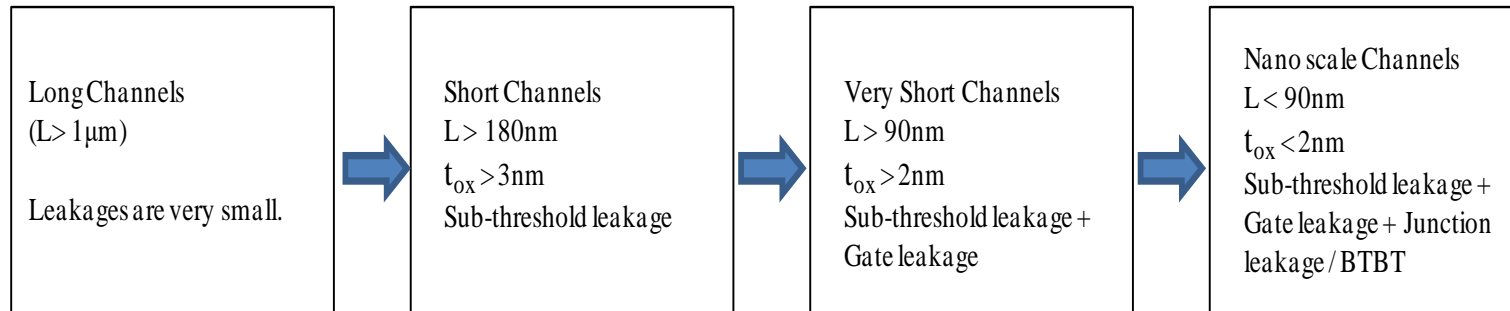
- gate tunnelling (I_{gate})
- pn-junction leakage (I_{junction})

- If channel is **switching**:

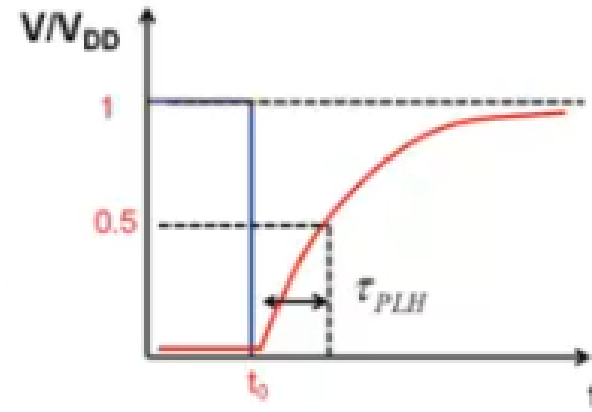
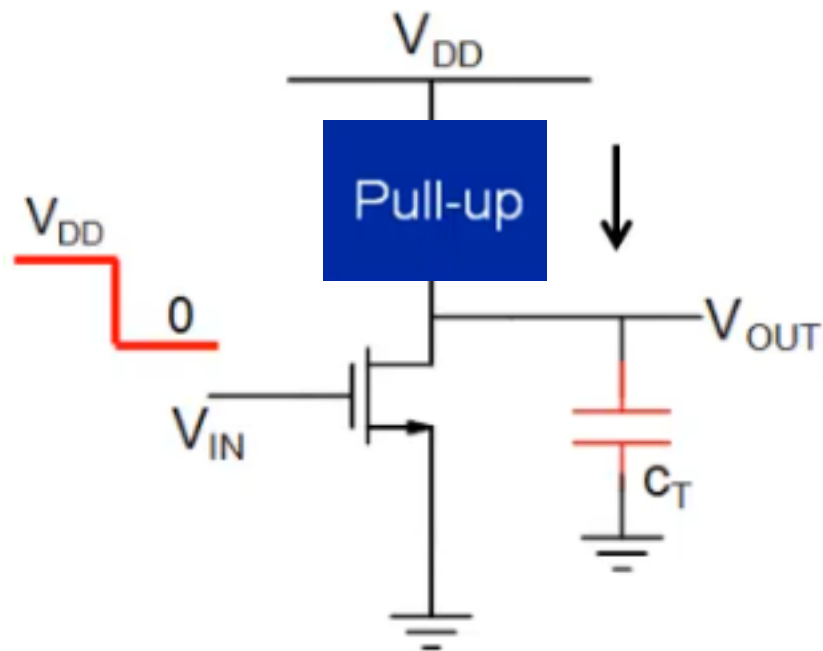
- hot carrier injection (I_{HCI})



Roy03



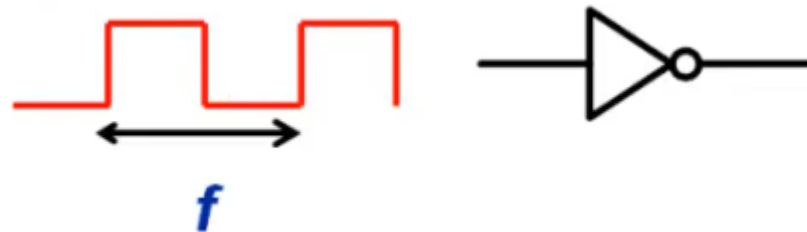
Contribution of new leakage currents with scaled technologies



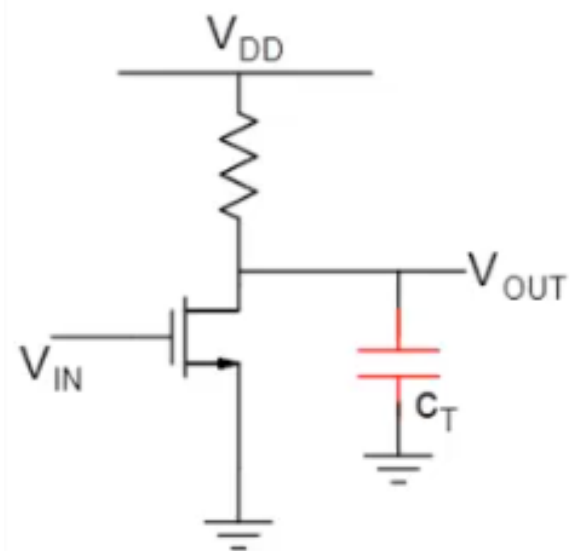
$$E_{supply} = \int V_{DD} \times I_{pu} dt = C_T \times V_{DD}^2$$

Half of it is dissipated in the resistor and the other half is stored in capacitor

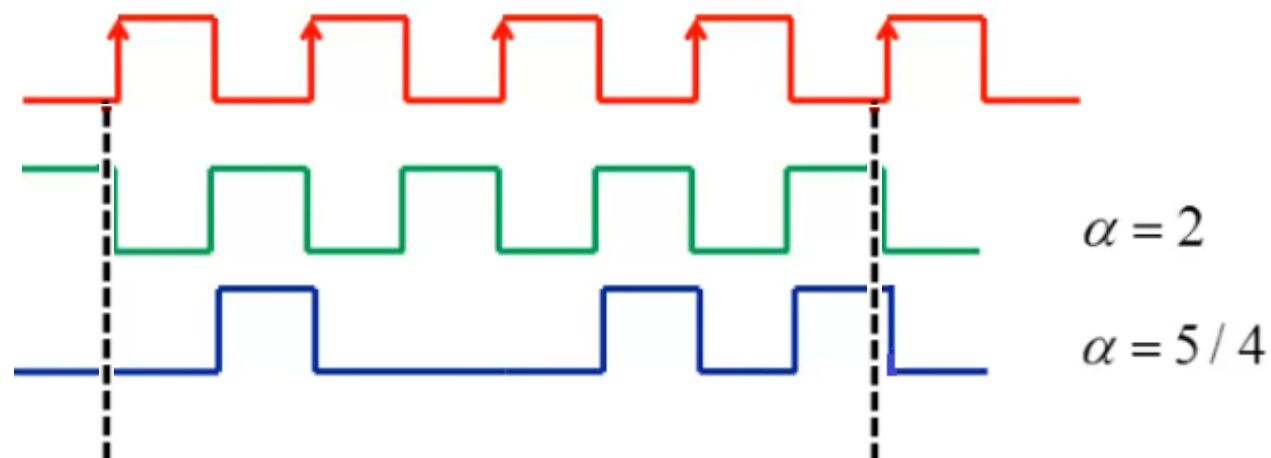
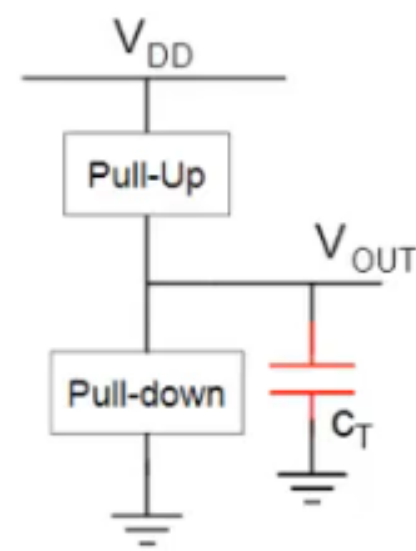
When the inverter switches back to zero, the energy stored on capacitor is also dissipated



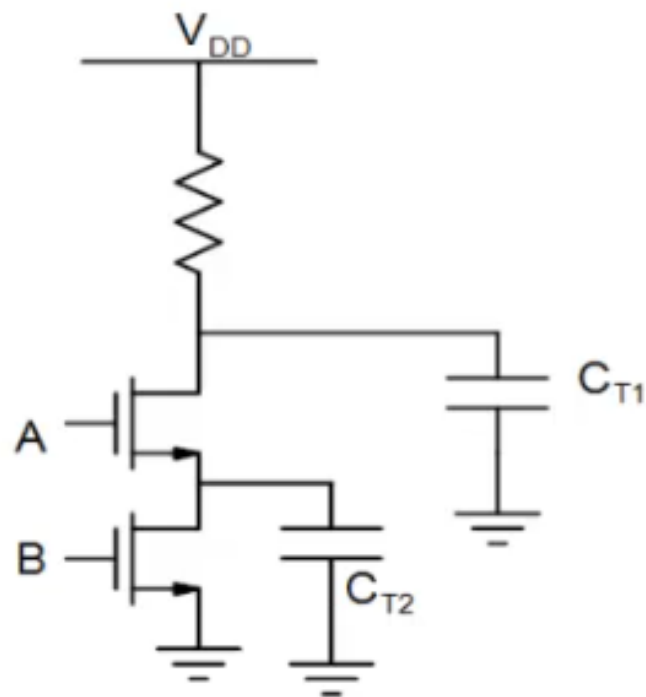
$$P_{dynamic} = \frac{0.5C_T \times V_{DD}^2 + 0.5C_T \times V_{DD}^2}{T} = C_T \times V_{DD}^2 \times f$$



$$P_{dynamic} = C_T \times V_{DD}^2 \times f$$



$$P_{dynamic} = \sum (0.5 C_j \times V_j^2) \times f \times \alpha_j$$



NAND gate

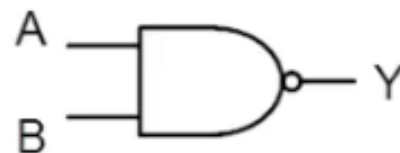
$$P_{dynamic} = (0.5C_{T1} \times V_{j1}^2) \times f \times \alpha_1 + (0.5C_{T2} \times V_{j2}^2) \times f \times \alpha_2$$

Suppose B= 1 and A switches with clock frequency

$$P_{dynamic} \cong (0.5C_{T1} \times V_{DD}^2) \times f \times 2$$

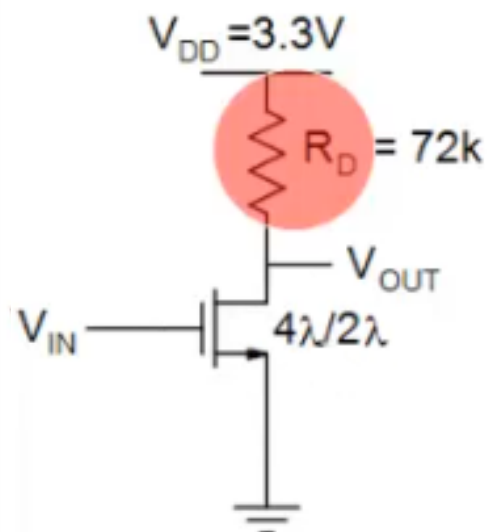
Suppose A= 1 and B switches with clock frequency

$$P_{dynamic} \cong (0.5C_{T1} \times V_{DD}^2) \times f \times 2 + (0.5C_{T2} \times V_{DD}^2) \times f \times 2$$

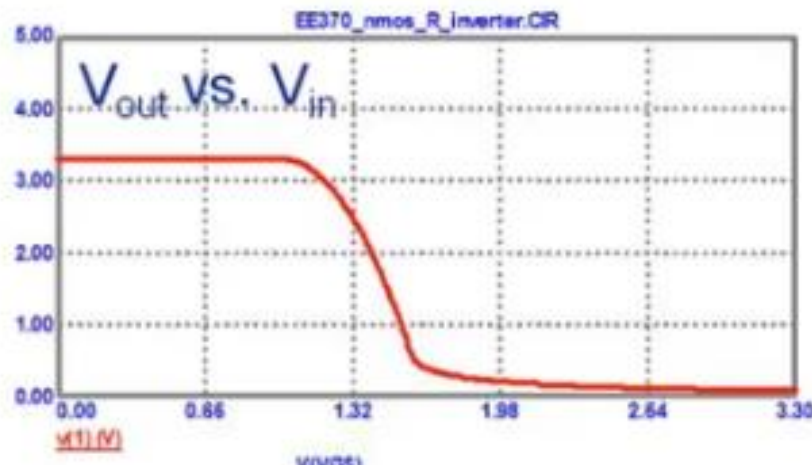


What about delays ?

Summary



1. Noise Margins
2. Area
3. Delay
4. Power

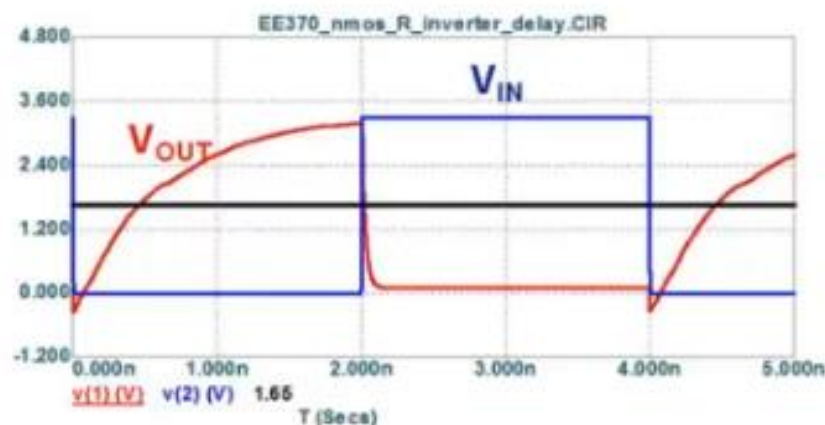
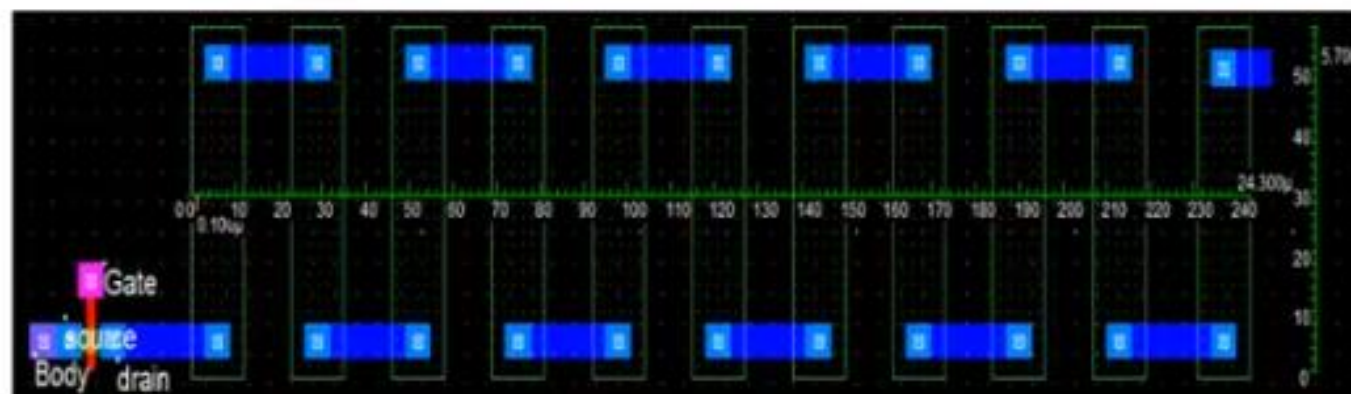


$$R_D = 72k \Rightarrow V_{OL} = 0.1V; V_{OH} = 3.3V$$

$$V_{IL} = 1.07V; V_{IH} = 1.7V$$

$$NM_L \sim 0.97V; NM_H \sim 1.6V$$

$$V_{inv} = 1.5V$$

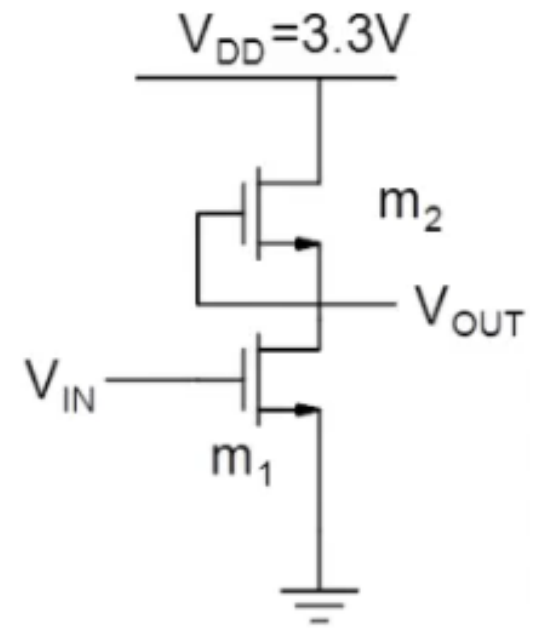
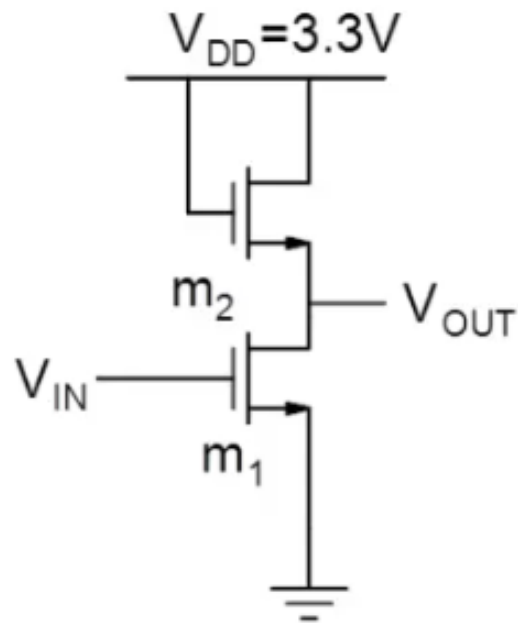
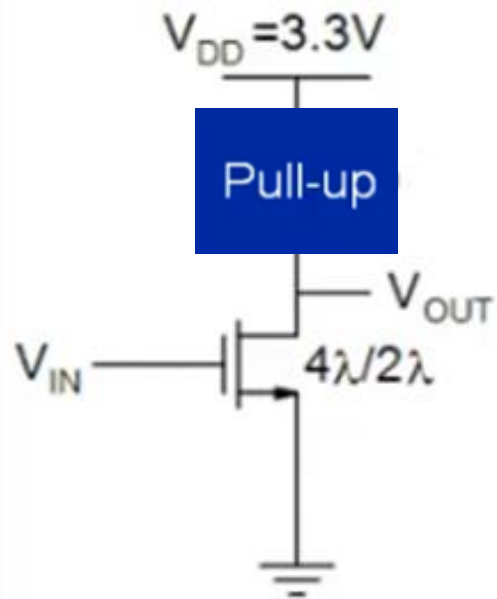


$$\tau_{PLH} \cong 424ps; \tau_{PHL} \sim 39ps$$

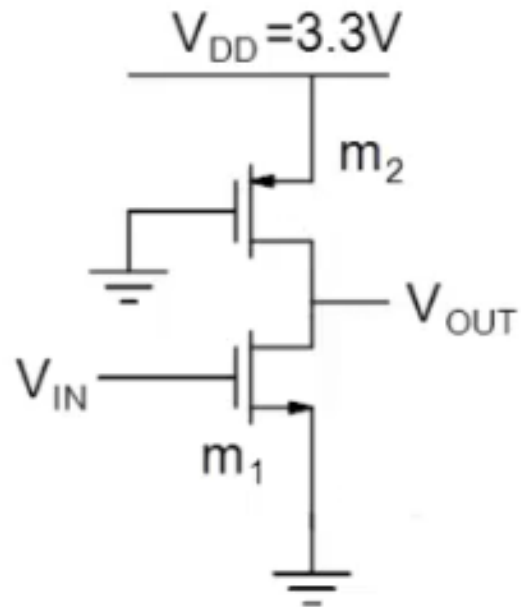
$$\tau_{PLH} \cong 0.693 \times R_D \times \tilde{C}_T$$

$$P_{static} \sim \frac{V_{DD}^2}{R_D}$$

$$P_{dynamic} = C_T \times V_{DD}^2 \times f$$

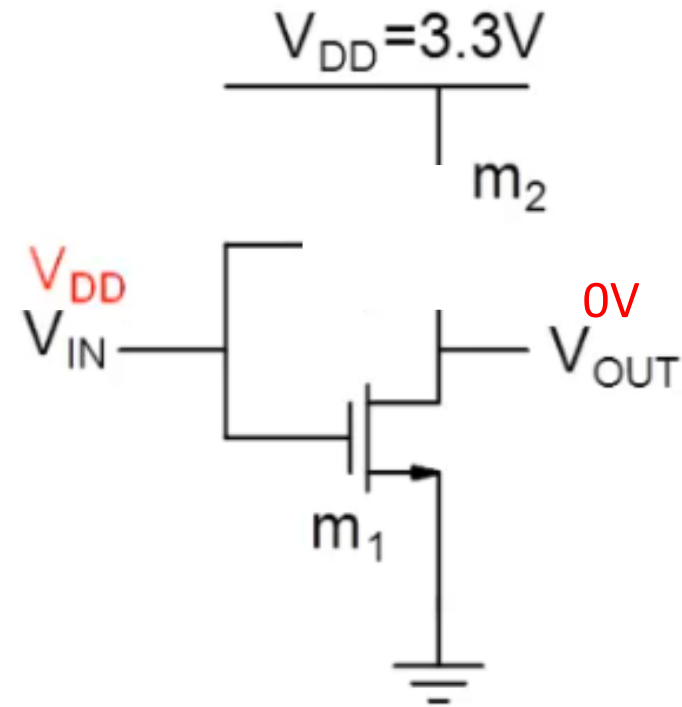
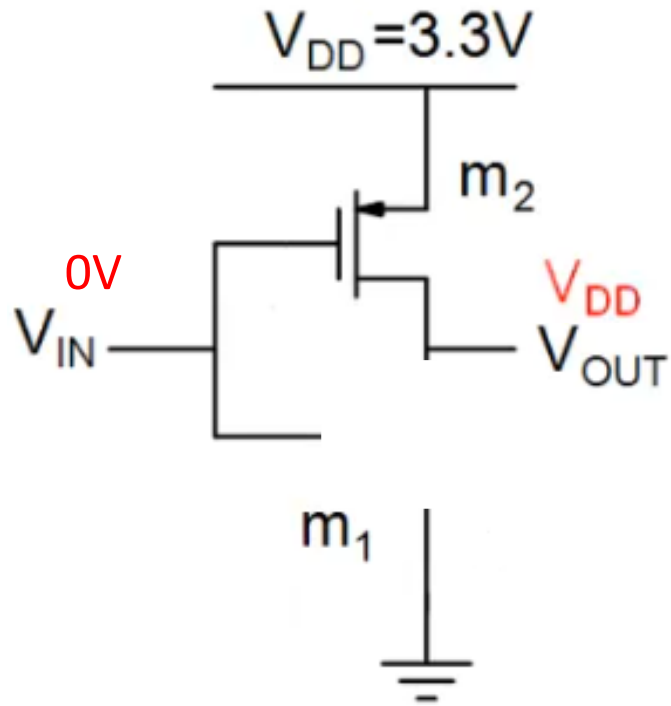


Make m_2 depletion mode



They all have static power dissipation when output is low.

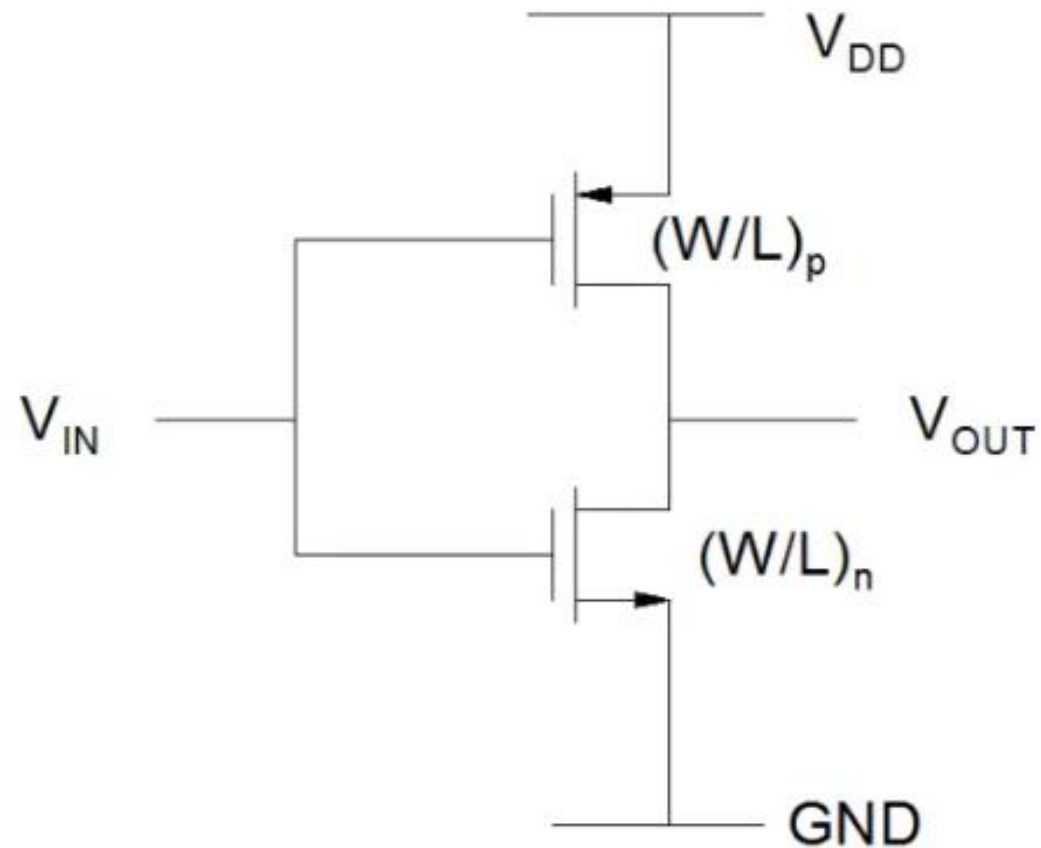
Pseudo-NMOS logic



Logic "1" is V_{DD} and "logic 0" is GND independent of size of transistors.

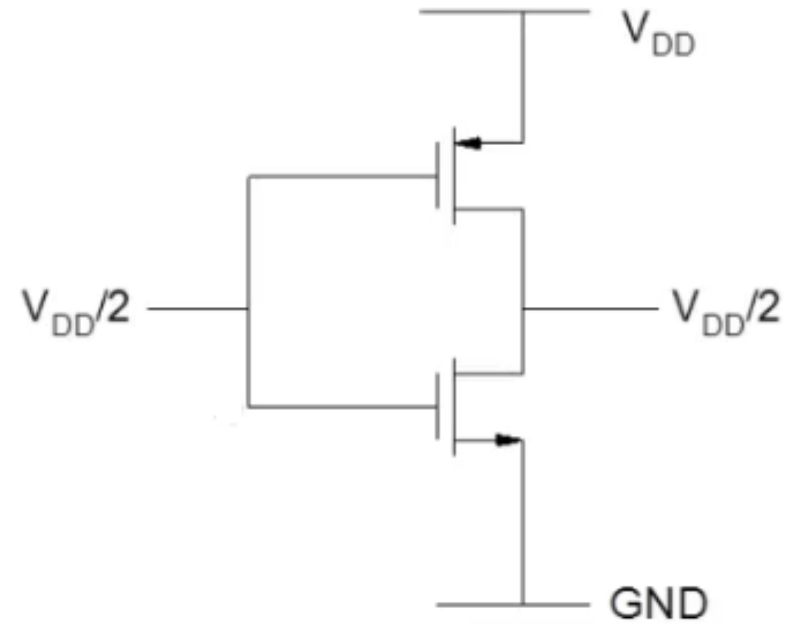
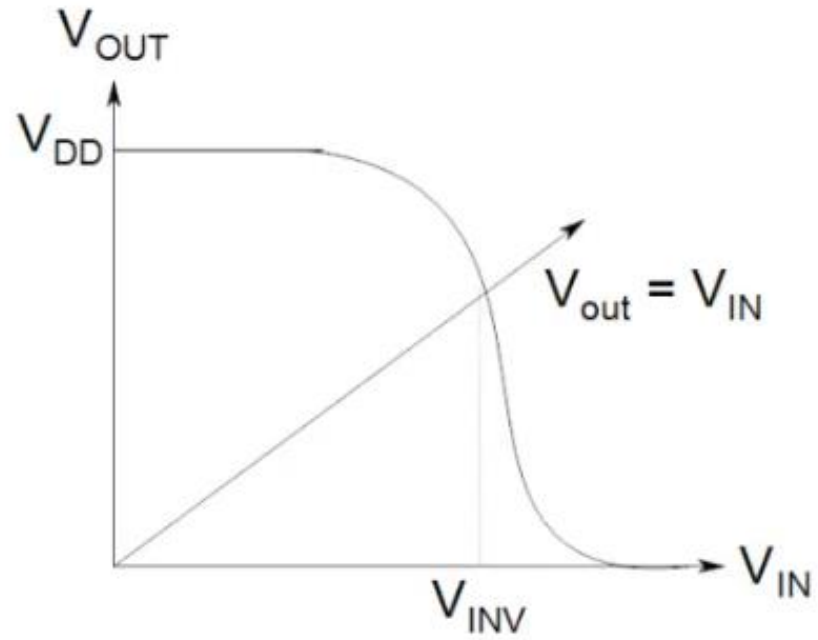
There is "no" static power dissipation in the circuit

CMOS Inverter



How should we size to obtain symmetrical VTC ?

CMOS Inverter : VTC



Both NMOS and PMOS are in saturation region

CMOS Inverter : VTC

$$I_{DSN} = I_{SDP}$$

$$\frac{\beta_N}{2}(V_{inv} - V_{THN})^2 = \frac{\beta_P}{2}(V_{SGP} + V_{THP})^2$$

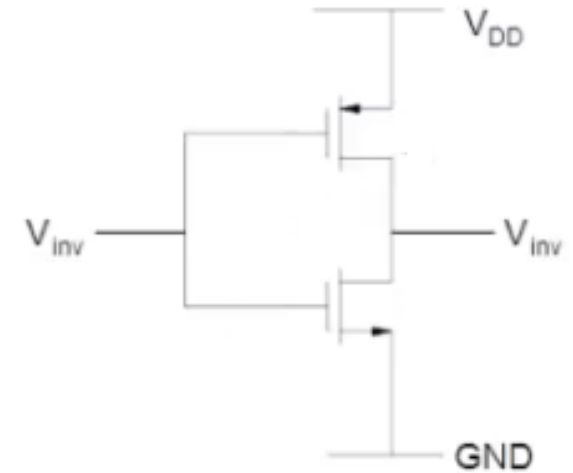
$$V_{SGP} = V_{DD} - V_{inv}$$

$$\beta_N = W_N/L_N KP_N$$

$$\beta_P = W_P/L_P KP_P$$

$$V_{INV} = \frac{V_{THN} + \frac{1}{\sqrt{\beta_R}}(V_{DD} + V_{THP})}{1 + \frac{1}{\sqrt{\beta_R}}}$$

$$\beta_R = \frac{\beta_N}{\beta_P} = \left(\frac{W_N/L_N}{W_P/L_P} \right) \times \left(\frac{KP_N}{KP_P} \right)$$



CMOS Inverter : VTC

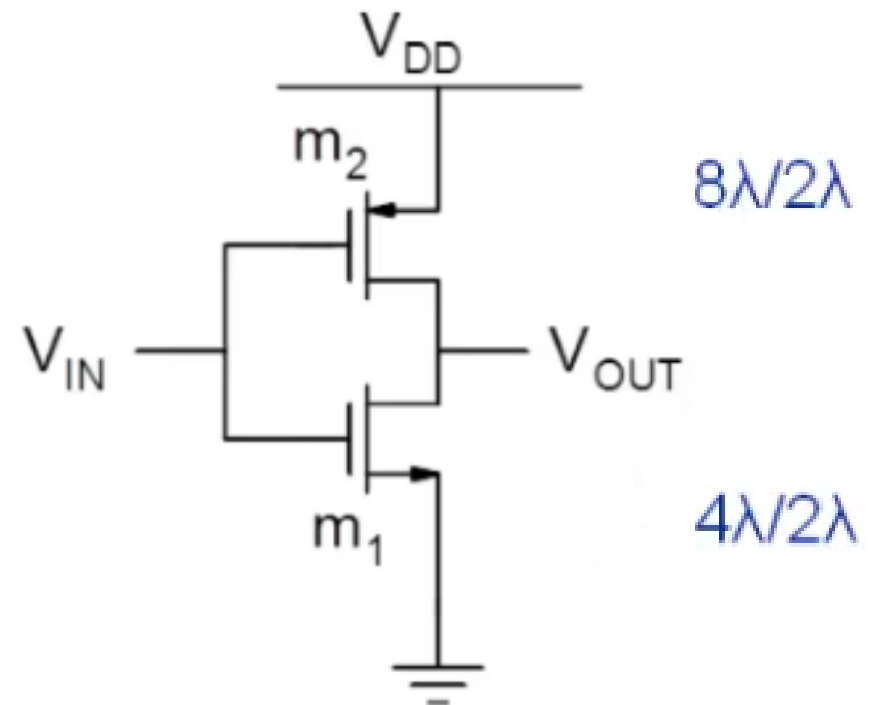
$$V_{INV} = \frac{V_{THN} + \frac{1}{\sqrt{\beta_R}}(V_{DD} + V_{THP})}{1 + \frac{1}{\sqrt{\beta_R}}}$$

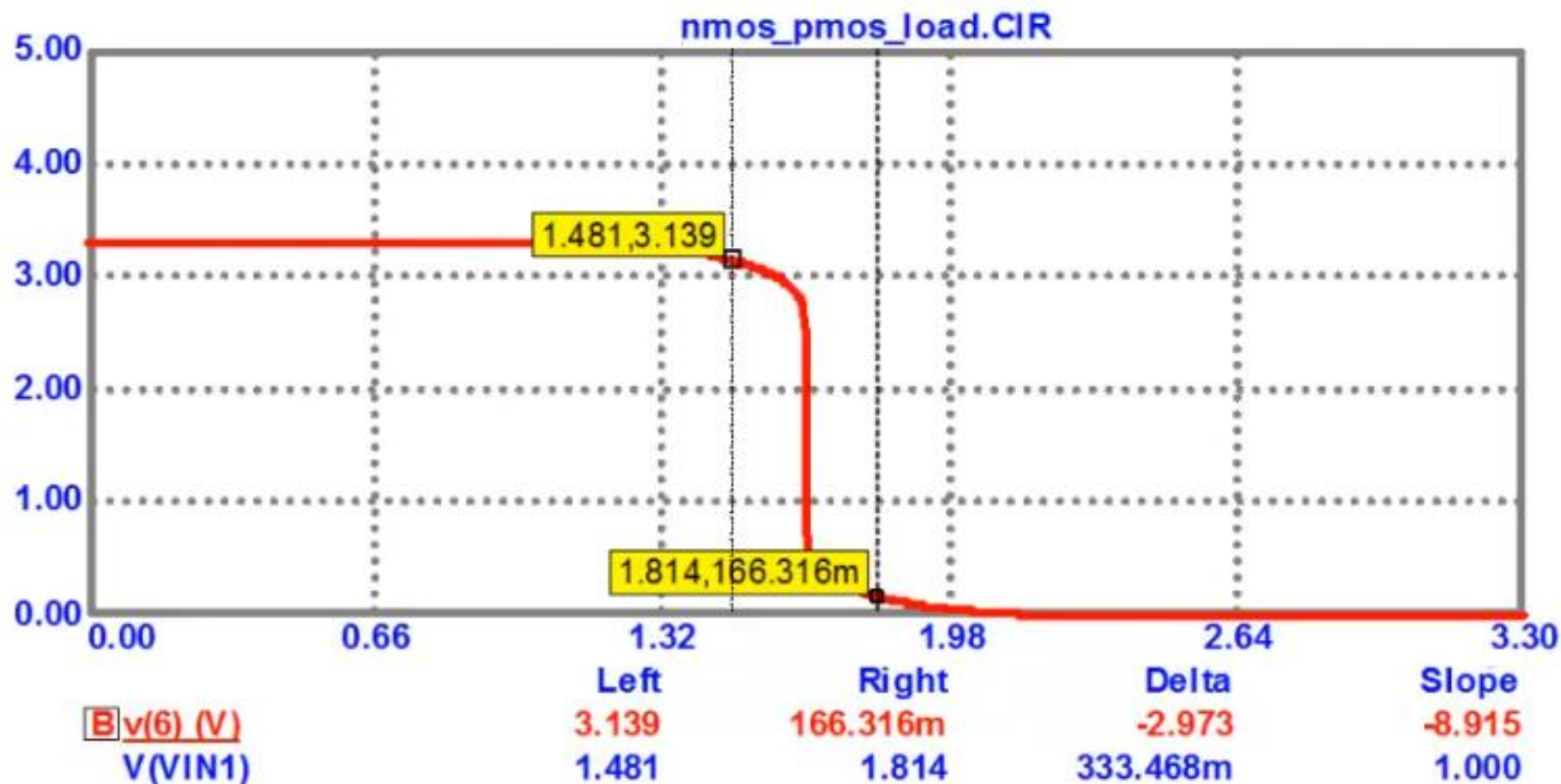
$$V_{INV} = 0.5V_{DD}$$

$$\beta_R = \frac{0.5V_{DD} + V_{THP}}{0.5V_{DD} - V_{THN}}$$

$$\Rightarrow \beta_R = 1$$

$$\frac{W_P/L_P}{W_N/L_N} = \frac{KP_N}{KP_P} \quad 2.0$$





$$V_{IL} = 1.48V; v_{ol} = 0V$$

$$V_{IH} = 1.814V; v_{oh} = 3.3V$$

$$NM_H = 1.48V; NM_L = 1.48V$$

$$\frac{NM_H}{0.5V_{DD}} = 0.9$$