Data Structure and Algorithms

Lab Report

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Experiment # 1
ASSEMBLY LANGUAGE Code

Objective

The objectives of this lab session are to understand the basic and various operations on Memory operations in Assembly Language.

Software Tool

1. Emu8086

1 Code

```
org 100h

MOV AX, 0B800h
MOV DS, AX
MOV CH, 'A'
MOV CH, 01011111b
MOV BX, 15Eh
MOV [BX], CX
ret \\   \\
```
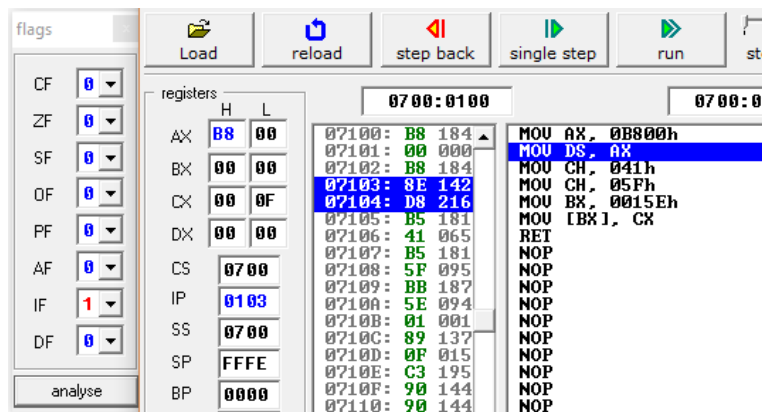
Outputs:

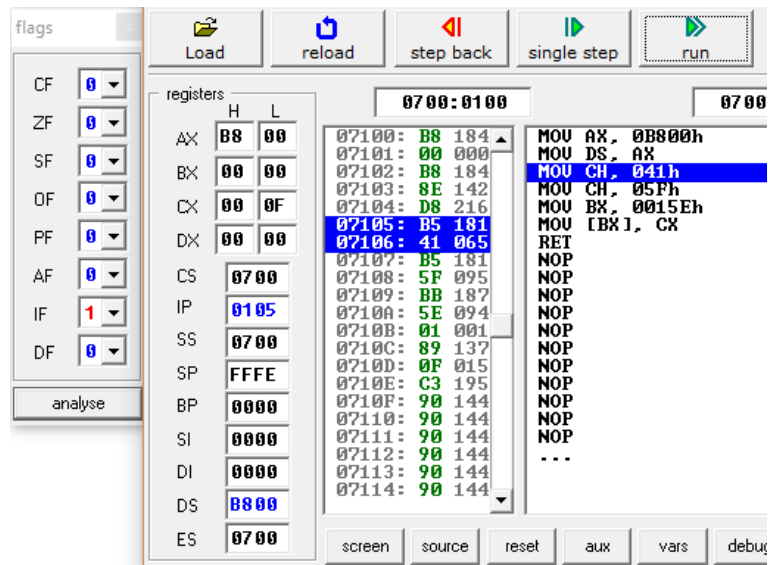
Figure : 1 (After 1st Execution)

flags

Load	reload	step back	single step	run

CF 0

ZF 0

SF 0

OF 0

PF 0

AF 0

IF 1

DF 0

analyse

registers

0700:0100

0700

```
AX  B8 00
BX  00 00
CX  00 0F
DX  00 00
CS  0700
IP  0105
SS  0700
SP  FFFE
BP  0000
SI  0000
DI  0000
DS  B800
ES  0700
```

```
07100: B8 184   MOV AX, 0B800h
07101: 00 000   MOV DS, AX
07102: B8 184   MOV CH, 041h
07103: 8E 142   MOV CH, 05Fh
07104: D8 216   MOV BX, 0015Eh
07105: B5 181   MOV [BX], CX
07106: 41 065   RET
07107: B5 181   NOP
07108: 5F 095   NOP
07109: BB 187   NOP
0710A: 5E 094   NOP
0710B: 01 001   NOP
0710C: 89 137   NOP
0710D: 0F 015   NOP
0710E: C3 195   NOP
0710F: 90 144   NOP
07110: 90 144   NOP
07111: 90 144   NOP
07112: 90 144   ...
07113: 90 144
07114: 90 144
```

screen source reset aux vars debug

Figure : 1 (After 2nd Execution)

flags

Load	reload	step back	single step	run

CF 0

ZF 0

SF 0

OF 0

PF 0

AF 0

IF 1

DF 0

analyse

registers

0700:0107

0700:

```
AX  B8 00
BX  00 00
CX  41 0F
DX  00 00
CS  0700
IP  0107
SS  0700
SP  FFFE
BP  0000
SI  0000
DI  0000
DS  B800
ES  0700
```

```
07100: B8 184   MOV AX, 0B800h
07101: 00 000   MOV DS, AX
07102: B8 184   MOV CH, 041h
07103: 8E 142   MOV CH, 05Fh
07104: D8 216   MOV BX, 0015Eh
07105: B5 181   MOV [BX], CX
07106: 41 065   RET
07107: B5 181   NOP
07108: 5F 095   NOP
07109: BB 187   NOP
0710A: 5E 094   NOP
0710B: 01 001   NOP
0710C: 89 137   NOP
0710D: 0F 015   NOP
0710E: C3 195   NOP
0710F: 90 144   NOP
07110: 90 144   NOP
07111: 90 144   NOP
07112: 90 144   ...
07113: 90 144
07114: 90 144
```

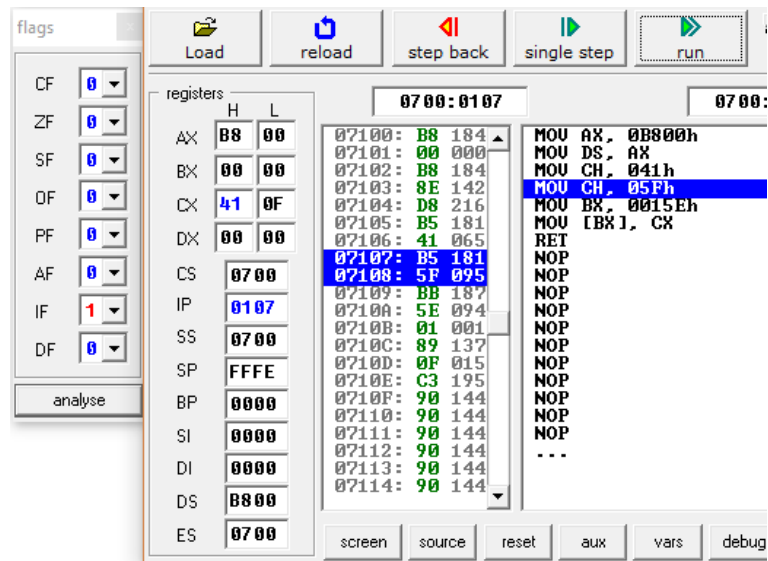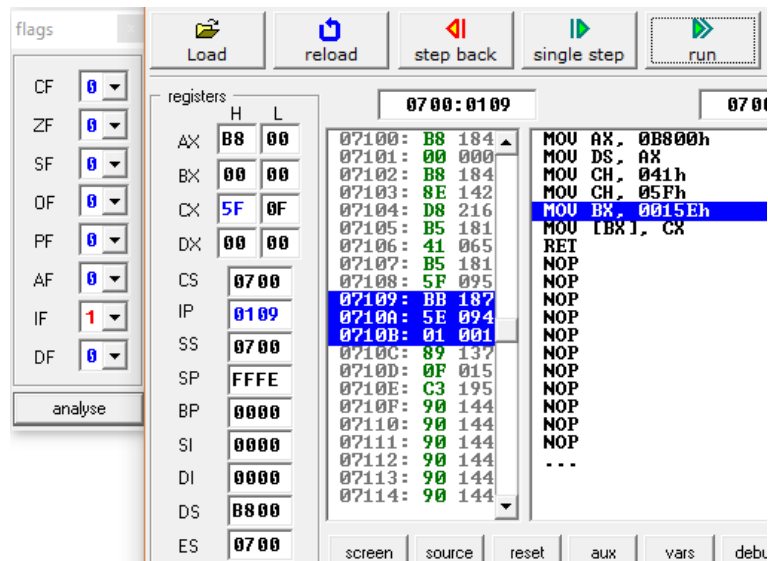screen source reset aux vars debug
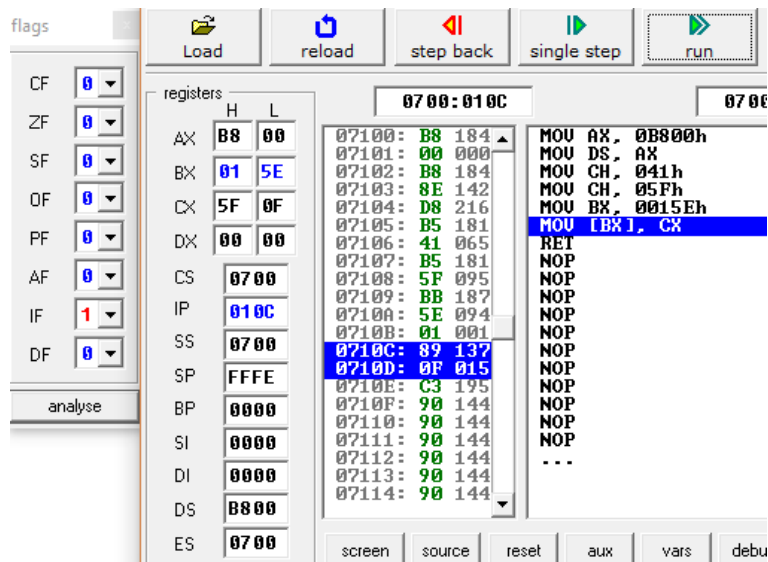
Figure : 1 (After 3rd Execution)

Figure : 1 (After 4th Execution)

Figure : 1 (After 5th Execution)

3

Load | reload | step back | single step | run | step delay ms: 0

registers

	H	L
AX	B8	00
BX	01	5E
CX	5F	0F
DX	00	00

CF 0
ZF 0
SF 0
OF 0
PF 0
AF 0
IF 1
DF 0

analyse

CS 0700
IP 010E
SS 0700
SP FFFE
BP 0000
SI 0000
DI 0000
DS B800
ES 0700

0700:010E   0700:010E

```
07100: B8 184    MOV AX, 0B800h
07101: 00 000    MOV DS, AX
07102: B8 184    MOV CH, 041h
07103: 8E 142    MOV CH, 05Fh
07104: D8 216    MOV BX, 0015Eh
07105: B5 181    MOV [BX], CX
07106: 41 065    RET
07107: B5 181    NOP
07108: 5F 095    NOP
07109: BB 187    NOP
0710A: 5E 094    NOP
0710B: 01 001
0710C: 89 137
0710D: 0F 015
0710E: C3 195
0710F: 90 144
07110: 90 144
07111: 90 144
07112: 90 144
07113: 90 144
07114: 90 144
```

emulator screen (...   —   □   ×
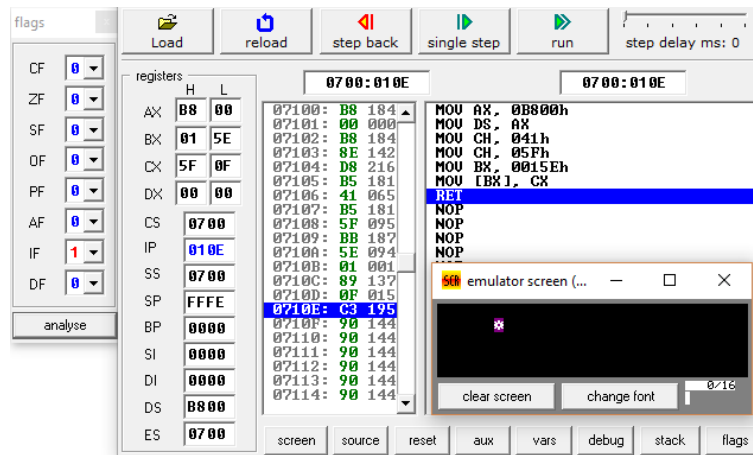
clear screen | change font | 0/16

screen | source | reset | aux | vars | debug | stack | flags

Figure : 1 (After 6th Execution)