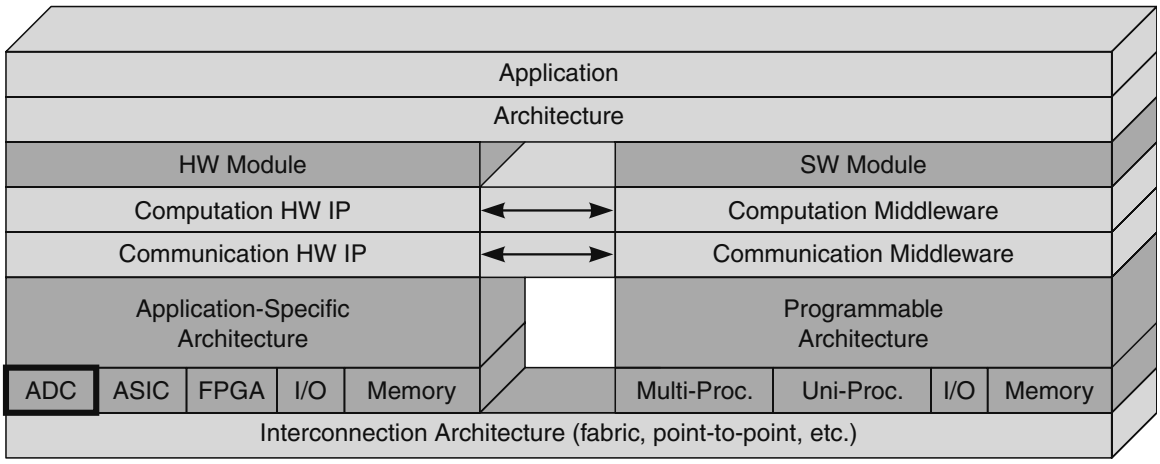
7 Analog-to-Digital Conversion

James C. Anderson and
Helen H. Kim, MIT Lincoln Laboratory



This chapter outlines the performance metrics commonly used by engineers to specify analog-to-digital conversion (ADC) requirements. An overview of the technological issues of high-end ADC architectures is also presented.

7.1 INTRODUCTION

An analog-to-digital converter (ADC) converts an analog signal into discrete digital numbers. In a sensor application, the ADC interfaces a front-end processor to an IF (intermediate frequency) circuit and converts the IF signal for digital processing. ADC characteristics (e.g., dynamic range, sampling rate, etc.) often determine the application design and performance. For example, channelization is commonly used to divide a wideband signal into narrow subbands and thus suppress the noise floor for detection of weak (below noise) signal targets. The performance of channelization is hinged on the ADC spurious-free dynamic range (SFDR). Without a sufficiently large SFDR, the target cannot be distinguished from the spurious noise.

High performance ADCs are critical in defense applications. However, in the last decade, the demand for high performance, low-cost ADCs has been driven largely by the need for rapidly improving embedded digital systems such as multifeatured cellular telephones and personal digital assistants (PDAs) to interface with a "real-world" environment. The wide range of ADC options available today requires that embedded systems designers make complex device-selection decisions based on a trade-off space with many variables, including performance, cost, and power consumption.

In July 1989, the draft form of the *IEEE Trial-Use Standard for Digitizing Waveform Recorders* (IEEE Std 1057) was issued with the intent of providing a set of measurement standards and test techniques for waveform recorders (IEEE 1989). Device characteristics measured as set forth in this standard were consistent and repeatable, so that performance comparisons could be made between devices provided by many different manufacturers (Crawley et al. 1992; 1994). Subsequently, in

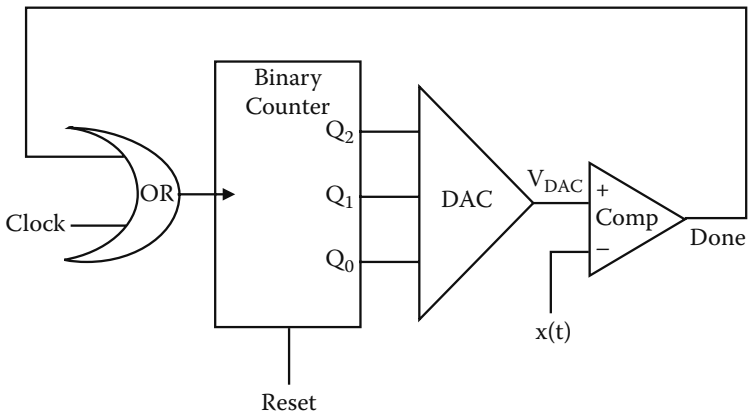


FIGURE 7-1 Conceptual analog-to-digital converter.

December 2000, the *IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters* (IEEE Std 1241-2000) was issued with the intent of identifying ADC error sources and providing test methods with which to perform the required error measurements (IEEE 2000). A subset of the IEEE performance metrics most often used by engineers to specify ADC requirements for embedded systems is outlined in this chapter, followed by an overview of the technological issues of high-end ADC architectures.

7.2 CONCEPTUAL ADC OPERATION

ADC parameters that impact performance can best be illustrated using the highly simplified, conceptual ADC design shown in Figure 7-1. Note that this conceptual ADC is not a practical architecture and is provided solely to illustrate the concept of analog-to-digital conversion.

This conceptual ADC has three bits of "resolution" (binary counter output Q_2, Q_1, and Q_0). In practice, a *sample-and-hold* (SAH) circuit prevents the ADC input, a time-varying analog voltage $x(t)$, from changing during the conversion time. For this discussion, assume that $x(t)$ does not change during the following operation. The counter stops counting when its output, which is converted into a voltage by the DAC (digital-to-analog converter), equals $x(t)$ as indicated by the comparator COMP. The counter output is then the ADC output code corresponding to $x(t)$.

Example DAC output voltages resulting from the changing binary counter values (i.e., the DAC's *transfer function*) are given in Table 7-1. In this conceptual design, the least significant bit (LSB) Q_0 corresponds to a *step size* of 0.25 volt. The resulting overall ADC transfer function (ADC digital output code vs. analog input voltage over the limited range of interest) is shown in Figure 7-2.

TABLE 7-1
Digital-to-Analog Converter Transfer Function

ADC Output Code (Q2, Q1, Q0)	V_{DAC} (volts)
000	–0.75
001	–0.50
010	–0.25
011	0.00
100	0.25
101	0.50
110	0.75
111	1.00

7.3 STATIC METRICS

The most basic ADC performance metrics deal with the static, DC (direct current, or zero-frequency constant input) performance of devices.

7.3.1 Offset Error

The offset error of an ADC, which is similar to the offset error of an amplifier, is defined as a deviation of the ADC output code transition points that is present across all output codes

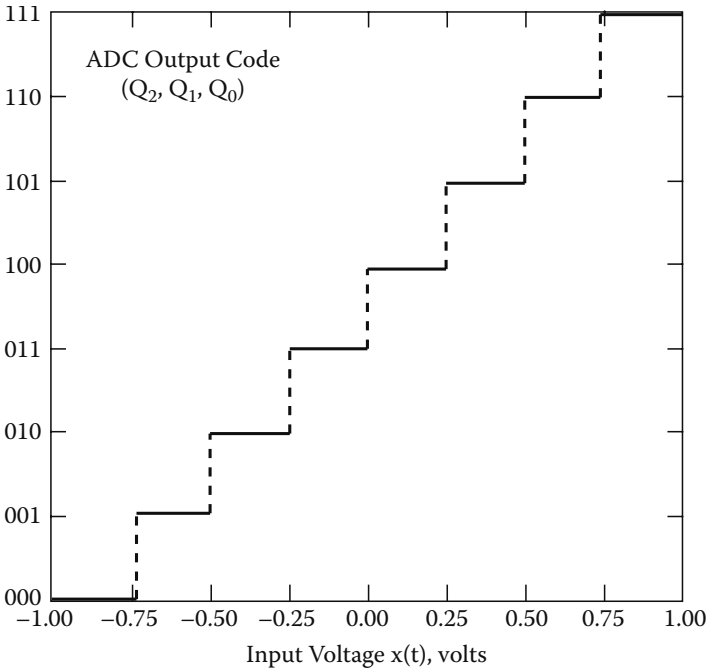


FIGURE 7-2 Conceptual ADC transfer function.

(Bowling 2000). This error has the effect of shifting, or translating, the ADC's actual transfer function away from the ideal transfer function shown in Figure 7-3. For example, by comparing the conceptual ADC's transfer function of Figure 7-2 with that of the ideal transfer function defined by Figure 7-3, it is apparent that the conceptual ADC's offset error is –1/2 LSB. In practice, the ideal transfer function may be defined by either Figure 7-2 (known as the *mid-riser* convention) or Figure 7-3 (known as the *mid-tread* convention) depending on the manufacturer's specifications for a particular ADC (IEEE 2000). Once the offset error has been characterized, it may be possible to compensate for this error source by adjusting a variable "trimming" resistor in the analog domain, or by adding (or subtracting) an appropriate offset value to the ADC output in the digital domain. Note that changes in the offset error as a function of time create a *dynamic offset error*, the effects of which may be mitigated through a variety of design techniques described later.

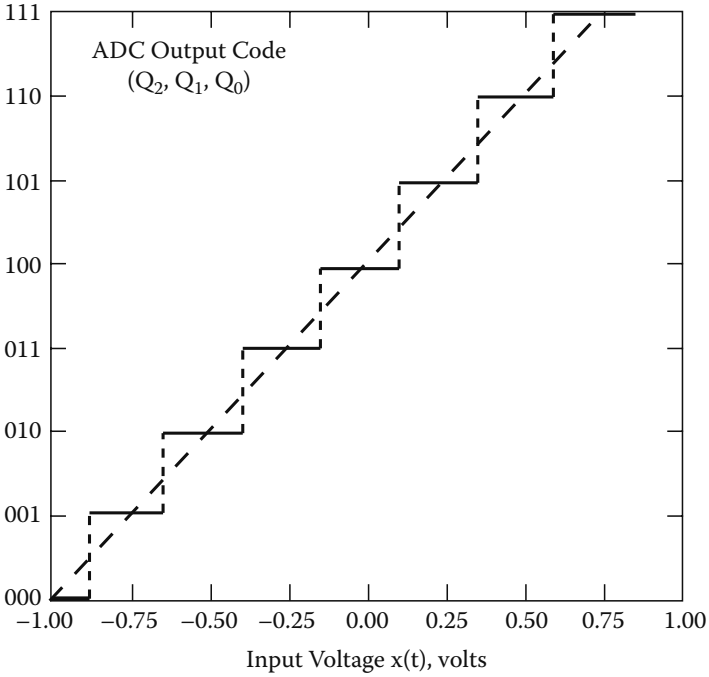


FIGURE 7-3 Ideal ADC transfer function.

7.3.2 Gain Error

The gain error of an ADC is similar to the gain error of an amplifier. Assuming that the ADC's offset error has been removed, the gain error then determines the amount of "rotational" deviation away from the ADC's ideal transfer function slope (i.e., the dashed diagonal line of Figure 7-3). Once the gain error has been characterized, it may be possible to compensate for this error source by adjusting a variable "trimming" resistor in the analog domain, or by multiplying (or dividing) the ADC output by an appropriate scaling factor in the digital domain. As with offset error, changes in the gain error as a function of time create a *dynamic gain error.*

7.3.3 Differential Nonlinearity

For an ideal ADC, the difference in the analog input voltage is constant from one output code transition point to the next. The differential nonlinearity (DNL) for a nonideal ADC (after compensating for any offset and gain errors) specifies the deviation of any code in the transfer function from the ideal code width of one LSB. DNL test data for an ADC may be provided in the form of a graph that shows DNL values (relative to an LSB) versus the digital code. If specifications indicate a minimum value of –1 for DNL, then *missing codes* will occur; i.e., specific output codes will not reliably be produced by the ADC in response to any analog input voltage. Changes in DNL as a function of time create a *dynamic DNL.*

7.3.4 Integral Nonlinearity

Integral nonlinearity (INL) is the result of cumulative DNL errors and specifies deviation of the overall transfer function from a linear response. The resulting linearity error may be measured as a deviation of the response as compared to a line that extends from the origin of the transfer function to the full scale point (*end-point* method) or, alternatively, a line may be found that provides a *best fit* to the transfer function and deviations are then measured from that line (best-fit method). Although the best-fit method produces lower INL values for a given ADC and provides a better measure of distortion for dynamic inputs, the end-point method provides a better measure of absolute worst-case error versus the ideal transfer function (Kester and Bryant 2000). Changes in INL as a function of time create a *dynamic INL.*

7.4 DYNAMIC METRICS

The static parameters described in the last section also have dynamic AC (alternating current, or time-varying input) counterparts that play an important role in the design of high-speed devices, as discussed below.

7.4.1 Resolution

ADC resolution, specified in bits, is a value that determines the number of distinct output codes the device is capable of producing. For example, an 8-bit ADC has 8 bits of resolution and $2^8 = 256$ different output codes. Resolution is one of the primary factors to consider in determining whether or not a signal can be captured over a required dynamic range with any degree of accuracy. For example, some humans can hear audio signals over a 120 dB dynamic range from 20 Hz to 20 kHz. Therefore, for certain high-fidelity audio applications, an ADC with at least a 20-bit resolution is required (i.e., $20\log_{10}2^{20} \approx 120$ dB) that can operate over this frequency range. Similar considerations apply when developing ADC requirements for communication systems that must simultaneously

receive radio signals from distant aircraft as well as from aircraft nearby. As long as the signals in space (i.e., signals traveling through some transmission medium) can be captured, it may be possible to apply digital post-processing to overcome many ADC and other system-level deficiencies. Conversely, if the ADC resolution is not adequate to capture the signals in space over the necessary dynamic range, it is often the case that no amount of digital post-processing can compensate for the resulting loss of information, and the ADC may introduce unwanted distortion (e.g., *flat topping* or *peak clipping*) in the digitized output.

7.4.2 Monotonicity

An ADC is monotonic if an increasing (decreasing) analog input voltage generates increasing (decreasing) output code values, noting that an output code will remain constant until the corresponding input voltage threshold has been reached. In other words, a monotonic ADC is one having output codes that do not decrease (increase) for a uniformly increasing (decreasing) input signal in the absence of noise.

7.4.3 Equivalent Input-Referred Noise (Thermal Noise)

Assume that the input voltage to an ADC, $x(t)$, consists of a desired signal (in this case, a long-term average value that is not changing with time) that has been corrupted by additive white Gaussian noise (WGN). Although the source of this WGN may actually be wideband thermal noise from amplifiers inside the ADC (with the WGN being added to signals within the ADC), this noise is modeled as an equivalent noise present at the input for analysis purposes [i.e., equivalent input-referred noise (Kester and Bryant 2000)].

Qualitatively, if one were to take a series of M measurements (where M is an integer >0) of the value of $x(t)$ using, for example, an analog oscilloscope with unlimited vertical resolution, then add the resulting sample values and divide by M, one would expect the noise to "average out" and leave only the desired DC value of interest. Quantitatively, this amounts to forming the sum of M Gaussian random variables, each of which has the same mean μ (voltage appearing across a unit resistance) and variance σ^2 (noise power in the same unit resistance), to obtain a new Gaussian random variable with mean $M\mu$ (corresponding to a signal power of $M^2\mu^2$) and variance $M\sigma^2$ (Walpole and Myers 1972), then dividing the result by M to obtain the average. Whereas the signal-to-noise ratio (SNR) for any individual sample, expressed in dB, is $20\log_{10}(\mu/\sigma)$, the SNR for the sum (or average) of M samples is given (in dB) as

$$\mathrm{SNR}_{\mathrm{WGN}} = 10\log_{10}(M\mu^2/\sigma^2) = 20\log_{10}(\mu/\sigma) + 10\log_{10}M\,. \tag{7.1}$$

This result indicates that, in the presence of WGN, an SNR improvement (relative to a single sample) of up to $10\log_{10}M$ dB could be obtained by digitally processing M samples (e.g., processing four samples may provide up to a 6 dB SNR processing-gain improvement when dealing with WGN).

Although Equation (7.1) was motivated by a case in which the signal portion of the input waveform did not change with time, the same result applies for any synchronously sampled periodic signal (similar to an analog oscilloscope operated in triggered-sweep mode). More generally, once any input waveform has been digitized, narrowband signals can be separated, to a great extent, from broadband WGN in the frequency domain using a variety of digital signal processing techniques.

7.4.4 Quantization Error

In addition to other noise sources, each ADC digital output sample represents the sum of an analog input waveform value with a quantization error value. The time-domain sequence of quantization error values resulting from a series of samples is known as *quantization noise*, and this type of

noise decreases with increasing ADC resolution. For this reason, embedded system designers often choose an ADC having the highest possible resolution for the frequency range of interest.

Unlike WGN, quantization noise is correlated with the input waveform. For example, if the input $x(t)$ is a constant voltage, then the quantization error and ADC output do not change from sample to sample. In this particular case, unlike WGN, no SNR improvement can be achieved by digitally processing multiple samples. Similarly, it can be shown that for many time-varying input waveforms, the quantization noise appears in the same frequency bands as the input waveform and at other frequencies as well (Bowling 2000; Kester and Bryant 2000).

A further characterization of the quantization noise is possible using probability theory (Drake 1967). Normalizing both the signal and quantization noise values to the ADC's full-scale value, the following result for quantization-noise-related SNR is valid for any number of resolution bits (N):

$$\mathrm{SNR}_{\mathrm{QUANT}} \approx (1.76 + 6.02N)\ \mathrm{dB}\ . \tag{7.2}$$

7.4.5 Ratio of Signal to Noise and Distortion

The ratio of signal to noise and distortion (SINAD) is measured using a nearly full-scale sine wave input to the ADC, where the sine wave frequency is nearly half the sampling rate. A fast Fourier transform (FFT) analysis is performed on the output data, and the ratio of the root-mean-square (RMS) input signal level to the root-sum-square of all noise and distortion components (excluding any zero-frequency component) is computed. The SINAD value, therefore, includes the effects of all noise (e.g., thermal and quantization), distortion, harmonics (e.g., DNL effects), and sampling errors (e.g., aperture jitter in the sample-and-hold circuitry) that may be introduced by the ADC. SINAD for a given ADC typically decreases as the sampling rate increases. The SINAD ratio may also be abbreviated as SNDR (signal to noise-plus-distortion ratio).

7.4.6 Effective Number of Bits

The effective number of bits (ENOB) for an ADC is computed by rearranging Equation (7.2) and using the measured SINAD instead of the theoretical $\mathrm{SNR}_{\mathrm{QUANT}}$:

$$\mathrm{ENOB} = (\mathrm{SINAD} - 1.76)/6.02\ , \tag{7.3}$$

where SINAD is expressed in dB. The ENOB for a given ADC typically decreases as the sampling rate increases.

Equation (7.3) indicates that each 6 dB increase in SINAD corresponds to an improvement of one effective bit. Therefore, when WGN is the dominant factor limiting SINAD, up to a one-bit improvement can theoretically be obtained by digitally processing sets of four samples in accordance with Equation (7.1). For example, data from a 100 MSPS (million samples per second) ADC having ENOB = 10 may be processed to generate data similar to that from a 25 MSPS ADC having ENOB = 11.

7.4.7 Spurious-Free Dynamic Range

The SFDR is a frequency-domain measurement that determines the minimum signal level that can be distinguished from spurious components, and includes all spurious components over the full Nyquist band regardless of their origin (IEEE 2000; Kester and Bryant 2000). SFDR for a given ADC typically decreases as the sampling rate increases. SFDR values may be referenced either to a carrier level (dBc) or to an input level that is nearly full-scale (dBFS), as shown in Figure 7-4. SFDR is often caused by the worst of second or third harmonic distortion. Since it is one of the main factors limiting the effectiveness of digital signal processing techniques for signal enhancement, a number of technologies have been developed to improve SFDR performance (Batruni 2006;

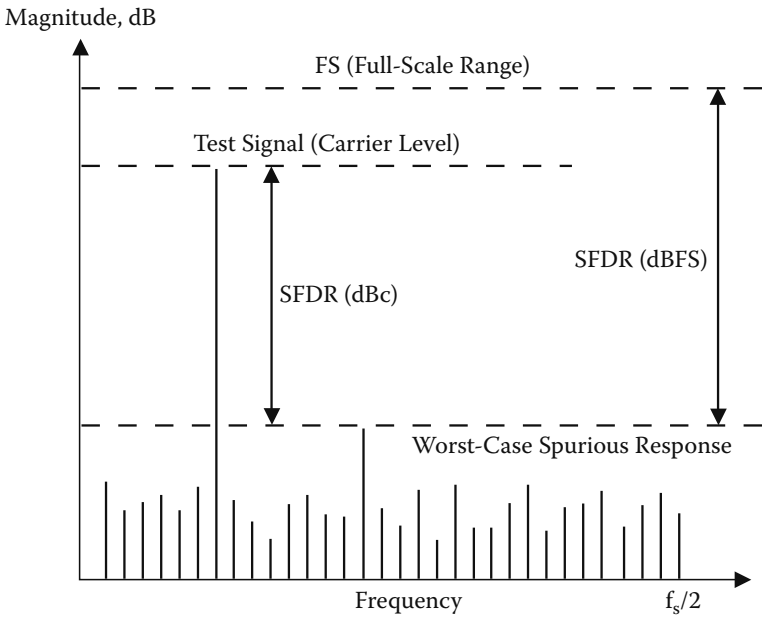


FIGURE 7-4 Spurious-free dynamic range measurement.

Lundin, Skoglund, and Handel 2005; Raz 2003; Velazquez and Velazquez 2002; White, Rica, and Massie 2003).

7.4.8 Dither

When dealing with low-level signals (on the order of a few LSBs), it is often useful to add a user-controlled dither waveform to the input waveform, causing an increase in the number of times the ADC output changes value. For example, by adding a square wave with voltage that alternates between 0 and 1/2 LSB to the sample-and-hold output, assuming the square wave has half the period of the clock used for the sample-and-hold, it may be possible to obtain sample pairs from which a new LSB can be formed via digital post-processing. Such *deterministic* dither is not limited to square waves, and sinusoids or triangle waveforms are sometimes used for ADC testing purposes (Sheingold 1972).

A more popular approach is to add *random* dither such as WGN with 1/2 LSB RMS voltage (Callegari, Rovatti, and Setti 2005; Zozor and Amblard 2005). Since 1998, some ADC manufacturers have provided on-chip circuitry that adds *pseudorandom* dither to the input while subtracting a digital estimate of the dither value from the output. In such cases, dither amplitude that is 25% of the ADC's full-scale range may be used (IEEE 2000).

7.4.9 Aperture Uncertainty

For high-speed ADCs in particular, the dominant SNR limitation may come from jitter in the sampling clock or sample-and-hold circuitry, and other short-term timing instabilities such as phase noise (IEEE 1989). For a full-scale sine wave input with frequency f_{in} (in Hz) and total RMS aperture uncertainty τ (in seconds), the maximum SNR (in dB) is approximately (Kester and Bryant 2000)

$$\mathrm{SNR}_{\mathrm{APERTURE}} = -20\log_{10}(2\pi f_{in}\tau) \,. \tag{7.4}$$

For example, the aperture uncertainty of the conceptual ADC sampling at 1 Hz must be <16 msec RMS to achieve ENOB ≈ 3. Similarly, if aperture uncertainty is the dominant component of SINAD, then an ADC with τ = 1 ps RMS sampling a 100 MHz sine wave will have ENOB < 10.3.

Note that, for a given aperture uncertainty, $SNR_{APERTURE}$ decreases by 6 dB (and ENOB decreases by 1 bit) for every doubling (i.e., octave) of f_{in}.

7.5 SYSTEM-LEVEL PERFORMANCE TRENDS AND LIMITATIONS

Historic ADC device-level performance improvement rates may not be sustainable as technical and economic limits are approached, and rates may also level off after requirements for key markets have been met. For example, by 2002, ADCs for the digital audio market had achieved 24-bit resolution (with ENOB = 18) over a 40 kHz analog input bandwidth and provided an audio quality exceeding the discrimination limits of human hearing (AES 2003; Aude 1998; Neesgaard 2001). Future performance improvements for these ADCs are likely to be limited by internal thermal noise considerations, but the bandwidths of these devices may continue to increase due to future improvements in semiconductor processes. Although devices with greater bandwidth may well find application in broadband sonar systems, the sonar market may be much smaller than the historical consumer digital audio market. Therefore, future improvements are more likely to lie in the areas of cost and power reduction or addition of special features (e.g., on-chip data buffers and anti-aliasing filters) rather than performance parameters.

In many cases, individual ADC chips can be interconnected to form small subsystems that fill a need not otherwise met at the component level. By 2003, for example, commercial off-the-shelf (COTS) ADC modules were available with 12-bit resolution (ENOB = 9.8) at 400 MSPS created from a pair of 12-bit ADCs (each with ENOB = 10.5 @ 210 MSPS) and onboard digital post-processing. This two-way time-interleaved, or "ping-pong," approach doubled the sampling rate while losing ~0.7 effective bit compared to the individual component ADCs. More recently, time-interleaved designs ranging from 16-way (Elbornsson et al. 2005) to 80-way on a single chip (Poulton et al. 2003) have been developed. Also in 2003, an effort to combine ADCs for higher resolution yielded COTS modules with 16-bit resolution (ENOB = 12.9) at 80 MSPS created from four 14-bit ADCs (each with ENOB = 12.0 @ 105 MSPS) and onboard digital post-processing. Note that, in the following, no distinction is made as to whether any given specification was achieved using a single monolithic ADC versus a multichip module.

For applications in which the input waveform has a small bandwidth with respect to its center frequency (e.g., as in radio receivers), it is often convenient to represent the digitized signal as a sequence of complex numbers in the time domain. This representation may be achieved by multiplying the narrowband analog input waveform with a cosine wave having the same center frequency as that of the input waveform, then low-pass filtering the result to form an in-phase, or I, waveform prior to conversion by an ADC (Shaw and Pohlig 1995). The narrowband waveform is simultaneously multiplied by a sine wave and filtered to form a quadrature, or Q, waveform prior to conversion by a separate ADC. Once digitized, the I samples are generally taken as the real part of a complex sample, while the Q samples form the imaginary part. Using this approach, it is possible to digitize the input signal using a pair of ADCs, each of which operates at a sampling rate (in samples per second) that numerically corresponds to the input signal bandwidth (in Hz), rather than using a single ADC operating at a rate that numerically corresponds to twice the input signal bandwidth and produces purely real samples. For such applications, it is desirable to use a pair of ADCs on the same chip to minimize I/Q channel mismatch, and many dual converters have on-chip circuitry to facilitate operation in either an I/Q or two-way time-interleaved mode.

7.5.1 Trends in Resolution

Figure 7-5 is intended to give a sense of improvements in resolution for state-of-the-art COTS ADCs over a 20-year time span. One particularly noteworthy trend is that, from 1992 through 2003, 12-bit devices (ENOB ≈ 10) roughly doubled in speed every three years.

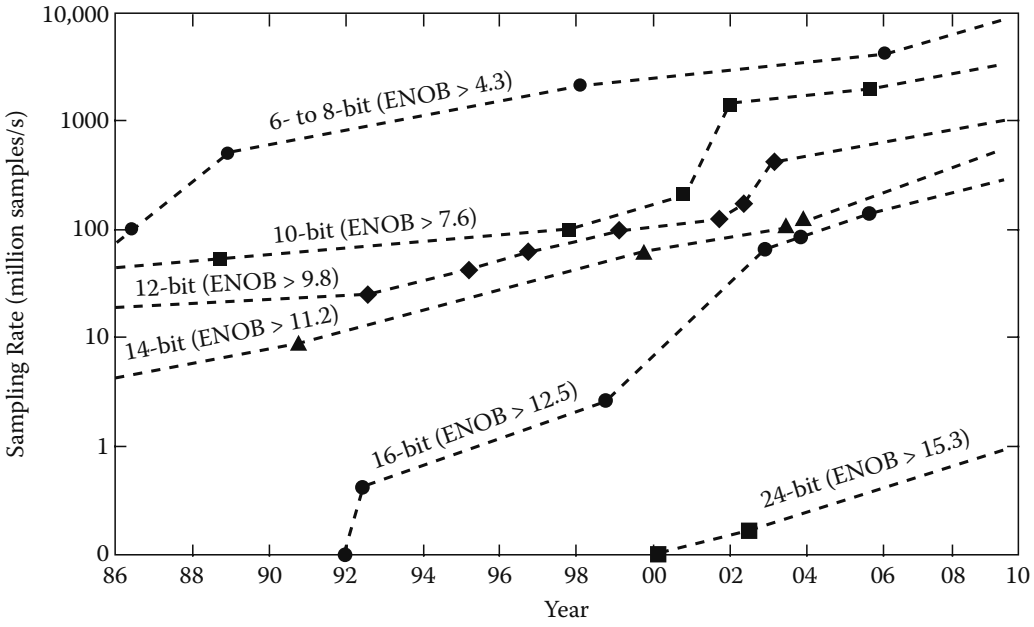


FIGURE 7-5 Resolution improvement timeline.

Trend lines at the right-hand side of Figure 7-5 give a general indication of possible near-term future resolution improvements. For example, as of 2004, a system had been demonstrated [incorporating the non-COTS ADC of Poulton et al. (2003)] that could digitize a 5 GHz sine wave (using a 10 GSPS effective sampling rate with data from a 20 GSPS data stream) with ENOB = 5.0. Therefore, there is no theoretical limitation that would preclude a COTS ADC from achieving such a performance level in the foreseeable future. Aperture uncertainty limits the near-term future performance of 10-bit ADCs (ENOB ≈ 8) to 3 GSPS, 12-bit ADCs (ENOB ≈ 10) to 1 GSPS, and 16-bit ADCs (ENOB ≈ 12) to 200 MSPS, while 14-bit devices are expected to lie between the 12- and 16-bit ADCs. Thermal noise is expected to limit the 24-bit devices (ENOB ≈ 16) to <1 MSPS.

7.5.2 Trends in Effective Number of Bits

From 1999 through 2005, the ENOB for 100 MSPS state-of-the-art COTS ADCs improved at a rate of approximately 0.28 bit per year, as shown in Figure 7-6. Over the same time period, the sampling

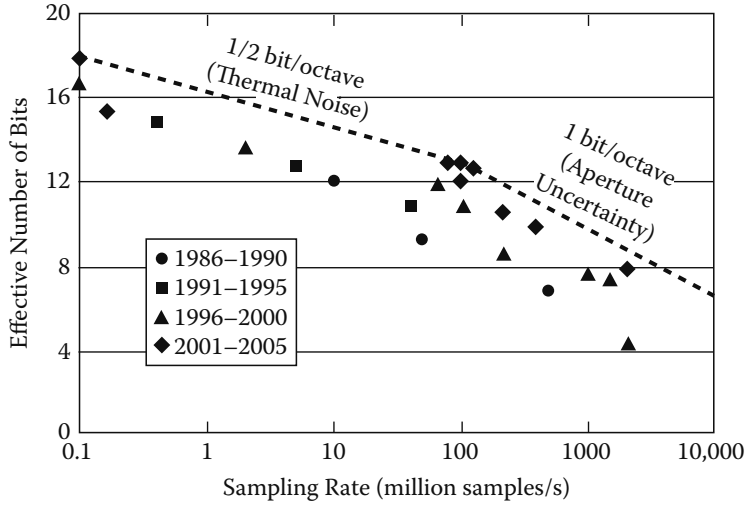


FIGURE 7-6 ENOB (effective number of bits) improvements.

rate of the fastest COTS ADCs (with ENOB ≈ 7.7) roughly doubled (i.e., the equivalent of up to 0.5 bit processing gain in 6.3 years).

Future ENOB improvements may depend on the ability of manufacturers to overcome certain design challenges which may or may not prove to be "hard limits." For example, a 34 ohm resistor produces 150 nV RMS thermal Johnson noise across a 40 kHz bandwidth (i.e., the mean-square voltage per Hz is $4RkT$, where R is in ohms, k is Boltzman's constant = 1.38×10^{-23} Joule per degree Kelvin and T is 298 degrees Kelvin at room temperature), which is one-half the step size of a 24-bit resolution ADC with 5 V full-scale range. If design of ADCs with such a low input resistance presents a significant challenge, then future ENOB improvements for low-speed, high-resolution ADCs are likely to be limited by thermal noise from their internal circuitry. Although such noise can be mitigated through the use of cryogenics and superconducting materials, it remains to be seen if such technologies are appropriate for COTS ADCs (Mukhanov et al. 2004). Similarly, although optical technologies are being investigated to mitigate the effects of aperture uncertainty (and for other reasons as well), such technologies have not historically been applicable to COTS ADCs (Juodawlkis et al. 2003; Miao et al. 2006).

As shown in Figure 7-6, a monolithic 16-bit (ENOB = 12.8) 100 MSPS COTS ADC was available by the end of 2005. This device lies near the intersection of two theoretical performance limiter lines (the dotted lines shown in Figure 7-6), one representing thermal noise corresponding to a 2000 Ω equivalent resistance and the other representing 0.2 ps aperture jitter (Le et al. 2005; Walden 1999). Note that these performance limiters are not intended to represent hard limits for COTS devices, as semiconductor process improvements continue to reduce aperture uncertainty. Rather, as shown in the following, these lines are used to illustrate an important design trade-off space.

When digitizing a signal that has frequency components distributed throughout a range from 0 to 12.5 MHz, for example, it is necessary to place a 12.5 MHz bandwidth low-pass anti-aliasing filter prior to the ADC (although some modern ADCs have such circuitry on chip). In this example, the ADC must sample the signal at or above the Nyquist rate of 25 MSPS. Figure 7-6 indicates that a suitable COTS ADC may not be readily available at this sampling rate, so instead consider the use of an ADC with ENOB = 12.8 operating at 100 MSPS to obtain a set of samples. The resulting samples may then be digitally processed to obtain a data stream approximating that from an ADC operating at 25 MSPS and having ENOB up to 13.8 (i.e., an improvement of 0.5 bit/octave). In this example, the anti-aliasing filter bandwidth remains at 12.5 MHz to eliminate any out-of-band signals that might otherwise dominate ADC resolution requirements. Note that the digital post-processing discussed here is directed toward reducing noise that has been introduced by the ADC, rather than reducing noise that may have corrupted a signal prior to its arrival at the ADC input (as discussed later). The 100 MSPS ADC with ENOB = 12.8 could similarly be used in lieu of ADCs with sampling rates down to approximately 100 KSPS (i.e., 10 octaves, with correspondingly lower anti-aliasing filter bandwidths), providing up to five additional effective bits. Below 100 KSPS, as shown in Figure 7-6, COTS ADCs with ENOB ≈ 17.8 are available that may offer lower cost and power versus the 100 MSPS ADC.

Figure 7-6 shows a rapid drop-off in performance (more than 1 bit/octave) above ~100 MSPS for COTS technology ca. 2005, primarily due to aperture uncertainty. As a result, it may not be desirable to use higher-speed ADCs with reduced ENOB in lieu of lower-speed devices with higher ENOB above ~100 MSPS. For example, if a signal is sampled at 2 GSPS using an ADC with ENOB = 7.8, then digital post-processing may only provide the equivalent of ENOB = 9.8 at 125 MSPS, whereas COTS ADCs are available that provide ENOB = 12.6 (i.e., an improvement of 2.8 effective bits) at this rate.

7.5.3 Trends in Spurious-Free Dynamic Range

Like ENOB, the SFDR data shown in Figure 7-7 fall off with increasing sampling rate and exhibit a steeper fall-off above 100 MSPS. Over the last 20 years, SFDR for state-of-the-art COTS ADCs has

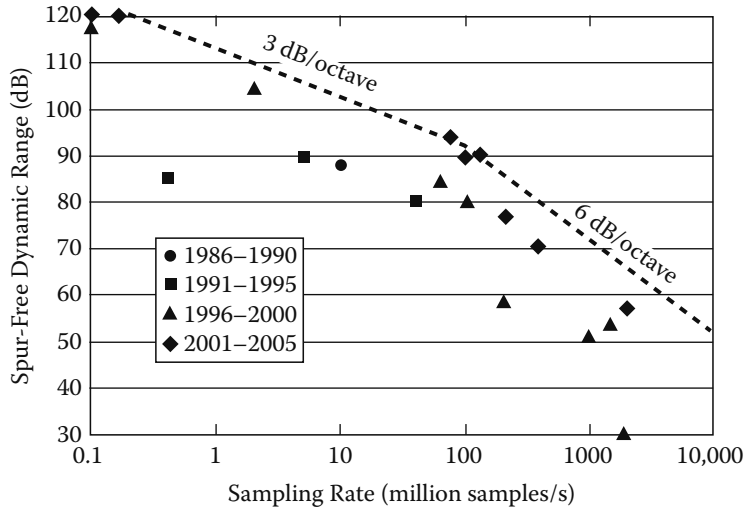


FIGURE 7-7 SFDR (spurious-free dynamic range) improvements.

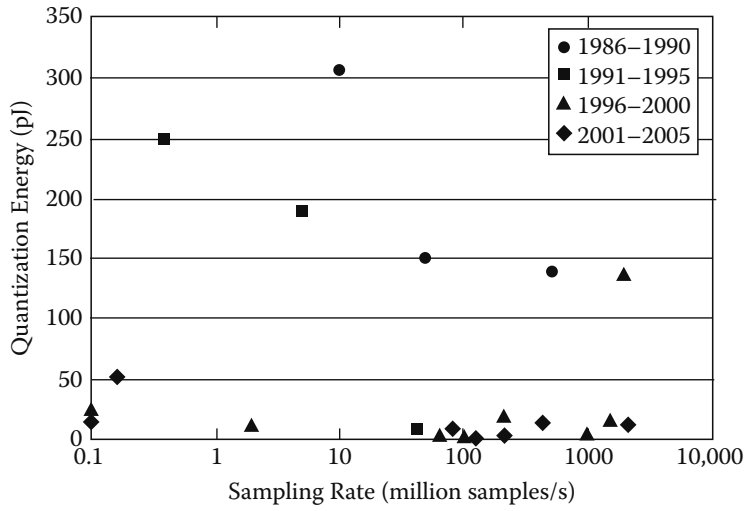


FIGURE 7-8 EQ (energy per effective quantization level).

generally improved at a rate consistent with improvements in ENOB. However, it must be cautioned that Figure 7-7 shows only approximate values due to variations in manufacturer's specifications (e.g., values may be in dB with unspecified measurement technique, dBFS or dBc).

7.5.4 Trends in Power Consumption

One useful power-performance figure of merit is the ADC energy required per effective quantization level, or EQ:

$$\text{EQ} = \text{Power}/[2^{\text{ENOB}} \times (\text{Sampling rate})], \tag{7.5}$$

where power is in watts, sampling rate is in samples per second, and EQ is in Joules (noting that 1 pJ = 10^{-12} watt-sec). As shown in Figure 7-8, there are many examples of COTS ADCs in the 2001–2005 time frame with EQ < 5 pJ.

For sampling rates in excess of approximately 200 MSPS, an on-chip demultiplexer (DMUX) capability is often included to provide multiple ADC output data streams at rates compatible with low-cost, low-power processors and memories. The DMUX, whether on-chip or external, may be an important factor in system-level power consumption. For example, a 2 GSPS ADC in 2005 included

an on-chip 1:4 DMUX and provided EQ = 15 pJ. This is a substantial improvement over 2002, when the same manufacturer provided a comparable ADC with EQ = 27 pJ, or EQ = 61 pJ when operating with the manufacturer's external DMUX.

7.5.5 ADC Impact on Processing Gain

In the preceding discussion, care has been taken to distinguish noise introduced in the analog-to-digital conversion process from other types of noise (e.g., noise that corrupts a signal traveling through a transmission medium, or that enters a receiver chain prior to an ADC). However, it is often the case that digital signal processing techniques applied to an ADC output data stream attempt to compensate for many different noise sources simultaneously, regardless of the noise's origin (e.g., receiver "nonlinear equalization"). The degree to which such post-processing can succeed depends to some extent on ADC performance parameters, as outlined in the following.

First, consider the numerical representation of data from a 24-bit ADC having ENOB = 18. Assume that accuracy of the conversion process is limited by thermal noise coming from within the ADC, and it is not necessary to add dither. If each 24-bit ADC output sample is to be numerically represented as an "IEEE 754 format" 32-bit floating-point word, then care must be taken to map the ADC's most significant bit (MSB) into the sign bit of the floating-point word, and the ADC's 23 LSBs into the 23-bit mantissa of the floating-point word. A variety of digital signal processing techniques can then be applied that will automatically replace the sample bits with "effective" bits in the 23-bit mantissa (up to a limit of 5 bits from processing gain in addition to the original 18 effective ADC bits). In practice, the ADC's SFDR performance typically limits the processing gain to approximately 5 bits (i.e., an additional 30 dB) or less.

In applications that require separation of narrowband signals from broadband noise, an algorithm such as the FFT may be used to provide processing gain. In the complex radix-2 FFT, for example, each butterfly stage provides a factor of two bandwidth reduction, causing rejection of half the noise power and providing a 3 dB (0.5 bit) SNR improvement. A $2^{10} = 1024$-point complex FFT has 10 stages, with the output potentially providing up to 5 bits processing gain simultaneously within each of the 1024 distinct output frequency bins (assuming any desired signal lies entirely within one frequency bin). This result is comparable to the 30 dB maximum processing gain when 1024 samples are processed to remove WGN, as indicated in Equation (7.1). Since FFT processing is typically performed on samples of a broad bandwidth ADC input waveform that contains both signals and noise, ADC performance parameter variations across the input waveform's entire frequency range must be taken into consideration for post-processing purposes.

7.6 HIGH-SPEED ADC DESIGN

The increasingly closer placement of the ADC to the antenna in a radar processing flow has created strong demands of wideband and high dynamic range ADCs. For instance, a 0.3 m spot size of synthetic aperture radar (SAR) imaging requires 600 MHz of instantaneous bandwidth, which is currently limited by ADC performance. In addition, clutter cancellation and Doppler processing require high SNR, SINAD, and SFDR, which implies at least 8 to 10 ENOB. The high-speed ADCs discussed in this section are those that operate in the range from hundreds of MSPS to several GSPS and provide 8 to 10 ENOB.

The current semiconductor process has produced transistors with high transit frequencies (f_T, the frequency at which the transistor current gain drops to unity). For example, transistors fabricated in the 90 nm CMOS (complementary metal oxide semiconductor) and 130 nm SiGe BiCMOS (bipolar CMOS) processes have f_T's that approach 100 GHz and 200 GHz, respectively. A myth in ADC technology is that "device scaling alone will push f_T up and thus the sampling rate higher, and power dissipation lower." However, scaling alone has not provided the desired ADC performance. New architectures and circuit topologies are needed to take advantage of new devices. For example,

the 8-bit Maxim MAX108 (1.5 GSPS), which was fabricated in 2000 using a bipolar process with 29 GHz f_T, dissipates approximately 5.3 W. In 2005, National Semiconductor introduced a dual 8-bit ADC (ADC08D1500), which was built using a 0.18 μm CMOS process with a 49 GHz f_T. This 1.5 GSPS dual ADC chip dissipates only ~1.8 W. This nearly 6× reduction in power dissipation was made possible by applying new circuit techniques and architectural solutions that take advantage of the faster process.

The effect of scaling on the performance of ADCs is a mixture of benefits and detriments. For example, the reduced power-supply voltage forced by the reduction of gate length (CMOS) or emitter width (bipolar transistors) has been a serious challenge for analog and ADC designers for some time. The scaling without new circuitry and architecture will not yield a dramatic improvement in performance. The development of high-speed ADCs requires a thorough understanding of the limiting factors of resolution, sampling rate, and power dissipation, as well as the impacts of architecture and circuit design techniques on them. Two of the most common architectures for medium resolution ADCs, flash and pipeline architectures, will be used to discuss these design issues.

7.6.1 Flash ADC

A parallel or flash architecture achieves the highest conversion rate at the cost of area and power consumption. As shown in Figure 7-9(a), an n-bit converter comprises $2^n - 1$ comparators and subsequent decoding stages. The comparators compare the analog input voltage V_{in} simultaneously with $2^n - 1$ equally spaced reference voltages V_{r1} through V_{rn}, quantizing the signal into a so-called thermometer code. The thermometer code, which consists of a list of "0's" followed by a list of "1's," is named after the reading style of a mercury thermometer. For example, in an 8-bit flash ADC, $n = 8$, so 255 comparators are used. If the full-scale reference voltage V_{ref} is 1 V, the resistor ladder divides V_{ref} into 256 equal segments (i.e., $V_{r1} = 1/256$ V, $V_{r2} = 2/256$ V, etc.). Figure 7-9(a) shows that the level of V_{in} triggers the lower five comparators to produce a thermometer code of 00…011111. The digital encoder converts the thermometer code to a binary number 00000101 (5 in decimal).

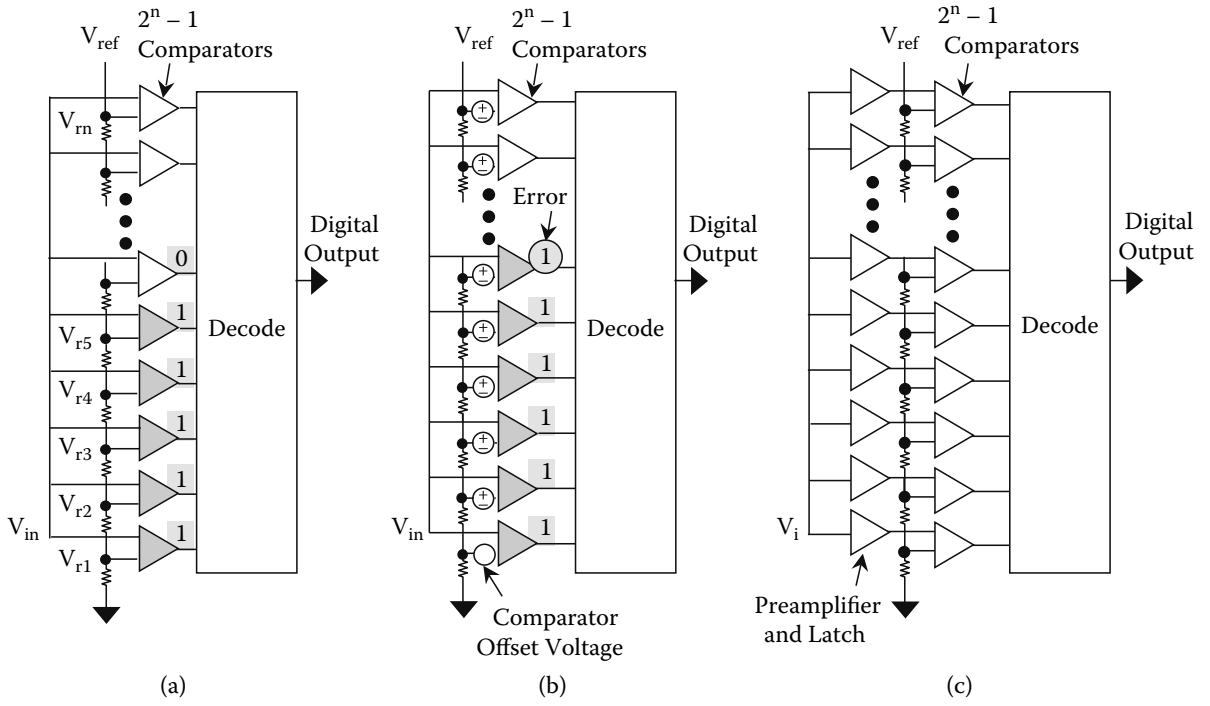


FIGURE 7-9 An n-bit flash ADC: (a) basic architecture; (b) model with comparator offset voltages; (c) the use of preamplifiers and latches to correct offset voltages.

The above explanation assumes that all comparators (255 in the example) are sensing the incoming voltage accurately. However, due to mismatch between transistors, comparators unavoidably have offset voltages, which are modeled by the voltage sources added to the reference voltages in Figure 7-9(b). Typical comparator offset voltages are 2 to 10 mV for silicon bipolar technology, 15 to 50 mV for CMOS technology (Bult and Buchwald 1997), and >50 mV for III-V (e.g., GaAs) technology. In the 8-bit ADC example, a 5 mV offset voltage (>1 LSB = 4 mV) could have caused comparators 1 to 6 (or 1 to 4) to be triggered and resulted in an error, as shown in Figure 7-9(b). Since offset voltages are caused by random, statistical events in the fabrication process, in order for the 8-bit ADC to have a 99% yield, the offset voltage should be <0.2 LSB (0.8 mV in the ongoing example) (Kinget and Steyaert 1996; Uyttenhove and Steyaert 2002).

Figure 7-9(c) shows that in order to minimize the impact of offset voltages, each comparator is equipped with a preamplifier (preamp) and a latch (see also Figure 7-11). The preamp gain reduces the offset voltage in the reference caused by the latch. The gain of a preamp implemented in a bipolar technology is typically 3× to 5×. Depending on the required amount of offset reduction, more than one stage of preamplification may be needed to achieve the necessary gain. Unfortunately, preamps also have offset voltages (0.1 to 2 mV for silicon bipolar technology, 3 to 10 mV for CMOS technology, and >20 mV for III-V technology), so a delicate design optimization is needed to achieve the desired accuracy.

As the gate length (or emitter width) scales down, the supply and reference voltages must also be scaled down. In Figure 7-9, if V_{ref} is 0.5 V, the LSB is reduced to merely 2 mV. The offset voltage must also be scaled down to maintain the same performance. However, it was shown that the mismatch parameters contributing to offset voltages had been scaling down up to, but not beyond, the 180 nm CMOS technology (Kinget and Steyaert 1996). The reason for the discontinuity of scaling is that there are two major mismatch parameters: variation in threshold voltage V_T, and variation in gain β. As the oxide thickness scales down with a finer gate-length technology, the mismatch due to V_T has been scaling proportionally. However, the mismatch due to β has not scaled as fast as that of V_T. Up to the 180 nm CMOS technology, the impact of V_T mismatch dominates. For 120 nm and a gate-over-drive voltage (i.e., gate voltage – V_T) of 0.2 V, the β mismatch becomes dominant (Uyttenhove and Steyaert 2002).

The slow scaling of the offset voltage is the fundamental limitation to accuracy in advanced ADC technology. Additional preamp stages and larger-size transistors and resistors can somewhat improve the situation at the expense of higher power dissipation since larger devices require more current to drive. The power-dissipation situation may worsen when the technology is scaled for higher f_T. Analog designers have developed architectural solutions to overcome this limitation. Techniques that alleviate the non-scaling effect of offset voltage are discussed below.

Instead of increasing the preamp device size and thus the power consumption, various averaging techniques have been successfully implemented (Bult and Buchwald 1997; Choi and Abidi 2001; Kattmann and Barrow 1991). First presented in Kattmann and Barrow (1991), the averaging technique has reduced the dynamic differential nonlinearity error by 3× and improved the 8-bit ADC yield by 5×.

The averaging technique presented in Kattmann and Barrow (1991) places series resistors between neighboring preamp output loads, as shown in Figure 7-10(a). Instead of taking an output voltage from an individual preamp, the averaging resistor network averages the preamp output value. Figure 7-10(b) shows a preamp bank with series resistors R_{A1} to $R_{An\text{-}1}$ placed between R_{L1} and R_{Ln}. While Figure 7-10(b) shows an implementation of the preamps in bipolar technology, the same architecture is also applicable to the CMOS technology. Other examples of averaging technique to further improve offset voltages can be found in Bult and Buchwald (1997) and Choi and Abidi (2001).

Another factor limiting the ADC resolution is the input-referred noise of the preamp and latch combination. The signal at the latch is higher in amplitude so the noise of the preamp usually dominates the result. Figure 7-11 shows a simplified comparator consisting of a differential pair preamp

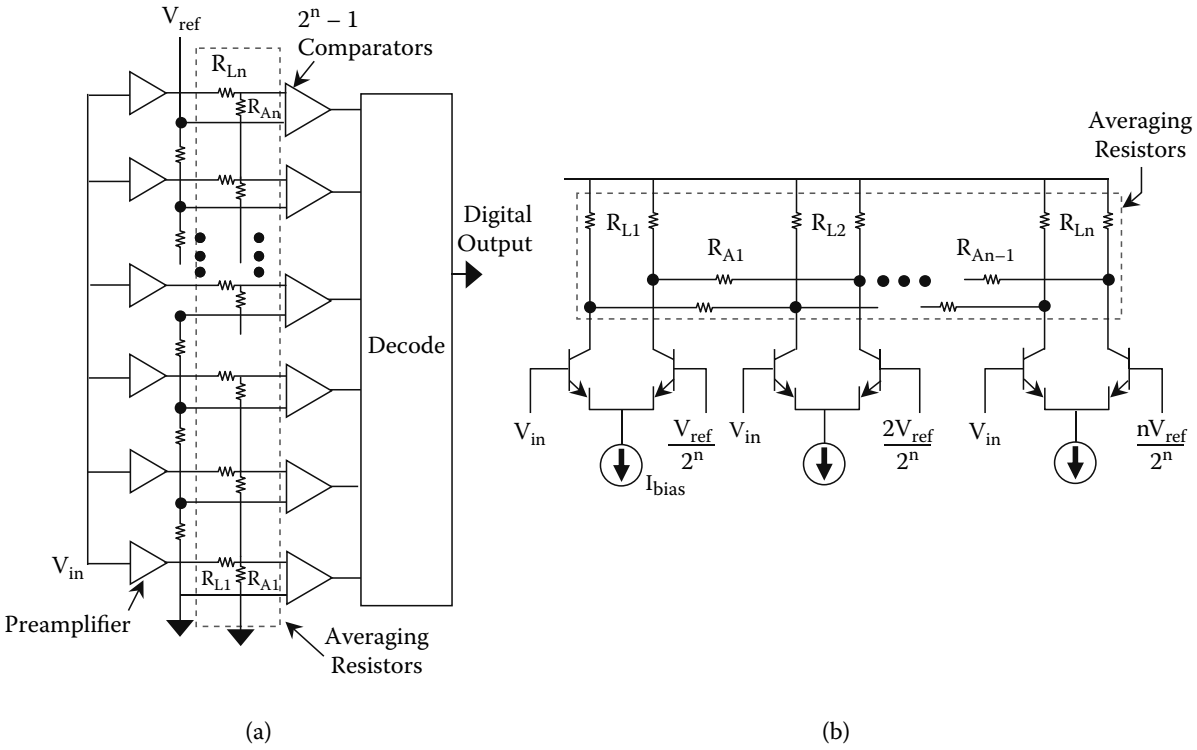


FIGURE 7-10 (a) A simplified flash ADC with averaging resistor network; (b) preamps with averaging resistor network.

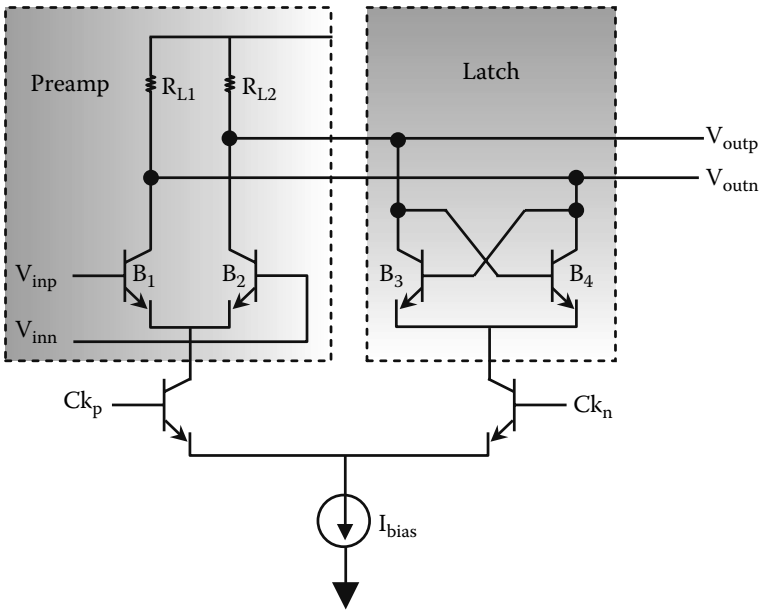


FIGURE 7-11 A comparator composed of preamp and latch.

and a latch implemented in bipolar technology. The input-referred noise of the preamp consists of thermal and shot noise.

The noise spectral density is the thermal and shot noise of transistors B_1 and B_2 and the thermal noise of the load resistors R_{L1} and R_{L2} (Gray et al. 2001). The spectral density of input-referred noise is

$$\begin{aligned} v_n^2/\Delta f &= 4kT(r_{b1}+r_{b2}+r_{e1}+r_{e2})+4kT(1/2g_{m1}+1/2g_{m2}) \\ &\quad +4kT(1/g_{m1}^2R_{L1}+1/g_{m2}^2R_{L2}), \end{aligned} \tag{7.6}$$

where r_{b1} and r_{b2} are the base resistance of transistors B_1 and B_2, respectively; r_{e1} and r_{e2} are the emitter resistance of transistors B_1 and B_2, respectively; g_{m1} and g_{m2} are the transconductance of B_1 and B_2; R_{L1} and R_{L2} are the load resistors of the preamp. In Equation (7.6), the first and second terms are the thermal noise and shot noise of B_1 and B_2, respectively, and the third term is the thermal noise of R_{L1} and R_{L2} (see Section 7.5.2).

The following example is used to illustrate the limiting effect of the input-referred noise on the ADC resolution. Typical values are used in this example: the collector currents of B_1 and B_2 are ~1 mA; g_{m1} and g_{m2} are ~0.02 A/V; R_{L1} and R_{L2} are 200 Ω, which give ~400 mV of differential swing at the output; and r_b and r_e are ~50 Ω and ~35 Ω, respectively. Also, assume that the tail current of the comparator, I_{bias}, is 2 mA. The offset requirement usually determines the differential gain of the preamp. Using the typical values in this example, this gain is

$$A_v = R_{L1}/(1/g_{m1} + r_{e1}) = 200/[(1/0.0386) + 35] \approx 3.3\ . \tag{7.7}$$

The spectral noise density is determined by Equation (7.6) as $v^2_n/\Delta f = 3.3 \times 10^{-18}$ V²/Hz. If the input signal bandwidth is 1 GHz, the input referred noise voltage is ~58 μV. For an 8-bit ADC, the total input-referred noise of 255 preamps is ~922 μV. The noise-induced SNR loss, which is referred to as $SNR_{penalty}$ and defined in Equation (7.8), should be limited to <3 dB or about 1/2 LSB (Vorenkamp and Roovers 1997).

$$SNR_{penalty}(\text{dB}) = 20 * \log\sqrt{1+\frac{v_n^2}{\varepsilon_q^2}}\ , \tag{7.8}$$

where v_n is the total input-referred noise and ε_q is the quantization noise.

In this example, the $SNR_{penalty}$ is 2.2 dB < 3 dB, which is acceptable (assuming the input swing is 1 V). The thermal noise of the transistors B_1 and B_2 dominates the noise, which is typical when the signal bandwidth is much less than the f_T of the device. The designer can increase the device size to reduce the thermal noise. However, just as in the case of the offset voltage, a larger device area does not only reduce r_b and r_e, but also increases the input capacitance and limits the bandwidth. This is a design trade-off that a designer must make.

The limited preamp bandwidth also affects the ADC resolution. As shown in Figure 7-12(b), the ADC input signals distributed to the multiple comparators do not arrive at the same time. This variable delay can cause an incorrect input signal level when the latch is triggered, leading to an error in the digital readout as indicated in the example of Figure 7-12(a). The propagation delay is caused by the parasitic nonlinear capacitance of the comparators, the routing capacitance, the varying input signal level, and the limited bias current. A combination of these effects causes a third-order harmonic distortion in the ADC (Dalton et al. 1998), which causes distortion and degrades SFDR and SINAD of the ADC (Peetz, Hamilton, and Kang 1986). As the preamp bandwidth is limited by the nonlinear capacitance, the relationship between the third-order harmonic distortion and the preamp bandwidth at different input voltage swings can be established (van de Plassache 1994). For instance,

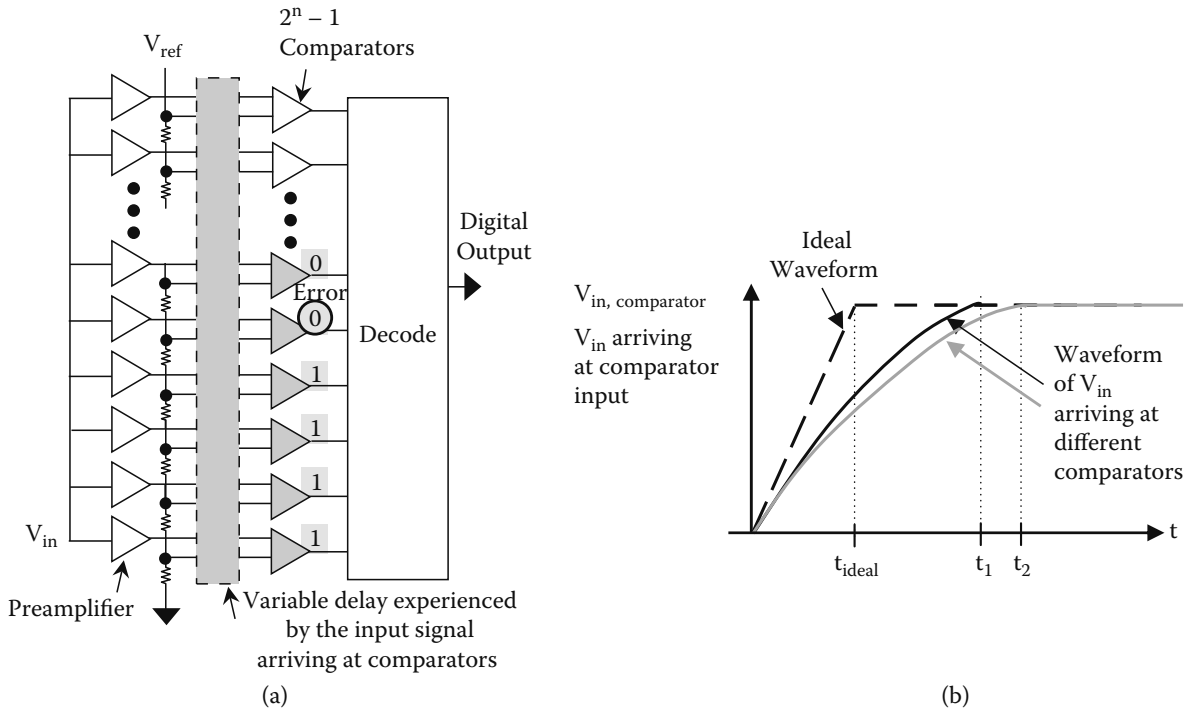


FIGURE 7-12 (a) Comparators experiencing an effective variable delay at the input; (b) waveforms of input signal arriving at comparator inputs at different times.

according to van de Plassche (1994), if we want to achieve –55 dBc of third-order distortion level for an input swing of 1 V, the preamp bandwidth should be 10× the input signal bandwidth.

Ideally, the unity gain bandwidth of a preamp is close to the f_T of the technology. However, in order to reduce offset and noise, the devices in an ADC are often designed to be larger than minimum size so their f_T's are typically less than the value quoted (for minimum size devices). Also, although the bias current is set high enough to drive the input swing without causing distortion, it is generally set at a level that is slightly lower than what is required to support the peak f_T. This bias current reduction is necessary to avoid the high-level injection that causes f_T to drop rapidly if the bias current exceeds the level associated with the peak f_T.

The bandwidth of the latches in a flash ADC is much higher than the preamps. The flash ADC sampling rate is thus constrained by the speed of its preamps. As an example, the unity gain frequency can be ~35 GHz for a preamp fabricated in 0.18 μm CMOS (with a peak f_T of 49 GHz). As the gain-bandwidth product is a constant, if a preamp gain of 10× is needed to reduce the offset voltage, the bandwidth of preamp is ~5 GHz. The input signal bandwidth for the ADC is then 0.5 GHz, which requires a Nyquist sampling rate of 1 GSPS.

As discussed and illustrated in Figure 7-12(b), the signals arriving at the comparators may experience variable delay. In theory, a flash ADC structure does not require the use of a sample-and-hold amplifier (SHA). However, the use of an SHA to feed the comparators alleviates the dispersion problem pronounced at higher sampling rates (e.g., >100 MSPS). Figure 7-13 shows an 8-bit flash ADC enhanced with an SHA. The SHA samples and holds the input value (at 22 mV in Figure 7-13) and the comparators compare the held value with equally spaced reference voltages.

7.6.2 Architectural Techniques for Power Saving

As mentioned earlier, the MAX108 (Maxim) and the ADC08D1500 (National Semiconductor) ADCs dissipate 5.3 W and 1.8 W, respectively. Besides a 2× improvement in f_T, (49 GHz versus 29 GHz), the significant power reduction (6×) is the result of the architectural techniques (e.g., folding, interpolation, interleaving, and calibration) used extensively in the ADC08D1500.

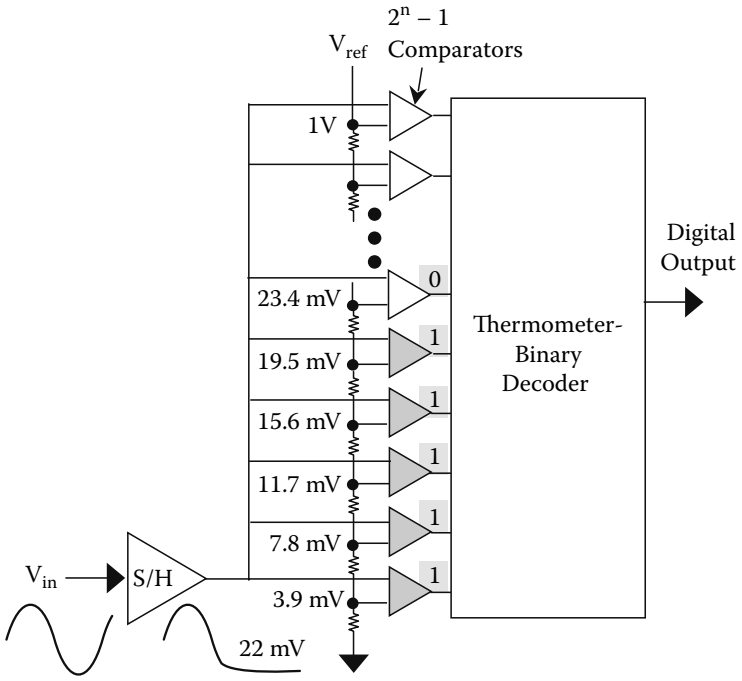


FIGURE 7-13 Eight-bit flash ADC with a sample-and-hold circuit.

In the example shown in Figure 7-9, each comparator dissipates 7.2 mW (assuming a 1.8 V power supply). For an 8-bit flash ADC, the comparators alone consume ~2 W (255 × 7.2 mW). A high-speed ADC requires the use of an SHA, which can consume 100 mW or more. Note that the total ADC power dissipation figure also has to account for the power consumption of the resistor ladder network, decoder, bias circuits, demultiplexer, and clock driver. For a flash architecture, the power dissipation depends on the resolution and the sampling rate. The power dissipation is proportional to 2^N, where N is the number of resolution bits. Also, for a given resolution, the power dissipation goes up with the sampling rate (Onodera 2000).

One of the power-saving techniques is to reduce the number of comparators by folding. The folding technique allows a single comparator to be associated with multiple preamps. Figure 7-14(a) shows a modified flash architecture with folding, which is similar to the two-step architecture of a coarse-fine approach shown in Figure 7.14(b). In the two-step architecture, a coarse flash ADC gen-

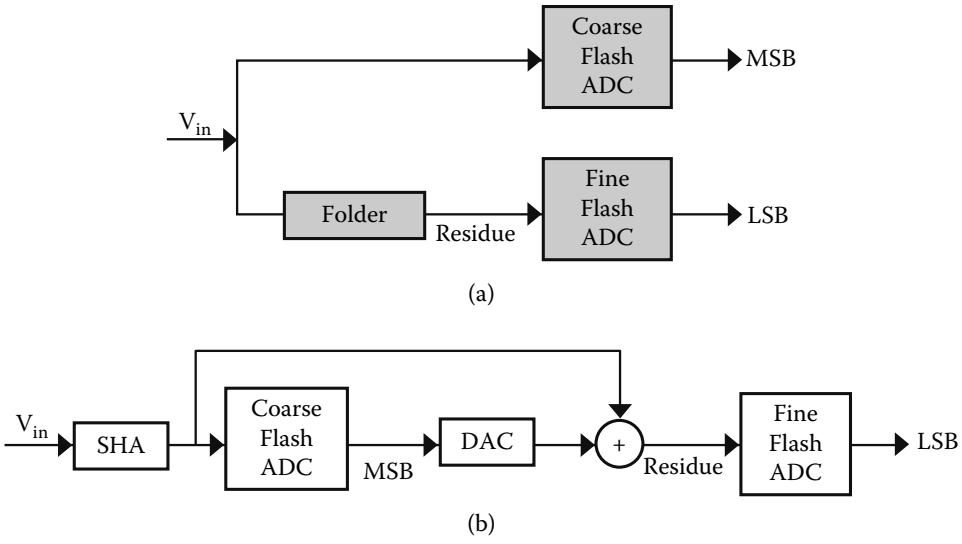


FIGURE 7-14 (a) Flash ADC architecture with a folder; (b) two-step ADC architecture.

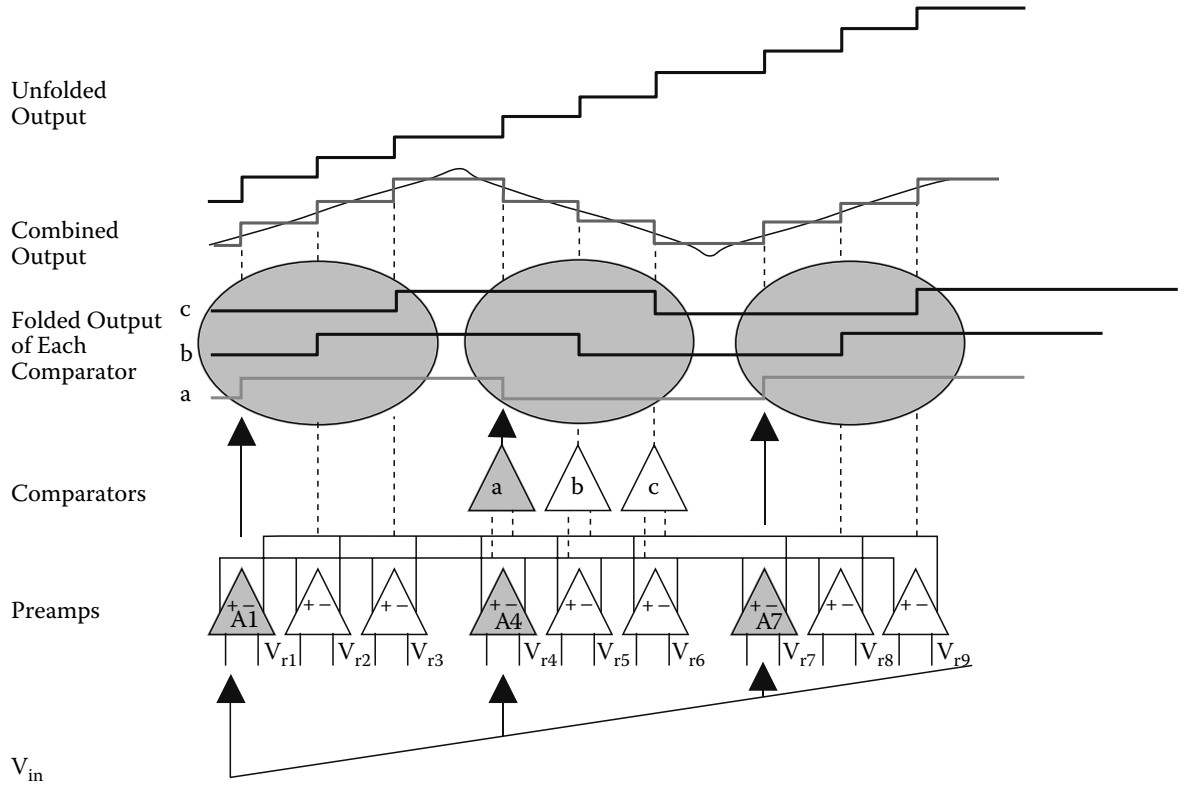


FIGURE 7-15 Folding example.

erates the MSBs of the result. A DAC converts the MSBs back into an analog signal. The residue (i.e., the difference between the original input signal and the DAC output) goes through a fine flash ADC to generate the LSBs of the result. The major difference between the folding and two-step architectures is that the former remains a parallel approach, in which a folder circuit produces the residue for the conversion of LSBs. In theory, the folding ADC does not require an SHA, but in practice one is often included to minimize the distortion, especially at high sample rates (e.g., >100 MHz).

The bandwidth of an op-amp-based, switched-cap SHA is roughly $f_T/6$ to $f_T/10$ (Cho 1995). As the bandwidth must be at least 10× the sampling rate to minimize distortion, the sampling rate of an ADC with sample-and-hold is limited to $\sim f_T/60 - f_T/100$.

The maximum input voltage level is divided into regions, each of which covers multiple reference voltages. The input signal is then folded into these regions. Figure 7-15 shows an example of folding by three (Bult and Buchwald 1997). Instead of assigning a single reference voltage to a comparator, in a folding architecture each comparator is associated with three separate preamps. For instance, comparator *a* is connected to preamps A1, A4, and A7.

For the sake of illustration, V_{in} is shown as a ramp signal in Figure 7-15. When V_{in} passes the threshold set by reference voltage $Vr1$, the output of preamp $A1$ switches from low to high. As V_{in} continues to increase, it exceeds $Vr4$ of the second preamp A2, and as this amplifier has reversed polarity, it will cause the comparator to go from high to low. At the moment the input signal passes the amplifier on the right, the comparator will again change from low to high. Comparator *b* will be connected to preamps A2, A5, and A8, producing the folded output curve *b*, and Comparator *c* will be connected with A3, A6, and A9, producing the folded output curve *c*. Figure 7-15 also shows the combined output and the unfolded output.

For an 8-bit ADC, the number of comparators can be reduced from 255 to 87 ($2^N/k + k - 1$, where k is the folding factor and assume $k = 3$). However, the power dissipation would not be reduced by a factor of three because the bias current of the preamps must increase to accommodate the folding. An interpolation technique can be used to eliminate some preamps and thus further reduce the power dissipation. For instance, instead of using 255 preamps for distinct reference volt-

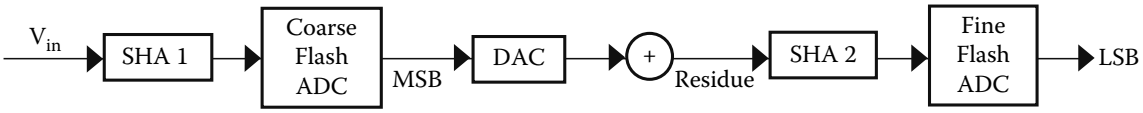


FIGURE 7-16 Two-step pipeline ADC.

age points, a design can use 64 preamps and interpolate the reference voltage points between them with resistive dividers. Because multiple folding amplifiers are connected to a comparator, the load resistor and parasitic capacitance at the output of the folding amplifiers can limit the bandwidth and cause distortion. Therefore, the folding amplifier should be designed to have a bandwidth at least 10× larger than the maximum input frequency to keep the SINAD degradation to less than 3 dB (Limotyrakis, Nam, and Wooley 2002). With fewer comparators, the large offsets become a significant problem that requires offset cancellation. This offset issue is especially significant in the CMOS technology, which is the reason why folding and interpolation techniques appear first in the bipolar process (van de Grift and van de Plassche 1984; van de Plassche and Baltus 1988), and subsequently migrate to the BiCMOS (Vorenkamp and Roovers 1997) and CMOS (Bult and Buchwald 1997; Taft et al. 2004) processes.

7.6.3 Pipeline ADC

Section 7.6.2 discussed the use of folding [Figure 7-14(a)] and two-step architectures [Figure 7-14(b)] to mitigate the problems of high power dissipation and large footprint area of a full flash architecture. In a two-step ADC, the entire conversion—which consists of the operations of an SHA, a coarse flash ADC, a DAC, a subtraction, and a fine flash ADC—must be completed in one sampling period. The sampling rate is thus limited by the settling time of these components. A folding architecture alleviates this issue by precomputing the residue. Alternatively, as shown in Figure 7-16, an SHA (SHA2) can be inserted before the fine flash ADC to form a two-step pipeline operation. While SHA2 holds a sample (i.e., the residue) for the conversion of the fine ADC, SHA1 holds the next sample for the coarse ADC, virtually doubling the throughput. The two-step architecture can be generalized into the *k*-stage pipeline shown in Figure 7-17.

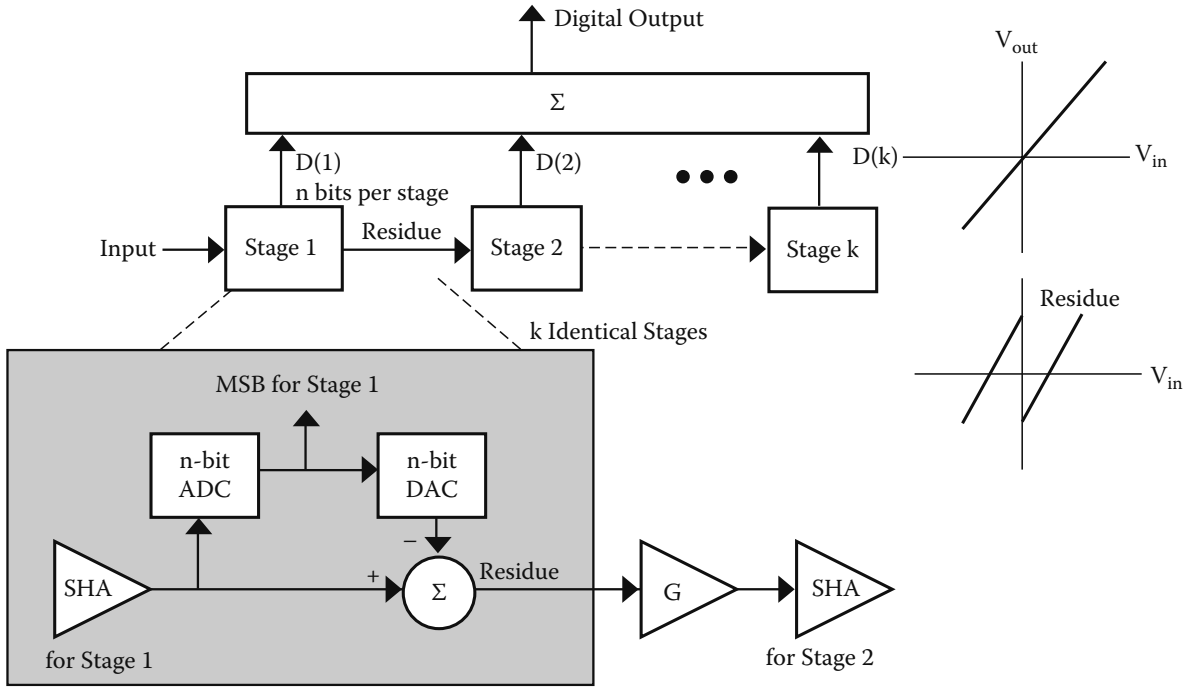


FIGURE 7-17 Pipeline ADC.

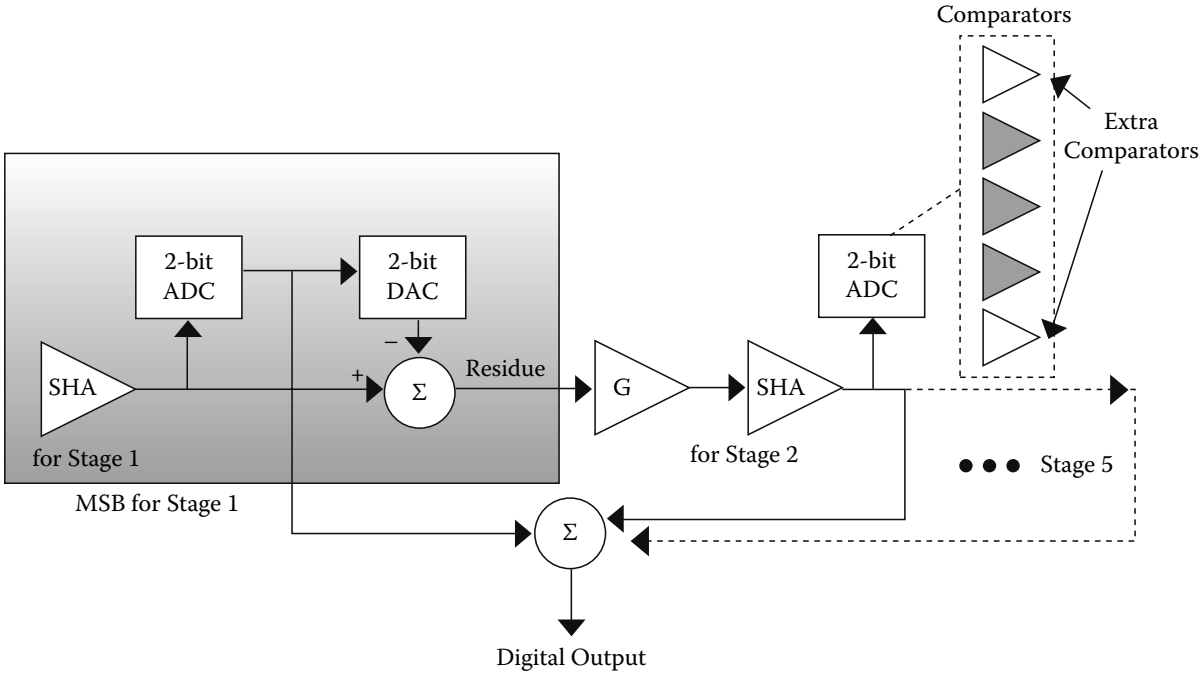


FIGURE 7-18 Ten-bit pipeline ADC with 2-bit-per-stage ADC and 1-bit redundancy.

Even though each pipeline stage only has to contribute n bits of the conversion result, its SHA must have enough dynamic range and bandwidth so that later stages can perform accurate conversions. Therefore, the SHA is often the limiting factor of a high-speed pipeline ADC. For example, a 10-bit pipeline ADC has five stages, each of which contributes two bits. The first stage samples and holds the analog input signal V_{in}, generates 2 bits of the digital output, converts the 2-bit digital signal into an analog signal, and subtracts it from the held output of the SHA. The difference (residue) is amplified and then processed by the next stage. In theory, amplification is unnecessary, although a larger signal level eases the subsequent operations. As the same process repeats for the subsequent stages, the resolution requirement is reduced by a factor of four for each stage. In the example, the first-stage SHA has to provide a resolution of 10 bits, the second-stage SHA only needs a resolution of 8 bits, etc.

The comparator offset in a pipeline can be corrected digitally. Assume that each stage is resolving 2 bits for a 10-bit pipeline ADC in Figure 7-18. In addition to the three comparators required for the conversion, two extra comparators can be added for each of the second to the fifth stages. The extra comparators detect any overflow level outside the nominal level set by the three main comparators. The ADC output can be digitally corrected by adding or subtracting (depending on the overflow direction) the detected error. In this example, a 1-bit redundancy is achieved by overlapping the ranges of neighboring (1st and 2nd, 2nd and 3rd) stages.

Instead of adding extra comparators as shown in Figure 7-18, another approach (see Figure 7-19) adds extra stages to perform digital calibration (Karanicolas, Lee, and Bacrania 1993). For instance, 12 stages can be used for a 10-bit pipeline ADC to provide two stages of redundancy.

With the offsets in comparators and preamps and the mismatches in capacitors, the residue deviates from ideal characteristics. The residue can be outside the nominal range, resulting in a missing decision level as shown in Figures 7-20(b) and (c). In order to ensure that the residue range is within the detection level, the gain (G) is reduced according to the amount of maximum mismatch and offset, as shown in Figure 7-20(d). The reduced gain is made up by the extra stages. The gain reduction prevents the missing decision levels but cannot deal with the missing codes. A calibration is performed digitally in each stage to recover the missing code (Karanicolas, Lee, and Bacrania 1993).

Another source of error is the nonlinearity of the SHA. In order to minimize the nonlinearity, a closed-loop op-amp is used in pipeline ADCs. However, the closed-loop amplifier has a higher

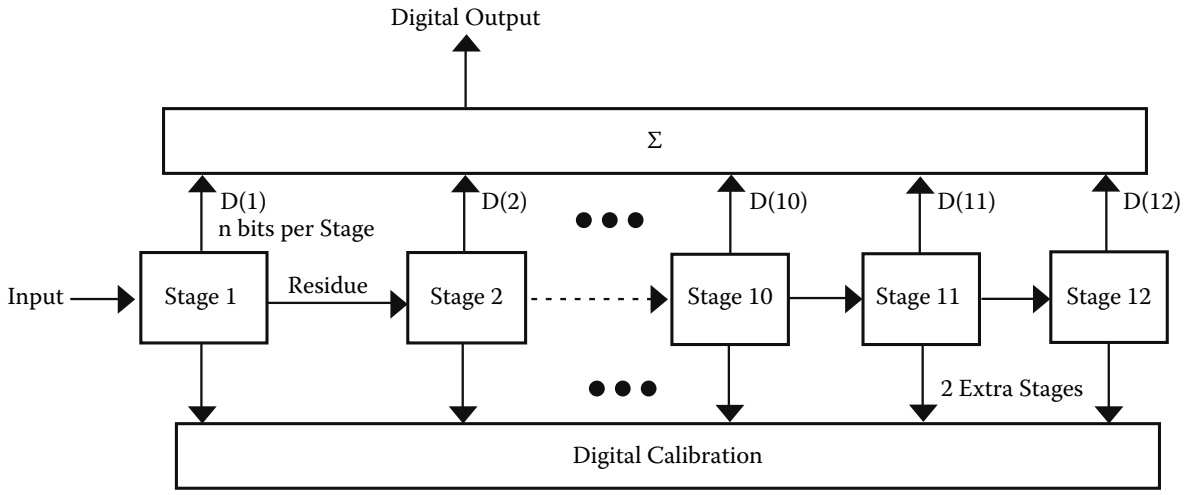


FIGURE 7-19 Ten-bit pipeline ADC with digital calibration.

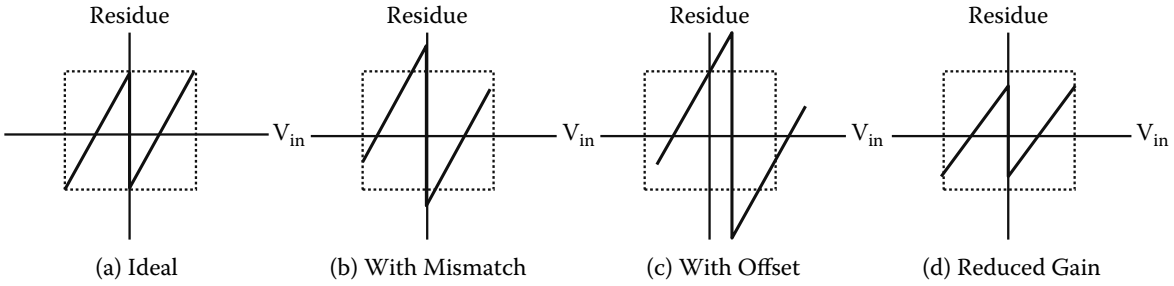


FIGURE 7-20 Residue characteristics.

noise and a smaller bandwidth, and consumes more power than does its open-loop counterpart. An open-loop amplifier can be used where error caused by the amplifier nonlinearity is corrected digitally (Murmann and Boser 2004). This technique is claimed to save a pipeline ADC power by 75% (Murmann and Boser 2004). Since this technique allows the use of an open-loop amplifier in a pipeline ADC, the sampling rate can also improve.

7.7 POWER DISSIPATION ISSUES IN HIGH-SPEED ADCS

It is very difficult to compare power-dissipation performance of high-speed ADCs. Power dissipation depends strongly on the architecture and device technology used. For a given architecture, the power dissipation increases linearly with a sampling rate (if $f_s \ll f_T$). In flash ADCs, as the number of resolution bits N increases, the required power increases at a faster rate than 2^N because the offset voltages must be reduced. In pipeline ADCs, the power increases nonlinearly depending on the number of bits per stage and the digital correction circuitry (Lewis 1992).

In CMOS, the sample-and-hold and gain stages can be combined into a single circuit to save power. Also, low-power CMOS digital circuits can correct for offsets, mismatches, gain errors, and nonlinearity. Such techniques cannot be readily applied to the III-V technologies, which must use very large devices to reduce the offset (since III-V transistors have much higher offset than Si and digital offset cancellation is not readily available). Clearly one must choose a device technology that can take advantage of power-reduction schemes (power-efficient architectures and digital correction circuits).

7.8 SUMMARY

This chapter introduced the performance metrics used to characterize ADCs. The development trends of ADC technology were discussed. The design issues and performance deciding factors of

flash and pipeline ADCs were presented. Since digital circuit performance improves at a rate much faster than analog circuit performance, it is expected that increasingly more digital techniques will be applied to improve the performance of ADC circuits.

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