EE 4490 Project #1 Assignment

Tentative due date: October 16, 11:59pm

Purpose: Gain familiarity with using Verilog and Xilinx Vivado to implement a timing-critical serial communications project using the Digilent Basys 3 FPGA board.

Procedure: Your task is to design, simulate and test in hardware (on the Digilent Basys 3 FPGA prototyping board) a "Device" which displays variable color patterns on a string of five (5) WS2812B GRB LEDs in the following manner. The possible score range shown below for your project is associated with the difficulty of the requirements that your design meets.

The pattern of how the GRB LEDs change is entirely up to you. The sophistication and inventiveness of your design will have some impact on the score awarded for your project. You may also choose to utilize other user-interface display elements on the Basys 3 board (for example, the seven-segment displays and the 16 individual green LEDs), depending upon the needs of your "Device".

- If your project just simply turns on one to five LEDs but does nothing to change their color beyond the capabilities provided in the SimpleSend example project, your team will be awarded a score in the vicinity of 50%.
- If your project animates the color display, for example by providing a controllable timing loop to automatically vary the color of the GRB LEDs, your team will be awarded a score in the vicinity of 70-85%.
- If your project utilizes additional inputs and interacts with the user when enabled by moving a singularly colored LED "sprite" across the sequence of GRB LEDs (for example, a user press of the left button causes the "sprite" to move to the left while a user press of the right button causes the "sprite" to move to the right), your team will be awarded a score in the vicinity of 80-95%.
- If your project implements an "interactive game" between the Basys 3 and the human user, where a clear goal is described in the one-page written description listed below, a score is maintained and displayed in some way, and the game terminates with an understood "win" or "loss" score, your team will be awarded a score in the vicinity of 90-100%.

There is an intentional overlap in the score ranges listed above, to account for variations in the quality of the design and the accompanying documentation.

Turn in: For this Project, turn in electronically (as one zip-file attachment) the following items. You may upload the zip file on WyoCourses. The zip file must contain:

1. A one-page written description of the functionality to be provided by your design, as a stand-alone PDF file. That is, explain in layman's terms (i.e., in language that does not require an education in electrical or computer engineering) specifically what your "Device" does.

2. A 2-4 page technical description of your modular implementation of the "Device", as a separate, stand-alone PDF file. This description should include the following:

- An "RTL Schematic" of the top-level design of your implementation.

- An inventory (tabular list, for example) of the Basys 3 user-interface resources which are utilized by your design. For example, which switches, buttons and Basys 3 LEDs are utilized for what user-interface functionality, and what Basys 3 PMOD port usage will be required to connect to the WS2812B LED strip.
- A brief description of the functionality of the individual Verilog modules (that is, from a black-box sense, what functionality each module provides). Feel free to include ASM charts for one or more modules (as an appendix that doesn't count against the page limit) to document the operation of your FSMs, if you feel it helps convey the desired information.

3. Your zip file must also include the following (in a separate folder within the zip file):

- All Verilog source files (filename extension .v) utilized in the implementation of your project. You should also include any test benches and simulation results to demonstrate the desired behavior of your appropriate modules.
- The Xilinx Vivado design constraints file (filename extension .xdc) utilized by your project.
- The bitstream file (filename extension .bit) produced by Vivado to program the FPGA.

4. Finally, to visually show how your project works, submit a brief video file (in a standard file format such as .mp4) that demonstrates your project in operation. At the beginning of the video, identify you and your team member to show that it's your design. Don't go overboard with this and be careful of file size! File size of 10-20MB is preferred, and file size larger than that is discouraged.

These specific files (and ONLY THESE FILES, no other content) should be placed in a zipped archive file with the following name:

EE4490_Proj01_Lastname1_Lastname2.zip

The two students for the team should substitute their last names in the obvious two positions of the file name. Note that the separators in the filename are underscore characters, not spaces.

You are free to create the written documents described above using any program, such as LaTeX, Microsoft Word, etc., but the file you submit must be a valid PDF file, having a page size of 8.5 x 10 inches, with approximately 1-inch margins all around, and with the main body font size no smaller than 10 points (12 points is preferred). The writing style should be serious yet also brief, clear, and concise.