

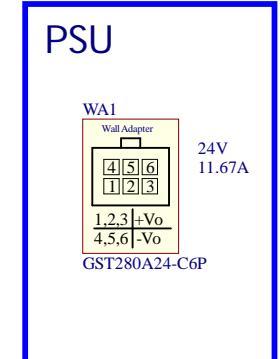
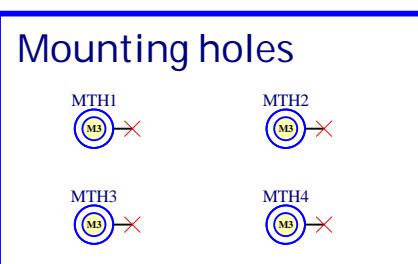
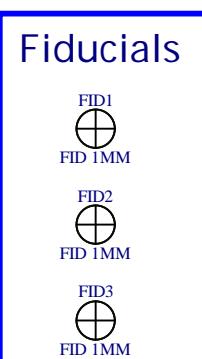
P07

Radio reconfigurable

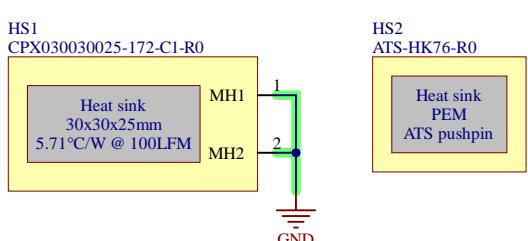
Ultracom

Revision 1.000

Date: 2021-01-13



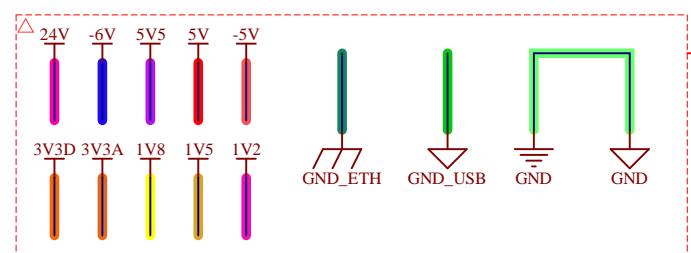
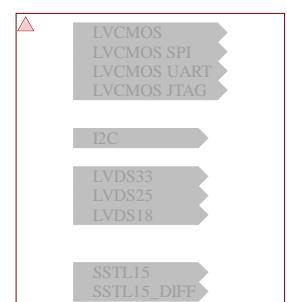
Heat sink



Rth HS = 5.71 °C @ 100LFM
RJC = 4 °C/W
Rth interface = 0.5°C/W
[http://vendor.parker.com/852568C80043FA7A/468ea5de5ac341d385257d39005641c7/1BD00D0D0B1B018C852569580073DD53/\\$FILE/THERMATTA CH-TAPES-THERM-CAT.pdf](http://vendor.parker.com/852568C80043FA7A/468ea5de5ac341d385257d39005641c7/1BD00D0D0B1B018C852569580073DD53/$FILE/THERMATTA CH-TAPES-THERM-CAT.pdf)

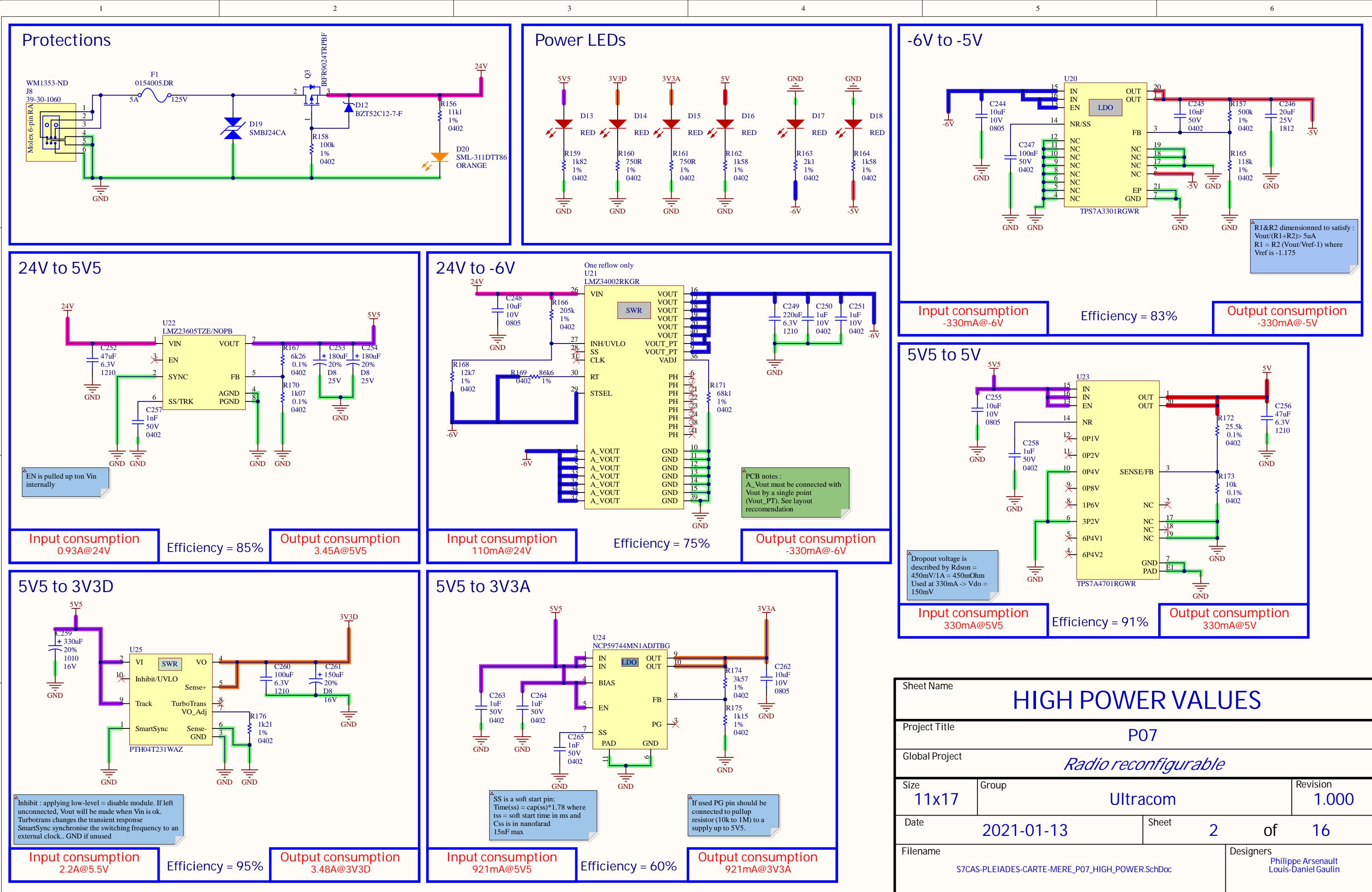
Revision history	

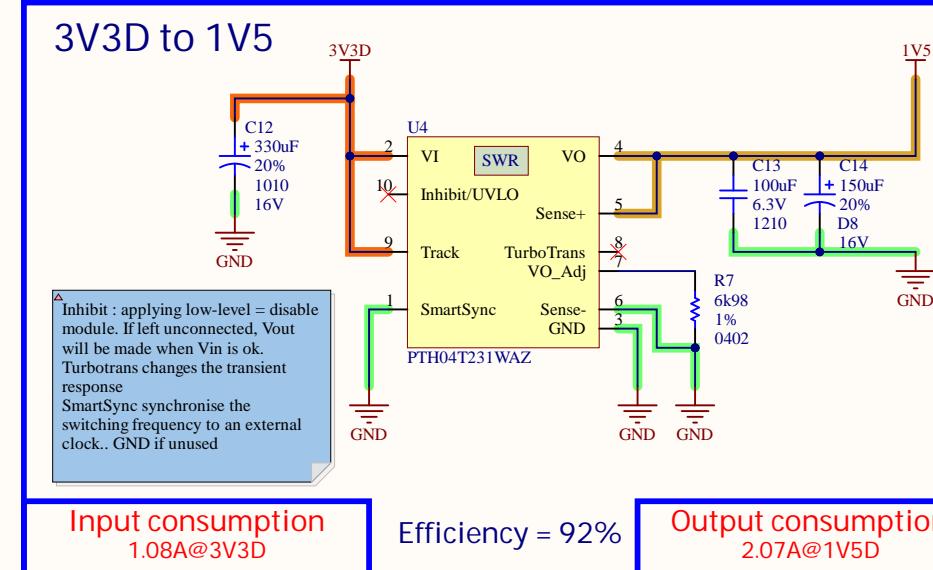
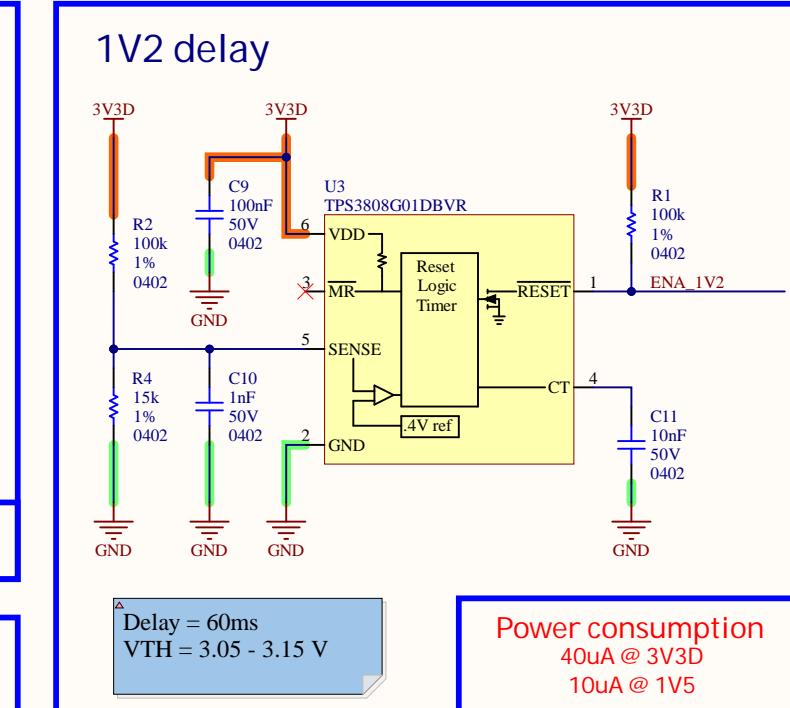
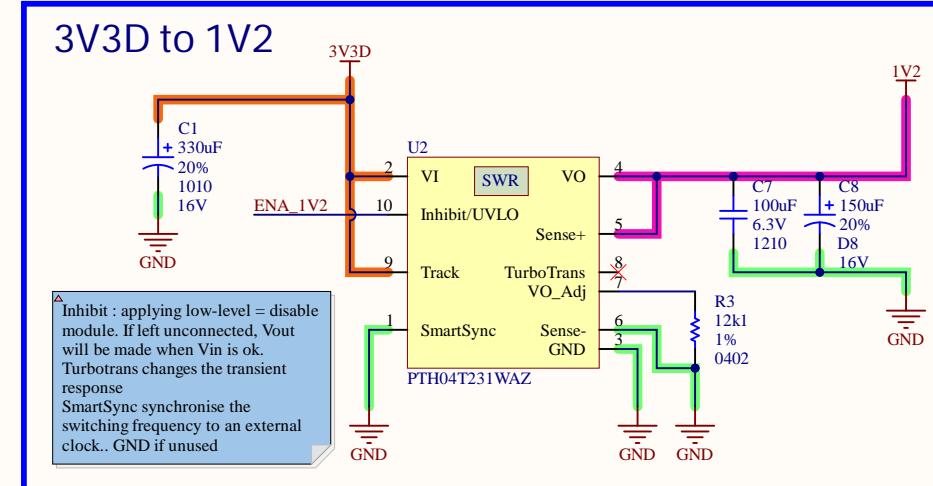
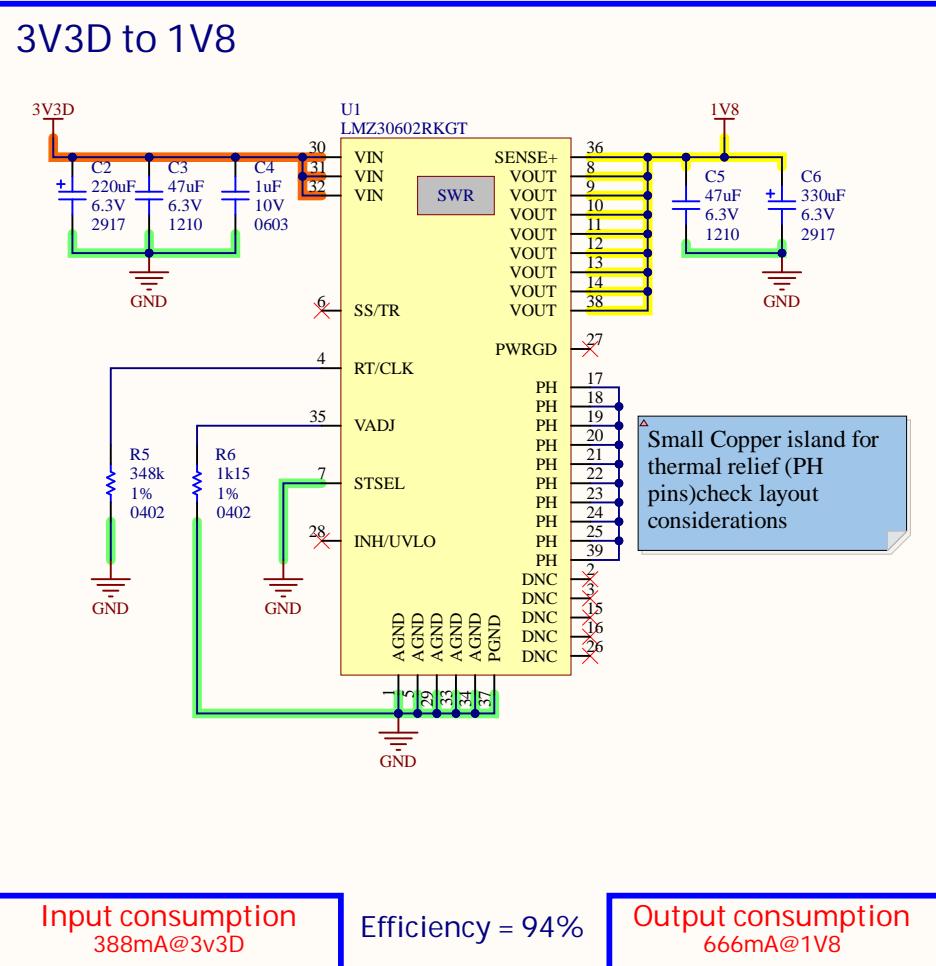
Package size conversion	
Metric	Imperial
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512



Design notes:
Analog ground (arrow) and signal GND (normal power net) are connected together.
PCB NOTE: Segregate currents return between AGND and GND

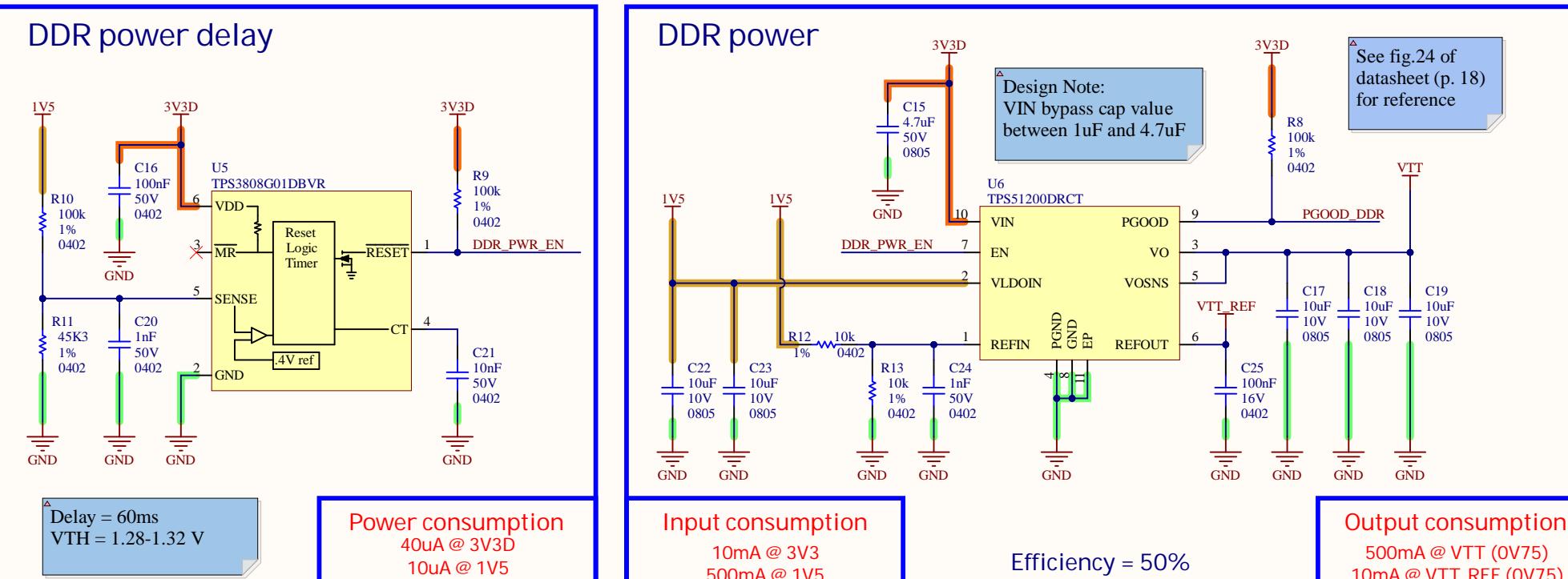
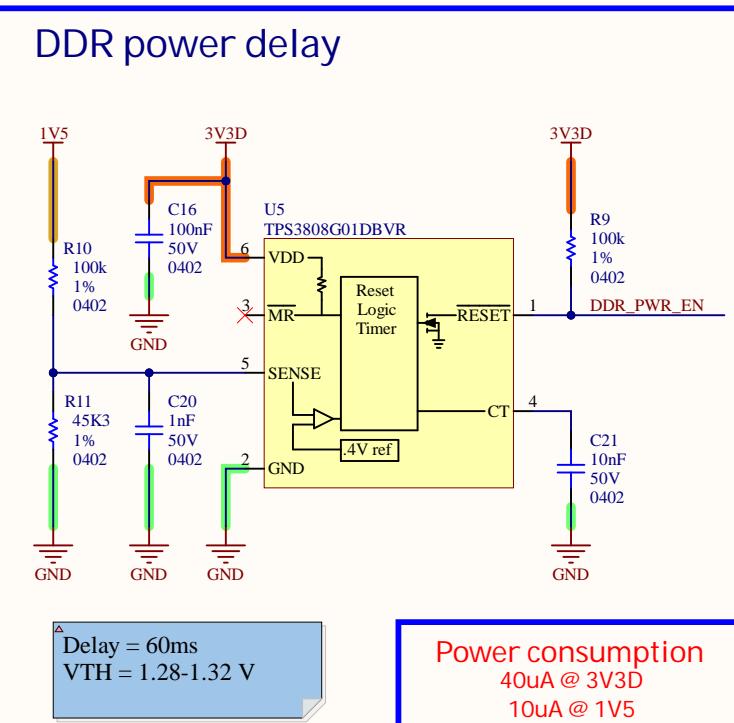
Project Title	P07		
Global Project	Radio reconfigurable		
Size	11x17	Group	Revision 1.000
Date	2021-01-13	Sheet	1 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_TITLE.SchDoc		
Designers	Philippe Arsenault Louis-Daniel Gaulin		





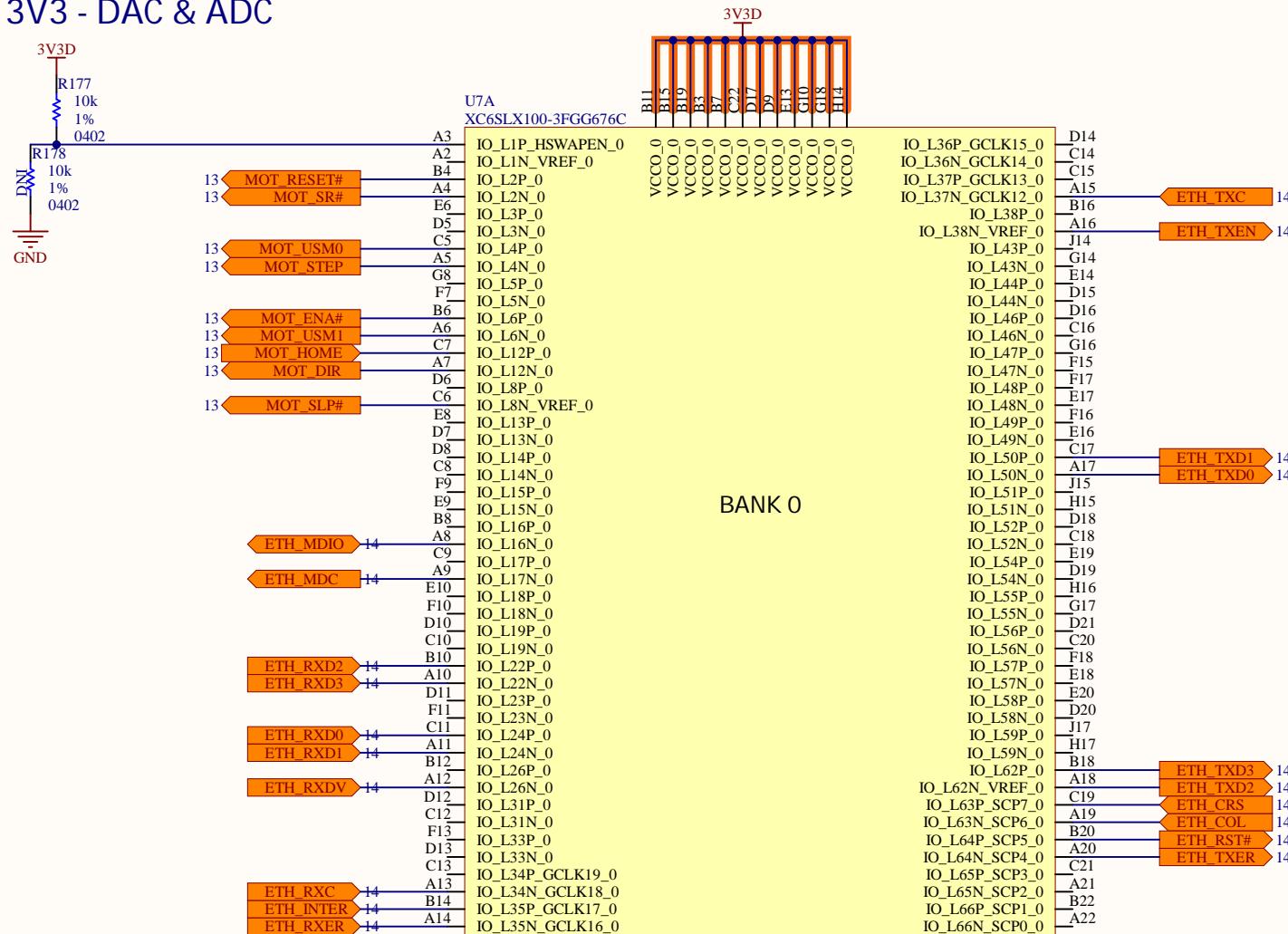
If used PG pin should be connected to pullup resistor (10k to 1M) to a supply up to 5V5.

Only constraint of power-on sequence :
VTT (0.75V) must come after 1V5 -> 1V5 is used to make VTT
The FPGA core (1V2) must come after the flash (3V3D) -> 3V3D is used to make 1V2D
Furthermore, the PTH04T230W has a soft start feature.

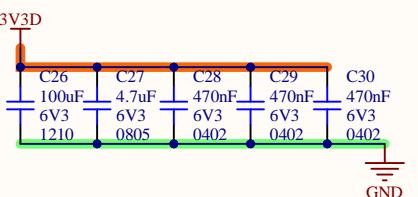


Sheet Name	LOW VALUE POWER		
Project Title	P07		
Global Project	<i>Radio reconfigurable</i>		
Size	11x17	Group	Revision
Date	2021-01-13	Sheet	3 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_LOW_POWER.SchDoc		
Designers	Philippe Arsenault Louis-Daniel Gaulin		

Bank 0 - 3V3 - DAC & ADC

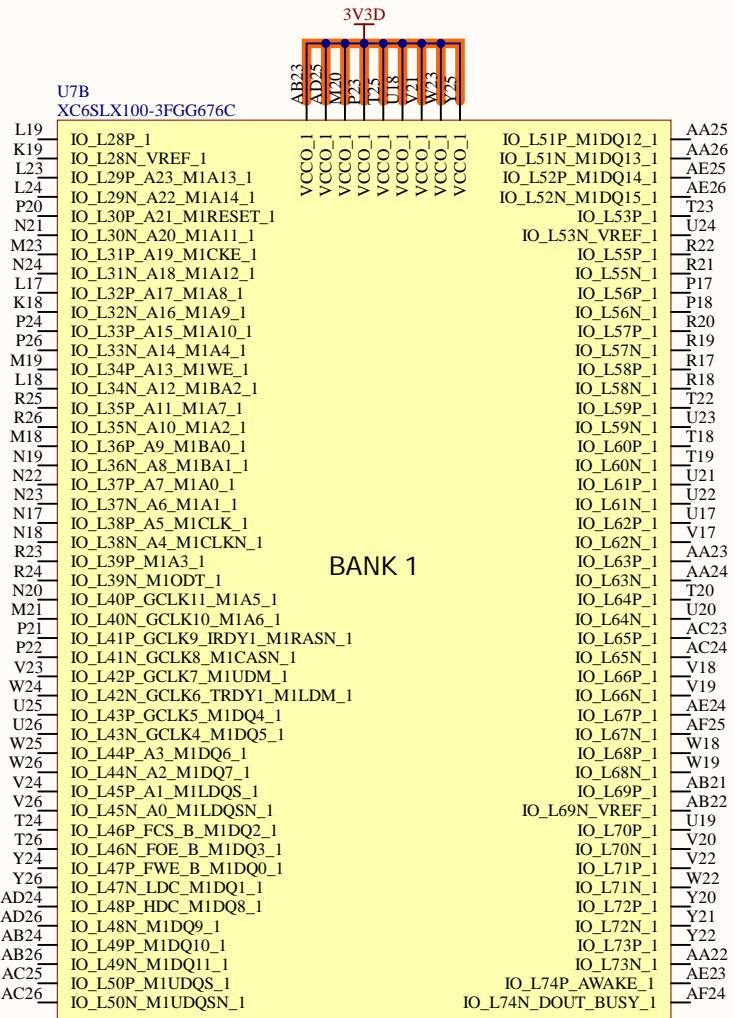


FPGA Bank 0 Decoupling Capacitors



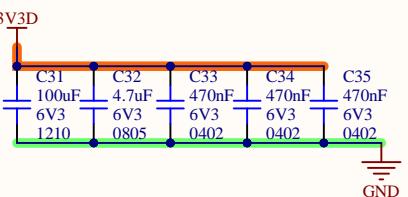
Sheet Name		FPGA_O	
Project Title		P07	
Global Project		<i>Radio reconfigurable</i>	
Size	Group	Revision	1.000
11x17	Ultracom		
Date	2021-01-13	Sheet	4 of 16
Filename		Designers Philippe Arsenault Louis-Daniel Gaulin	
S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_O.SchDoc			

Bank 1 - 3V3 - Unused



Current consumption

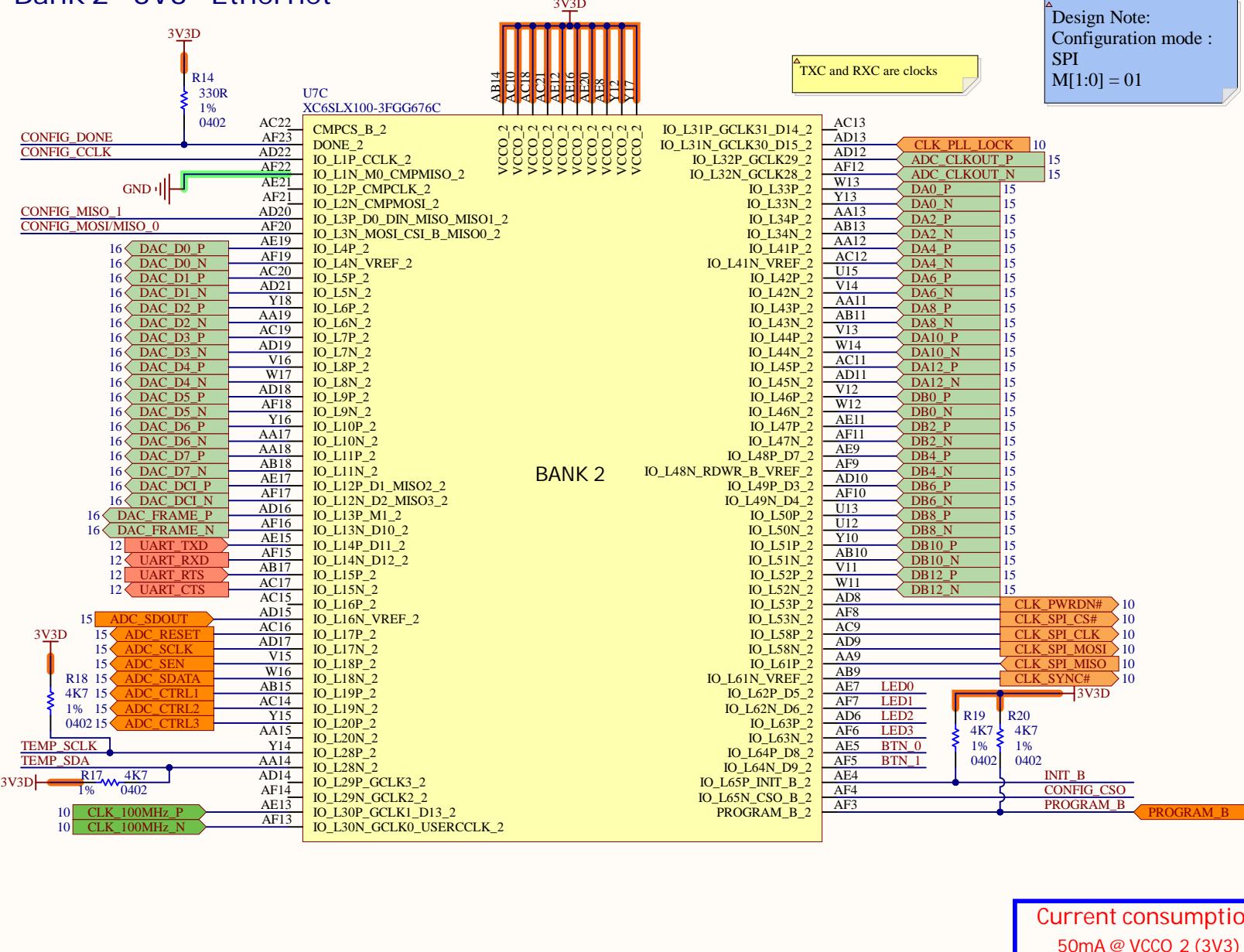
FPGA Bank 1 Decoupling Capacitors



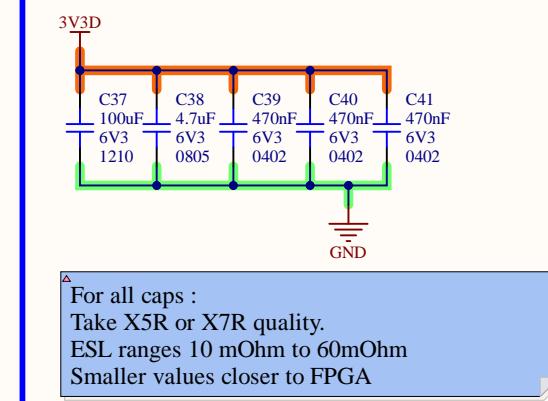
- △ Design notes:
 - For all caps :
 - Take X5R or X7R quality.
 - ESL ranges 10 mOhm to 60mOhm
 - Smaller values closer to FPGA

Sheet Name	FPGA_1		
Project Title	P07		
Global Project	<i>Radio reconfigurable</i>		
Size 11x17	Group Ultracom	Revision 1.000	
Date 2021-01-13	Sheet 5	of 16	
Filename S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_1.SchDoc	Designers Philippe Arsenault Louis-Daniel Gaulin		

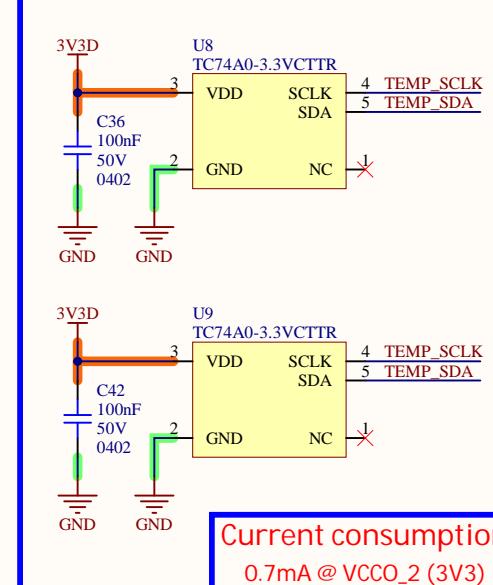
Bank 2 - 3V3 - Ethernet



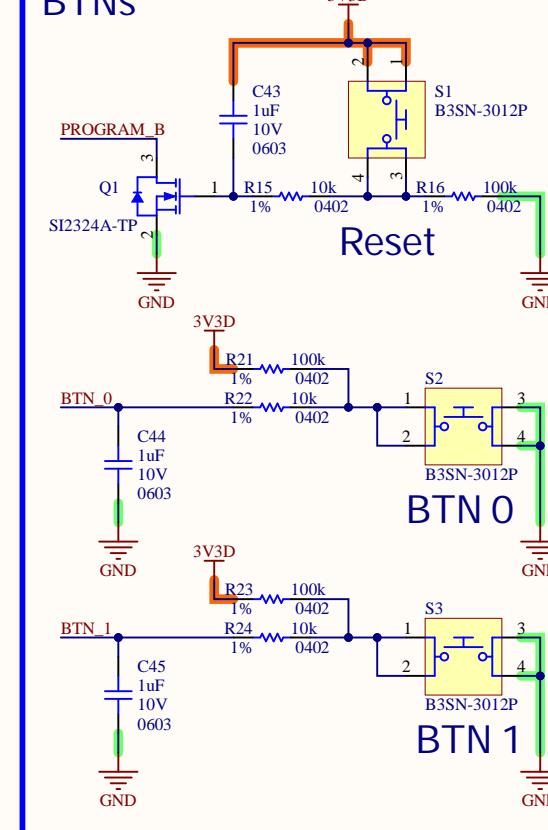
FPGA Bank 2 Decoupling Capacitors



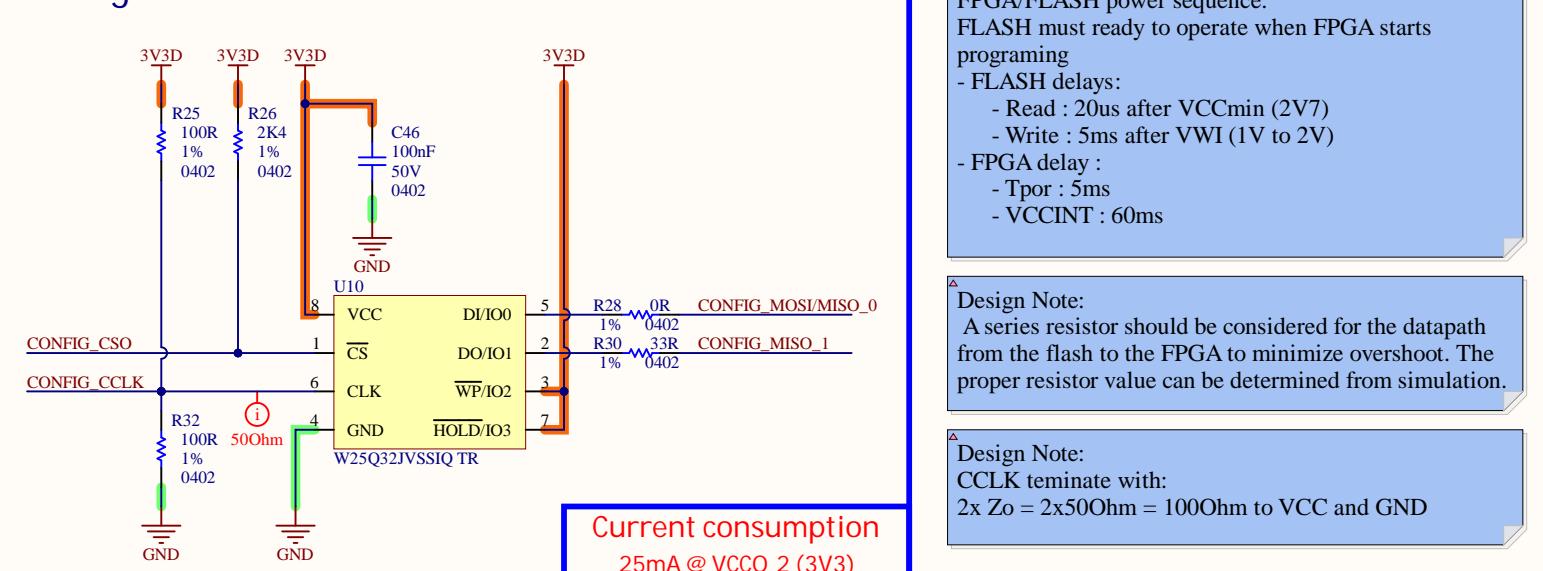
Temperature sensors



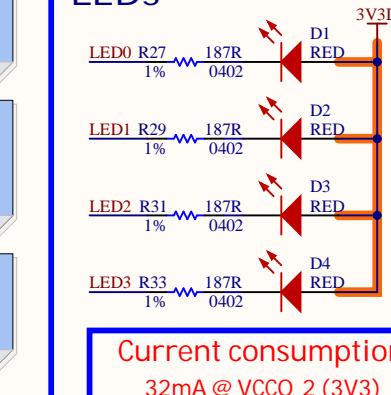
BTNs



Configuration FLASH



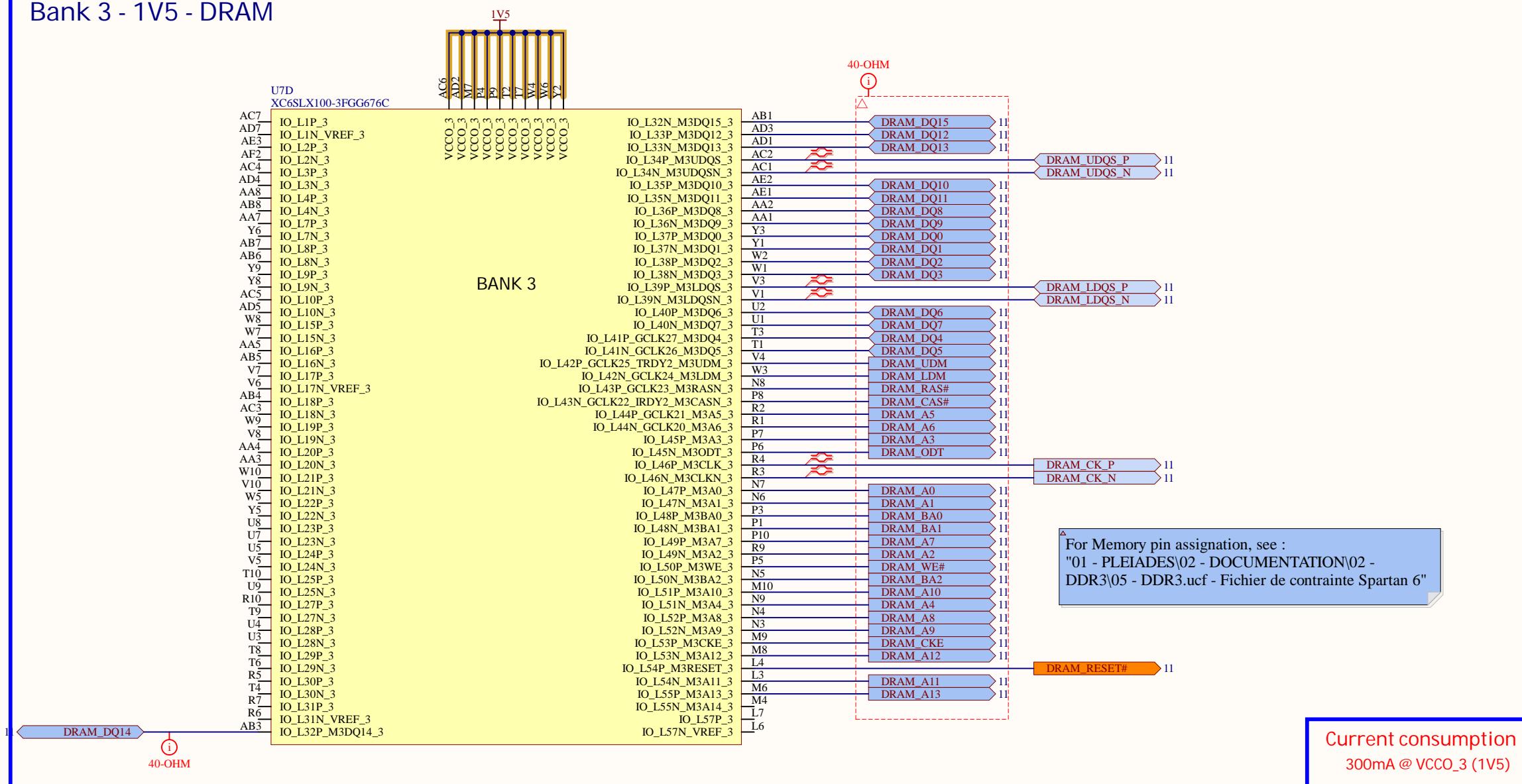
LEDs



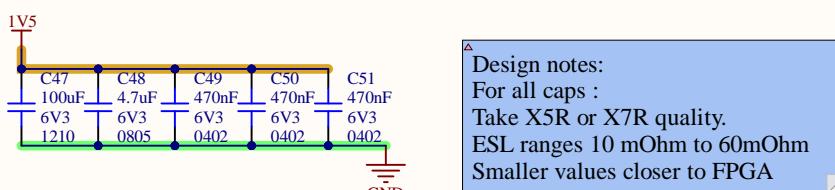
Sheet Name

FPGA_2	
Project Title	P07
Global Project	Radio reconfigurable
Size	11x17
Group	Ultracom
Date	2021-01-13
Sheet	6 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_2.SchDoc
Designers	Philippe Arsenault Louis-Daniel Gaulin

Bank 3 - 1V5 - DRAM

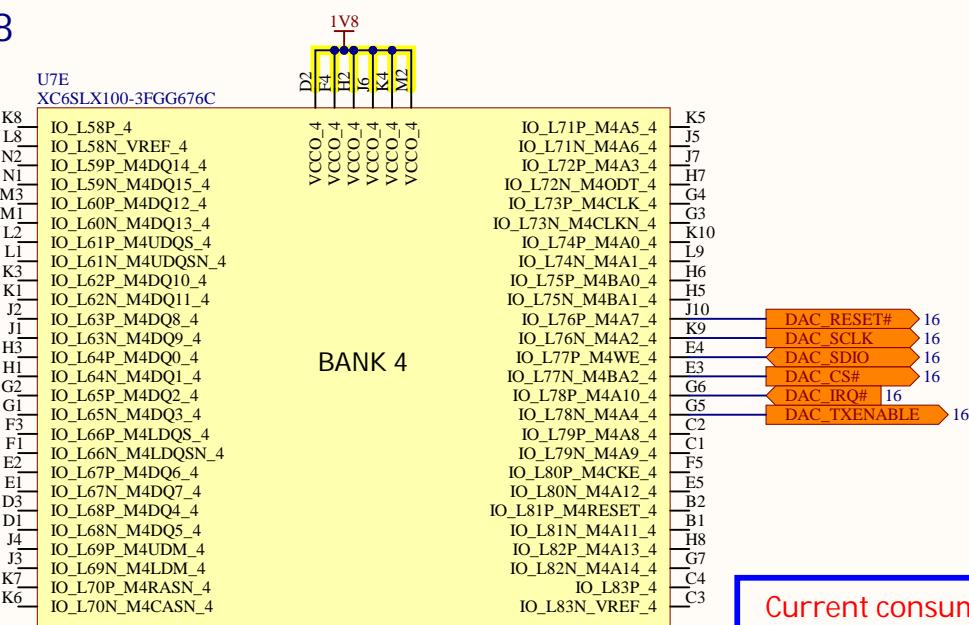


FPGA Bank 3 Decoupling Capacitors

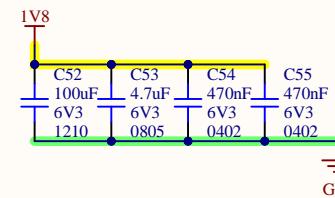


Sheet Name		FPGA_3	
Project Title		P07	
Global Project		Radio reconfigurable	
Size	Group	11x17	Revision
11x17	Ultracom	1.000	
Date	2021-01-13	Sheet	7 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_3.SchDoc		Designers
Philippe Arsenault Louis-Daniel Gaulin			

Bank 4 - 1V8

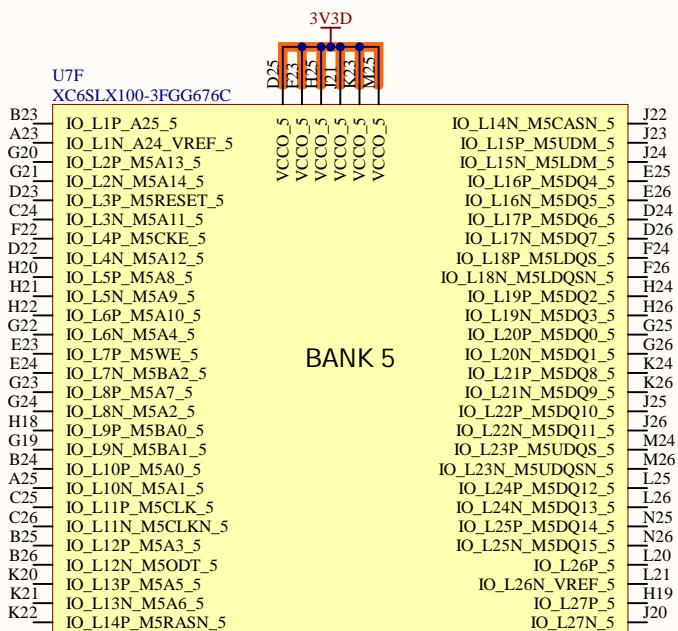


FPGA Bank 4 Decoupling Capacitors

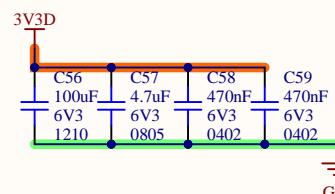


Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Bank 5 - 3V3 (Unused)



FPGA Bank 5 Decoupling Capacitors



Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Sheet Name

FPGA_4

Project Title

P07

Global Project

Radio reconfigurable

Size

11x17

Group

Ultracom

Revision

1.000

Date

2021-01-13

Sheet

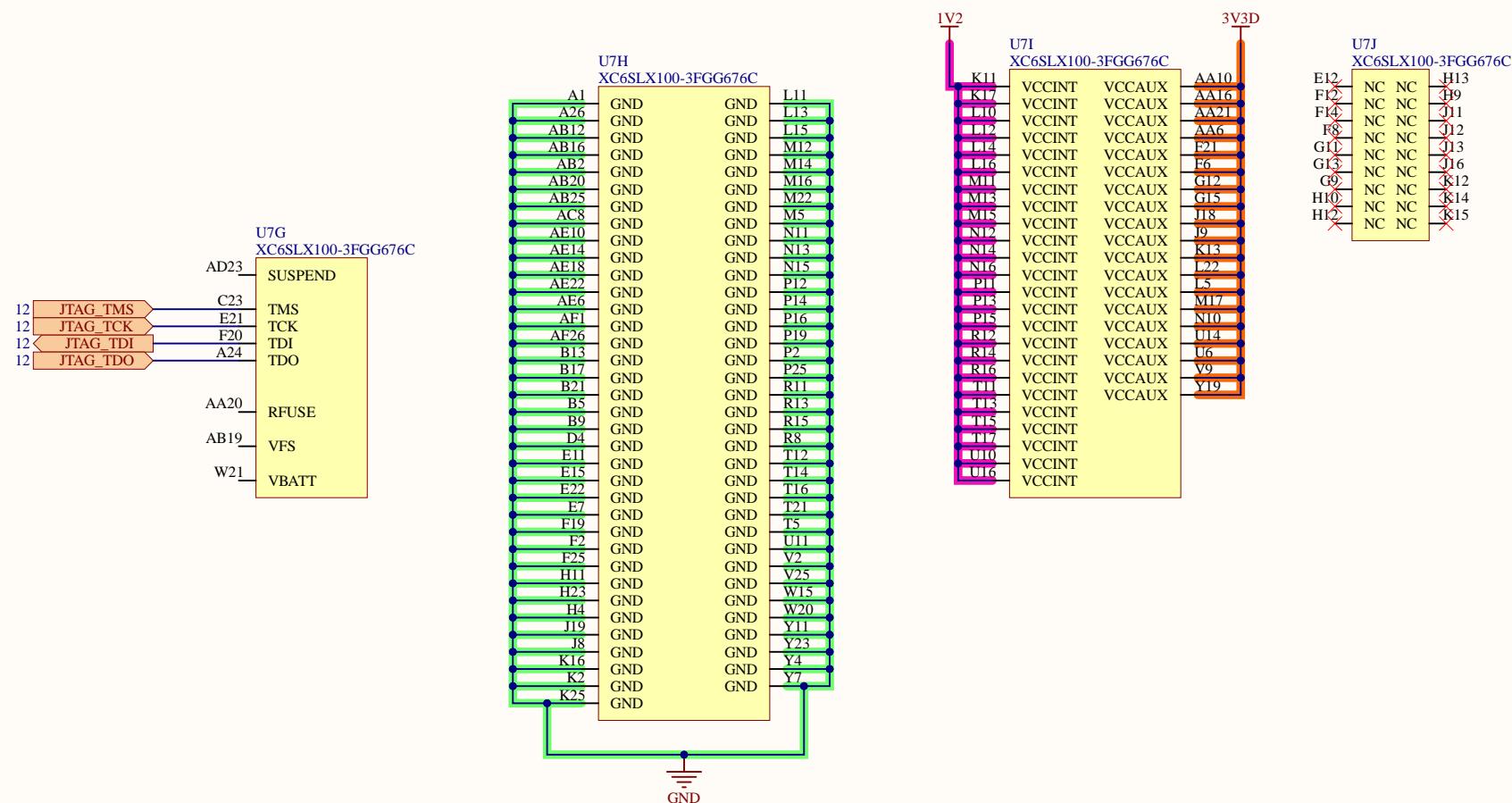
8 of 16

Filename

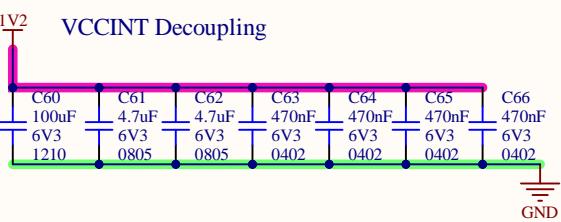
S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_4-5.SchDoc

Designers
Philippe Arsenault
Louis-Daniel Gaulin

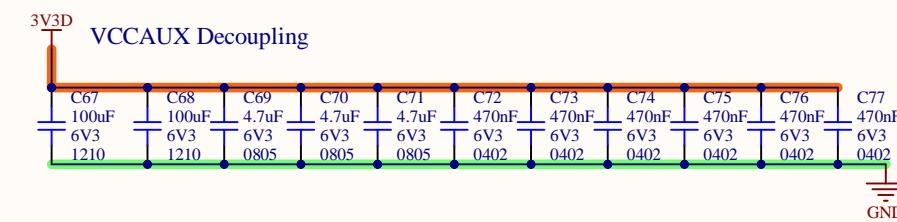
A FPGA Power Parts



D FPGA Decoupling Capacitors

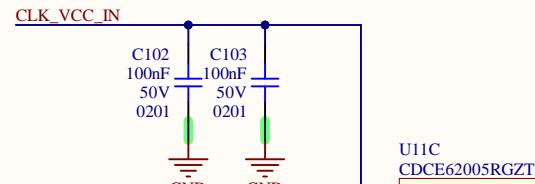
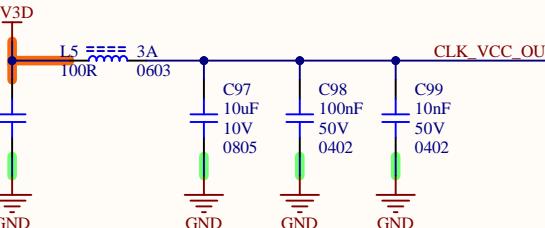
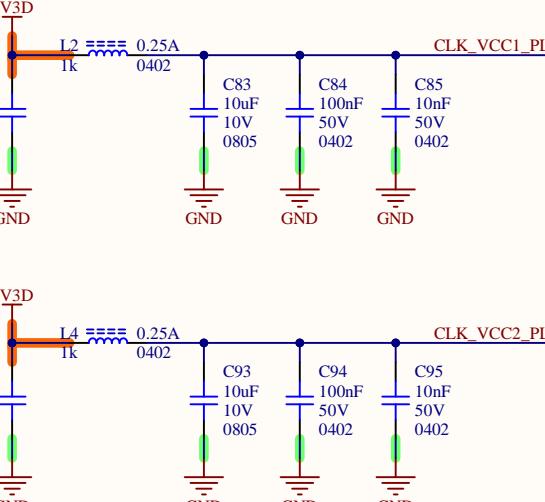
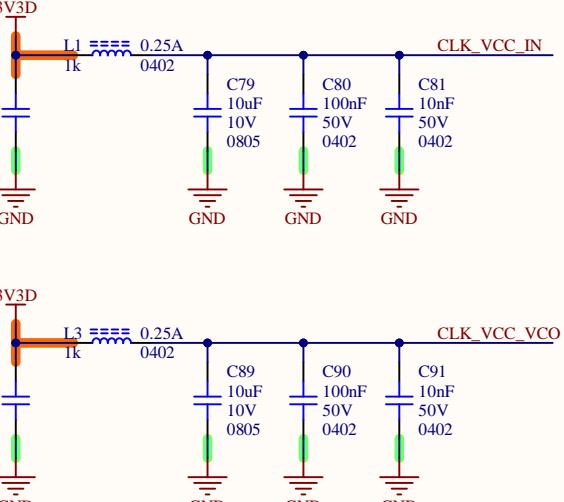


Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to
60mOhm
Smaller values closer to
FPGA

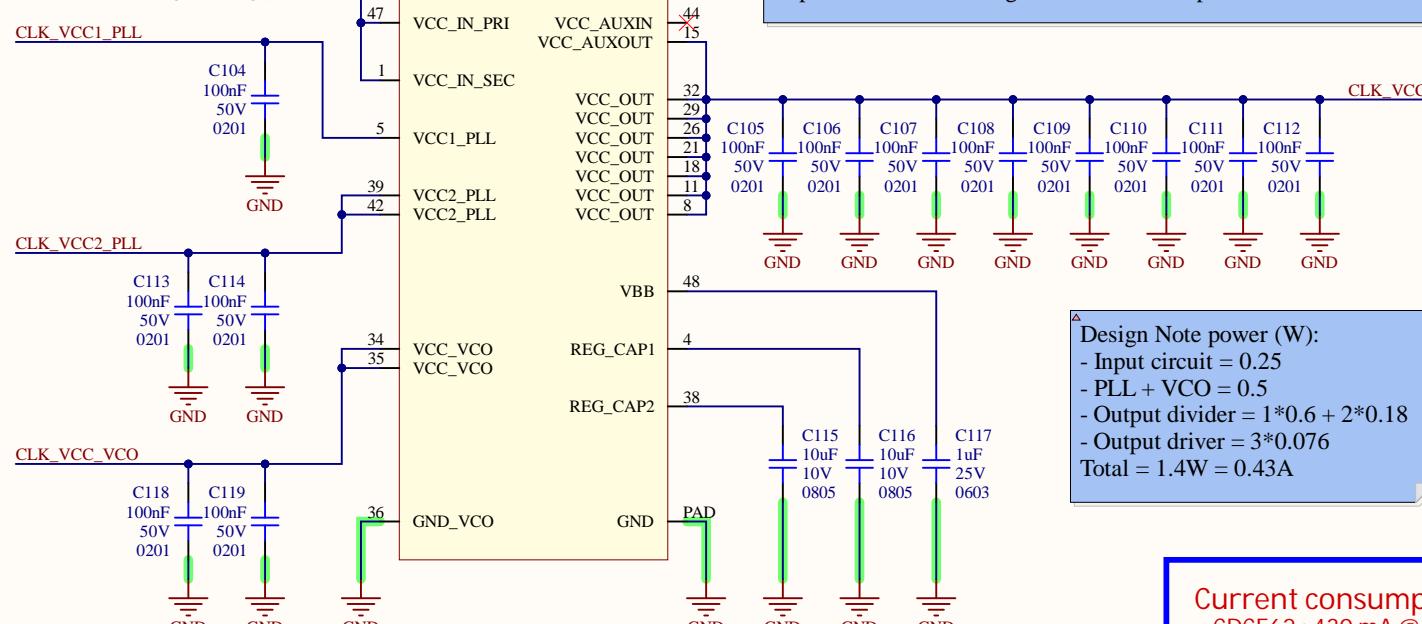


Sheet Name		FPGA_MISC	
Project Title		P07	
Global Project		<i>Radio reconfigurable</i>	
Size	Group	Revision	
11x17		1.000	
Date	2021-01-13	Sheet	9 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_MISC.SchDoc		Designers Philippe Arsenault Louis-Daniel Gaulin

Clock power

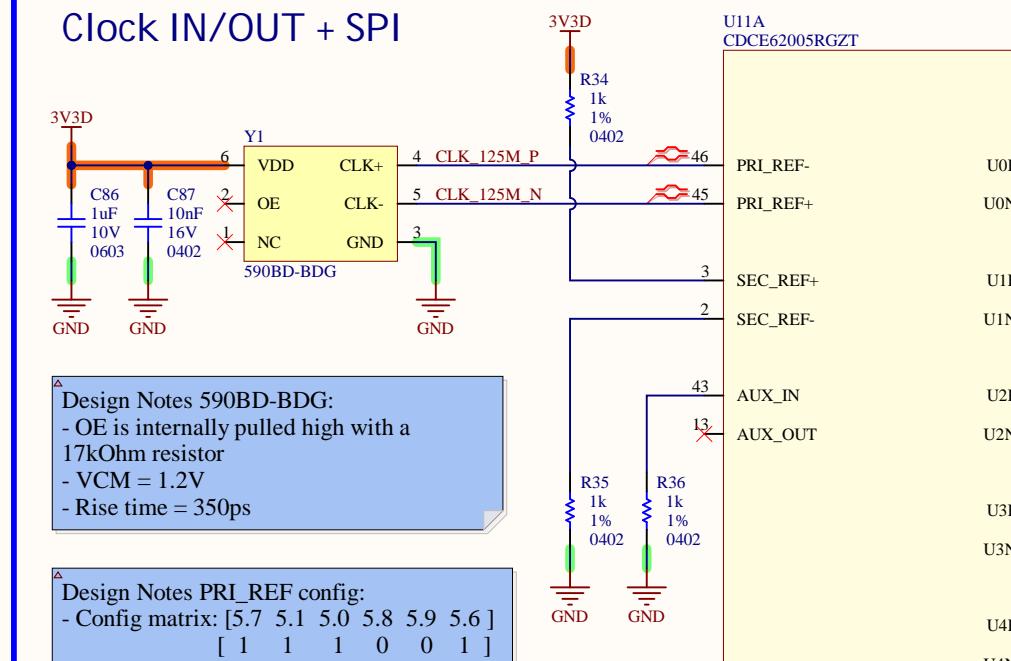


Design Note:
 - X5R or X7R are required for VBB, REG_CAP1 & RAG_CAP2
 - VCC_AUX is not used and can be left unconnected
 - Decoupling reference :
<https://www.ti.com/lit/an/scaa096/scaa096.pdf?ts=1612186266989+>
<https://www.ti.com/lit/ug/scau024/scau024.pdf?ts=1612185556858>



Current consumption
 CDCE62 : 430 mA @ 3V3
 SI590 : 100 mA @ 3V3

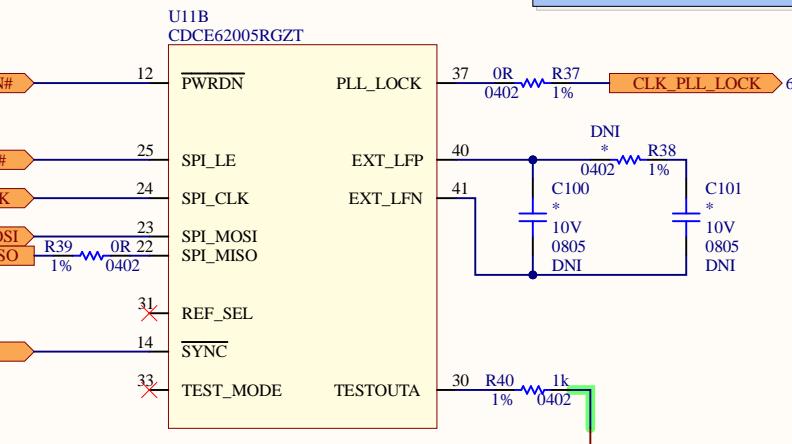
Clock IN/OUT + SPI



Design Notes 590BD-BDG:
 - OE is internally pulled high with a 17kOhm resistor
 - VCM = 1.2V
 - Rise time = 350ps

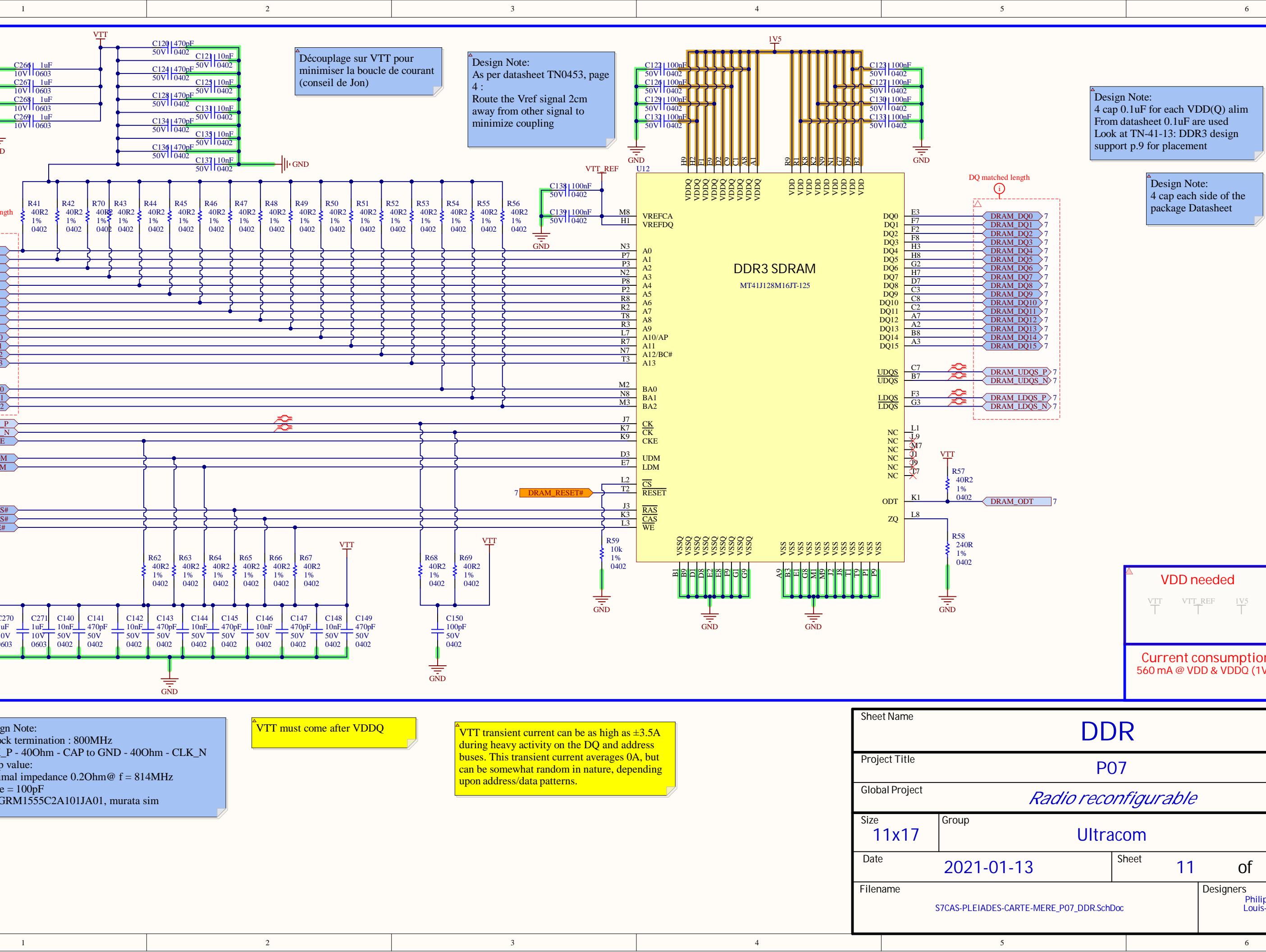
Design Notes PRI_REF config:
 - Config matrix: [5.7 5.1 5.0 5.8 5.9 5.6]
 [1 1 1 0 0 1]
 - > Hysteresis, LVDS, DC coupling, Internal term , Vbb = 1.2V
 - Internally terminated, no external needed
 - [6.25 6.24] = [X 0] to disable AUX_OUT

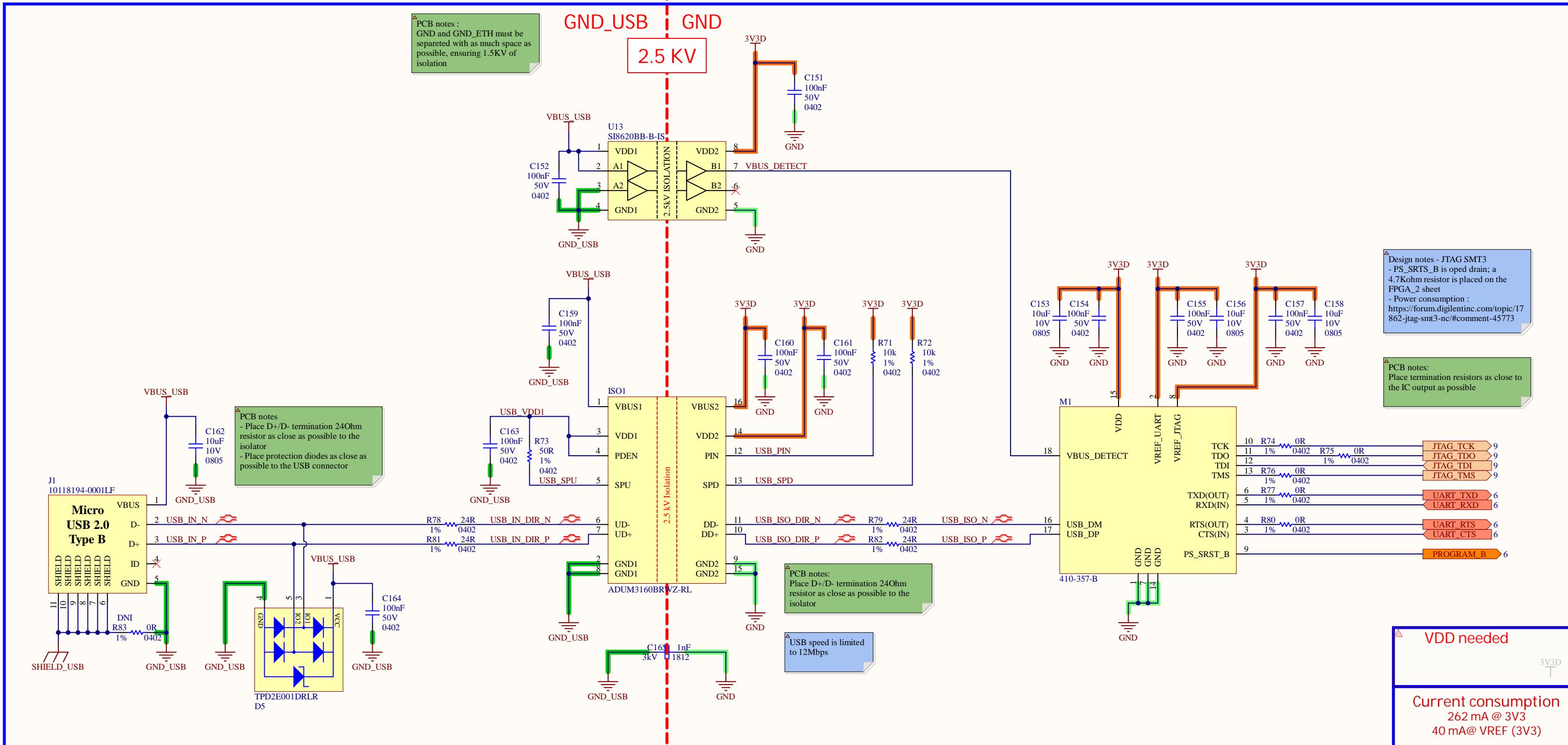
Design Note:
 - REF_SEL ([1] = PRI ; [0] = SEC) is internally pulled up (150kOhm)
 - SYNC# is internally pulled up (150kOhm)
 - PWRDN# is internally pulled up (150kOhm)
 - SPI LE must be high to load the EEPROM during rising edge of PWRDN#



The PLL external loop bandwidth set is recommended for dirty clock. The clock we use is considered as clean enough and components are not installed normally

Sheet Name		Clock	
Project Title		P07	
Global Project		Radio reconfigurable	
Size	Group	Ultracom	
11x17		Revision 1.000	
Date	2021-01-13	Sheet	10 of 16
Filename			Designers
S7CAS-PLEIADES-CARTE-MERE_P07_CLOCK.SchDoc			Philippe Arsenault Louis-Daniel Gaulin



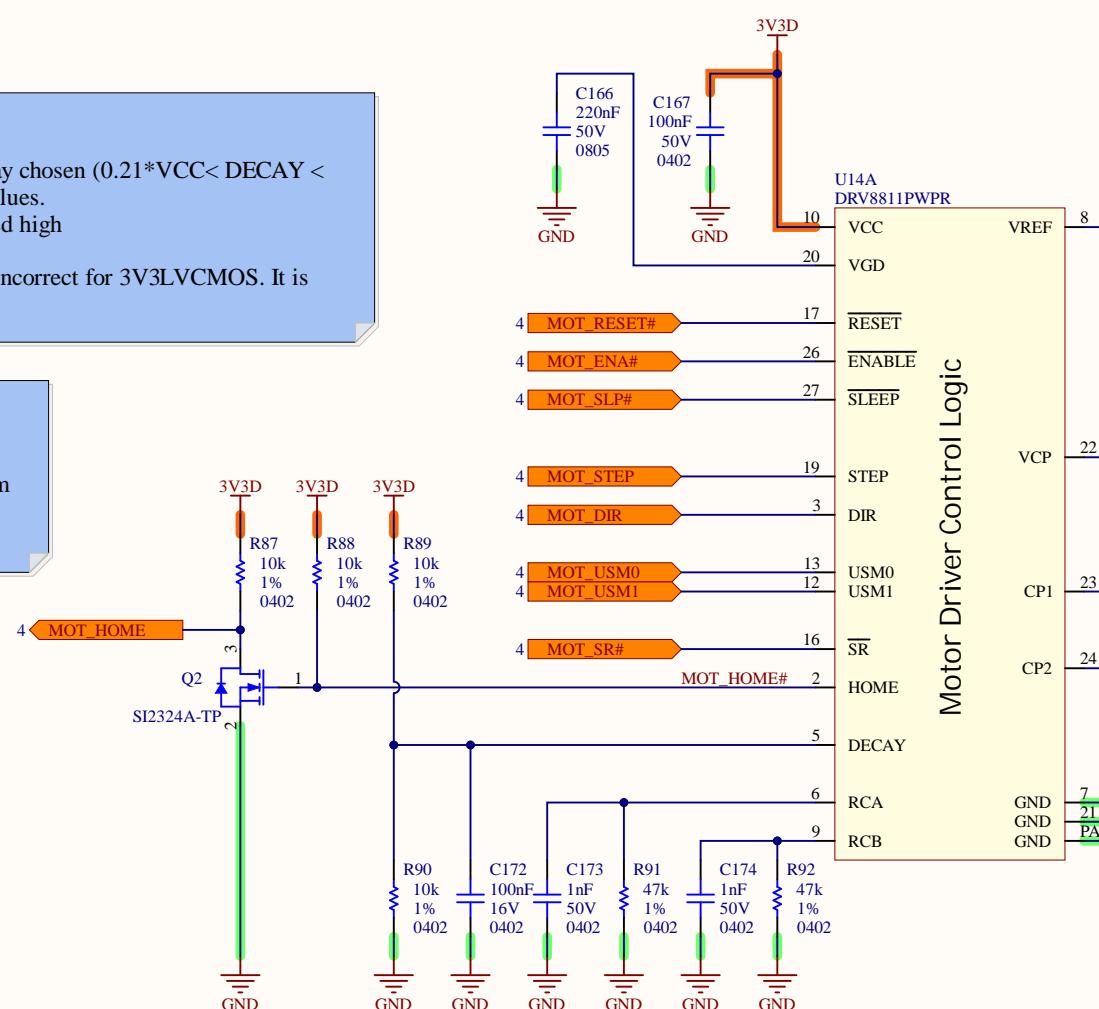


Sheet Name:	USB	
Project Title:	P07	
Global Project:	<i>Radio reconfigurable</i>	
Size: 11x17	Group: Ultracom	Revision: 1.000
Date: 2021-01-13	Sheet: 12 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_USB.SchDoc		Designers: Philippe Arsenault, Louis-Daniel Gaulin

Motor driver

- Design notes - DRV8811:
 - VCC = 3 to 5.5V
 - No decay mode specified. Mixed decay chosen ($0.21 \times VCC < DECAY < 0.6 \times VCC$) with common application values.
 - RESET# & ENA# are internally pulled high
 - All other inputs are pulled low
 - MOT_HOME's logic levels could be incorrect for 3V3LVC MOS. It is therefore inverted and redriven

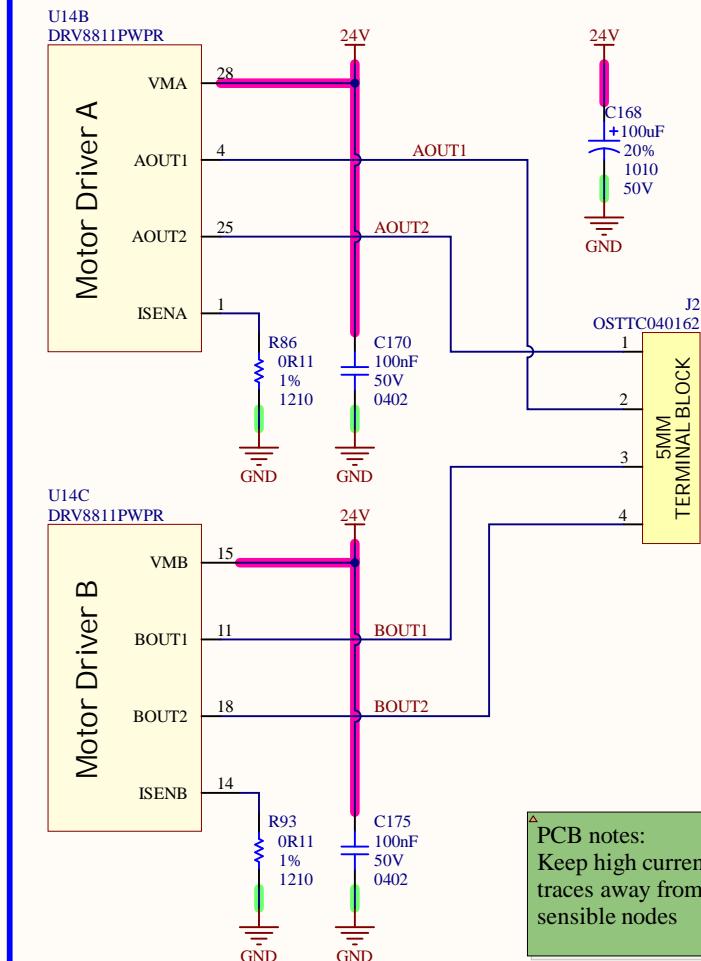
Design notes DRV8811 - ISENSE:
Current (per winding) = 1.9A
 $1.9A = Vref / (8 * Rsense)$
 $Rsense = 1.65V / (8 * 1.9A) = 108mOhm$
Rsense actual = 110mOhm
Imax actual = 1.875A



Current consumption

4MA @ VCC (5V)

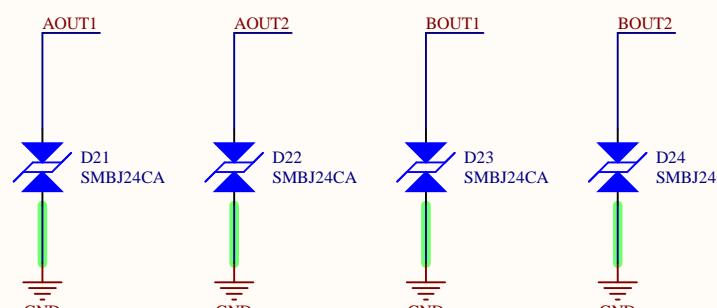
Drive power output + bulk capacitors



► PCB notes:
Keep high current
traces away from
sensible nodes

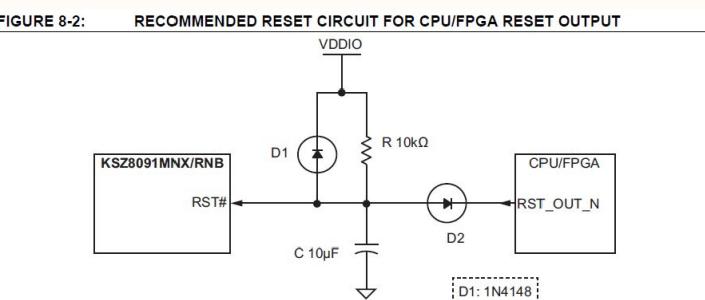
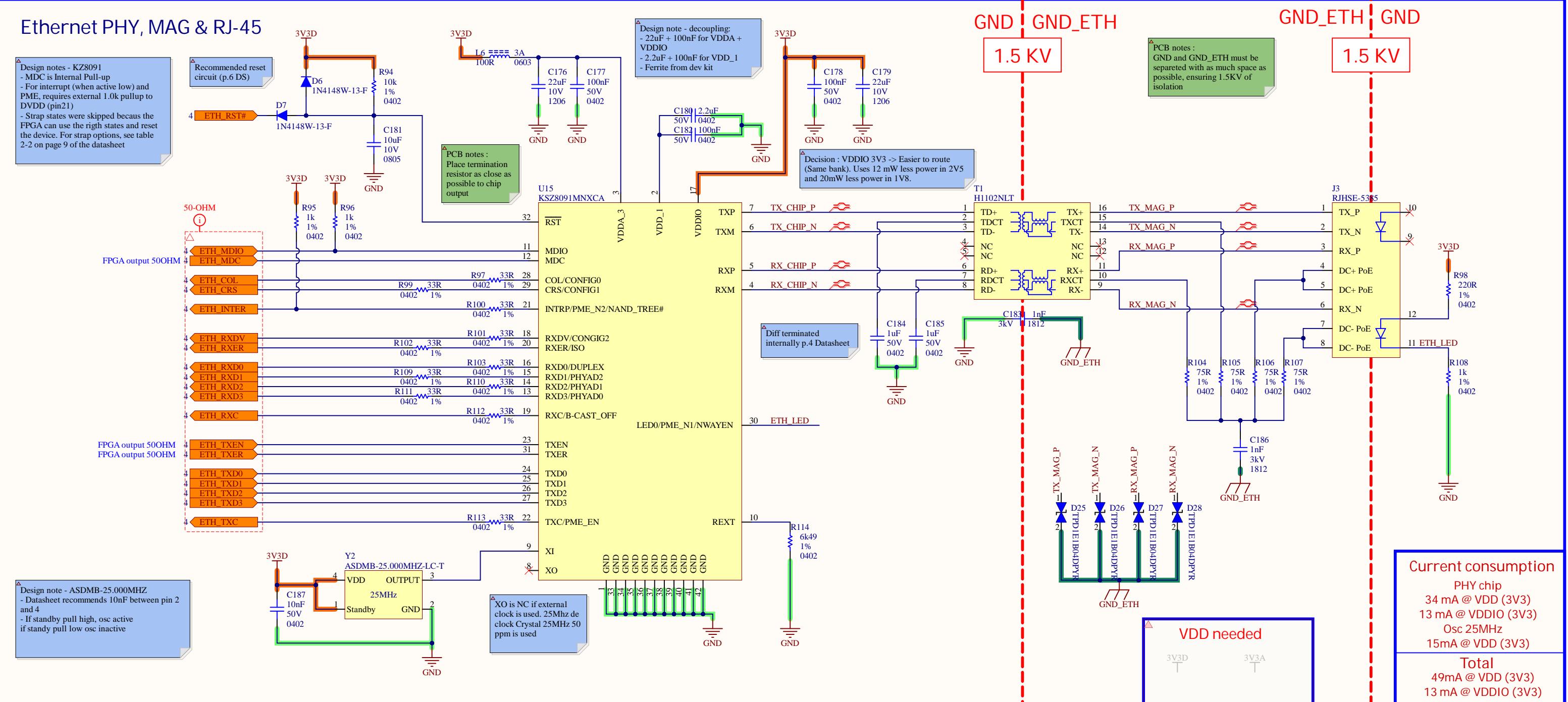
Current consumption

Protection TVS

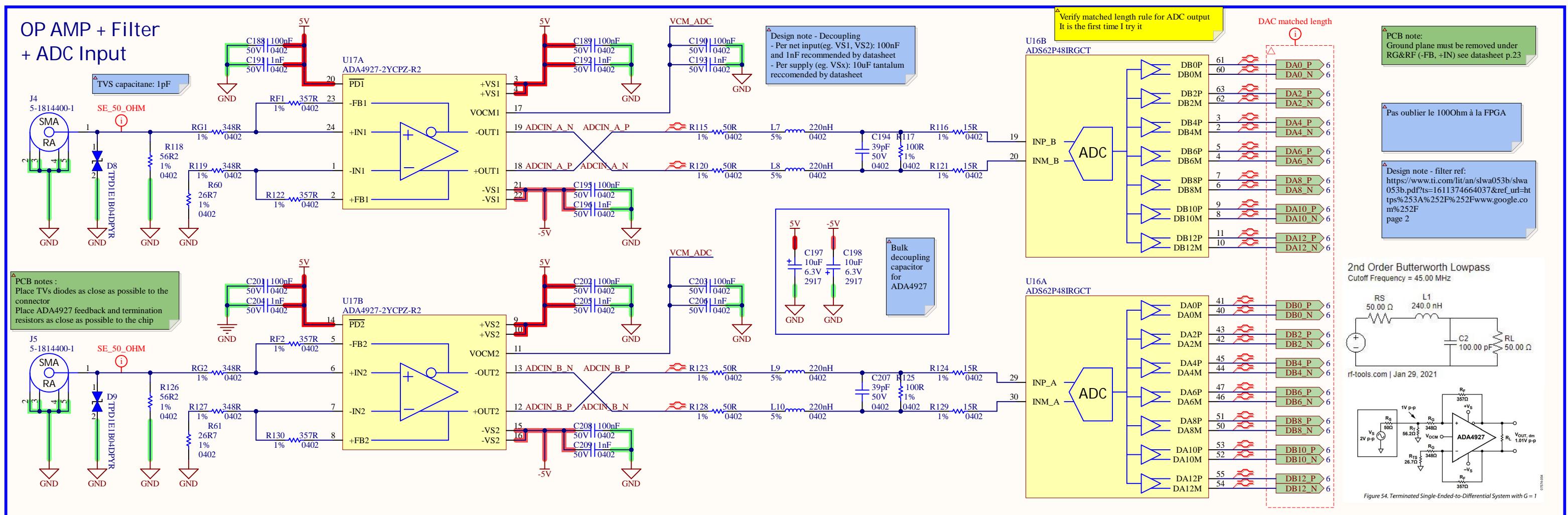


VDD needed

Sheet Name	MOT		
Project Title	P07		
Global Project	<i>Radio reconfigurable</i>		
Size 11x17	Group Ultracom	Revision 1.000	
Date 2021-01-13	Sheet 13	of 16	
Filename S7CAS-PLEIADES-CARTE-MERE_P07_MOT.SchDoc	Designers Philippe Arsenault Louis-Daniel Gaulin		



Sheet Name		ETH	
Project Title		P07	
Global Project		<i>Radio reconfigurable</i>	
Size	Group	Revision	1.000
11x17			
Date	2021-01-13	Sheet	14 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_ETH.SchDoc	Designers	Philippe Arsenault Louis-Daniel Gaulin



PCB note:
Ground plane must be removed under
RG&RF (-FB, +IN) see datasheet p.23

Pas oublier le 100Ohm à la FPGA

Design note - filter ref:
https://www.ti.com/lit/an/slwa053b/slwa053b.pdf?ts=1611374664037&ref_url=https%253A%252Fwww.google.com%252Fpage_2

2nd Order Butterworth Lowpass
Cutoff Frequency = 45.00 MHz

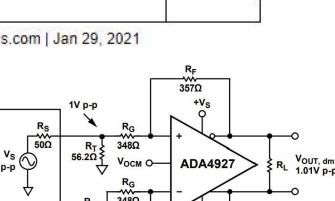
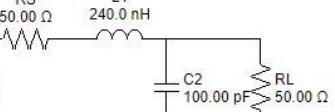
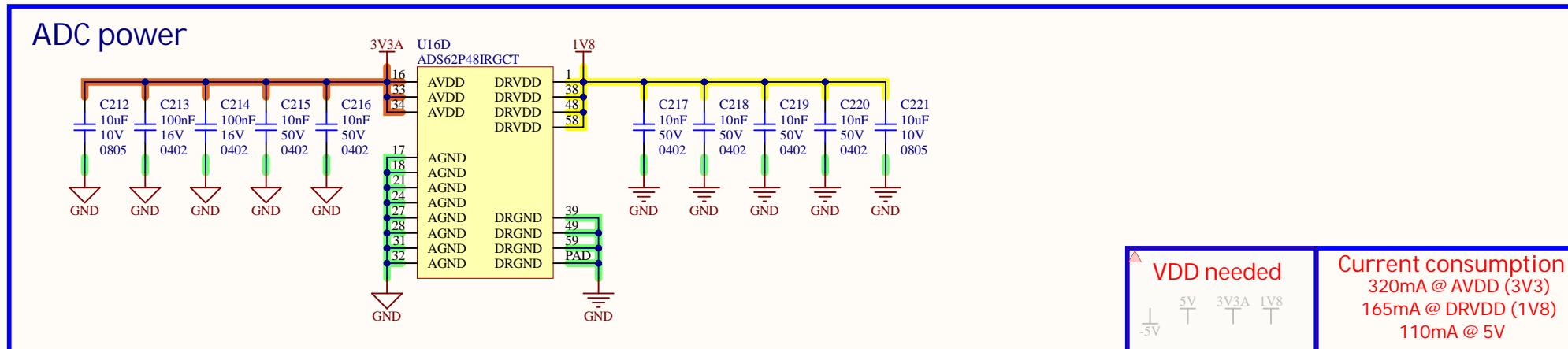
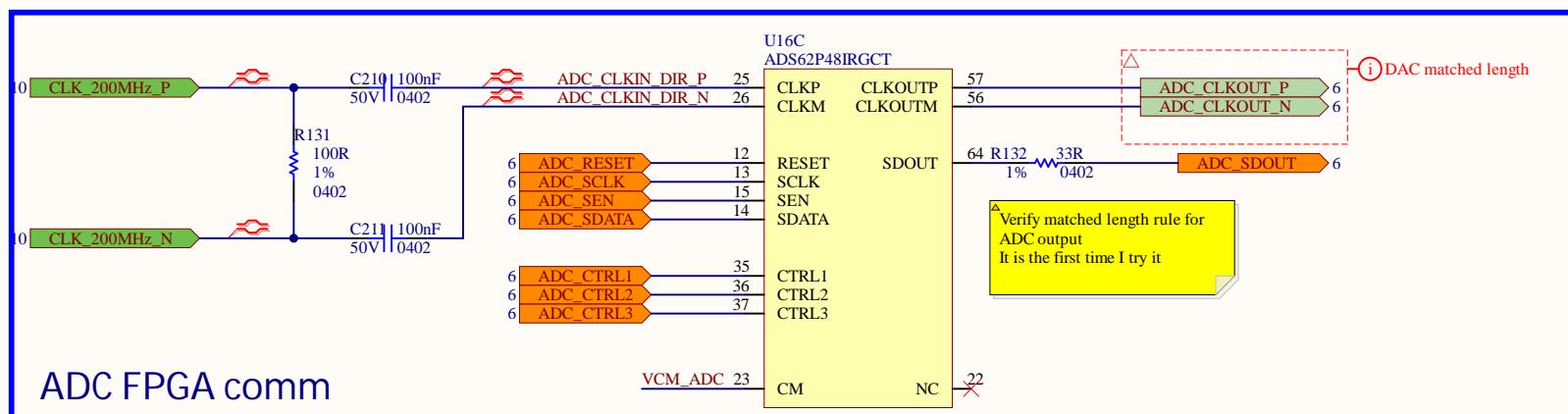


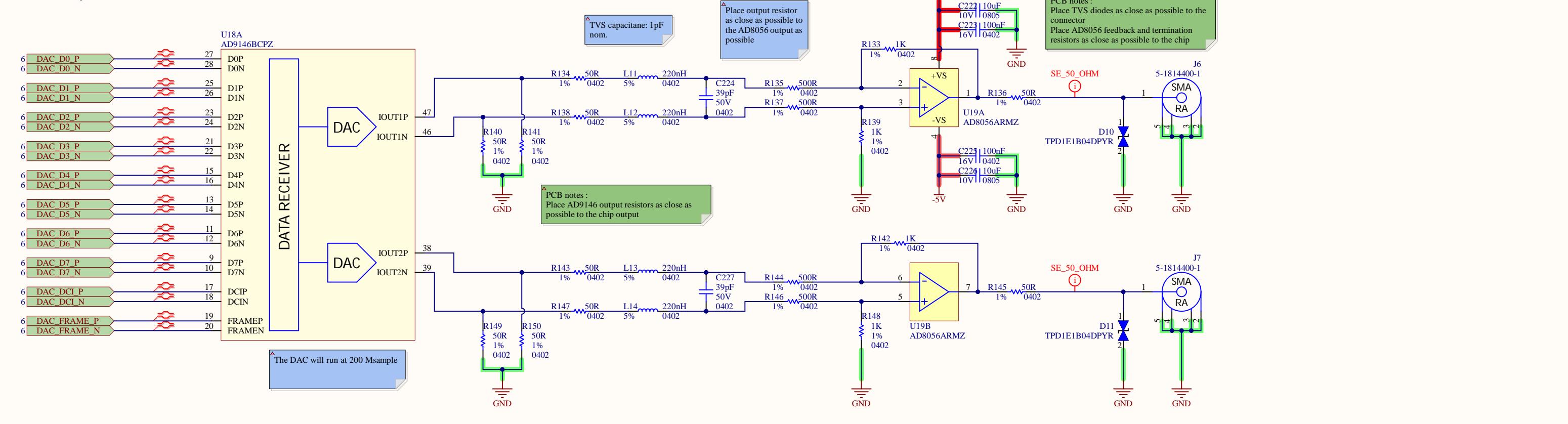
Figure 54. Terminated Single-Ended-to-Differential System with $G = 1$

07/14/04

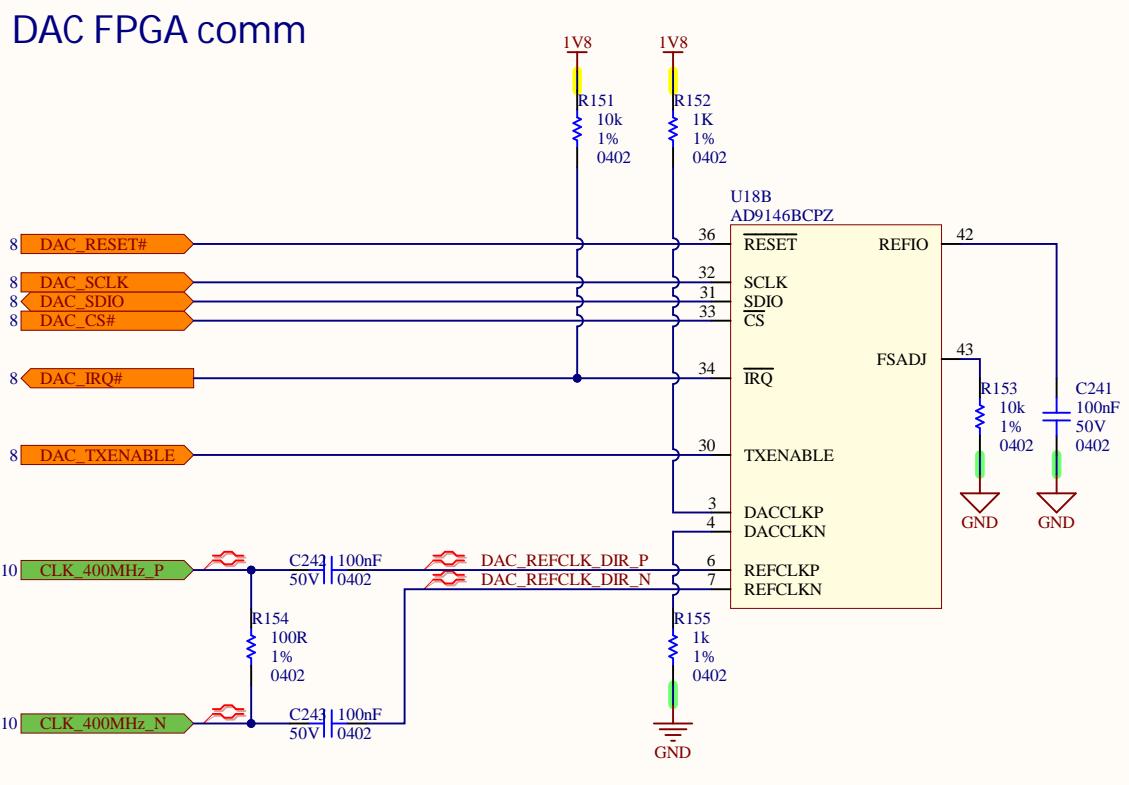


Sheet Name		ADC	
Project Title		P07	
Global Project		Radio reconfigurable	
Size	11x17	Group	Ultracom
Date	2021-01-13	Sheet	15 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_ADC.SchDoc	Designers	Philippe Arsenault, Louis-Daniel Gaulin

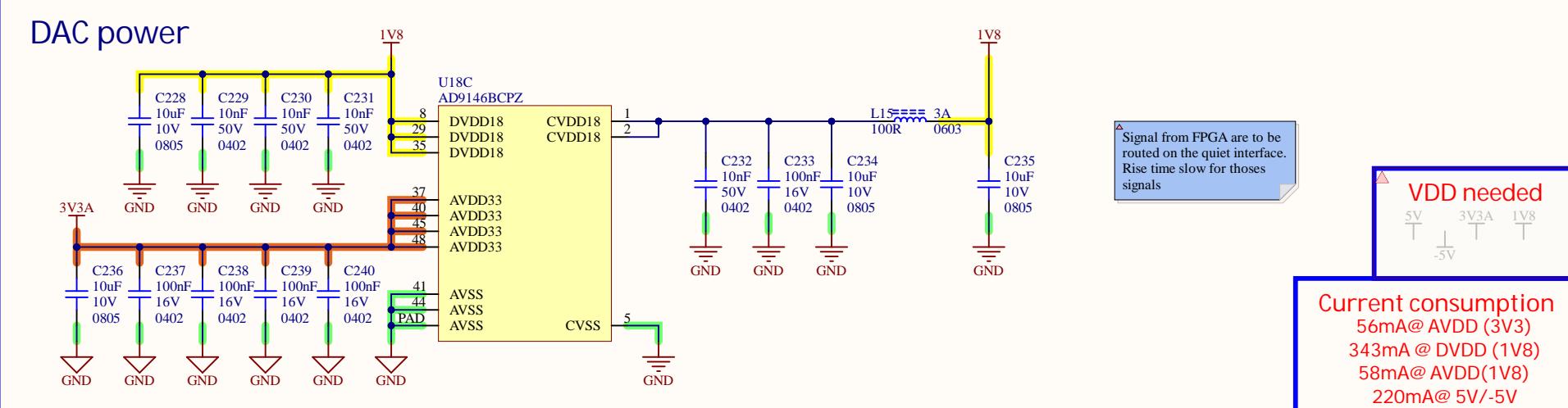
DAC output + filter + OP AMP



DAC FPGA comm



DAC power



Sheet Name

DAC

P07

Radio reconfigurable

Project Title

Revision

1.000

Global Project

Size

11x17

Group

Ultracom

Date

2021-01-13

Sheet

16 of 16

Filename

S7CAS-PLEIADES-CARTE-MERE_P07_DAC.SchDoc

Designers

Philippe Arsenault
Louis-Daniel Gaulin