P07

Radio reconfigurable

Ultracom

Revision 1.000

Date : 2021-01-13

Revision history

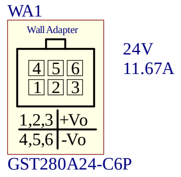
Fiducials

FID1
FID 1MM
FID2
FID 1MM
FID3
FID 1MM

Mounting holes

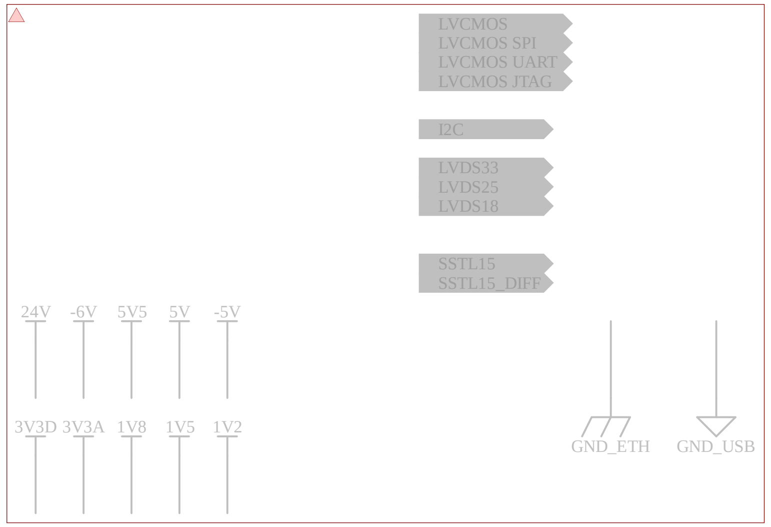
TODO with requirements

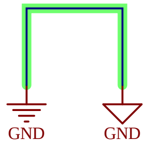
PSU


WA1
Wall Adapter
4 5 6
1 2 3
1,2,3 +Vo
4,5,6 -Vo
24V
11.67A
GST280A24-C6P

Mouse Bites

TODO with pannel

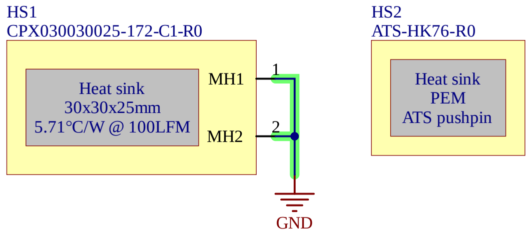

LVCMOS
LVCMOS SPI
LVCMOS UART
LVCMOS JTAG
I2C
LVDS33
LVDS25
LVDS18
SSTL15
SSTL15_DIFF
24V
-6V
5V5
5V
-5V
3V3D
3V3A
1V8
1V5
1V2
GND_ETH
GND_USB



Package size conversion	
Metric	*Imperial*
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

Design notes:
AGND and GND are connected together.
PCB NOTE: Segregate currents return between AGND and GND

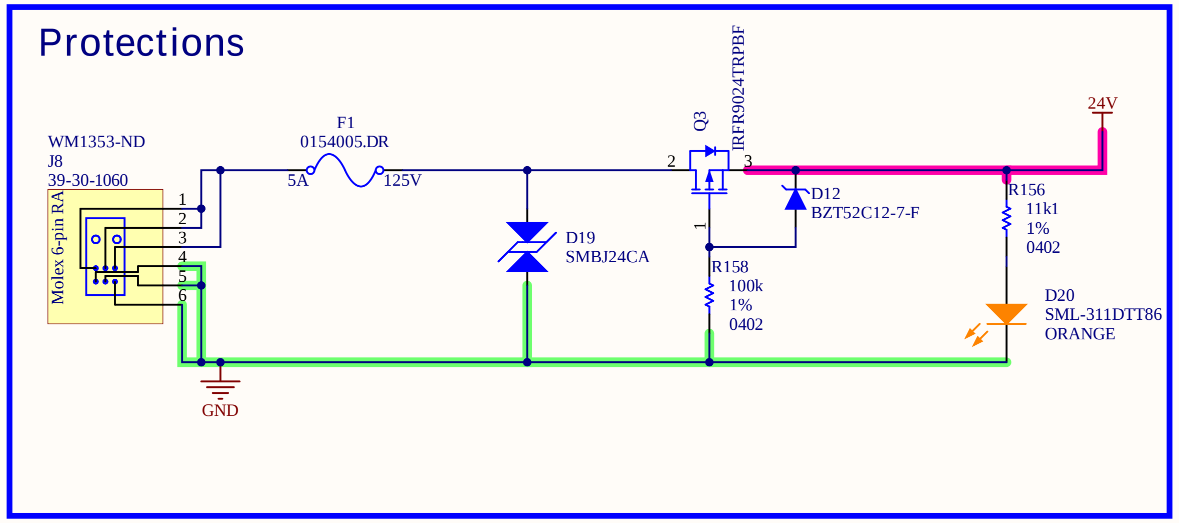
Heat sink


HS1
CPX030030025-172-C1-R0
Heat sink
30x30x25mm
5.71°C/W @ 100LFM
MH1
MH2
1
2
GND
HS2
ATS-HK76-R0
Heat sink
PEM
ATS pushpin

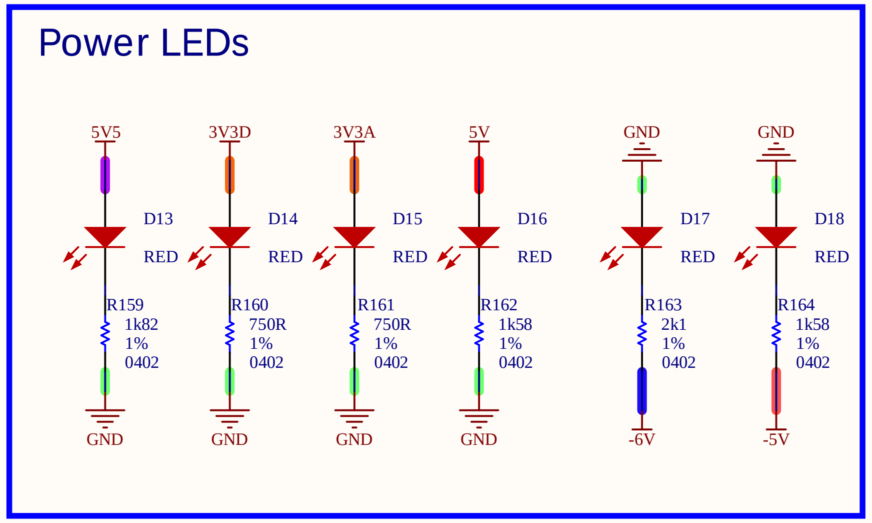
Rth HS = 5.71 °C @ 100LFM
RJC = 4 °C/W
Rth interface = 0.5°C/W
http://vendor.parker.com/852568C80043FA7A/468ea5de5ac341d385257d39005641c7/1BD00D0D0B1B018C852569580073DD53/$FILE/THERMATTACH-TAPES-THERM-CAT.pdf

Project Title P07			
Global Project *Radio reconfigurable*			
Size 11x17	Group Ultracom		Revision 1.000
Date 2021-01-13	Sheet 1 of 16		
Filename S7CAS-PLEIADES-CARTE-MERE_P07_TITLE.SchDoc		Designers Philippe Arsenault Louis-Daniel Gaulin	

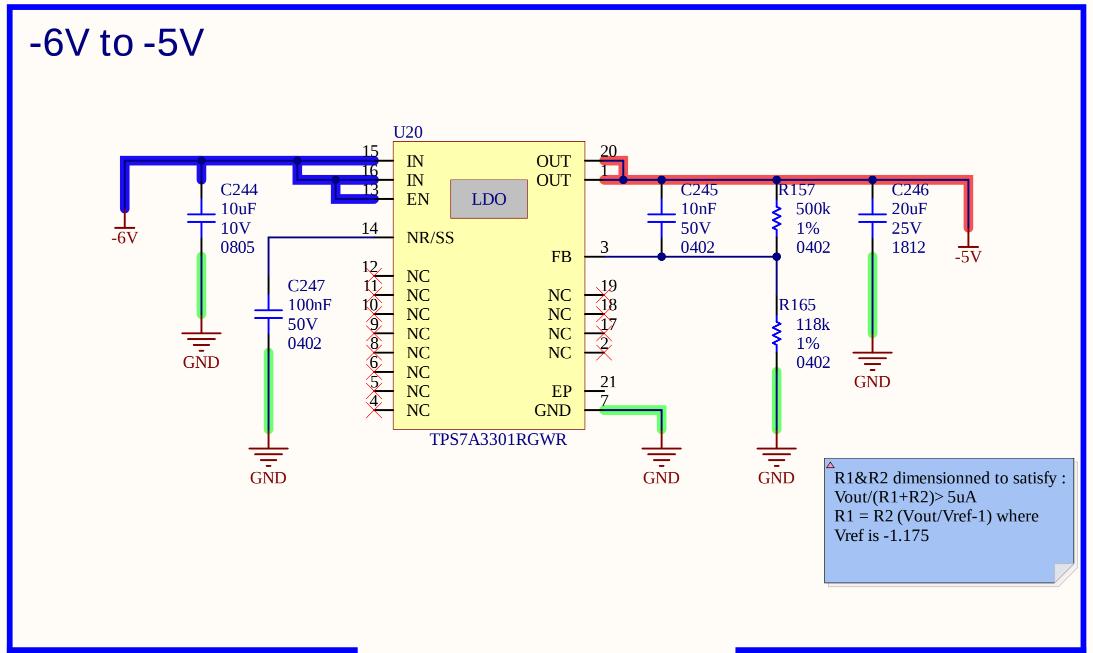
Protections


WM1353-ND
J8
39-30-1060
Molex 6-pin RA
1
2
3
4
5
6
F1
0154005.DR
5A
125V
Q3
IRFR9024TRPBF
2
3
1
D19
SMBJ24CA
D12
BZT52C12-7-F
R158
100k
1%
0402
R156
11k1
1%
0402
24V
D20
SML-311DTT86
ORANGE
GND

Power LEDs


5V5
3V3D
3V3A
5V
GND
GND
D13
RED
D14
RED
D15
RED
D16
RED
D17
RED
D18
RED
R159
1k82
1%
0402
R160
750R
1%
0402
R161
750R
1%
0402
R162
1k58
1%
0402
R163
2k1
1%
0402
R164
1k58
1%
0402
GND
GND
GND
GND
-6V
-5V

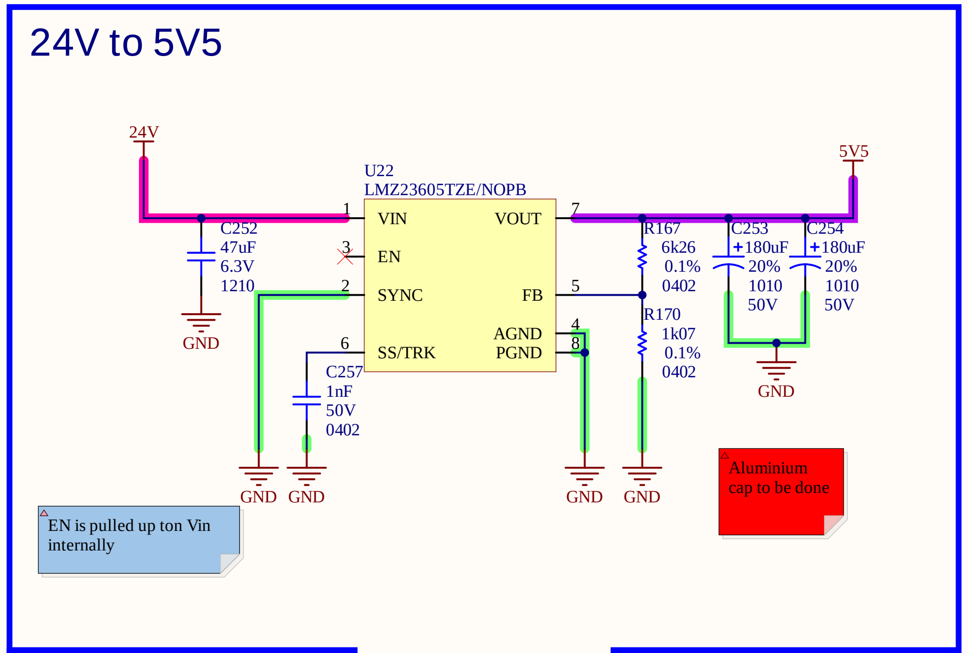
-6V to -5V


-6V
C244
10uF
10V
0805
GND
U20
15
16
13
IN
IN
EN
LDO
OUT
OUT
20
1
14
NR/SS
FB
3
C247
100nF
50V
0402
GND
12
11
10
9
8
6
5
4
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
19
18
17
2
EP
GND
21
7
TPS7A3301RGWR
C245
10nF
50V
0402
R157
500k
1%
0402
C246
20uF
25V
1812
-5V
R165
118k
1%
0402
GND
GND
GND

R1&R2 dimensionned to satisfy :
Vout/(R1+R2)> 5uA
R1 = R2 (Vout/Vref-1) where
Vref is -1.175

Input consumption -330mA@-6V	Efficiency = 83%	Output consumption -330mA@-5V

24V to 5V5

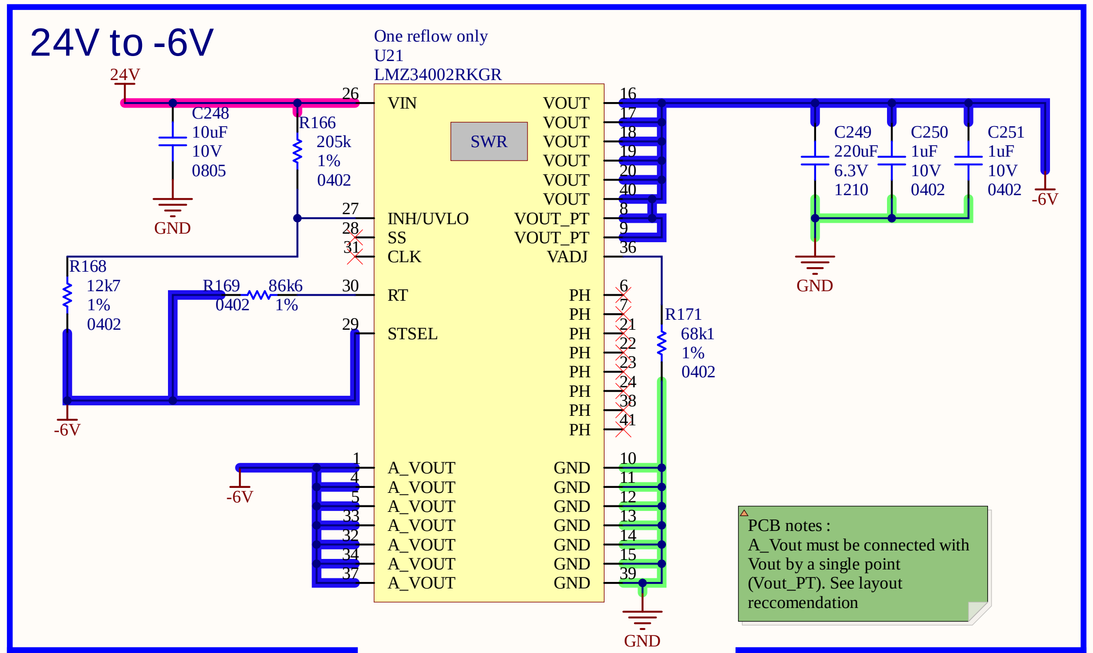

24V
C252
47uF
6.3V
1210
GND
U22
LMZ23605TZE/NOPB
1
VIN
VOUT
7
3
EN
2
SYNC
FB
5
6
SS/TRK
AGND
PGND
4
8
C257
1nF
50V
0402
GND
GND
R167
6k26
0.1%
0402
R170
1k07
0.1%
0402
C253
+180uF
20%
1010
50V
C254
+180uF
20%
1010
50V
5V5
GND
GND
GND

Aluminium cap to be done

EN is pulled up ton Vin internally

Input consumption 0.93A@24V	Efficiency = 85%	Output consumption 3.45A@5V5

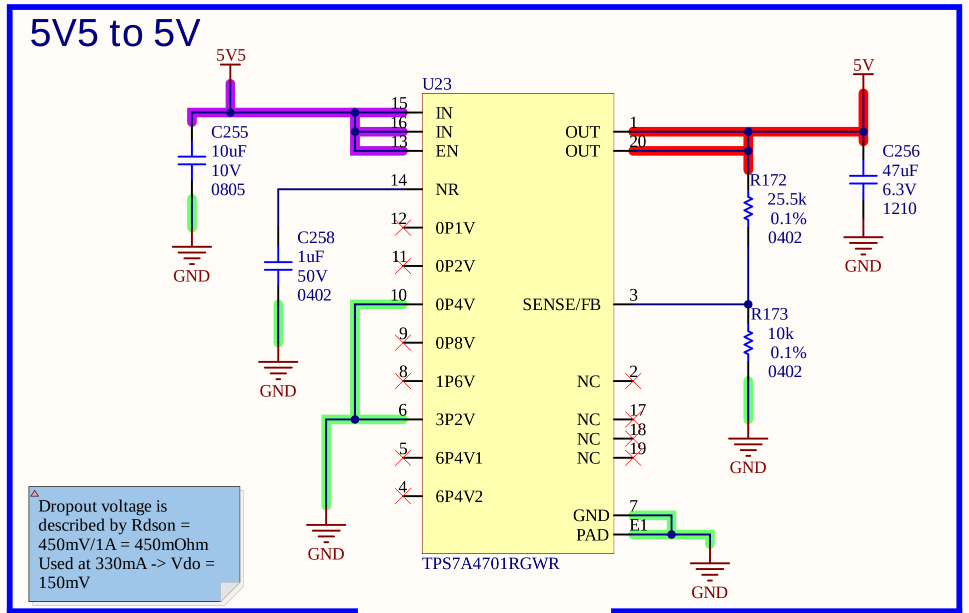
24V to -6V


24V
One reflow only
U21
LMZ34002RKGR
C248
10uF
10V
0805
GND
R166
205k
1%
0402
26
VIN
SWR
VOUT
VOUT
VOUT
VOUT
VOUT
VOUT
16
17
18
19
20
40
27
INH/UVLO
VOUT_PT
VOUT_PT
8
9
28
SS
31
CLK
VADJ
36
R168
12k7
1%
0402
R169
86k6
0402
1%
30
RT
29
STSEL
PH
PH
PH
PH
PH
PH
PH
PH
6
7
21
22
23
24
38
41
R171
68k1
1%
0402
-6V
-6V
1
2
3
4
5
33
34
35
37
A_VOUT
A_VOUT
A_VOUT
A_VOUT
A_VOUT
A_VOUT
A_VOUT
GND
GND
GND
GND
GND
GND
GND
10
11
12
13
14
15
39
GND
C249
220uF
6.3V
1210
C250
1uF
10V
0402
C251
1uF
10V
0402
-6V
GND

PCB notes :
A_Vout must be connected with Vout by a single point (Vout_PT). See layout reccomendation

Input consumption 110mA@24V	Efficiency = 75%	Output consumption -330mA@-6V

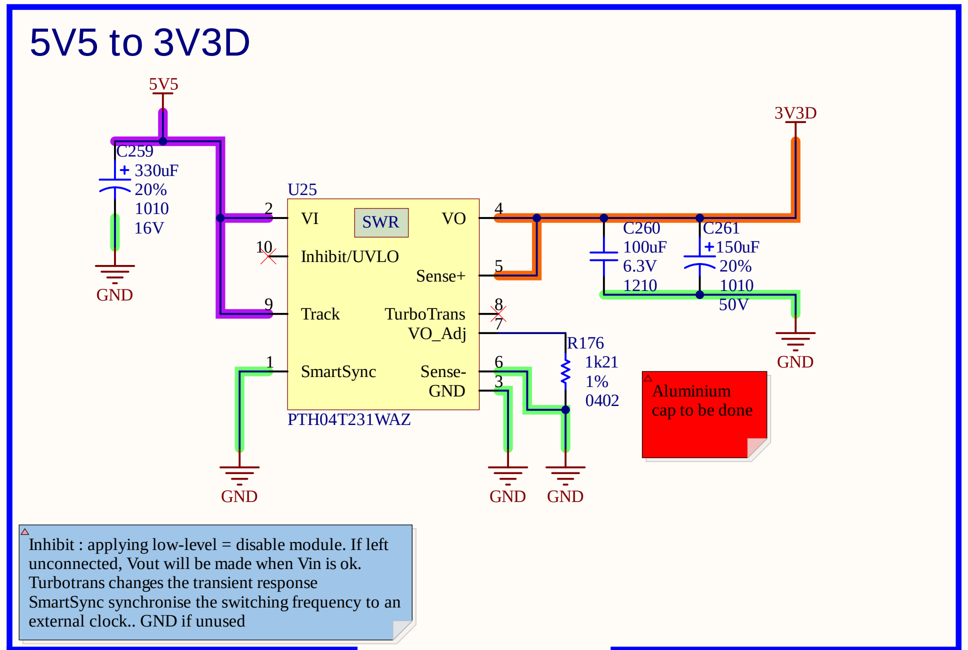
5V5 to 5V


5V5
C255
10uF
10V
0805
GND
U23
15
16
13
IN
IN
EN
OUT
OUT
1
20
14
NR
12
0P1V
11
0P2V
10
0P4V
SENSE/FB
3
9
0P8V
8
1P6V
NC
2
6
3P2V
NC
NC
NC
17
18
19
5
6P4V1
4
6P4V2
GND
PAD
7
E1
TPS7A4701RGWR
C258
1uF
50V
0402
GND
GND
R172
25.5k
0.1%
0402
R173
10k
0.1%
0402
GND
5V
C256
47uF
6.3V
1210
GND
GND

Dropout voltage is described by Rdson = 450mV/1A = 450mOhm
Used at 330mA -> Vdo = 150mV

Input consumption 330mA@5V5	Efficiency = 91%	Output consumption 330mA@5V

5V5 to 3V3D

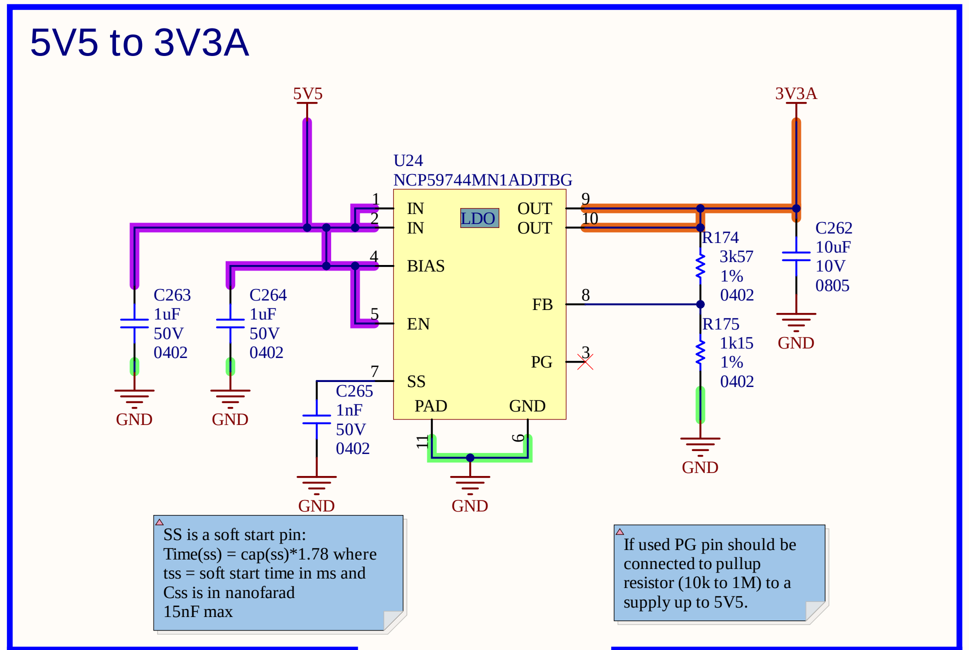

5V5
C259
+ 330uF
20%
1010
16V
GND
U25
2
VI
SWR
VO
4
10
Inhibit/UVLO
Sense+
5
9
Track
TurboTrans
VO_Adj
8
7
1
SmartSync
Sense-
GND
6
3
PTH04T231WAZ
GND
C260
100uF
6.3V
1210
C261
+150uF
20%
1010
50V
3V3D
GND
R176
1k21
1%
0402
GND
GND

Aluminium cap to be done

Inhibit : applying low-level = disable module. If left unconnected, Vout will be made when Vin is ok.
Turbotrans changes the transient response
SmartSync synchronise the switching frequency to an external clock.. GND if unused

Input consumption 2.2A@5.5V	Efficiency = 95%	Output consumption 3.48A@3V3D

5V5 to 3V3A


5V5
U24
NCP59744MN1ADJTBG
1
2
IN
IN
LDO
OUT
OUT
9
10
4
BIAS
5
EN
FB
8
7
SS
PG
3
PAD
GND
11
6
C263
1uF
50V
0402
C264
1uF
50V
0402
C265
1nF
50V
0402
GND
GND
GND
GND
R174
3k57
1%
0402
R175
1k15
1%
0402
GND
3V3A
C262
10uF
10V
0805
GND

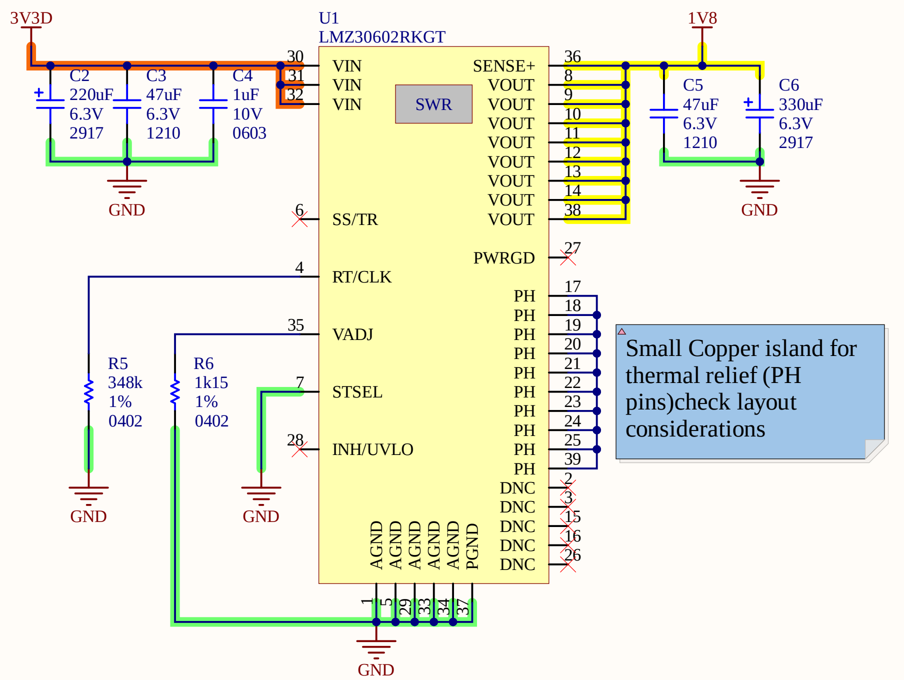
SS is a soft start pin:
Time(ss) = cap(ss)*1.78 where
tss = soft start time in ms and
Css is in nanofarad
15nF max

If used PG pin should be connected to pullup resistor (10k to 1M) to a supply up to 5V5.

Input consumption 921mA@5V5	Efficiency = 60%	Output consumption 921mA@3V3A

Sheet Name	HIGH POWER VALUES		
Project Title	P07		
Global Project	*Radio reconfigurable*		
Size 11x17	Group Ultracom		Revision 1.000
Date 2021-01-13	Sheet 2 of 16		
Filename S7CAS-PLEIADES-CARTE-MERE_P07_HIGH_POWER.SchDoc	Designers Philippe Arsenault Louis-Daniel Gaulin		

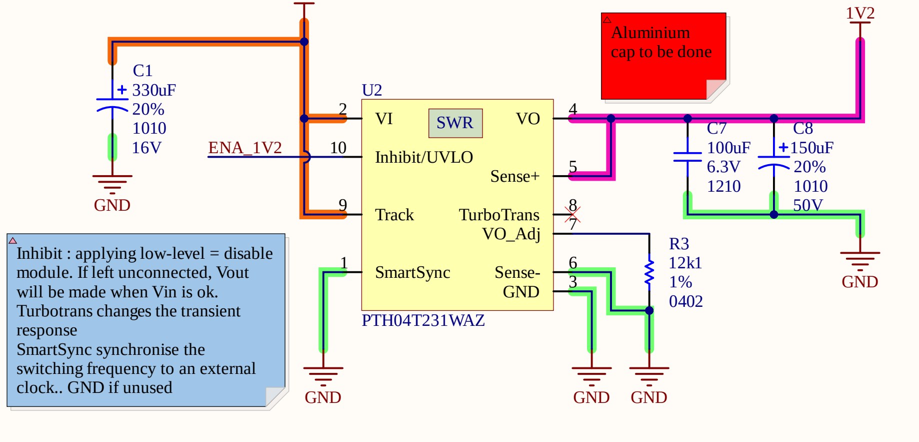
3V3D to 1V8


3V3D
C2 220uF 6.3V 2917
C3 47uF 6.3V 1210
C4 1uF 10V 0603
GND
U1 LMZ30602RKGT
VIN VIN VIN SWR
SS/TR
RT/CLK
VADJ
STSEL
INH/UVLO
SENSE+ VOUT PWRGD PH DNC
AGND AGND AGND AGND AGND PGND
1V8
C5 47uF 6.3V 1210
C6 330uF 6.3V 2917
R5 348k 1% 0402
R6 1k15 1% 0402
GND

Small Copper island for thermal relief (PH pins)check layout considerations

Input consumption 388mA@3v3D	Efficiency = 94%	Output consumption 666mA@1V8

3V3D to 1V2

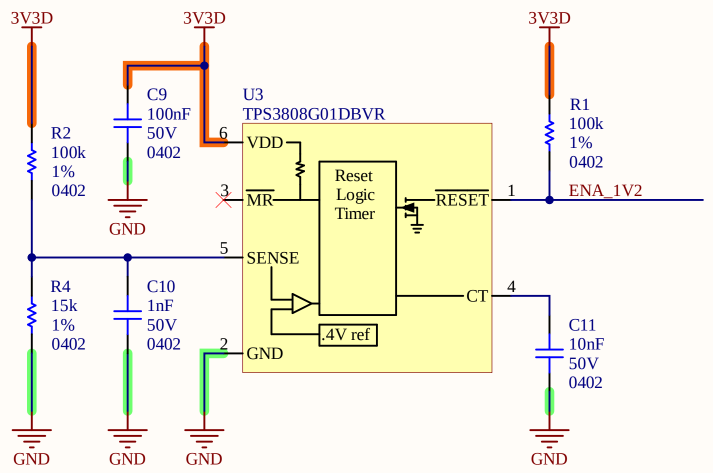

3V3D
C1 330uF 20% 1010 16V
GND
ENA_1V2
U2 VI SWR VO
Inhibit/UVLO Sense+
Track TurboTrans VO_Adj
SmartSync Sense- GND
PTH04T231WAZ
1V2
C7 100uF 6.3V 1210
C8 150uF 20% 1010 50V
R3 12k1 1% 0402
GND

Aluminium cap to be done

Inhibit : applying low-level = disable module. If left unconnected, Vout will be made when Vin is ok. Turbotrans changes the transient response SmartSync synchronise the switching frequency to an external clock.. GND if unused

Input consumption 1.18A@3V3D	Efficiency = 92%	Output consumption 3A@1V2D

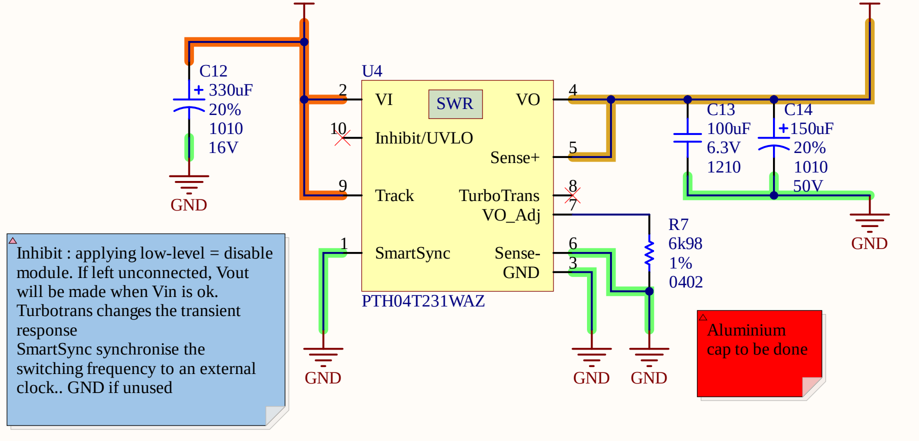
1V2 delay


3V3D
R2 100k 1% 0402
R4 15k 1% 0402
C9 100nF 50V 0402
C10 1nF 50V 0402
U3 TPS3808G01DBVR
VDD MR SENSE GND
Reset Logic Timer
RESET CT
.4V ref
R1 100k 1% 0402
ENA_1V2
C11 10nF 50V 0402
GND

Delay = 60ms
VTH = 3.05 - 3.15 V

Power consumption 40uA @ 3V3D 10uA @ 1V5

3V3D to 1V5


3V3D
C12 330uF 20% 1010 16V
GND
U4 VI SWR VO
Inhibit/UVLO Sense+
Track TurboTrans VO_Adj
SmartSync Sense- GND
PTH04T231WAZ
1V5
C13 100uF 6.3V 1210
C14 150uF 20% 1010 50V
R7 6k98 1% 0402
GND

Inhibit : applying low-level = disable module. If left unconnected, Vout will be made when Vin is ok. Turbotrans changes the transient response SmartSync synchronise the switching frequency to an external clock.. GND if unused

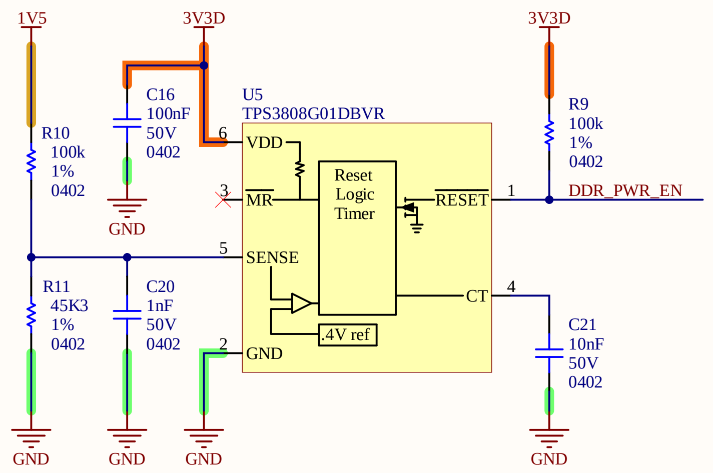
Aluminium cap to be done

Input consumption 1.08A@3V3D	Efficiency = 92%	Output consumption 2.07A@1V5D

If used PG pin should be connected to pullup resistor (10k to 1M) to a supply up to 5V5.

Only constraint of power-on sequence :
VTT (0.75V) must come after 1V5 -> 1V5 is used to make VTT
The FPGA core (1V2) must come after the flash (3V3D) -> 3V3D is used to make 1V2D
Futhermore, the PTH04T230W has a soft start feature.

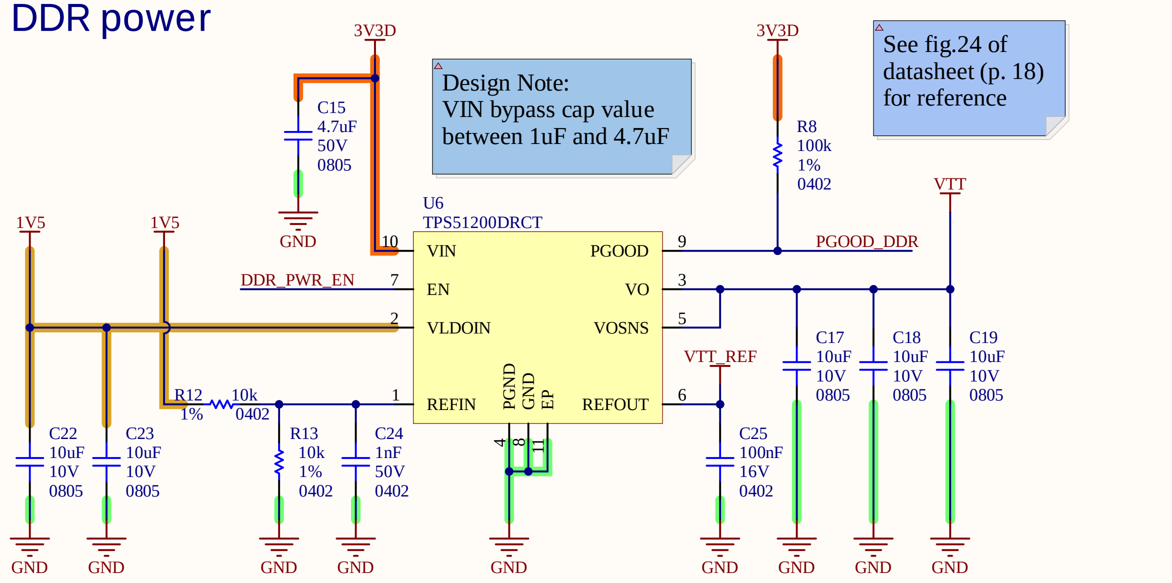
DDR power delay


1V5
3V3D
R10 100k 1% 0402
R11 45K3 1% 0402
C16 100nF 50V 0402
C20 1nF 50V 0402
U5 TPS3808G01DBVR
VDD MR SENSE GND
Reset Logic Timer
RESET CT
.4V ref
R9 100k 1% 0402
DDR_PWR_EN
C21 10nF 50V 0402
GND

Delay = 60ms
VTH = 1.28-1.32 V

Power consumption 40uA @ 3V3D 10uA @ 1V5

DDR power


3V3D
C15 4.7uF 50V 0805
GND
1V5
DDR_PWR_EN
U6 TPS51200DRCT
VIN EN VLDOIN REFIN PGND GND EP
PGOOD VO VOSNS REFOUT
R8 100k 1% 0402
PGOOD_DDR
VTT
VTT_REF
C22 10uF 10V 0805
C23 10uF 10V 0805
R12 1% 10k 0402
R13 10k 1% 0402
C24 1nF 50V 0402
C25 100nF 16V 0402
C17 10uF 10V 0805
C18 10uF 10V 0805
C19 10uF 10V 0805

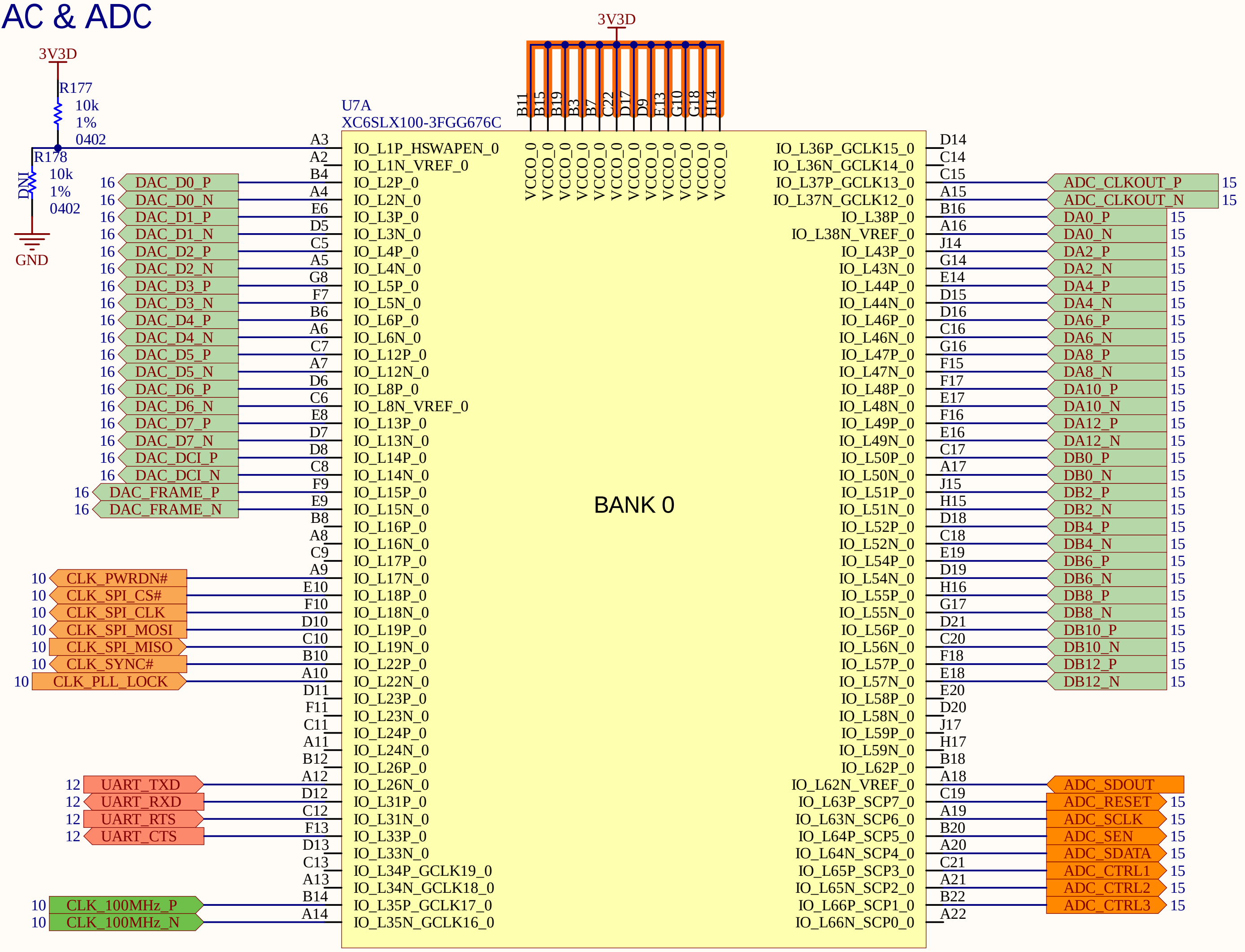
Design Note:
VIN bypass cap value between 1uF and 4.7uF

See fig.24 of datasheet (p. 18) for reference

Input consumption 10mA @ 3V3 500mA @ 1V5	Efficiency = 50%	Output consumption 500mA @ VTT (0V75) 10mA @ VTT_REF (0V75)

Sheet Name	LOW VALUE POWER
Project Title	P07
Global Project	*Radio reconfigurable*
Size	11x17
Group	Ultracom
Revision	1.000
Date	2021-01-13
Sheet	3 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_LOW_POWER.SchDoc
Designers	Philippe Arsenault Louis-Daniel Gaulin

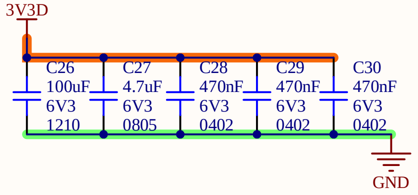
Bank 0 - 3V3 - DAC & ADC


3V3D
R177 10k 1% 0402
R178 10k 1% 0402 DNI
GND
U7A
XC6SLX100-3FGG676C
3V3D
B11 B15 B19 B3 B7 C22 D17 D9 E13 G10 G18 H14
VCCO_0 VCCO_0 VCCO_0 VCCO_0 VCCO_0 VCCO_0 VCCO_0 VCCO_0 VCCO_0 VCCO_0 VCCO_0 VCCO_0
BANK 0
A3 IO_L1P_HSWAPEN_0
A2 IO_L1N_VREF_0
16 DAC_D0_P B4 IO_L2P_0
16 DAC_D0_N A4 IO_L2N_0
16 DAC_D1_P E6 IO_L3P_0
16 DAC_D1_N D5 IO_L3N_0
16 DAC_D2_P C5 IO_L4P_0
16 DAC_D2_N A5 IO_L4N_0
16 DAC_D3_P G8 IO_L5P_0
16 DAC_D3_N F7 IO_L5N_0
16 DAC_D4_P B6 IO_L6P_0
16 DAC_D4_N A6 IO_L6N_0
16 DAC_D5_P C7 IO_L12P_0
16 DAC_D5_N A7 IO_L12N_0
16 DAC_D6_P D6 IO_L8P_0
16 DAC_D6_N C6 IO_L8N_VREF_0
16 DAC_D7_P E8 IO_L13P_0
16 DAC_D7_N D7 IO_L13N_0
16 DAC_DCI_P D8 IO_L14P_0
16 DAC_DCI_N C8 IO_L14N_0
16 DAC_FRAME_P F9 IO_L15P_0
16 DAC_FRAME_N E9 IO_L15N_0
B8 IO_L16P_0
A8 IO_L16N_0
C9 IO_L17P_0
10 CLK_PWRDN# A9 IO_L17N_0
10 CLK_SPI_CS# E10 IO_L18P_0
10 CLK_SPI_CLK F10 IO_L18N_0
10 CLK_SPI_MOSI D10 IO_L19P_0
10 CLK_SPI_MISO C10 IO_L19N_0
10 CLK_SYNC# B10 IO_L22P_0
10 CLK_PLL_LOCK A10 IO_L22N_0
D11 IO_L23P_0
F11 IO_L23N_0
C11 IO_L24P_0
A11 IO_L24N_0
B12 IO_L26P_0
12 UART_TXD A12 IO_L26N_0
12 UART_RXD D12 IO_L31P_0
12 UART_RTS C12 IO_L31N_0
12 UART_CTS F13 IO_L33P_0
D13 IO_L33N_0
C13 IO_L34P_GCLK19_0
A13 IO_L34N_GCLK18_0
10 CLK_100MHz_P B14 IO_L35P_GCLK17_0
10 CLK_100MHz_N A14 IO_L35N_GCLK16_0
IO_L36P_GCLK15_0 D14
IO_L36N_GCLK14_0 C14
IO_L37P_GCLK13_0 C15 ADC_CLKOUT_P 15
IO_L37N_GCLK12_0 A15 ADC_CLKOUT_N 15
IO_L38P_0 B16 DA0_P 15
IO_L38N_VREF_0 A16 DA0_N 15
IO_L43P_0 J14 DA2_P 15
IO_L43N_0 G14 DA2_N 15
IO_L44P_0 E14 DA4_P 15
IO_L44N_0 D15 DA4_N 15
IO_L46P_0 D16 DA6_P 15
IO_L46N_0 C16 DA6_N 15
IO_L47P_0 G16 DA8_P 15
IO_L47N_0 F15 DA8_N 15
IO_L48P_0 F17 DA10_P 15
IO_L48N_0 E17 DA10_N 15
IO_L49P_0 F16 DA12_P 15
IO_L49N_0 E16 DA12_N 15
IO_L50P_0 C17 DB0_P 15
IO_L50N_0 A17 DB0_N 15
IO_L51P_0 J15 DB2_P 15
IO_L51N_0 H15 DB2_N 15
IO_L52P_0 D18 DB4_P 15
IO_L52N_0 C18 DB4_N 15
IO_L54P_0 E19 DB6_P 15
IO_L54N_0 D19 DB6_N 15
IO_L55P_0 H16 DB8_P 15
IO_L55N_0 G17 DB8_N 15
IO_L56P_0 D21 DB10_P 15
IO_L56N_0 C20 DB10_N 15
IO_L57P_0 F18 DB12_P 15
IO_L57N_0 E18 DB12_N 15
IO_L58P_0 E20
IO_L58N_0 D20
IO_L59P_0 J17
IO_L59N_0 H17
IO_L62P_0 B18
IO_L62N_VREF_0 A18 ADC_SDOUT
IO_L63P_SCP7_0 C19 ADC_RESET 15
IO_L63N_SCP6_0 A19 ADC_SCLK 15
IO_L64P_SCP5_0 B20 ADC_SEN 15
IO_L64N_SCP4_0 A20 ADC_SDATA 15
IO_L65P_SCP3_0 C21 ADC_CTRL1 15
IO_L65N_SCP2_0 A21 ADC_CTRL2 15
IO_L66P_SCP1_0 B22 ADC_CTRL3 15
IO_L66N_SCP0_0 A22

Current consumption

100mA @ VCCO_0 (3V3)

FPGA Bank 0 Decoupling Capacitors


3V3D
C26 100uF 6V3 1210
C27 4.7uF 6V3 0805
C28 470nF 6V3 0402
C29 470nF 6V3 0402
C30 470nF 6V3 0402
GND

Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Sheet Name
FPGA_0

Project Title
P07

Global Project
Radio reconfigurable

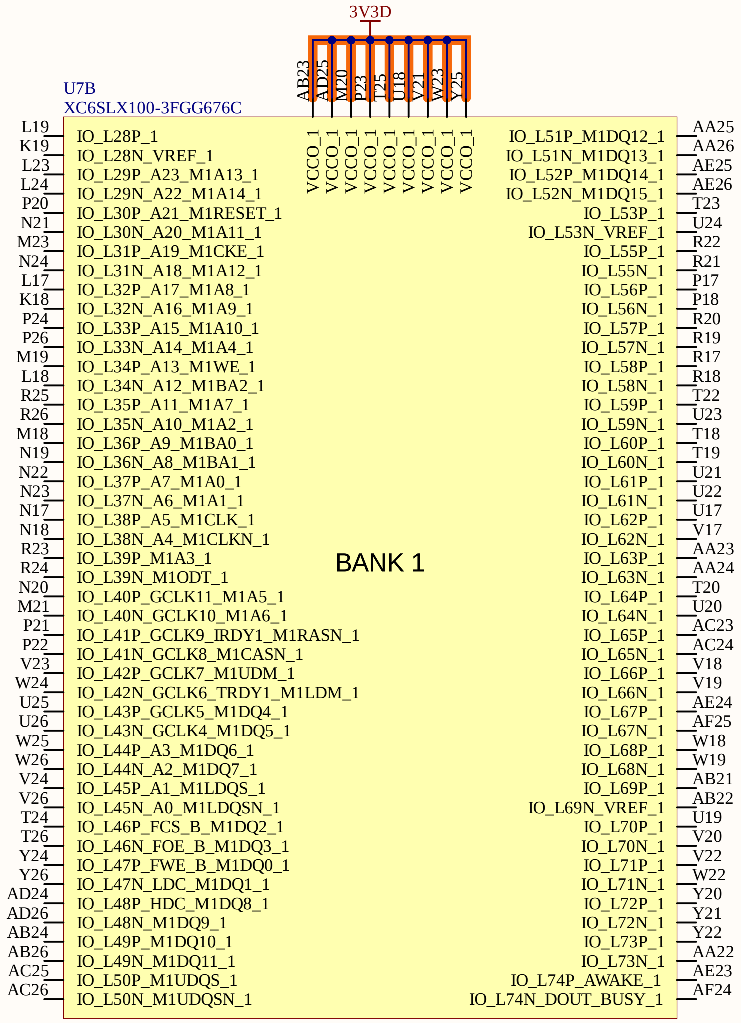
Size 11x17
Group Ultracom
Revision 1.000

Date 2021-01-13
Sheet 4 of 16

Filename
S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_0.SchDoc

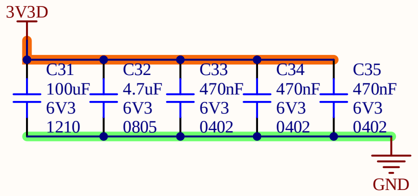
Designers
Philippe Arsenault
Louis-Daniel Gaulin

Bank 1 - 3V3 - Unused


3V3D
U7B
XC6SLX100-3FGG676C
AB23 VCCO_1
AD25 VCCO_1
M20 VCCO_1
P23 VCCO_1
T25 VCCO_1
U18 VCCO_1
V21 VCCO_1
W23 VCCO_1
Y25 VCCO_1
BANK 1
L19 IO_L28P_1
K19 IO_L28N_VREF_1
L23 IO_L29P_A23_M1A13_1
L24 IO_L29N_A22_M1A14_1
P20 IO_L30P_A21_M1RESET_1
N21 IO_L30N_A20_M1A11_1
M23 IO_L31P_A19_M1CKE_1
N24 IO_L31N_A18_M1A12_1
L17 IO_L32P_A17_M1A8_1
K18 IO_L32N_A16_M1A9_1
P24 IO_L33P_A15_M1A10_1
P26 IO_L33N_A14_M1A4_1
M19 IO_L34P_A13_M1WE_1
L18 IO_L34N_A12_M1BA2_1
R25 IO_L35P_A11_M1A7_1
R26 IO_L35N_A10_M1A2_1
M18 IO_L36P_A9_M1BA0_1
N19 IO_L36N_A8_M1BA1_1
N22 IO_L37P_A7_M1A0_1
N23 IO_L37N_A6_M1A1_1
N17 IO_L38P_A5_M1CLK_1
N18 IO_L38N_A4_M1CLKN_1
R23 IO_L39P_M1A3_1
R24 IO_L39N_M1ODT_1
N20 IO_L40P_GCLK11_M1A5_1
M21 IO_L40N_GCLK10_M1A6_1
P21 IO_L41P_GCLK9_IRDY1_M1RASN_1
P22 IO_L41N_GCLK8_M1CASN_1
V23 IO_L42P_GCLK7_M1UDM_1
W24 IO_L42N_GCLK6_TRDY1_M1LDM_1
U25 IO_L43P_GCLK5_M1DQ4_1
U26 IO_L43N_GCLK4_M1DQ5_1
W25 IO_L44P_A3_M1DQ6_1
W26 IO_L44N_A2_M1DQ7_1
V24 IO_L45P_A1_M1LDQS_1
V26 IO_L45N_A0_M1LDQSN_1
T24 IO_L46P_FCS_B_M1DQ2_1
T26 IO_L46N_FOE_B_M1DQ3_1
Y24 IO_L47P_FWE_B_M1DQ0_1
Y26 IO_L47N_LDC_M1DQ1_1
AD24 IO_L48P_HDC_M1DQ8_1
AD26 IO_L48N_M1DQ9_1
AB24 IO_L49P_M1DQ10_1
AB26 IO_L49N_M1DQ11_1
AC25 IO_L50P_M1UDQS_1
AC26 IO_L50N_M1UDQSN_1
IO_L51P_M1DQ12_1 AA25
IO_L51N_M1DQ13_1 AA26
IO_L52P_M1DQ14_1 AE25
IO_L52N_M1DQ15_1 AE26
IO_L53P_1 T23
IO_L53N_VREF_1 U24
IO_L55P_1 R22
IO_L55N_1 R21
IO_L56P_1 P17
IO_L56N_1 P18
IO_L57P_1 R20
IO_L57N_1 R19
IO_L58P_1 R17
IO_L58N_1 R18
IO_L59P_1 T22
IO_L59N_1 U23
IO_L60P_1 T18
IO_L60N_1 T19
IO_L61P_1 U21
IO_L61N_1 U22
IO_L62P_1 U17
IO_L62N_1 V17
IO_L63P_1 AA23
IO_L63N_1 AA24
IO_L64P_1 T20
IO_L64N_1 U20
IO_L65P_1 AC23
IO_L65N_1 AC24
IO_L66P_1 V18
IO_L66N_1 V19
IO_L67P_1 AE24
IO_L67N_1 AF25
IO_L68P_1 W18
IO_L68N_1 W19
IO_L69P_1 AB21
IO_L69N_VREF_1 AB22
IO_L70P_1 U19
IO_L70N_1 V20
IO_L71P_1 V22
IO_L71N_1 W22
IO_L72P_1 Y20
IO_L72N_1 Y21
IO_L73P_1 Y22
IO_L73N_1 AA22
IO_L74P_AWAKE_1 AE23
IO_L74N_DOUT_BUSY_1 AF24

Current consumption
50mA @ VCCO_1 (3V3)

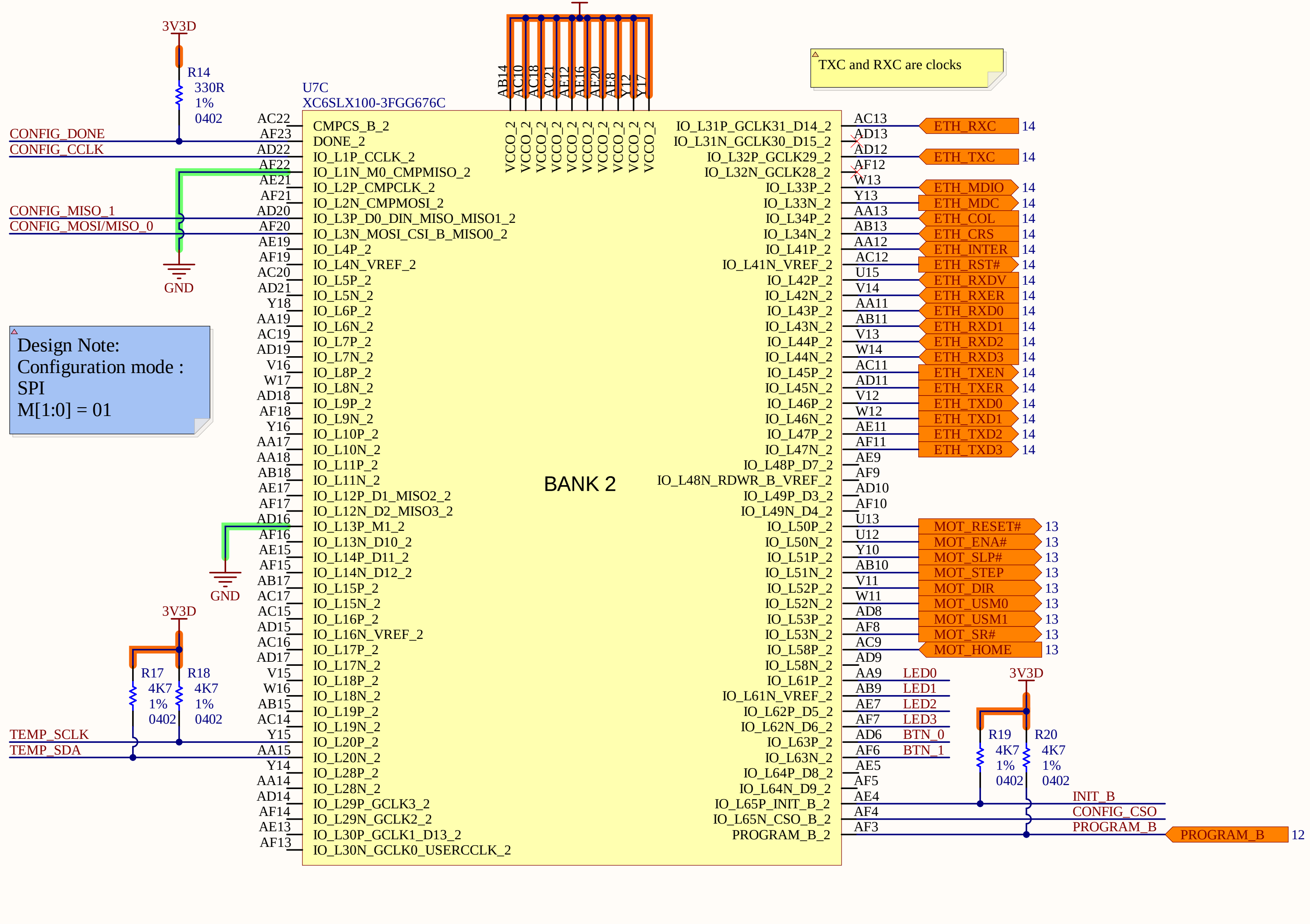
FPGA Bank 1 Decoupling Capacitors


3V3D
C31
100uF
6V3
1210
C32
4.7uF
6V3
0805
C33
470nF
6V3
0402
C34
470nF
6V3
0402
C35
470nF
6V3
0402
GND

Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Sheet Name	FPGA_1	
Project Title	P07	
Global Project	*Radio reconfigurable*	
Size 11x17	Group Ultracom	Revision 1.000
Date 2021-01-13	Sheet 5 of 16	
Filename S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_1.SchDoc	Designers Philippe Arsenault Louis-Daniel Gaulin	

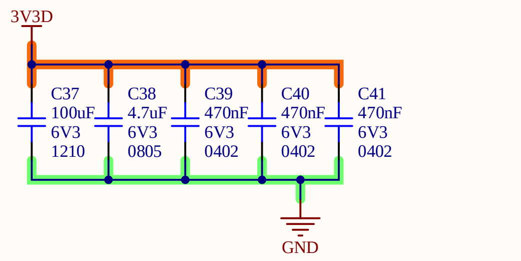
Bank 2 - 3V3 - Ethernet


3V3D
R14 330R 1% 0402
U7C XC6SLX100-3FGG676C
CONFIG_DONE
CONFIG_CCLK
CONFIG_MISO_1
CONFIG_MOSI/MISO_0
GND
AC22 CMPCS_B_2
AF23 DONE_2
AD22 IO_L1P_CCLK_2
AF22 IO_L1N_M0_CMPMISO_2
AE21 IO_L2P_CMPCLK_2
AF21 IO_L2N_CMPMOSI_2
AD20 IO_L3P_D0_DIN_MISO_MISO1_2
AF20 IO_L3N_MOSI_CSI_B_MISO0_2
AE19 IO_L4P_2
AF19 IO_L4N_VREF_2
AC20 IO_L5P_2
AD21 IO_L5N_2
Y18 IO_L6P_2
AA19 IO_L6N_2
AC19 IO_L7P_2
AD19 IO_L7N_2
V16 IO_L8P_2
W17 IO_L8N_2
AD18 IO_L9P_2
AF18 IO_L9N_2
Y16 IO_L10P_2
AA17 IO_L10N_2
AA18 IO_L11P_2
AB18 IO_L11N_2
AE17 IO_L12P_D1_MISO2_2
AF17 IO_L12N_D2_MISO3_2
AD16 IO_L13P_M1_2
AF16 IO_L13N_D10_2
AE15 IO_L14P_D11_2
AF15 IO_L14N_D12_2
AB17 IO_L15P_2
AC17 IO_L15N_2
AC15 IO_L16P_2
AD15 IO_L16N_VREF_2
AC16 IO_L17P_2
AD17 IO_L17N_2
V15 IO_L18P_2
W16 IO_L18N_2
AB15 IO_L19P_2
AC14 IO_L19N_2
Y15 IO_L20P_2
AA15 IO_L20N_2
Y14 IO_L28P_2
AA14 IO_L28N_2
AD14 IO_L29P_GCLK3_2
AF14 IO_L29N_GCLK2_2
AE13 IO_L30P_GCLK1_D13_2
AF13 IO_L30N_GCLK0_USERCCLK_2
BANK 2
A14 AC10 AC18 AC21 AF16 AF20 AF8 Y12 Y17
VCCO_2
IO_L31P_GCLK31_D14_2 AC13 ETH_RXC 14
IO_L31N_GCLK30_D15_2 AD13
IO_L32P_GCLK29_2 AD12 ETH_TXC 14
IO_L32N_GCLK28_2 AF12
IO_L33P_2 W13 ETH_MDIO 14
IO_L33N_2 Y13 ETH_MDC 14
IO_L34P_2 AA13 ETH_COL 14
IO_L34N_2 AB13 ETH_CRS 14
IO_L41P_2 AA12 ETH_INTER 14
IO_L41N_VREF_2 AC12 ETH_RST# 14
IO_L42P_2 U15 ETH_RXDV 14
IO_L42N_2 V14 ETH_RXER 14
IO_L43P_2 AA11 ETH_RXD0 14
IO_L43N_2 AB11 ETH_RXD1 14
IO_L44P_2 V13 ETH_RXD2 14
IO_L44N_2 W14 ETH_RXD3 14
IO_L45P_2 AC11 ETH_TXEN 14
IO_L45N_2 AD11 ETH_TXER 14
IO_L46P_2 V12 ETH_TXD0 14
IO_L46N_2 W12 ETH_TXD1 14
IO_L47P_2 AE11 ETH_TXD2 14
IO_L47N_2 AF11 ETH_TXD3 14
IO_L48P_D7_2 AE9
IO_L48N_RDWR_B_VREF_2 AF9
IO_L49P_D3_2 AD10
IO_L49N_D4_2 AF10
IO_L50P_2 U13 MOT_RESET# 13
IO_L50N_2 U12 MOT_ENA# 13
IO_L51P_2 Y10 MOT_SLP# 13
IO_L51N_2 AB10 MOT_STEP 13
IO_L52P_2 V11 MOT_DIR 13
IO_L52N_2 W11 MOT_USM0 13
IO_L53P_2 AD8 MOT_USM1 13
IO_L53N_2 AF8 MOT_SR# 13
IO_L58P_2 AC9 MOT_HOME 13
IO_L58N_2 AD9
IO_L61P_2 AA9 LED0
IO_L61N_VREF_2 AB9 LED1
IO_L62P_D5_2 AE7 LED2
IO_L62N_D6_2 AF7 LED3
IO_L63P_2 AD6 BTN_0
IO_L63N_2 AF6 BTN_1
IO_L64P_D8_2 AE5
IO_L64N_D9_2 AF5
IO_L65P_INIT_B_2 AE4 INIT_B
IO_L65N_CSO_B_2 AF4 CONFIG_CSO
PROGRAM_B_2 AF3 PROGRAM_B
PROGRAM_B 12
R17 4K7 1% 0402
R18 4K7 1% 0402
TEMP_SCLK
TEMP_SDA
R19 4K7 1% 0402
R20 4K7 1% 0402
TXC and RXC are clocks

Design Note:
Configuration mode :
SPI
M[1:0] = 01

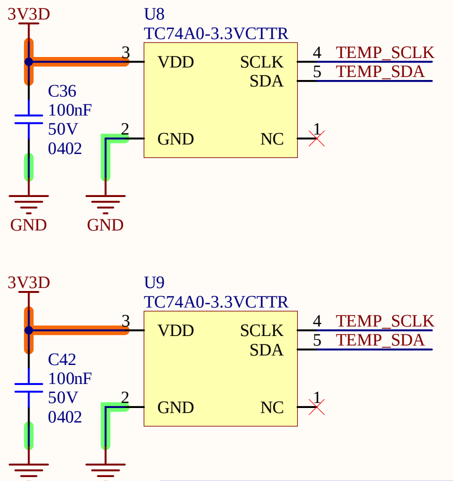
Current consumption
50mA @ VCCO_2 (3V3)

FPGA Bank 2 Decoupling Capacitors


3V3D
C37 100uF 6V3 1210
C38 4.7uF 6V3 0805
C39 470nF 6V3 0402
C40 470nF 6V3 0402
C41 470nF 6V3 0402
GND

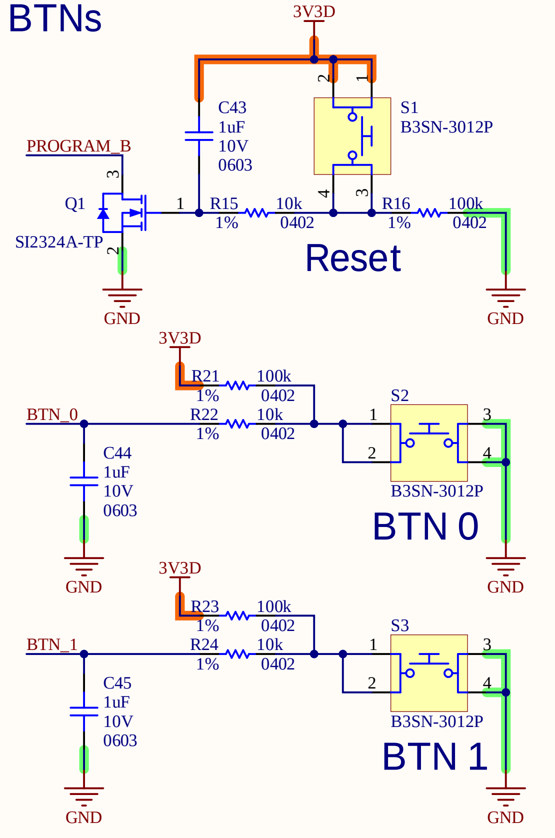
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Temperature sensors


3V3D
U8
TC74A0-3.3VCTTR
C36 100nF 50V 0402
VDD
SCLK
SDA
GND
NC
TEMP_SCLK
TEMP_SDA
GND
3V3D
U9
TC74A0-3.3VCTTR
C42 100nF 50V 0402
VDD
SCLK
SDA
GND
NC
TEMP_SCLK
TEMP_SDA
GND

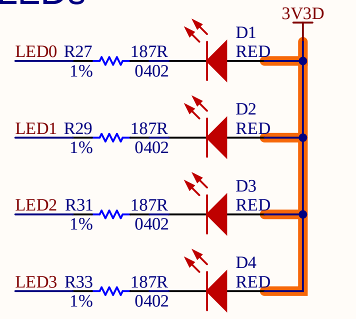
Current consumption
0.7mA @ VCCO_2 (3V3)

BTNs


3V3D
C43 1uF 10V 0603
S1 B3SN-3012P
PROGRAM_B
Q1
SI2324A-TP
R15 1% 10k 0402
R16 1% 100k 0402
Reset
GND
3V3D
R21 1% 100k 0402
R22 1% 10k 0402
BTN_0
C44 1uF 10V 0603
S2
B3SN-3012P
BTN 0
GND
3V3D
R23 1% 100k 0402
R24 1% 10k 0402
BTN_1
C45 1uF 10V 0603
S3
B3SN-3012P
BTN 1
GND

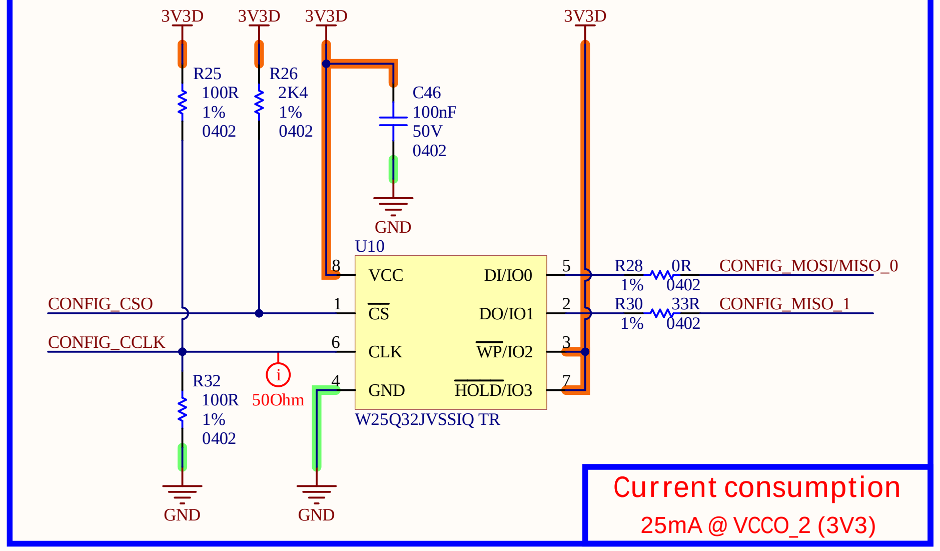
Design notes - Buttons
- Debounce time 100-500ms

LEDs


3V3D
LED0 R27 1% 187R 0402 D1 RED
LED1 R29 1% 187R 0402 D2 RED
LED2 R31 1% 187R 0402 D3 RED
LED3 R33 1% 187R 0402 D4 RED

Current consumption
32mA @ VCCO_2 (3V3)

Configuration FLASH


3V3D
R25 100R 1% 0402
R26 2K4 1% 0402
C46 100nF 50V 0402
GND
U10
VCC
CS
CLK
GND
DI/IO0
DO/IO1
WP/IO2
HOLD/IO3
W25Q32JVSSIQ TR
CONFIG_CSO
CONFIG_CCLK
R32 100R 1% 0402
50Ohm
R28 1% 0R 0402
R30 1% 33R 0402
CONFIG_MOSI/MISO_0
CONFIG_MISO_1
GND

Current consumption
25mA @ VCCO_2 (3V3)

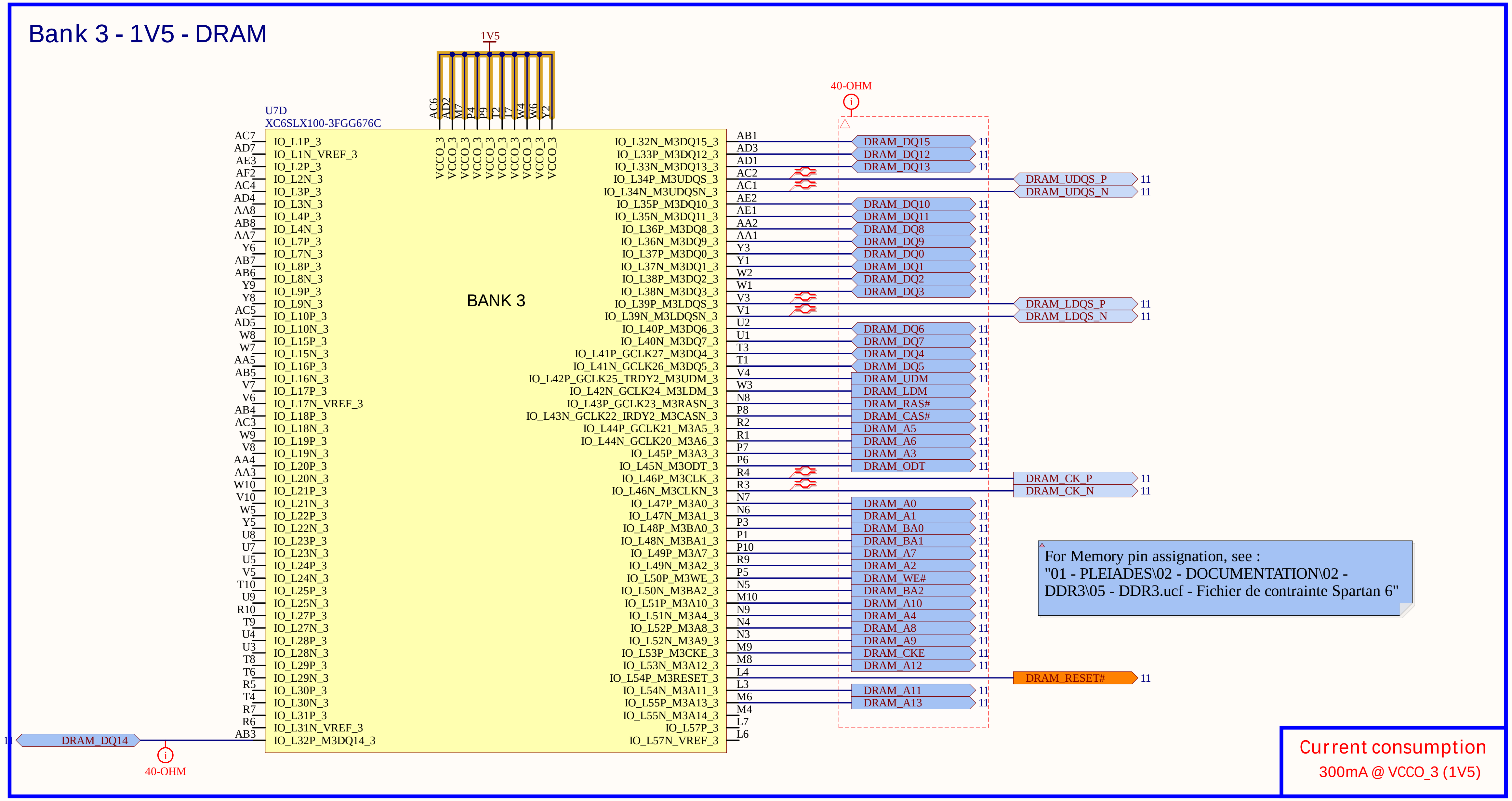
Design Note:
FPGA/FLASH power sequence:
FLASH must ready to operate when FPGA starts programing
- FLASH delays:
  - Read : 20us after VCCmin (2V7)
  - Write : 5ms after VWI (1V to 2V)
- FPGA delay :
  - Tpor : 5ms
  - VCCINT : 60ms

Design Note:
A series resistor should be considered for the datapath from the flash to the FPGA to minimize overshoot. The proper resistor value can be determined from simulation.

Design Note:
CCLK teminate with:
2x Zo = 2x50Ohm = 100Ohm to VCC and GND

Sheet Name	FPGA_2		
Project Title	P07		
Global Project	*Radio reconfigurable*		
Size 11x17	Group Ultracom		Revision 1.000
Date	2021-01-13	Sheet	6 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_2.SchDoc	Designers	Philippe Arsenault Louis-Daniel Gaulin

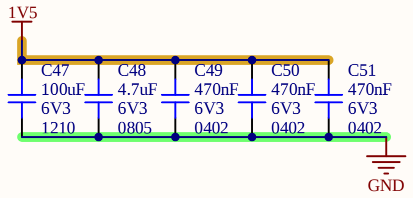
Bank 3 - 1V5 - DRAM


U7D
XC6SLX100-3FGG676C
BANK 3
1V5
AC6 AD2 M7 P4 P9 T2 T7 W4 W6 Y2
VCCO_3
40-OHM
AC7 IO_L1P_3
AD7 IO_L1N_VREF_3
AE3 IO_L2P_3
AF2 IO_L2N_3
AC4 IO_L3P_3
AD4 IO_L3N_3
AA8 IO_L4P_3
AB8 IO_L4N_3
AA7 IO_L7P_3
Y6 IO_L7N_3
AB7 IO_L8P_3
AB6 IO_L8N_3
Y9 IO_L9P_3
Y8 IO_L9N_3
AC5 IO_L10P_3
AD5 IO_L10N_3
W8 IO_L15P_3
W7 IO_L15N_3
AA5 IO_L16P_3
AB5 IO_L16N_3
V7 IO_L17P_3
V6 IO_L17N_VREF_3
AB4 IO_L18P_3
AC3 IO_L18N_3
W9 IO_L19P_3
V8 IO_L19N_3
AA4 IO_L20P_3
AA3 IO_L20N_3
W10 IO_L21P_3
V10 IO_L21N_3
W5 IO_L22P_3
Y5 IO_L22N_3
U8 IO_L23P_3
U7 IO_L23N_3
U5 IO_L24P_3
V5 IO_L24N_3
T10 IO_L25P_3
U9 IO_L25N_3
R10 IO_L27P_3
T9 IO_L27N_3
U4 IO_L28P_3
U3 IO_L28N_3
T8 IO_L29P_3
T6 IO_L29N_3
R5 IO_L30P_3
T4 IO_L30N_3
R7 IO_L31P_3
R6 IO_L31N_VREF_3
AB3 IO_L32P_M3DQ14_3 DRAM_DQ14 1
40-OHM
IO_L32N_M3DQ15_3 AB1 DRAM_DQ15 11
IO_L33P_M3DQ12_3 AD3 DRAM_DQ12 11
IO_L33N_M3DQ13_3 AD1 DRAM_DQ13 11
IO_L34P_M3UDQS_3 AC2 DRAM_UDQS_P 11
IO_L34N_M3UDQSN_3 AC1 DRAM_UDQS_N 11
IO_L35P_M3DQ10_3 AE2 DRAM_DQ10 11
IO_L35N_M3DQ11_3 AE1 DRAM_DQ11 11
IO_L36P_M3DQ8_3 AA2 DRAM_DQ8 11
IO_L36N_M3DQ9_3 AA1 DRAM_DQ9 11
IO_L37P_M3DQ0_3 Y3 DRAM_DQ0 11
IO_L37N_M3DQ1_3 Y1 DRAM_DQ1 11
IO_L38P_M3DQ2_3 W2 DRAM_DQ2 11
IO_L38N_M3DQ3_3 W1 DRAM_DQ3 11
IO_L39P_M3LDQS_3 V3 DRAM_LDQS_P 11
IO_L39N_M3LDQSN_3 V1 DRAM_LDQS_N 11
IO_L40P_M3DQ6_3 U2 DRAM_DQ6 11
IO_L40N_M3DQ7_3 U1 DRAM_DQ7 11
IO_L41P_GCLK27_M3DQ4_3 T3 DRAM_DQ4 11
IO_L41N_GCLK26_M3DQ5_3 T1 DRAM_DQ5 11
IO_L42P_GCLK25_TRDY2_M3UDM_3 V4 DRAM_UDM 11
IO_L42N_GCLK24_M3LDM_3 W3 DRAM_LDM
IO_L43P_GCLK23_M3RASN_3 N8 DRAM_RAS# 11
IO_L43N_GCLK22_IRDY2_M3CASN_3 P8 DRAM_CAS# 11
IO_L44P_GCLK21_M3A5_3 R2 DRAM_A5 11
IO_L44N_GCLK20_M3A6_3 R1 DRAM_A6 11
IO_L45P_M3A3_3 P7 DRAM_A3 11
IO_L45N_M3ODT_3 P6 DRAM_ODT 11
IO_L46P_M3CLK_3 R4 DRAM_CK_P 11
IO_L46N_M3CLKN_3 R3 DRAM_CK_N 11
IO_L47P_M3A0_3 N7 DRAM_A0 11
IO_L47N_M3A1_3 N6 DRAM_A1 11
IO_L48P_M3BA0_3 P3 DRAM_BA0 11
IO_L48N_M3BA1_3 P1 DRAM_BA1 11
IO_L49P_M3A7_3 P10 DRAM_A7 11
IO_L49N_M3A2_3 R9 DRAM_A2 11
IO_L50P_M3WE_3 P5 DRAM_WE# 11
IO_L50N_M3BA2_3 N5 DRAM_BA2 11
IO_L51P_M3A10_3 M10 DRAM_A10 11
IO_L51N_M3A4_3 N9 DRAM_A4 11
IO_L52P_M3A8_3 N4 DRAM_A8 11
IO_L52N_M3A9_3 N3 DRAM_A9 11
IO_L53P_M3CKE_3 M9 DRAM_CKE 11
IO_L53N_M3A12_3 M8 DRAM_A12 11
IO_L54P_M3RESET_3 L4 DRAM_RESET# 11
IO_L54N_M3A11_3 L3 DRAM_A11 11
IO_L55P_M3A13_3 M6 DRAM_A13 11
IO_L55N_M3A14_3 M4
IO_L57P_3 L7
IO_L57N_VREF_3 L6

For Memory pin assignation, see :
"01 - PLEIADES\02 - DOCUMENTATION\02 - DDR3\05 - DDR3.ucf - Fichier de contrainte Spartan 6"

Current consumption
300mA @ VCCO_3 (1V5)

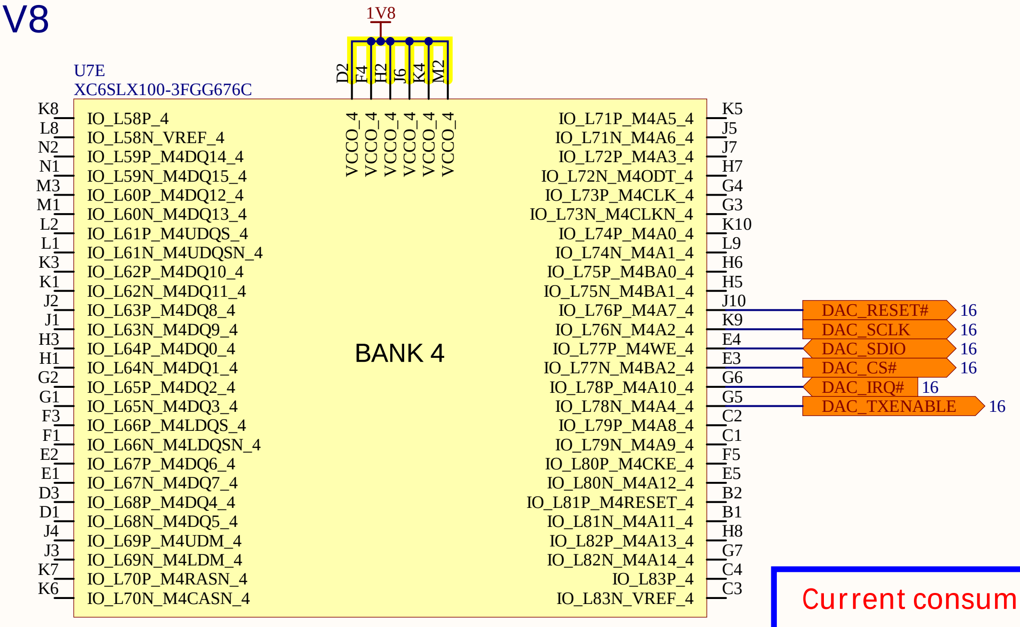
FPGA Bank 3 Decoupling Capacitors


1V5
C47 100uF 6V3 1210
C48 4.7uF 6V3 0805
C49 470nF 6V3 0402
C50 470nF 6V3 0402
C51 470nF 6V3 0402
GND

Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Sheet Name	FPGA_3
Project Title	P07
Global Project	*Radio reconfigurable*
Size	11x17
Group	Ultracom
Revision	1.000
Date	2021-01-13
Sheet	7 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_3.SchDoc
Designers	Philippe Arsenault Louis-Daniel Gaulin

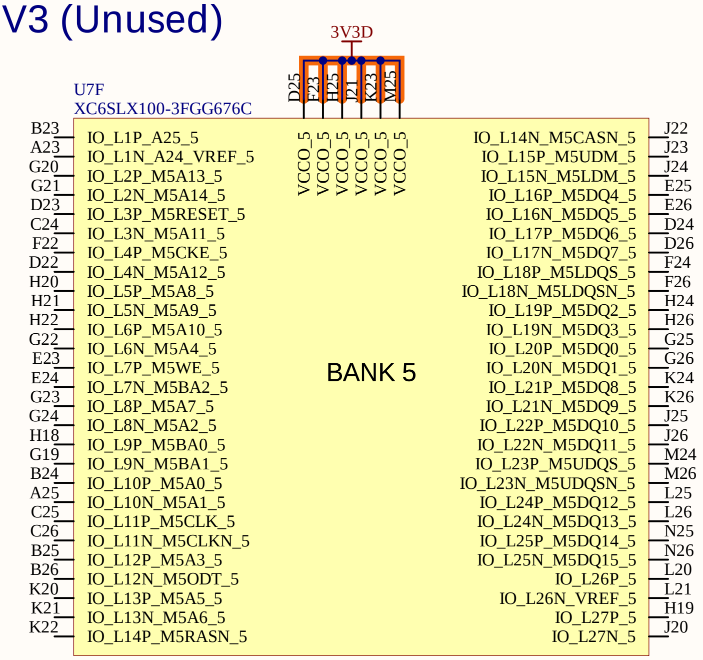
Bank 4 - 1V8


1V8
U7E
XC6SLX100-3FGG676C
D2
F4
H2
J6
K4
M2
VCCO_4
VCCO_4
VCCO_4
VCCO_4
VCCO_4
VCCO_4
K8 IO_L58P_4
L8 IO_L58N_VREF_4
N2 IO_L59P_M4DQ14_4
N1 IO_L59N_M4DQ15_4
M3 IO_L60P_M4DQ12_4
M1 IO_L60N_M4DQ13_4
L2 IO_L61P_M4UDQS_4
L1 IO_L61N_M4UDQSN_4
K3 IO_L62P_M4DQ10_4
K1 IO_L62N_M4DQ11_4
J2 IO_L63P_M4DQ8_4
J1 IO_L63N_M4DQ9_4
H3 IO_L64P_M4DQ0_4
H1 IO_L64N_M4DQ1_4
G2 IO_L65P_M4DQ2_4
G1 IO_L65N_M4DQ3_4
F3 IO_L66P_M4LDQS_4
F1 IO_L66N_M4LDQSN_4
E2 IO_L67P_M4DQ6_4
E1 IO_L67N_M4DQ7_4
D3 IO_L68P_M4DQ4_4
D1 IO_L68N_M4DQ5_4
J4 IO_L69P_M4UDM_4
J3 IO_L69N_M4LDM_4
K7 IO_L70P_M4RASN_4
K6 IO_L70N_M4CASN_4
BANK 4
IO_L71P_M4A5_4 K5
IO_L71N_M4A6_4 J5
IO_L72P_M4A3_4 J7
IO_L72N_M4ODT_4 H7
IO_L73P_M4CLK_4 G4
IO_L73N_M4CLKN_4 G3
IO_L74P_M4A0_4 K10
IO_L74N_M4A1_4 L9
IO_L75P_M4BA0_4 H6
IO_L75N_M4BA1_4 H5
IO_L76P_M4A7_4 J10 DAC_RESET# 16
IO_L76N_M4A2_4 K9 DAC_SCLK 16
IO_L77P_M4WE_4 E4 DAC_SDIO 16
IO_L77N_M4BA2_4 E3 DAC_CS# 16
IO_L78P_M4A10_4 G6 DAC_IRQ# 16
IO_L78N_M4A4_4 G5 DAC_TXENABLE 16
IO_L79P_M4A8_4 C2
IO_L79N_M4A9_4 C1
IO_L80P_M4CKE_4 F5
IO_L80N_M4A12_4 E5
IO_L81P_M4RESET_4 B2
IO_L81N_M4A11_4 B1
IO_L82P_M4A13_4 H8
IO_L82N_M4A14_4 G7
IO_L83P_4 C4
IO_L83N_VREF_4 C3

Current consumption

50mA @ VCCO_4 (1V8)

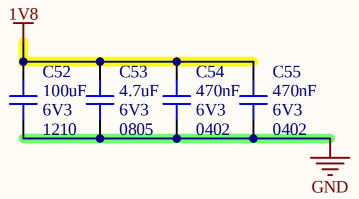
Bank 5 - 3V3 (Unused)


3V3D
U7F
XC6SLX100-3FGG676C
D25
F23
H25
J21
K23
M25
VCCO_5
VCCO_5
VCCO_5
VCCO_5
VCCO_5
VCCO_5
B23 IO_L1P_A25_5
A23 IO_L1N_A24_VREF_5
G20 IO_L2P_M5A13_5
G21 IO_L2N_M5A14_5
D23 IO_L3P_M5RESET_5
C24 IO_L3N_M5A11_5
F22 IO_L4P_M5CKE_5
D22 IO_L4N_M5A12_5
H20 IO_L5P_M5A8_5
H21 IO_L5N_M5A9_5
H22 IO_L6P_M5A10_5
G22 IO_L6N_M5A4_5
E23 IO_L7P_M5WE_5
E24 IO_L7N_M5BA2_5
G23 IO_L8P_M5A7_5
G24 IO_L8N_M5A2_5
H18 IO_L9P_M5BA0_5
G19 IO_L9N_M5BA1_5
B24 IO_L10P_M5A0_5
A25 IO_L10N_M5A1_5
C25 IO_L11P_M5CLK_5
C26 IO_L11N_M5CLKN_5
B25 IO_L12P_M5A3_5
B26 IO_L12N_M5ODT_5
K20 IO_L13P_M5A5_5
K21 IO_L13N_M5A6_5
K22 IO_L14P_M5RASN_5
BANK 5
IO_L14N_M5CASN_5 J22
IO_L15P_M5UDM_5 J23
IO_L15N_M5LDM_5 J24
IO_L16P_M5DQ4_5 E25
IO_L16N_M5DQ5_5 E26
IO_L17P_M5DQ6_5 D24
IO_L17N_M5DQ7_5 D26
IO_L18P_M5LDQS_5 F24
IO_L18N_M5LDQSN_5 F26
IO_L19P_M5DQ2_5 H24
IO_L19N_M5DQ3_5 H26
IO_L20P_M5DQ0_5 G25
IO_L20N_M5DQ1_5 G26
IO_L21P_M5DQ8_5 K24
IO_L21N_M5DQ9_5 K26
IO_L22P_M5DQ10_5 J25
IO_L22N_M5DQ11_5 J26
IO_L23P_M5UDQS_5 M24
IO_L23N_M5UDQSN_5 M26
IO_L24P_M5DQ12_5 L25
IO_L24N_M5DQ13_5 L26
IO_L25P_M5DQ14_5 N25
IO_L25N_M5DQ15_5 N26
IO_L26P_5 L20
IO_L26N_VREF_5 L21
IO_L27P_5 H19
IO_L27N_5 J20

Current consumption

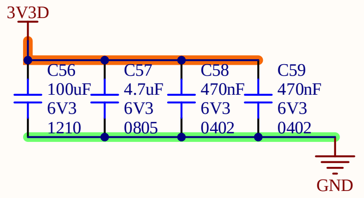
50mA @ VCCO_5 (3V3)

FPGA Bank 4 Decoupling Capacitors


1V8
C52
100uF
6V3
1210
C53
4.7uF
6V3
0805
C54
470nF
6V3
0402
C55
470nF
6V3
0402
GND

Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

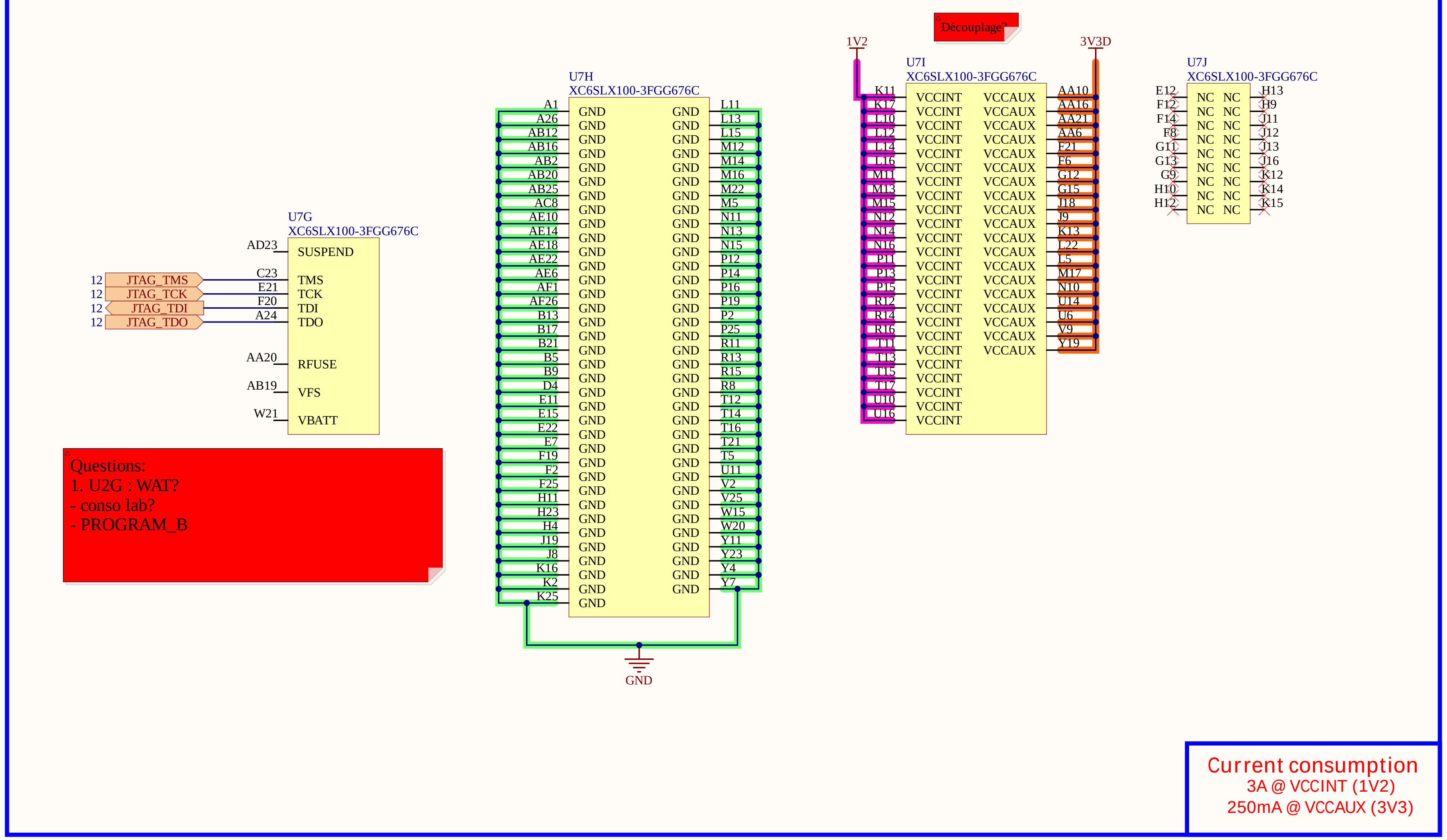
FPGA Bank 5 Decoupling Capacitors


3V3D
C56
100uF
6V3
1210
C57
4.7uF
6V3
0805
C58
470nF
6V3
0402
C59
470nF
6V3
0402
GND

Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Sheet Name FPGA_4
Project Title P07
Global Project *Radio reconfigurable*
Size 11x17
Group Ultracom
Revision 1.000
Date 2021-01-13
Sheet 8 of 16
Filename S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_4-5.SchDoc
Designers Philippe Arsenault
Louis-Daniel Gaulin

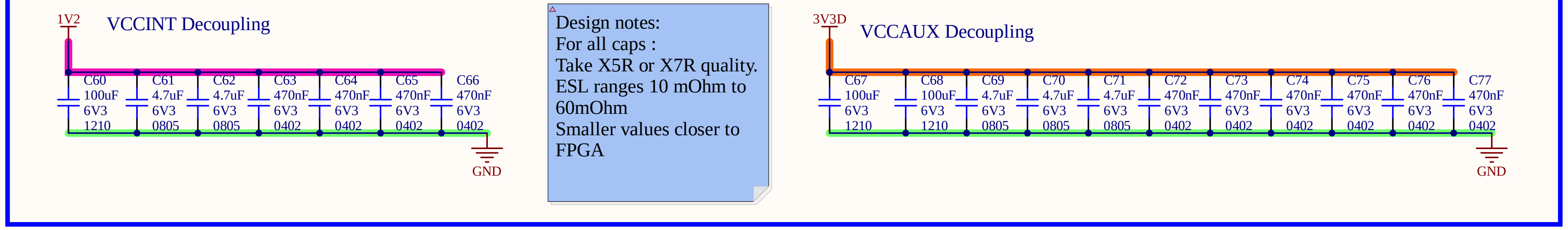
FPGA Power Parts


U7G
XC6SLX100-3FGG676C
AD23 SUSPEND
12 JTAG_TMS C23 TMS
12 JTAG_TCK E21 TCK
12 JTAG_TDI F20 TDI
12 JTAG_TDO A24 TDO
AA20 RFUSE
AB19 VFS
W21 VBATT
U7H
XC6SLX100-3FGG676C
GND
A1 A26 AB12 AB16 AB2 AB20 AB25 AC8 AE10 AE14 AE18 AE22 AE6 AF1 AF26 B13 B17 B21 B5 B9 D4 E11 E15 E22 E7 F19 F2 F25 H11 H23 H4 J19 J8 K16 K2 K25
L11 L13 L15 M12 M14 M16 M22 M5 N11 N13 N15 P12 P14 P16 P19 P2 P25 R11 R13 R15 R8 T12 T14 T16 T21 T5 U11 V2 V25 W15 W20 Y11 Y23 Y4 Y7
GND
Decouplage
1V2
3V3D
U7I
XC6SLX100-3FGG676C
VCCINT
K11 K17 L10 L12 L14 L16 M11 M13 M15 N12 N14 N16 P11 P13 P15 R12 R14 R16 T11 T13 T15 T17 U10 U16
VCCAUX
AA10 AA16 AA21 AA6 F21 F6 G12 G15 J18 J9 K13 L22 L5 M17 N10 U14 U6 V9 Y19
U7J
XC6SLX100-3FGG676C
NC
E12 F12 F14 F8 G11 G13 G9 H10 H12
H13 H9 J11 J12 J13 J16 K12 K14 K15

Questions:
1. U2G : WAT?
- conso lab?
- PROGRAM_B

Current consumption
3A @ VCCINT (1V2)
250mA @ VCCAUX (3V3)

FPGA Decoupling Capacitors


1V2
VCCINT Decoupling
C60 100uF 6V3 1210
C61 4.7uF 6V3 0805
C62 4.7uF 6V3 0805
C63 470nF 6V3 0402
C64 470nF 6V3 0402
C65 470nF 6V3 0402
C66 470nF 6V3 0402
GND
3V3D
VCCAUX Decoupling
C67 100uF 6V3 1210
C68 100uF 6V3 1210
C69 4.7uF 6V3 0805
C70 4.7uF 6V3 0805
C71 4.7uF 6V3 0805
C72 470nF 6V3 0402
C73 470nF 6V3 0402
C74 470nF 6V3 0402
C75 470nF 6V3 0402
C76 470nF 6V3 0402
C77 470nF 6V3 0402
GND

Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Sheet Name
FPGA_MISC

Project Title
P07

Global Project
Radio reconfigurable

Size 11x17
Group Ultracom
Revision 1.000

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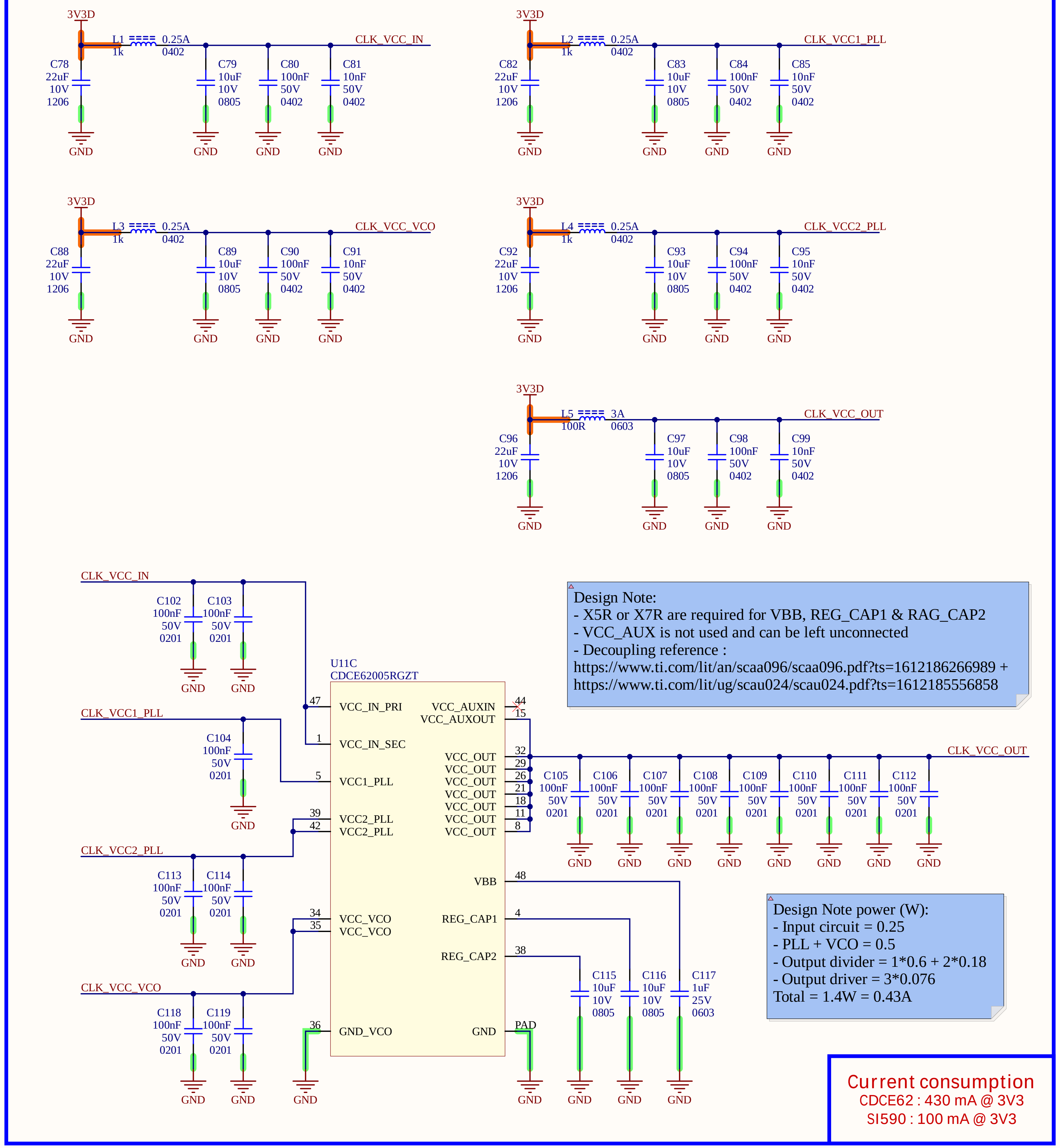
Sheet 9 of 16

Filename
S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_MISC.SchDoc

Designers
Philippe Arsenault
Louis-Daniel Gaulin

Clock power

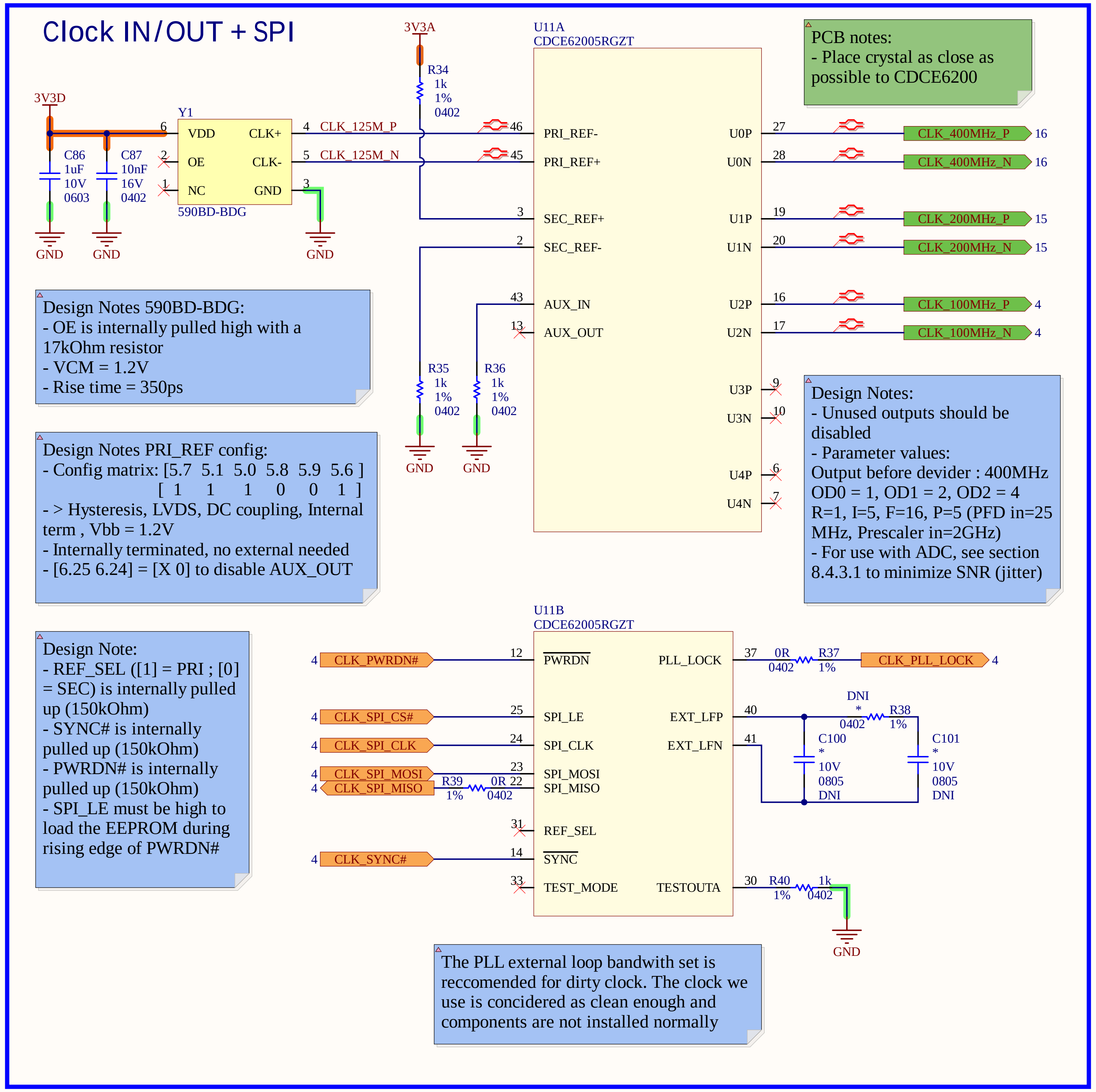

3V3D
L1 1k 0.25A 0402
CLK_VCC_IN
C78 22uF 10V 1206
C79 10uF 10V 0805
C80 100nF 50V 0402
C81 10nF 50V 0402
L2 1k 0.25A 0402
CLK_VCC1_PLL
C82 22uF 10V 1206
C83 10uF 10V 0805
C84 100nF 50V 0402
C85 10nF 50V 0402
L3 1k 0.25A 0402
CLK_VCC_VCO
C88 22uF 10V 1206
C89 10uF 10V 0805
C90 100nF 50V 0402
C91 10nF 50V 0402
L4 1k 0.25A 0402
CLK_VCC2_PLL
C92 22uF 10V 1206
C93 10uF 10V 0805
C94 100nF 50V 0402
C95 10nF 50V 0402
L5 100R 3A 0603
CLK_VCC_OUT
C96 22uF 10V 1206
C97 10uF 10V 0805
C98 100nF 50V 0402
C99 10nF 50V 0402
GND
C102 100nF 50V 0201
C103 100nF 50V 0201
C104 100nF 50V 0201
C113 100nF 50V 0201
C114 100nF 50V 0201
C118 100nF 50V 0201
C119 100nF 50V 0201
U11C
CDCE62005RGZT
47 VCC_IN_PRI
1 VCC_IN_SEC
5 VCC1_PLL
39 VCC2_PLL
42 VCC2_PLL
34 VCC_VCO
35 VCC_VCO
36 GND_VCO
VCC_AUXIN 44
VCC_AUXOUT 15
VCC_OUT 32
VCC_OUT 29
VCC_OUT 26
VCC_OUT 21
VCC_OUT 18
VCC_OUT 11
VCC_OUT 8
VBB 48
REG_CAP1 4
REG_CAP2 38
GND PAD
C105 100nF 50V 0201
C106 100nF 50V 0201
C107 100nF 50V 0201
C108 100nF 50V 0201
C109 100nF 50V 0201
C110 100nF 50V 0201
C111 100nF 50V 0201
C112 100nF 50V 0201
C115 10uF 10V 0805
C116 10uF 10V 0805
C117 1uF 25V 0603

Design Note:
- X5R or X7R are required for VBB, REG_CAP1 & RAG_CAP2
- VCC_AUX is not used and can be left unconnected
- Decoupling reference :
https://www.ti.com/lit/an/scaa096/scaa096.pdf?ts=1612186266989 +
https://www.ti.com/lit/ug/scau024/scau024.pdf?ts=1612185556858

Design Note power (W):
- Input circuit = 0.25
- PLL + VCO = 0.5
- Output divider = 1*0.6 + 2*0.18
- Output driver = 3*0.076
Total = 1.4W = 0.43A

Current consumption
CDCE62 : 430 mA @ 3V3
SI590 : 100 mA @ 3V3

Clock IN/OUT + SPI


3V3A
R34 1k 1% 0402
U11A
CDCE62005RGZT
3V3D
Y1
6 VDD
2 OE
1 NC
CLK+ 4
CLK- 5
GND 3
590BD-BDG
C86 1uF 10V 0603
C87 10nF 16V 0402
CLK_125M_P
CLK_125M_N
46 PRI_REF-
45 PRI_REF+
3 SEC_REF+
2 SEC_REF-
43 AUX_IN
13 AUX_OUT
R35 1k 1% 0402
R36 1k 1% 0402
U0P 27
U0N 28
U1P 19
U1N 20
U2P 16
U2N 17
U3P 9
U3N 10
U4P 6
U4N 7
CLK_400MHz_P 16
CLK_400MHz_N 16
CLK_200MHz_P 15
CLK_200MHz_N 15
CLK_100MHz_P 4
CLK_100MHz_N 4
GND
U11B
CDCE62005RGZT
4 CLK_PWRDN# 12 PWRDN
4 CLK_SPI_CS# 25 SPI_LE
4 CLK_SPI_CLK 24 SPI_CLK
4 CLK_SPI_MOSI 23 SPI_MOSI
4 CLK_SPI_MISO R39 0R 1% 0402 22 SPI_MISO
31 REF_SEL
4 CLK_SYNC# 14 SYNC
33 TEST_MODE
PLL_LOCK 37
0R R37 0402 1%
CLK_PLL_LOCK 4
EXT_LFP 40
EXT_LFN 41
DNI
* R38 0402 1%
C100 * 10V 0805 DNI
C101 * 10V 0805 DNI
TESTOUTA 30
R40 1% 1k 0402

PCB notes:
- Place crystal as close as possible to CDCE6200

Design Notes 590BD-BDG:
- OE is internally pulled high with a 17kOhm resistor
- VCM = 1.2V
- Rise time = 350ps

Design Notes PRI_REF config:
- Config matrix: [5.7 5.1 5.0 5.8 5.9 5.6]
[1 1 1 0 0 1]
- > Hysteresis, LVDS, DC coupling, Internal term , Vbb = 1.2V
- Internally terminated, no external needed
- [6.25 6.24] = [X 0] to disable AUX_OUT

Design Notes:
- Unused outputs should be disabled
- Parameter values:
Output before devider : 400MHz
OD0 = 1, OD1 = 2, OD2 = 4
R=1, I=5, F=16, P=5 (PFD in=25 MHz, Prescaler in=2GHz)
- For use with ADC, see section 8.4.3.1 to minimize SNR (jitter)

Design Note:
- REF_SEL ([1] = PRI ; [0] = SEC) is internally pulled up (150kOhm)
- SYNC# is internally pulled up (150kOhm)
- PWRDN# is internally pulled up (150kOhm)
- SPI_LE must be high to load the EEPROM during rising edge of PWRDN#

The PLL external loop bandwith set is reccomended for dirty clock. The clock we use is concidered as clean enough and components are not installed normally

Sheet Name
CLOCK

Project Title
P07

Global Project
Radio reconfigurable

Size
11x17

Group
Ultracom

Revision
1.000

Date
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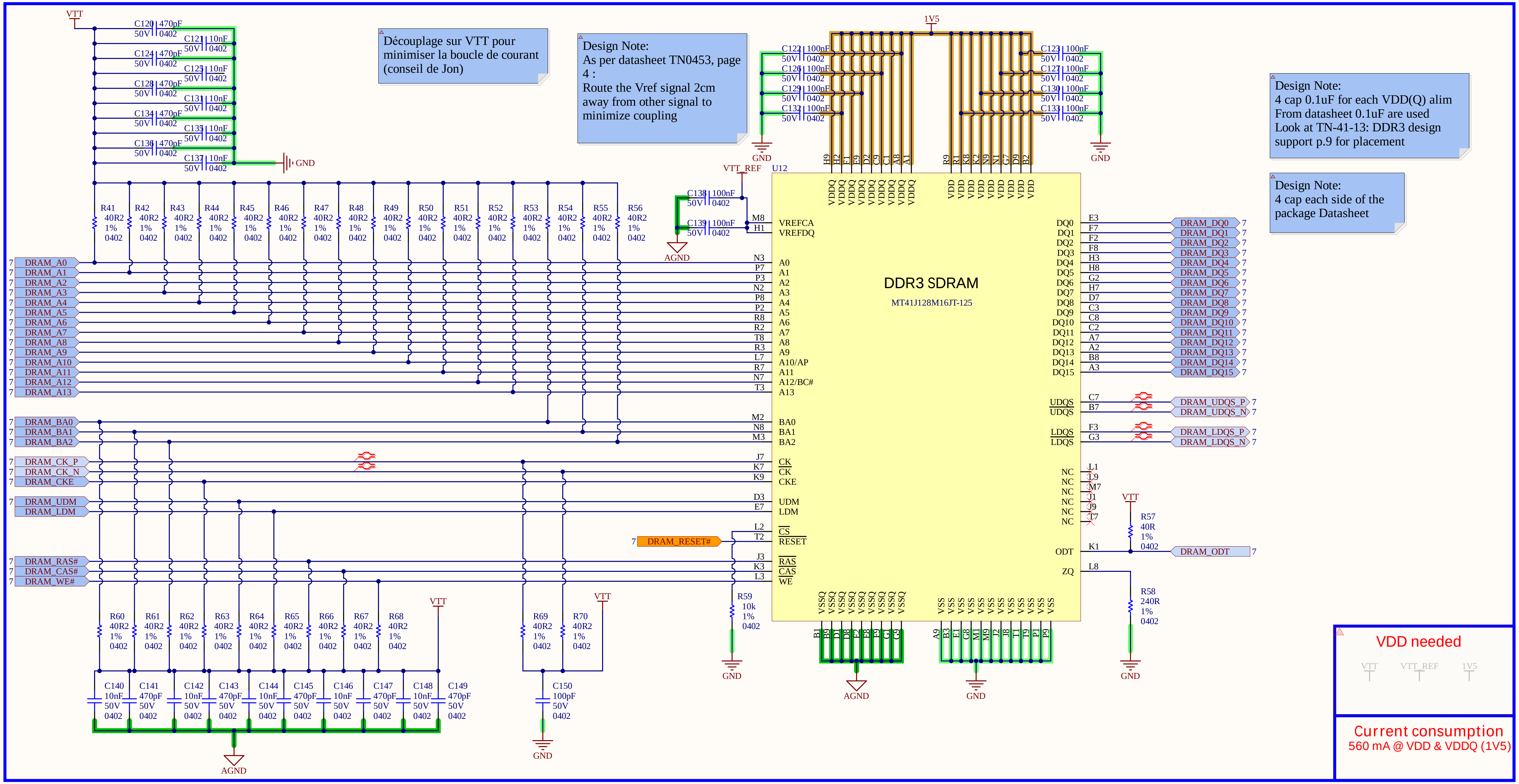
Filename
S7CAS-PLEIADES-CARTE-MERE_P07_CLOCK.SchDoc

Designers
Philippe Arsenault
Louis-Daniel Gaulin


VTT
GND
AGND
1V5
VTT_REF
U12
DDR3 SDRAM
MT41J128M16JT-125
VREFCA
VREFDQ
DRAM_A0 … DRAM_A13
DRAM_BA0
DRAM_BA1
DRAM_BA2
DRAM_CK_P
DRAM_CK_N
DRAM_CKE
DRAM_UDM
DRAM_LDM
DRAM_RAS#
DRAM_CAS#
DRAM_WE#
DRAM_RESET#
DRAM_DQ0 … DRAM_DQ15
DRAM_UDQS_P
DRAM_UDQS_N
DRAM_LDQS_P
DRAM_LDQS_N
DRAM_ODT
ODT
ZQ
RESET
R41 … R56 40R2 1% 0402
R60 … R68 40R2 1% 0402
R69 40R2 1% 0402
R70 40R2 1% 0402
R57 40R 1% 0402
R58 240R 1% 0402
R59 10k 1% 0402
C120 … C137 470pF / 10nF 50V 0402
C122 … C133 100nF 50V 0402
C138 100nF 50V 0402
C139 100nF 50V 0402
C140 … C149 10nF / 470pF 50V 0402
C150 100pF 50V 0402

Découplage sur VTT pour minimiser la boucle de courant (conseil de Jon)

Design Note:
As per datasheet TN0453, page 4 :
Route the Vref signal 2cm away from other signal to minimize coupling

Design Note:
4 cap 0.1uF for each VDD(Q) alim
From datasheet 0.1uF are used
Look at TN-41-13: DDR3 design support p.9 for placement

Design Note:
4 cap each side of the package Datasheet

VDD needed

VTT VTT_REF 1V5

Current consumption
560 mA @ VDD & VDDQ (1V5)

Design Note:
- Clock termination : 800MHz
CLK_P - 40Ohm - CAP to GND - 40Ohm - CLK_N
- Cap value:
Minimal impedance 0.2Ohm@ f = 814MHz
Value = 100pF
Ref:GRM1555C2A101JA01, murata sim

VTT must come after VDDQ

VTT transient current can be as high as ±3.5A during heavy activity on the DQ and address buses. This transient current averages 0A, but can be somewhat random in nature, depending upon address/data patterns.

Questions:
- Decouplage overkill ou pas
- Séparer GND
-Est-ce que le VTT_REF de la DDR a besoin d'avoir un ground analogique afin d'être stable? Et, question complémentaire, est-ce que le fait d'avoir un ground plus analogique (plus filtré, connecté aux circuits analogiques seulement) est une bonne idée?

- Dans la fiche de la DDR il est mentionné que les VTT Island devrait avoir un bulk cap de 100uF, Est-ce que nos condos sur le TPS51200 (3*10uF) et des plus petits plus proche de la DDR (3*10nF et 3* 470p) sont suffisant?

Sheet Name	DDR
Project Title	P07
Global Project	*Radio reconfigurable*
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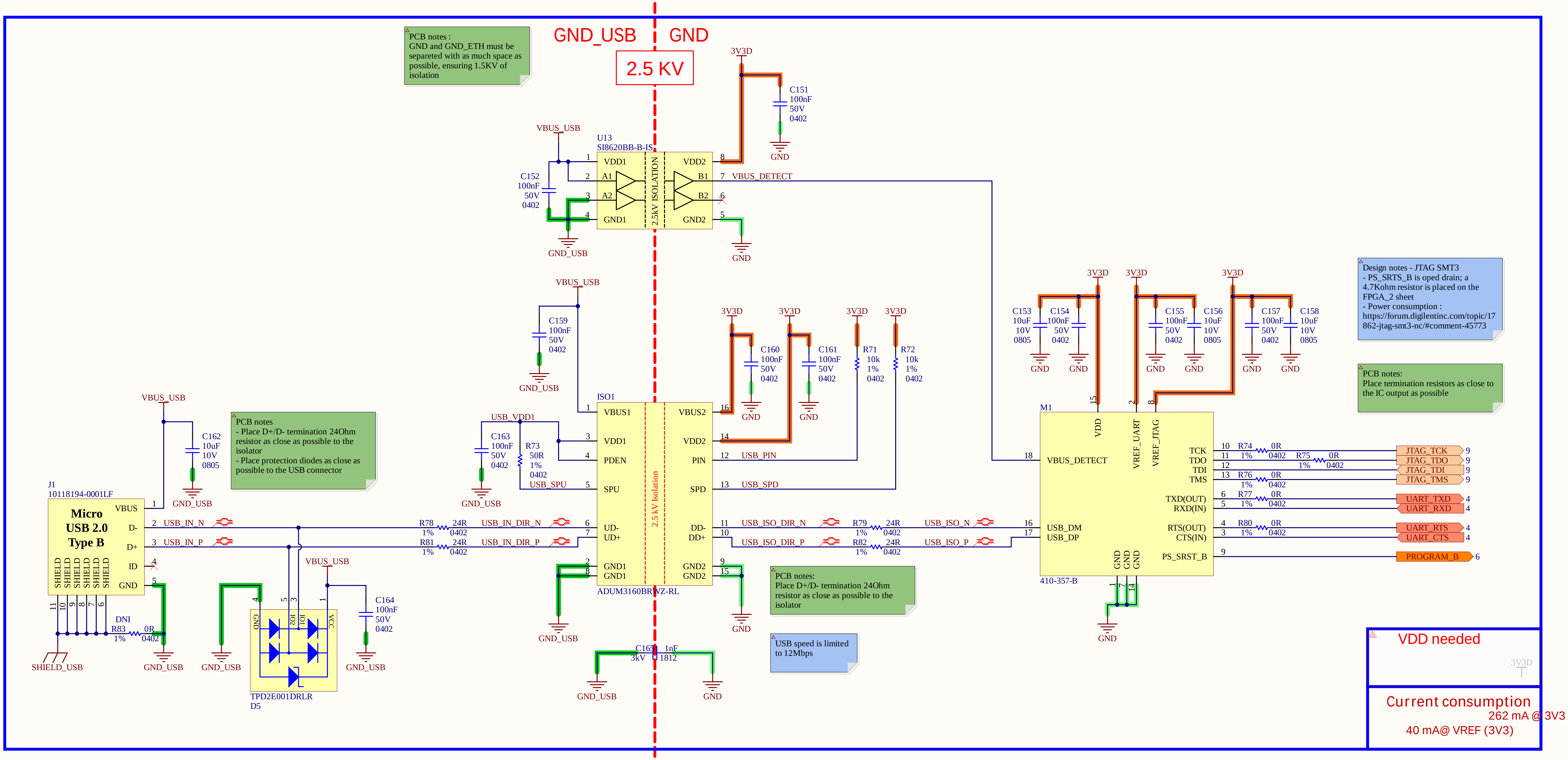
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_DDR.SchDoc
Designers	Philippe Arsenault Louis-Daniel Gaulin


GND_USB
GND
2.5 KV
3V3D
C151 100nF 50V 0402
VBUS_USB
U13 SI8620BB-B-IS
VDD1
A1
A2
GND1
2.5kV ISOLATION
VDD2
B1
B2
GND2
VBUS_DETECT
C152 100nF 50V 0402
ISO1
VBUS1
VDD1
PDEN
SPU
UD-
UD+
GND1
VBUS2
VDD2
PIN
SPD
DD-
DD+
GND2
2.5 kV Isolation
ADUM3160BRWZ-RL
USB_VDD1
USB_SPU
USB_PIN
USB_SPD
C159 100nF 50V 0402
C163 100nF 50V 0402
R73 50R 1% 0402
C160 100nF 50V 0402
C161 100nF 50V 0402
R71 10k 1% 0402
R72 10k 1% 0402
C165 1nF 3kV 1812
J1 10118194-0001LF
Micro USB 2.0 Type B
VBUS
D-
D+
ID
GND
SHIELD
SHIELD_USB
DNI R83 0R 1% 0402
C162 10uF 10V 0805
USB_IN_N
USB_IN_P
R78 24R 1% 0402
R81 24R 1% 0402
USB_IN_DIR_N
USB_IN_DIR_P
TPD2E001DRLR D5
GND IO2 IO1 VCC
C164 100nF 50V 0402
USB_ISO_DIR_N
USB_ISO_DIR_P
R79 24R 1% 0402
R82 24R 1% 0402
USB_ISO_N
USB_ISO_P
M1 410-357-B
VDD
VREF_UART
VREF_JTAG
VBUS_DETECT
USB_DM
USB_DP
TCK
TDO
TDI
TMS
TXD(OUT)
RXD(IN)
RTS(OUT)
CTS(IN)
PS_SRST_B
C153 10uF 10V 0805
C154 100nF 50V 0402
C155 100nF 50V 0402
C156 10uF 10V 0805
C157 100nF 50V 0402
C158 10uF 10V 0805
R74 0R 1% 0402
R75 0R 1% 0402
R76 0R 1% 0402
R77 0R 1% 0402
R80 0R 1% 0402
JTAG_TCK 9
JTAG_TDO 9
JTAG_TDI 9
JTAG_TMS 9
UART_TXD 4
UART_RXD 4
UART_RTS 4
UART_CTS 4
PROGRAM_B 6
VDD needed
3V3D

PCB notes :
GND and GND_ETH must be separeted with as much space as possible, ensuring 1.5KV of isolation

PCB notes
- Place D+/D- termination 24Ohm resistor as close as possible to the isolator
- Place protection diodes as close as possible to the USB connector

PCB notes:
Place D+/D- termination 24Ohm resistor as close as possible to the isolator

USB speed is limited to 12Mbps

Design notes - JTAG SMT3
- PS_SRTS_B is oped drain; a 4.7Kohm resistor is placed on the FPGA_2 sheet
- Power consumption :
https://forum.digilentinc.com/topic/17862-jtag-smt3-nc/#comment-45773

PCB notes:
Place termination resistors as close to the IC output as possible

Current consumption
262 mA @ 3V3
40 mA@ VREF (3V3)

Sheet Name
USB

Project Title
P07

Global Project
Radio reconfigurable

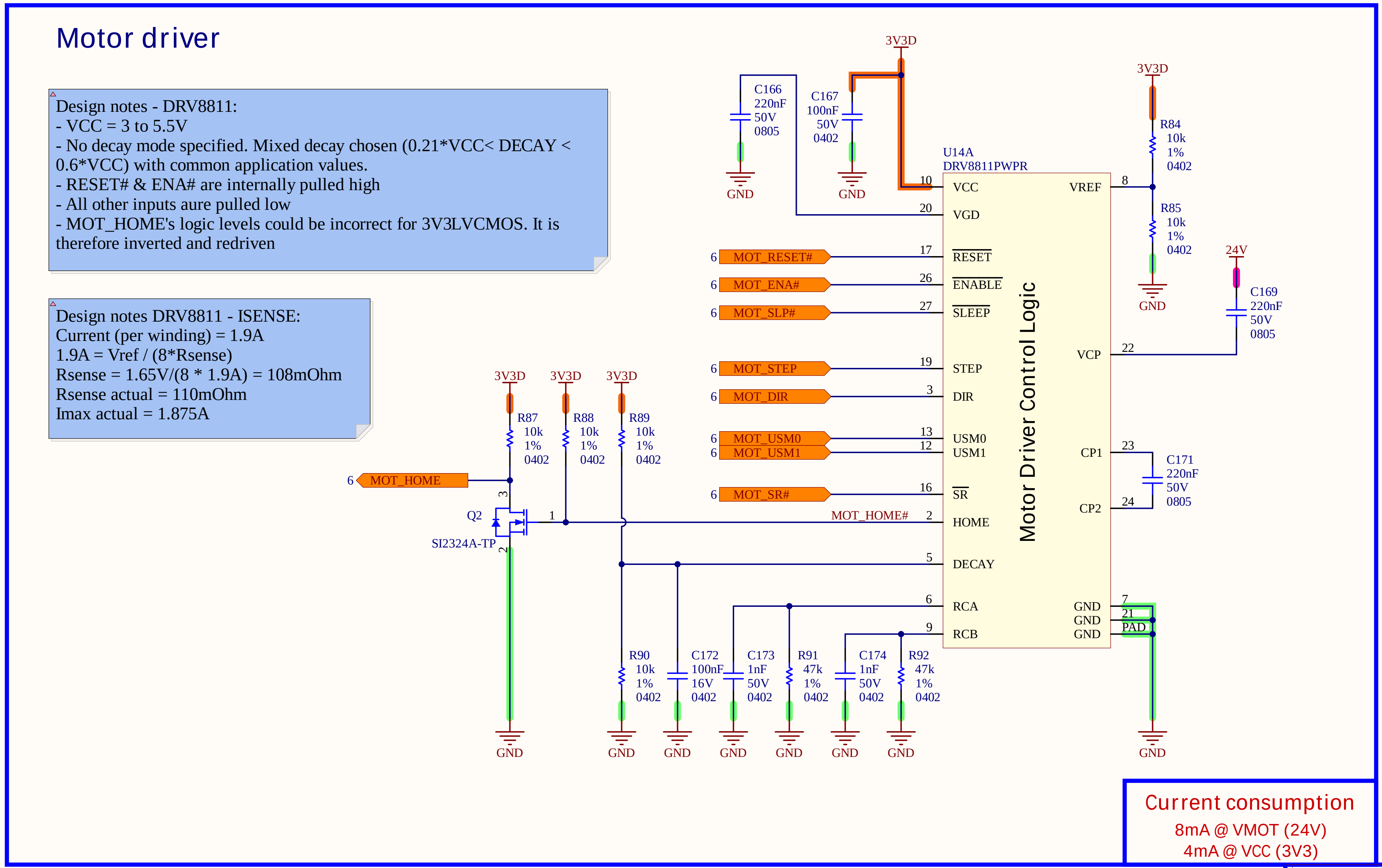
Size 11x17
Group Ultracom
Revision 1.000

Date 2021-01-13
Sheet 12 of 16

Filename
S7CAS-PLEIADES-CARTE-MERE_P07_USB.SchDoc

Designers
Philippe Arsenault
Louis-Daniel Gaulin

Motor driver

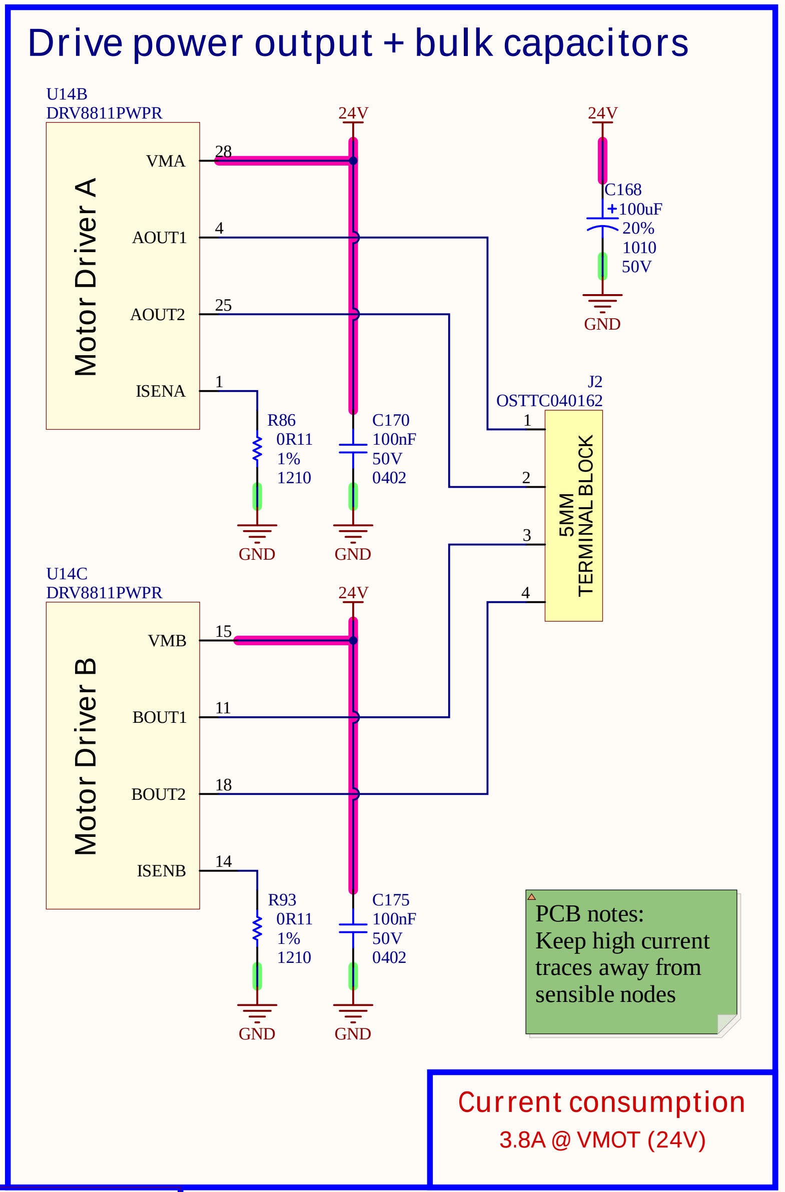

3V3D
C166
220nF
50V
0805
C167
100nF
50V
0402
GND
U14A
DRV8811PWPR
10 VCC
20 VGD
8 VREF
3V3D
R84
10k
1%
0402
R85
10k
1%
0402
24V
C169
220nF
50V
0805
22 VCP
6 MOT_RESET# 17 RESET
6 MOT_ENA# 26 ENABLE
6 MOT_SLP# 27 SLEEP
6 MOT_STEP 19 STEP
6 MOT_DIR 3 DIR
6 MOT_USM0 13 USM0
6 MOT_USM1 12 USM1
6 MOT_SR# 16 SR
MOT_HOME# 2 HOME
5 DECAY
6 RCA
9 RCB
Motor Driver Control Logic
23 CP1
24 CP2
C171
220nF
50V
0805
7 GND
21 GND
PAD GND
3V3D
R87
10k
1%
0402
R88
10k
1%
0402
R89
10k
1%
0402
6 MOT_HOME
Q2
SI2324A-TP
3
1
2
R90
10k
1%
0402
C172
100nF
16V
0402
C173
1nF
50V
0402
R91
47k
1%
0402
C174
1nF
50V
0402
R92
47k
1%
0402

Design notes - DRV8811:
- VCC = 3 to 5.5V
- No decay mode specified. Mixed decay chosen (0.21*VCC< DECAY < 0.6*VCC) with common application values.
- RESET# & ENA# are internally pulled high
- All other inputs aure pulled low
- MOT_HOME's logic levels could be incorrect for 3V3LVCMOS. It is therefore inverted and redriven

Design notes DRV8811 - ISENSE:
Current (per winding) = 1.9A
1.9A = Vref / (8*Rsense)
Rsense = 1.65V/(8 * 1.9A) = 108mOhm
Rsense actual = 110mOhm
Imax actual = 1.875A

Current consumption
8mA @ VMOT (24V)
4mA @ VCC (3V3)

Drive power output + bulk capacitors


U14B
DRV8811PWPR
Motor Driver A
28 VMA
4 AOUT1
25 AOUT2
1 ISENA
24V
R86
0R11
1%
1210
C170
100nF
50V
0402
GND
24V
C168
100uF
20%
1010
50V
J2
OSTTC040162
5MM TERMINAL BLOCK
1
2
3
4
U14C
DRV8811PWPR
Motor Driver B
15 VMB
11 BOUT1
18 BOUT2
14 ISENB
R93
0R11
1%
1210
C175
100nF
50V
0402

PCB notes:
Keep high current traces away from sensible nodes

Current consumption
3.8A @ VMOT (24V)

VDD needed
24V 3V3D

Sheet Name
MOT

Project Title
P07

Global Project
Radio reconfigurable

Size 11x17
Group Ultracom
Revision 1.000

Date 2021-01-13
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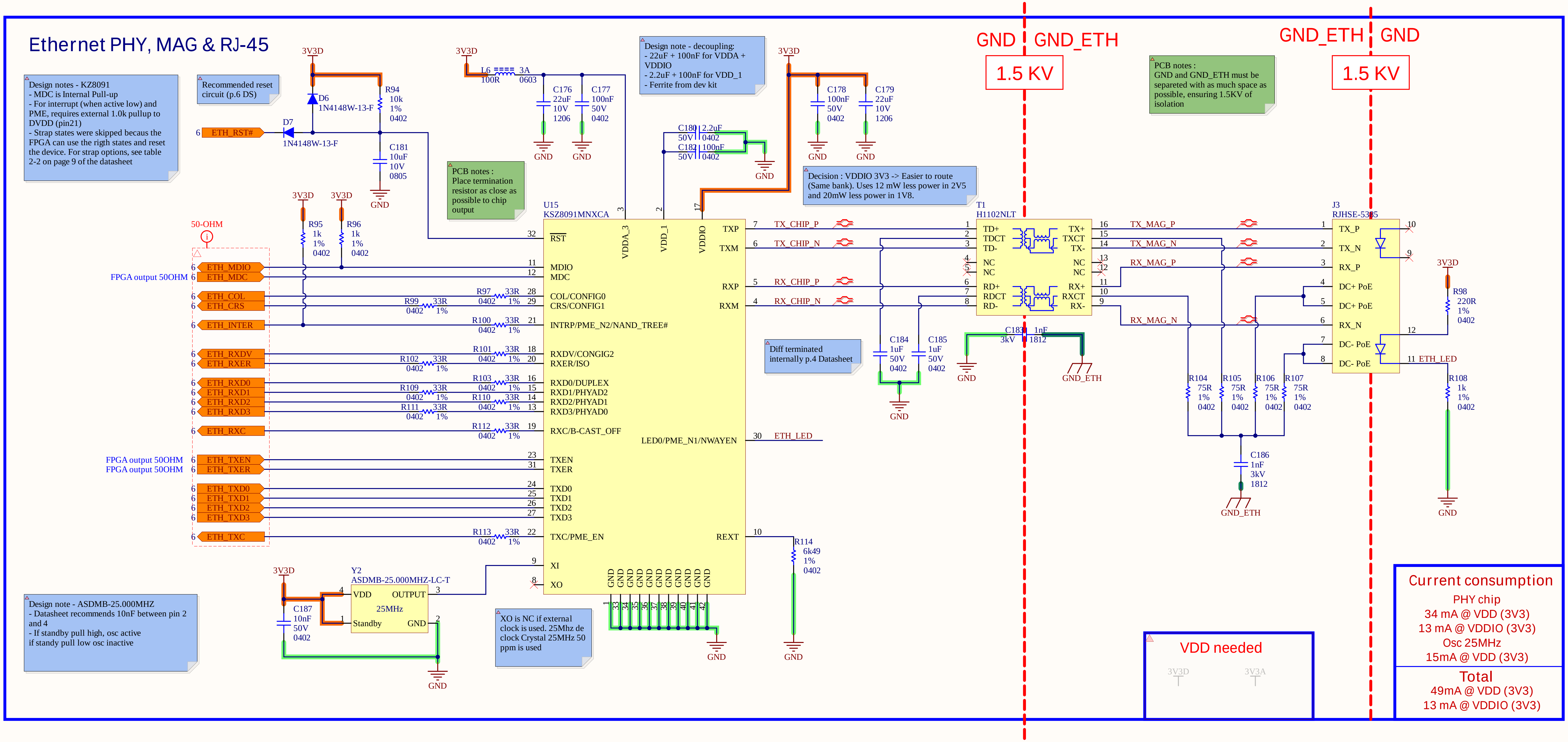
Filename
S7CAS-PLEIADES-CARTE-MERE_P07_MOT.SchDoc

Designers
Philippe Arsenault
Louis-Daniel Gaulin

Ethernet PHY, MAG & RJ-45


GND
GND_ETH
1.5 KV
GND_ETH
GND
1.5 KV
3V3D
D6
1N4148W-13-F
R94
10k
1%
0402
ETH_RST#
D7
1N4148W-13-F
C181
10uF
10V
0805
GND
L6 3A
100R 0603
C176
22uF
10V
1206
C177
100nF
50V
0402
C180 2.2uF 50V 0402
C182 100nF 50V 0402
C178
100nF
50V
0402
C179
22uF
10V
1206
U15
KSZ8091MNXCA
RST
VDDA_3
VDD_1
VDDIO
MDIO
MDC
COL/CONFIG0
CRS/CONFIG1
INTRP/PME_N2/NAND_TREE#
RXDV/CONGIG2
RXER/ISO
RXD0/DUPLEX
RXD1/PHYAD2
RXD2/PHYAD1
RXD3/PHYAD0
RXC/B-CAST_OFF
TXEN
TXER
TXD0
TXD1
TXD2
TXD3
TXC/PME_EN
XI
XO
TXP
TXM
RXP
RXM
LED0/PME_N1/NWAYEN
REXT
50-OHM
R95 1k 1% 0402
R96 1k 1% 0402
ETH_MDIO
ETH_MDC
FPGA output 50OHM
ETH_COL
ETH_CRS
ETH_INTER
ETH_RXDV
ETH_RXER
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_RXC
FPGA output 50OHM
FPGA output 50OHM
ETH_TXEN
ETH_TXER
ETH_TXD0
ETH_TXD1
ETH_TXD2
ETH_TXD3
ETH_TXC
R97 33R 0402 1%
R99 33R 0402 1%
R100 33R 0402 1%
R101 33R 0402 1%
R102 33R 0402 1%
R103 33R 0402 1%
R109 33R 0402 1%
R110 33R 0402 1%
R111 33R 0402 1%
R112 33R 0402 1%
R113 33R 0402 1%
TX_CHIP_P
TX_CHIP_N
RX_CHIP_P
RX_CHIP_N
ETH_LED
R114 6k49 1% 0402
Y2
ASDMB-25.000MHZ-LC-T
VDD
OUTPUT
25MHz
Standby
GND
C187 10nF 50V 0402
T1
H1102NLT
TD+ TDCT TD- NC NC RD+ RDCT RD-
TX+ TXCT TX- NC NC RX+ RXCT RX-
C184 1uF 50V 0402
C185 1uF 50V 0402
C183 1nF 3kV 1812
TX_MAG_P
TX_MAG_N
RX_MAG_P
RX_MAG_N
J3
RJHSE-5385
TX_P TX_N RX_P DC+ PoE DC+ PoE RX_N DC- PoE DC- PoE
R104 75R 1% 0402
R105 75R 1% 0402
R106 75R 1% 0402
R107 75R 1% 0402
C186 1nF 3kV 1812
R98 220R 1% 0402
R108 1k 1% 0402
ETH_LED
GND_ETH

Design notes - KZ8091
- MDC is Internal Pull-up
- For interrupt (when active low) and PME, requires external 1.0k pullup to DVDD (pin21)
- Strap states were skipped becaus the FPGA can use the rigth states and reset the device. For strap options, see table 2-2 on page 9 of the datasheet

Recommended reset circuit (p.6 DS)

PCB notes : Place termination resistor as close as possible to chip output

Design note - decoupling:
- 22uF + 100nF for VDDA + VDDIO
- 2.2uF + 100nF for VDD_1
- Ferrite from dev kit

Decision : VDDIO 3V3 -> Easier to route (Same bank). Uses 12 mW less power in 2V5 and 20mW less power in 1V8.

PCB notes : GND and GND_ETH must be separeted with as much space as possible, ensuring 1.5KV of isolation

Diff terminated internally p.4 Datasheet

Design note - ASDMB-25.000MHZ
- Datasheet recommends 10nF between pin 2 and 4
- If standby pull high, osc active
if standy pull low osc inactive

XO is NC if external clock is used. 25Mhz de clock Crystal 25MHz 50 ppm is used

VDD needed

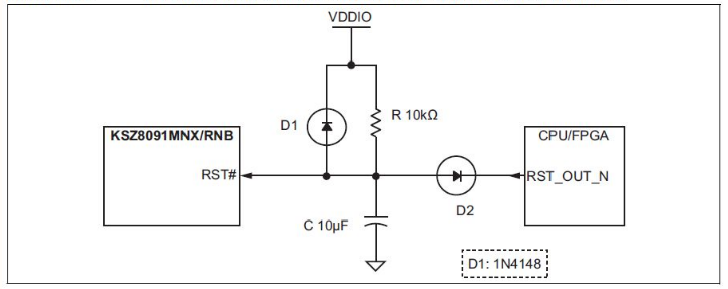
3V3D 3V3A

Current consumption

PHY chip
34 mA @ VDD (3V3)
13 mA @ VDDIO (3V3)
Osc 25MHz
15mA @ VDD (3V3)

Total
49mA @ VDD (3V3)
13 mA @ VDDIO (3V3)

FIGURE 8-2: RECOMMENDED RESET CIRCUIT FOR CPU/FPGA RESET OUTPUT


VDDIO
D1
R 10kΩ
KSZ8091MNX/RNB
RST#
CPU/FPGA
RST_OUT_N
D2
C 10µF
D1: 1N4148

Sheet Name	ETH		
Project Title	P07		
Global Project	*Radio reconfigurable*		
Size 11x17	Group Ultracom		Revision 1.000
Date	2021-01-13	Sheet 14	of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_ETH.SchDoc	Designers	Philippe Arsenault Louis-Daniel Gaulin

OP AMP + Filter + ADC Input

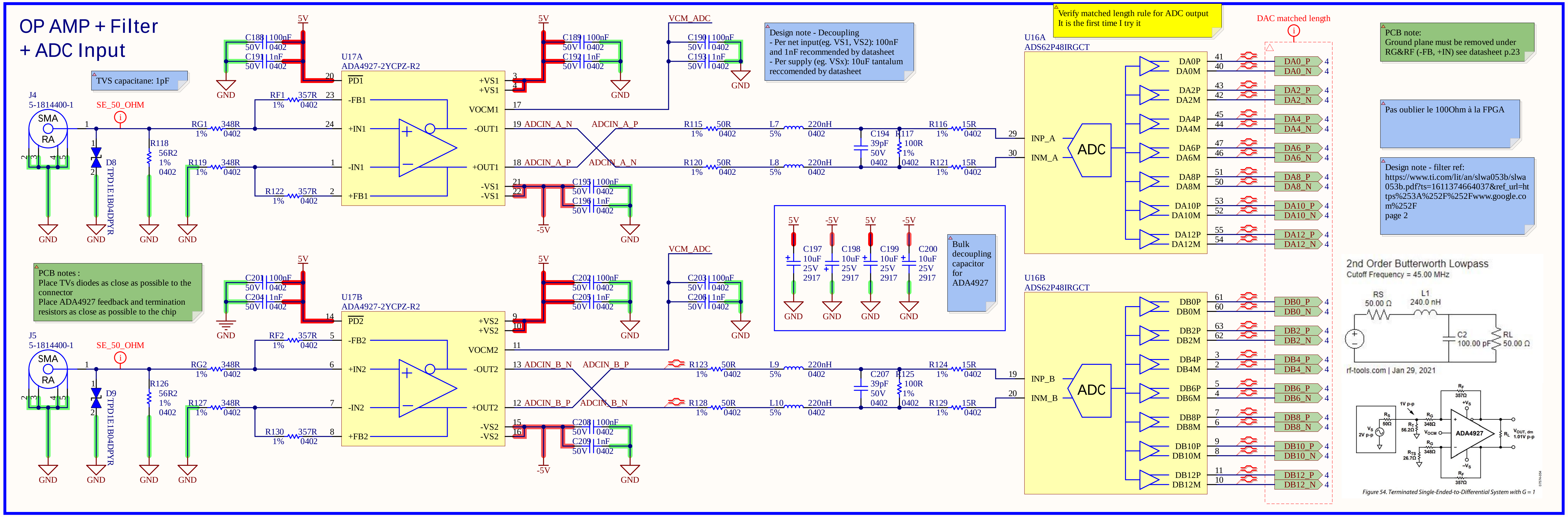

J4
5-1814400-1
SMA RA
SE_50_OHM
D8 TPD1E1B04DPYR
R118 56R2 1% 0402
RG1 348R 1% 0402
R119 348R 1% 0402
RF1 357R 1% 0402
R122 357R 1% 0402
C188 100nF 50V 0402
C191 1nF 50V 0402
U17A
ADA4927-2YCPZ-R2
PD1
-FB1
+IN1
-IN1
+FB1
+VS1
VOCM1
-OUT1
+OUT1
-VS1
5V
-5V
GND
VCM_ADC
C189 100nF 50V 0402
C192 1nF 50V 0402
C190 100nF 50V 0402
C193 1nF 50V 0402
C195 100nF 50V 0402
C196 1nF 50V 0402
ADCIN_A_N
ADCIN_A_P
R115 50R 1% 0402
R120 50R 1% 0402
L7 220nH 5% 0402
L8 220nH 5% 0402
C194 39pF 50V 0402
R117 100R 1% 0402
R116 15R 1% 0402
R121 15R 1% 0402
U16A
ADS62P48IRGCT
INP_A
INM_A
ADC
DA0P DA0M DA2P DA2M DA4P DA4M DA6P DA6M DA8P DA8M DA10P DA10M DA12P DA12M
DA0_P DA0_N DA2_P DA2_N DA4_P DA4_N DA6_P DA6_N DA8_P DA8_N DA10_P DA10_N DA12_P DA12_N
DAC matched length
J5
5-1814400-1
D9 TPD1E1B04DPYR
R126 56R2 1% 0402
RG2 348R 1% 0402
R127 348R 1% 0402
RF2 357R 1% 0402
R130 357R 1% 0402
C201 100nF 50V 0402
C204 1nF 50V 0402
U17B
ADA4927-2YCPZ-R2
PD2
-FB2
+IN2
-IN2
+FB2
+VS2
VOCM2
-OUT2
+OUT2
-VS2
C202 100nF 50V 0402
C205 1nF 50V 0402
C203 100nF 50V 0402
C206 1nF 50V 0402
C208 100nF 50V 0402
C209 1nF 50V 0402
ADCIN_B_N
ADCIN_B_P
R123 50R 1% 0402
R128 50R 1% 0402
L9 220nH 5% 0402
L10 220nH 5% 0402
C207 39pF 50V 0402
R125 100R 1% 0402
R124 15R 1% 0402
R129 15R 1% 0402
U16B
ADS62P48IRGCT
INP_B
INM_B
DB0P DB0M DB2P DB2M DB4P DB4M DB6P DB6M DB8P DB8M DB10P DB10M DB12P DB12M
DB0_P DB0_N DB2_P DB2_N DB4_P DB4_N DB6_P DB6_N DB8_P DB8_N DB10_P DB10_N DB12_P DB12_N
C197 10uF 25V 2917
C198 10uF 25V 2917
C199 10uF 25V 2917
C200 10uF 25V 2917
2nd Order Butterworth Lowpass
Cutoff Frequency = 45.00 MHz
RS 50.00 Ω
L1 240.0 nH
C2 100.00 pF
RL 50.00 Ω
rf-tools.com | Jan 29, 2021
RF 357Ω
RG 348Ω
RT 56.2Ω
RTS 26.7Ω
RS 50Ω
VS 2V p-p
1V p-p
VOCM
ADA4927
+VS
−VS
RL
VOUT, dm 1.01V p-p
07574-054

Figure 54. Terminated Single-Ended-to-Differential System with G = 1

TVS capacitane: 1pF

PCB notes :
Place TVs diodes as close as possible to the connector
Place ADA4927 feedback and termination resistors as close as possible to the chip

Design note - Decoupling
- Per net input(eg. VS1, VS2): 100nF and 1nF recommended by datasheet
- Per supply (eg. VSx): 10uF tantalum reccomended by datasheet

Bulk decoupling capacitor for ADA4927

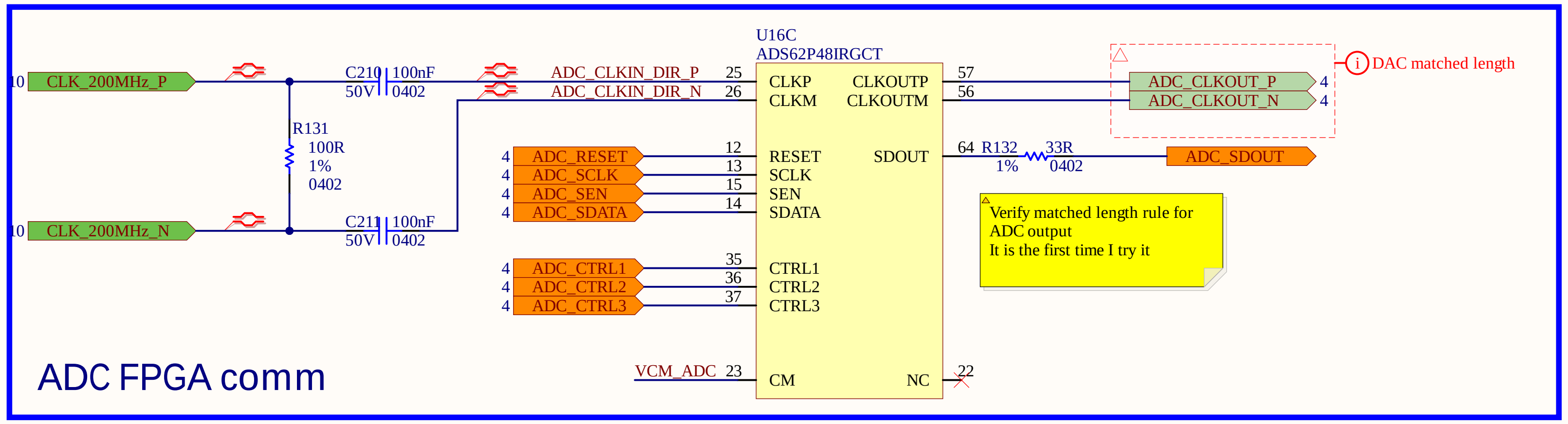
Verify matched length rule for ADC output
It is the first time I try it

PCB note:
Ground plane must be removed under RG&RF (-FB, +IN) see datasheet p.23

Pas oublier le 100Ohm à la FPGA

Design note - filter ref:
https://www.ti.com/lit/an/slwa053b/slwa053b.pdf?ts=1611374664037&ref_url=https%253A%252F%252Fwww.google.com%252F
page 2

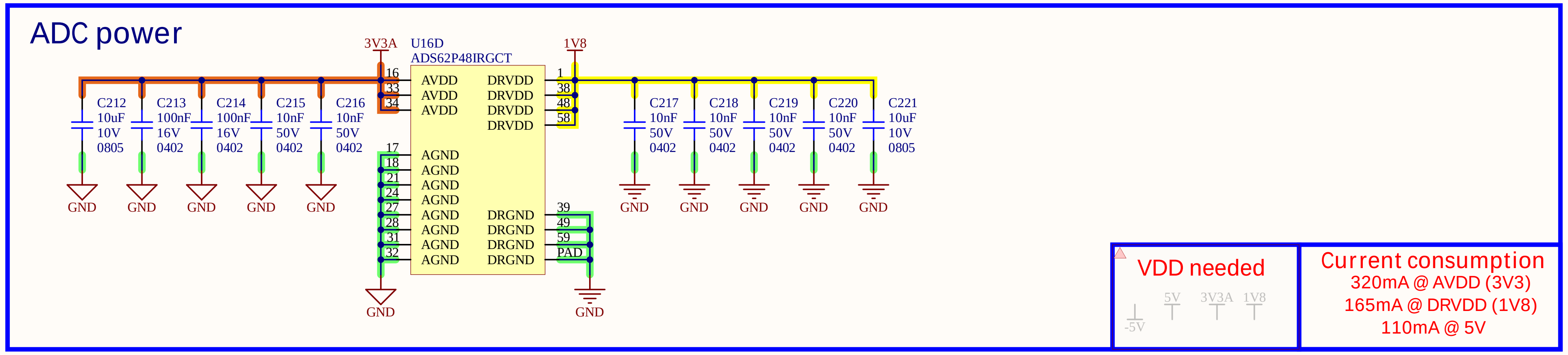
ADC FPGA comm


CLK_200MHz_P
CLK_200MHz_N
C210 100nF 50V 0402
C211 100nF 50V 0402
R131 100R 1% 0402
ADC_CLKIN_DIR_P
ADC_CLKIN_DIR_N
U16C
ADS62P48IRGCT
CLKP
CLKM
CLKOUTP
CLKOUTM
RESET
SCLK
SEN
SDATA
SDOUT
CTRL1
CTRL2
CTRL3
CM
NC
ADC_CLKOUT_P
ADC_CLKOUT_N
DAC matched length
R132 33R 1% 0402
ADC_SDOUT
ADC_RESET
ADC_SCLK
ADC_SEN
ADC_SDATA
ADC_CTRL1
ADC_CTRL2
ADC_CTRL3
VCM_ADC

Verify matched length rule for ADC output
It is the first time I try it

Questions :
- Gain vs filtre

ADC power

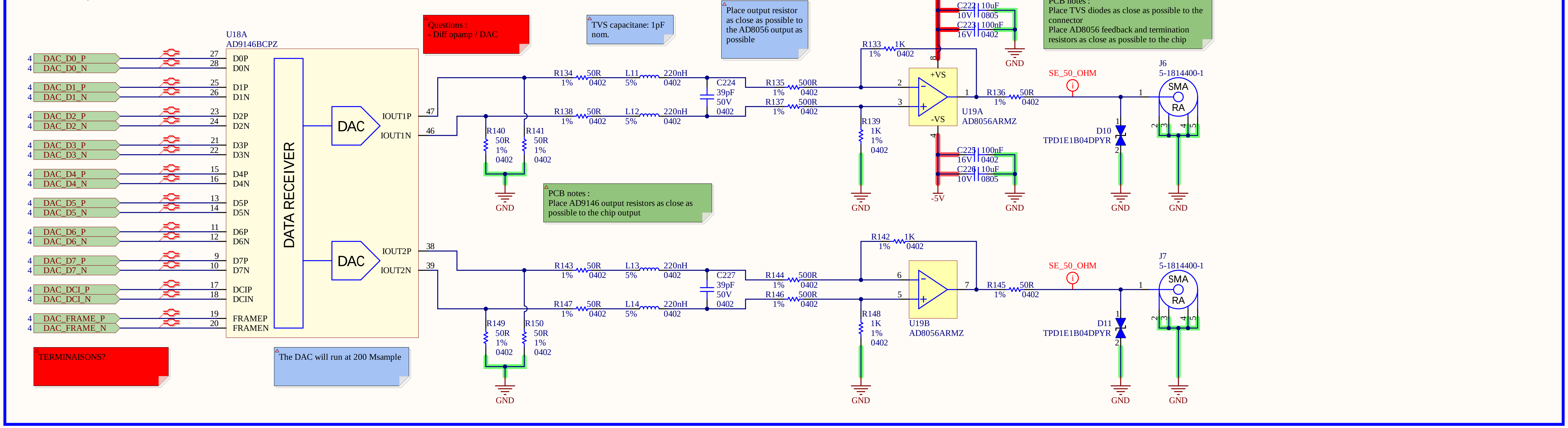

3V3A
U16D
ADS62P48IRGCT
AVDD
DRVDD
AGND
DRGND
1V8
C212 10uF 10V 0805
C213 100nF 16V 0402
C214 100nF 16V 0402
C215 10nF 50V 0402
C216 10nF 50V 0402
C217 10nF 50V 0402
C218 10nF 50V 0402
C219 10nF 50V 0402
C220 10nF 50V 0402
C221 10uF 10V 0805
GND
PAD
5V
3V3A
1V8
-5V

VDD needed

Current consumption
320mA @ AVDD (3V3)
165mA @ DRVDD (1V8)
110mA @ 5V

Sheet Name	ADC
Project Title	P07
Global Project	*Radio reconfigurable*
Size	11x17
Group	Ultracom
Revision	1.000
Date	2021-01-13
Sheet	15 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_ADC.SchDoc
Designers	Philippe Arsenault Louis-Daniel Gaulin

DAC output + filter + OP AMP


4 DAC_D0_P
4 DAC_D0_N
4 DAC_D1_P
4 DAC_D1_N
4 DAC_D2_P
4 DAC_D2_N
4 DAC_D3_P
4 DAC_D3_N
4 DAC_D4_P
4 DAC_D4_N
4 DAC_D5_P
4 DAC_D5_N
4 DAC_D6_P
4 DAC_D6_N
4 DAC_D7_P
4 DAC_D7_N
4 DAC_DCI_P
4 DAC_DCI_N
4 DAC_FRAME_P
4 DAC_FRAME_N
U18A
AD9146BCPZ
27 D0P
28 D0N
25 D1P
26 D1N
23 D2P
24 D2N
21 D3P
22 D3N
15 D4P
16 D4N
13 D5P
14 D5N
11 D6P
12 D6N
9 D7P
10 D7N
17 DCIP
18 DCIN
19 FRAMEP
20 FRAMEN
DATA RECEIVER
DAC
IOUT1P 47
IOUT1N 46
DAC
IOUT2P 38
IOUT2N 39
R134 1% 50R 0402
L11 5% 220nH 0402
R138 1% 50R 0402
L12 5% 220nH 0402
C224 39pF 50V 0402
R135 1% 500R 0402
R137 1% 500R 0402
R140 50R 1% 0402
R141 50R 1% 0402
R133 1% 1K 0402
R139 1K 1% 0402
5V
C222 10V 10uF 0805
C223 16V 100nF 0402
+VS
-VS
2
3
1
8
4
U19A
AD8056ARMZ
C225 16V 100nF 0402
C226 10V 10uF 0805
-5V
R136 1% 50R 0402
SE_50_OHM
J6
5-1814400-1
SMA
RA
1
2 3 4 5
D10
TPD1E1B04DPYR
GND
R143 1% 50R 0402
L13 5% 220nH 0402
R147 1% 50R 0402
L14 5% 220nH 0402
C227 39pF 50V 0402
R144 1% 500R 0402
R146 1% 500R 0402
R149 50R 1% 0402
R150 50R 1% 0402
R142 1% 1K 0402
R148 1K 1% 0402
6
5
7
U19B
AD8056ARMZ
R145 1% 50R 0402
SE_50_OHM
J7
5-1814400-1
SMA
RA
D11
TPD1E1B04DPYR
GND

Questions :
- Diff opamp / DAC

TVS capacitane: 1pF nom.

Place output resistor as close as possible to the AD8056 output as possible

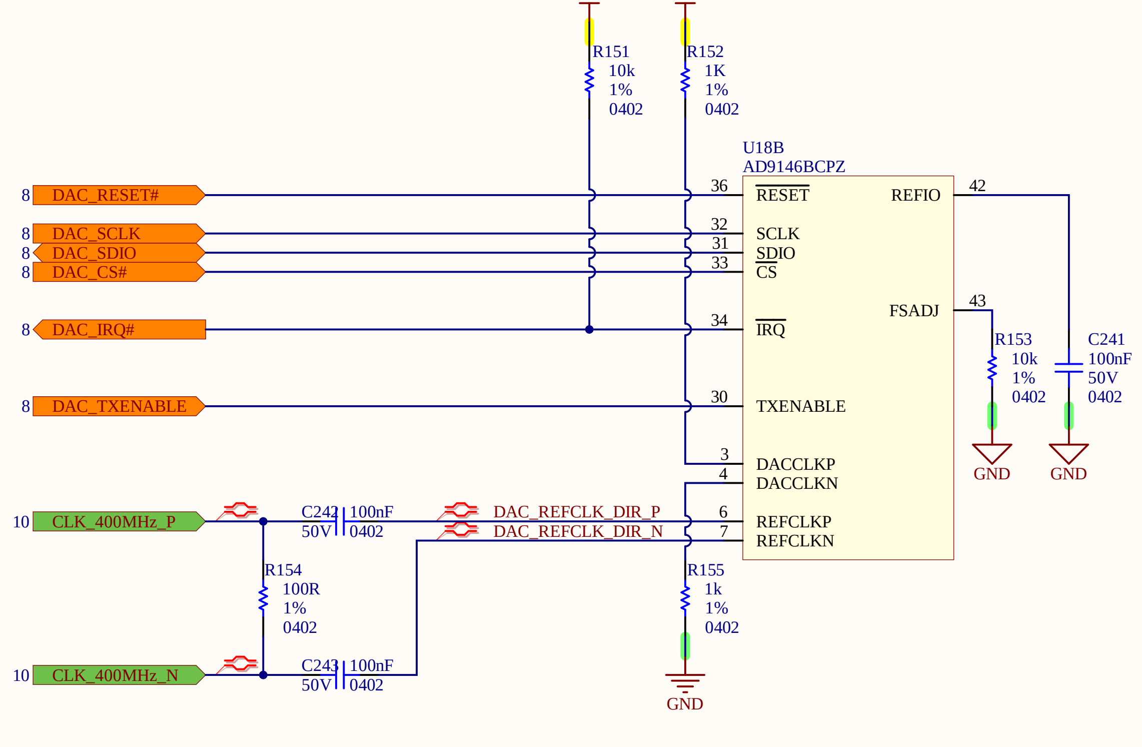
PCB notes :
Place TVS diodes as close as possible to the connector
Place AD8056 feedback and termination resistors as close as possible to the chip

PCB notes :
Place AD9146 output resistors as close as possible to the chip output

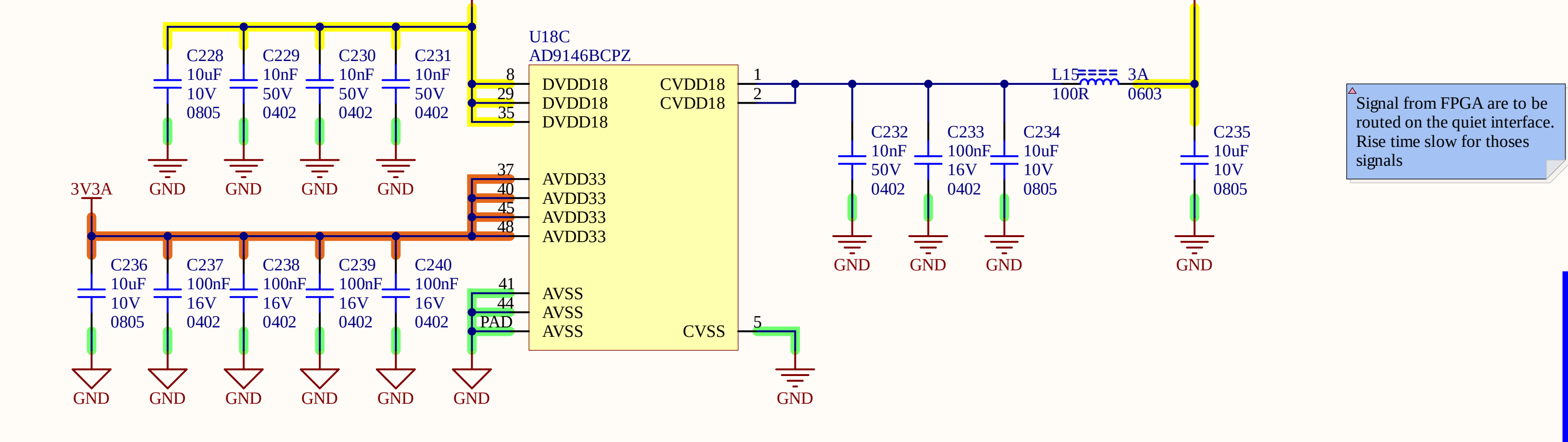
TERMINAISONS?

The DAC will run at 200 Msample

DAC FPGA comm


1V8
R151 10k 1% 0402
1V8
R152 1K 1% 0402
U18B
AD9146BCPZ
8 DAC_RESET#
36 RESET
8 DAC_SCLK
32 SCLK
8 DAC_SDIO
31 SDIO
8 DAC_CS#
33 CS
8 DAC_IRQ#
34 IRQ
8 DAC_TXENABLE
30 TXENABLE
3 DACCLKP
4 DACCLKN
6 REFCLKP
7 REFCLKN
REFIO 42
FSADJ 43
R153 10k 1% 0402
C241 100nF 50V 0402
GND
10 CLK_400MHz_P
C242 50V 100nF 0402
R154 100R 1% 0402
10 CLK_400MHz_N
C243 50V 100nF 0402
DAC_REFCLK_DIR_P
DAC_REFCLK_DIR_N
R155 1k 1% 0402
GND

DAC power


1V8
C228 10uF 10V 0805
C229 10nF 50V 0402
C230 10nF 50V 0402
C231 10nF 50V 0402
U18C
AD9146BCPZ
8 DVDD18
29 DVDD18
35 DVDD18
CVDD18 1
CVDD18 2
37 AVDD33
40 AVDD33
45 AVDD33
48 AVDD33
41 AVSS
44 AVSS
PAD AVSS
CVSS 5
3V3A
C236 10uF 10V 0805
C237 100nF 16V 0402
C238 100nF 16V 0402
C239 100nF 16V 0402
C240 100nF 16V 0402
L15 100R 3A 0603
C232 10nF 50V 0402
C233 100nF 16V 0402
C234 10uF 10V 0805
1V8
C235 10uF 10V 0805
GND

Signal from FPGA are to be routed on the quiet interface. Rise time slow for those signals

VDD needed

5V 3V3A 1V8 -5V

Current consumption
56mA@ AVDD (3V3)
343mA @ DVDD (1V8)
58mA@ AVDD(1V8)
220mA@ 5V/-5V

Sheet Name
DAC

Project Title
P07

Global Project
Radio reconfigurable

Size 11x17
Group Ultracom
Revision 1.000

Date 2021-01-13
Sheet 16 of 16

Filename
S7CAS-PLEIADES-CARTE-MERE_P07_DAC.SchDoc

Designers
Philippe Arsenault
Louis-Daniel Gaulin