DRV8811 Stepper Motor Controller IC

1 Features

- Pulse Width Modulation (PWM) Microstepping Motor Driver
  - Built-In Microstepping Indexer
  - Up to 1/8 Microstepping
  - Step and Direction Control
  - Programmable Mixed Decay, Blanking, and Off-Time
- Up to 1.9-A Current Per Winding
- Low 1.0-Ω (HS+LS) MOSFET $R_{DS(ON)}$ (25°C)
- 8-V to 38-V Operating Supply Voltage Range
- Pin to Pin with the DRV8818
- Thermally Enhanced Surface Mount Package
- Protection Features:
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Fault Condition Indication Pin (nFAULT)

2 Applications

- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

3 Description

The DRV8811 provides an integrated stepper motor driver solution for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers, as well as microstepping indexer logic to control a stepper motor.

The output driver block consists of N-channel power MOSFETs configured as full H-bridges to drive the motor windings.

A simple STEP/DIR interface allows easy interfacing to controller circuits. Step mode pins allow for configuration of the motor in full-step, half-step, quarter-step, or eighth-step modes. Decay mode and PWM off time are programmable.

Internal shutdown functions are provided for over current protection, short circuit protection, under-voltage lockout and overtemperature.

The DRV8811 is packaged in a PowerPAD™ 28-pin HTSSOP package with thermal pad (Eco-friendly: RoHS and no Sb/Br).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8811	HTSSOP (28)	9.70 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

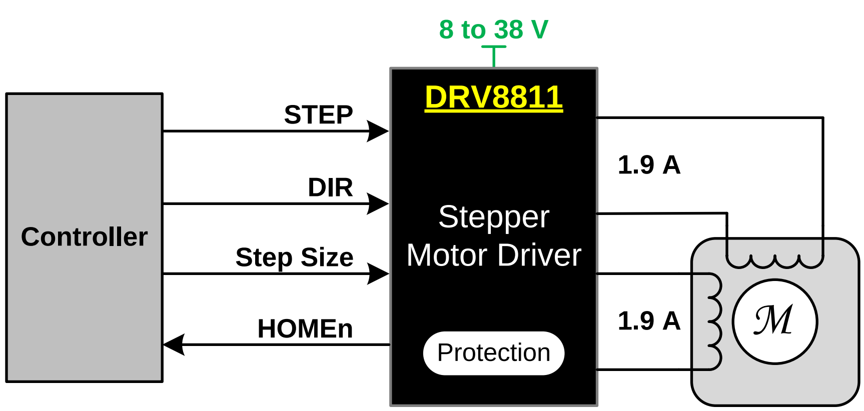


Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (November 2013) to Revision I — **Page**

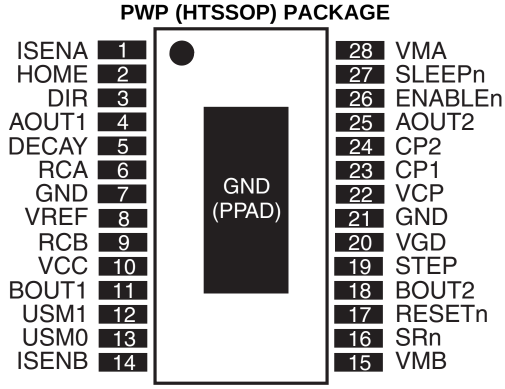
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 4

Changes from Revision G (May 2010) to Revision H — **Page**

- Changed Features bullet 1
- Changed $I_{O(peak)}$ and deleted I_O in Absolute Maximum Ratings table 4
- Changed maximum digital pin voltage 4
- Added parameters to Logic-Level Inputs section of the ELECTRICAL CHARACTERISTICS 5
- Changed *Timing Requirements* 7

6 Pin Configuration and Functions

PWP (HTSSOP) PACKAGE



Pin Functions

PIN		I/O [(1)]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
GND	7, 21	-	Device ground	
VMA	28	-	Bridge A power supply	Connect to motor supply (8 V to 38 V). Both VMA and VMB must be connected to same supply.
VMB	15	-	Bridge B power supply	
VCC	10	-	Logic supply voltage	Connect to 3-V to 5-V logic supply. Bypass to GND with a 0.1-μF ceramic capacitor
CP1	23	IO	Charge pump flying capacitor	Connect a 0.22-μF capacitor between CP1 and CP2
CP2	24	IO	Charge pump flying capacitor	Connect a 0.22-μF capacitor between CP1 and CP2
VCP	22	IO	High-side gate drive voltage	Connect a 0.22-μF ceramic capacitor to V_M
VGD	20	IO	Low-side gate drive voltage	Bypass to GND with a 0.22-μF ceramic capacitor
CONTROL				
ENABLEn	26	I	Enable input	Logic high to disable device outputs, logic low to enable outputs
SLEEPn	27	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode
DECAY	5	I	Decay mode select	Voltage applied sets decay mode - see motor driver description for details. Bypass to GND with a 0.1-μF ceramic capacitor
STEP	19	I	Step input	Rising edge causes the indexer to move one step
DIR	3	I	Direction input	Level sets the direction of stepping
USM0	13	I	Microstep mode 0	USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step
USM1	12	I	Microstep mode 1	USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step
RESETn	17	I	Reset input	Active-low reset input initializes the indexer logic and disables the H-bridge outputs
SRn	16	I	Sync. Rect. enable input	Active-low. When low, synchronous rectification is enabled. Weak internal pulldown.
VREF	8	I	Current set reference input	Reference voltage for winding current set
RCA	6	I	Bridge A blanking and off time adjust	Connect a parallel resistor and capacitor to GND - see motor driver description for details
RCB	9	I	Bridge B blanking and off time adjust	Connect a parallel resistor and capacitor to GND - see motor driver description for details
ISENA	1	-	Bridge A ground / Isense	Connect to current sense resistor for bridge A
ISENB	14	-	Bridge B ground / Isense	Connect to current sense resistor for bridge B
OUTPUTS				
AOUT1	4	O	Bridge A output 1	Connect to bipolar stepper motor winding A

(1) Directions: I = input, O = output, OZ = 3-state output, OD = open-drain output, IO = input/output

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
AOUT2	25	O	Bridge A output 2	Positive current is AOUT1 → AOUT2
BOUT1	11	O	Bridge B output 1	Connect to bipolar stepper motor winding B
BOUT2	18	O	Bridge B output 2	Positive current is BOUT1 → BOUT2
HOMEn	2	O	Home position	Logic low when at home state of step table, logic high at other states

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2] [3]

		MIN	MAX	UNIT
V_{MX}	Power supply voltage range	–0.3	40	V
V_{CC}	Power supply voltage range	–0.3	7	V
	Digital pin voltage range	–0.5	7	V
V_{REF}	Input voltage range	–0.3	V_{CC}	V
ISENSEx[4]	Pin voltage range	–0.875	0.875	V
$I_{O(peak)}$	Peak motor drive output current, t < 1 μs	Internally limited		
P_D	Continuous total power dissipation	See *Dissipation Ratings*		
T_J	Operating virtual junction temperature range	–40	150	°C
T_A	Operating ambient temperature range	–40	85	°C
	Storage temperature range, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.
(4) Transients of ±1V for less than 25 ns are acceptable.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range[1]	8		38	V
V_{CC}	Logic power supply voltage range	3		5.5	V
V_{REF}	VREF input voltage			V_{CC}	V

(1) All V_M pins must be connected to the same supply voltage.

7.4 Thermal Information

THERMAL METRIC(1)		DRV8811 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	11.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Dissipation Ratings

BOARD	PACKAGE	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
Low-K(1)	PWP	67.5 °C/W	14.8 mW/°C	1.85 W	1.18 W	0.96 W
Low-K(2)	PWP	39.5 °C/W	25.3 mW/°C	3.16 W	2.02 W	1.64 W
High-K(3)	PWP	33.5 °C/W	29.8 mW/°C	3.73 W	2.38 W	1.94 W
High-K(4)	PWP	28 °C/W	35.7 mW/°C	4.46 W	2.85 W	2.32 W

(1) The JEDEC Low-K board used to derive this data was a 76 mm x 114 mm, 2-layer, 1.6 mm thick PCB with no backside copper.
(2) The JEDEC Low-K board used to derive this data was a 76 mm x 114 mm, 2-layer, 1.6 mm thick PCB with 25 cm^2 2-oz copper on backside.
(3) The JEDEC High-K board used to derive this data was a 76 mm x 114 mm, 4-layer, 1.6 mm thick PCB with no backside copper and solid 1 oz. internal ground plane.
(4) The JEDEC High-K board used to derive this data was a 76 mm x 114 mm, 4-layer, 1.6 mm thick PCB with 25 cm^2 1-oz copper on backside and solid 1 oz. internal ground plane.

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	V_M operating supply current	V_M = 35 V, f_{PWM} < 50 KHz		4.5	8	mA
I_{VCC}	V_{CC} operating supply current	f_{PWM} < 50 KHz		0.4	4	mA
I_{VMQ}	V_M sleep mode supply current	V_M = 35 V		12	20	μA
I_{VCCQ}	V_{CC} sleep mode supply current			5	20	μA
V_{UVLO}	V_M undervoltage lockout voltage	V_M rising		6.7	8	V
	V_{CC} undervoltage lockout voltage	V_{CC} rising		2.71	2.95	
VREF INPUT, CURRENT CONTROL ACCURACY						
I_{REF}	VREF input current	VREF = 3.3 V	–3		3	μA
ΔI_{CHOP}	Chopping current accuracy	VREF = 2.0 V, 70% to 100% current	–5%		5%	
		VREF = 2.0 V, 20% to 56% current	–10%		10%	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				0.3 × V_{CC}	V
V_{IH}	Input high voltage		0.7 × V_{CC}			V
I_{IL}	Input low current	VIN = 0.3 × V_{CC}	–20		20	μA
I_{IH}	Input high current	VIN = 0.3 × V_{CC}	–20		20	μA
R_{PU}	Pullup resistance	ENABLEn, RESETn		1		MΩ
R_{PD}	Pulldown resistance	DIR, STEP, SLEEPn, USM1, USM0, SRn		1		MΩ

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HOMEn OUTPUT						
V_{OL}	Output low voltage	I_O = 200 µA			0.3 × VCC	V
V_{OH}	Output high voltage	I_O = –200 µA	0.7 × VCC			V
DECAY INPUT						
V_{IL}	Input low threshold voltage	For fast decay mode		0.21 × VCC		V
V_{IH}	Input high threshold voltage	For slow decay mode		0.6 × VCC		V
H-BRIDGE FETS						
$R_{ds(on)}$	HS FET on resistance	V_M = 24 V, I_O = 2.5 A, T_J = 25°C		0.50		Ω
		V_M = 24 V, I_O = 2.5 A, T_J = 85°C		0.60	0.75	
$R_{ds(on)}$	LS FET on resistance	V_M = 24 V, I_O = 2.5 A, T_J = 25°C		0.50		Ω
		V_M = 24 V, I_O = 2.5 A, T_J = 85°C		0.60	0.75	
I_{OFF}			–20		20	µA
MOTOR DRIVER						
t_{OFF}	Off time	Rx = 56 kΩ, Cx = 680 pF	30	38	46	µs
t_{BLANK}	Current sense blanking time	Rx = 56 kΩ, Cx = 680 pF	700	950	1200	ns
t_{DT}	Dead time (1)	SRn = 0	100	475	800	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2.5	4.5	6.5	A
t_{TSD}	Thermal shutdown temperature (1)	Die temperature	150	160	180	°C

(1) Not tested in production - guaranteed by design.

7.7 Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

			MIN	TYP	MAX	UNIT
1	f_{STEP}	Step frequency			500	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	1			μs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	1			μs
4	$t_{SU(STEP)}$	Setup time, command before STEP rising	200			ns
5	$t_{H(STEP)}$	Hold time, command after STEP rising	200			ns
6	t_{WAKE}	Wakeup time, SLEEPn inactive high to STEP input accepted			1	ms
7	t_{SLEEP}	Sleep time, SLEEPn active low to outputs disabled			5	μs
8	t_{ENABLE}	Enable time, ENABLEn inactive high to outputs enabled			20	μs
9	$t_{DISABLE}$	Disable time, ENABLEn active low to outputs disabled			20	μs
10	t_{RESETR}	Reset release time, RESETn inactive high to outputs enabled			5	μs
11	t_{RESET}	Reset time, RESETn active low to outputs disabled			5	μs

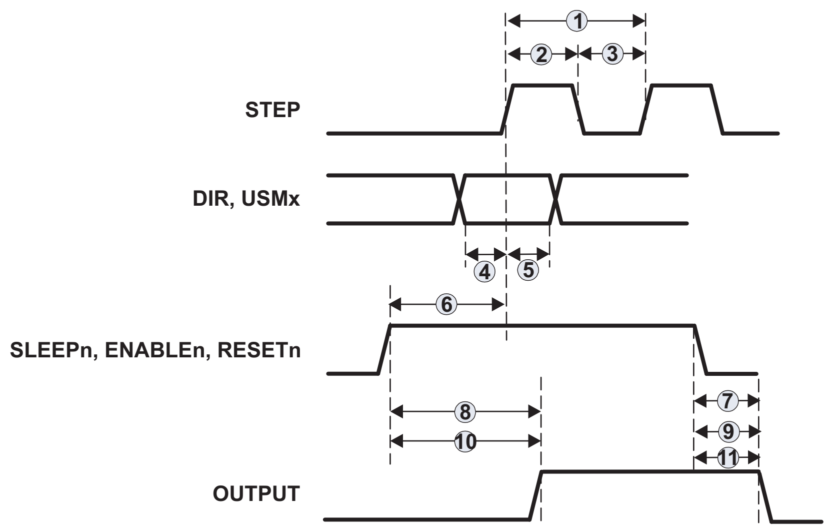


Figure 1. Timing Diagram

7.8 Typical Characteristics

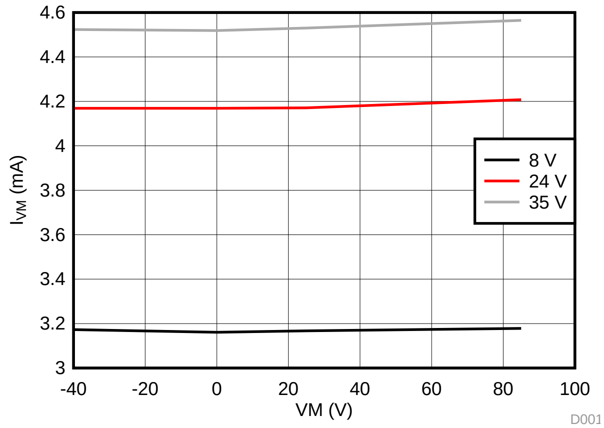


Figure 2. I_{VM} vs VM

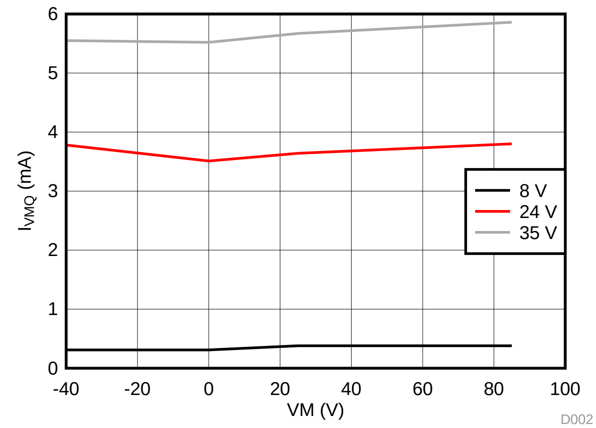


Figure 3. I_{VMQ} vs VM

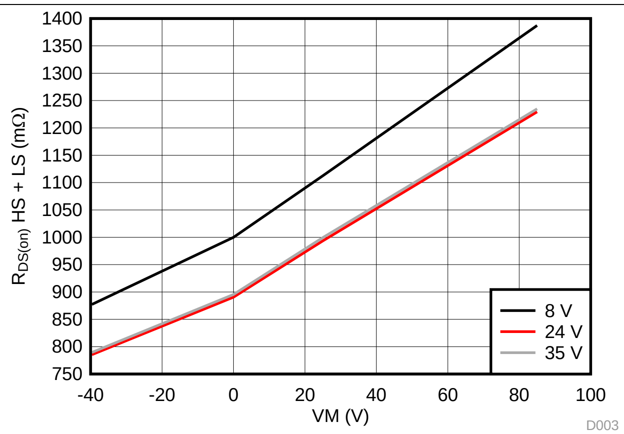


Figure 4. $R_{DS(ON)}$ HS + LS vs VM

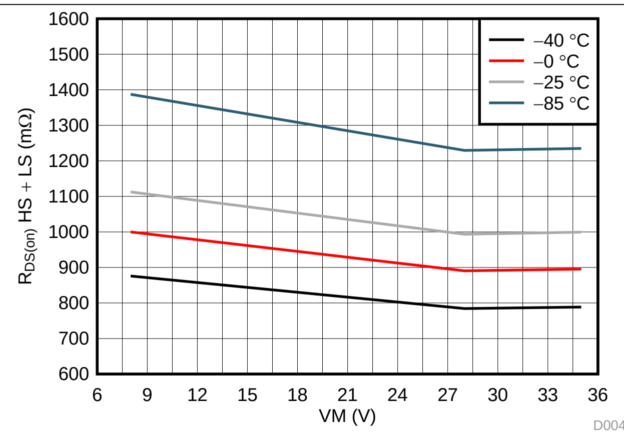


Figure 5. $R_{DS(ON)}$ HS +LS vs Temperature

8 Detailed Description

8.1 Overview

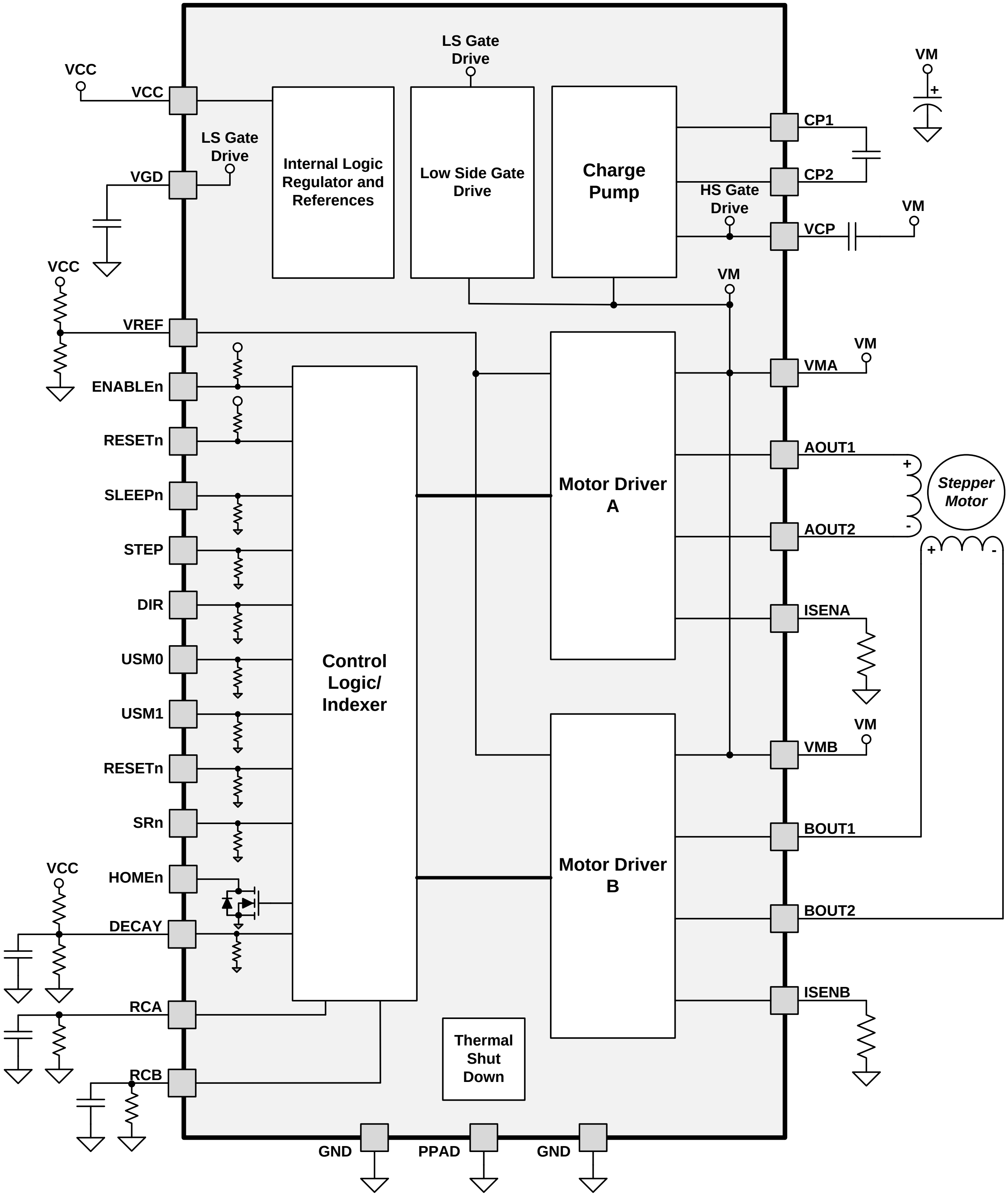
The DRV8811 is a highly configurable, integrated motor driver solution for bipolar stepper motors. The device integrates two H-bridges, current sense and regulation circuitry, and a microstepping indexer. The DRV8811 can be powered with a supply voltage between 8 V and 38 V and is capable of providing an output current up to 1.9 A full-scale.

A simple STEP/DIR interface allows for easy interfacing to the controller. The internal indexer is able to execute high-accuracy microstepping without requiring the controller to manage the current regulation loop.

The current regulation is highly configurable, with three decay modes of operation. They are fast, slow, and mixed decay, which can be selected depending on the application requirements. The DRV8811 also provides configurable mixed decay, blanking, and off time in order to adjust to a wide range of motors.

A low-power sleep mode is incorporated which allows for minimal power consumption when the system is idle.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PWM H-Bridge Drivers

DRV8811 contains two H-bridge motor drivers with current-control PWM circuitry, and a microstepping indexer. A block diagram of the motor control circuitry is shown below.

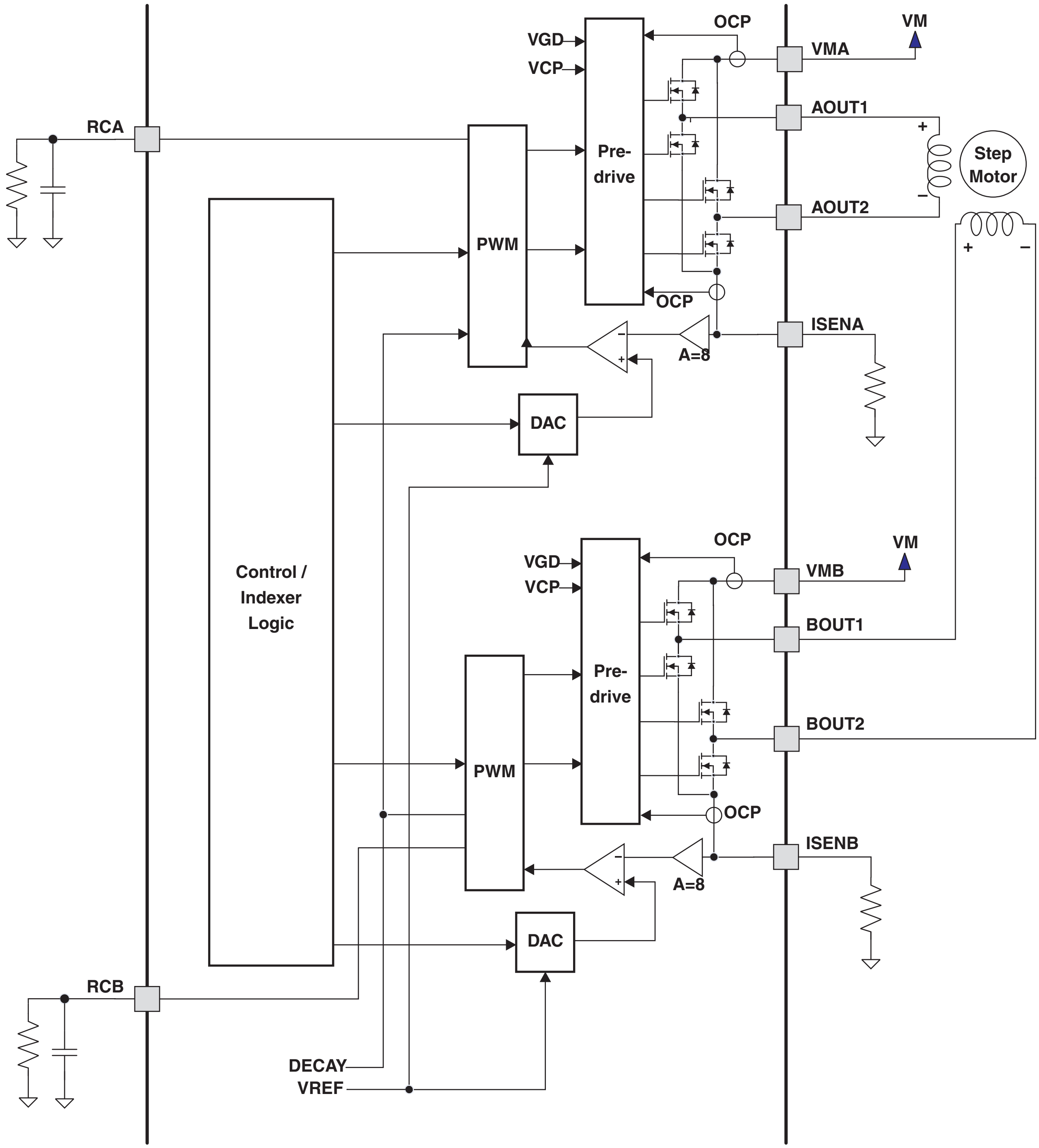


Figure 6. Motor Control Circuitry

Feature Description (continued)

8.3.2 Current Regulation

The PWM chopping current is set by a comparator, which compares the voltage across a current sense resistor, multiplied by a factor of 8, with a reference voltage. The reference voltage is input from the VREF pin. The full-scale (100%) chopping current is calculated as follows:

$$I_{CHOP} = \frac{V_{REFX}}{8 \bullet R_{ISENSE}} \quad (1)$$

Example:

If a 0.22-Ω sense resistor is used and the VREFx pin is 3.3 V, the full-scale (100%) chopping current is 3.3 V/(8 * 0.22 Ω) = 1.875 A.

The reference voltage is also scaled by an internal DAC that allows torque control for fractional stepping of a bipolar stepper motor, as described in the "Microstepping Indexer" section below.

When a winding is activated, the current through it rises until it reaches the chopping current threshold described above, then the current is switched off for a fixed off time. The off time is determined by the values of a resistor and capacitor connected to the RCA (for bridge A) and RCB (for bridge B) pins. The off time is approximated by:

$$t_{OFF} = R \bullet C \quad (2)$$

To avoid falsely tripping on transient currents when the winding is first activated, a blanking period is used immediately after turning on the FETs, during which the state of the current sense comparator is ignored. The blanking time is determined by the value of the capacitor connected to the RCx pin and is approximated by:

$$t_{BLANK} = 1400 \bullet C \quad (3)$$

8.3.3 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7, Item 1. The current flow direction shown indicates positive current flow in the step table below.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. If synchronous rectification is enabled (SRn pin logic low), the opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. If SRn is high, current is recirculated through the body diodes, or through external Schottky diodes. Fast-decay mode is shown in Figure 7, Item 2.

In slow-decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7, Item 3.

Feature Description (continued)

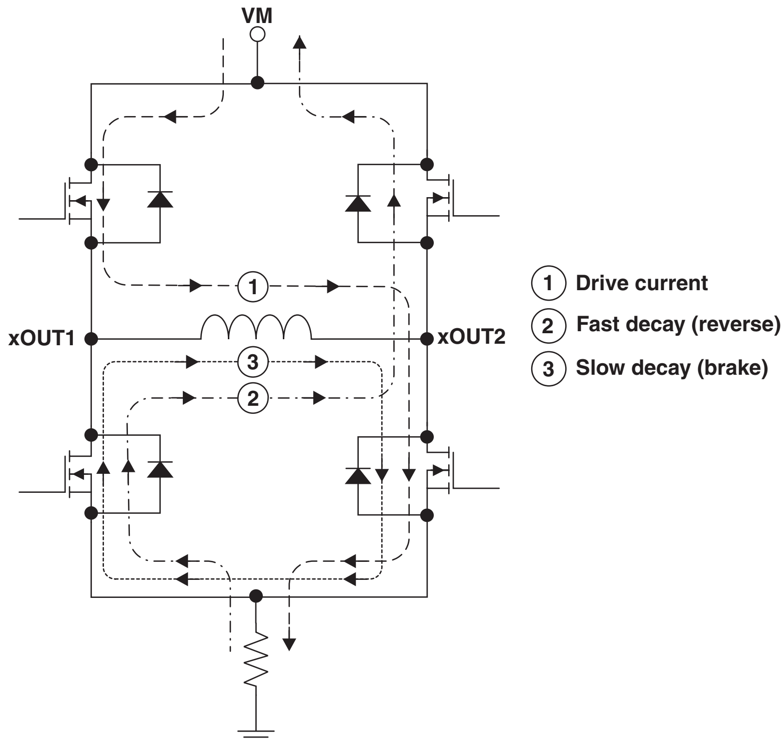


Figure 7. Decay Mode

The DRV8811 also supports a mixed decay mode. Mixed decay mode begins as fast decay, but after a period of time switches to slow decay mode for the remainder of the fixed off time.

Fast and mixed decay modes are only active if the current through the winding is decreasing; if the current is increasing, then slow decay is always used.

Which decay mode is used is selected by the voltage on the DECAY pin. If the voltage is greater than 0.6 x V_{CC}, slow decay mode is always used. If DECAY is less than 0.21 x V_{CC}, the device operates in fast decay mode when the current through the winding is decreasing. If the voltage is between these levels, mixed decay mode is enabled.

In mixed decay mode, the voltage on the DECAY pin sets the point in the cycle that the change to slow decay mode occurs. This time can be approximated by:

$$t_{FD} = R \bullet C \bullet ln\left(\frac{0.6 \bullet V_{CC}}{V_{DECAY}}\right) \tag{4}$$

Operation of the blanking, fixed off time, and mixed decay mode is illustrated in Figure 8.

Feature Description (continued)

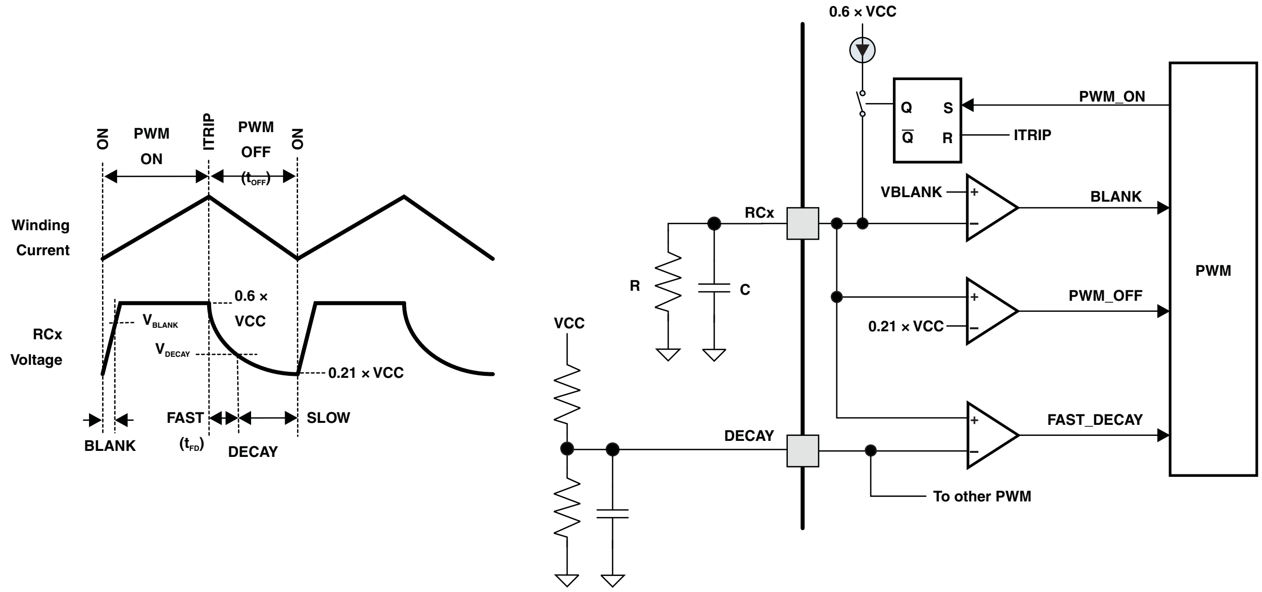


Figure 8. PWM

8.3.4 Microstepping Indexer

Built-in indexer logic in the DRV8811 allows a number of different stepping configurations. The USM1 and USM0 pins are used to configure the stepping format as shown in Table 1:

Table 1. Microstepping Selection Bits

USM1	USM0	STEP MODE
0	0	Full step (2-phase excitation)
0	1	1/2 step (1-2 phase excitation)
1	0	1/4 step (W1-2 phase excitation)
1	1	Eight microsteps/steps

Table 2 shows the relative current and step directions for different settings of USM1 and USM0. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high; if the DIR pin is low the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that the home state is 45 degrees. This state is entered at power-up or device reset. The HOMEn output pin is driven low in this state. In all other states it is driven logic high.

Table 2. Microstepping Indexer

FULL STEP USM = 00	1/2 STEP USM = 01	1/4 STEP USM = 10	1/8 STEP USM = 11	AOUTx CURRENT (% FULL-SCALE)	BOUTx CURRENT (% FULL-SCALE)	STEP ANGLE (DEGREES)
	1	1	1	100	0	0
			2	98	20	11.325
		2	3	92	38	22.5
			4	83	56	33.75
1	2	3	5	71	71	45 (home state)
			6	56	83	56.25
		4	7	38	92	67.5
			8	20	98	78.75

Table 2. Microstepping Indexer (continued)

FULL STEP USM = 00	1/2 STEP USM = 01	1/4 STEP USM = 10	1/8 STEP USM = 11	AOUTx CURRENT (% FULL-SCALE)	BOUTx CURRENT (% FULL-SCALE)	STEP ANGLE (DEGREES)
	3	5	9	0	100	90
			10	–20	98	101.25
		6	11	–38	92	112.5
			12	–56	83	123.75
2	4	7	13	–71	71	135
			14	–83	56	146.25
		8	15	–92	38	157.5
			16	–98	20	168.75
	5	9	17	–100	0	180
			18	–98	–20	191.25
		10	19	–92	–38	202.5
			20	–83	–56	213.75
3	6	11	21	–71	–71	225
			22	–56	–83	236.25
		12	23	–38	–92	247.5
			24	–20	–98	258.75
	7	13	25	0	–100	270
			26	20	–98	281.25
		14	27	38	–92	292.5
			28	56	–83	303.75
4	8	15	29	71	–71	315
			30	83	–56	326.25
		16	31	92	–38	337.5
			32	98	–20	348.75

8.3.5 Protection Circuits

8.3.5.1 Overcurrent Protection (OCP)

If the current through any FET exceeds the preset overcurrent threshold, all FETs in the H-bridge will be disabled until the ENABLEn pin has been brought inactive high and then back low, or power is removed and re-applied. Overcurrent conditions are sensed in both directions; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

Note that overcurrent protection does not use the current sense circuitry used for PWM current control and is independent of the Isense resistor value or VREF voltage. Additionally, in the case of an overcurrent event, the microstepping indexer will be reset to the home state.

8.3.5.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all drivers in the device are shut down and the indexer is reset to the home state. Once the die temperature has fallen to a safe level operation resumes.

8.3.5.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device is disabled and the indexer is reset to the home state. Operation resumes when VM rises above the UVLO threshold.

8.4 Device Functional Modes

8.4.1 RESETn, ENABLEn and SLEEPn Operation

The RESETn pin, when driven active low, resets the step table to the home position. It also disables the H-bridge drivers. The STEP input is ignored while RESETn is active.

The ENABLEn pin is used to control the output drivers. When ENABLEn is low, the output H-bridges are enabled. When ENABLEn is high, the H-bridges are disabled and the outputs are in a high-impedance state.

Note that when ENABLEn is high, the input pins and control logic, including the indexer (STEP and DIR pins) are still functional.

The SLEEPn pin is used to put the device into a low power state. If SLEEPn is low, the H-bridges are disabled, the gate drive charge pump is stopped, and all internal clocks are stopped. In this state all inputs are ignored until the SLEEPn pin returns high.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8811 is used for bipolar stepper motor control. The microstepping motor driver provides precise regulation of the coil current and ensures a smooth rotation from the stepper motor.

9.2 Typical Application

Figure 9 shows a common system application of the DRV8811.

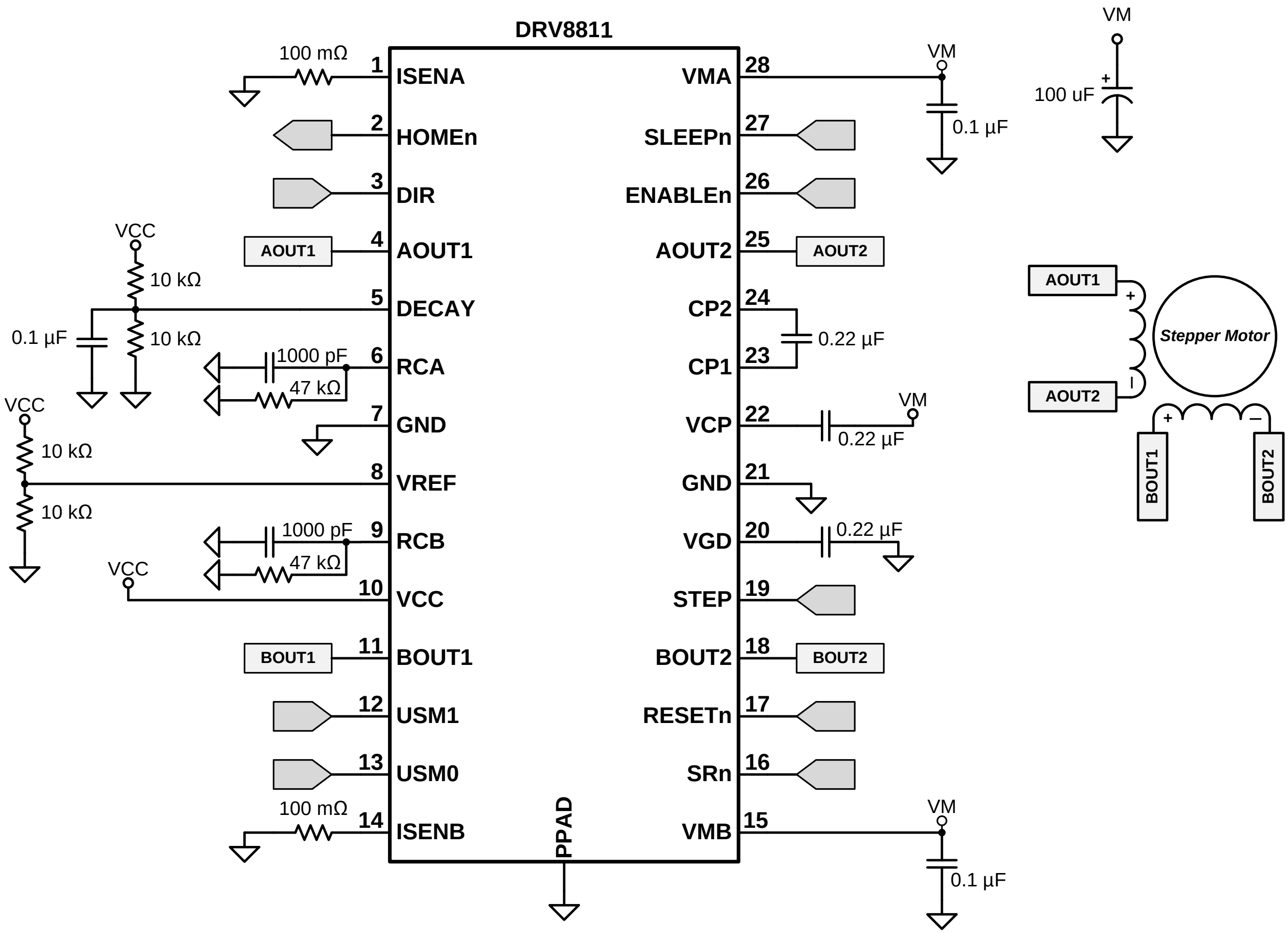


Figure 9. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

Table 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	VM	24 V
Motor Winding Resistance	R_L	4.0 Ω
Motor Winding Inductance	I_L	3.7 mH
Motor Full Step Angle	$θ_{step}$	1.8°/step
Target Microstepping Level	n_m	8 µsteps per step
Target Motor Speed	V	120 rpm
Target Full-Scale Current	I_{FS}	1.25 A

9.2.2 Detailed Design Procedure

9.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8811 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor startup speed is too high, the motor will not spin. Make sure that the motor can support the target speed or implement an acceleration profile to bring the motor up to speed.

For a desired motor speed (v), microstepping level (nm), and motor full step angle ($θ_{step}$),

$$f_{step}\left(\mu steps / second\right) = \frac{v\left(\frac{rotations}{minute}\right) \times 360\left(\frac{\circ}{rotation}\right) \times n_m\left(\frac{\mu steps}{step}\right)}{60\left(\frac{seconds}{minute}\right) \times \theta_{step}\left(\frac{\circ}{step}\right)} \quad (5)$$

$$f_{step}\left(\mu steps / second\right) = \frac{120\left(\frac{rotations}{minute}\right) \times 360\left(\frac{\circ}{rotation}\right) \times 8\left(\frac{\mu steps}{step}\right)}{60\left(\frac{seconds}{minute}\right) \times 1.8\left(\frac{\circ}{step}\right)} \quad (6)$$

$θ_{step}$ can be found in the stepper motor datasheet or written on the motor itself.

For the DRV8811, the microstepping level is set by the USMx pins. Higher microstepping will mean a smother motor motion and less audible noise, but will increase switching losses and require a higher f_{step} to achieve the same motor speed.

9.2.2.2 Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity will depend on the VREF analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. The gain of DRV8811 is set for 8 V/V.

$$I_{FS}\left(A\right) = \frac{VREF(V)}{A_V \ x \ R_{SENSE}\left(\Omega\right)} = \frac{VREF(V)}{8 \ x \ R_{SENSE}\left(\Omega\right)} \quad (7)$$

To achieve IFS = 1.25 A with RSENSE of 0.1 Ω, VREF should be 1.56 V.

9.2.2.3 Decay Modes

The DRV8811 supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor windings is regulated using a fixed off time scheme.

This means that the current will increase until it reaches the current chopping threshold (I_{TRIP}), after which it will enter the set decay mode for a fixed period of time. The cycle will then repeat after the decay period expires.

The blanking time T_{BLANK} defines the minimum drive time for the current chopping. I_{TRIP} is ignored during T_{BLANK}, so the winding current may overshoot the trip level.

9.2.3 Application Curves

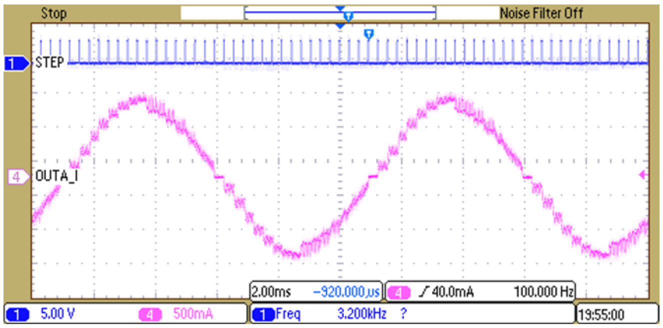


Figure 10. Mixed Decay

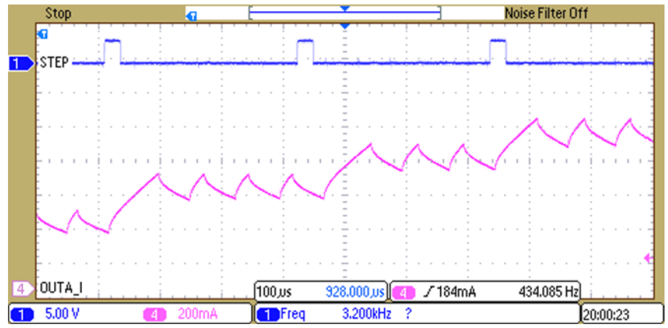


Figure 11. Slow Decay on Increasing Steps

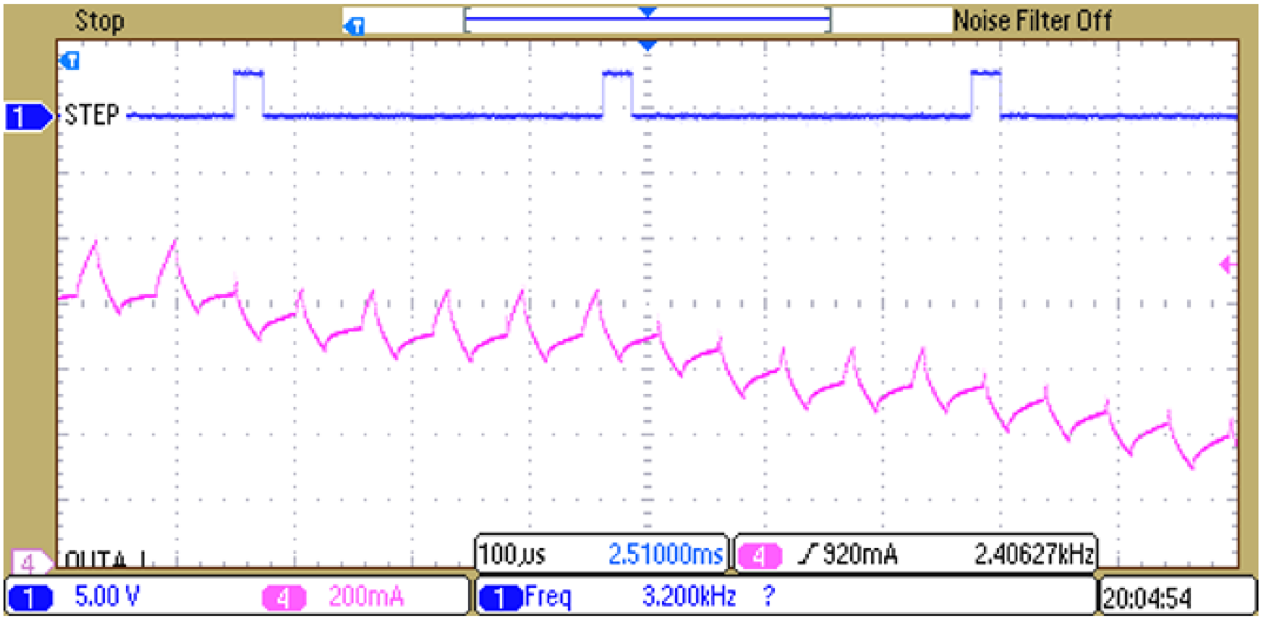


Figure 12. Mixed Decay on Decreasing Steps

10 Power Supply Recommendations

10.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (Brushed DC, Brushless DC, Stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

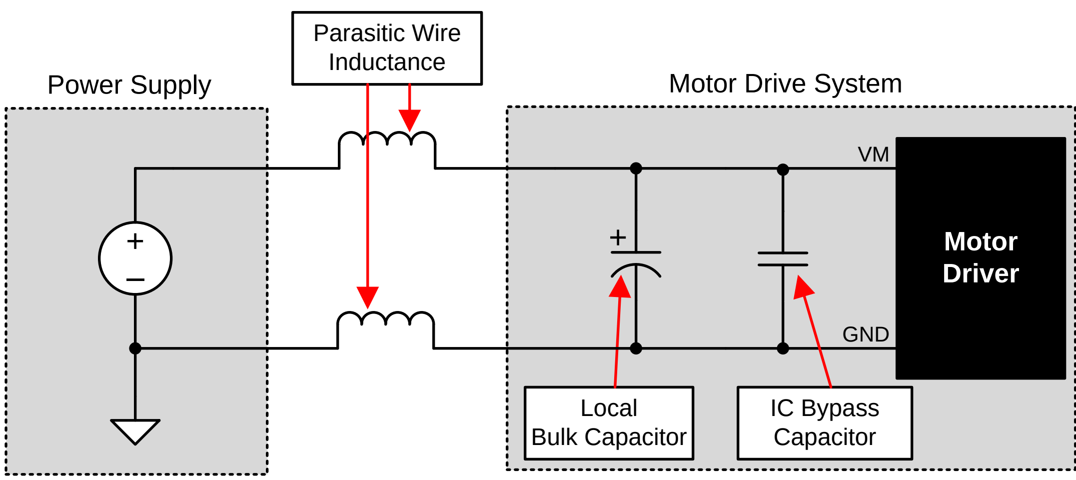


Figure 13. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

11 Layout

11.1 Layout Guidelines

The VMA and VMB pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for VM. This capacitor should be placed as close to the VMA and VMB pins as possible with a thick trace or ground plane connection to the device GND pin.

The VMA and VMB pins must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8811.

A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. TI recommends a value of 0.22 µF rated for VM. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.22 µF rated for 16 V. Place this component as close to the pins as possible.

Ensure proper connection of the DRV8811 PowerPAD to the PCB. The PowerPAD should be connected to a copper plane that is connected to GND. The copper plane should have a large area to allow for thermal dissipation from the DRV8811.

11.2 Layout Example

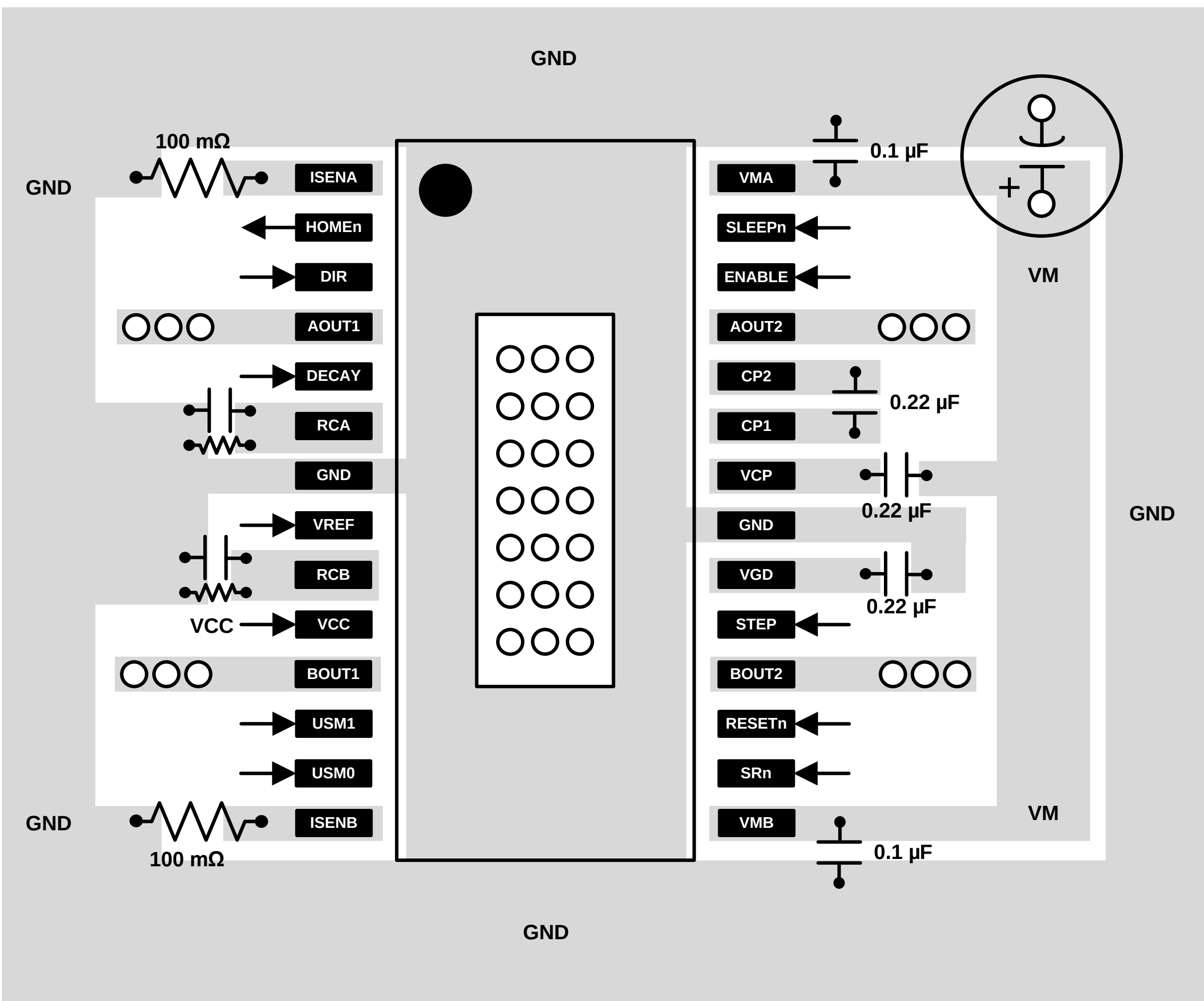


Figure 14. Layout Example Schematic

11.3 Thermal Information

The DRV8811 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

11.3.1 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI Application Report SLMA002, "PowerPAD™ Thermally Enhanced Package" and TI Application Brief SLMA004, "PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated. Figure 18 shows thermal resistance vs. copper plane area for a single-sided PCB with 2-oz. copper heatsink area. It can be seen that the heatsink effectiveness increases rapidly to about 20 cm^2, then levels off somewhat for larger areas.

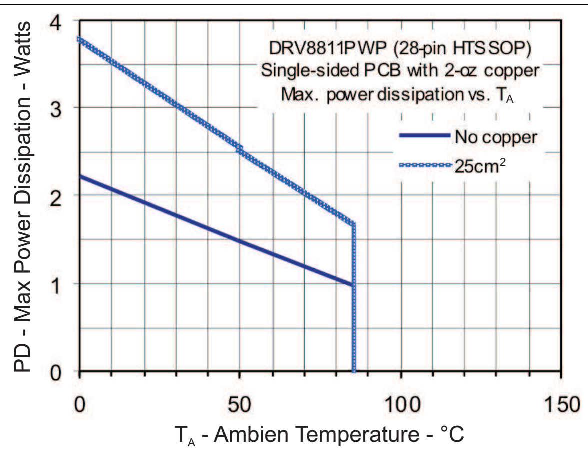


Figure 15. Power Dissipation (2-Layer)

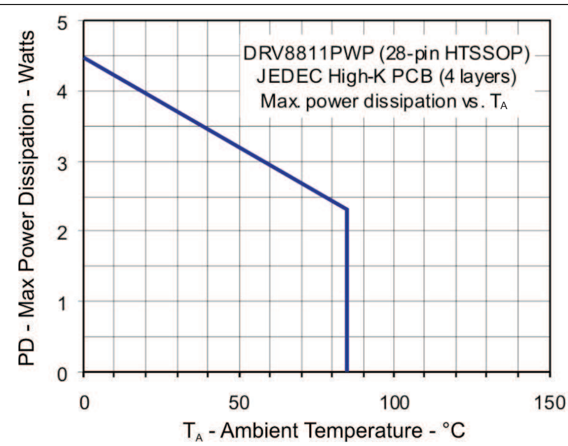


Figure 16. Power Dissipation (4-Layer)

Thermal Information (continued)

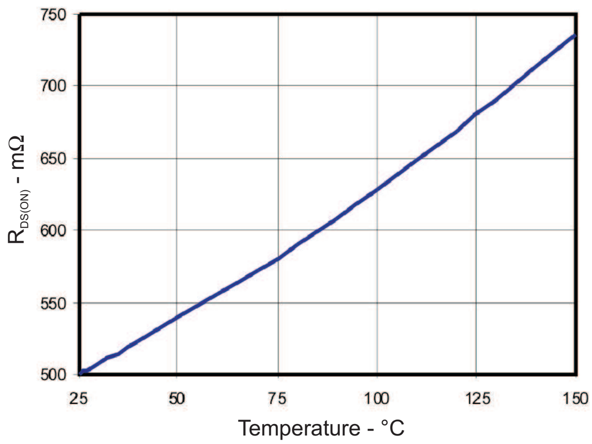


Figure 17. Typical $R_{DS(ON)}$ vs Temperature

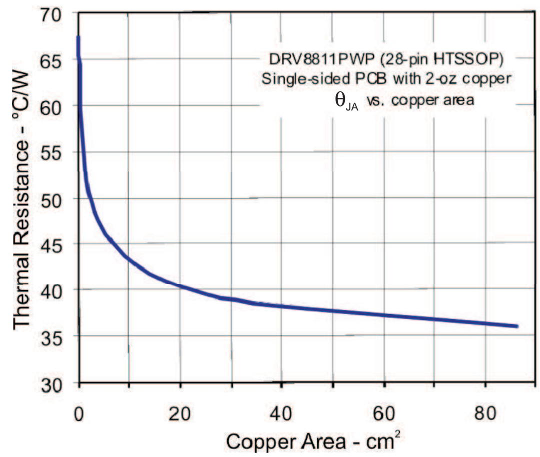


Figure 18. Thermal Resistance vs Copper Area

11.4 Power Dissipation

Power dissipation in the DRV8811 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by:

$$P_{TOT} = 4 \bullet R_{DS(ON)} \bullet (I_{OUT(RMS)})^2 \tag{8}$$

where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the DRV8811 is dependent on ambient temperature and heatsinking. Figure 15 and Figure 16 show how the maximum allowable power dissipation varies according to temperature and PCB construction. Figure 15 shows data for a JEDEC low-K board, 2-layers with 2-oz. copper,
76 mm x 114 mm x 1.6 mm thick, with either no backside copper or a 24 cm^2 copper area on the backside. Similarly, Figure 16 shows data for a JEDEC high-K board, 4 layers with 1-oz. copper, 76 mm x 114 mm x 1.6 mm thick, and a solid internal ground plane. In this case, the PowerPAD™ is tied to the ground plane using thermal vias, and no additional outer layer copper.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink. Refer to Figure 17.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

1. *PowerPAD™ Thermally Enhanced Package*, SLMA002
2. *PowerPAD™ Made Easy*, SLMA004
3. *Current Recirculation and Decay Modes*, SLVA321
4. *Calculating Motor Driver Power Dissipation*, SLVA504
5. *Understanding Motor Driver Current Ratings*, SLVA505

12.2 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8811PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8811	Samples
DRV8811PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8811	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

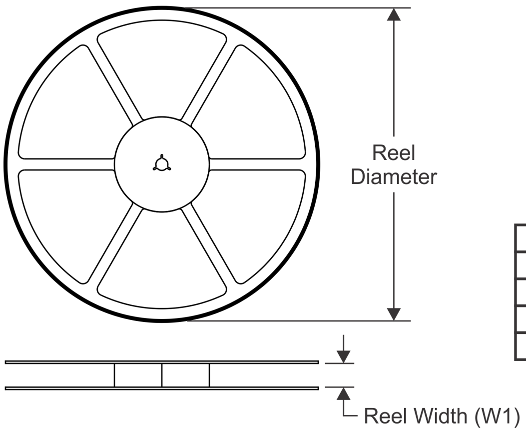
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

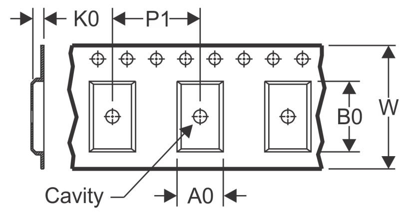
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

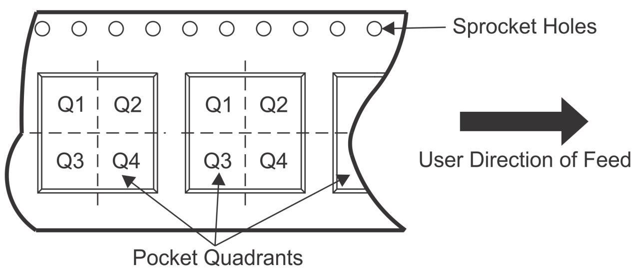
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

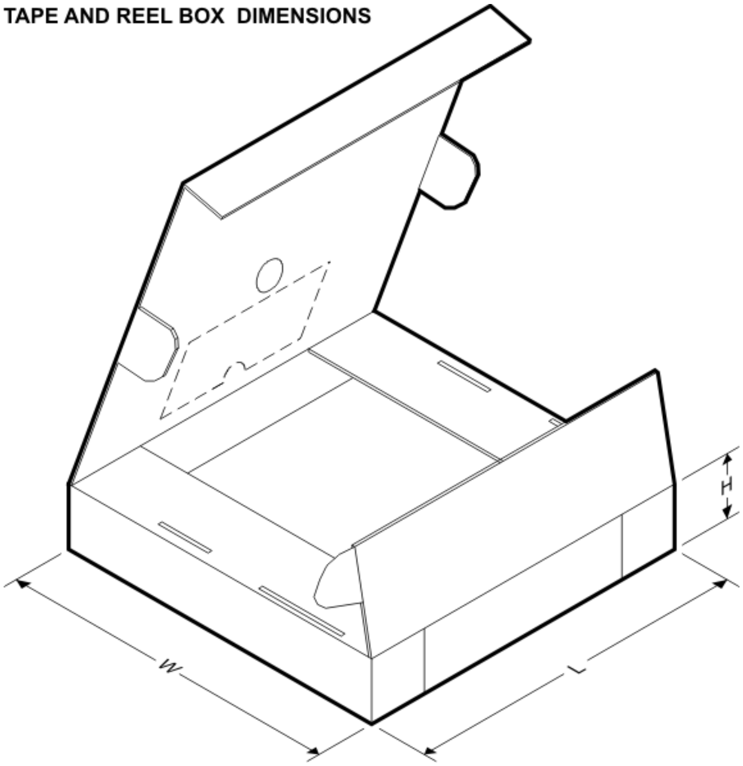
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8811PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

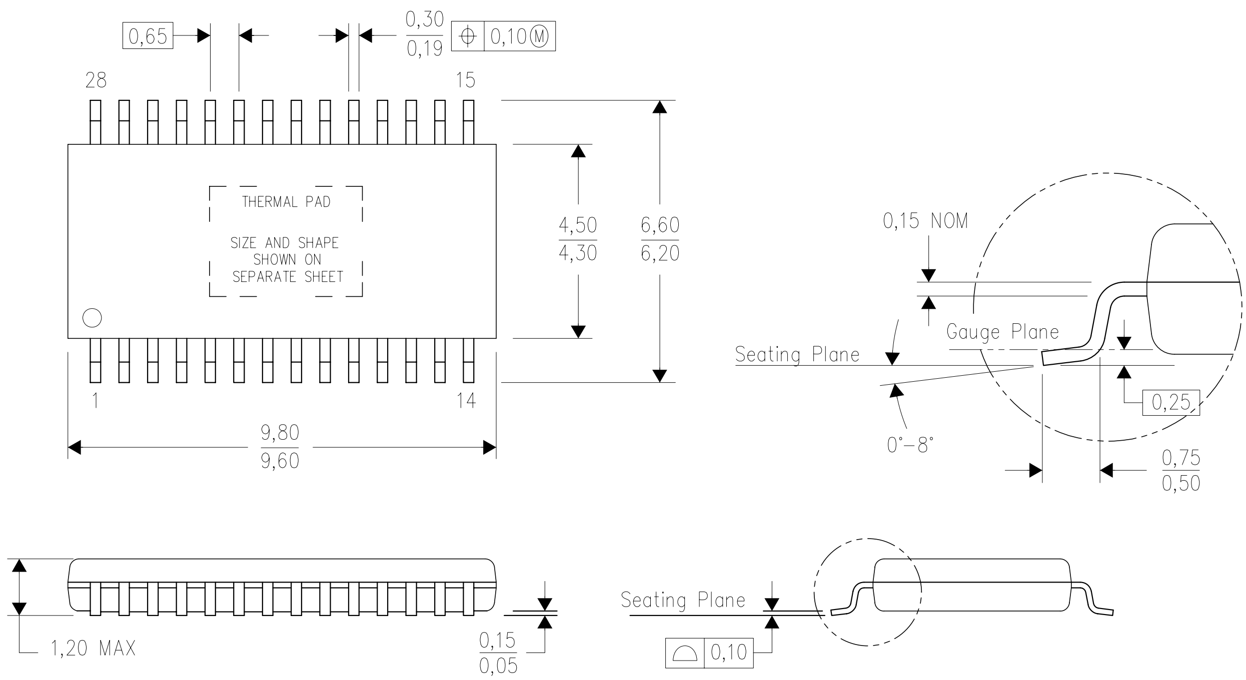
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8811PWPR	HTSSOP	PWP	28	2000	367.0	367.0	38.0

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



4073225-6/I 05/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

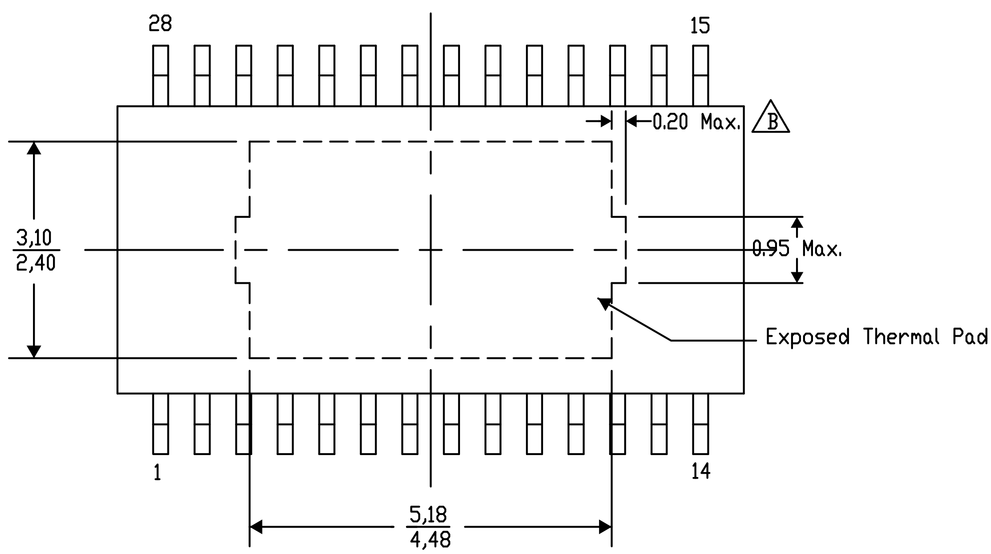
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

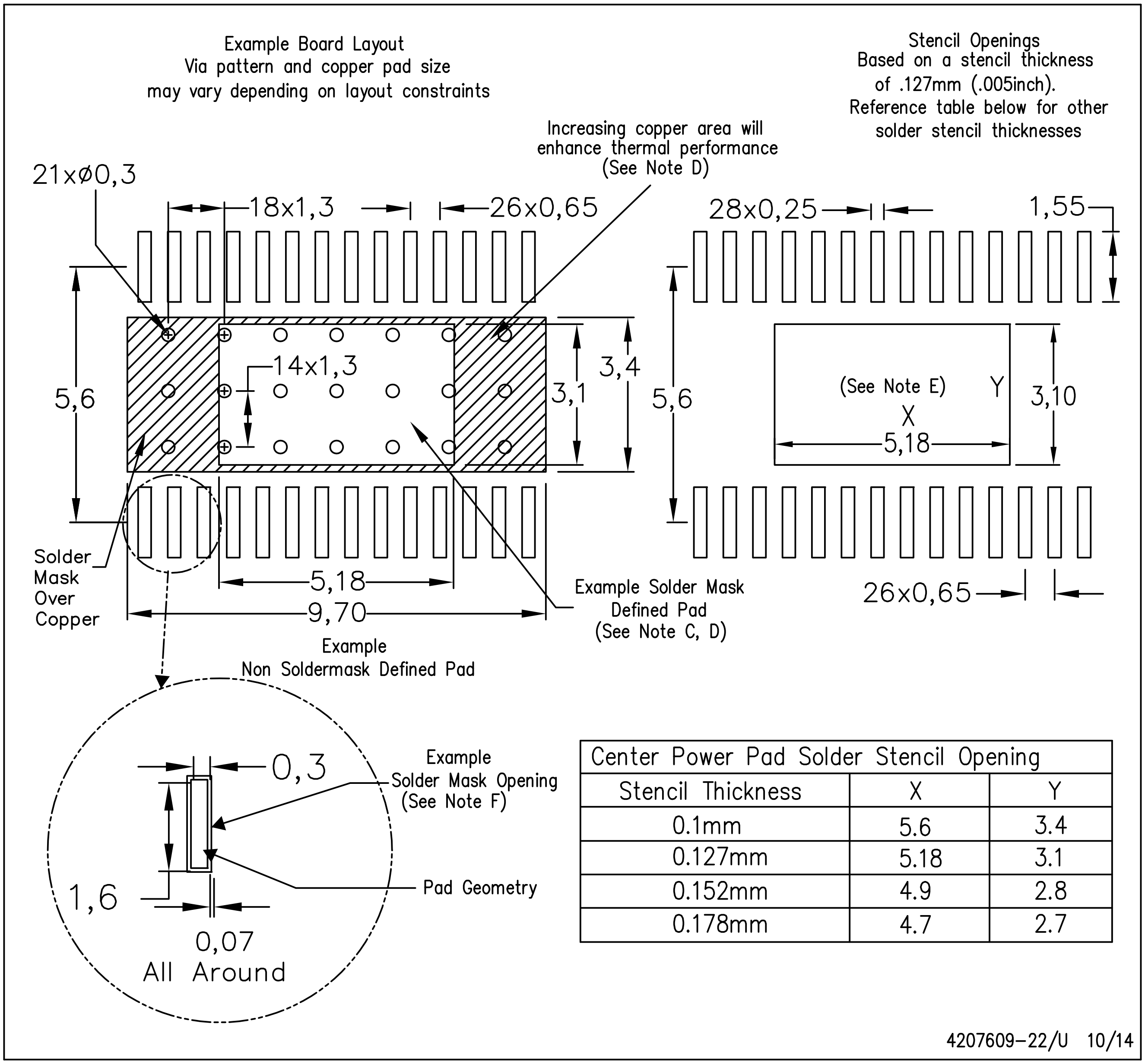
4206332–38/AJ 10/14

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.6	3.4
0.127mm	5.18	3.1
0.152mm	4.9	2.8
0.178mm	4.7	2.7

4207609-22/U 10/14

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265