P07

Radio reconfigurable

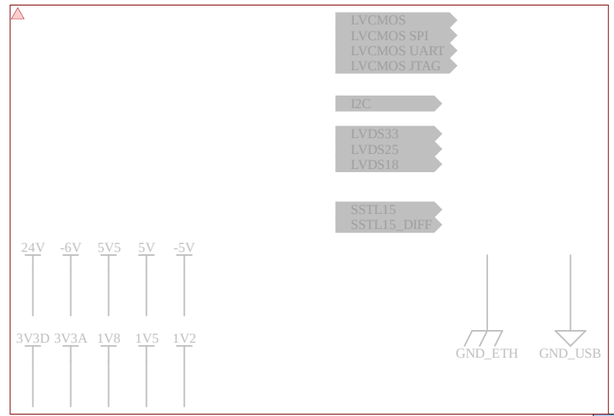
Ultracom

Revision 1.000

Date : 2021-01-13

Revision history	

Package size conversion	
Metric	*Imperial*
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512



Design notes:
Analog ground (arrow) and signal GND (normal power net) are connected together.
PCB NOTE: Segregate currents return between AGND and GND

Fiducials

FID1
FID 1MM

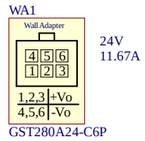
FID2
FID 1MM

FID3
FID 1MM

Mounting holes

TODO with requirements

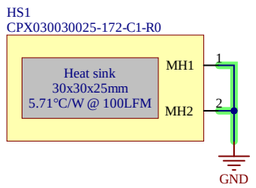
PSU



Mouse Bites

TODO with pannel

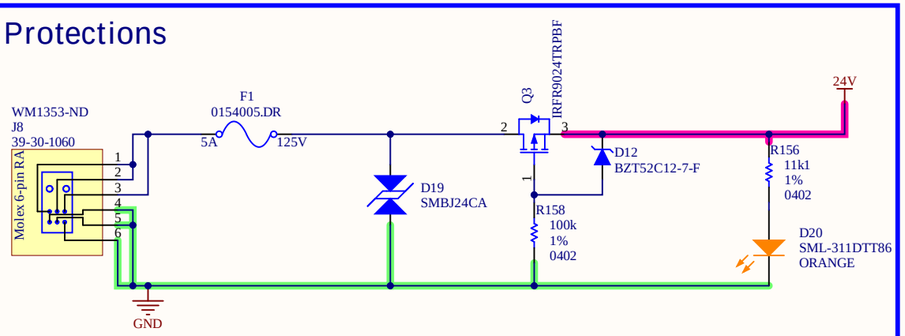
Heat sink



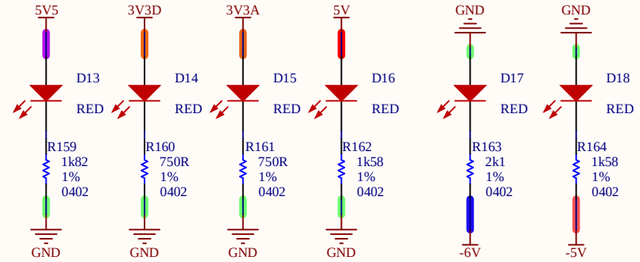
Rth HS = 5.71 °C @ 100LFM
RJC = 4 °C/W
Rth interface = 0.5°C/W
http://vendor.parker.com/852568C80043FA7A/468ea5de5ac341d385257d39005641c7/1BD00D0D0B1B018C852569580073DD53/$FILE/THERMATTACH-TAPES-THERM-CAT.pdf

Project Title	P07	
Global Project	*Radio reconfigurable*	
Size: 11x17	Group: Ultracom	Revision: 1.000
Date: 2021-01-13	Sheet: 1 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_TITLE.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin	

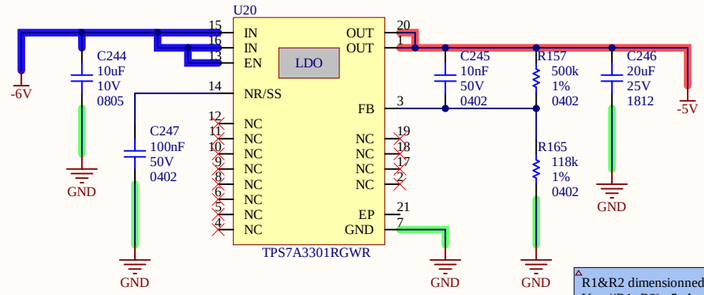
Protections



Power LEDs



-6V to -5V



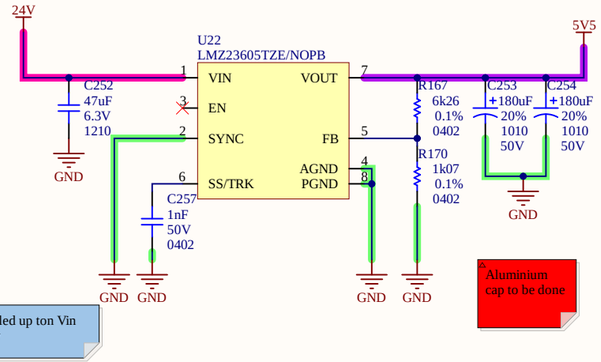
R1&R2 dimensionned to satisfy :
Vout/(R1+R2)> 5uA
R1 = R2 (Vout/Vref-1) where
Vref is -1.175

Input consumption
-330mA@-6V

Efficiency = 83%

Output consumption
-330mA@-5V

24V to 5V5



EN is pulled up ton Vin internally

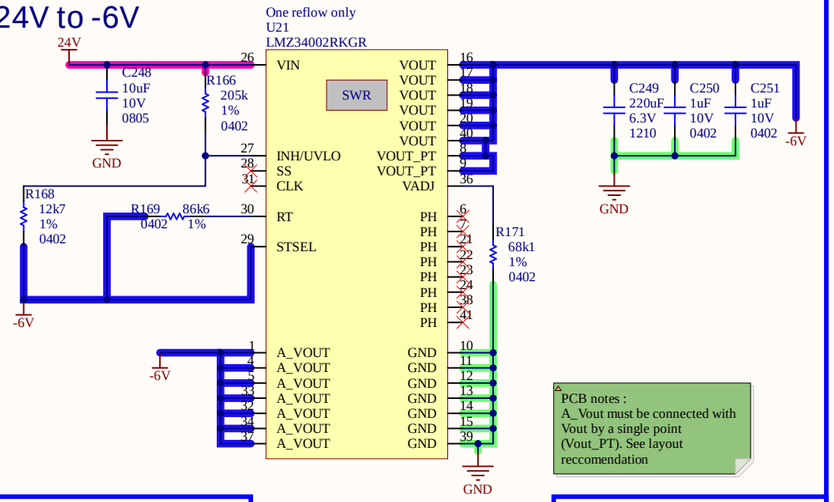
Aluminium cap to be done

Input consumption
0.93A@24V

Efficiency = 85%

Output consumption
3.45A@5V5

24V to -6V



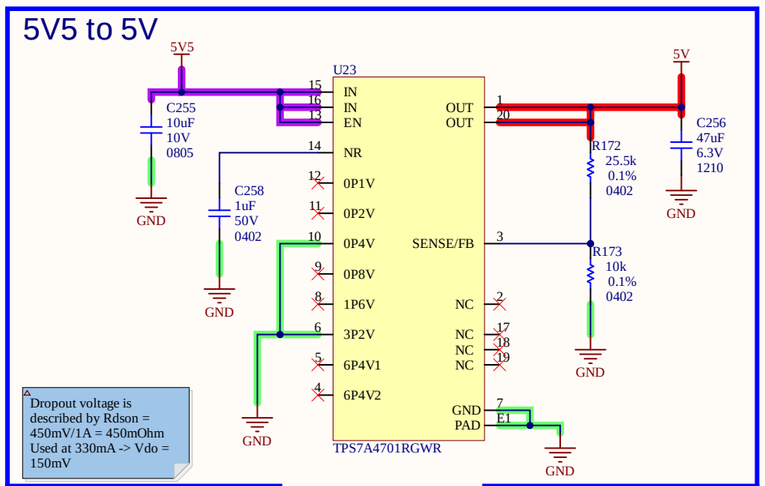
PCB notes :
A_Vout must be connected with Vout by a single point (Vout_PT). See layout reccomendation

Input consumption
110mA@24V

Efficiency = 75%

Output consumption
-330mA@-6V

5V5 to 5V



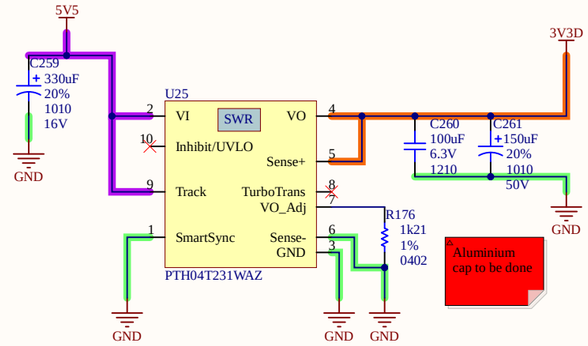
Dropout voltage is described by Rdson = 450mV/1A = 450mOhm
Used at 330mA -> Vdo = 150mV

Input consumption
330mA@5V5

Efficiency = 91%

Output consumption
330mA@5V

5V5 to 3V3D



Aluminium cap to be done

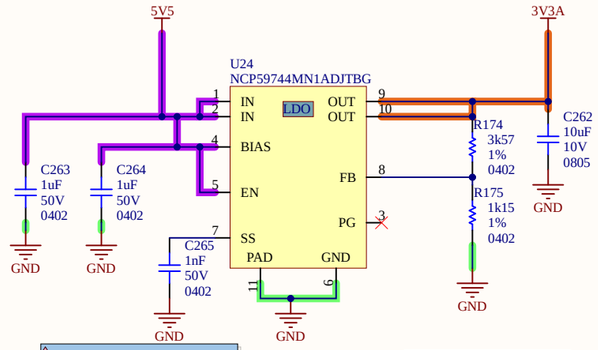
Inhibit : applying low-level = disable module. If left unconnected, Vout will be made when Vin is ok. Turbotrans changes the transient response
SmartSync synchronise the switching frequency to an external clock.. GND if unused

Input consumption
2.2A@5.5V

Efficiency = 95%

Output consumption
3.48A@3V3D

5V5 to 3V3A



SS is a soft start pin:
Time(ss) = cap(ss)*1.78 where tss = soft start time in ms and Css is in nanofarad
15nF max

If used PG pin should be connected to pullup resistor (10k to 1M) to a supply up to 5V5.

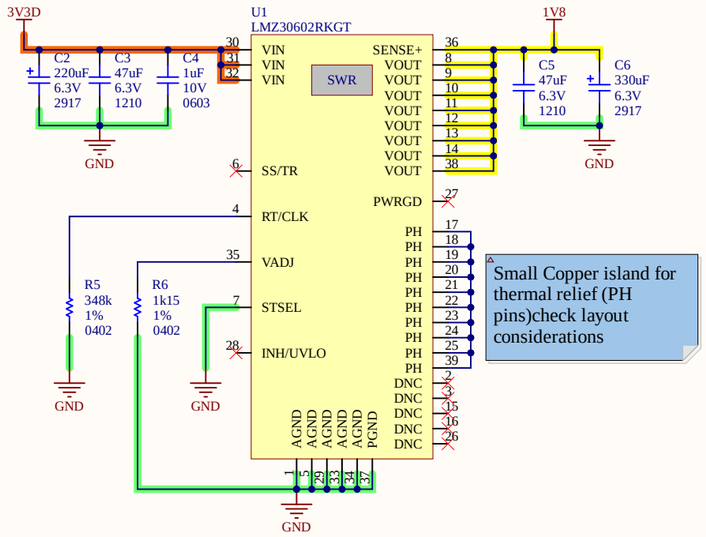
Input consumption
921mA@5V5

Efficiency = 60%

Output consumption
921mA@3V3A

Sheet Name	HIGH POWER VALUES
Project Title	P07
Global Project	*Radio reconfigurable*
Size: 11x17	Group: Ultracom — Revision: 1.000
Date: 2021-01-13	Sheet: 2 of 16
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_HIGH_POWER.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin

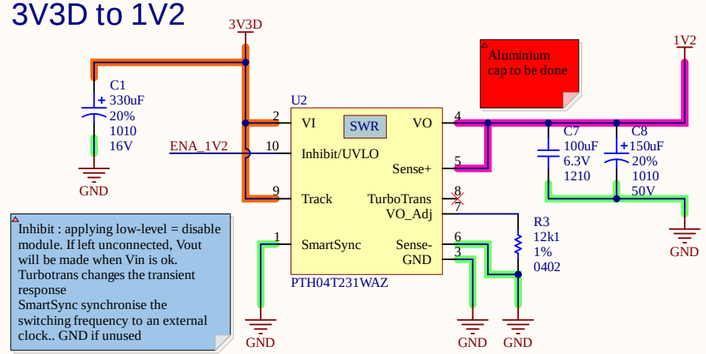
3V3D to 1V8



Small Copper island for thermal relief (PH pins)check layout considerations

Input consumption	Efficiency = 94%	Output consumption
388mA@3v3D		666mA@1V8

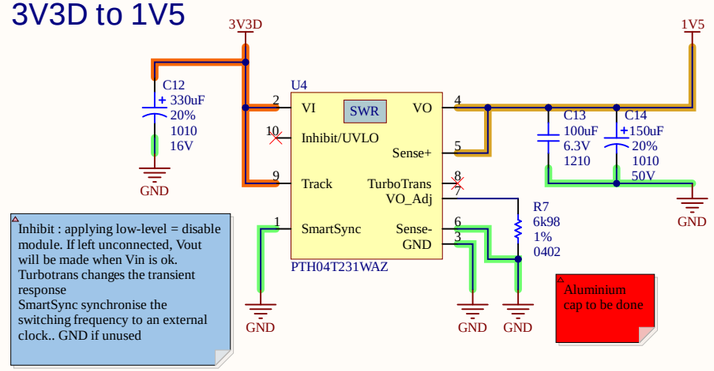
3V3D to 1V2



Inhibit : applying low-level = disable module. If left unconnected, Vout will be made when Vin is ok. Turbotrans changes the transient response
SmartSync synchronise the switching frequency to an external clock.. GND if unused

Input consumption	Efficiency = 92%	Output consumption
1.18A@3V3D		3A@1V2D

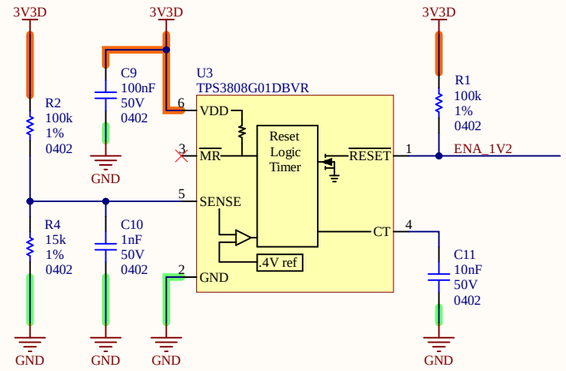
3V3D to 1V5



Inhibit : applying low-level = disable module. If left unconnected, Vout will be made when Vin is ok. Turbotrans changes the transient response
SmartSync synchronise the switching frequency to an external clock.. GND if unused

Input consumption	Efficiency = 92%	Output consumption
1.08A@3V3D		2.07A@1V5D

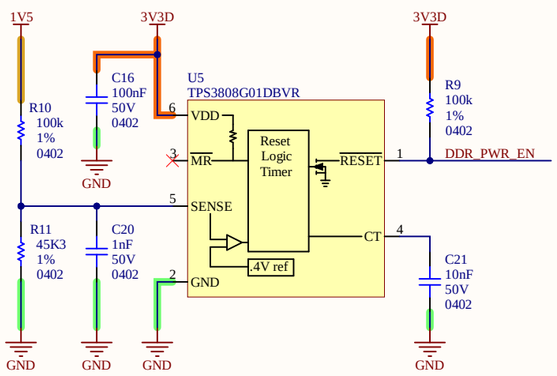
1V2 delay



Delay = 60ms
VTH = 3.05 - 3.15 V

Power consumption
40uA @ 3V3D
10uA @ 1V5

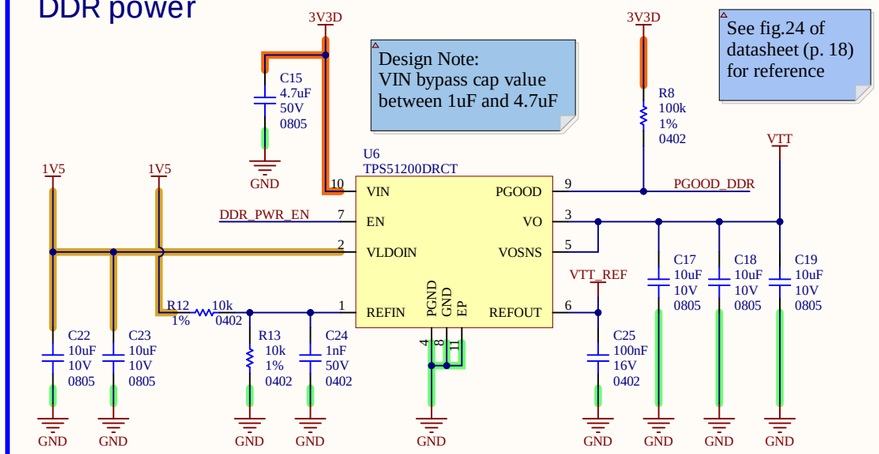
DDR power delay



Delay = 60ms
VTH = 1.28-1.32 V

Power consumption
40uA @ 3V3D
10uA @ 1V5

DDR power



Design Note:
VIN bypass cap value between 1uF and 4.7uF

See fig.24 of datasheet (p. 18) for reference

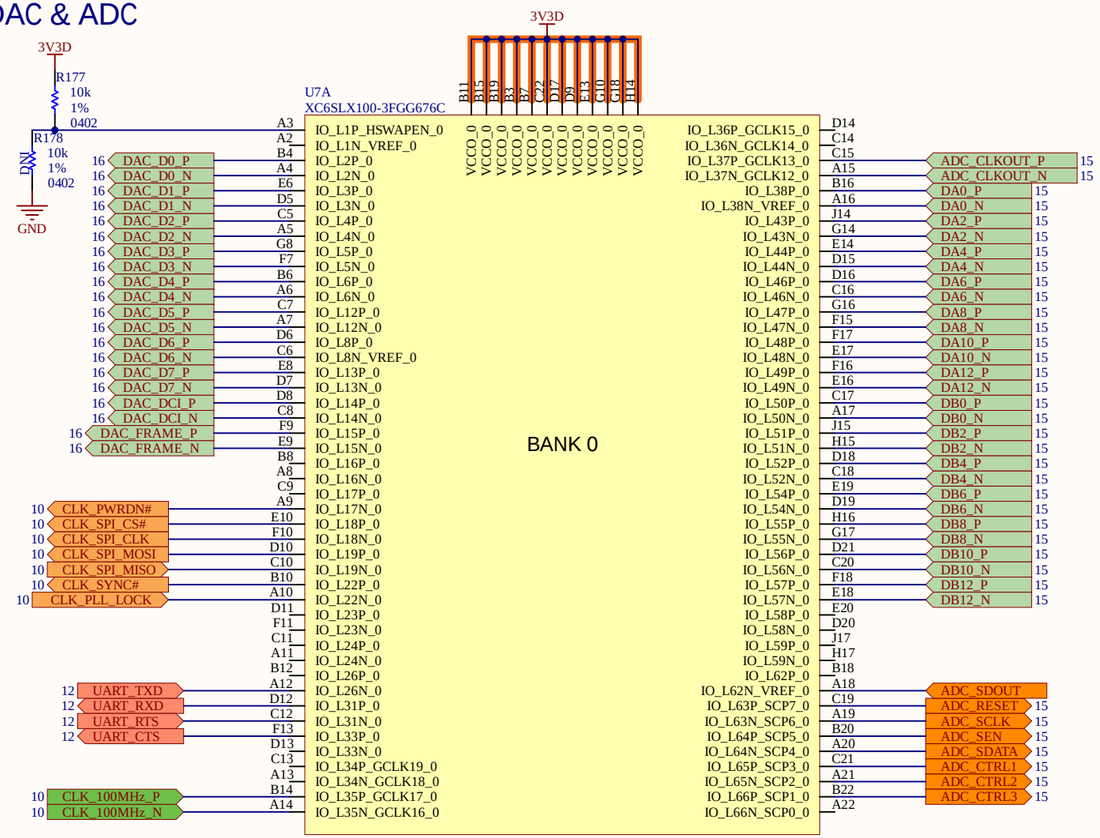
Input consumption	Efficiency = 50%	Output consumption
10mA @ 3V3 500mA @ 1V5		500mA @ VTT (0V75) 10mA @ VTT_REF (0V75)

If used PG pin should be connected to pullup resistor (10k to 1M) to a supply up to 5V5.

Only constraint of power-on sequence :
VTT (0.75V) must come after 1V5 -> 1V5 is used to make VTT
The FPGA core (1V2) must come after the flash (3V3D) -> 3V3D is used to make 1V2D
Futhermore, the PTH04T230W has a soft start feature.

Sheet Name	LOW VALUE POWER	
Project Title	P07	
Global Project	*Radio reconfigurable*	
Size: 11x17	Group: Ultracom	Revision: 1.000
Date: 2021-01-13	Sheet: 3 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_LOW_POWER.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin	

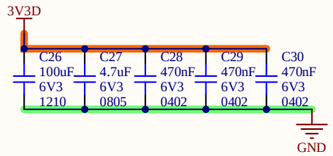
Bank 0 - 3V3 - DAC & ADC



Current consumption

100mA @ VCCO_0 (3V3)

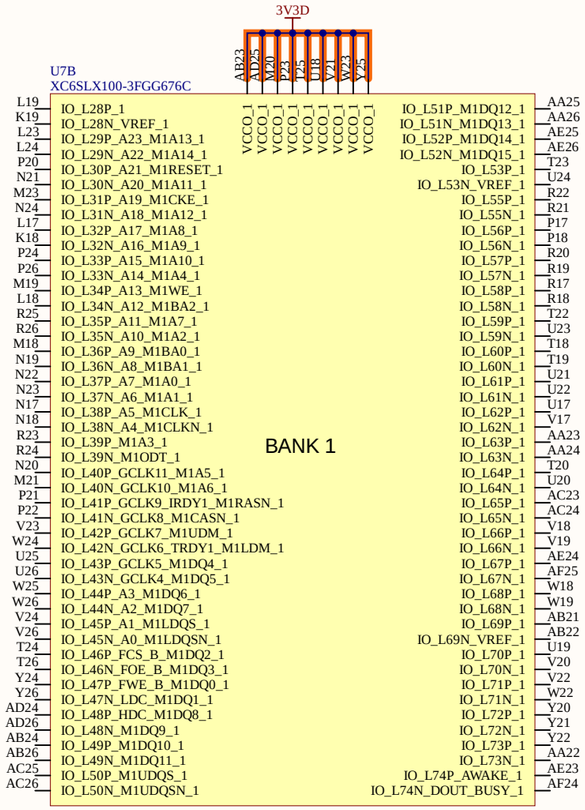
FPGA Bank 0 Decoupling Capacitors



Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

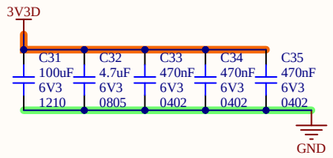
Sheet Name	FPGA_0	
Project Title	P07	
Global Project	*Radio reconfigurable*	
Size: 11x17	Group: Ultracom	Revision: 1.000
Date: 2021-01-13	Sheet: 4 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_0.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin	

Bank 1 - 3V3 - Unused



Current consumption
50mA @ VCCO_1 (3V3)

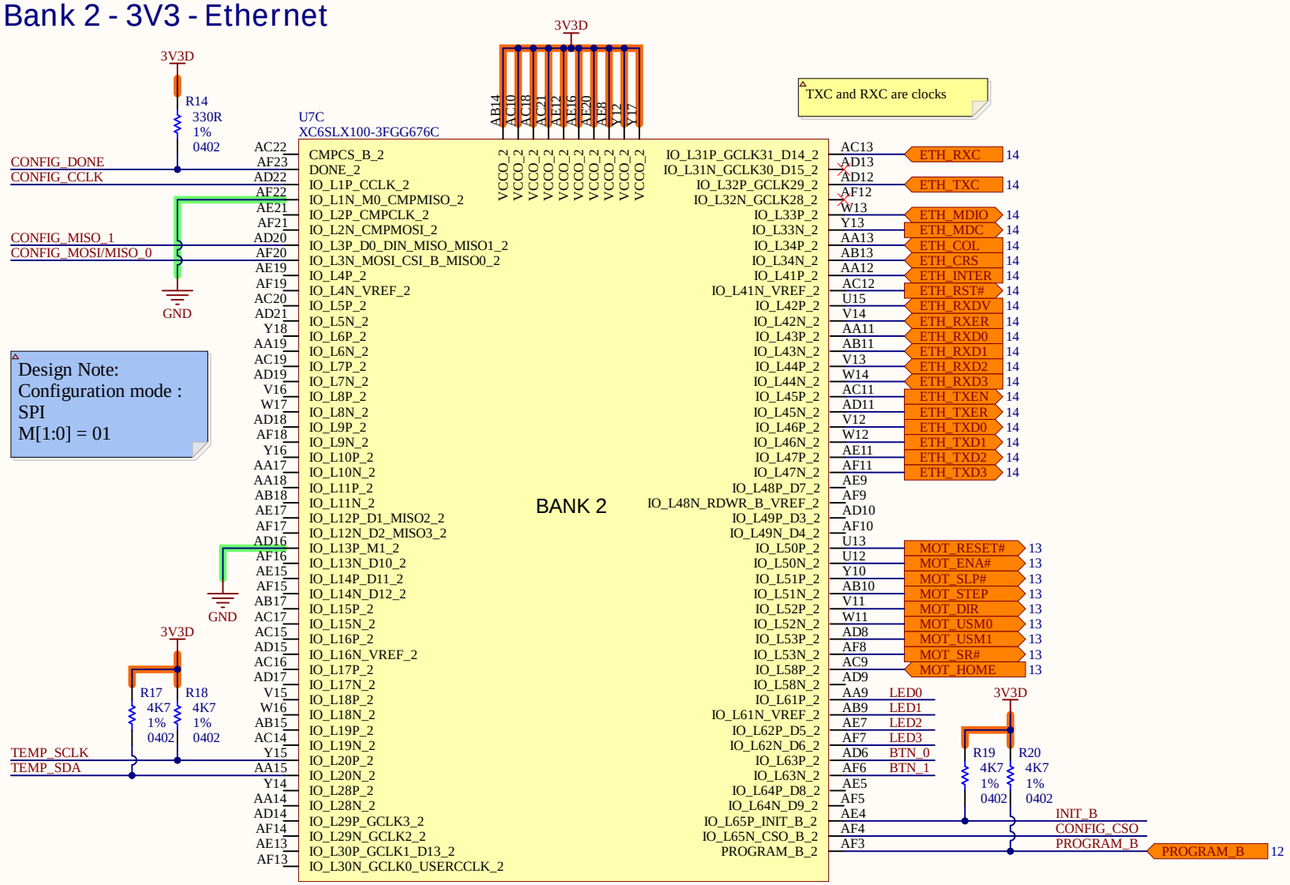
FPGA Bank 1 Decoupling Capacitors



Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Sheet Name	FPGA_1	
Project Title	P07	
Global Project	*Radio reconfigurable*	
Size: 11x17	Group: Ultracom	Revision: 1.000
Date: 2021-01-13	Sheet: 5 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_1.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin	

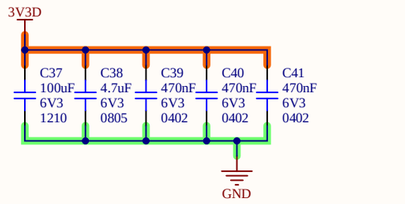
Bank 2 - 3V3 - Ethernet



Design Note:
Configuration mode :
SPI
M[1:0] = 01

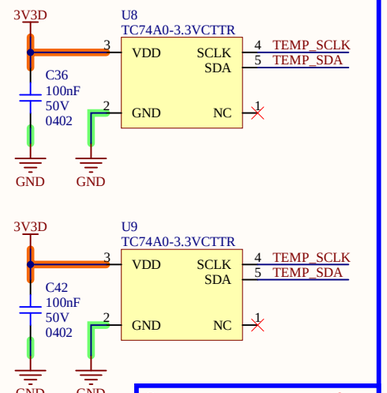
Current consumption
50mA @ VCCO_2 (3V3)

FPGA Bank 2
Decoupling Capacitors



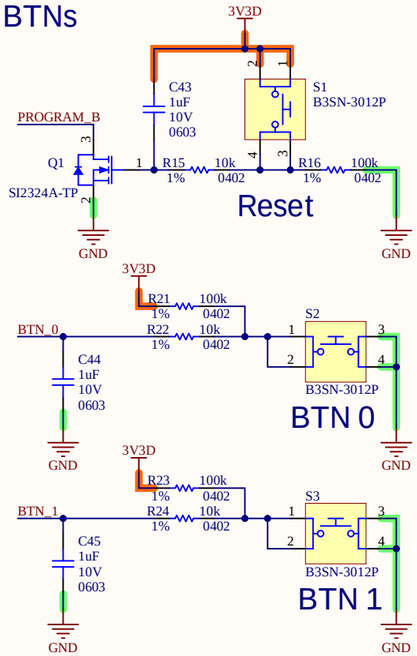
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Temperature sensors



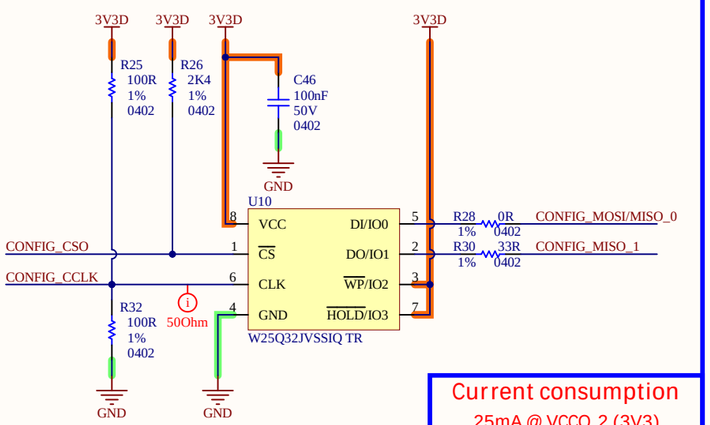
Current consumption
0.7mA @ VCCO_2 (3V3)

BTNs



Design notes - Buttons
- Debounce time 100-500ms

Configuration FLASH



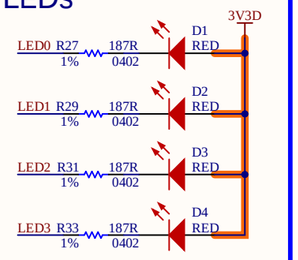
Current consumption
25mA @ VCCO_2 (3V3)

Design Note:
FPGA/FLASH power sequence:
FLASH must ready to operate when FPGA starts programing
- FLASH delays:
  - Read : 20us after VCCmin (2V7)
  - Write : 5ms after VWI (1V to 2V)
- FPGA delay :
  - Tpor : 5ms
  - VCCINT : 60ms

Design Note:
A series resistor should be considered for the datapath from the flash to the FPGA to minimize overshoot. The proper resistor value can be determined from simulation.

Design Note:
CCLK teminate with:
2x Zo = 2x50Ohm = 100Ohm to VCC and GND

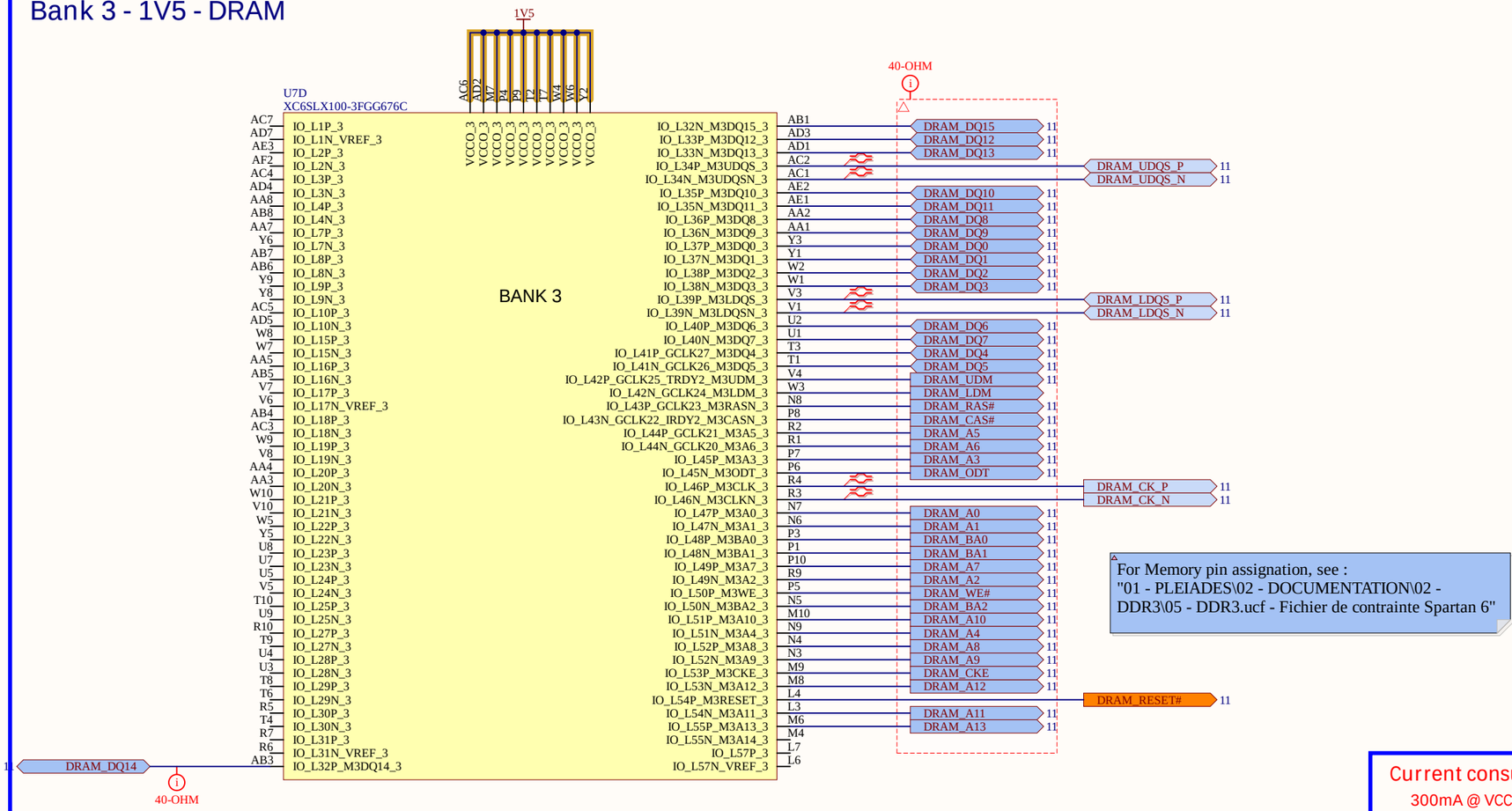
LEDs



Current consumption
32mA @ VCCO_2 (3V3)

Sheet Name	FPGA_2
Project Title	P07
Global Project	*Radio reconfigurable*
Size: 11x17 / Group: Ultracom / Revision: 1.000	
Date: 2021-01-13 / Sheet: 6 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_2.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin

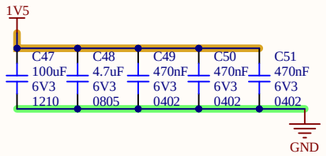
Bank 3 - 1V5 - DRAM



For Memory pin assignation, see :
"01 - PLEIADES\02 - DOCUMENTATION\02 - DDR3\05 - DDR3.ucf - Fichier de contrainte Spartan 6"

Current consumption
300mA @ VCCO_3 (1V5)

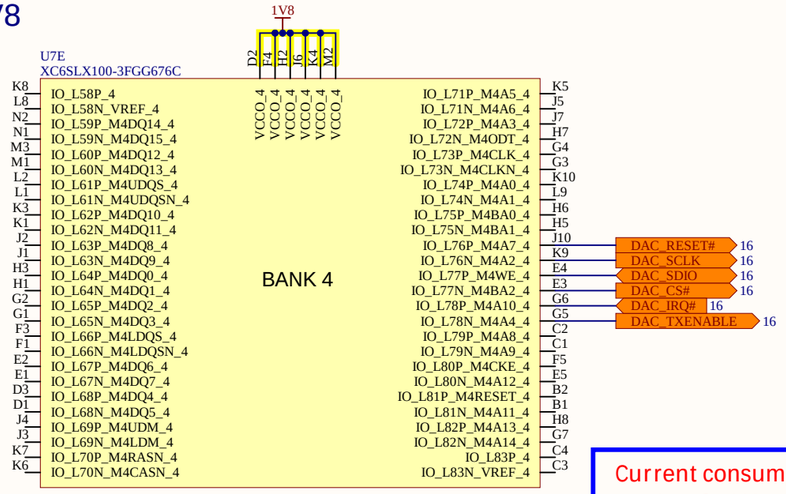
FPGA Bank 3 Decoupling Capacitors



Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Sheet Name	FPGA_3	
Project Title	P07	
Global Project	*Radio reconfigurable*	
Size: 11x17	Group: Ultracom	Revision: 1.000
Date: 2021-01-13	Sheet: 7 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_3.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin	

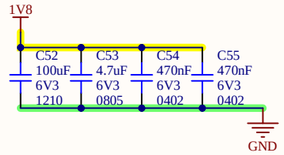
Bank 4 - 1V8



Current consumption

50mA @ VCCO_4 (1V8)

FPGA Bank 4 Decoupling Capacitors



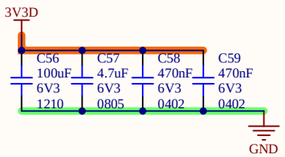
Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

Bank 5 - 3V3 (Unused)

Current consumption

50mA @ VCCO_5 (3V3)

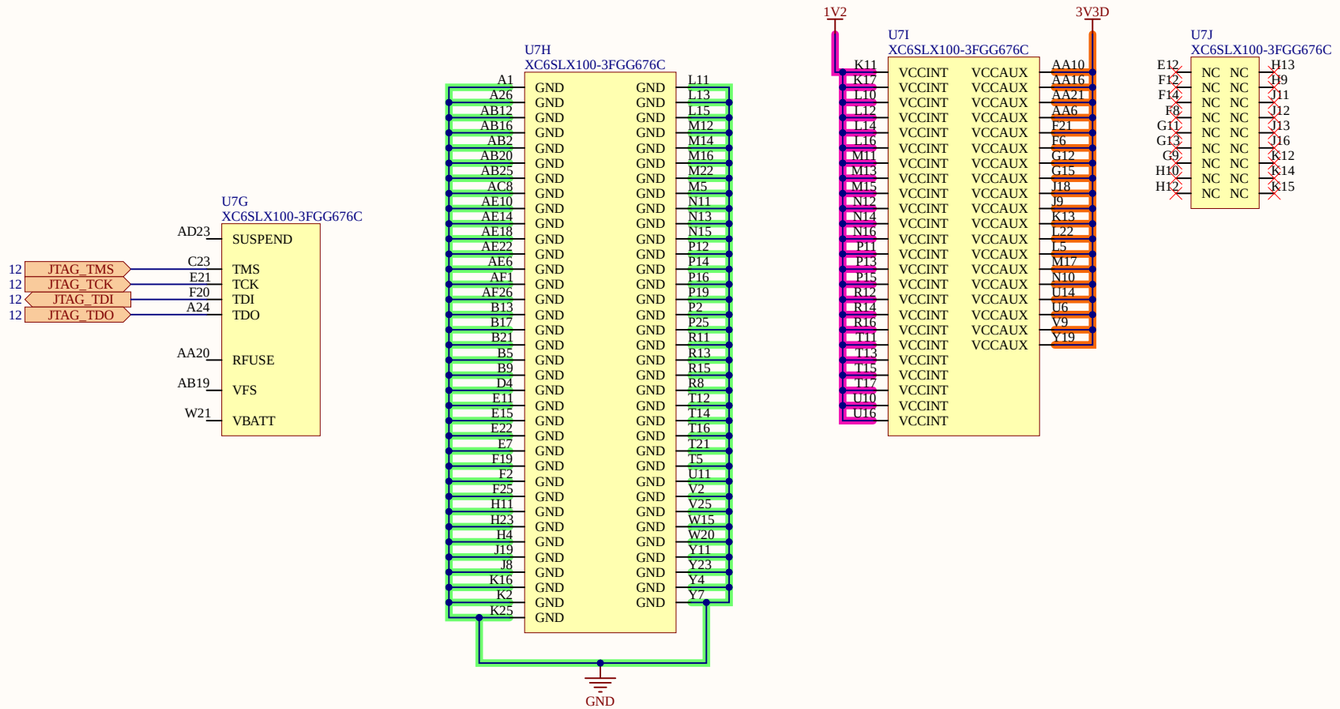
FPGA Bank 5 Decoupling Capacitors



Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

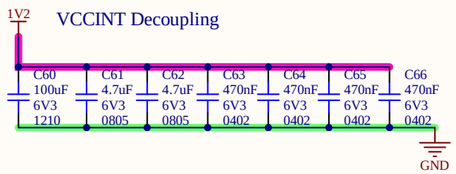
Sheet Name: FPGA_4		
Project Title: P07		
Global Project: *Radio reconfigurable*		
Size: 11x17	Group: Ultracom	Revision: 1.000
Date: 2021-01-13	Sheet: 8 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_4-5.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin	

FPGA Power Parts

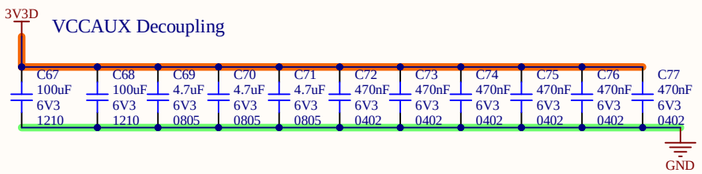


Current consumption
3A @ VCCINT (1V2)
250mA @ VCCAUX (3V3)

FPGA Decoupling Capacitors

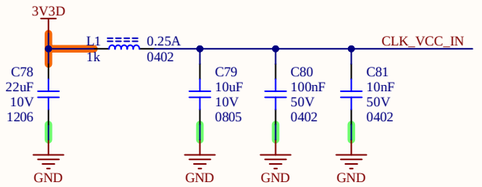


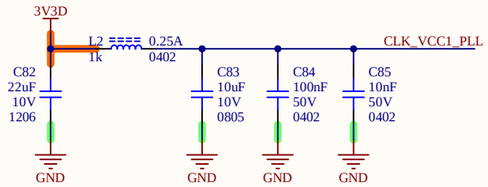
Design notes:
For all caps :
Take X5R or X7R quality.
ESL ranges 10 mOhm to 60mOhm
Smaller values closer to FPGA

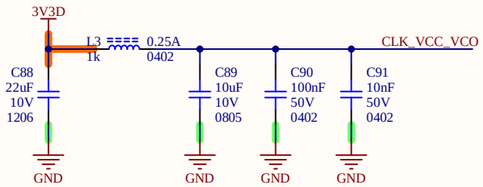


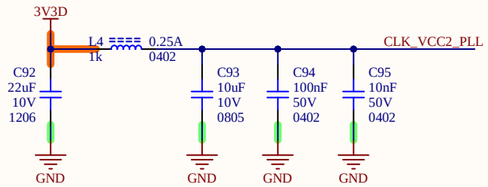
Sheet Name	FPGA_MISC	
Project Title	P07	
Global Project	*Radio reconfigurable*	
Size: 11x17	Group: Ultracom	Revision: 1.000
Date: 2021-01-13	Sheet: 9 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_FPGA_MISC.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin	

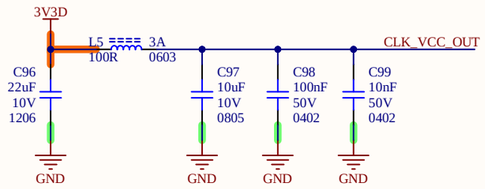
Clock power

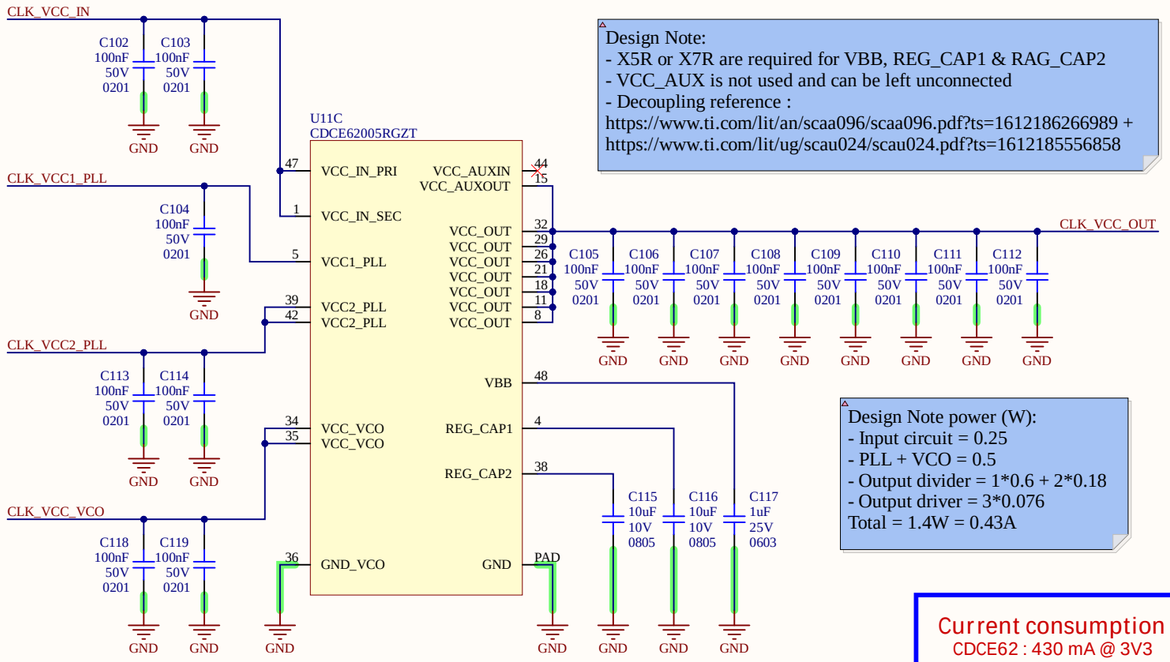










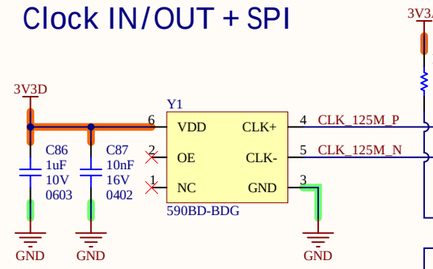


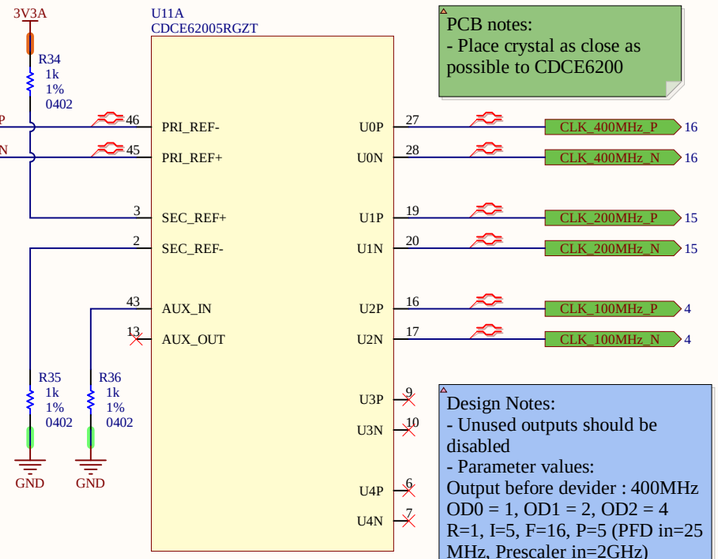
Design Note:
- X5R or X7R are required for VBB, REG_CAP1 & RAG_CAP2
- VCC_AUX is not used and can be left unconnected
- Decoupling reference :
https://www.ti.com/lit/an/scaa096/scaa096.pdf?ts=1612186266989 +
https://www.ti.com/lit/ug/scau024/scau024.pdf?ts=1612185556858

Design Note power (W):
- Input circuit = 0.25
- PLL + VCO = 0.5
- Output divider = 1*0.6 + 2*0.18
- Output driver = 3*0.076
Total = 1.4W = 0.43A

Current consumption
CDCE62 : 430 mA @ 3V3
SI590 : 100 mA @ 3V3

Clock IN/OUT + SPI





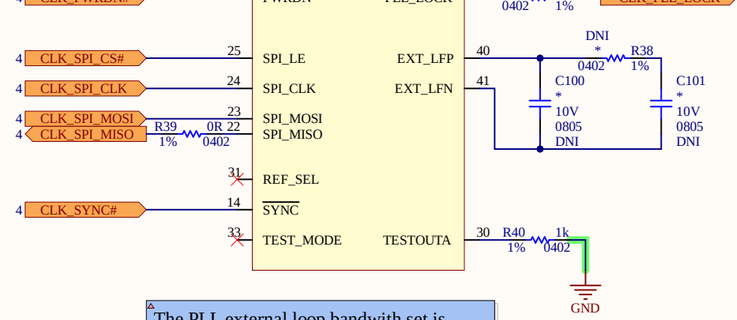
PCB notes:
- Place crystal as close as possible to CDCE6200

Design Notes 590BD-BDG:
- OE is internally pulled high with a 17kOhm resistor
- VCM = 1.2V
- Rise time = 350ps

Design Notes PRI_REF config:
- Config matrix: [5.7 5.1 5.0 5.8 5.9 5.6]
[1 1 1 0 0 1]
- > Hysteresis, LVDS, DC coupling, Internal term , Vbb = 1.2V
- Internally terminated, no external needed
- [6.25 6.24] = [X 0] to disable AUX_OUT

Design Notes:
- Unused outputs should be disabled
- Parameter values:
Output before devider : 400MHz
OD0 = 1, OD1 = 2, OD2 = 4
R=1, I=5, F=16, P=5 (PFD in=25 MHz, Prescaler in=2GHz)
- For use with ADC, see section 8.4.3.1 to minimize SNR (jitter)

Design Note:
- REF_SEL ([1] = PRI ; [0] = SEC) is internally pulled up (150kOhm)
- SYNC# is internally pulled up (150kOhm)
- PWRDN# is internally pulled up (150kOhm)
- SPI_LE must be high to load the EEPROM during rising edge of PWRDN#



The PLL external loop bandwith set is reccomended for dirty clock. The clock we use is concidered as clean enough and components are not installed normally

Sheet Name	CLOCK
Project Title	P07
Global Project	*Radio reconfigurable*
Size: 11x17	Group: Ultracom — Revision: 1.000
Date: 2021-01-13	Sheet: 10 of 16
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_CLOCK.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin

Découplage sur VTT pour minimiser la boucle de courant (conseil de Jon)

Design Note:
As per datasheet TN0453, page 4 :
Route the Vref signal 2cm away from other signal to minimize coupling

Design Note:
4 cap 0.1uF for each VDD(Q) alim
From datasheet 0.1uF are used
Look at TN-41-13: DDR3 design support p.9 for placement

Design Note:
4 cap each side of the package Datasheet

DDR3 SDRAM

MT41J128M16JT-125

U12

VTT_REF

VREFCA, VREFDQ

A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12/BC#, A13

BA0, BA1, BA2

CK, CK, CKE

UDM, LDM

CS, RESET

RAS, CAS, WE

ODT

ZQ

VDDQ, VSSQ

VDD, VSS

DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, DQ7, DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, DQ15

UDQS, UDQS

LDQS, LDQS

NC

DRAM_A0, DRAM_A1, DRAM_A2, DRAM_A3, DRAM_A4, DRAM_A5, DRAM_A6, DRAM_A7, DRAM_A8, DRAM_A9, DRAM_A10, DRAM_A11, DRAM_A12, DRAM_A13

DRAM_BA0, DRAM_BA1, DRAM_BA2

DRAM_CK_P, DRAM_CK_N, DRAM_CKE

DRAM_UDM, DRAM_LDM

DRAM_RESET#

DRAM_RAS#, DRAM_CAS#, DRAM_WE#

DRAM_DQ0, DRAM_DQ1, DRAM_DQ2, DRAM_DQ3, DRAM_DQ4, DRAM_DQ5, DRAM_DQ6, DRAM_DQ7, DRAM_DQ8, DRAM_DQ9, DRAM_DQ10, DRAM_DQ11, DRAM_DQ12, DRAM_DQ13, DRAM_DQ14, DRAM_DQ15

DRAM_UDQS_P, DRAM_UDQS_N

DRAM_LDQS_P, DRAM_LDQS_N

DRAM_ODT

VDD needed

VTT, VTT_REF, 1V5

Current consumption
560 mA @ VDD & VDDQ (1V5)

Design Note:
- Clock termination : 800MHz
CLK_P - 40Ohm - CAP to GND - 40Ohm - CLK_N
- Cap value:
Minimal impedance 0.2Ohm@ f = 814MHz
Value = 100pF
Ref:GRM1555C2A101JA01, murata sim

VTT must come after VDDQ

VTT transient current can be as high as ±3.5A during heavy activity on the DQ and address buses. This transient current averages 0A, but can be somewhat random in nature, depending upon address/data patterns.

Sheet Name	DDR	
Project Title	P07	
Global Project	*Radio reconfigurable*	
Size: 11x17	Group: Ultracom	Revision: 1.000
Date: 2021-01-13	Sheet: 11 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_DDR.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin	

PCB notes :
GND and GND_ETH must be separeted with as much space as possible, ensuring 1.5KV of isolation

GND_USB GND

2.5 KV

U13
SI8620BB-B-IS
VDD1 VDD2 A1 B1 A2 B2 GND1 GND2 2.5kV ISOLATION

C151 100nF 50V 0402
C152 100nF 50V 0402
C159 100nF 50V 0402
C160 100nF 50V 0402
C161 100nF 50V 0402
R71 10k 1% 0402
R72 10k 1% 0402
C153 10uF 10V 0805
C154 100nF 50V 0402
C155 100nF 50V 0402
C156 10uF 10V 0805
C157 100nF 50V 0402
C158 10uF 10V 0805

VBUS_USB
3V3D
GND
GND_USB
VBUS_DETECT
USB_VDD1

Design notes - JTAG SMT3
- PS_SRTS_B is oped drain; a 4.7Kohm resistor is placed on the FPGA_2 sheet
- Power consumption : https://forum.digilentinc.com/topic/17862-jtag-smt3-nc/#comment-45773

PCB notes:
Place termination resistors as close to the IC output as possible

PCB notes
- Place D+/D- termination 24Ohm resistor as close as possible to the isolator
- Place protection diodes as close as possible to the USB connector

C162 10uF 10V 0805
C163 100nF 50V 0402
R73 50R 1% 0402
USB_SPU

J1
10118194-0001LF
Micro USB 2.0 Type B
VBUS D- D+ ID GND SHIELD

USB_IN_N
USB_IN_P
DNI
R83 0R 1% 0402
SHIELD_USB

ISO1
VBUS1 VDD1 PDEN SPU UD- UD+ GND1 GND1
VBUS2 VDD2 PIN SPD DD- DD+ GND2 GND2
2.5 kV Isolation
ADUM3160BRWZ-RL

USB_PIN
USB_SPD
R78 24R 1% 0402 USB_IN_DIR_N
R81 24R 1% 0402 USB_IN_DIR_P
USB_ISO_DIR_N
USB_ISO_DIR_P
R79 24R 1% 0402 USB_ISO_N
R82 24R 1% 0402 USB_ISO_P

C164 100nF 50V 0402
TPD2E001DRLR
D5
GND VCC IO1 IO2

C165 1nF 3kV 1812

PCB notes:
Place D+/D- termination 24Ohm resistor as close as possible to the isolator

USB speed is limited to 12Mbps

M1
410-357-B
VDD VREF_UART VREF_JTAG VBUS_DETECT USB_DM USB_DP GND GND GND PS_SRST_B

TCK TDO TDI TMS
R74 0R 1% 0402
R75 0R 1% 0402
R76 0R 1% 0402
JTAG_TCK JTAG_TDO JTAG_TDI JTAG_TMS

TXD(OUT) RXD(IN)
R77 0R 1% 0402
UART_TXD UART_RXD

RTS(OUT) CTS(IN)
R80 0R 1% 0402
UART_RTS UART_CTS

PROGRAM_B

VDD needed
3V3D

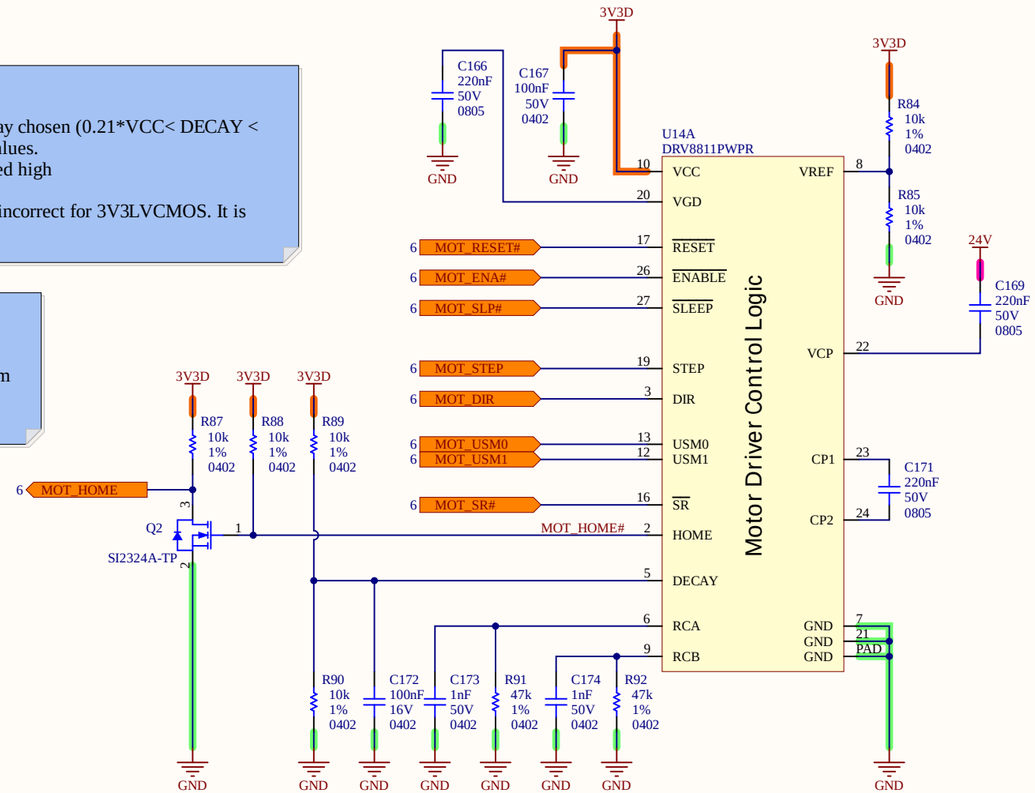
Current consumption
262 mA @ 3V3
40 mA@ VREF (3V3)

Sheet Name	USB	
Project Title	P07	
Global Project	*Radio reconfigurable*	
Size: 11x17	Group: Ultracom	Revision: 1.000
Date: 2021-01-13	Sheet: 12 of 16	
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_USB.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin	

Motor driver

Design notes - DRV8811:
- VCC = 3 to 5.5V
- No decay mode specified. Mixed decay chosen (0.21*VCC< DECAY < 0.6*VCC) with common application values.
- RESET# & ENA# are internally pulled high
- All other inputs aure pulled low
- MOT_HOME's logic levels could be incorrect for 3V3LVCMOS. It is therefore inverted and redriven

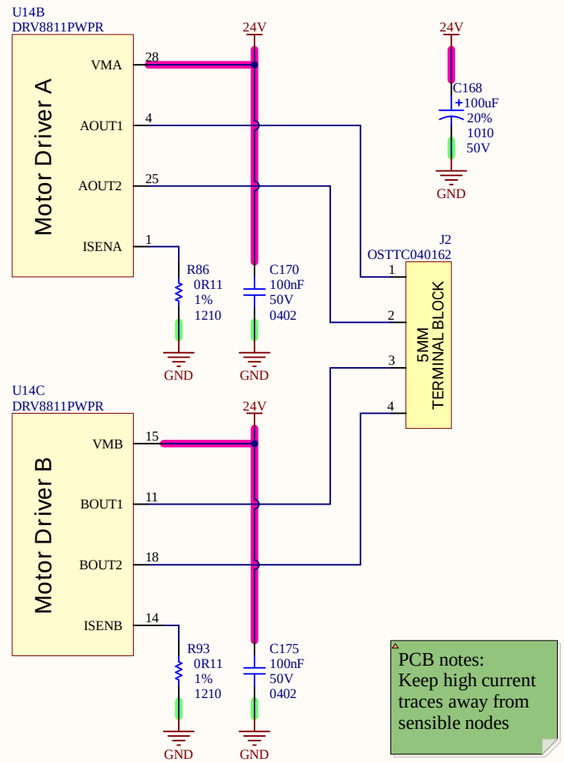
Design notes DRV8811 - ISENSE:
Current (per winding) = 1.9A
1.9A = Vref / (8*Rsense)
Rsense = 1.65V/(8 * 1.9A) = 108mOhm
Rsense actual = 110mOhm
Imax actual = 1.875A



Current consumption
8mA @ VMOT (24V)
4mA @ VCC (3V3)

VDD needed
24V
3V3D

Drive power output + bulk capacitors



PCB notes:
Keep high current traces away from sensible nodes

Current consumption
3.8A @ VMOT (24V)

Sheet Name	MOT		
Project Title	P07		
Global Project	*Radio reconfigurable*		
Size: 11x17	Group: Ultracom		Revision: 1.000
Date: 2021-01-13	Sheet: 13 of 16		
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_MOT.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin		

Ethernet PHY, MAG & RJ-45

Design notes - KZ8091
- MDC is Internal Pull-up
- For interrupt (when active low) and PME, requires external 1.0k pullup to DVDD (pin21)
- Strap states were skipped becaus the FPGA can use the rigth states and reset the device. For strap options, see table 2-2 on page 9 of the datasheet

Recommended reset circuit (p.6 DS)

Design note - decoupling:
- 22uF + 100nF for VDDA + VDDIO
- 2.2uF + 100nF for VDD_1
- Ferrite from dev kit

PCB notes : Place termination resistor as close as possible to chip output

Decision : VDDIO 3V3 -> Easier to route (Same bank). Uses 12 mW less power in 2V5 and 20mW less power in 1V8.

PCB notes : GND and GND_ETH must be separeted with as much space as possible, ensuring 1.5KV of isolation

GND | GND_ETH — 1.5 KV

GND_ETH | GND — 1.5 KV

U15 KSZ8091MNXCA

T1 H1102NLT

J3 RJHSE-5385

50-OHM

FPGA output 50OHM: ETH_MDIO, ETH_MDC

ETH_COL, ETH_CRS, ETH_INTER, ETH_RXDV, ETH_RXER, ETH_RXD0, ETH_RXD1, ETH_RXD2, ETH_RXD3, ETH_RXC

FPGA output 50OHM: ETH_TXEN, ETH_TXER

ETH_TXD0, ETH_TXD1, ETH_TXD2, ETH_TXD3, ETH_TXC

Diff terminated internally p.4 Datasheet

Design note - ASDMB-25.000MHZ
- Datasheet recommends 10nF between pin 2 and 4
- If standby pull high, osc active
if standy pull low osc inactive

Y2 ASDMB-25.000MHZ-LC-T

XO is NC if external clock is used. 25Mhz de clock Crystal 25MHz 50 ppm is used

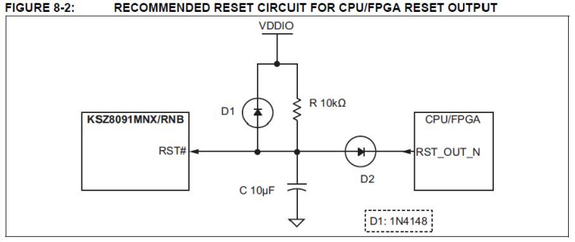
VDD needed: 3V3D, 3V3A

Current consumption

PHY chip
34 mA @ VDD (3V3)
13 mA @ VDDIO (3V3)
Osc 25MHz
15mA @ VDD (3V3)

Total
49mA @ VDD (3V3)
13 mA @ VDDIO (3V3)

FIGURE 8-2: RECOMMENDED RESET CIRCUIT FOR CPU/FPGA RESET OUTPUT



Sheet Name	ETH		
Project Title	P07		
Global Project	*Radio reconfigurable*		
Size: 11x17	Group: Ultracom		Revision: 1.000
Date: 2021-01-13	Sheet: 14 of 16		
Filename: S7CAS-PLEIADES-CARTE-MERE_P07_ETH.SchDoc	Designers: Philippe Arsenault, Louis-Daniel Gaulin		

OP AMP + Filter + ADC Input

TVS capacitane: 1pF

PCB notes :
Place TVs diodes as close as possible to the connector
Place ADA4927 feedback and termination resistors as close as possible to the chip

Design note - Decoupling
- Per net input(eg. VS1, VS2): 100nF and 1nF recommended by datasheet
- Per supply (eg. VSx): 10uF tantalum reccomended by datasheet

Verify matched length rule for ADC output
It is the first time I try it

PCB note:
Ground plane must be removed under RG&RF (-FB, +IN) see datasheet p.23

Pas oublier le 100Ohm à la FPGA

Design note - filter ref:
https://www.ti.com/lit/an/slwa053b/slwa053b.pdf?ts=1611374664037&ref_url=https%253A%252F%252Fwww.google.com%252F
page 2

Bulk decoupling capacitor for ADA4927

DAC matched length

U16A
ADS62P48IRGCT

U16B
ADS62P48IRGCT

U17A
ADA4927-2YCPZ-R2

U17B
ADA4927-2YCPZ-R2

J4
5-1814400-1
SE_50_OHM

J5
5-1814400-1
SE_50_OHM

D8 TPD1E1B04DPYR

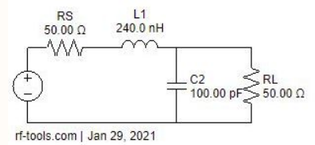
D9 TPD1E1B04DPYR

VCM_ADC

ADCIN_A_N ADCIN_A_P

ADCIN_B_N ADCIN_B_P

2nd Order Butterworth Lowpass
Cutoff Frequency = 45.00 MHz



rf-tools.com | Jan 29, 2021

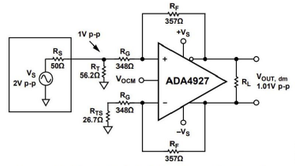


Figure 54. Terminated Single-Ended-to-Differential System with G = 1

ADC FPGA comm

U16C
ADS62P48IRGCT

DAC matched length

Verify matched length rule for ADC output
It is the first time I try it

ADC power

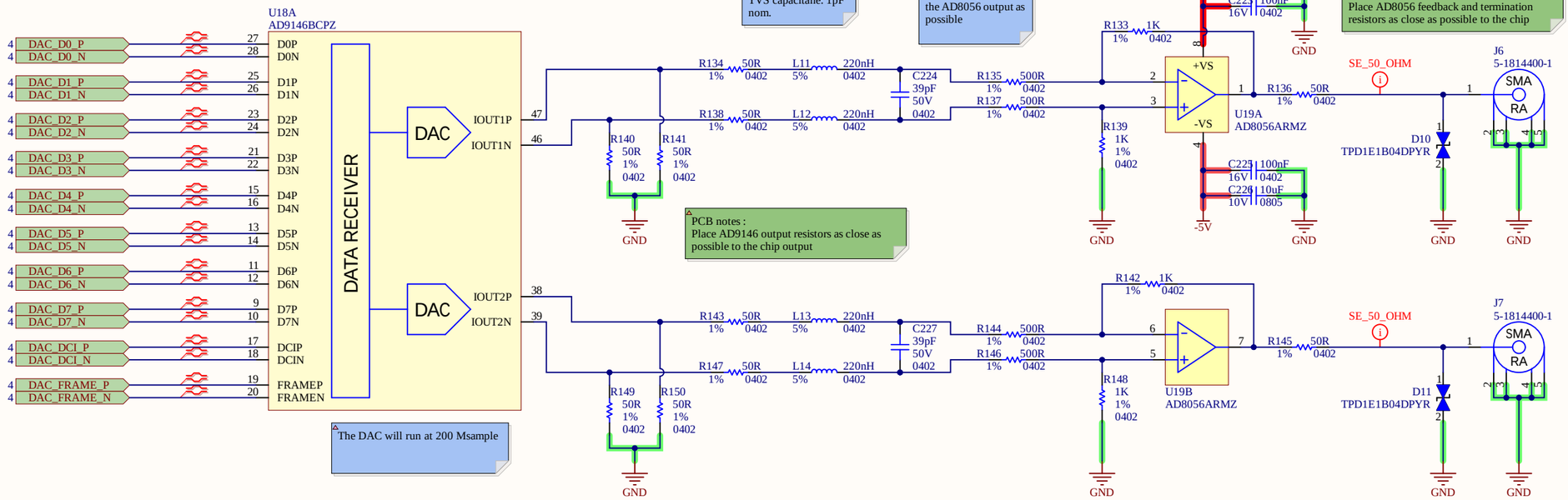
U16D
ADS62P48IRGCT

VDD needed

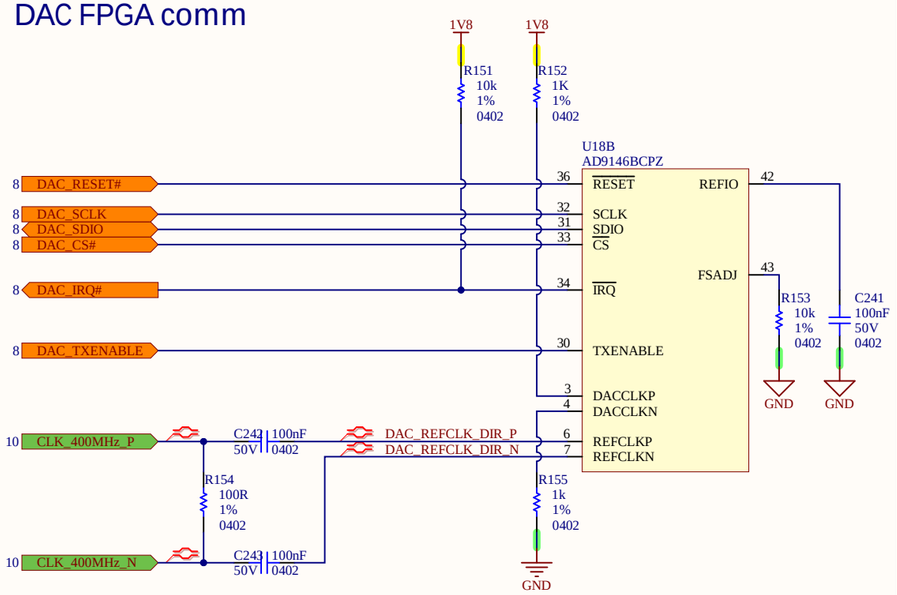
Current consumption
320mA @ AVDD (3V3)
165mA @ DRVDD (1V8)
110mA @ 5V

Sheet Name	ADC
Project Title	P07
Global Project	*Radio reconfigurable*
Size	11x17
Group	Ultracom
Revision	1.000
Date	2021-01-13
Sheet	15 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_ADC.SchDoc
Designers	Philippe Arsenault Louis-Daniel Gaulin

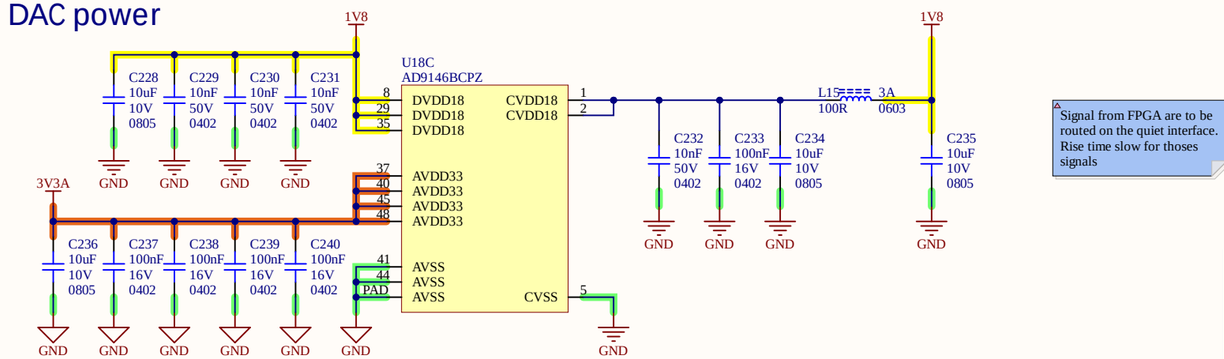
DAC output + filter + OP AMP



DAC FPGA comm



DAC power



Sheet Name	DAC
Project Title	P07
Global Project	*Radio reconfigurable*
Size	11x17
Group	Ultracom
Revision	1.000
Date	2021-01-13
Sheet	16 of 16
Filename	S7CAS-PLEIADES-CARTE-MERE_P07_DAC.SchDoc
Designers	Philippe Arsenault Louis-Daniel Gaulin