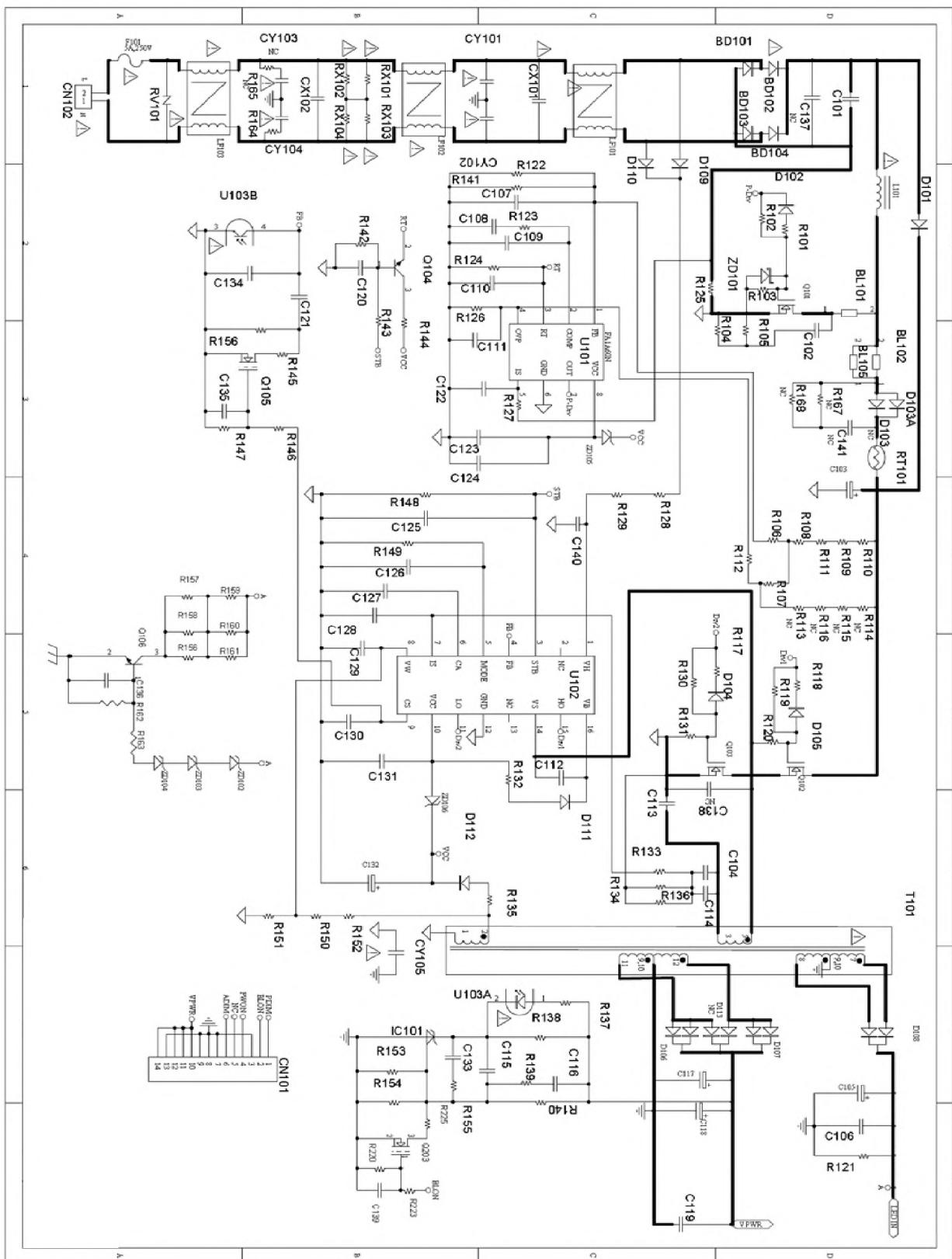
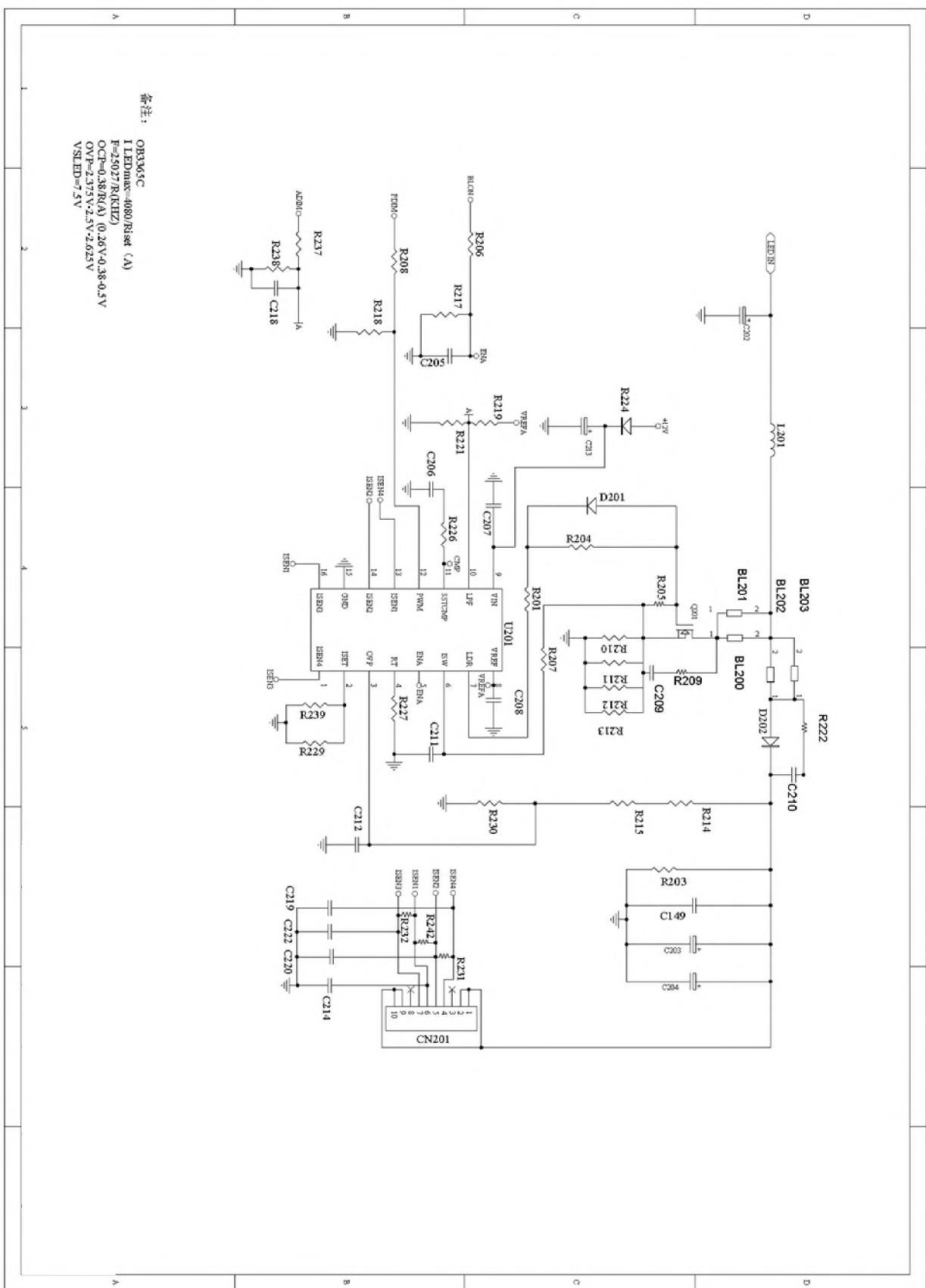


8 线路图 (CIRCUIT SCH)

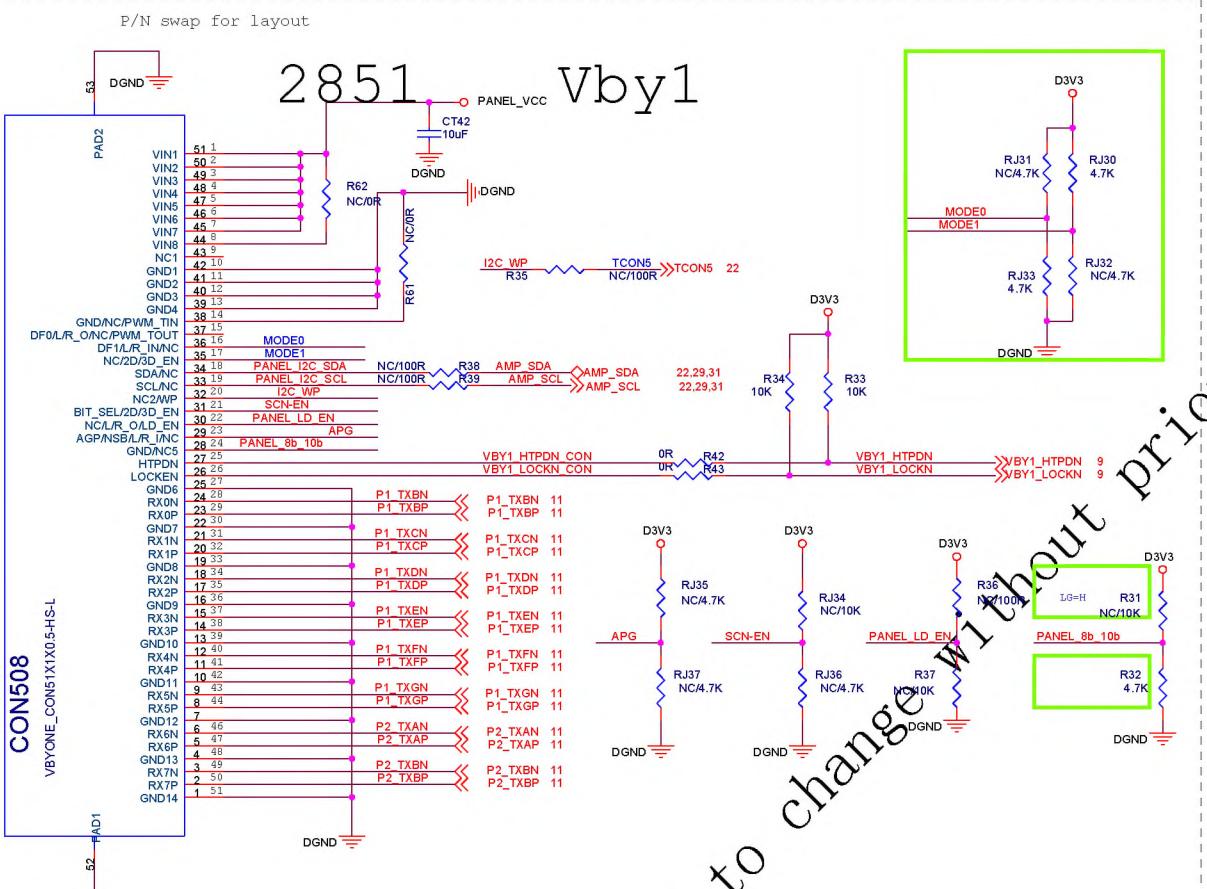


AC-DC 部分



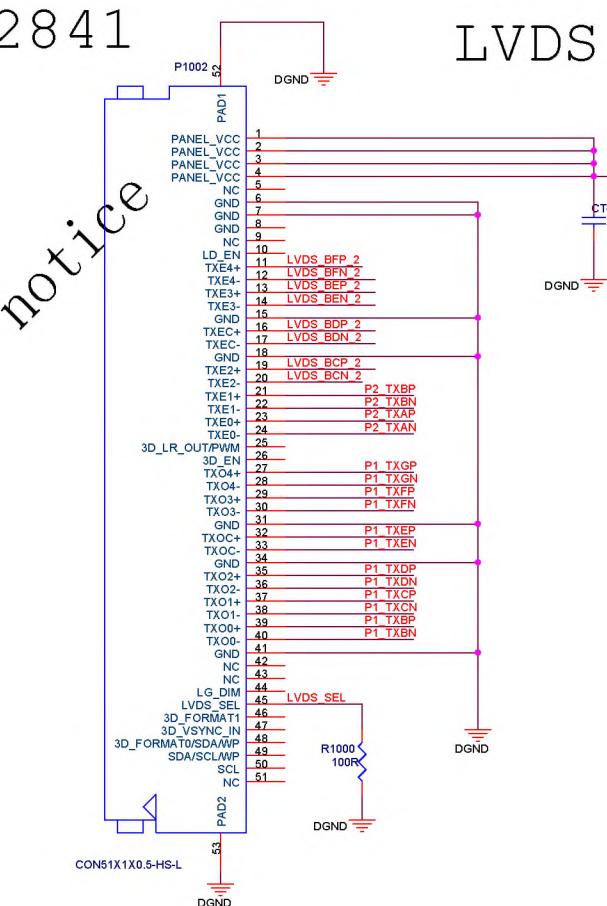
LED 驱动部分

9. 原理图



The schematic diagram illustrates a complex electronic circuit with the following key components and connections:

- Power and Ground:** Various power supplies (D3V3) and ground connections (DGND) are distributed throughout the circuit.
- Serial Communication:** The circuit includes multiple serial communication paths:
 - A top path involving TCON5, TCON5, R35, and R36.
 - A middle path involving AMP_SDA, AMP_SCL, AMP_SCL, R42, R43, and VBY1_HTPDN.
 - A bottom path involving TXBN, TXBP, TXCN, TXCP, TXDN, TXDP, TXEN, TXEP, TXFN, TXFP, TXGN, TXGP, TXAN, TXAP, and TXBN, TXBP.
- Resistors:** Numerous resistors are used for biasing and protection, including R34 (10K), R33 (10K), RJ35 (NC/4.7K), RJ34 (NC/10K), RJ36 (NC/4.7K), R37 (NC/10K), RJ33 (4.7K), RJ32 (NC/4.7K), and R32 (4.7K).
- Switches:** Two sets of switches are shown, each consisting of two parallel paths. One set is controlled by MODE0 and MODE1, and the other is controlled by VBY1_HTPDN and VBY1_LOCKN.
- Panel Control:** The circuit includes logic for panel control, such as PANEL_LD_EN and PANEL_Bd_10b.
- Red Boxes:** Two red boxes highlight specific areas of the circuit:
 - A red box labeled 'without prior notice' covers the area around the MODE0/MODE1 switch and the RJ33/RJ32 resistors.
 - A red box labeled 'to change' covers the area around the TXEN/TXEP and TXFN/TXFP pins.

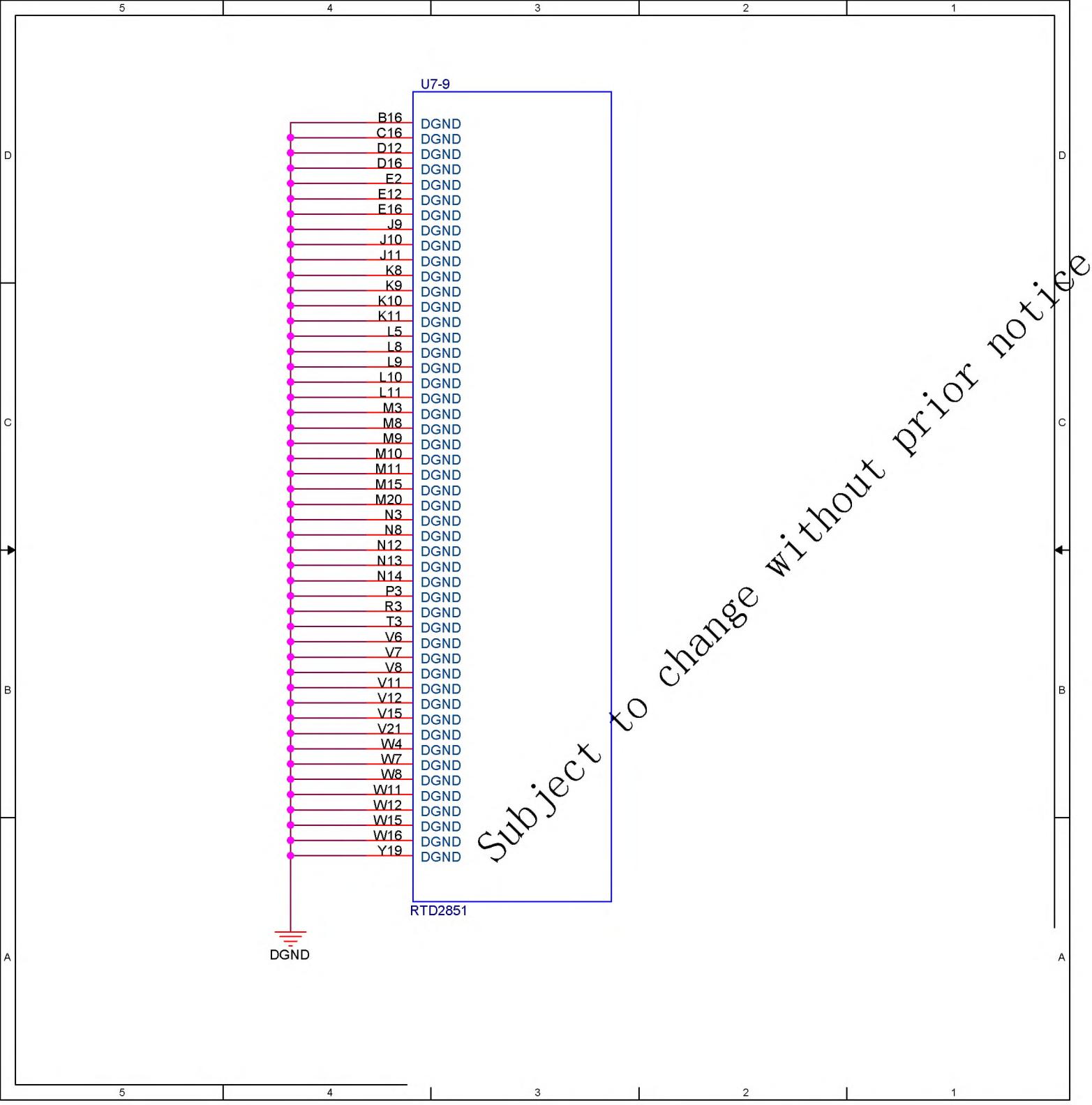


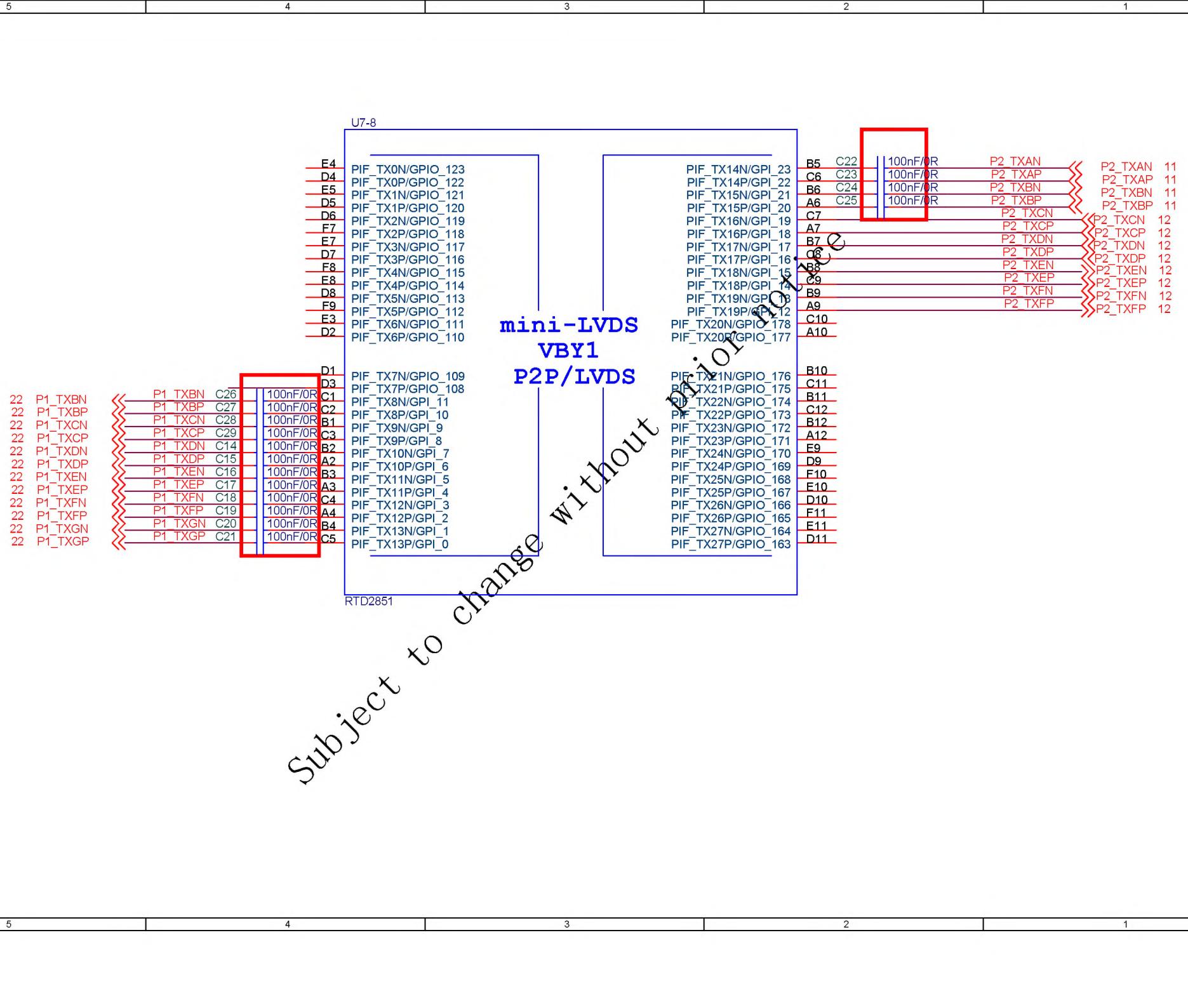
The diagram illustrates the internal connections of the RPN5 NC/0/R module. It shows two sets of P2 port connections:

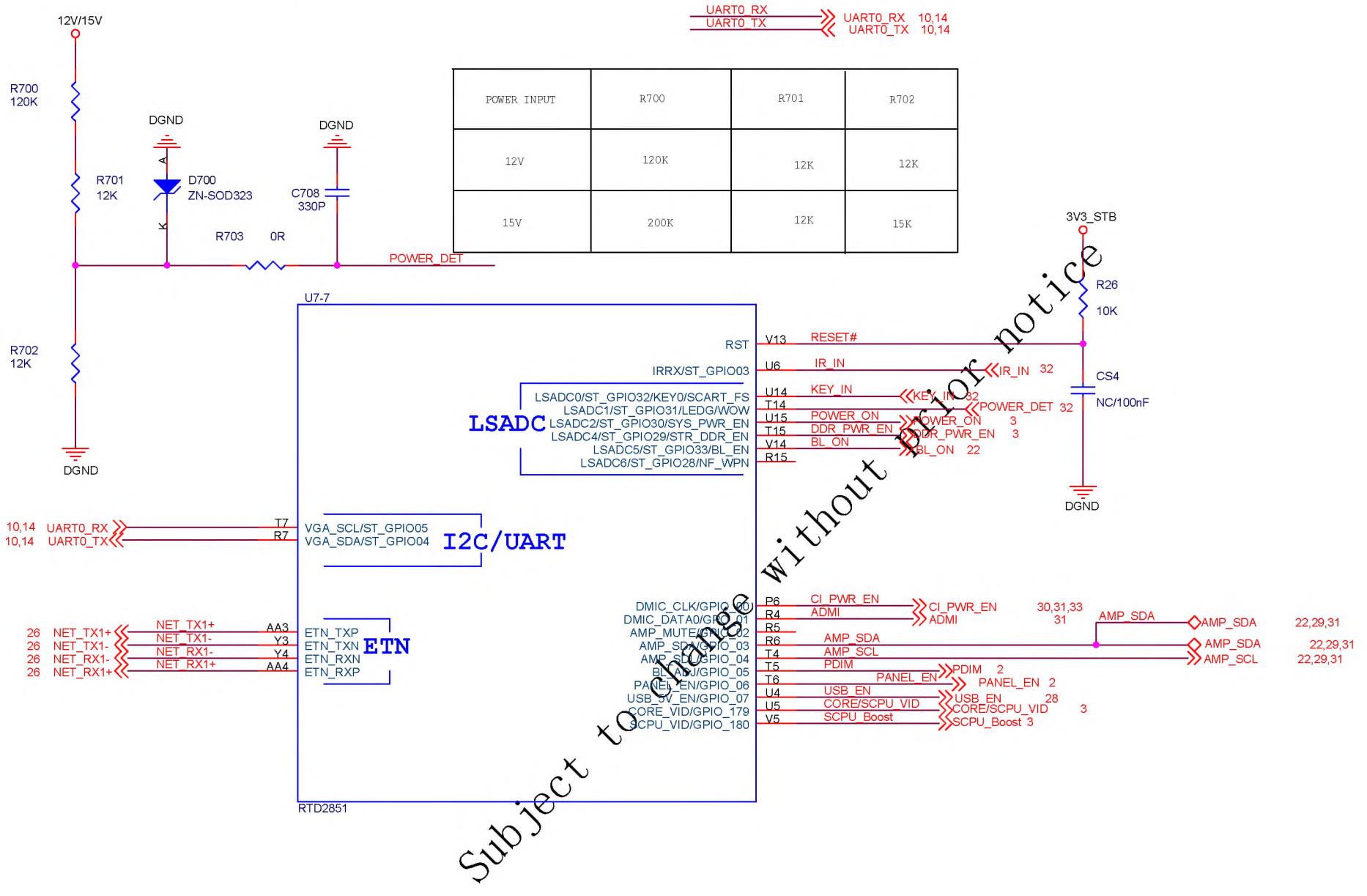
- Top Set:** P2_TXDP, P2_TXDN, P2_TCXP, P2_TXCN, and P2_TXCH are connected to TX17P_R, TX17N_R, TX16P_R, TX16N_R, and TX16R_R respectively.
- Bottom Set:** P2_TXFP, P2_TXFN, P2_TXEP, P2_TXEN, and P2_TXEN are connected to TX19P_R, TX19N_R, TX18P_R, TX18N_R, and TX18R_R respectively.

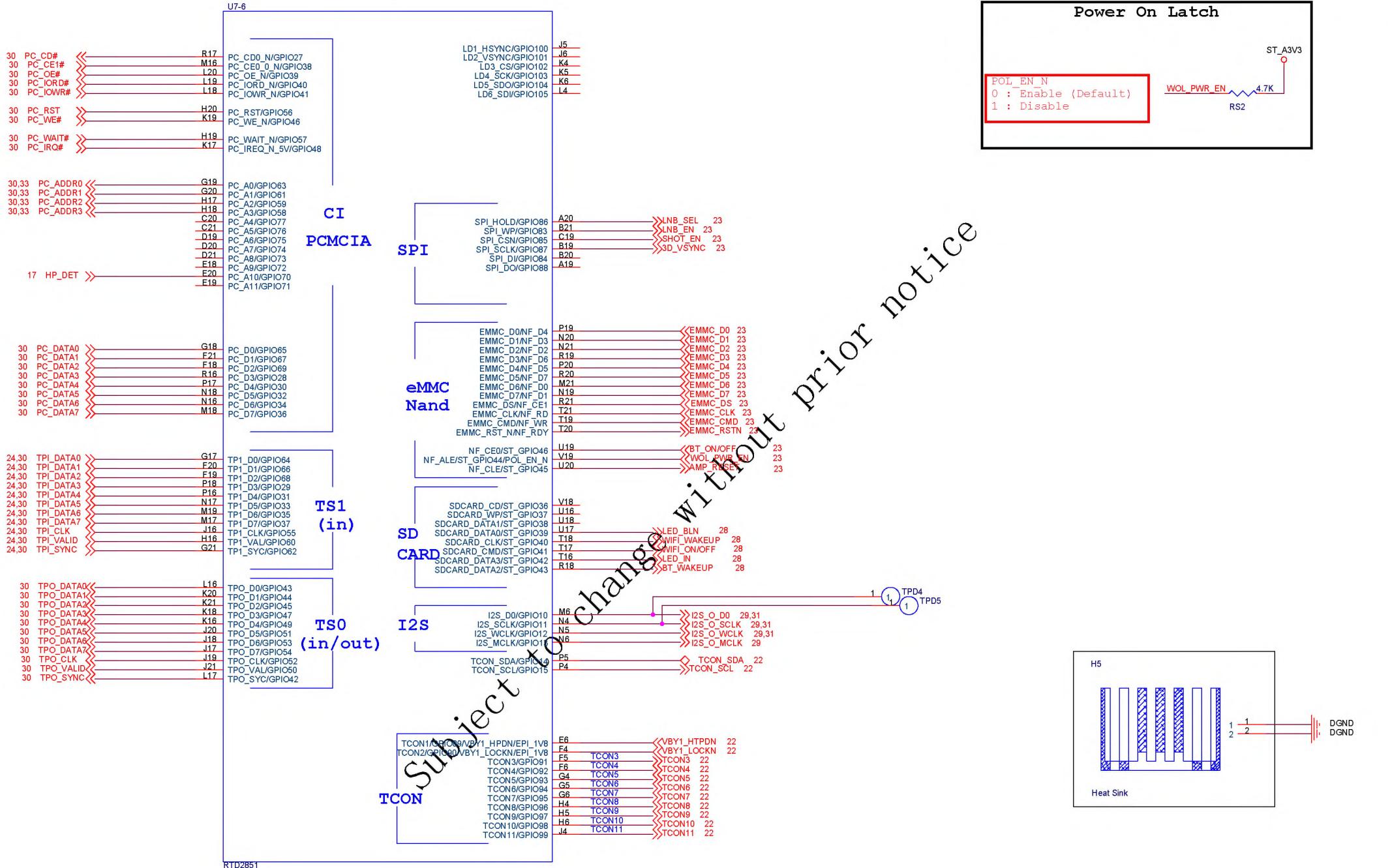
These internal blocks are then connected to external LVDS buffers (BDP, BPN, BCP, BCN) and BPF buffers. The connections are summarized in the following table:

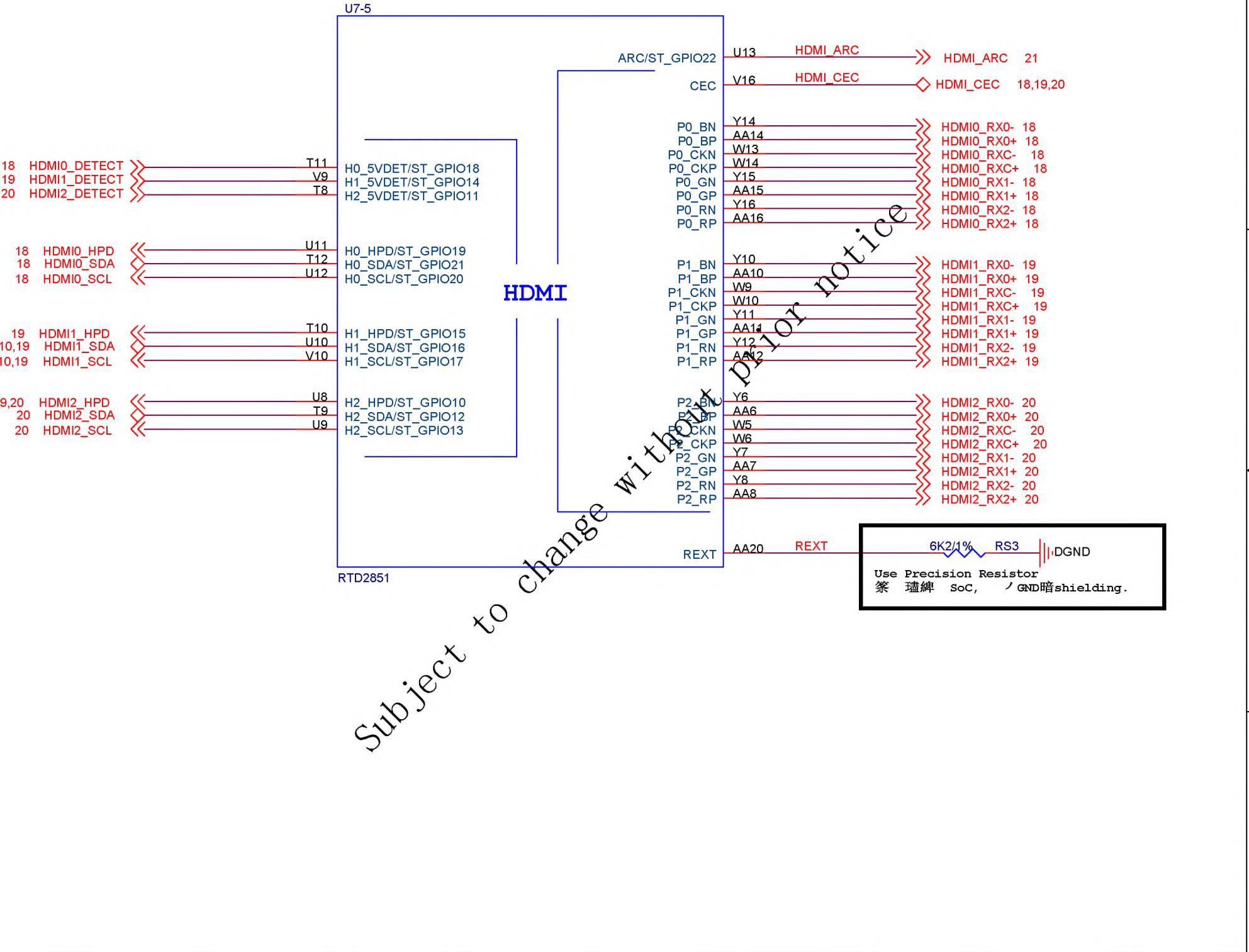
P2 Port	Internal Block	External Buffer
P2_TXDP	TX17P_R	LVDS BDP 2
P2_TXDN	TX17N_R	LVDS BDN 2
P2_TCXP	TX16P_R	LVDS BCP 2
P2_TXCN	TX16N_R	LVDS BCN 2
P2_TXCH	TX16R_R	
P2_TXFP	TX19P_R	LVDS BFP 2
P2_TXFN	TX19N_R	LVDS BPN 2
P2_TXEP	TX18P_R	LVDS BCP 2
P2_TXEN	TX18N_R	LVDS BCN 2
P2_TXEN	TX18R_R	LVDS BEN 2

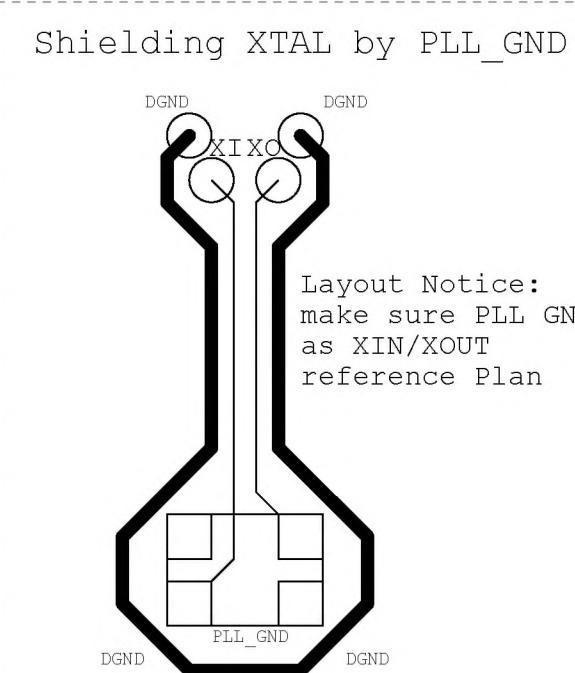
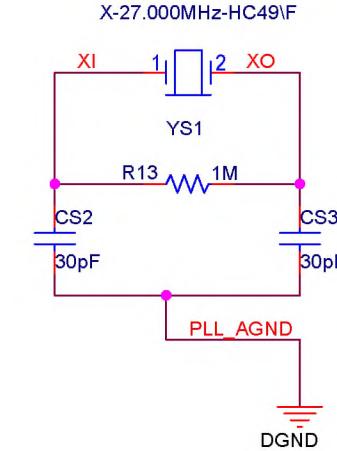
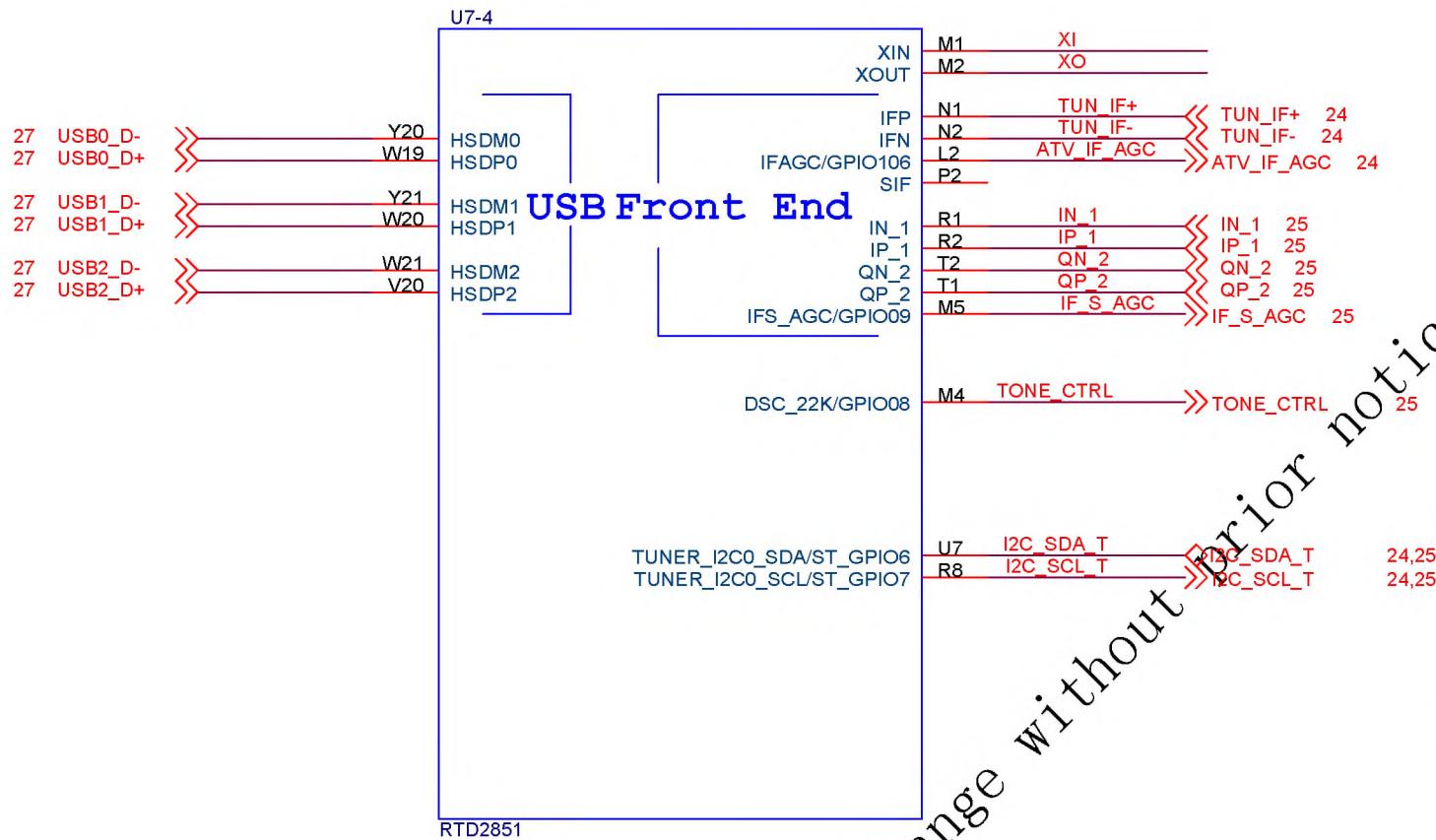


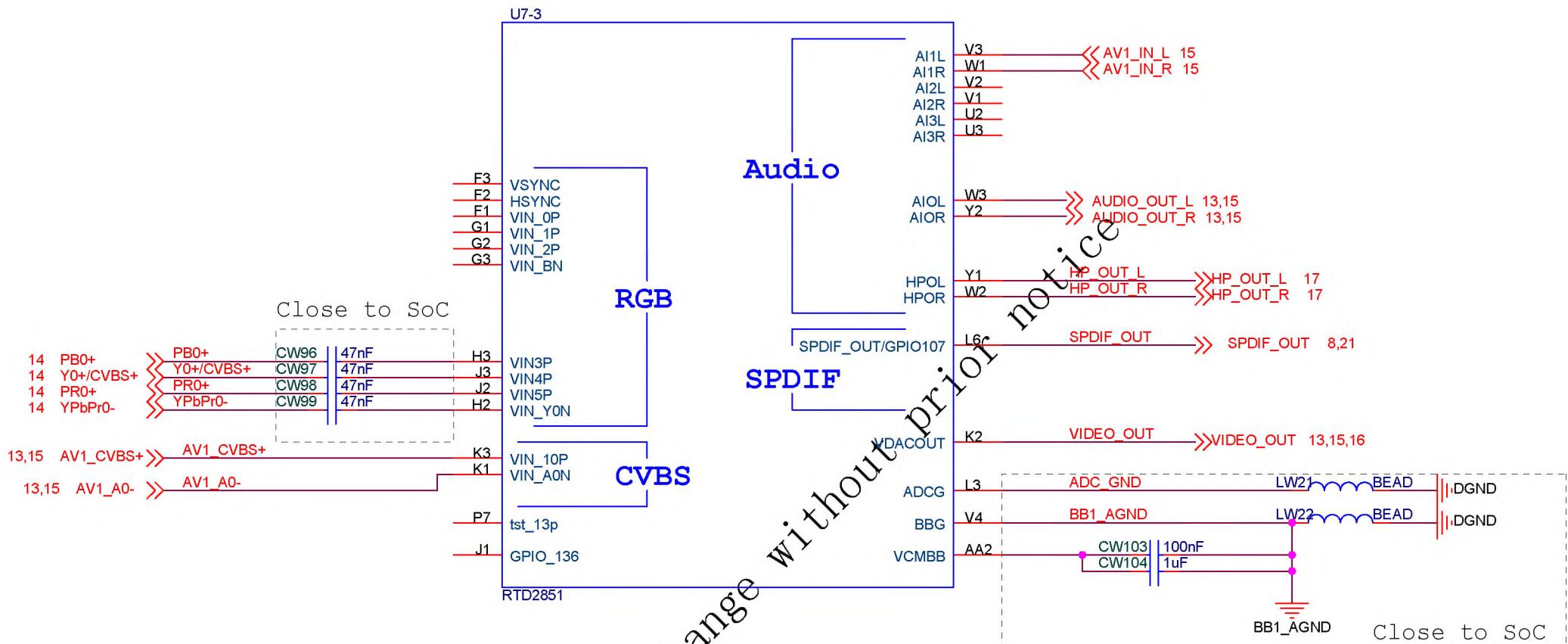












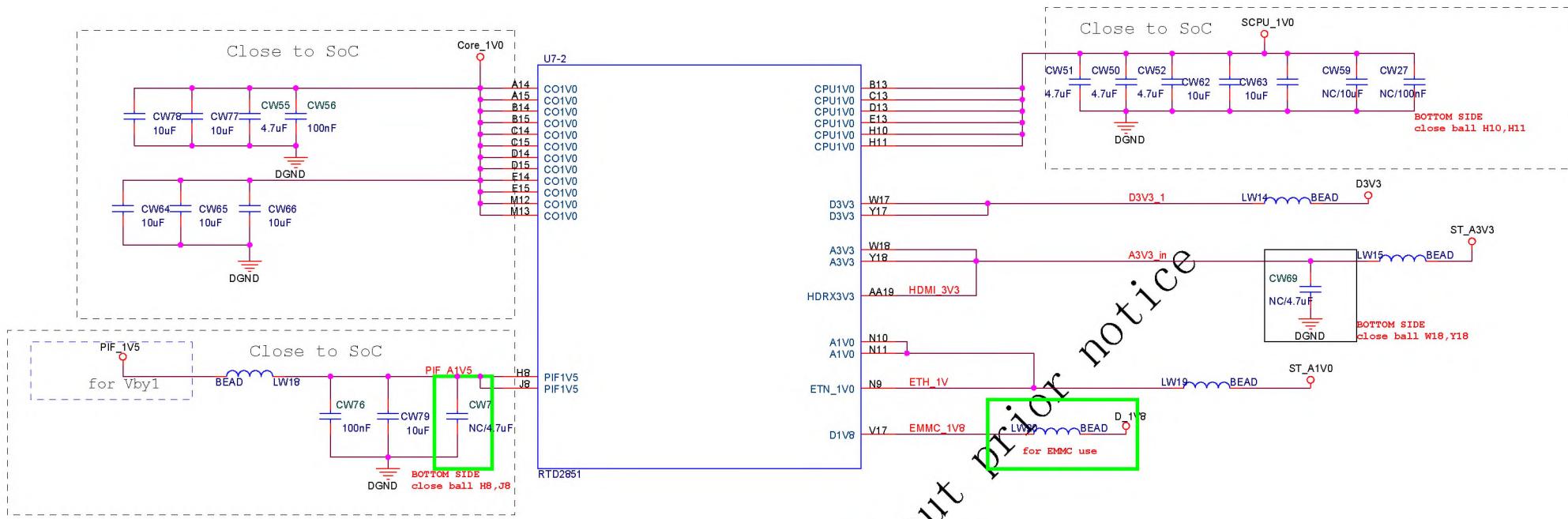
Subject to change without prior notice

Close to SoC

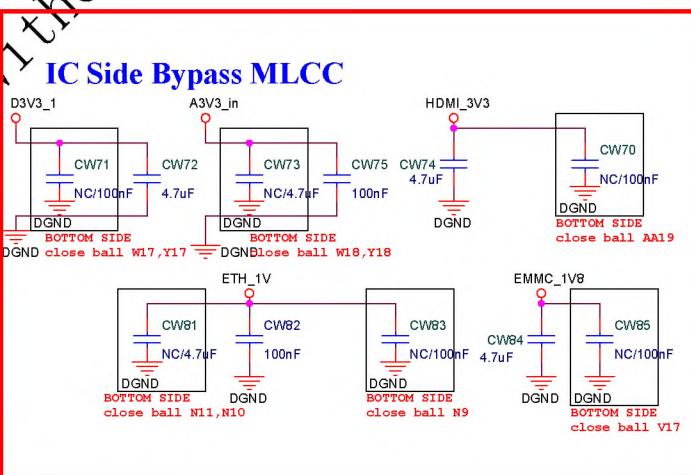
SPDIF

Audio

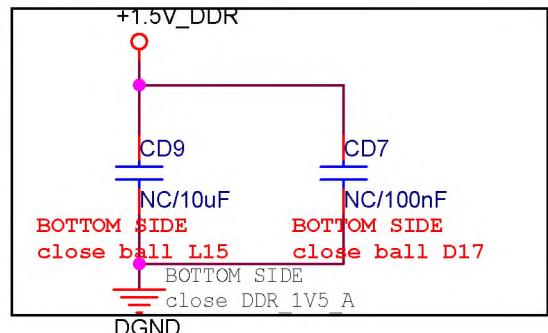
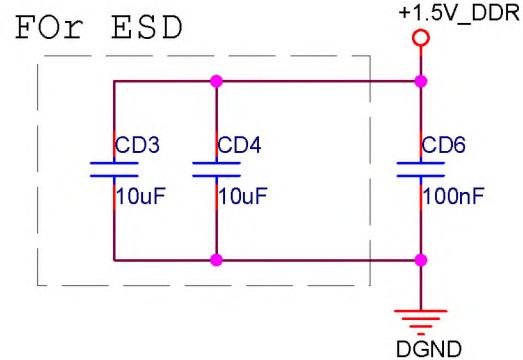
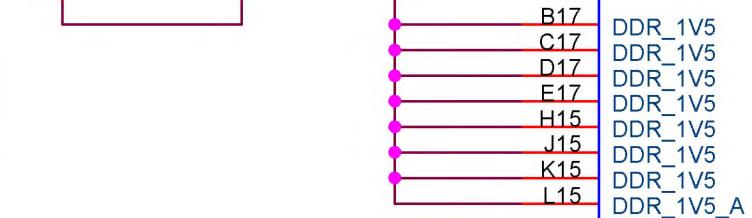
Close to SoC



Subject to change without prior notice

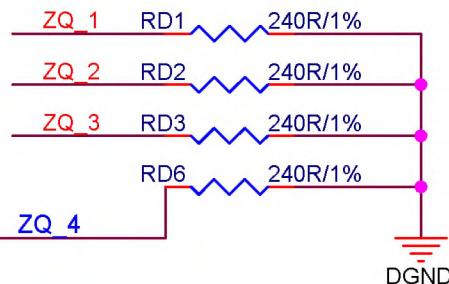


DRAM Controller

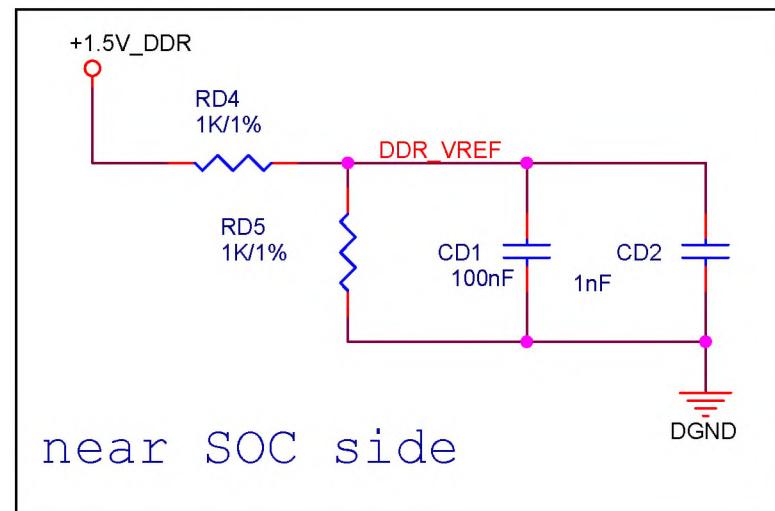


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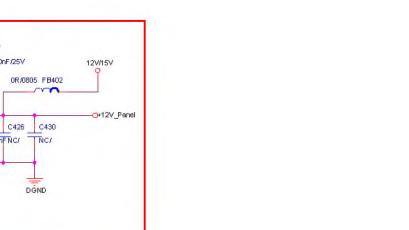
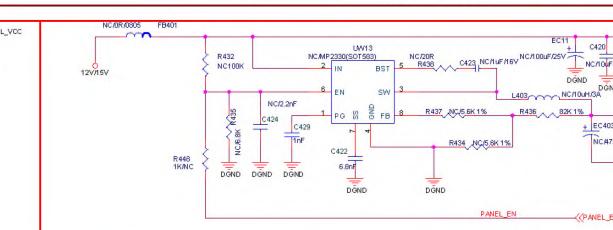
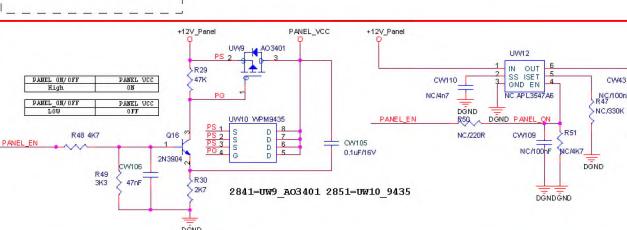
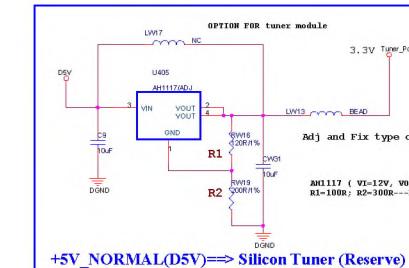
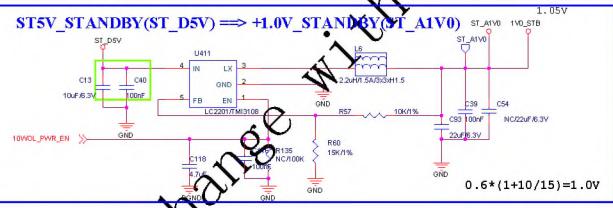
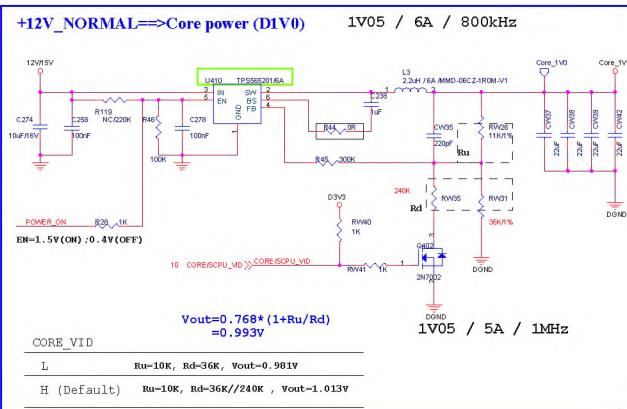
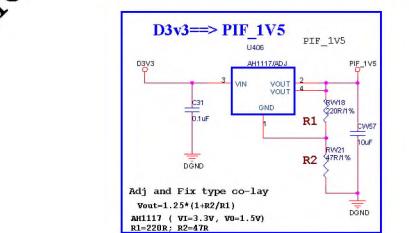
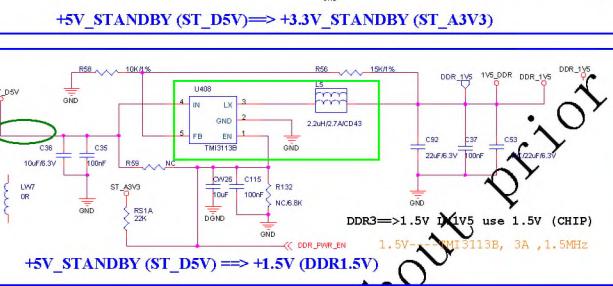
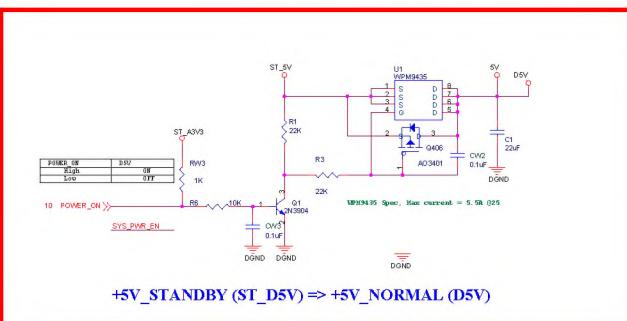
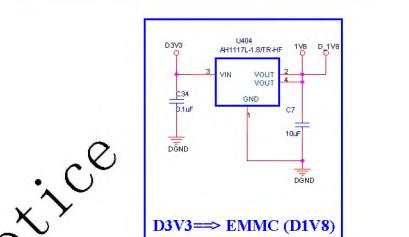
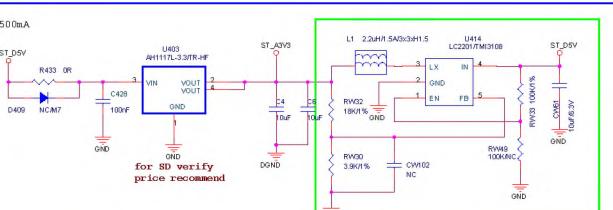
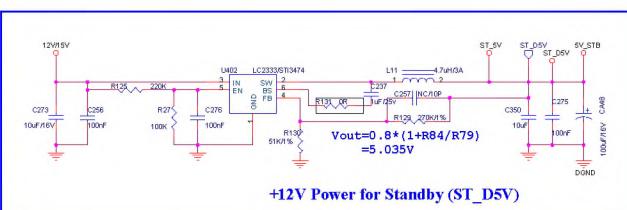
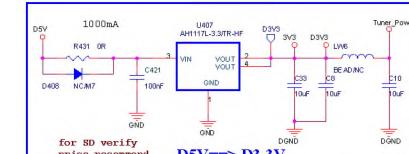
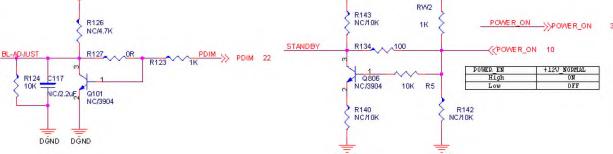
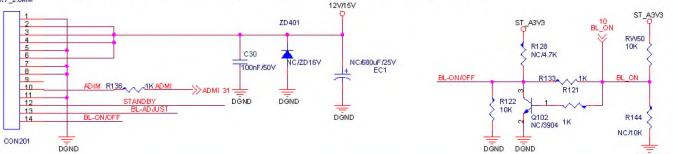
Vref
ZQ1
ZQ2
ZQ3
ZQ4
A18 DDR_VREF
B18 ZQ_1
C18 ZQ_2
D18 ZQ_3
G16
ZQ_4

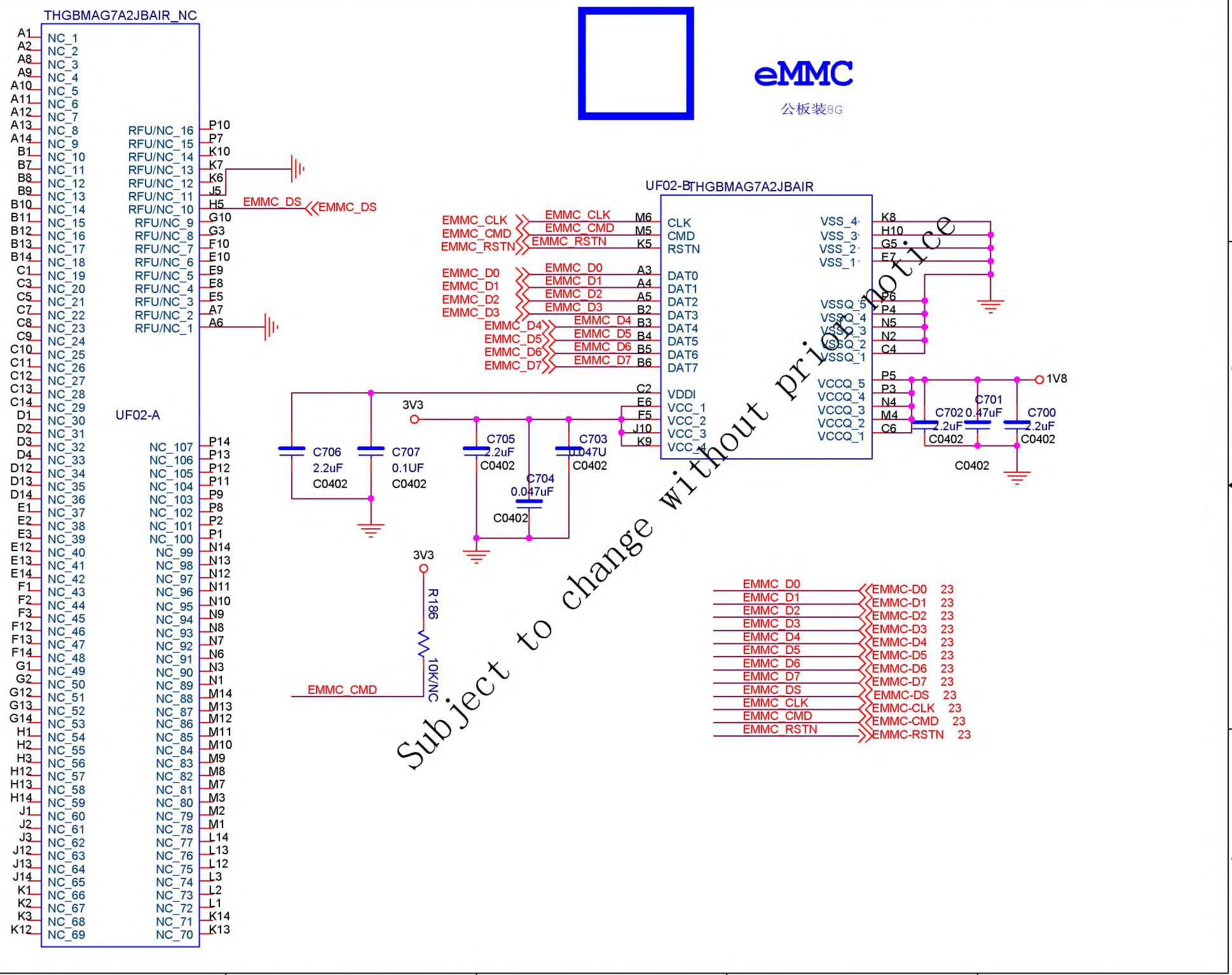


DDR Size Option
2.0GB: RD1, RD2, RD3, RD6 mount
1.5GB/1GB: RD1, RD2, RD3 mount

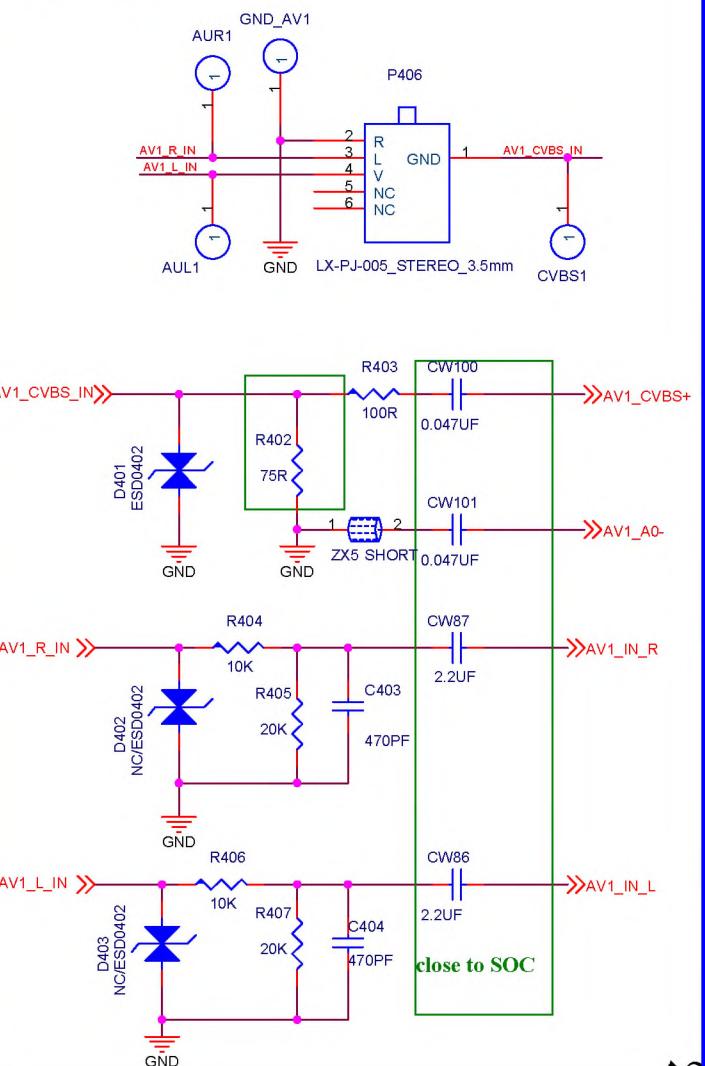


Power socket and Signal switching control

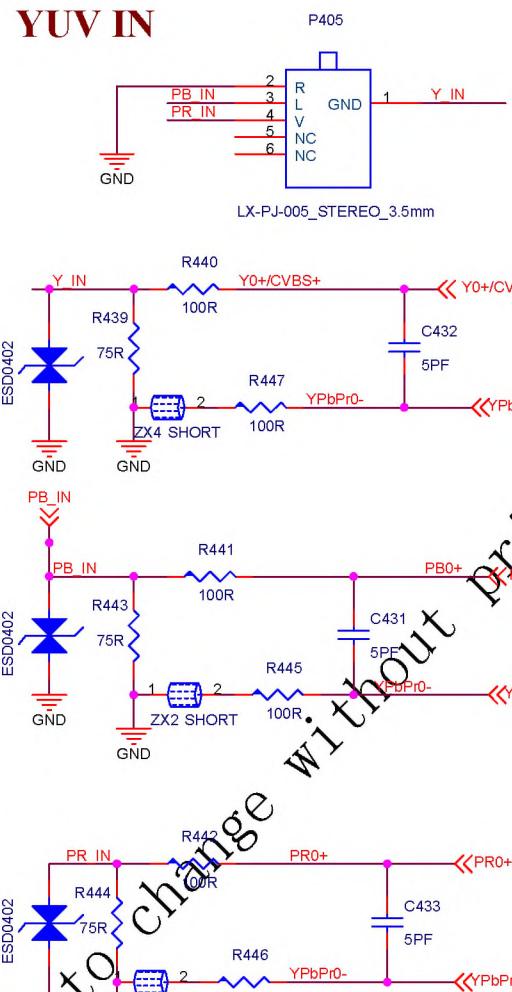




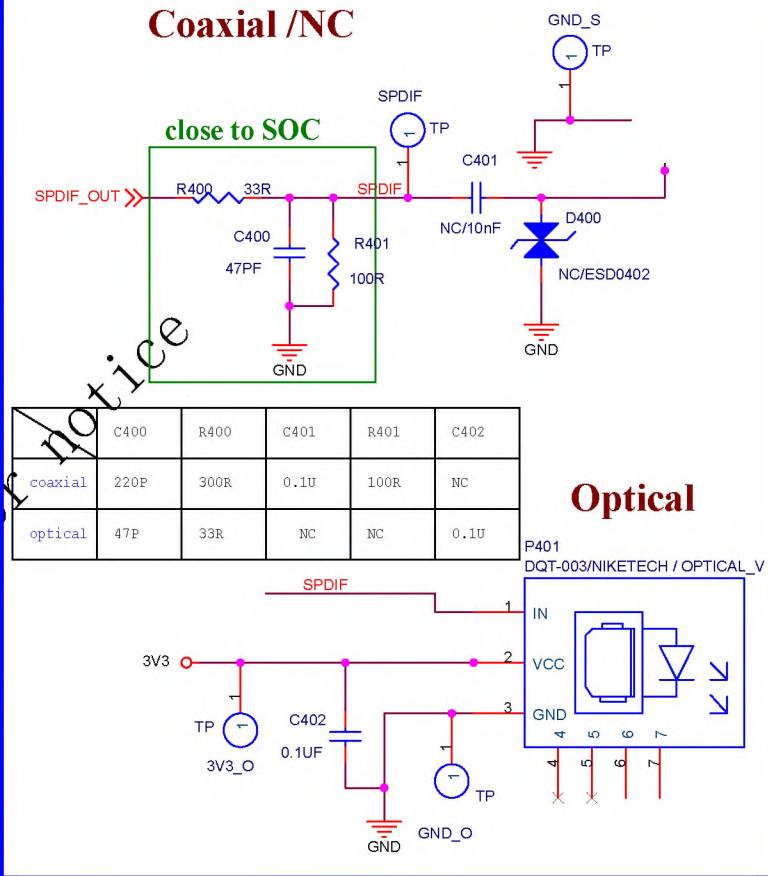
AV IN



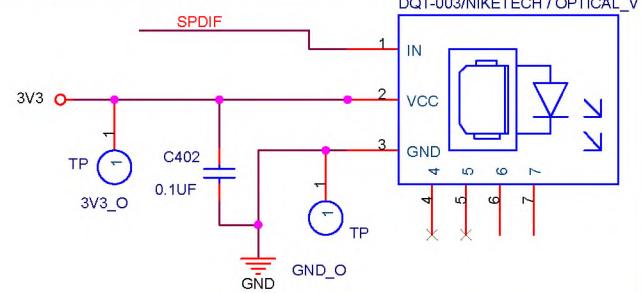
YUV IN

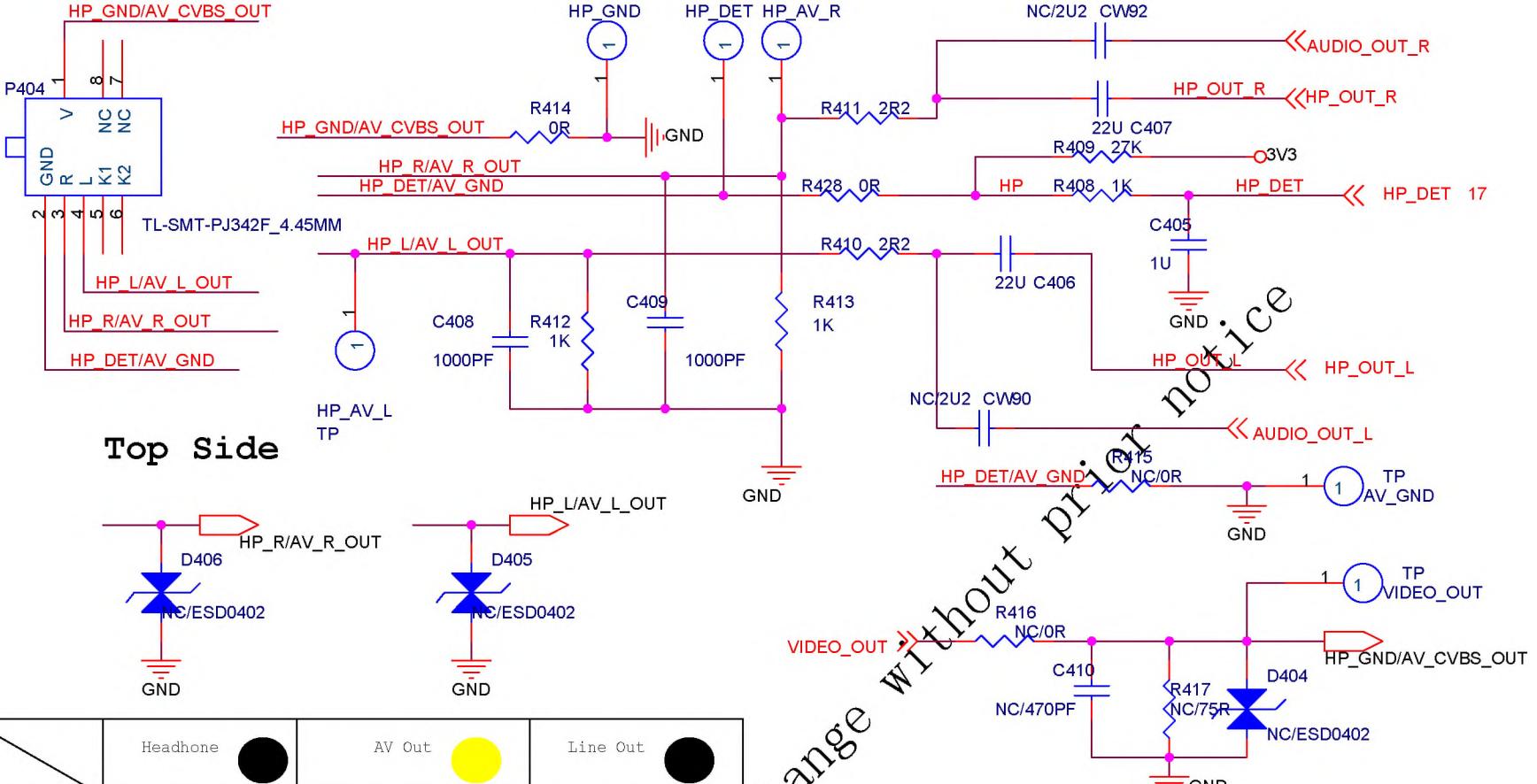


Coaxial / NC

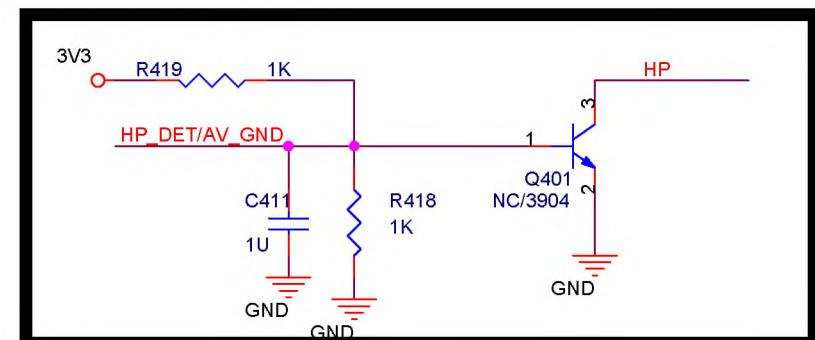


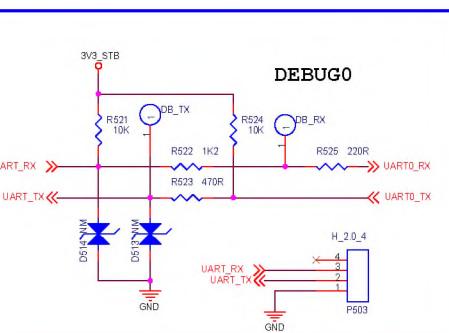
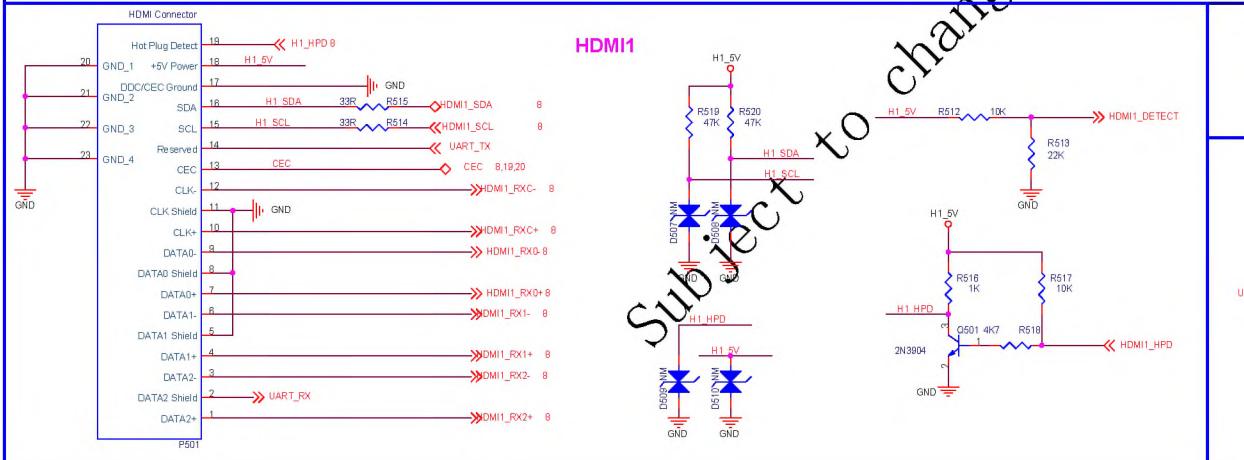
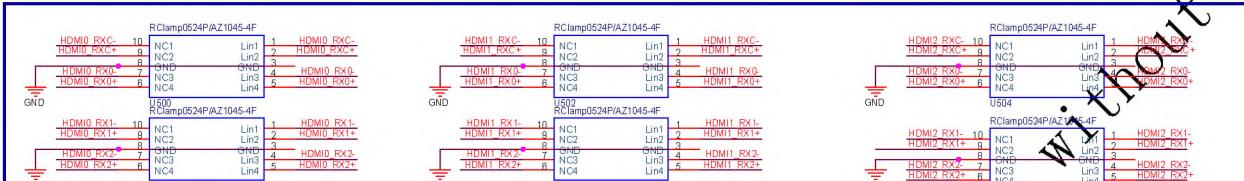
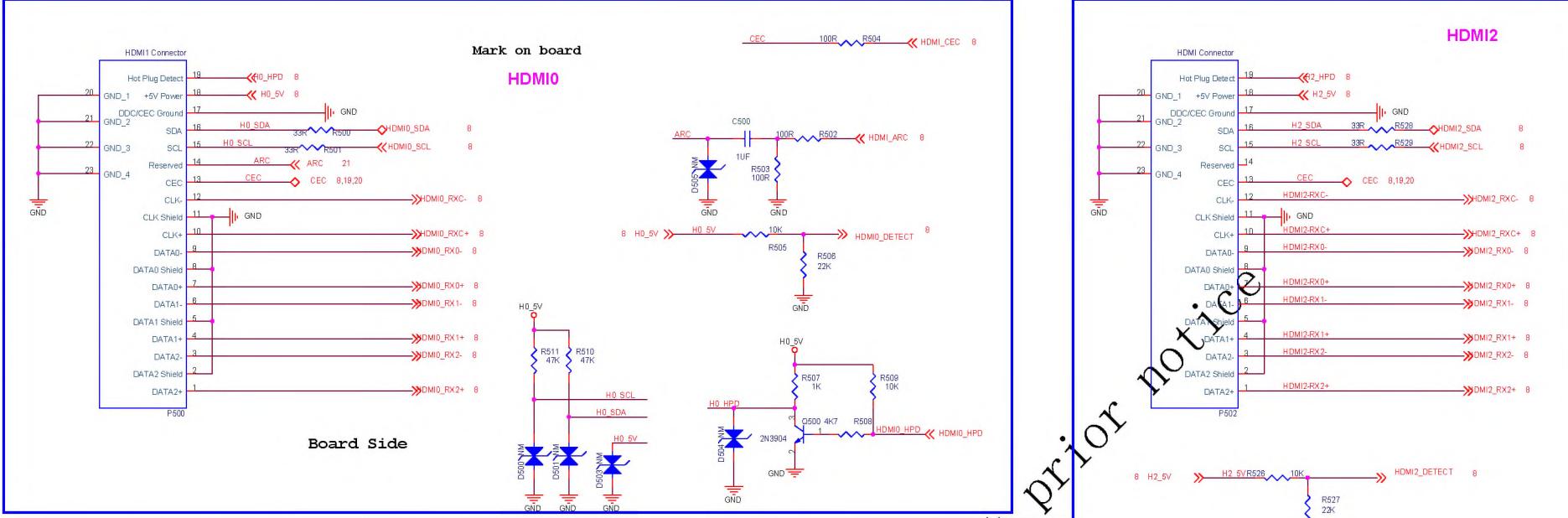
Optical



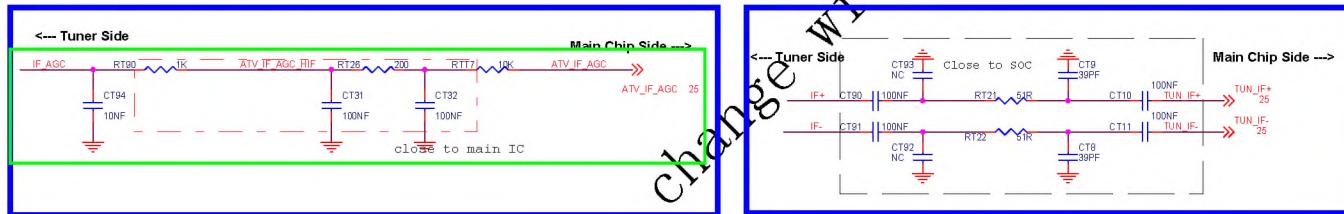
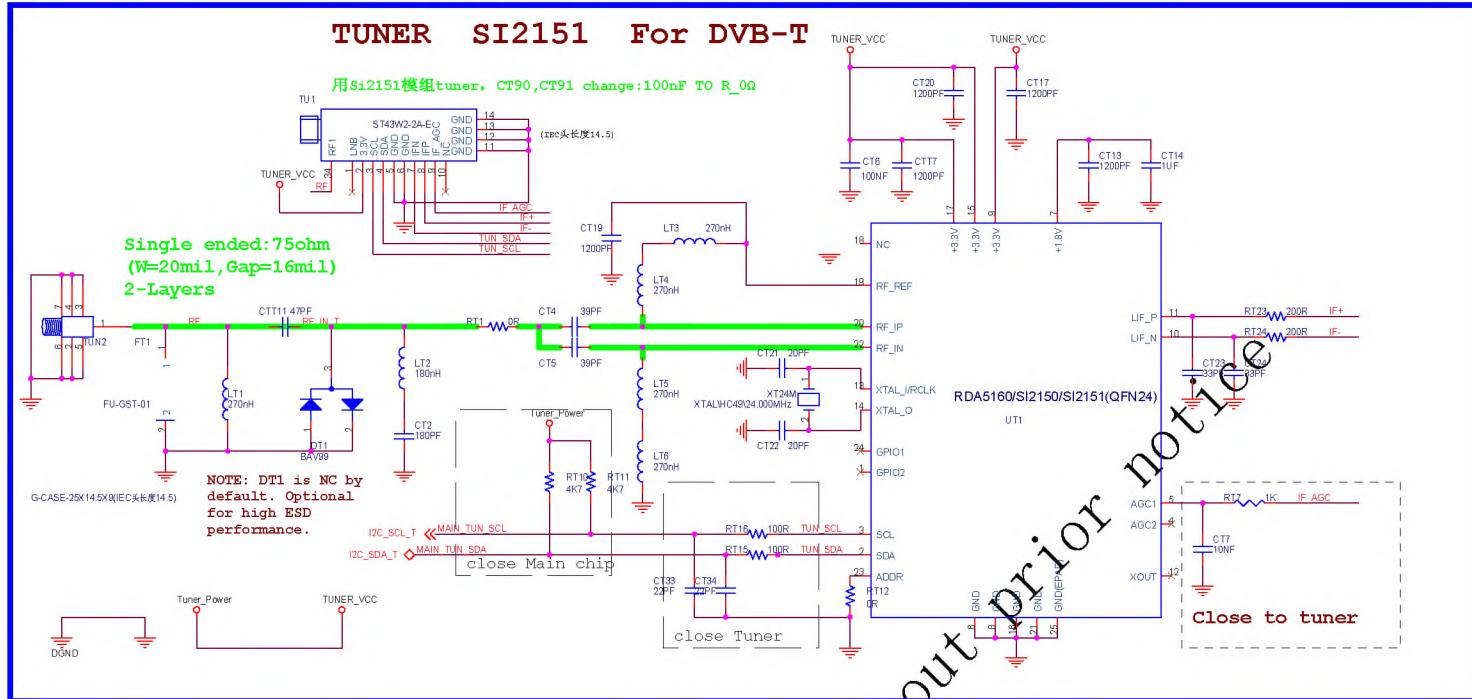


	Headphone	AV Out	Line Out
P1	HP_GND	VIDEO_OUT	NC
P2	HP_DET	AV_GND	AV_GND
P3	HP_R	AV_R_OUT	LINE_OUT_R
P4	HP_L	AV_L_OUT	LINE_OUT_L
R414	0R	NC	NC
R415	NC	0R	0R
R428	0R	NC	NC
R412, R413	1K	10K	10K
C408, C409			





TUNER SI2151 For DVB-T



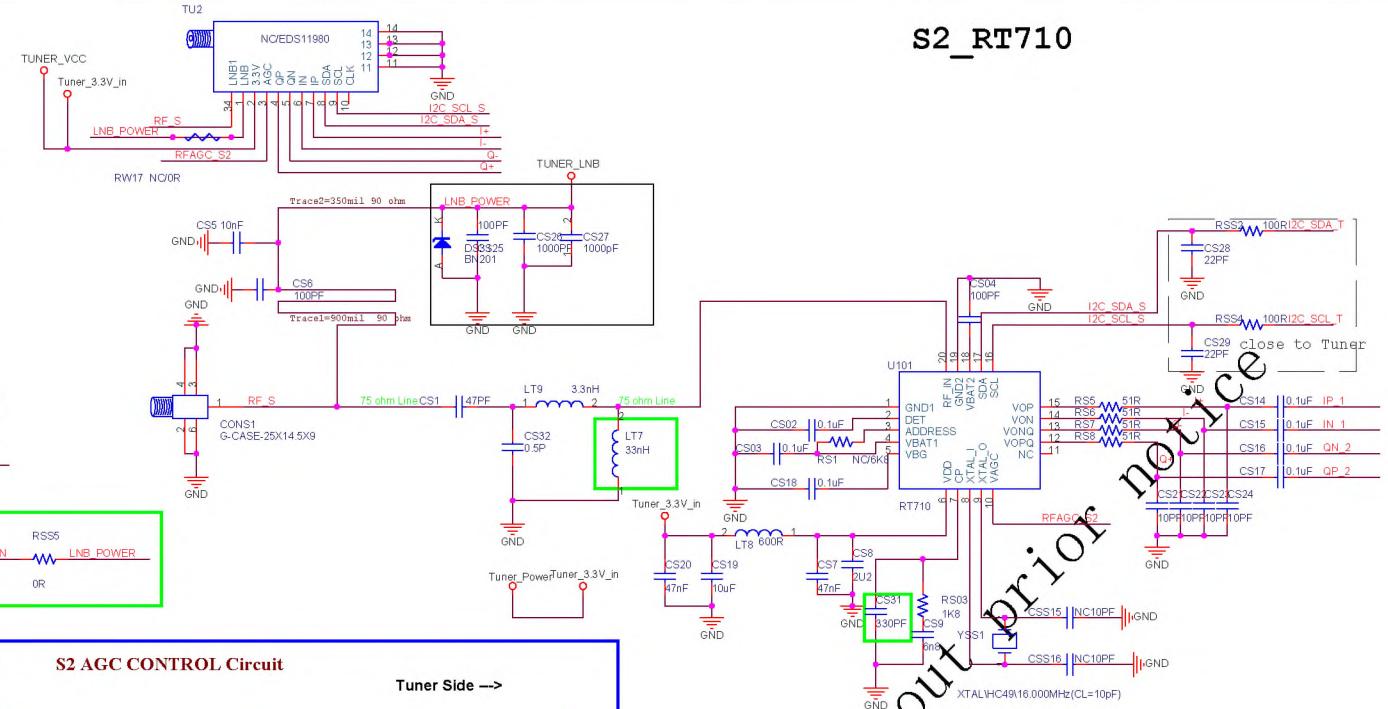
Subject to
change

S2_RT710

Main Chip <--

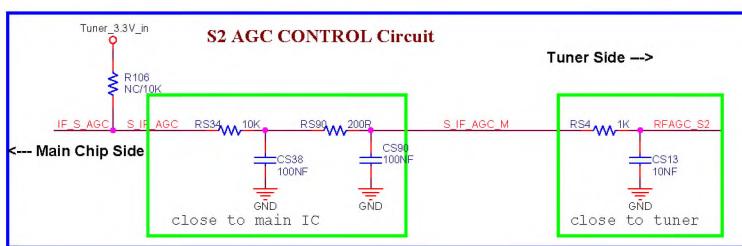
- 24,25 IF_AGC >> IF_AGC
- 7,24 I2C_SCL_T >> I2C_SDA_T
- 7,24 I2C_SDA_T >> I2C_SCL_T
- 7 QP_2
- 7 QN_2
- 7 IP_1
- 7 IN_1
- 7 IF_S_AGC >> IF_S_AGC
- 24,25 IF+ >> IF+
- 24,25 IF- >> IF-

- 7 LNB_EN << LNB_EN
- 7 LNB_SEL << LNB_SEL
- 7 TONE_CTRL << TONE_CTRL
- 9 SHOT_EN >> SHOT_EN



S2 AGC CONTROL Circuit

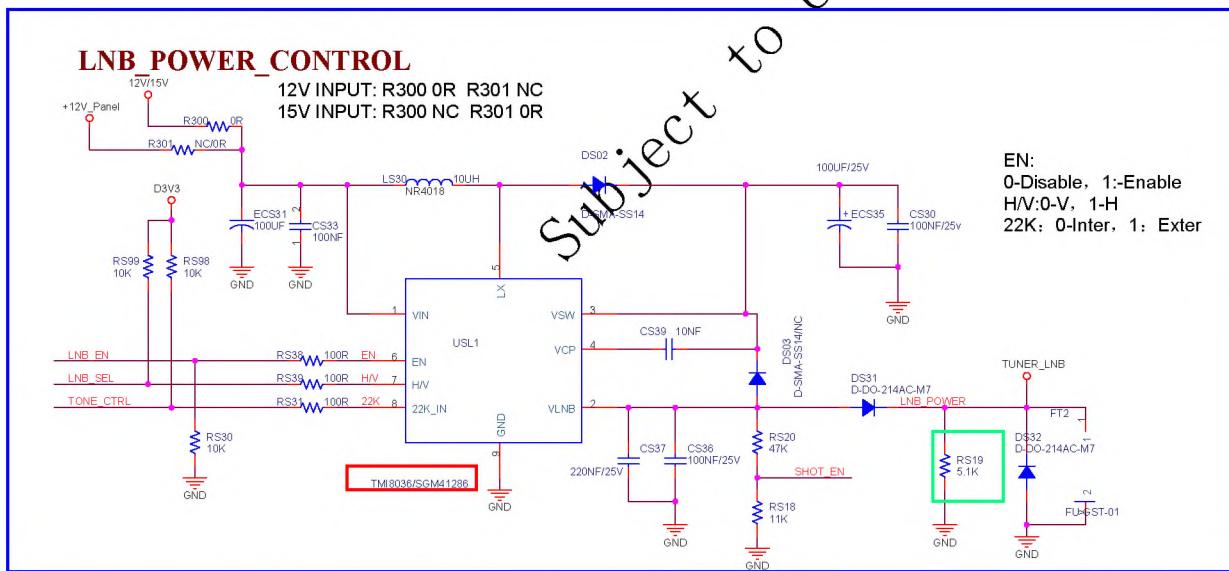
Tuner Side -->

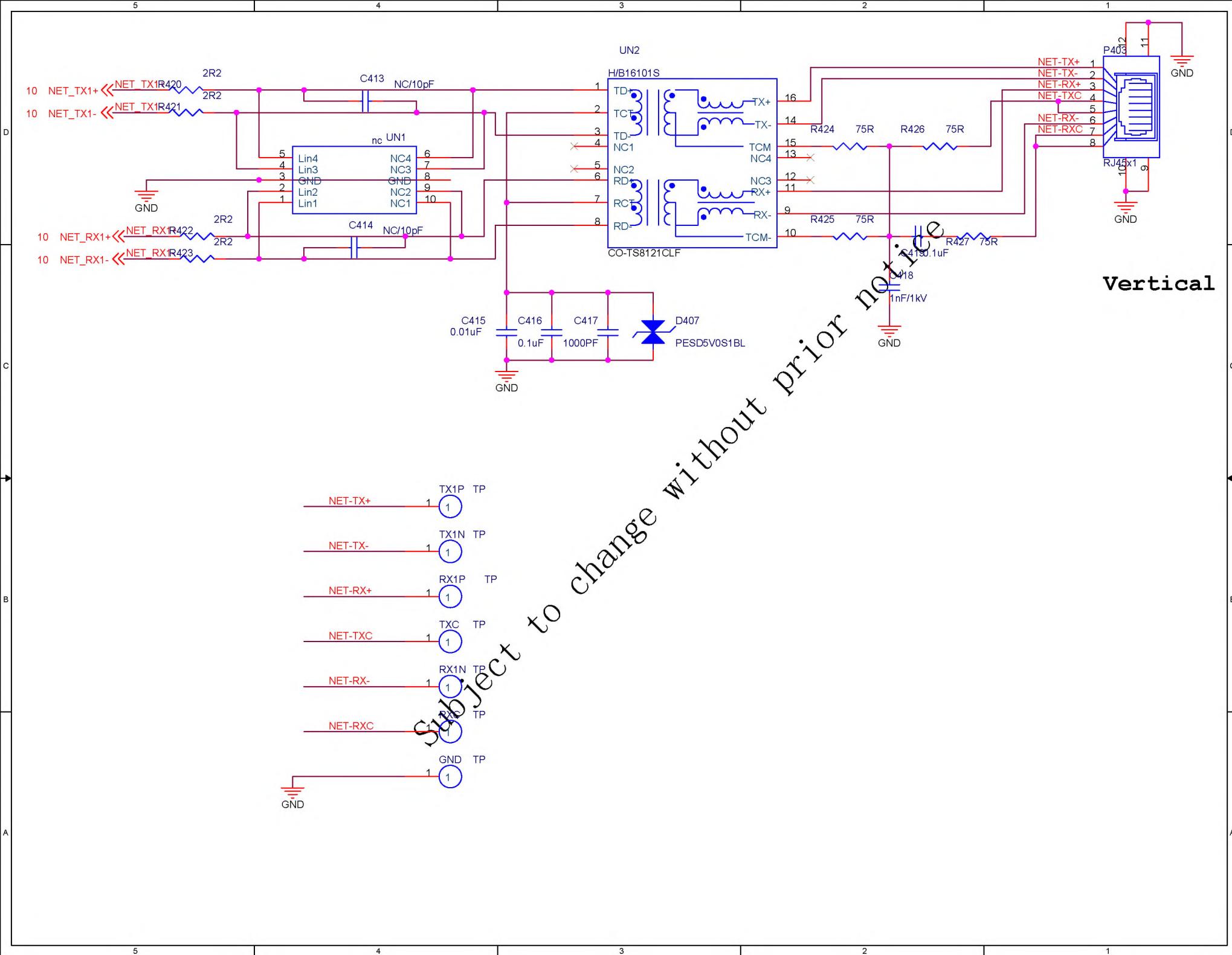


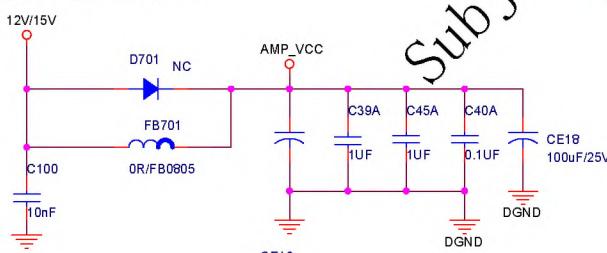
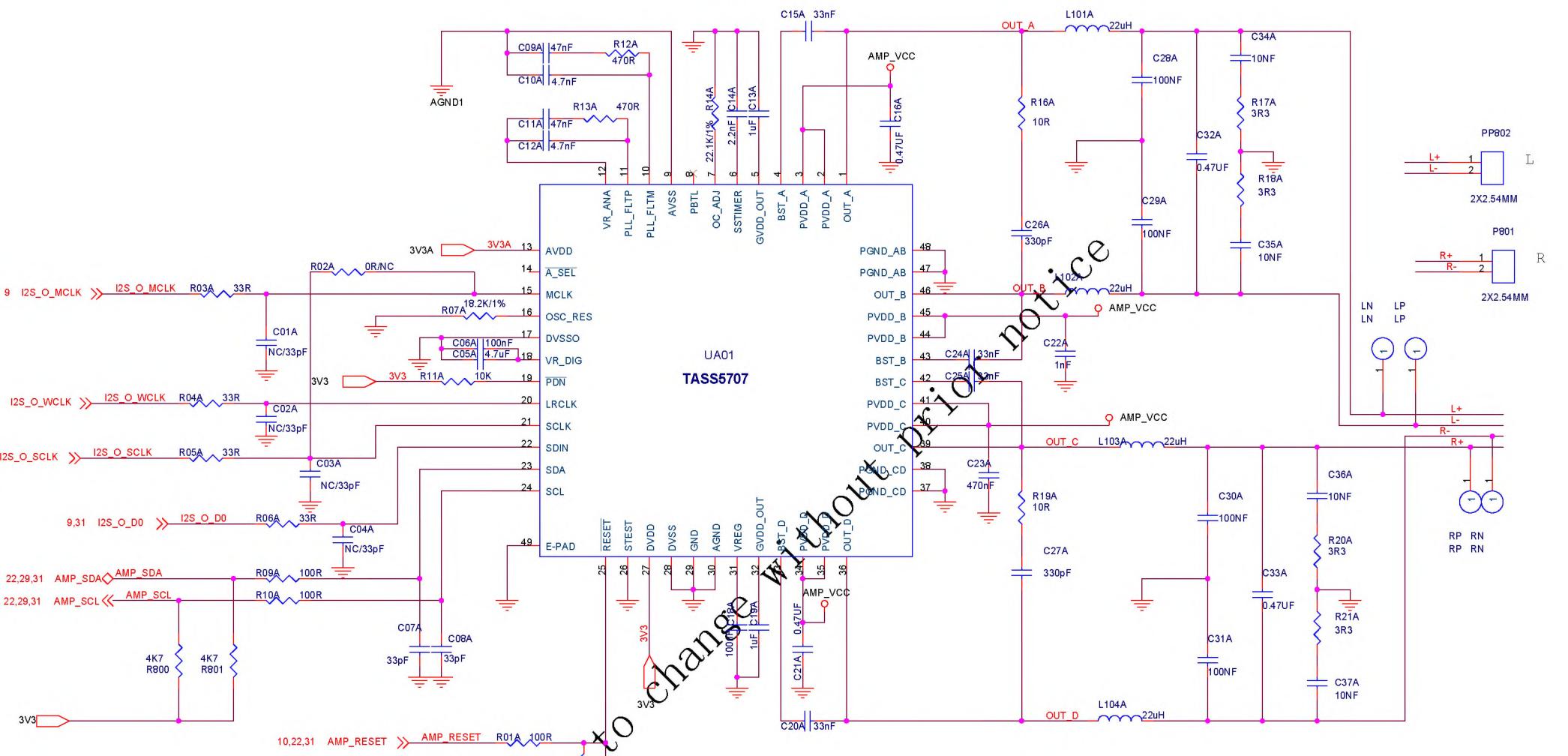
LNB POWER_CONTROL

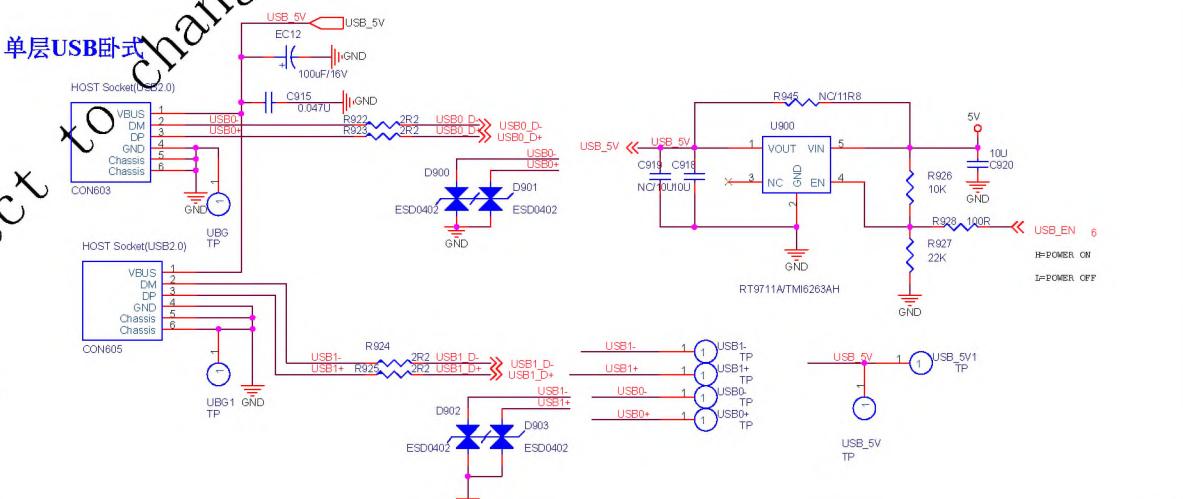
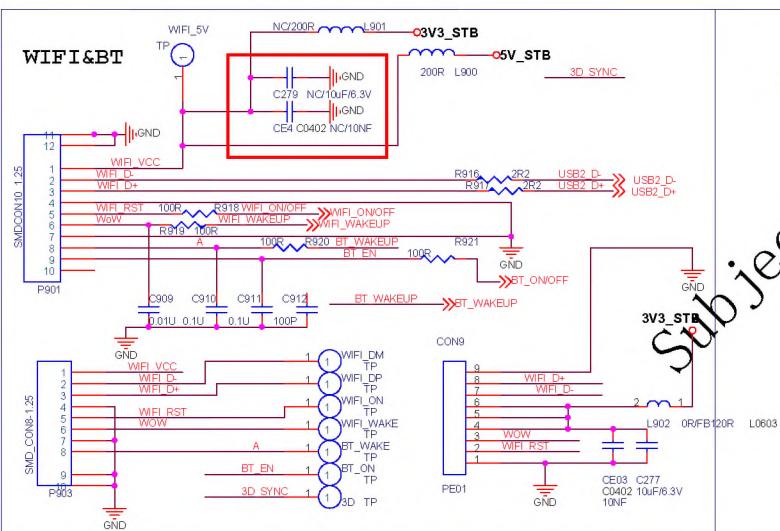
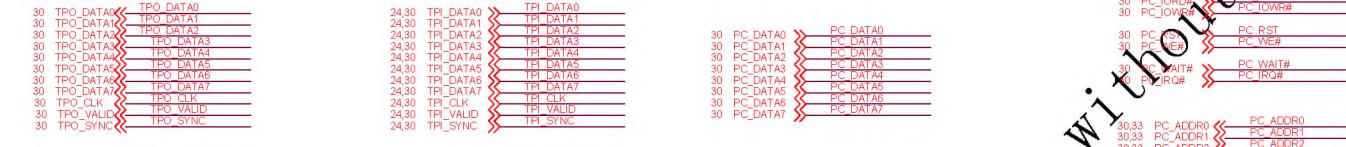
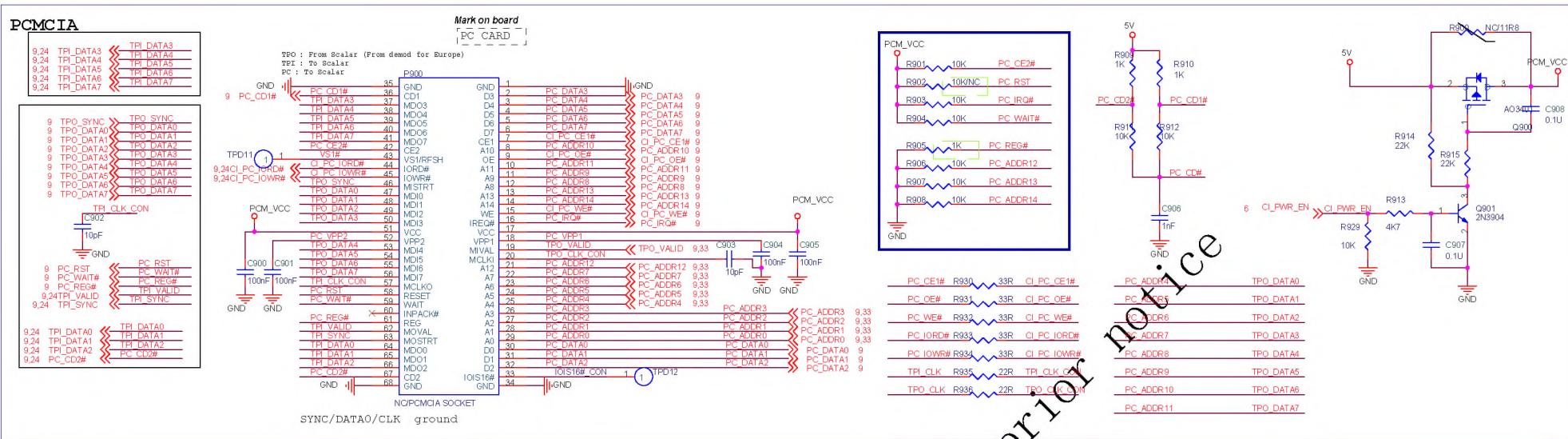
12V INPUT: R300 0R R301 NC
15V INPUT: R300 NC R301 0R

EN:
0-Disable, 1-Enable
H/V:0-V, 1-H
22K: 0-Inter, 1: Exter

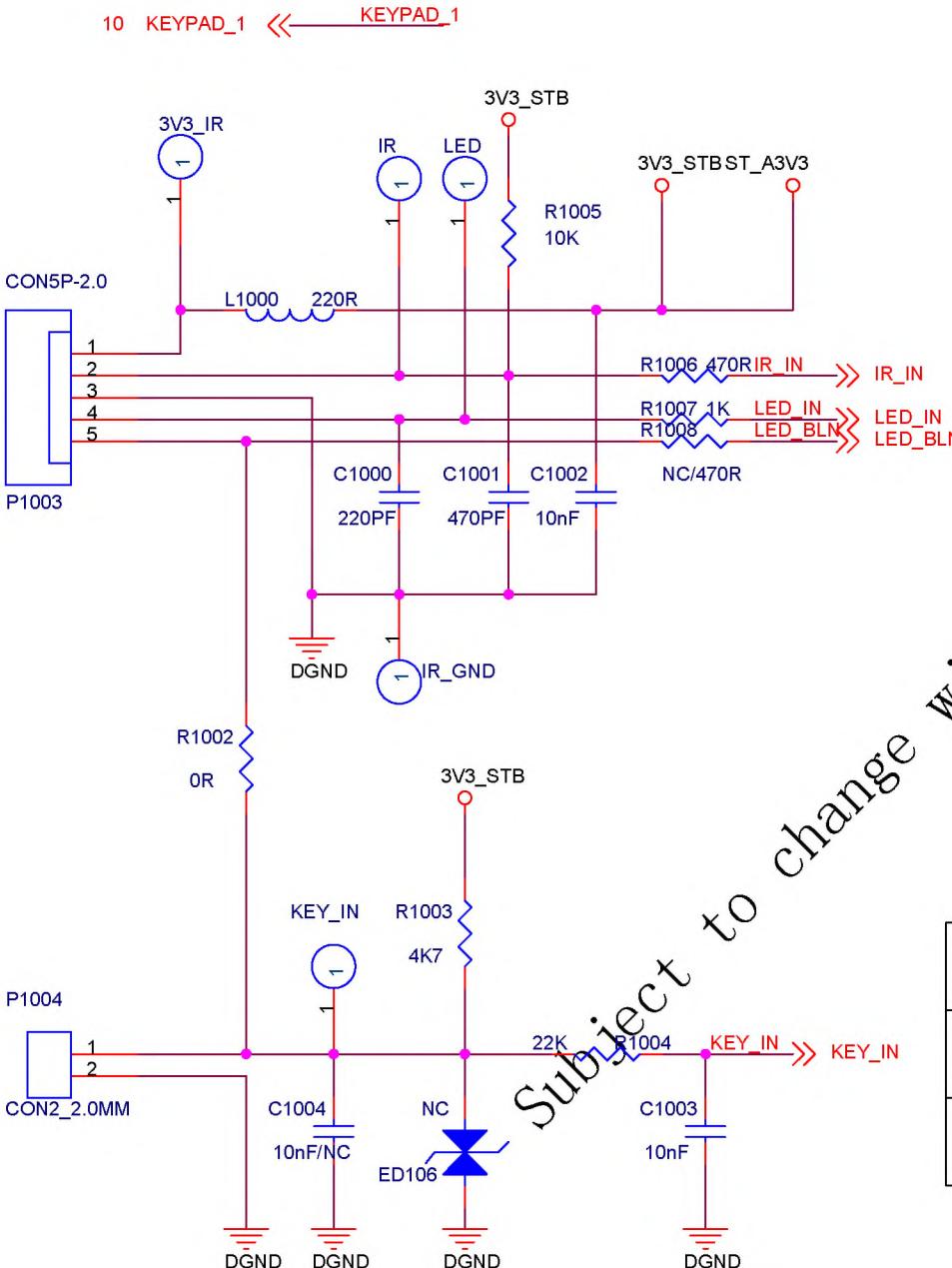








From Main Chip



Subject to change without prior notice

Note:	P1003	P1004	R1002	R1008	LED_BLN
Key&IR 2IN1	ON	NC	ON	NC	N.A
Separate	ON	ON	NC	NC	N.A
	ON	ON	NC	ON	Separate