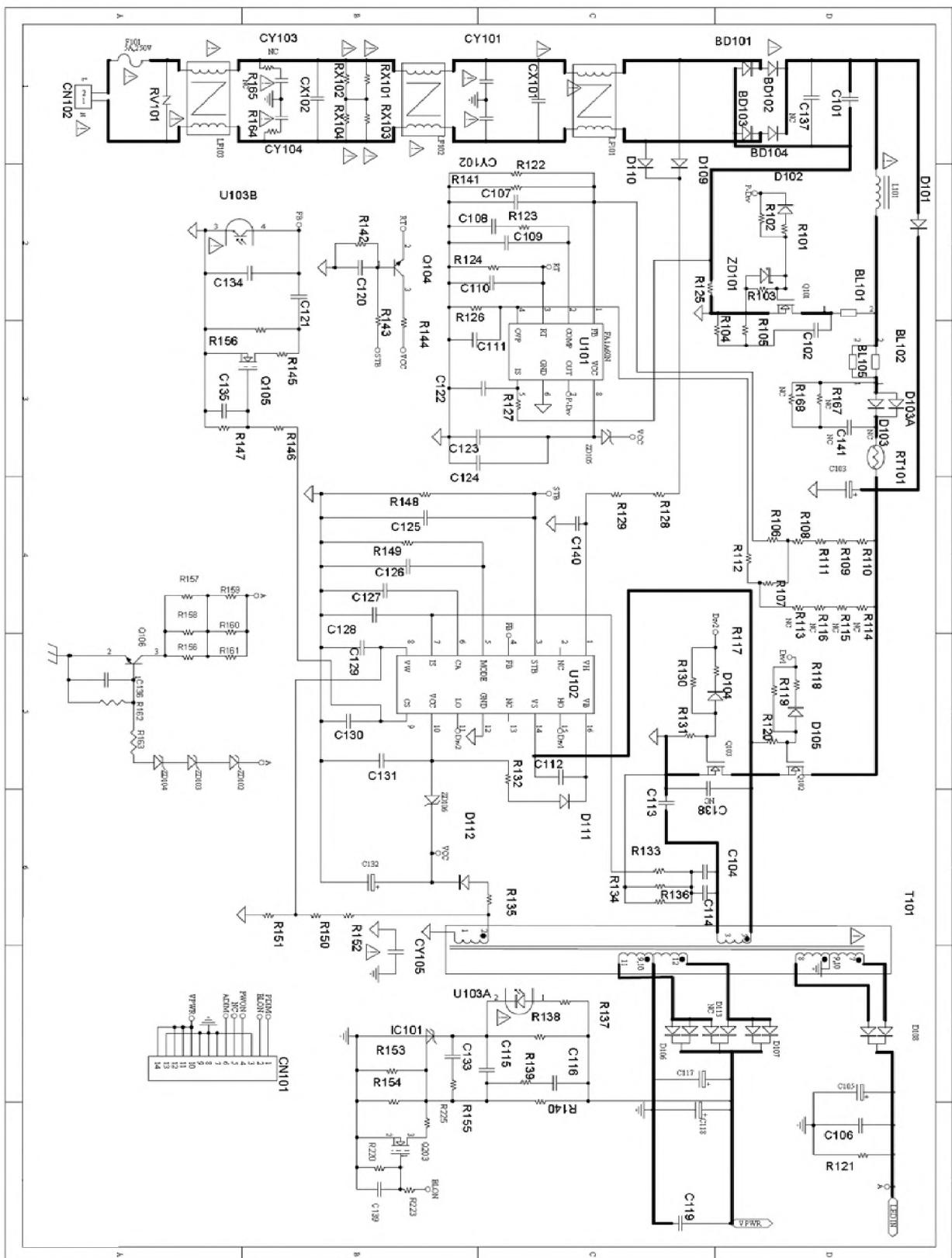
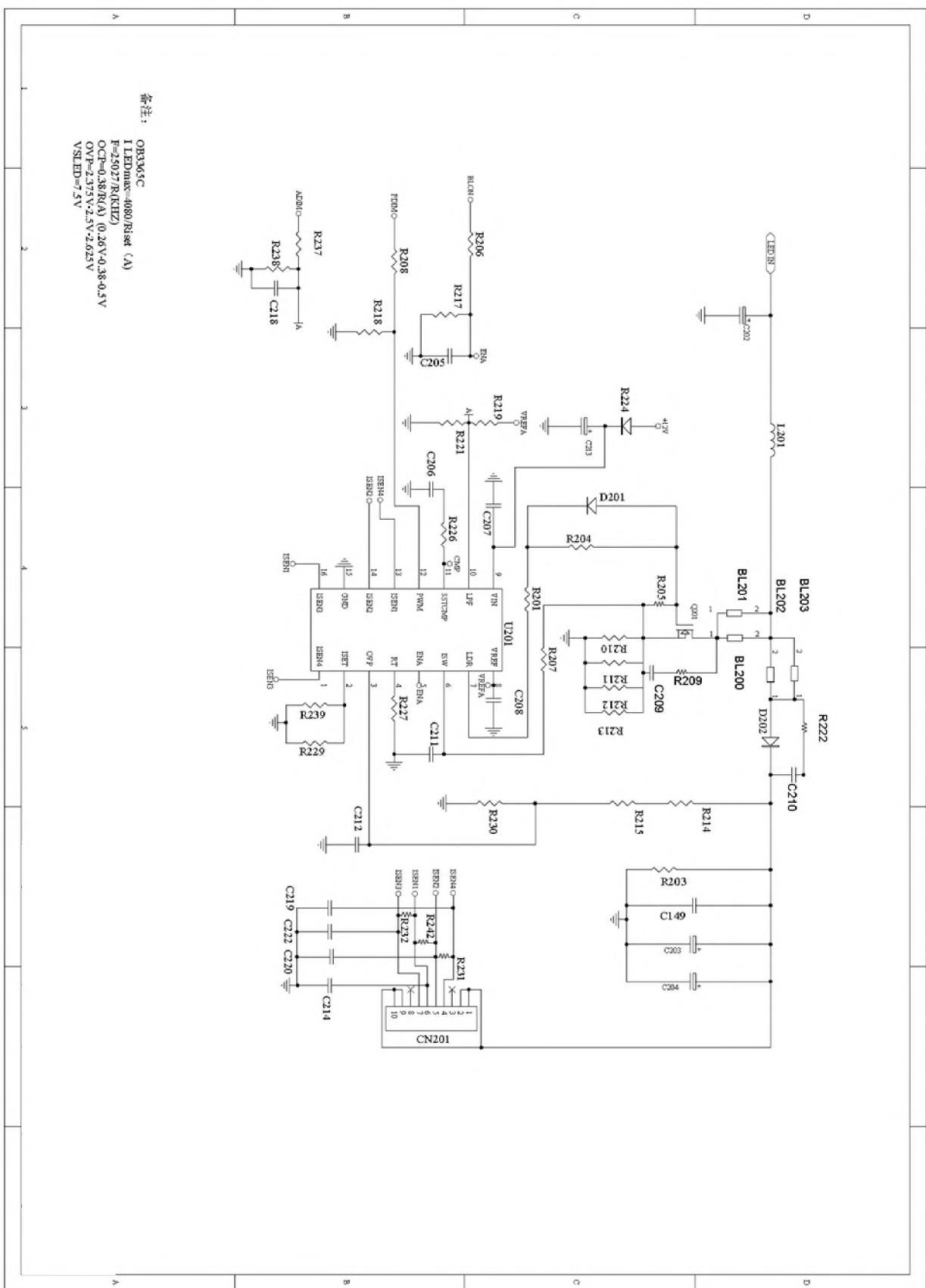


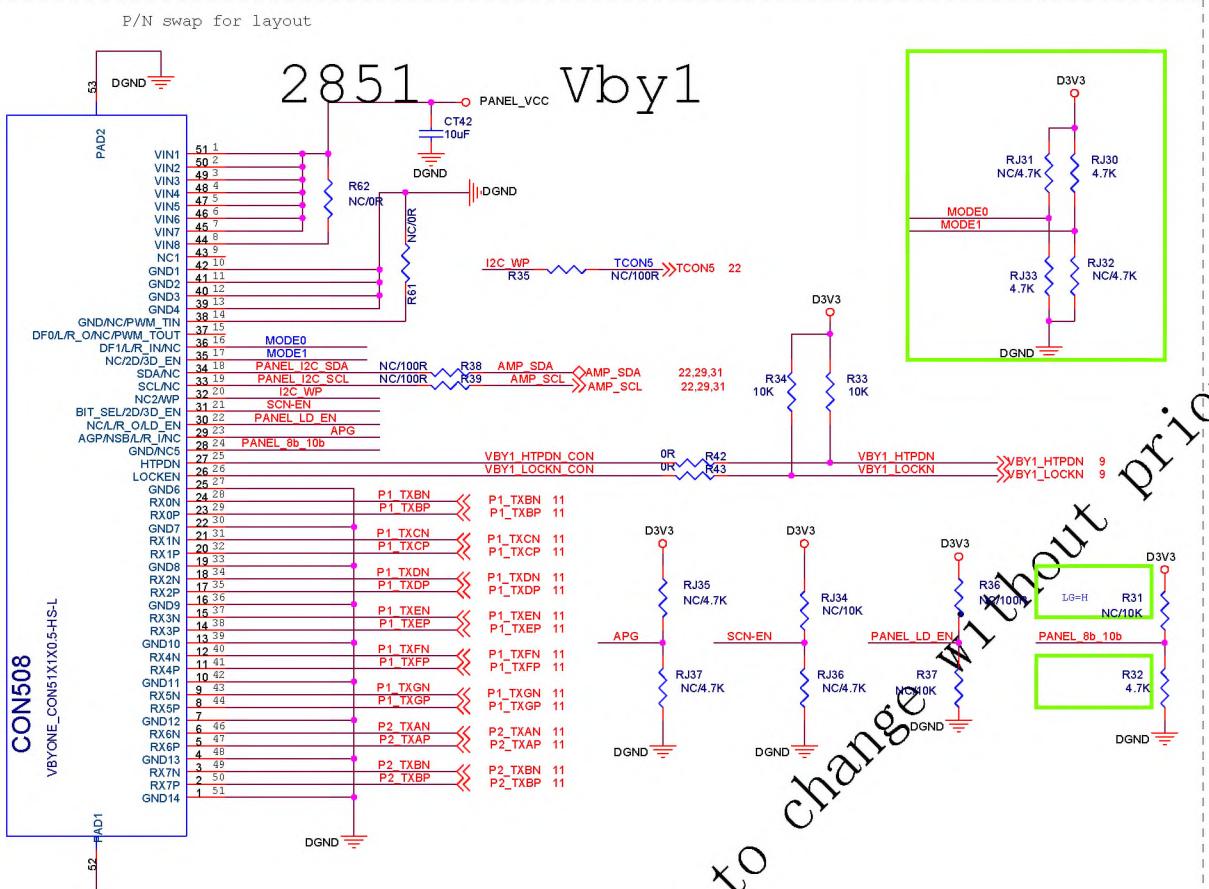
8 线路图 (CIRCUIT SCH)



AC-DC 部分

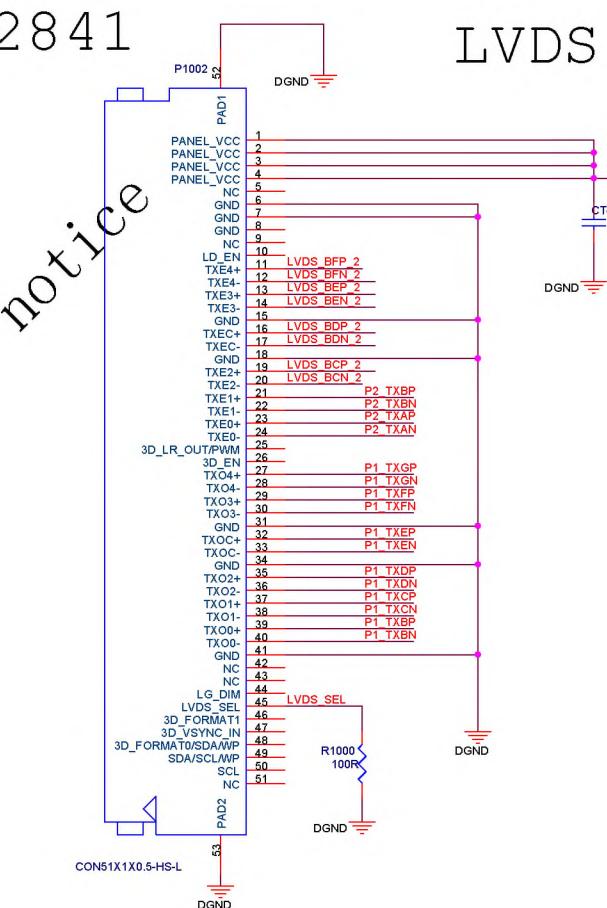


9. 原理图



The schematic diagram illustrates a complex electronic circuit with the following key components and connections:

- Power and Ground:** Various power supplies (D3V3) and ground connections (DGND) are distributed throughout the circuit.
- Serial Communication:** The circuit includes multiple serial communication paths, such as I_HTPDN CON, TXBN, TXCP, TXDN, TXDP, TXEN, TXEP, TXFN, TXFP, TXGN, TXGP, TXAN, TXAP, and TXBN, TXBP.
- Switches and Relays:** Components like TCON5, TCON6, R35, R36, R37, R38, R39, R40, R41, R42, R43, RJ32, RJ33, RJ34, RJ35, RJ36, RJ37, and RJ38 are used for switching logic and signal transmission.
- Logic Circuits:** Logic gates and buffers are represented by symbols like AND, OR, NOT, and others.
- Feedback and Control:** Feedback paths include MODE0, MODE1, VBY1_HTPDN, VBY1_LOCKN, and VBY1_HTPDN.
- Red Boxes:** Two red boxes highlight specific sections of the circuit:
 - A red box labeled "without prior notice" encloses a section involving R32, R31, R36, and R37.
 - A red box labeled "to change" encloses a section involving R32, R31, R36, and R37.

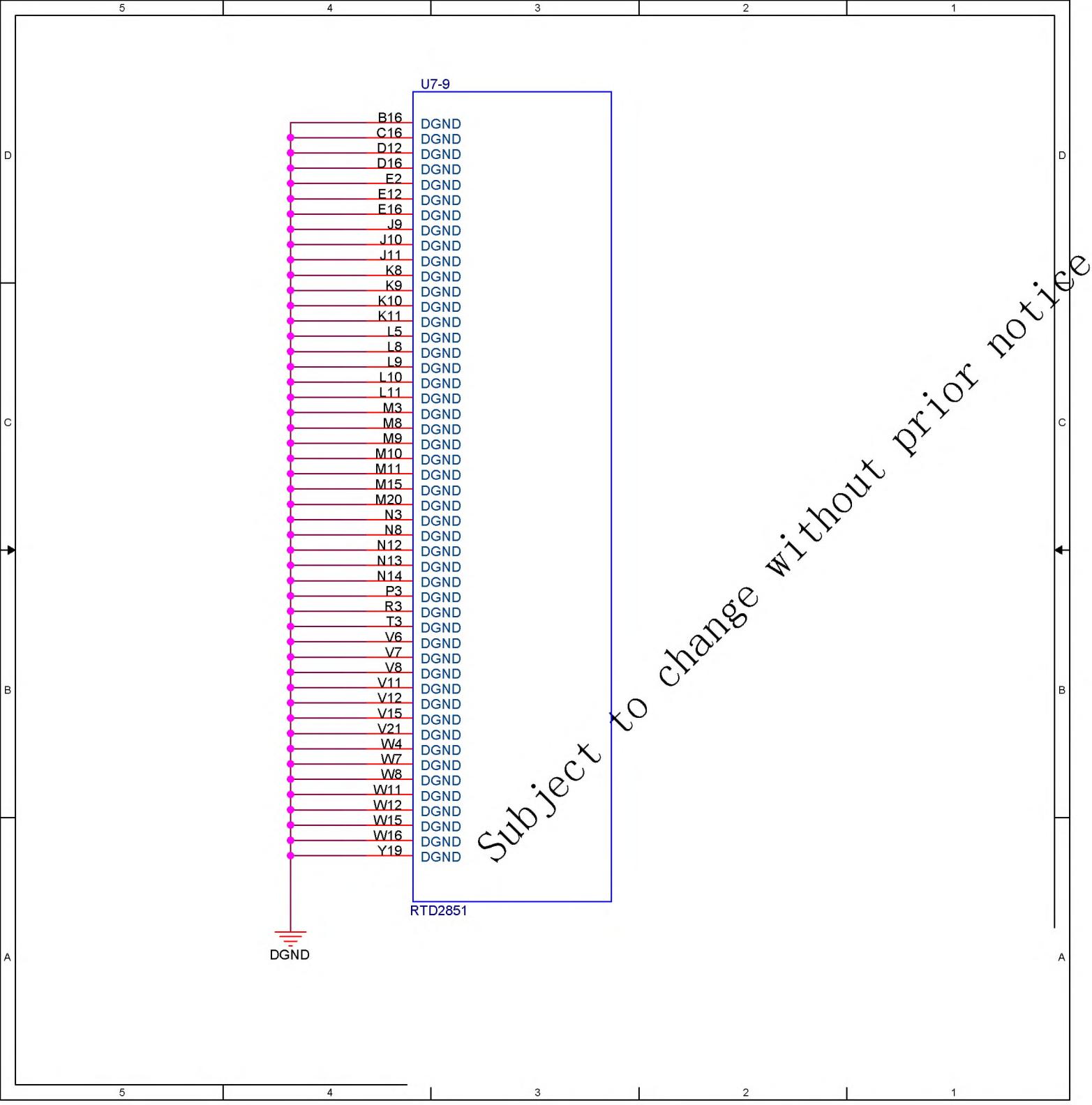


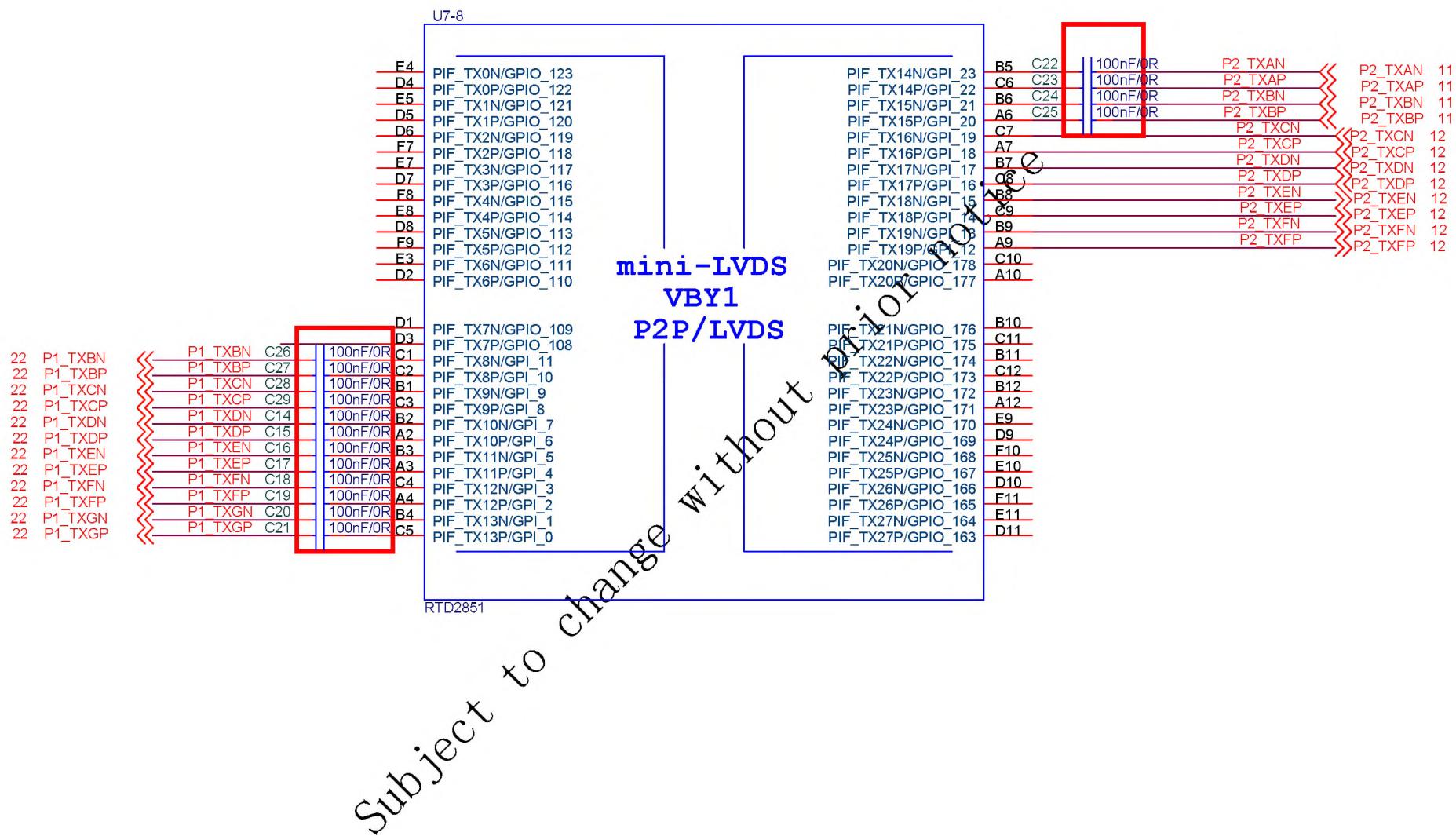
The diagram illustrates the internal connections of the RPN5 NC/0/R module. It shows two sets of P2 port connections:

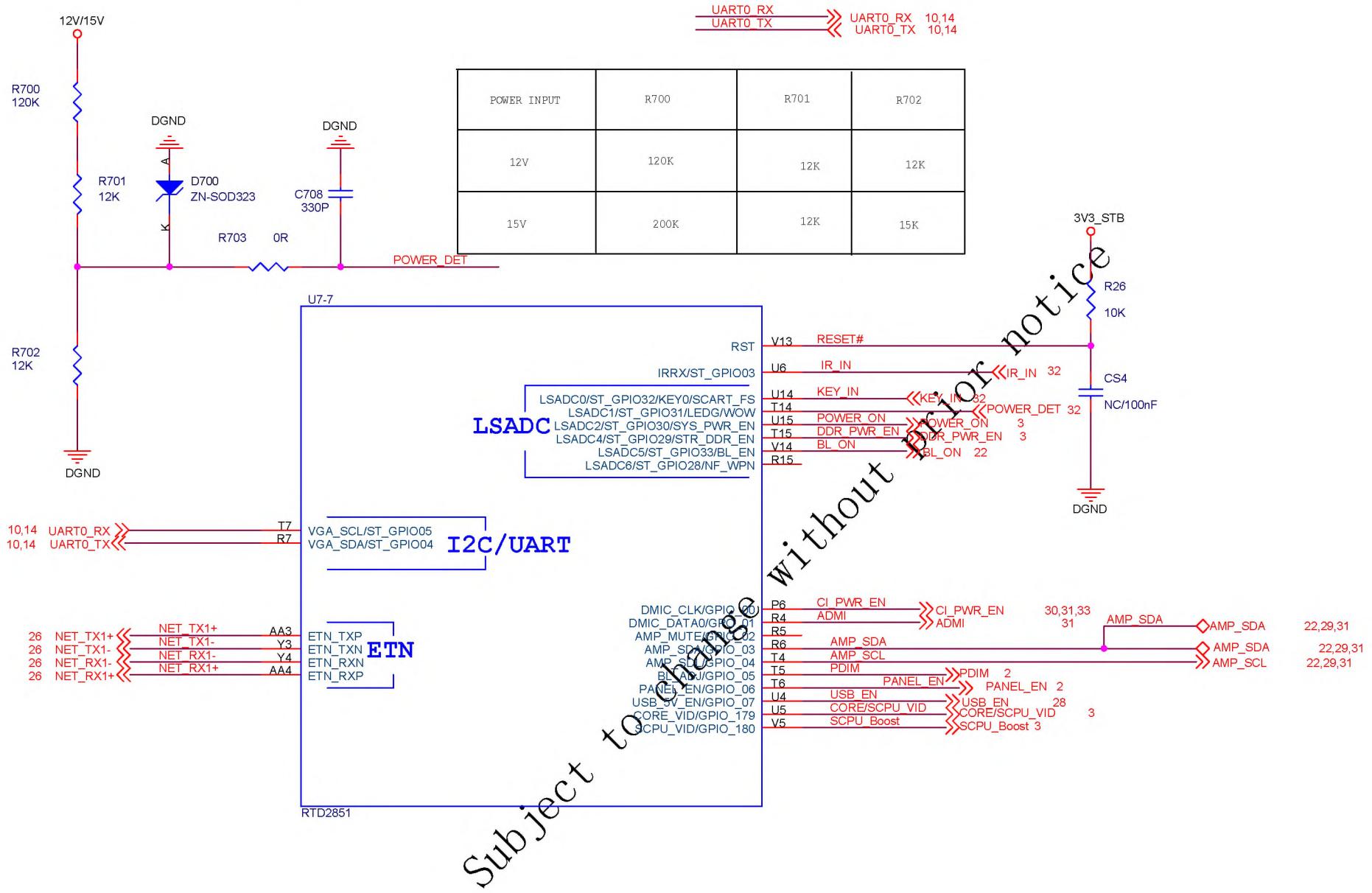
- Top Set:** P2_TXDP, P2_TXDN, P2_TCXP, P2_TXCN, and P2_TXCH are connected to TX17P_R, TX17N_R, TX16P_R, TX16N_R, and TX16R_R respectively.
- Bottom Set:** P2_RXFP, P2_RXFN, P2_RXEP, P2_RXEN, and P2_RXEN are connected to RX19P_R, RX19N_R, RX18P_R, RX18N_R, and RX18R_R respectively.

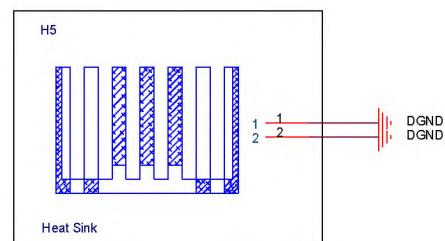
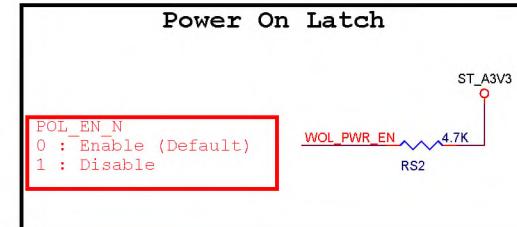
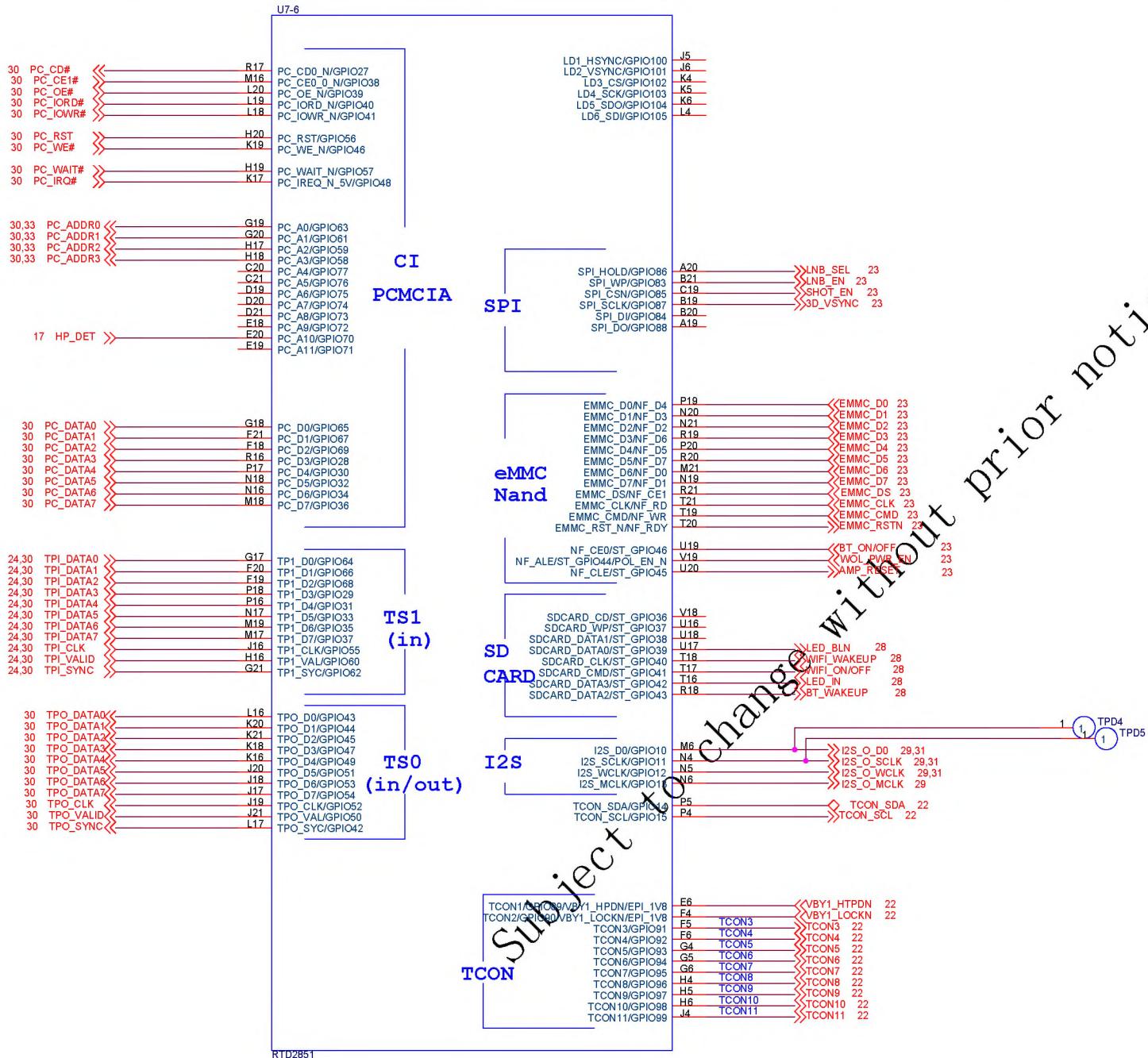
These internal blocks are then connected to external LVDS buffers (BDP, BDN, BCP, BCN) and BFP, BFN, BEP, BEN buffers. The connections are summarized in the following table:

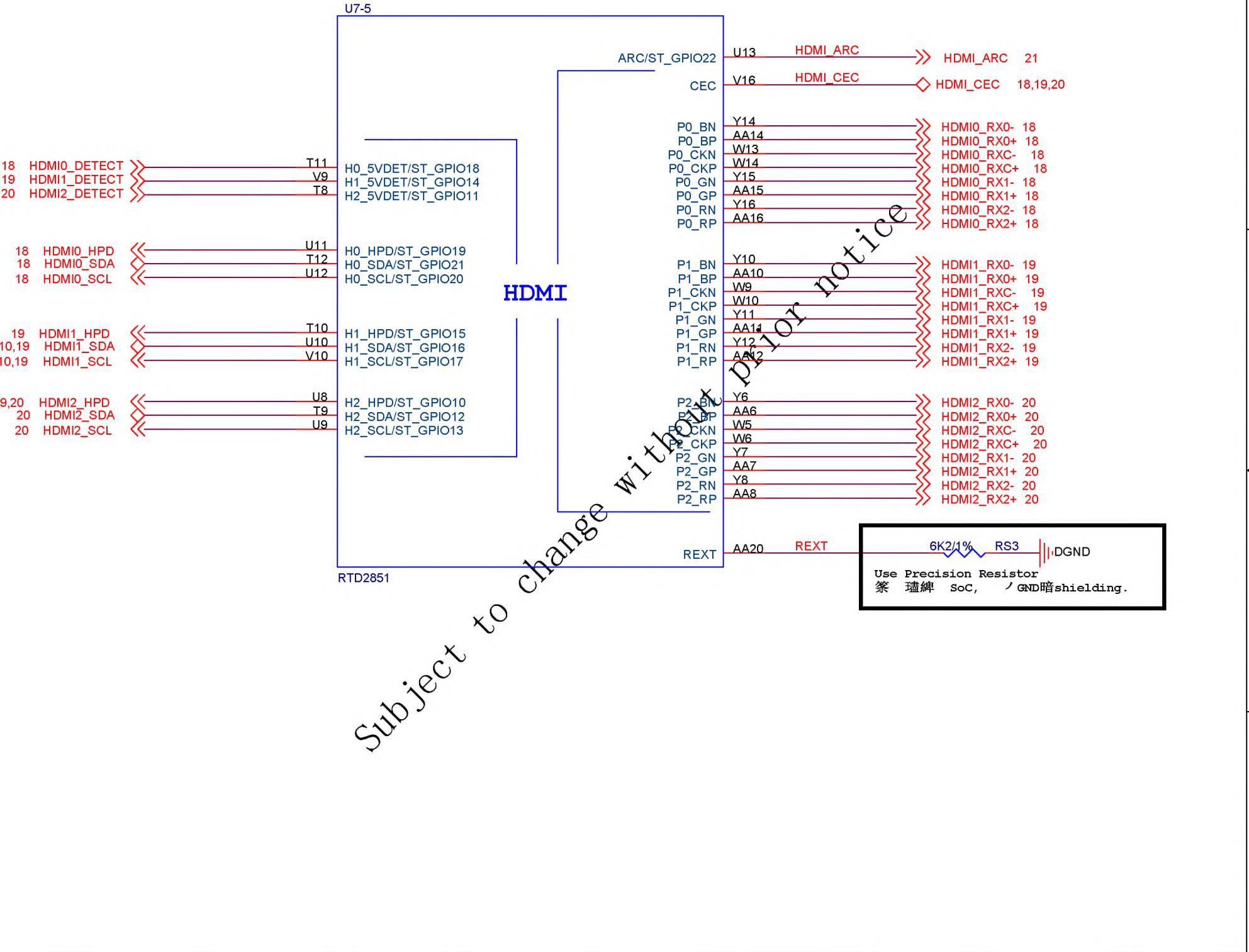
P2 Port	Internal Block	External Buffer
P2_TXDP	TX17P_R	5 LVDS BDP 2
P2_TXDN	TX17N_R	6 LVDS BDN 2
P2_TCXP	TX16P_R	7 LVDS BCP 2
P2_TXCN	TX16N_R	8 LVDS BCN 2
P2_RXFP	RX19P_R	4 LVDS BFP 2
P2_RXFN	RX19N_R	5 LVDS BFN 2
P2_RXEP	RX18P_R	6 LVDS BEP 2
P2_RXEN	RX18N_R	7 LVDS BEN 2
P2_RXEN	RX18R_R	8 LVDS BEN 2

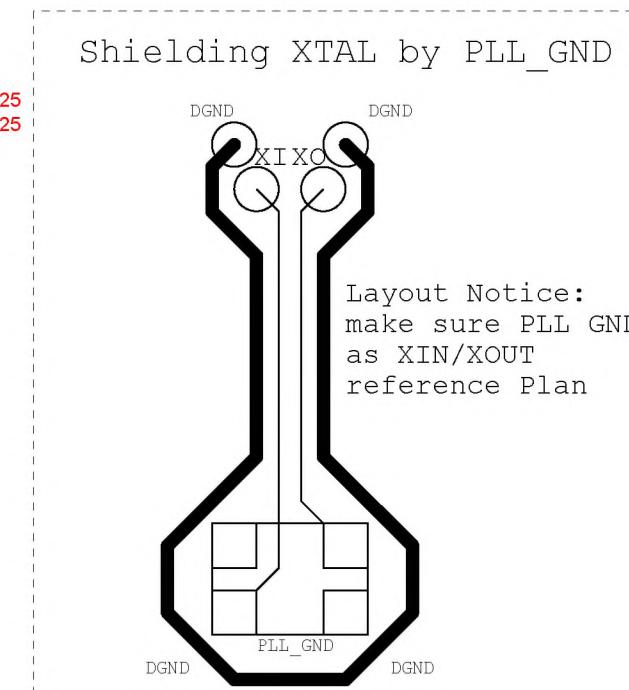
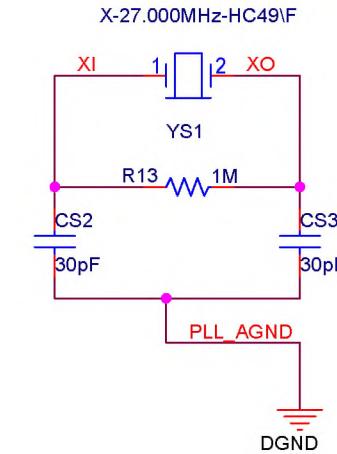
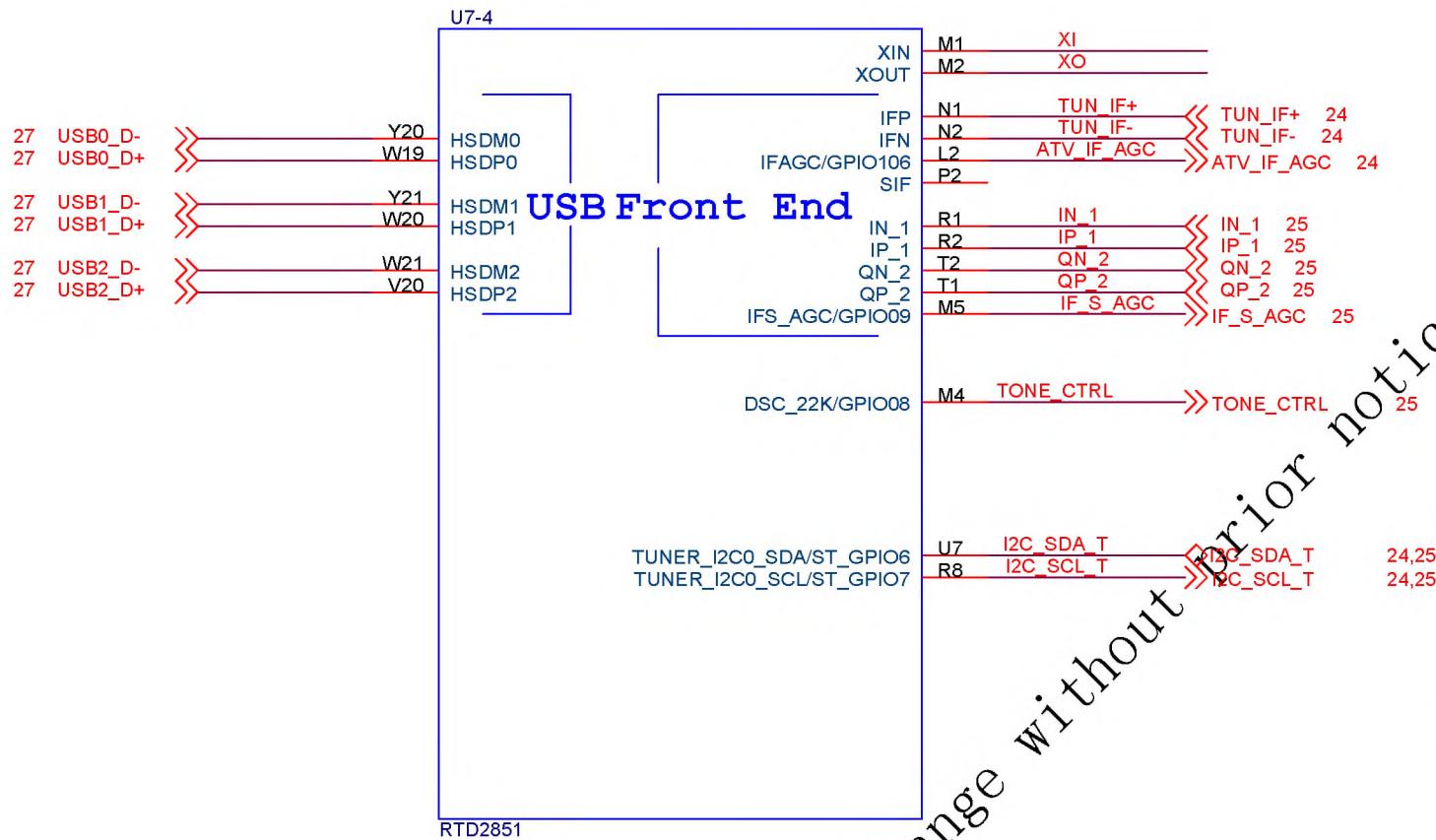


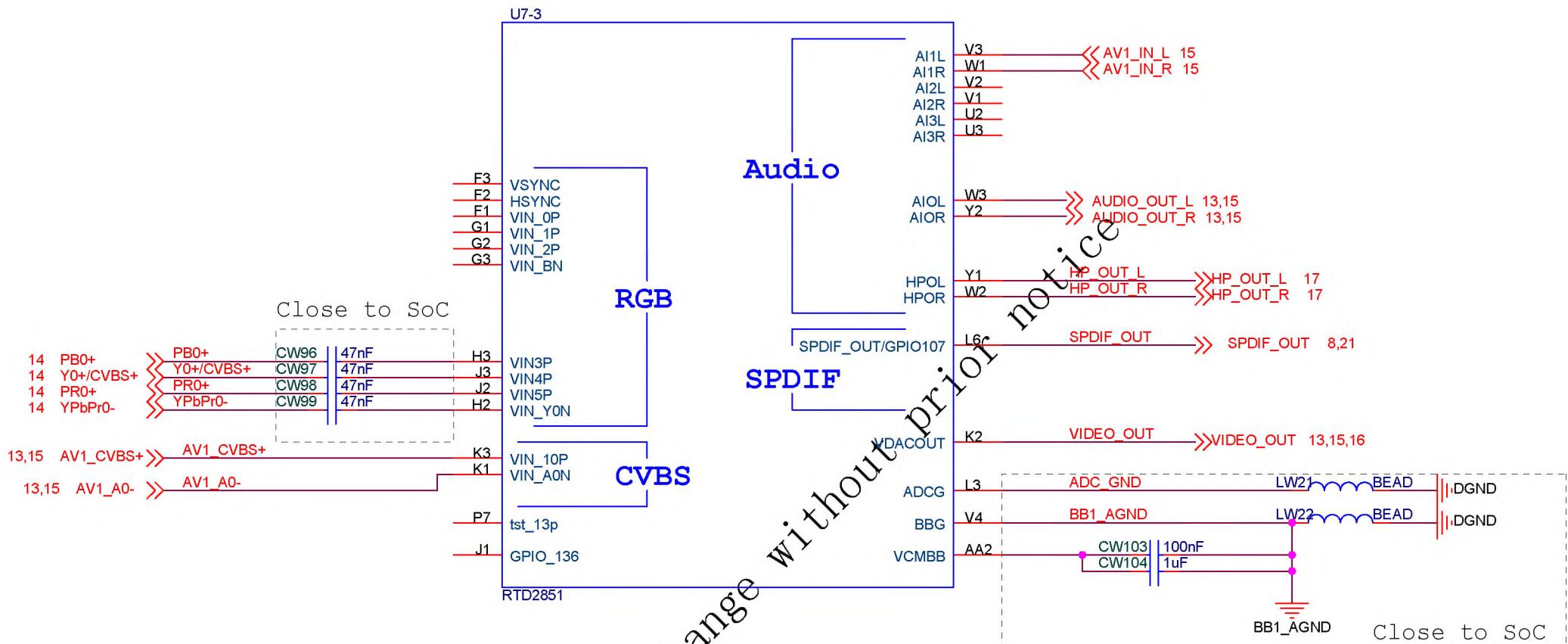












Subject to change without prior notice

C

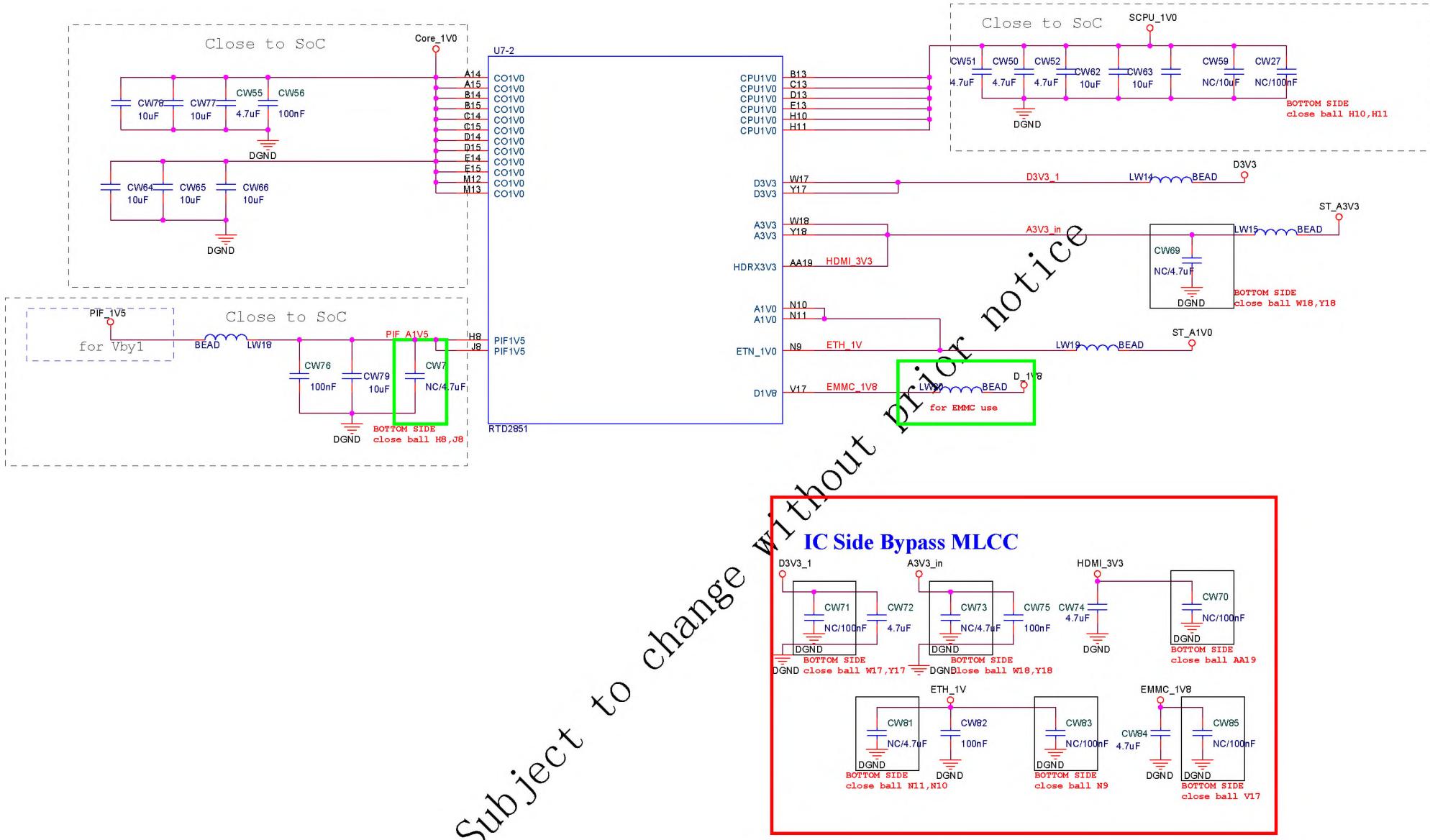
B

A

D

C

A



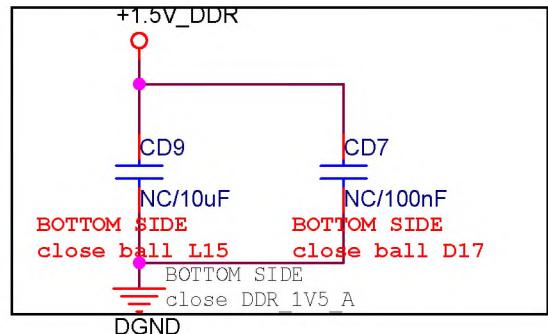
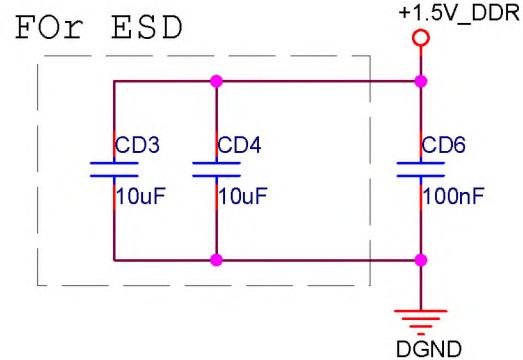
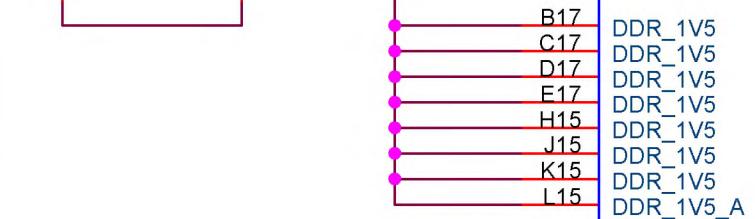
Subject to change without notice

for EMMC use

IC Side Bypass MLCC

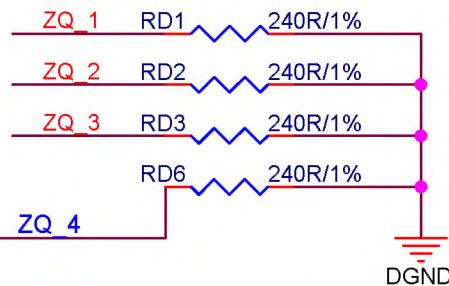
Detailed description: The diagram shows a portion of a PCB layout. At the top, there are several components and connections: PIF1V5, RTD2651, HDRX3V3, A1V0, ETN_1V0, D1V8, V17, and A3V3/A3V3. A red box highlights a section labeled "for EMMC use" which includes components like A1V0, N10, N11, N9, ETH_1V, V17, EMMC_1V8, LW19, BEAD, and D_1V8. Below this, another red box encloses the "IC Side Bypass MLCC" section. This section contains two sets of parallel bypass networks. Each network consists of a capacitor (CW71, CW72, CW73) connected between a power rail and ground, with a NC/100nF component in series with CW71. The bottom side of each network is connected to a close ball (W17/Y17 or W18/Y18). The top side of CW72 is connected to the A3V3_in rail. Below the networks, labels indicate "BOTTOM SIDE close ball W17,Y17" and "BOTTOM SIDE close ball W18,Y18". The bottom part of the diagram shows two more parallel bypass networks for ETH_1V, labeled CW81 and CW82, with similar component and connection details.

DRAM Controller

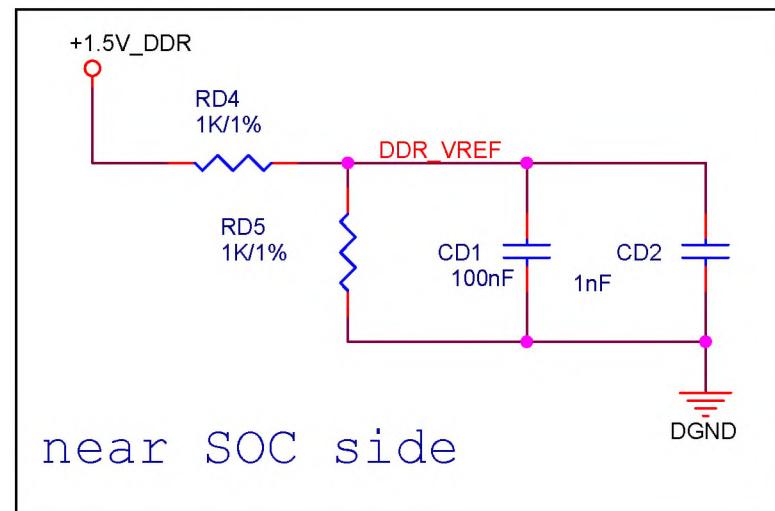


Subject to change without prior notice

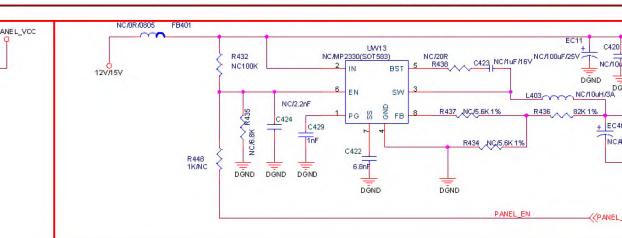
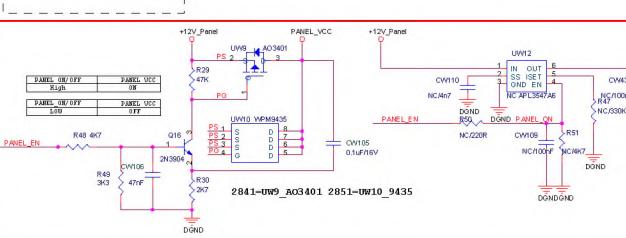
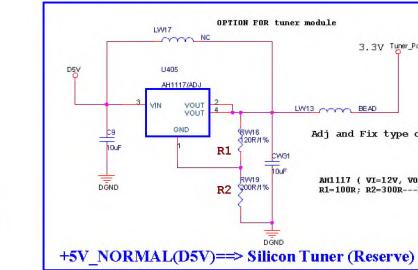
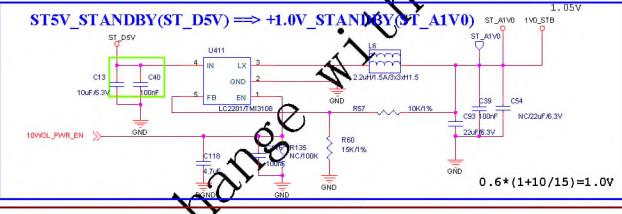
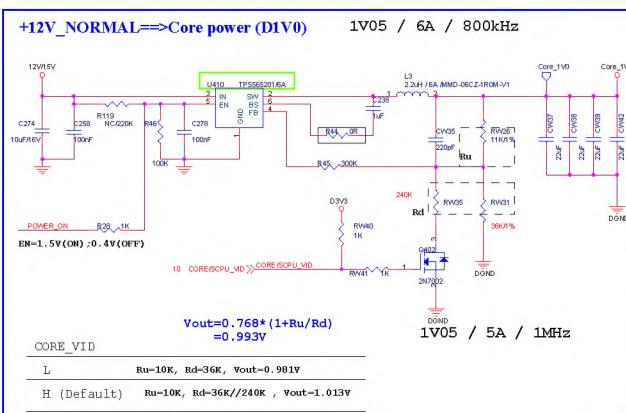
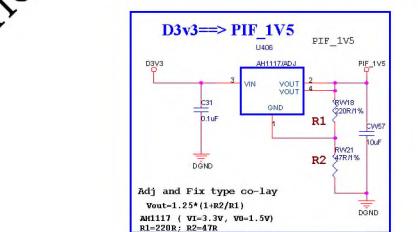
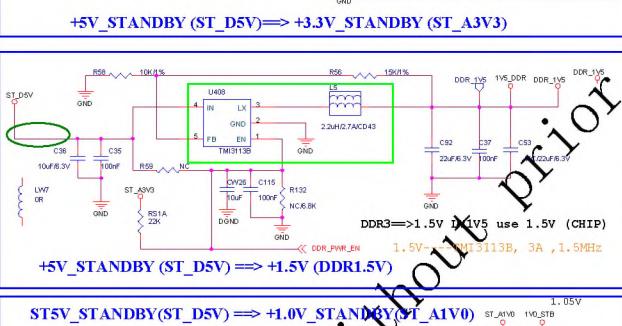
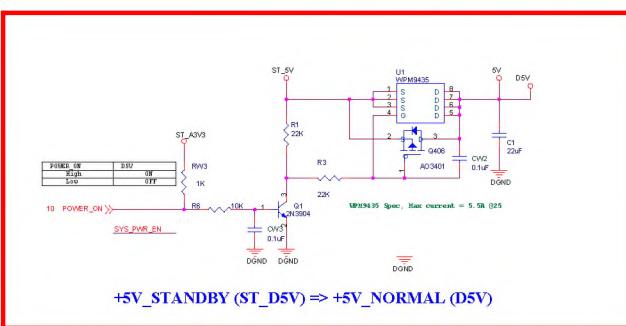
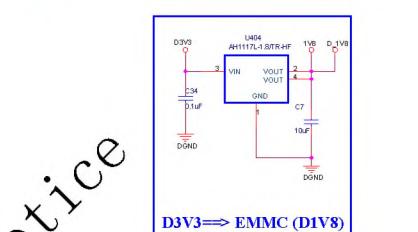
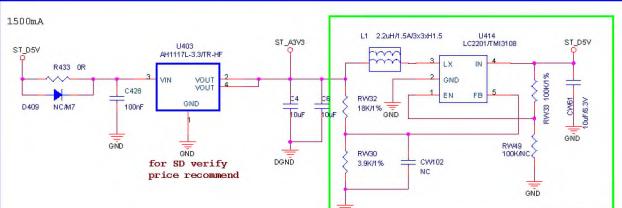
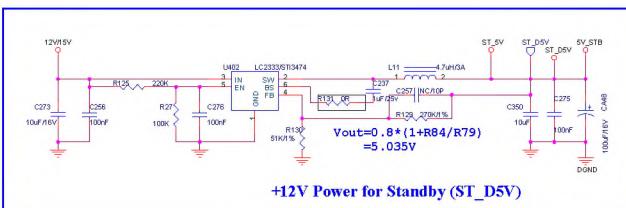
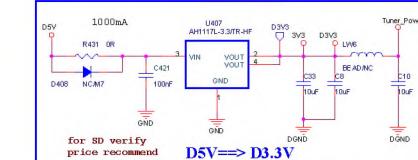
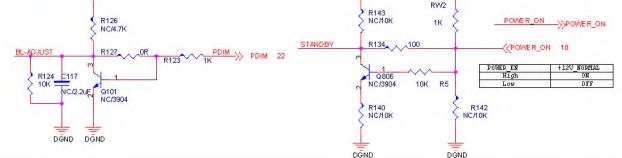
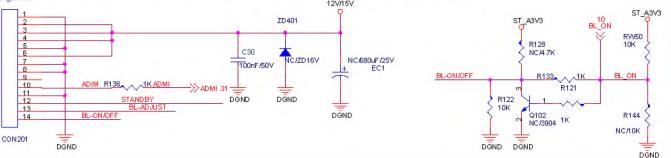
Vref
ZQ1
ZQ2
ZQ3
ZQ4
A18 DDR_VREF
B18 ZQ_1
C18 ZQ_2
D18 ZQ_3
G16
ZQ_4

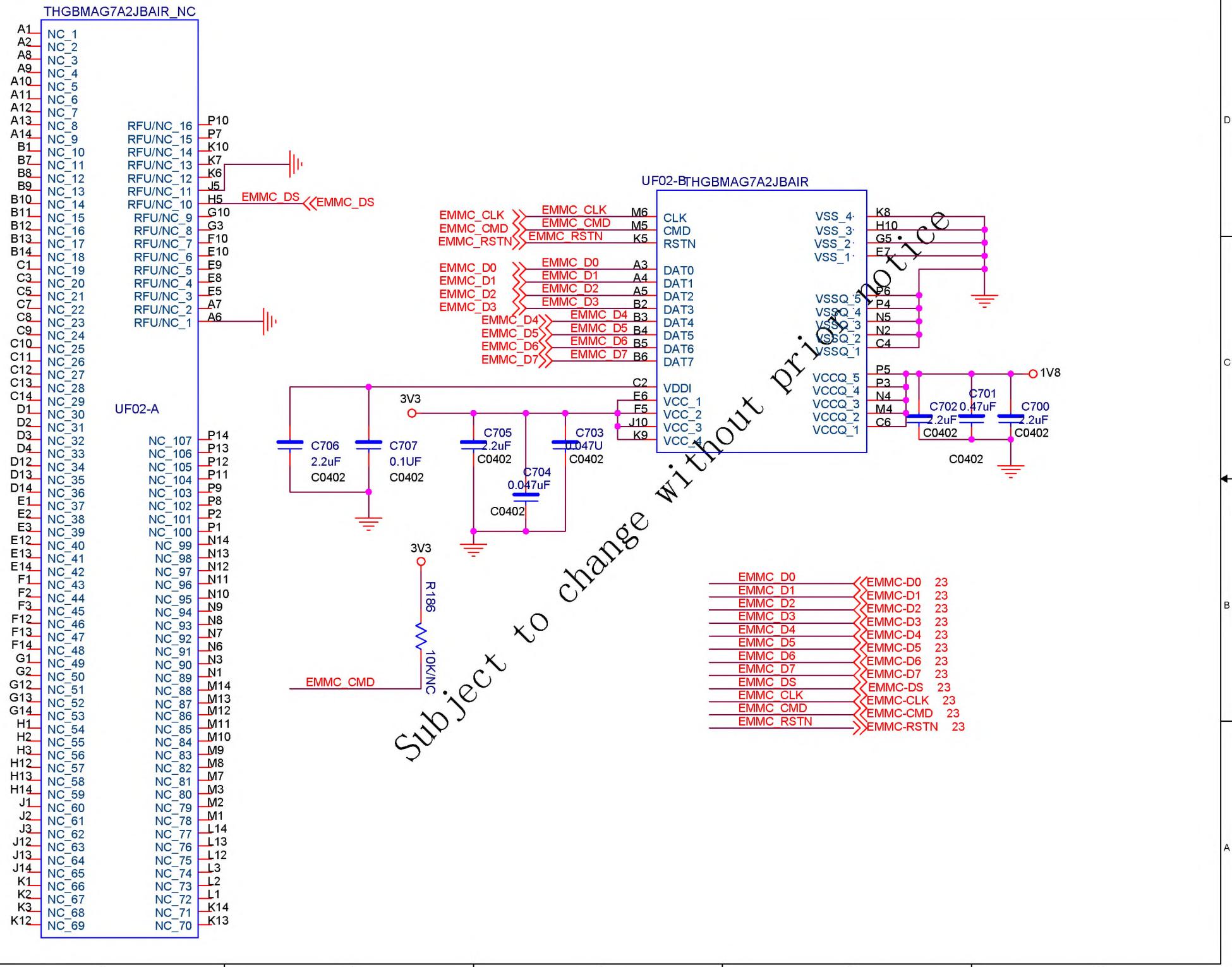


DDR Size Option
2.0GB: RD1, RD2, RD3, RD6 mount
1.5GB/1GB: RD1, RD2, RD3 mount

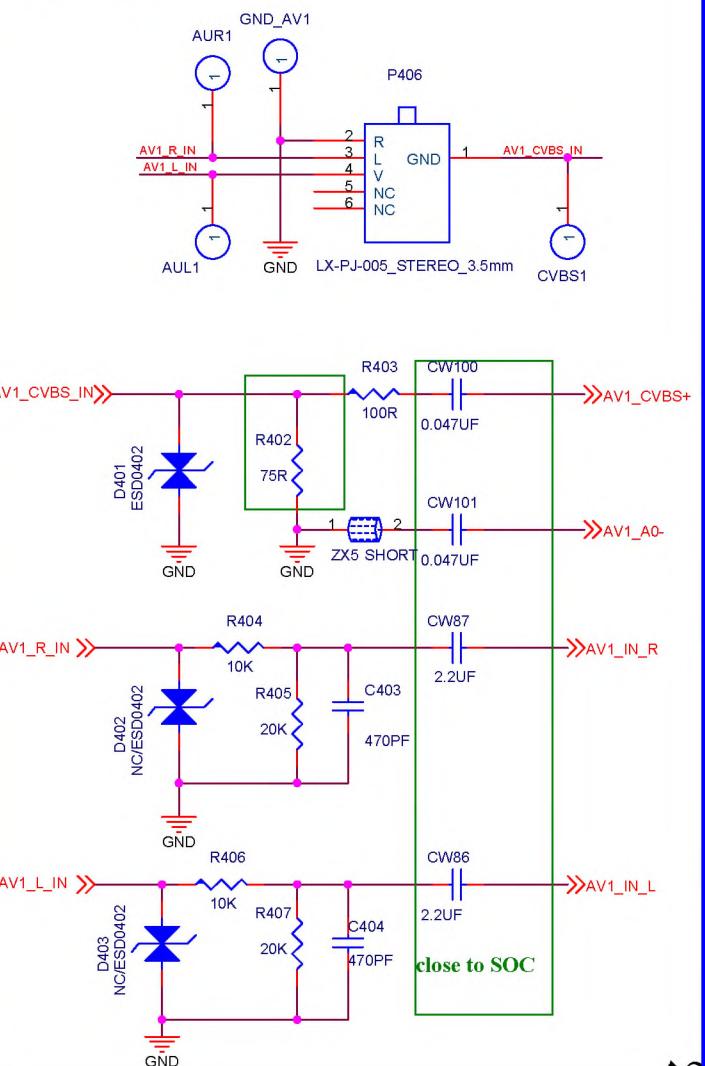


Power socket and Signal switching control

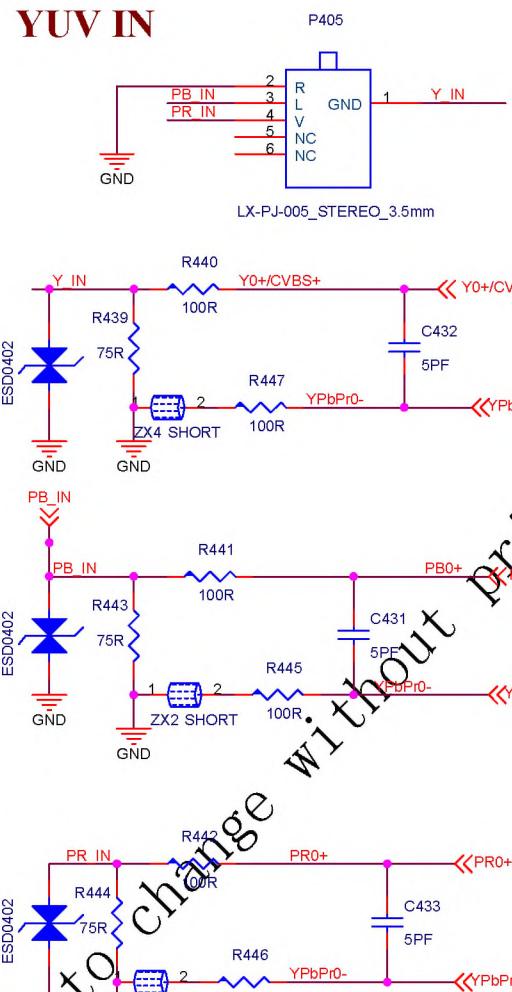




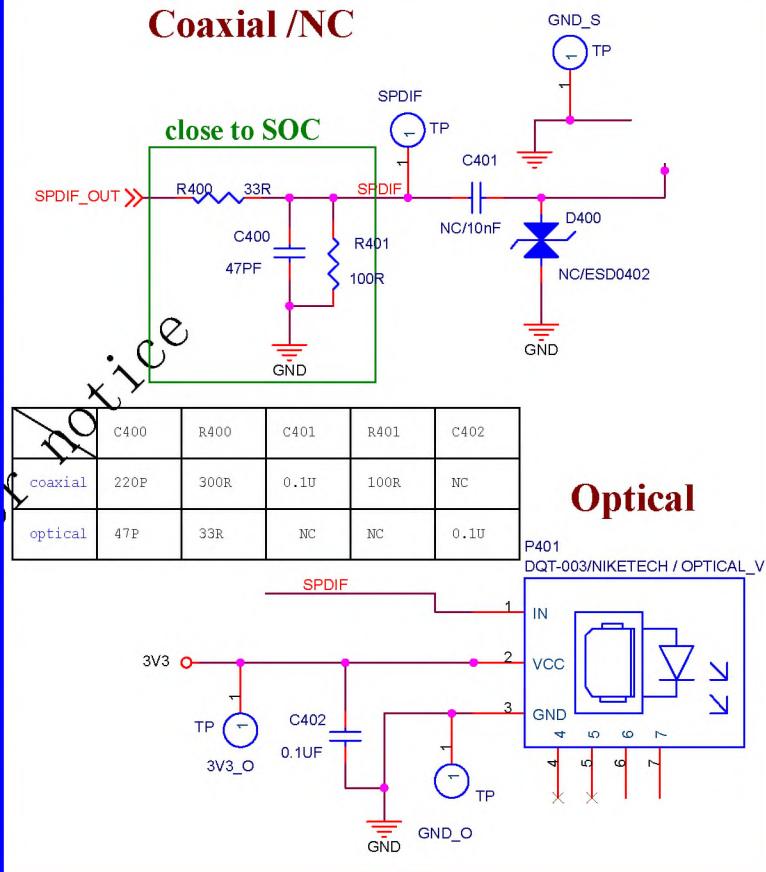
AV IN



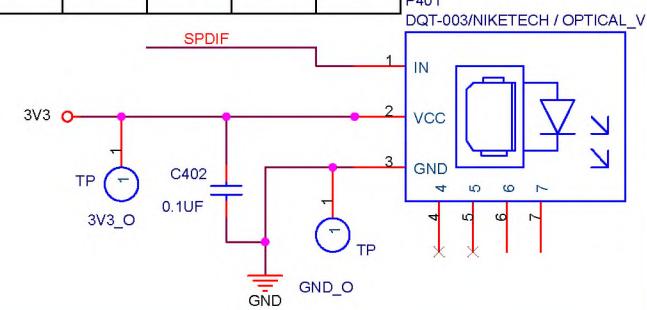
YUV IN

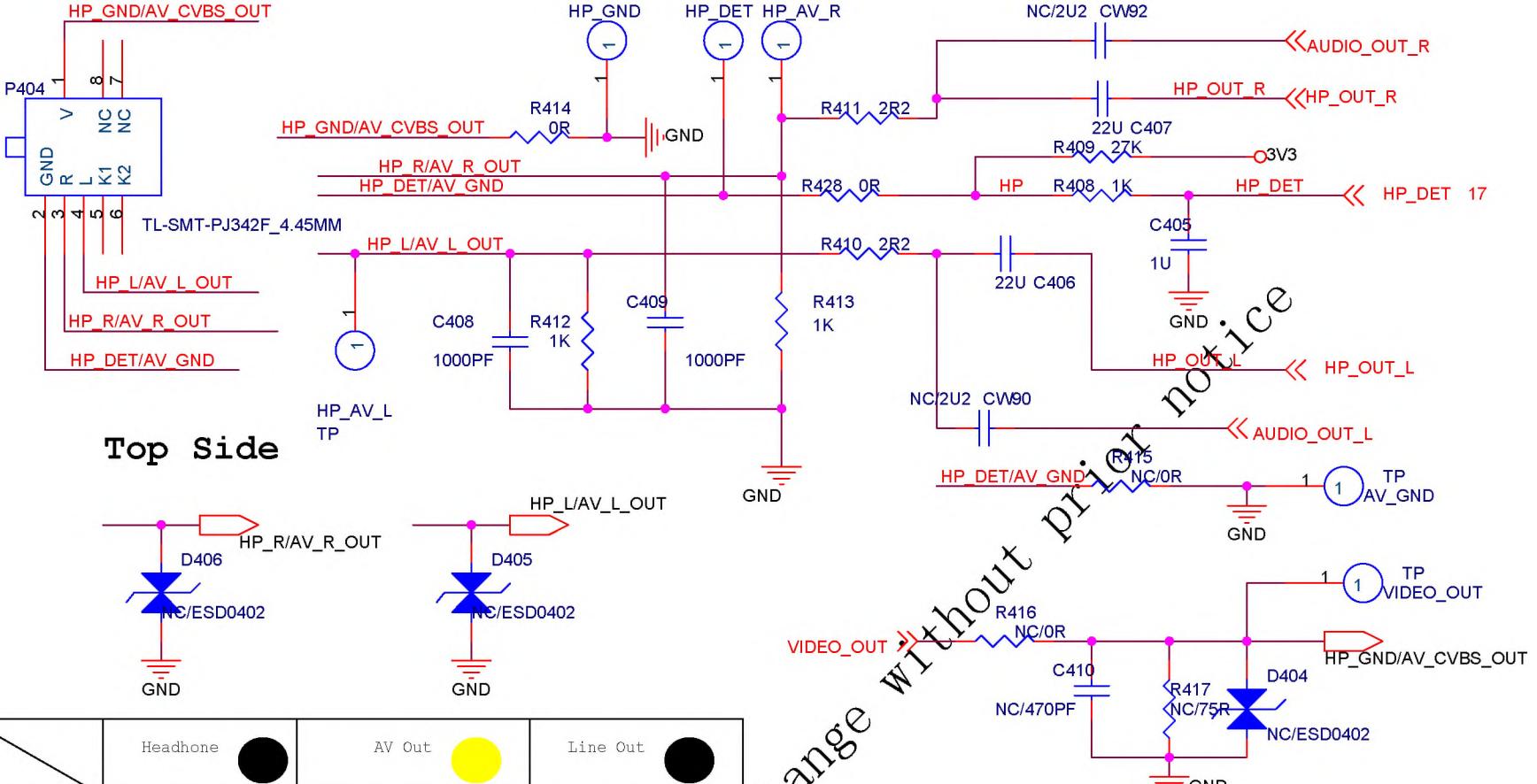


Coaxial / NC

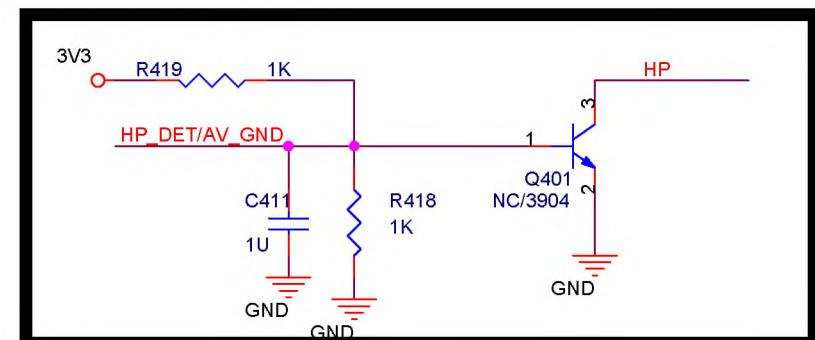


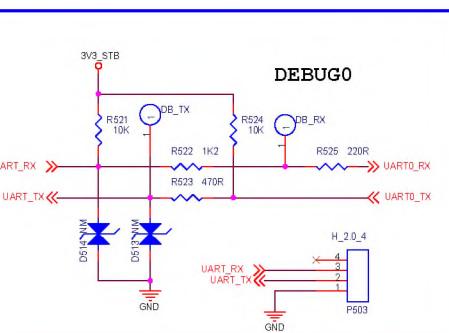
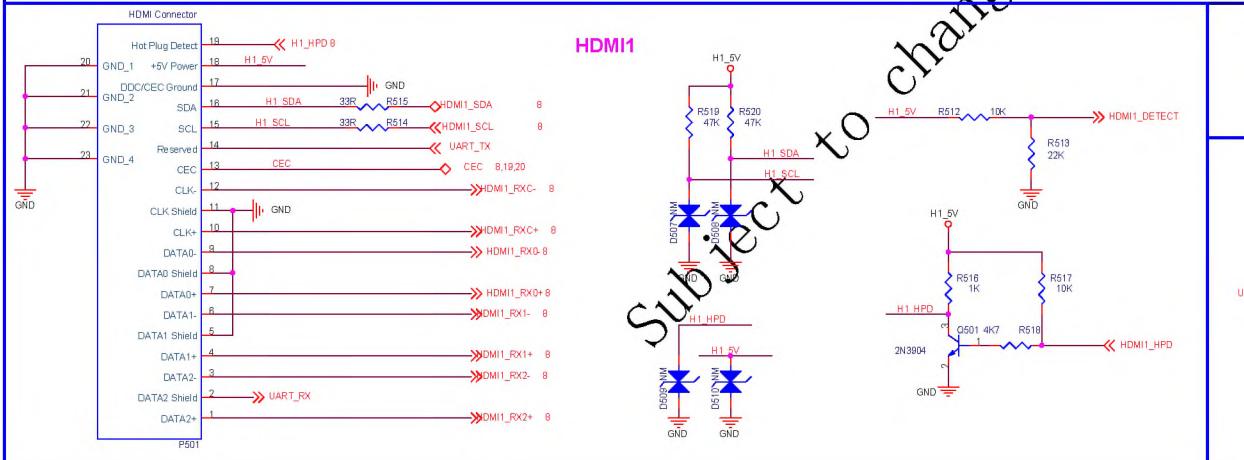
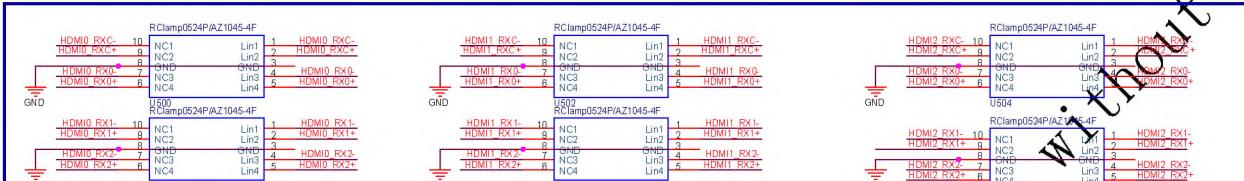
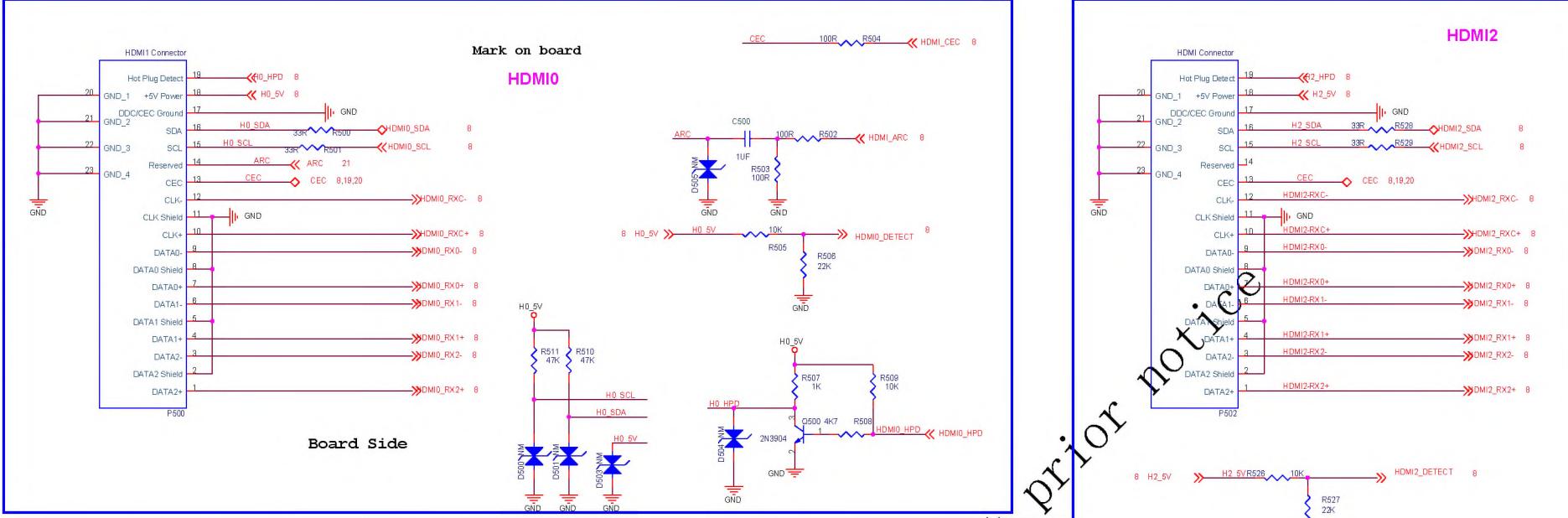
Optical



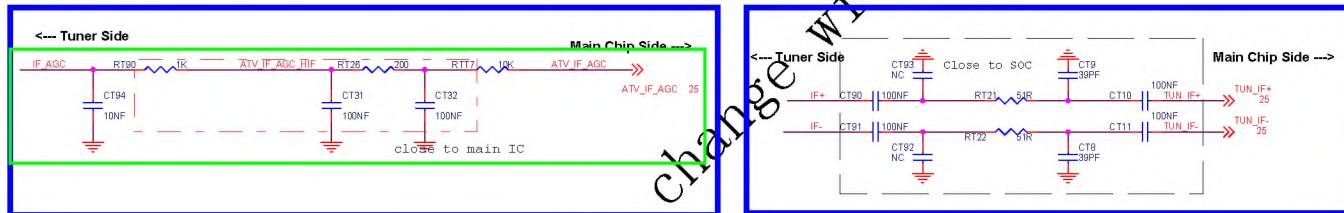
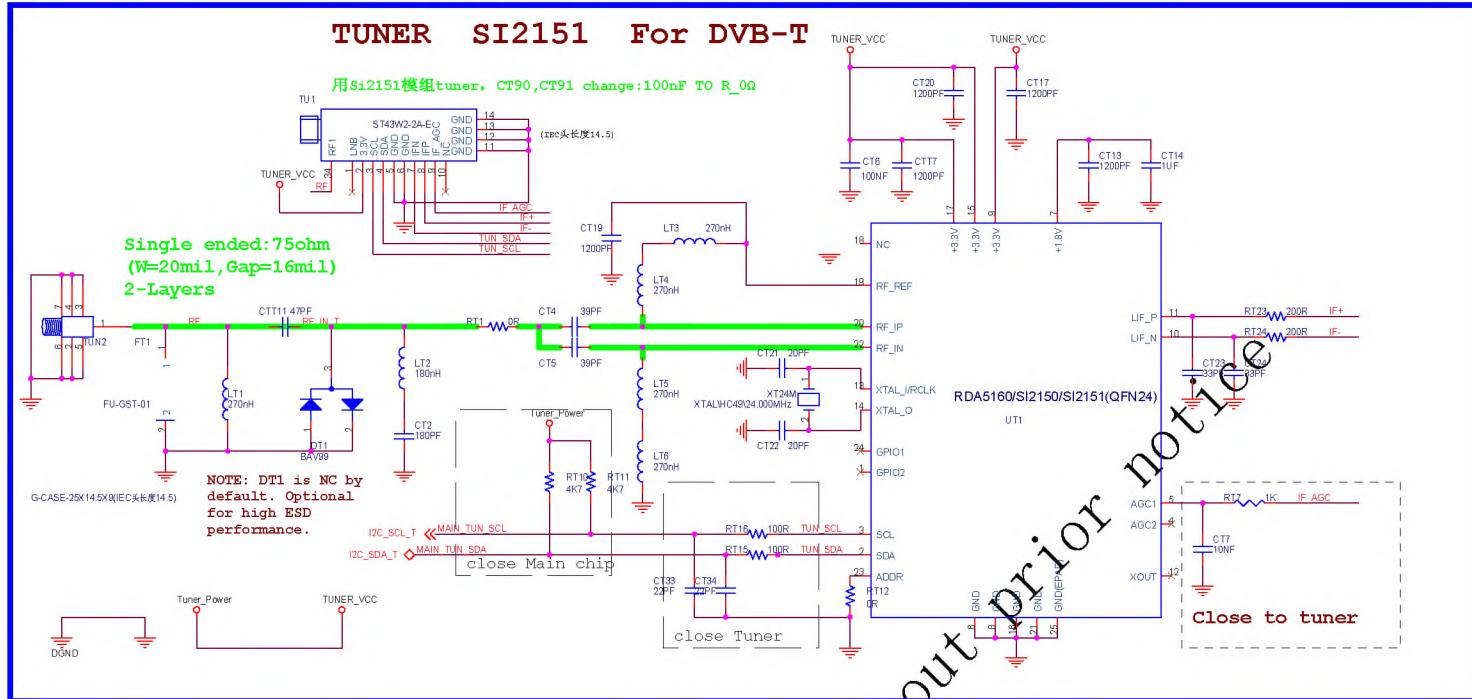


	Headphone	AV Out	Line Out
P1	HP_GND	VIDEO_OUT	NC
P2	HP_DET	AV_GND	AV_GND
P3	HP_R	AV_R_OUT	LINE_OUT_R
P4	HP_L	AV_L_OUT	LINE_OUT_L
R414	0R	NC	NC
R415	NC	0R	0R
R428	0R	NC	NC
R412, R413	1K	10K	10K
C408, C409			





TUNER SI2151 For DVB-T



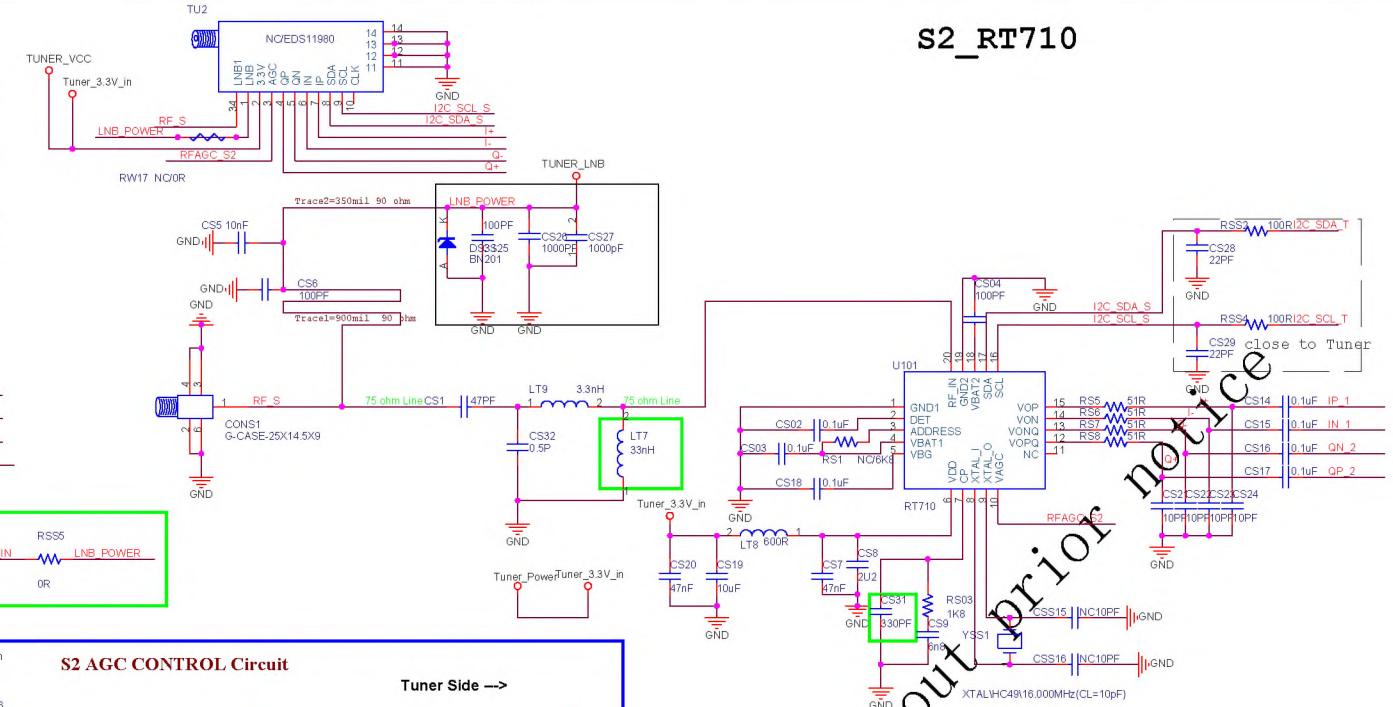
Subject to
change

S2_RT710

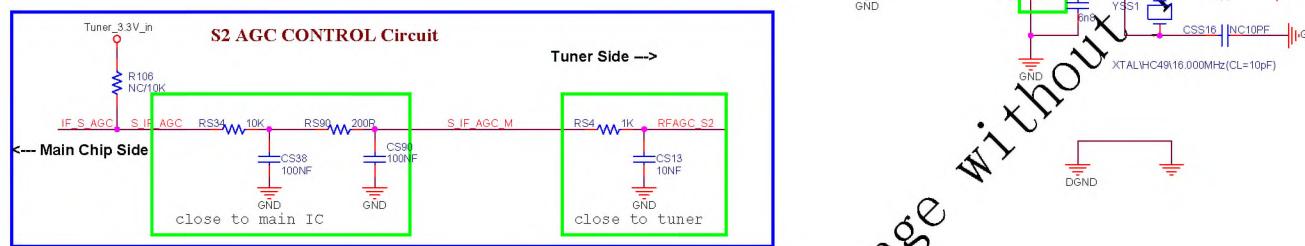
Main Chip <--

- 24,25 IF_AGC >> IF_AGC
- 7,24 I2C_SCL_T >> I2C_SCL_T
- 7,24 I2C_SDA_T >> I2C_SDA_T
- 7 QP_2
- 7 QN_2
- 7 IP_1
- 7 IN_1
- 7 IF_S_AGC >> IF_S_AGC
- 24,25 IF+ >> IF+
- 24,25 IF- >> IF-

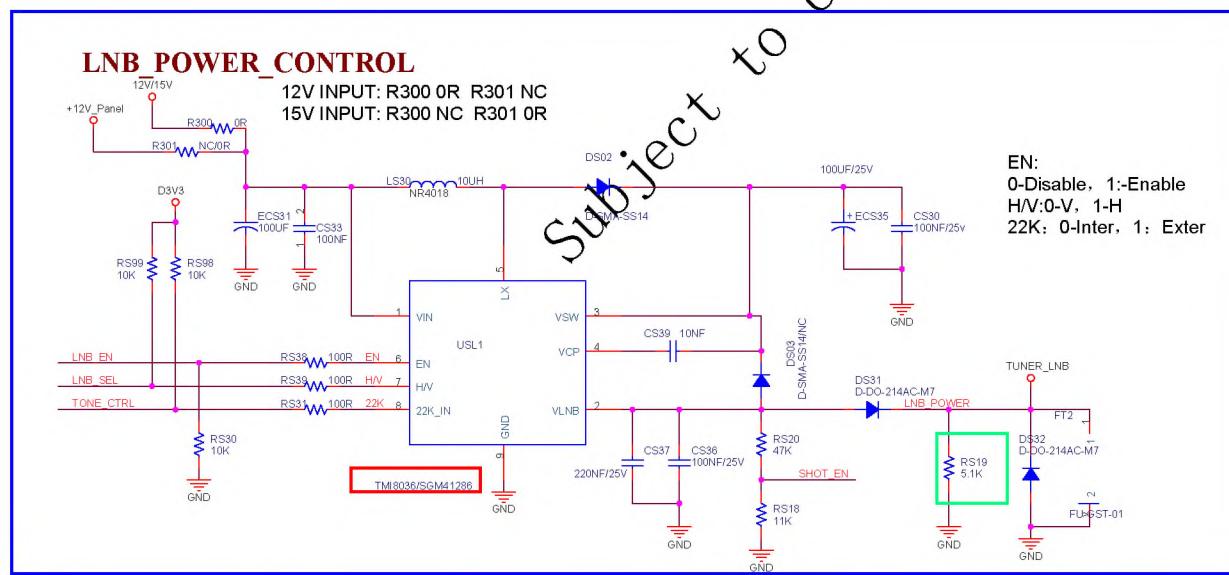
- 7 LNB_EN << LNB_EN
- 7 LNB_SEL << LNB_SEL
- 7 TONE_CTRL << TONE_CTRL
- 9 SHOT_EN >> SHOT_EN

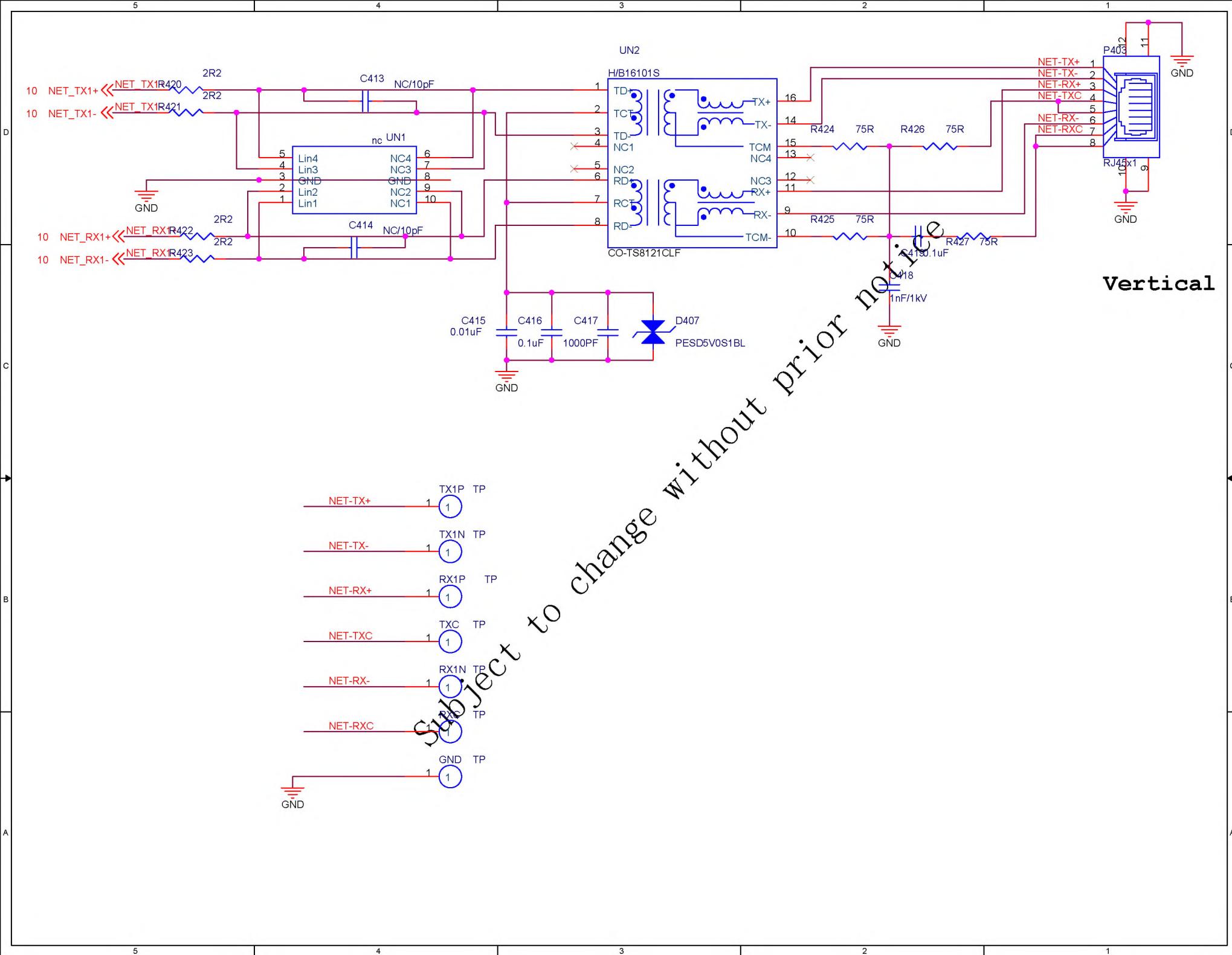


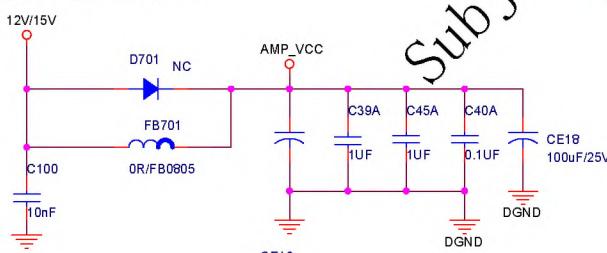
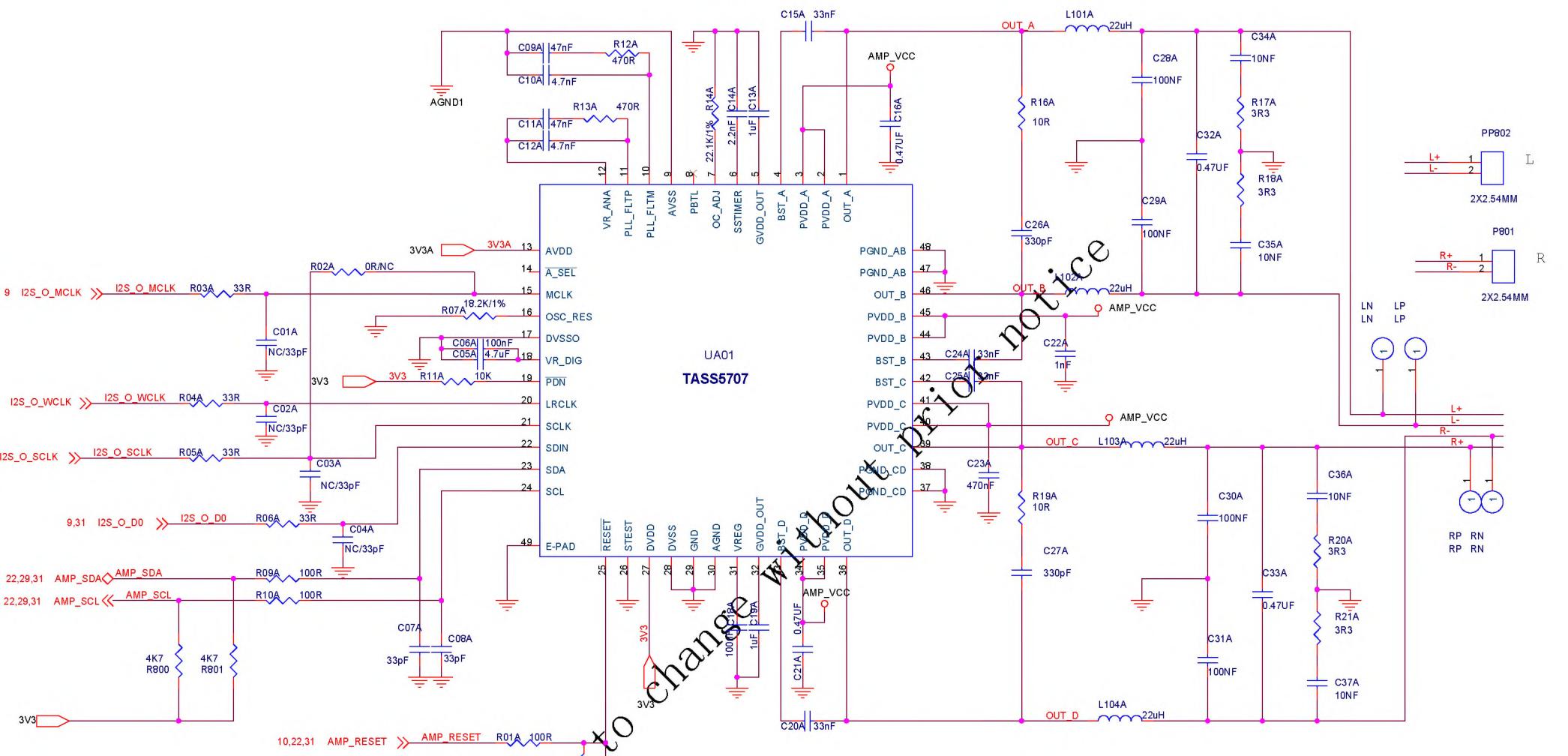
S2 AGC CONTROL Circuit

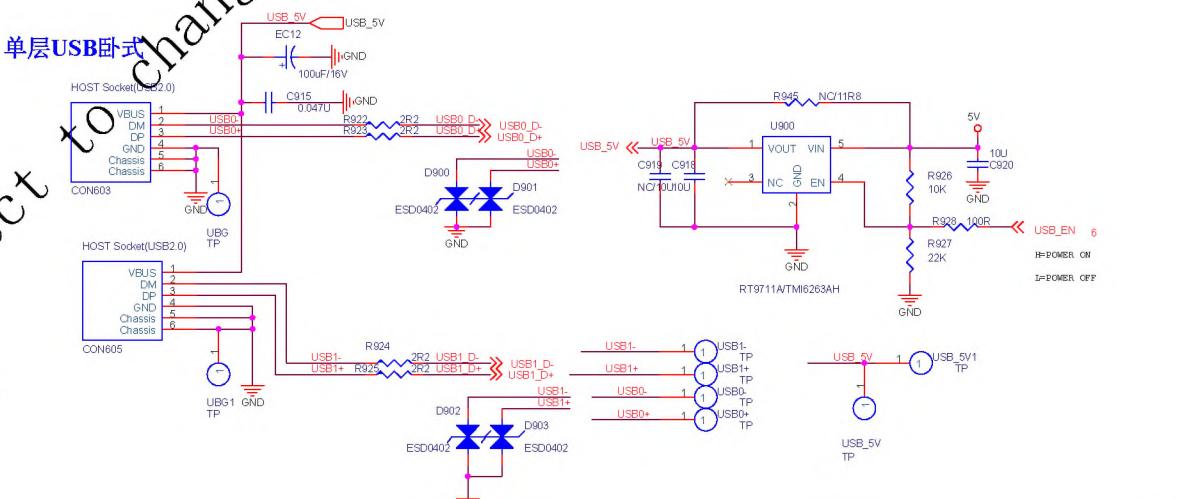
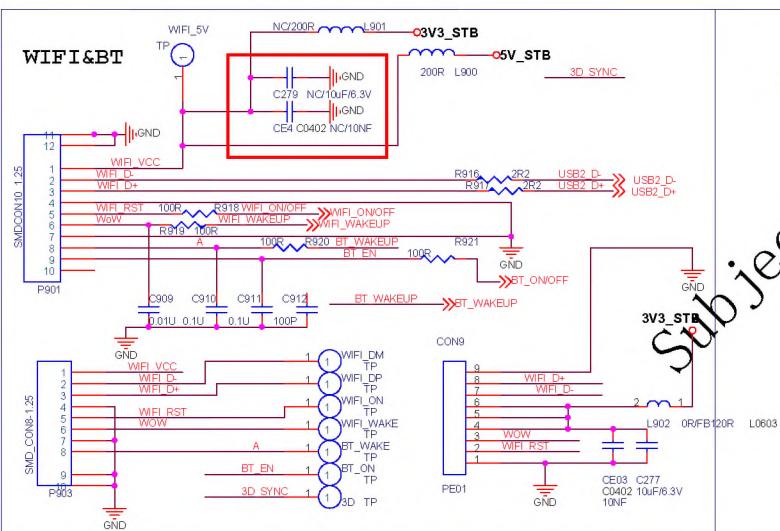
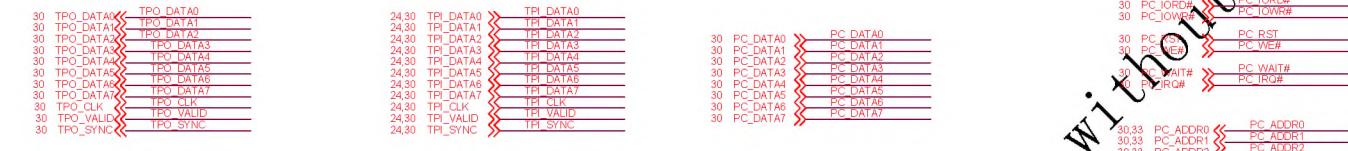
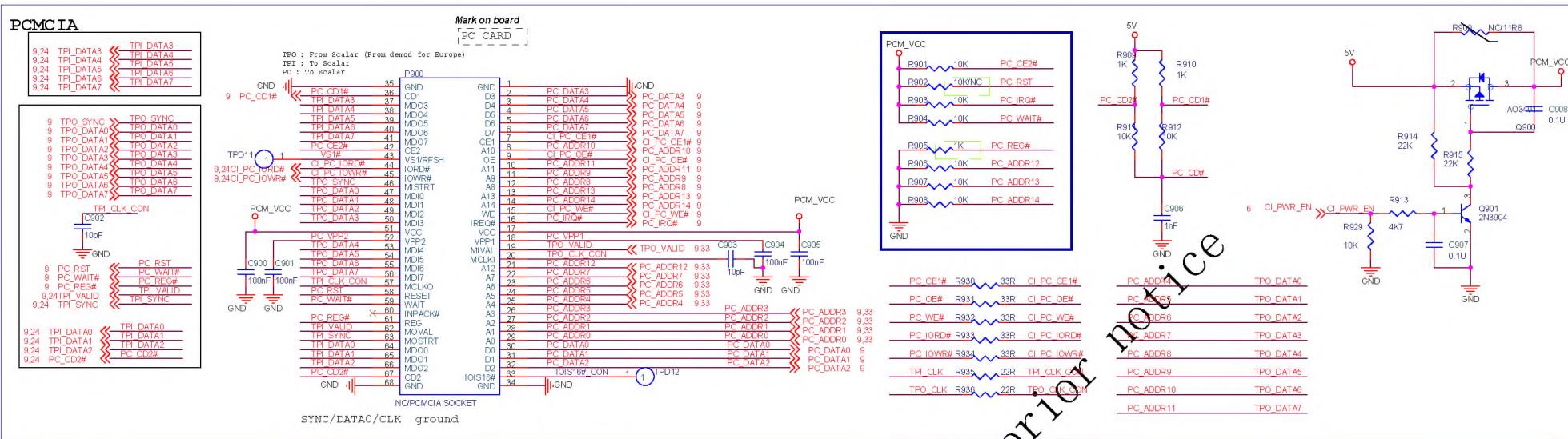


LNB_POWER_CONTROL

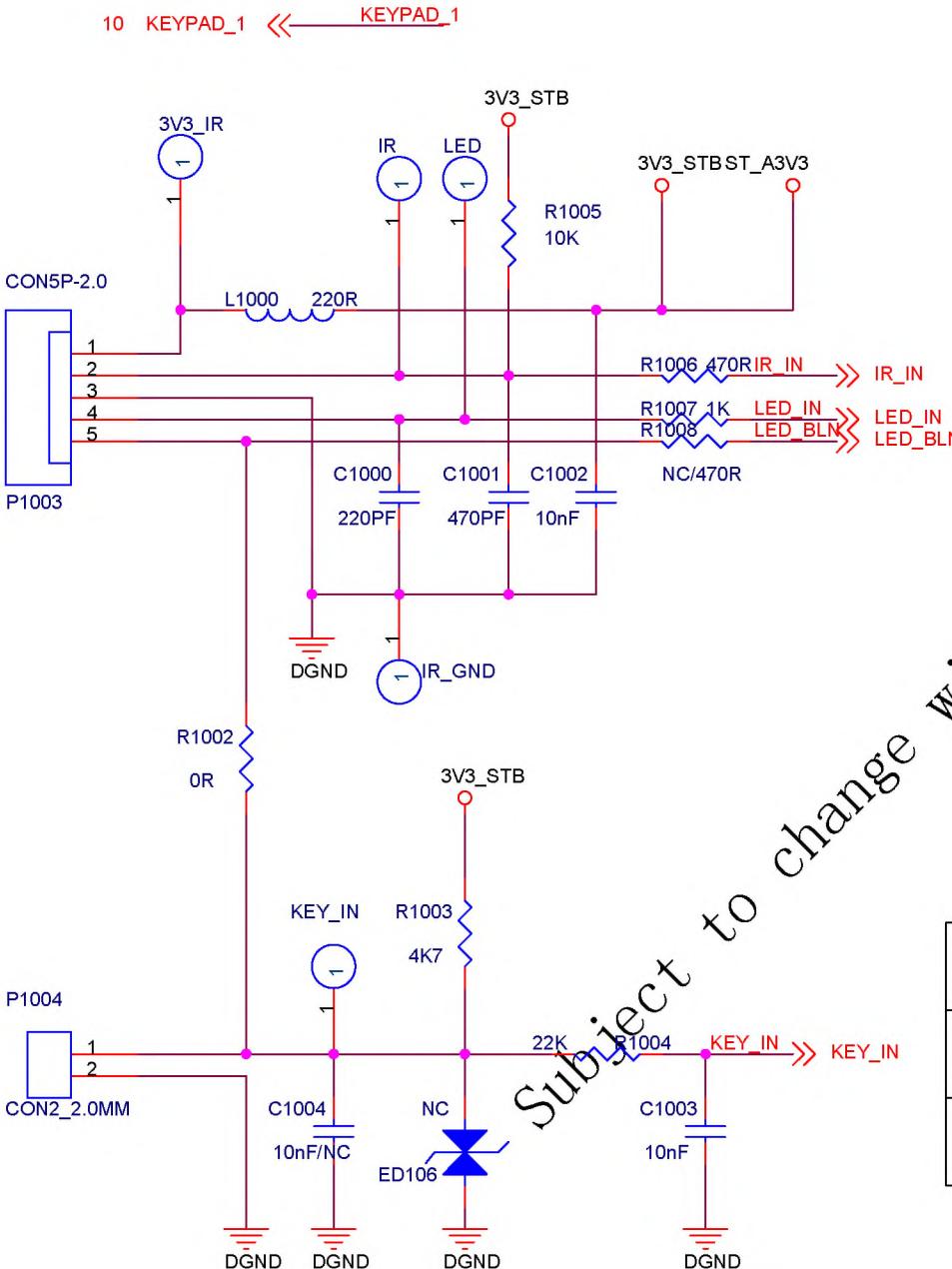








From Main Chip



Subject to change without prior notice

Note:	P1003	P1004	R1002	R1008	LED_BLN
Key&IR 2IN1	ON	NC	ON	NC	N.A
Separate	ON	ON	NC	NC	N.A
	ON	ON	NC	ON	Separate