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Embedded Systems

Natural Logarithm Implementation For BFloat16 FPU

REV. 0.1

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Abstract

The goal of the project was to add the support for the FLOG operation to a Floating Point Unit and verify the correctness against the results produced by the corresponding C function. Thus we designed a module which calculates the natural logarithm of a number in bfloat16 floating-point format (Brain Floating Point) and provides the result in the same format.

Chapter 1

Algorithm and Architecture

Considering only the case where the input X s a valid positive bfloat16 number, i.e.

$$X = 1.F * 2^{(E-E_0)}$$

If we calculate its natural logarithm, we obtain:

$$R = log(X) = log(1.F) + (E - E_0) * log(2)$$

Therefore the evaluation of the result is divided in two main parts:

- computation of $log(1.F)$ with$1.F \in [1, 2)$
- computation of the product $(E - E_0) * log(2)$

In order to get a better accuracy the output range of $log(1.F)$ is centered around zero in the following way:

$$R = \begin{cases} log(1.F) + (E - E_0)log(2) & when\ 1.\text{F}\in [1, \sqrt{2}) \\ log(\frac{1.F}{2}) + (1 + E - E_0)log(2) & when\ 1.\text{F}\in [\sqrt{2}, 2) \end{cases}$$

Input operators different from the X specified above are handeled as special cases, in particular:

Input		**Output**
sign bit	**special cases**	**special cases**
1(negative)	Any value	NaN
0(positive)	Zero	Negative Infinite
	Positive Denormalized	Negative Infinite
	Positive Infinite	Positive Infinite
	NaN	NaN

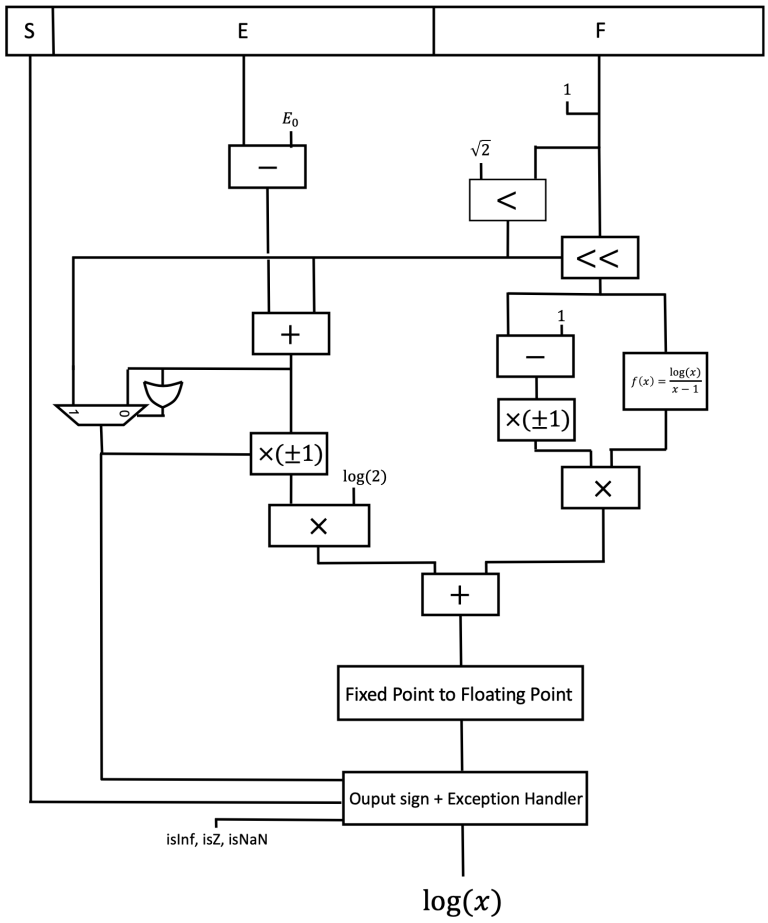

Figure 1.1: Block design of the implemented algorithm

Chapter 2

TestBench and Simulation

Before instantiating the module in lampFPU_top, a simulation was mandatory in order to check all possible errors and bugs.
It was decided to simulate the module on Vivado with an ad hoc testbench, so to fix in first approximation the main problems of the algorithm. To test the precision, a simulation with all of the acceptable inputs was executed (the full range from $00x000x00$ to $00xFF0x7F$, 32768 values), the results were dumped on a csv file and parsed by means of a MATLAB script.
In the following figures, an error histogram is plotted, and the average and percentage errors are computed. The denormal numbers are approximated as zeroes, so they produce a negative infinite at the output. This script takes into account all the possible special cases in input, i.e. SNan, QNan. The errors are more significant with respect to the simulations based on the DPI, because MATLAB is much more precise.

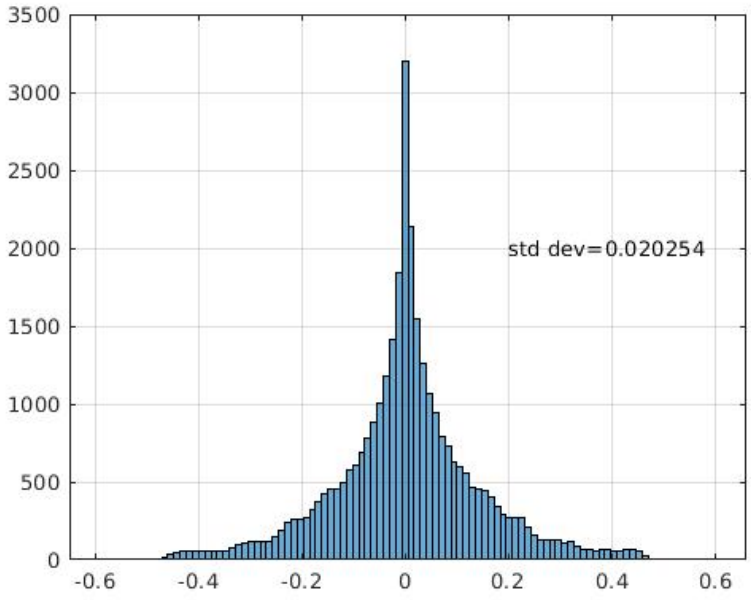

Figure 2.1: Histogram of the error.

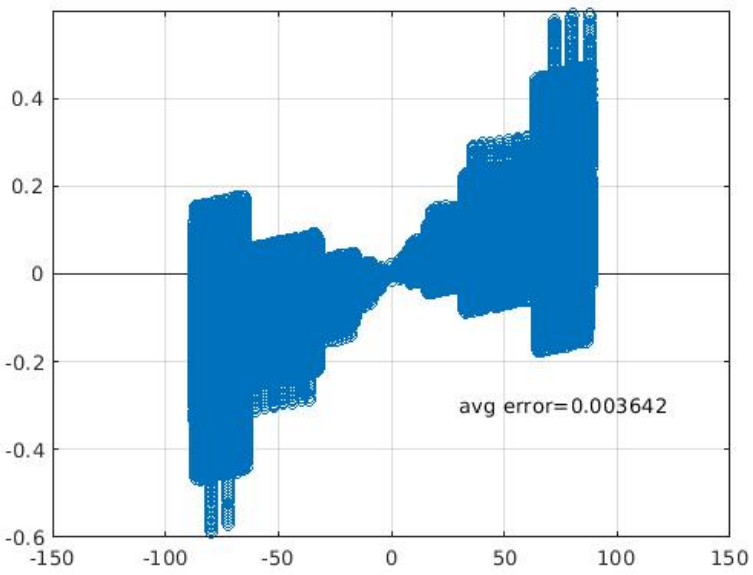

Figure 2.2: Committed error.

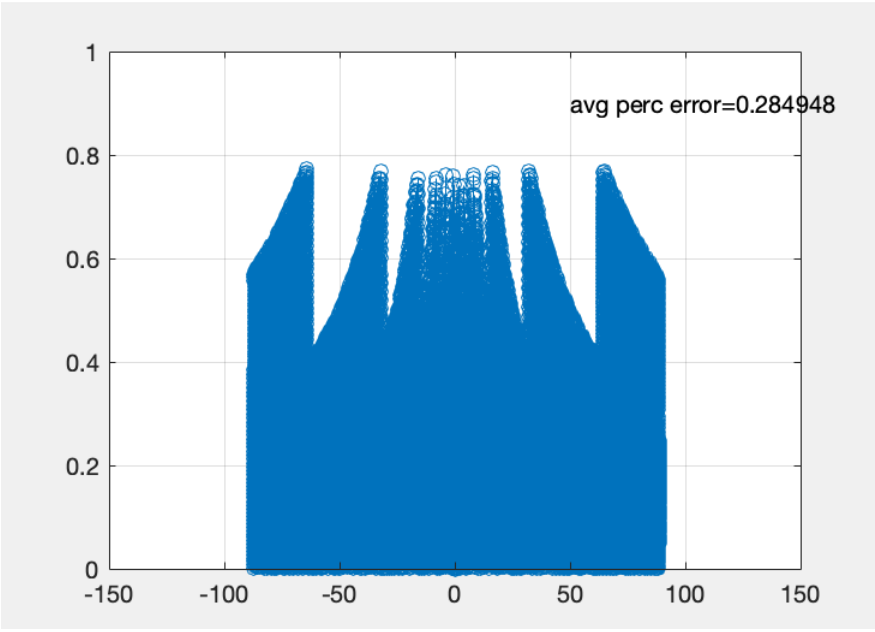

Figure 2.3: Percentage error.

Chapter 3

Integration

The aim of the project was to implement the natural logarithm module inside an already existing Floating Point Unit (FPU) provided by Andrea Galimberti and Davide Zoni [1]

The signals used in the module are:

INPUT:	COMMENT:
clk	clock signal
rst	reset signal
doLog_i	activates the module
s_op_i	sign of the input operand
extE_op1_i	extended exponent of the input operand
extF_op1_i	extended fractional of the input operand
isZ_op_i	flag: true if input is zero
isInf_op_i	flag: true if input is infinite
isSNAN_op_i	flag: true if input is SNaN
isQNAN_op_i	flag: true if input is QNaN
isDN_op_i	flag: true if input is denormal number
OUTPUT:	**COMMENT:**
s_res_o	sign of the output
e_res_o	exponent of the output
f_res_o	fractional of the output
valid_o	asserted to 1 when the result is ready
isOverflow_o	never 1
ifUnderflow_o	never 1
isToRound	1 if the output must be rounded

The integration part consisted in the connection of the submodule to the top module, and the adding of the new state into the Finite State Machine logic.
Also the Package was modified, with the addition of the folllowing functions:
LUT_log, FUNC_fix2float_log, FUNC_calcInfNanResLog
The first is a 7 bit look-up table used to calculate $\frac{log(X)}{X-1}$ [2];
The second is a function used to transform a fixed point number into a $BFloat_{16}$ SEF notation;
The last one is a function used to raise the correct output basing on the input flags.

[1] LAMP - BFloat16FPU
[2] See Chapter 1 for more details

3.1 Performances

The whole algorithm performs within 7 clock cycles while from the *doLog_i* assertion to the raise of *valid_o* register happens after just 4 clock cycles.

The algorithm had to be divided into a finite state machine with two states, because the multiplication operation between internal registers was too slow to perform within one clock cycle and so caused the presence of a negative slack.

	W\O LOG	**W\ LOG**
LUT	1065 (1.68%)	1265 (2%)
FF	376 (0.3%)	402 (0.32%)
DSP	2 (0.83%)	4 (1.67%)
IO	91 (43.33%)	91 (43.33%)
BUFG	1 (3.13%)	1 (3.13%)
WNS	0.448ns	0.4ns

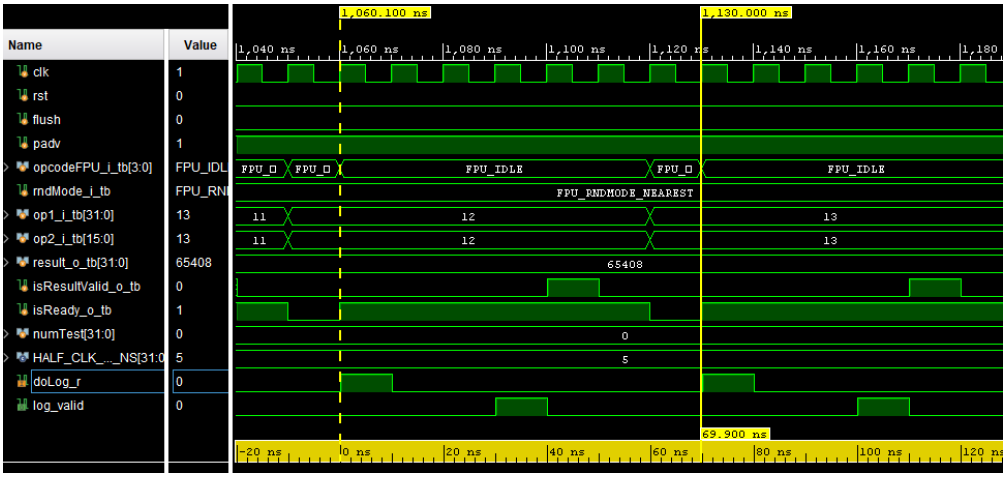

Figure 3.1: example waveforms of the Log module.

The simulation was done with the support of a Direct Programming Interface (DPI) that calculates the natural logarithm with the *math.h* C library performed on a 32bit float value, and returns a 32bit floating point value, that then is transformed to bfloat16 by truncation[3]. This translates into a discrepancy between some results calculated by the DPI and the ones calculated by the FPU-RTL module, with an error that is no bigger than 1LSB, due to the rounding to the next even performed on the FPU-RTL output.

[3]As the denormal numbers were treated as tending to zeroes, for these values the function returns a negative infinite value