Charotar University of Science and Technology (CHARUSAT)
Faculty of Technology and Engineering (FTE)

Subject: Computer Organization and Architecture (CEUC202)

Semester: 4th

Teaching Scheme:

Teaching Scheme	Theory	Practical	Tutorial	Total	Credit
Hours/Week	3	0	-	3	3
Marks	100	0	-	100	

Course Pre-requisites:

- Digital Electronics

Course Description:

This course offers a fundamental understanding of the concepts in Computer Organization and architecture. It provides students with an understanding of the design of fundamental blocks used for building a computer system and interfacing techniques of these blocks to achieve different configurations of an "entire computer system". The course emphasizes on computer design & parameter measurement, computer arithmetic used in commuting, cache memory configuration and optimization principles.

Course Objectives:

1. To provide introduction to Instruction Set Architecture and Practical exposure through simulation tools/Microprocessor Kits
2. To explore the basic concepts of computer organization & computer architecture design, Computer System Components: Processor, Memory, and Performance evaluation
3. To provide insight details in Processor Components: Control Unit, Registers, Caches Memory, ALU, and Instruction Execution Unit.

Course Outcomes:

By the end of the course, students will be able to:

1. **CO1**: Understand and Design of Arithmetic circuit, Logic circuit, Shift circuit and Control Unit circuit by using elements of digital logic.
2. **CO2**: Visualize and understand the working of CPU, different instruction formats, addressing modes, pipeline and vector processing.
3. **CO3**: Use various metrics to calculate and analyze clock periods, performance, and instruction throughput of single-cycle, multi-cycle, and pipelined implementations of a simple instruction set.
4. **CO4**: Understand and apply r's and r-1's complement in Addition, Subtraction and Multiplication of signed and unsigned numbers.
5. **CO5**: Show how cache design parameters affect the performance of program and Map a virtual address into a physical address.

Syllabus:

Unit No.	Unit/Topic Details		Hours (hr)	Evaluation Weightage (%)
1	**REGISTER TRANSFER AND MICROOPERATIONS BASIC COMPUTER ORGANIZATION AND DESIGN**		13	29
	1.1	Register Transfer Language		
	1.2	Register Transfer		
	1.3	Bus and Memory Transfers		
	1.4	Arithmetic, Logic and Shift Micro-Operations		
	1.5	Arithmetic Logic Shift Unit		
	1.6	Instruction Codes		
	1.7	Computer Registers, Computer Instructions		
	1.8	Timing and Control, Instruction Cycle		
	1.9	Memory Reference, Instructions, Input-Output and Interrupt		
	1.10	Complete Computer Description, Design of Basic Computer, Design of Accumulator Logic		
2	**CENTRAL PROCESSING UNIT & PIPELINE AND VECTOR PROCESSING**		12	26
	2.1	General Register Organization & Stack Organization,		
	2.2	Instruction Formats, Addressing Modes		
	2.3	Parallel Processing & Pipelining		
	2.4	Arithmetic Pipeline & Instruction Pipeline		
	2.5	RISC Pipeline		
3	**PERFORMANCE MEASURES**		04	09
	3.1	Performance and Cost, Purchasing perspective		
	3.2	Design perspective Notions of Performance: Latency and throughput, Performance and time, computer clocks, Computing CPU time and cycles, Improving Performance		
	3.3	Linking instruction, cycles and time, CIPS and MIPS examples, Computer Benchmarks, Sources of Benchmark: SPEC 89 and SPEC 95		
	3.4	Amdahl's law, Estimating performance improvements, poor performance metrics		
4	**COMPUTER ARITHMETIC**		08	18
	4.1	Introduction: Binary, Octal, Decimal, Hexadecimal representation		
	4.2	Integer Numbers: Sign-Magnitude,1's complement,2's complement		
	4.3	Addition, Subtraction & Multiplication Algorithm		
5	**MEMORY ORGANIZATION**		08	18
	5.1	Memory construction, size, speed, cost and data unit, Tradeoffs between them		
	5.2	PROM, EEPROM, DRAM, SRAM, Memory Technologies, Hierarchical organization		
	5.3	Principle of locality, Simple Cache organization, Miss rate, block size, cache policies		

	5.4	Cache Organization: Mapping alternatives- direct, associative and set associative, processor performance with cache, memory organization and miss penalty		
	5.5	Policies for read, load, fetch, replacement and write, How Caches work, Size of tags, Performance analysis examples		
			Total Hours:	**45**

Course Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	3	2	1	-	-	-	-	-	-	-	-
CO2	3	3	3	3	2	1	-	-	-	-	-	-	-	-
CO3	3	3	3	3	3	1	-	-	-	-	-	-	-	-
CO4	3	2	2	3	2	1	-	-	-	-	-	-	-	-
CO5	3	3	3	3	3	1	-	-	-	-	-	-	-	-

Enter correlation levels 1, 2 or 3 as defined below:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High), If there is no correlation, put "-"

Recommended Study Material:

- **Text books:**

1. "Computer System Architecture", by Morris Mano, 3rd Edition, Prentice Hall.
2. John L. Hennesy & David A. Patterson, "Computer Organization and Design MIPS Edition: The Hardware/Software Interface", (The Morgan Kaufmann Series in Computer Architecture and Design).

- **Reference Books:**

1. "Structured Computer Organization", A. S. Tananbum, Pearson Education.
2. "Computer Organization & Architecture-Designing for Performance", William Stalling, Pearson Prentice Hall, 8th Edition.
3. "The Essentials of Computer Organization and Architecture", by Linda Null, Julia Lobur.
4. "Computer Architecture & Organization", by John P Hayes, McGraw-Hill.
5. "Computer Architecture: Pipelined and Parallel Processor Design", by Michael J. Flynn, 4th Edition.

Online courses:

- High Performance Computer Architecture, Prof. Ajit Pal, IIT Kharagpur, https://nptel.ac.in/courses/106105033/ (For cache memory and Pipelining).

Web Material:

1. http://pages.cs.wisc.edu/~markhill/cs354/Fall2008/notes/flpt.apprec.html
2. https://www.youtube.com/watch?v=qlH4-oHnBb8
3. https://www.ebookbou.edu.bd/Books/Text/SST/DCSA/dcsa_2301/Unit-08.pdf
4. https://www.youtube.com/playlist?list=PLxCzCOWd7aiHMonh3G6QNKq53C6oNXGr X