

# RISC-V SiMPLE

Projeto e Desenvolvimento de processadores RISC-V com a *ISA RV32IMF* usando as microarquiteturas *Uniciclo*, *Multiciclo* e *Pipeline* em *FPGA*

Arthur Matos

Universidade de Brasília - UnB

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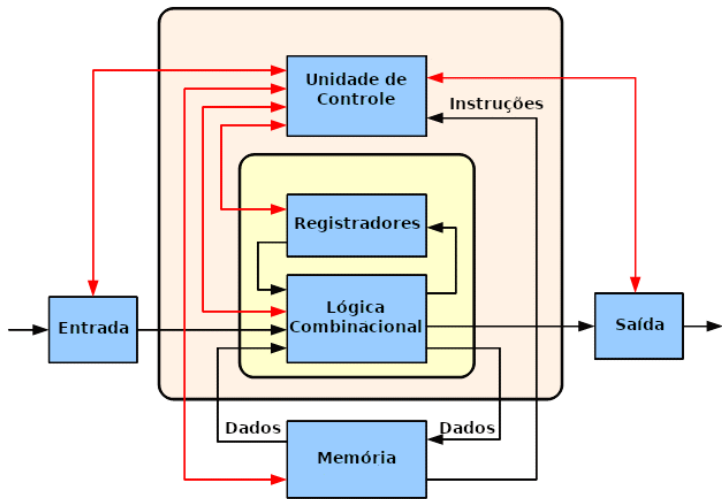
# Motivação e Objetivos

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## Revisão Teórica

# Arquitetura de computadores

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# RISC vs CISC

Fazer essa parte?

# ISA RISC-V





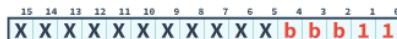
Falar sobre módulo 132/64/128 e E

# Extensões da arquitetura

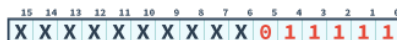
# Codificação do tamanho da instrução



16 bits ( $aa \neq 11$ )



32 bits ( $bbb \neq 111$ )



48 bits



64 bits

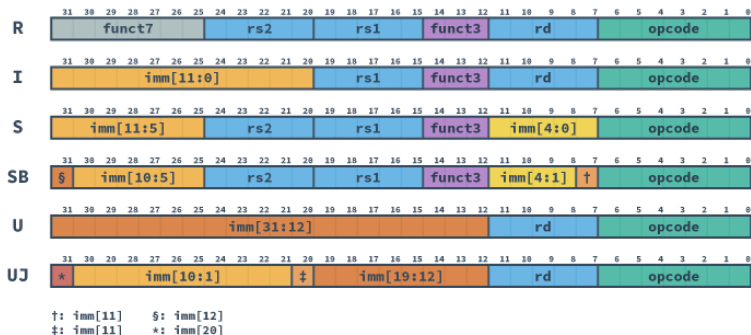


$80+16*nnn$  bits ( $nnn \neq 111$ )



Reserved for  $\geq 192$  bits

# Instruções de 32 bits



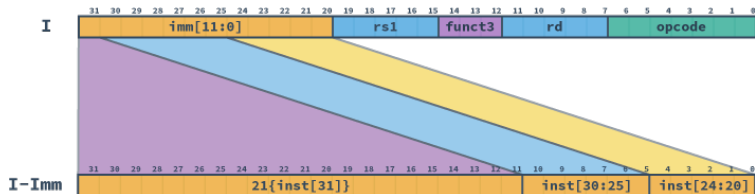
```
.text
```

```
...
```

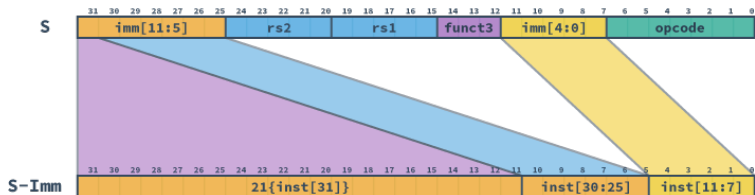
```
addi    t0, zero, 404
```

```
...
```

# Formação dos imediatos em instruções tipo I

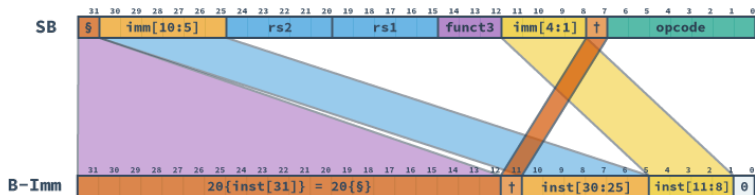


# Formação dos imediatos em instruções tipo S

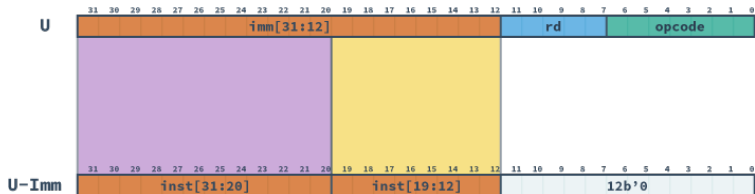




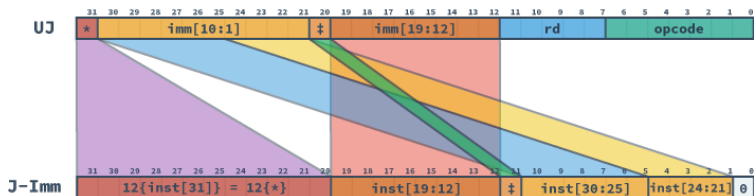
# Formação dos imediatos em instruções tipo B



# Formação dos imediatos em instruções tipo U



# Formação dos imediatos em instruções tipo J



# Programando para a *ISA RISC-V*

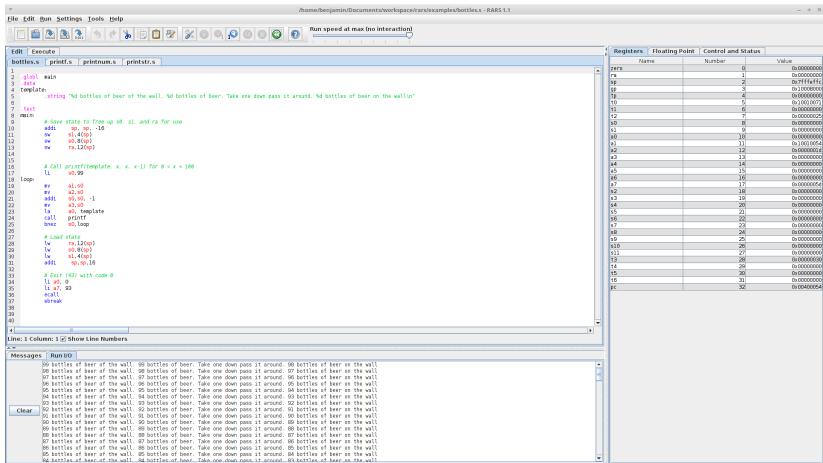
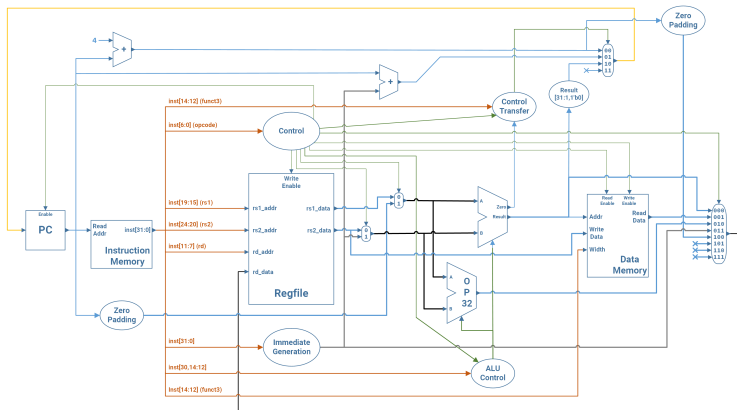


Figura: IDE RARS

# Organização de computadores

# Organização de computadores



# Alguns conceitos de microarquiteturas

- Uniciclo
- Multiciclo
- *Pipeline*
- Superescalar
- *Out-of-Order Execution*

## Representação de *hardware*



# Representação de *hardware*

- Programação visual
- Linguagens de descrição de *hardware* (*HDL*)
  - *Verilog*
  - *VHDL*
- Síntese de alto nível (*HLS*)
  - *C++*
  - *Matlab*

## Síntese de *hardware*

# Sintetizando projetos em *HDL*

The screenshot displays the Quartus Prime IDE interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The Project Navigator on the left shows the project hierarchy with 'Cyclone V: SC5EMAS31C6' and 'fpga\_top'. The main window is titled 'Compilation Report - fpga\_top' and shows the 'Flow Summary' tab. The 'Table of Contents' on the left lists various flow steps, with 'Flow Summary' selected. The 'Flow Summary' table provides a detailed overview of the compilation process, including the flow status, version, and various resource utilization metrics.

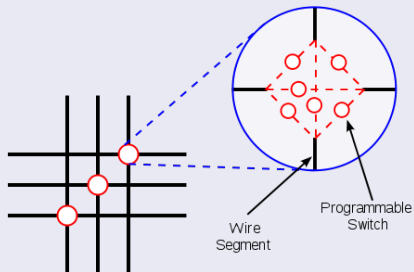
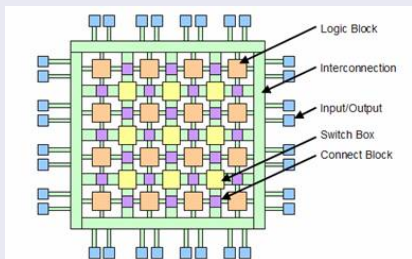
Flow Summary	
Flow Status	Successful - Mon May 17 18:37:36 2021
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	fpga_top
Top-level Entity Name	fpga_top
Family	Cyclone V
Device	SC5EMAS31C6
Timing Mode	Final
Logic utilization (in ALM)	8,790 / 32,070 (30 %)
Total registers	6508
Total pins	103 / 457 (23 %)
Total virtual pins	0
Total block memory bits	2,853,408 / 4,065,280 (70 %)
Total DSP Blocks	18 / 87 (21 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	1 / 6 (17 %)
Total DLLs	0 / 4 (0 %)

The bottom of the window shows a 'Messages' pane with a 'System' tab and a 'Processing' tab. The status bar at the bottom right indicates 0% completion and a time of 00:00:00.

# *FPGAs*

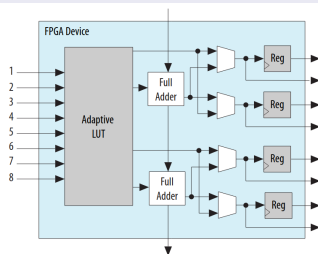
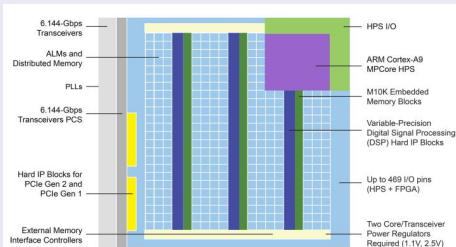
# Field Programmable Logic Arrays

## Arquitetura genérica de uma *FPGA*



# FPGA Altera Cyclone V

## Arquitetura da FPGA Altera Cyclone V



## Estado da Arte

# O Estado da Arte da *ISA RISC-V*



## Sistema Proposto

# Organização do projeto







