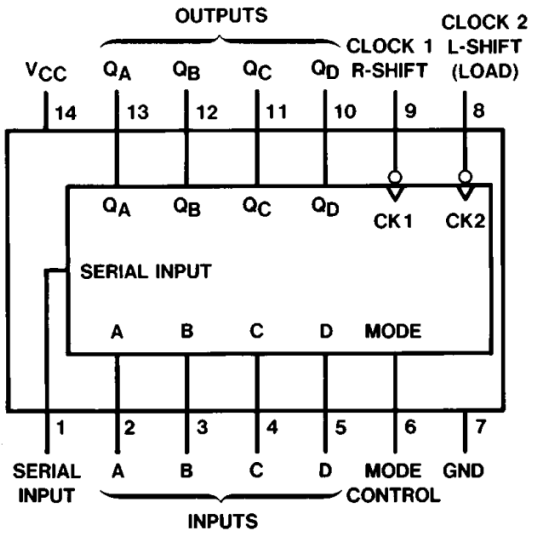
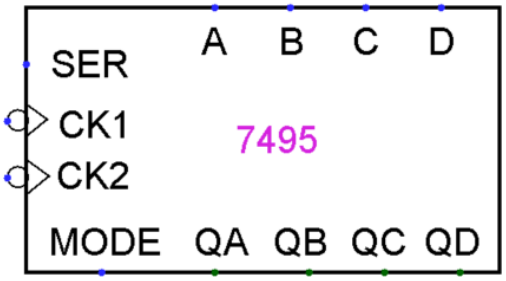
7495

4-BIT PARALLEL ACCESS SHIFT REGISTER

Connection Diagram



Symbol



- The 7495 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial Input and four Parallel Data inputs (A–C) and four Parallel Data outputs (Q_A–Q_D). The serial or parallel mode of operation is controlled by a Mode Control input (MODE) and two Clock Inputs (CK_1) and (CK_2). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input
- When the Mode Control input (MODE) is HIGH, CK_2 is enabled. A HIGH to LOW transition on enabled CK_2 transfers parallel data from the A–D inputs to the Q_A–Q_D outputs.
- When the Mode Control input (MODE) is LOW, CK_1 is enabled. A HIGH to LOW transition on enabled CK_1 transfers the data from Serial Input to Q_A and shifts the data in Q_A to Q_B, Q_B to Q_C, and Q_C to Q_D respectively (right-shift). A left-shift is accomplished by externally connecting Q_D to C, Q_C to B, and Q_B to A, and operating in the parallel mode (MODE=HIGH).
- For normal operation, MODE should only change states when both Clock inputs are LOW.

Truth Table

MODE	CK_1	CK_2	SER	Q_A^{t+1}	Q_B^{t+1}	Q_C^{t+1}	Q_D^{t+1}
L	↓	X	L	L	Q_A^t	Q_B^t	Q_C^t
L	↓	X	H	H	Q_A^t	Q_B^t	Q_C^t
H	X	↓	X	A	B	C	D

L – low value
H – high value
X – don't care
↓ – falling edge