

54LS160A/DM74LS160A, 54LS162A/DM74LS162A Synchronous Presettable BCD Decade Counters

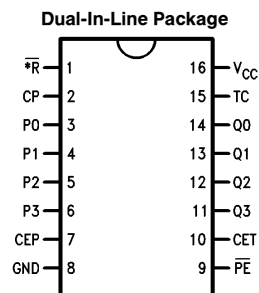
General Description

The 'LS160 and 'LS162 are high speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'LS160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'LS162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

Features

- Synchronous counting and loading
- High speed synchronous expansion
- Typical count rate of 35 MHz
- Fully edge triggered

Connection Diagram

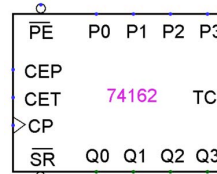


*MR for 'LS160 TL/F/10177-1
*SR for 'LS162

**Order Number 54LS160ADMB, 54LS160AFMB, 54LS160ALMB,
54LS162ADMB, 54LS162AFMB, 54LS162ALMB, DM74LS160AM,
DM74LS162AM or DM74LS162AN**

See NS Package Number E20A, J16A, M16A, N16E or W16A

Symbol



Truth Table

\overline{SR}	\overline{PE}	CET	CEP	CP	$Q_{3:0}^{t+1}$
0	X	X	X	\uparrow	$(0000)_2$
1	0	X	X	\uparrow	$(P_3P_2P_1P_0)_2$
1	1	1	1	\uparrow	$(Q_{3:0}^t + 1) \bmod 10$
1	1	0	X	X	$Q_{3:0}^t$
1	1	X	0	X	$Q_{3:0}^t$

$$TC = Q_3 \cdot \overline{Q_2} \cdot \overline{Q_1} \cdot Q_0 \cdot CET$$

$$\text{Count Enable} = CEP \cdot CET \cdot \overline{PE}$$

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
MR ('160)	Asynchronous Master Reset Input (Active LOW)
SR ('162)	Synchronous Reset Input (Active LOW)
P0-P3	Parallel Data Inputs
PE	Parallel Enable Input (Active LOW)
Q0-Q3	Flip-Flop Outputs
TC	Terminal Count Output

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS160A/162A			DM74LS160A/162A			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			−0.4			−0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	−55		125	0		70	°C
t _s (H) t _s (L)	Setup Time, HIGH or LOW P _n to CP	20 20			20 20			ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW P _n to CP	0.0 0.0			0.0 0.0			ns
t _s (H) t _s (L)	Setup Time, HIGH or LOW PE to CP	20 20			20 20			ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW PE to CP	0 0			0 0			ns
t _s (H) t _s (L)	Setup Time, HIGH or LOW CEP, CET or SR to CP	20 20			20 20			ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW CEP, CET or SR to CP	0 0			0 0			ns
t _w (H) t _w (L)	CP Pulse Width, HIGH or LOW	15 25			15 25			ns
t _w (L)	MR Pulse Width LOW (‘160)	15			15			ns
t _{rec}	Recovery Time MR to CP (‘160)	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)



Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −18 mA			−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	54LS 2.5 DM74 2.7			V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min	54LS DM74		0.4 0.5	V
		I _{OL} = 4 mA, V _{CC} = Min	DM74		0.4	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 7\text{V}$	Other			0.1	mA
		\overline{PE} , CET Inputs				0.2	
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7\text{V}$	Other			20	μA
		\overline{PE} , CET Inputs				40	
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4\text{V}$ Inputs	54LS			−0.4	mA
			DM74			−1.6	
		\overline{PE} , CET Inputs				−0.8	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs HIGH	$V_{CC} = \text{Max}, \overline{PE} = \text{GND}$ CP =  , Other Inputs = 4.5V				31	mA
I_{CCL}	Supply Current with Outputs LOW	$V_{CC} = \text{Max}, V_{IN} = \text{GND}$ CP = 				31	mA

Switching Characteristics $V_{CC} = +5.0\text{V}, T_A = +25^\circ\text{C}$

Symbol	Parameter	$R_L = 2\text{ k}\Omega$ $C_L = 15\text{ pF}$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	25		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to TC		25 21	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		24 27	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC		14 23	ns
t_{PHL}	Propagation Delay \overline{MR} to Q_n ('160)		28	ns

Functional Description

The 'LS160 and 'LS162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The '161 and '163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'LS160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('LS160), synchronous reset ('LS162), parallel load, count-up and hold. Five control inputs—Master Reset (\overline{MR} , 'LS160), Synchronous Reset (\overline{SR} , 'LS162), Parallel Enable (\overline{PE}), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the

Mode Select Table. A LOW signal on \overline{MR} overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on \overline{SR} overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on \overline{PE} overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With \overline{PE} and \overline{MR} ('LS160) or \overline{SR} ('LS162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'LS160A and 'LS162A use D-type edge-triggered flip-flops and changing the \overline{SR} , \overline{PE} , CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Functional Description (Continued)


The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in the 9310 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the decade counters of the 'LS160, 'LS162, the TC output is fully decoded and can only be HIGH in state 9.

LOGIC EQUATIONS:

Count Enable = $\text{CEP} \cdot \text{CET} \cdot \text{PE}$

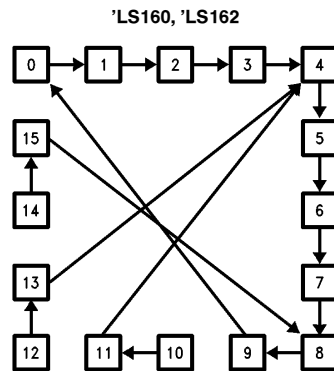
$\text{TC} = \text{Q}_0 \cdot \overline{\text{Q}}_1 \cdot \overline{\text{Q}}_2 \cdot \text{Q}_3 \cdot \text{CET}$

Mode Select Table

$\overline{\text{SR}}$	$\overline{\text{PE}}$	CET	CEP	Action on the Rising Clock Edge ()
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($\text{P}_n \rightarrow \text{Q}_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the 'LS162
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

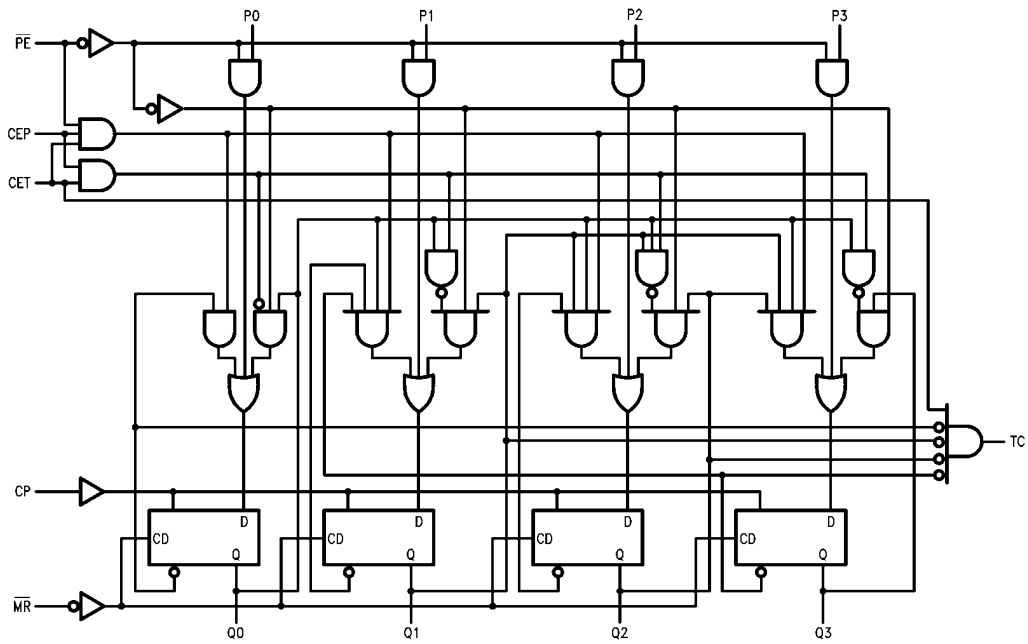
State Diagrams



TL/F/10177-5

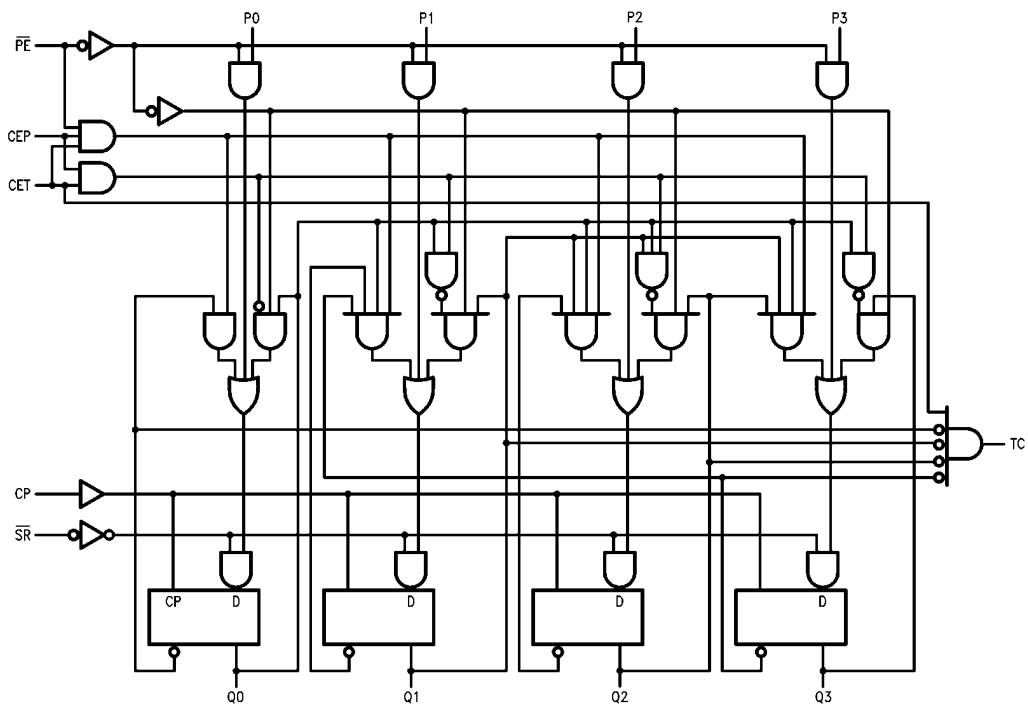
Logic Diagrams

'LS160



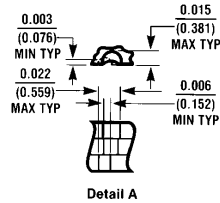
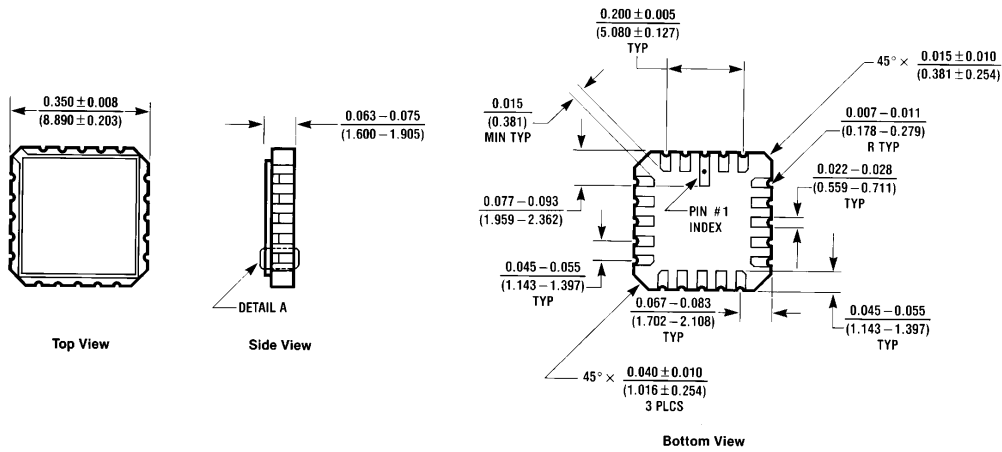
TL/F/10177-3

'LS162



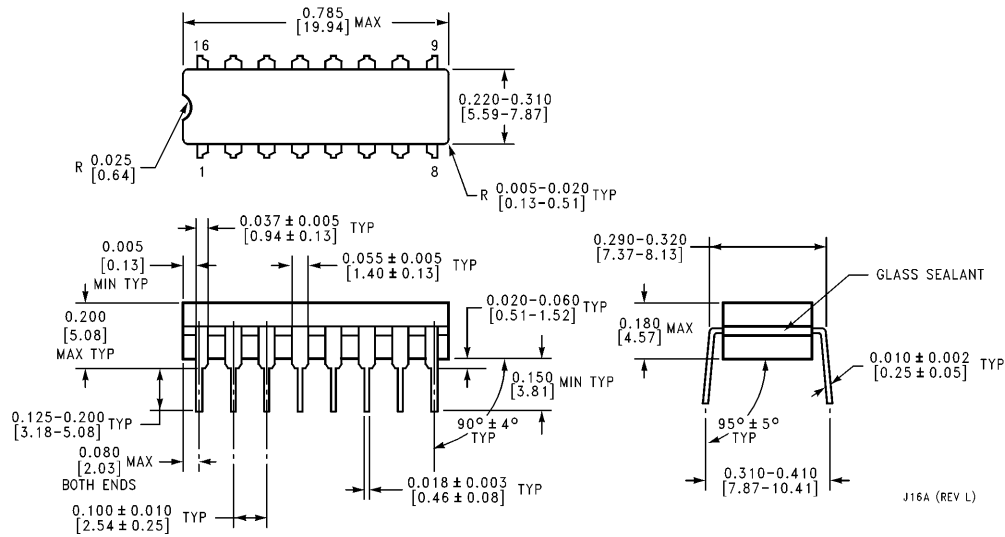
TL/F/10177-4

Physical Dimensions inches (millimeters)



E20A (REV D)

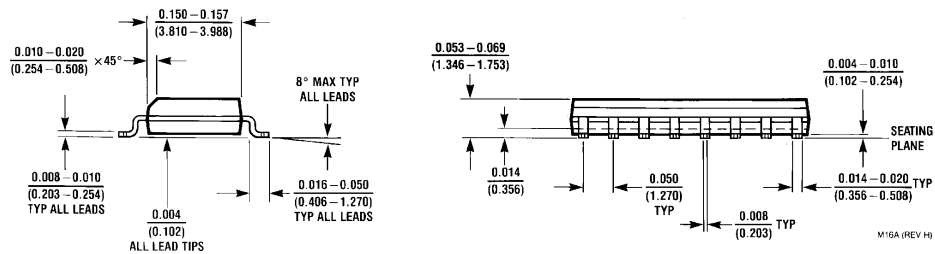
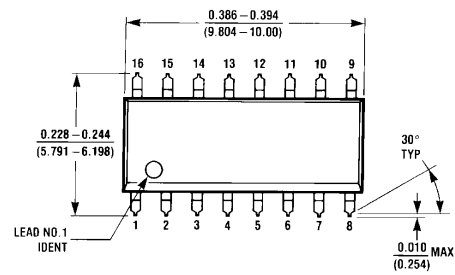
Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS160ALMQB or 54LS162ALMQB
NS Package Number E20A



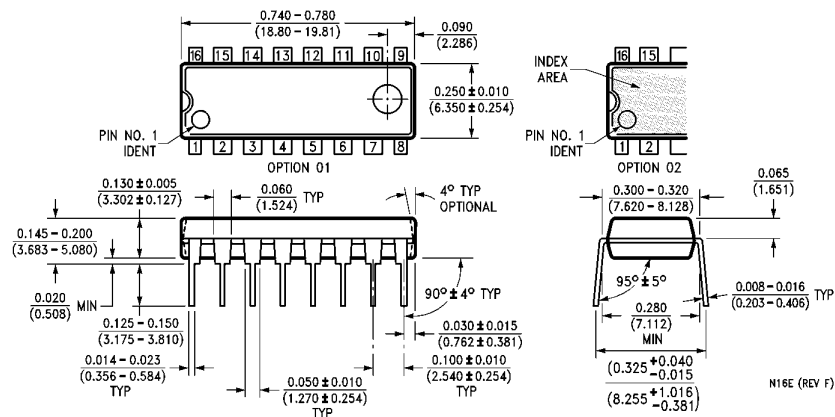
J16A (REV L)

Ceramic Dual-In-Line Package (J)
Order Number 54LS160ADMQB or 54LS162ADMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



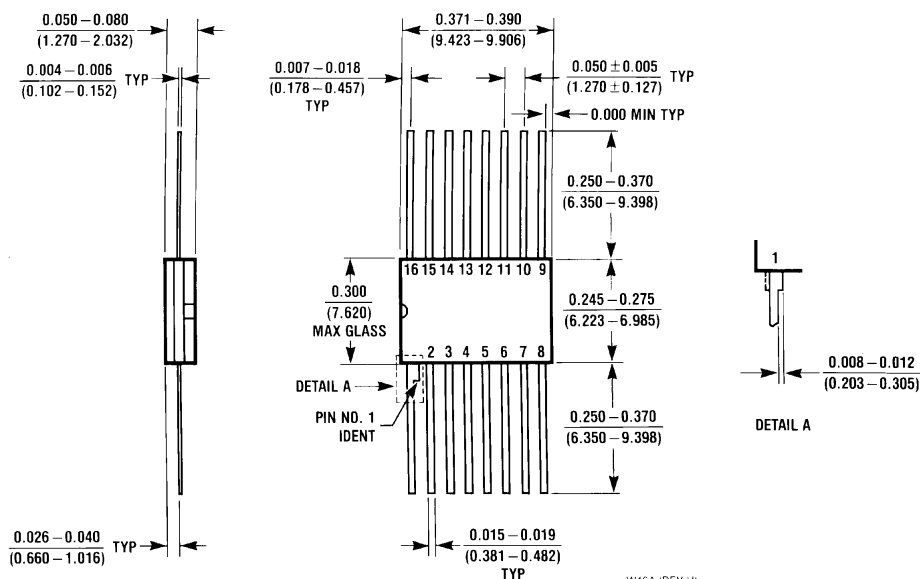
16-Lead Small Outline Molded Package (M)
Order Number DM74LS160AM DM74LS162AM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS160AN or DM74LS162AN
NS Package Number N16E

54LS160A/DM74LS160A, 54LS162A/DM74LS162A Synchronous Presettable BCD Decade Counters

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS160AFMQB or 54LS162AFMQB
NS Package Number W16A

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