



Dual P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)			
- 30	$0.025 \text{ at V}_{GS} = -10 \text{ V}$	- 7.1			
- 30	0.041 at V _{GS} = - 4.5 V	- 5.5			

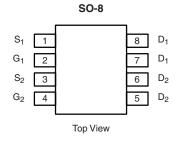
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Compliant to RoHS Directive 2002/95/EC

Pb-free RoHS COMPLIANT HALOGEN FREE

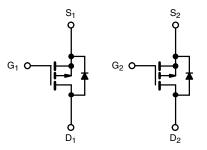
APPLICATIONS

- Load Switches
 - Notebook PCs
 - Desktop PCs
 - Game Stations



Ordering Information: Si4925BDY-T1-E3 (Lead (Pb)-free)

Si4925BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	- 30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Dusin Comment /T 150 90\8	T _A = 25 °C	I _D	- 7.1	- 5.3	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		- 5.7	- 4.3	
Pulsed Drain Current		I _{DM}	- 40		Α
Continuous Source Current (Diode Conduction) ^a		I _S	- 1.7	- 0.9	
M	T _A = 25 °C	P _D	2.0	1.1	W
Maximum Power Dissipation ^a	T _A = 70 °C] 'D	1.3	0.7] **
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Marrian Innation to Ambient	t ≤ 10 s	R _{thJA}	50	62.5	
Maximum Junction-to-Ambient ^a	Steady State	¹ ¹thJA	85	110	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	30	40]

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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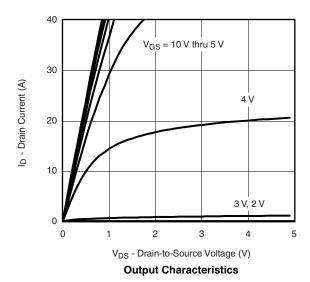
SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1		- 3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	1	V _{DS} = - 30 V, V _{GS} = 0 V			- 1	μΑ	
	IDSS	V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 55 °C			- 25		
On-State Drain Current ^a	I _{D(on)}	V _{DS} = - 5 V, V _{GS} = - 10 V	- 40			Α	
	D	V _{GS} = - 10 V, I _D = - 7.1 A		0.020	0.025	Ω	
Drain-Source On-State Resistance ^a	nDS(on)	$N_{DS(on)}$ $V_{GS} = -4.5 \text{ V}, I_D = -5.5 \text{ A}$		0.033	0.041		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 7.1 A		20		S	
Diode Forward Voltage ^a	V_{SD}	I _S = - 1.7 A, V _{GS} = 0 V		- 0.8	- 1.2	V	
Dynamic ^b							
Total Gate Charge	Q_g			33	50		
Gate-Source Charge	Q _{gs}	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -7.1 \text{ A}$		5.4		nC	
Gate-Drain Charge	Q _{gd}			8.9		1	
Turn-On Delay Time	t _{d(on)}			9	15		
Rise Time	t _r	V_{DD} = - 15 V, R_L = 15 Ω		12	20		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 1 A, $V_{GEN} =$ - 10 V, $R_g =$ 6 Ω		60	90	ns	
Fall Time	t _f			34	50		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 1.7 A, dI/dt = 100 A/μs		30	60		

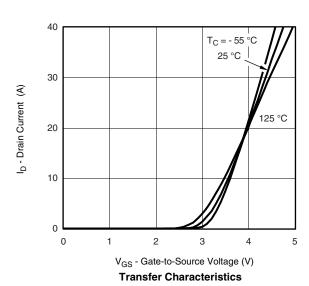
Notes:

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

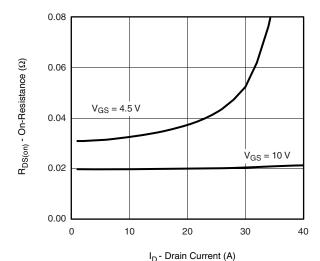




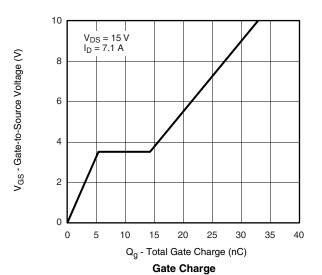


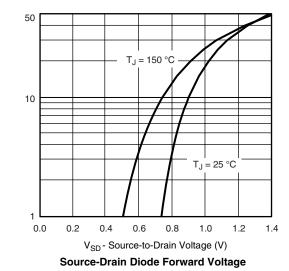


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



On-Resistance vs. Drain Current

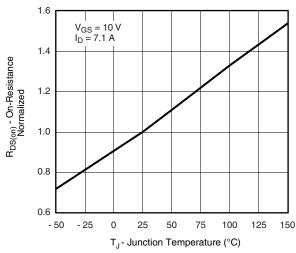




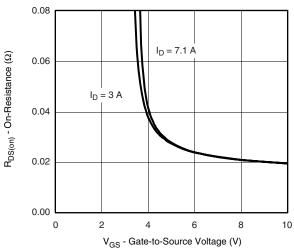
2500 2000 C_{iss} C - Capacitance (pF) 1500 1000 Coss 500 $\mathsf{C}_{\mathsf{rss}}$ 0 0 6 12 18 24 30

V_{DS} - Drain-to-Source Voltage (V)





On-Resistance vs. Junction Temperature

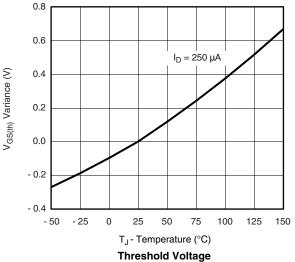


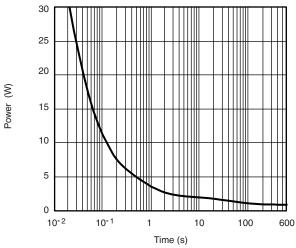
On-Resistance vs. Gate-to-Source Voltage

I_S - Source Current (A)

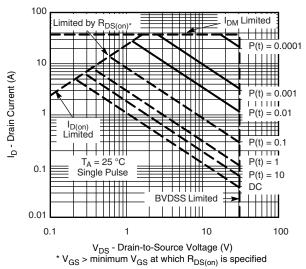
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

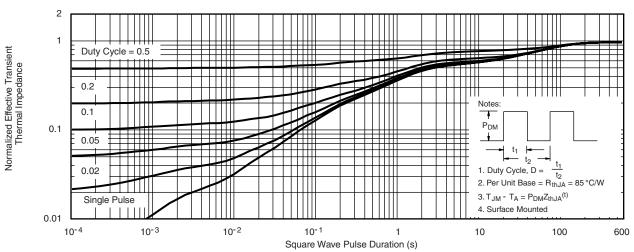




Single Pulse Power



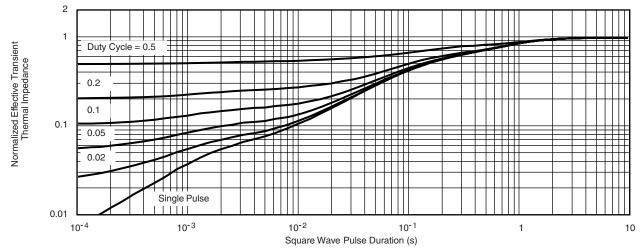
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72001.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	INCHES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

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