Lab 11: Programmable Logic Arrays

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CSE 2301: Principles and Practice of Digital Logic Design
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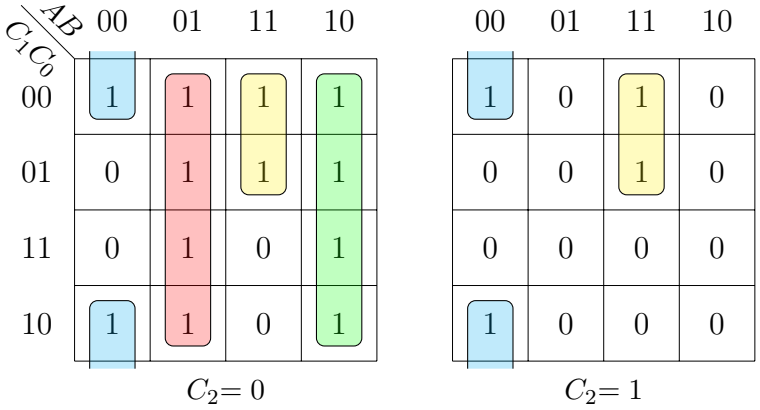
Coded in LaTeX

Theory

Karnaugh-Map Review

F Output



$$F = \overline{C_0}\,\overline{A}\,\overline{B} + \overline{C_1}AB + \overline{C_2}\,\overline{A}B + \overline{C_2}A\overline{B}$$

A	B	C	D	E	F	G	H	I	Error Position
0	0	0	0	0	0	0	0	0	None (No Error)
1	0	0	0	0	0	1	0	1	Parity Bit 5
1	1	0	0	0	0	1	0	0	Data Bit 4
1	0	1	0	0	0	0	1	1	Data Bit 3
1	0	0	1	0	0	0	1	0	Data Bit 2
1	0	0	0	1	0	0	0	1	Data Bit 1
0	1	0	0	0	1	0	0	1	Parity Bit 9
0	1	1	0	0	1	0	0	0	Data Bit 8
0	1	0	1	0	0	1	1	1	Data Bit 7
0	1	0	0	1	0	1	1	0	Data Bit 6
0	0	1	0	0	1	1	0	0	Parity Bit 12
0	0	1	1	0	1	0	1	1	Data Bit 11
0	0	1	0	1	1	0	1	0	Data Bit 10
0	0	0	1	0	1	1	1	0	Parity Bit 14
0	0	0	1	1	1	1	0	1	Data Bit 13
0	0	0	0	1	1	1	1	1	Parity Bit 15

Table 1: Truth Table for Error Detection (5 Inputs, 4 Outputs)