Lab 03: I/O and POSTNET

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Coded in LaTeX

Theory

The 7405 Chip DIP

The **7405 DIP** *(Dual-Inline-Package)* from Texas Instruments is a different kind of inverter called an *Open Collector*, compared to the **7404 DIP** by the same manufacturer which is a standard inverter with something called a *Push-Pull Output Stage.* Our application requires driving a load, in this case some Light Emitting Diodes. These LEDs require higher current draw which a **7404** IC cannot handle directly. The **7405** provides the ability to drive an external load by pulling the output signal to ground without having to supply or drive the current from the IC itself.

The Bipolar Junction Transistor

In order to properly explain this choice, the *emitter, base,* and *collector* of a Bipolar Junction Transistor must be properly defined.

Example 1 ***The Bipolar Junction Transistor Abstraction***
Emitter A *heavily* doped, medium-sized layer designated to inject or emit electrons.
Base A thin layer of *medium* doped material designed for electron transmission.
Collector A wide layer of *lightly* doped material designed to *collect* electrons.
Texas Instruments utilizes NPN Transistors in their schematics such as this:

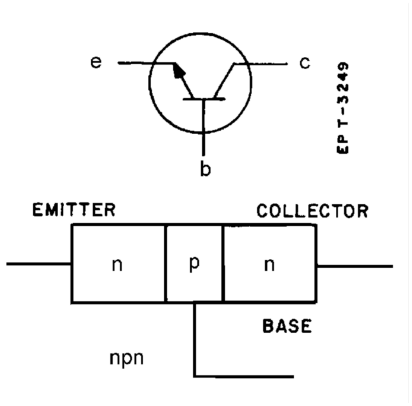


Figure 1: The NPN Transistor

Why the 7405?

All of this hand waving still doesn't answer the question as the difference hasn't been hammered home quite yet.

Example 2 shows the schematics from the official Texas Instrument's Datasheets and walks through the operation. When focusing on the output Y, the difference between the circuits is clear. The 7405 chip's output BJT's collector terminal is left unconnected within

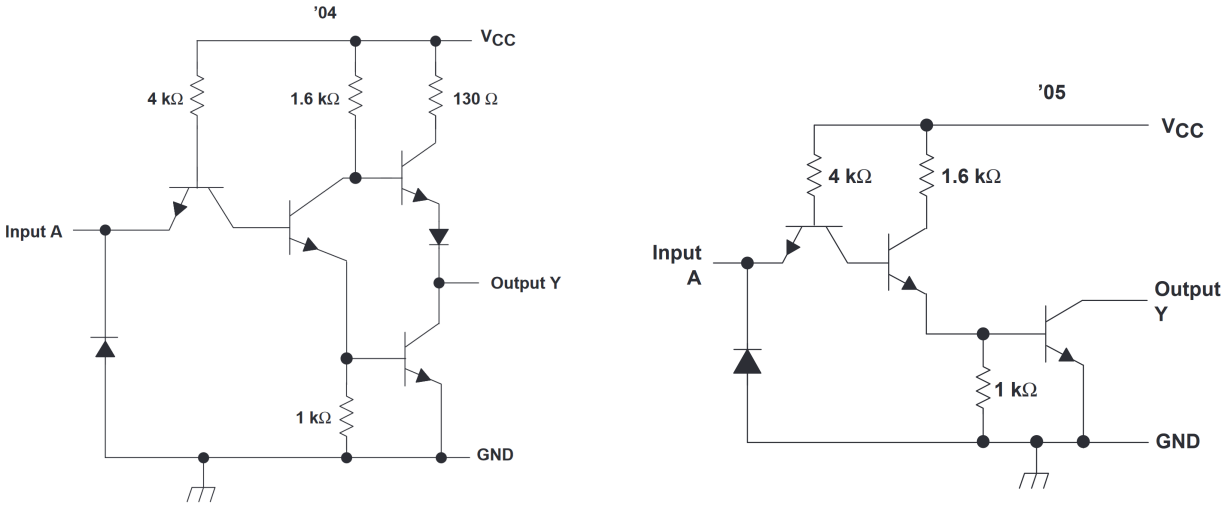
the chip. This is also known as an "open." This architecture allows the chip to be independent of the downstream current draw.

This makes it suitable for applications where a resistive load such as a motor, or in this case, an LED is connected to the output of the inverter. This does require some planning as the load requires a external pullup resistor in order to achieve a HIGH output.

There are three possible different configurations of a BJT circuit, a common emitter, common base, or a *common collector circuit* where "Common" references which two leads of the BJT are both part of the input and outputs circuits.

For the 7405, a positive-going input signal drives the base more positive with respect to the emitter, which causes the base current to increase. This results in more emitter current, causing a more positive output voltage at the emitter to drive our LED.

Example 2 ***Operation of the 7405***



(a) The Standard 7404

(b) The Standard 7405

Figure 2: Schematic View

When the input signal is high:

- *The base of the first NPN transistor is forward biased relative to its emitter, allowing base current to flow. This results in current flowing from the collector to the emitter, effectively grounding the output.*
- *The base current enables a larger current flow from the collector to the emitter, pulling the output low (close to ground).*
- *In this state, the transistor is "on," and the output is a logic LOW signal (approximately 0.0V to 0.8V in TTL logic).*

When the input signal is low:

- *The base of the first NPN transistor is not forward biased, so no current flows through the base-emitter junction. As a result, the collector-emitter path remains open, and the transistor is turned off.*
- *Since the transistor is off, the output floats and is pulled high by the external pull-up resistor, resulting in a logic HIGH output close to V_{CC}.*

In the 7405 open-collector configuration, the NPN transistor plays a crucial role in determining the output state based on the input signal.

As with any NPN transistor, the emitter, base, and collector function to control the current flow between the collector and emitter through the base current.

In this circuit, the NPN transistor's collector is left unconnected internally (hence the term "open collector"). The external load, such as an LED or a resistive element, is connected between the output (collector) and a pull-up resistor, which is tied to the supply voltage

In essence, the NPN transistor in the 7405 circuit acts as a switch that controls the flow of current to the output based on the base current. When there is base current, the transistor conducts, and the output is pulled low. When there is no base current, the transistor is off, and the output is pulled high by the external resistor.

This open-collector design is particularly useful for applications that require the driving of higher-current loads, such as LEDs, without requiring the IC itself to supply the current. Instead, the external load provides the necessary current, allowing the circuit to handle higher loads more efficiently.

To summarize, in plain non-electrical engineering speak, if the transistor is ON, current flows through the path of least resistance and robs the output (our LED) of its current, making the light go dim. If the transistor is OFF, the pullup resistor now makes the path of least resistance between the LED and ground and the LED illuminates.

Current Draw of Each LED

The current through each LED is calculated using Ohm's Law:

Example 3

$$I = \frac{V_R}{R} = \frac{V_{supply} - V_{LED}}{R}$$

Where:

- $V_{supply} = 5V$ *is the supply voltage.*
- V_{LED} *is the forward voltage of the LED. This is measured at* $1.786V$ *by my multimeter.*
- $R = 330\,\Omega$ *is the resistor value.*

$$I_{red} = \frac{5V - 1.786V}{330\,\Omega} = \frac{3.214V}{330\,\Omega} = 9.74\,mA$$

Deliverables

POSTNET to XS_3 Encoding

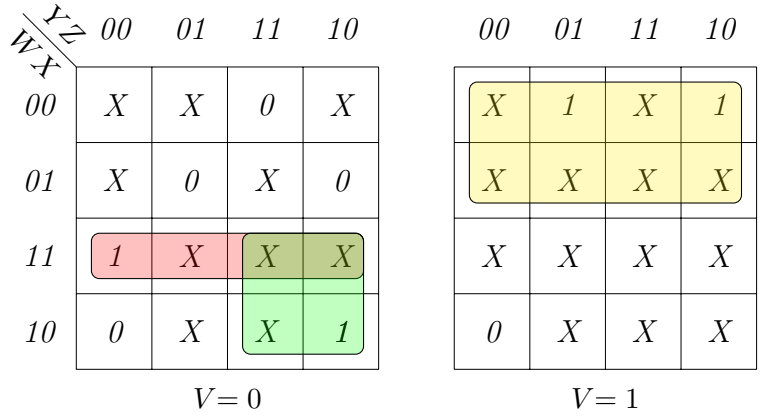
Decimal	V	W	X	Y	Z	D	C	B	A
0	1	1	0	0	0	0	0	1	1
1	0	0	0	1	1	0	1	0	0
2	0	0	1	0	1	0	1	0	1
3	0	0	1	1	0	0	1	1	0
4	0	1	0	0	1	0	1	1	1
5	0	1	0	1	0	1	0	0	0
6	0	1	1	0	0	1	0	0	1
7	1	0	0	0	1	1	0	1	0
8	1	0	0	1	0	1	0	1	1
9	1	0	1	0	0	1	1	0	0

Table 1: POSTNET to XS3 Conversion Table

From here, each output signal D, C, B, A is isolated into its own, separate equation, signifying the combination of inputs necessary to eventually output a 4-bit XS_3 encoded output.

Example 4 ***D Output***

The map is divided into two layers for $V = 0$ and $V = 1$. Pay Attention to V.



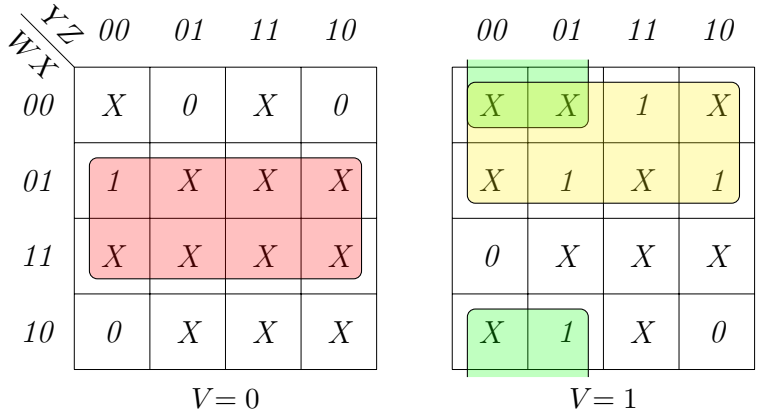
This produces:

$$D = \overline{V}(WX + WY) + V(\overline{W})$$

$$D = \overline{V}WX + \overline{V}WY + V\overline{W} \quad \textit{(Distribution)}$$

$$D = WX + WY + V\overline{W} \quad \textit{(Absorption)}$$

Example 5 ***C Output***

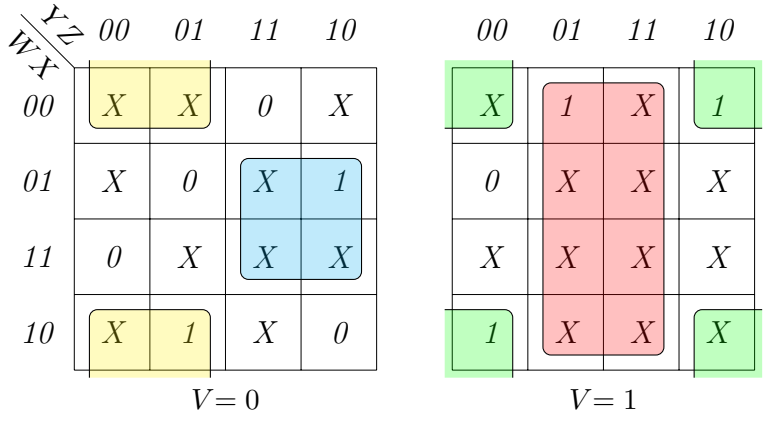


This produces:

$$C = \overline{V}(\overline{W} + \overline{X}Y) + V(X)$$

$$C = \overline{V}\overline{W} + \overline{V}\overline{X}Y + VX \quad \textit{(Distribution)}$$

Example 6 ***B Output***



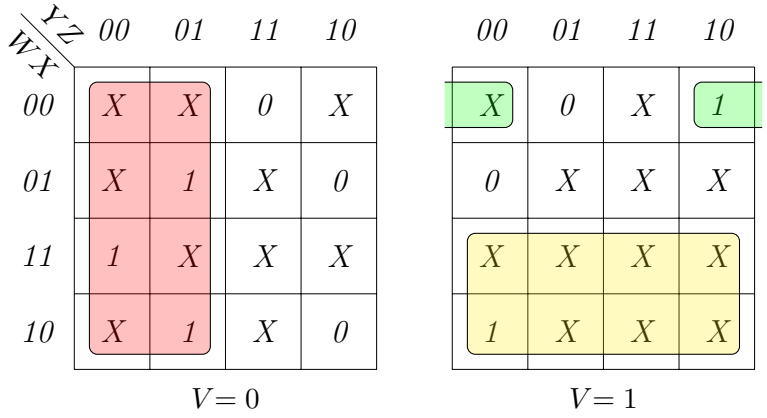
This produces:

$$B = \overline{V}(\overline{X}\overline{Y} + XY) + V(\overline{X}\overline{Z} + Z)$$

$$B = \overline{V}(\overline{X}\overline{Y} + XY) + V(\overline{X} + Z) \quad \textit{(Absorption)}$$

$$B = \overline{V}\overline{X}\overline{Y} + \overline{V}XY + V\overline{X} + VZ \quad \textit{(Distribution)}$$

Example 7 ***A Output***



This produces:

$$A = \overline{V}\overline{Y} + V(\overline{W}\overline{X}\overline{Z} + W)$$
$$A = \overline{V}\overline{Y} + V\overline{W}\overline{X}\overline{Z} + VW \quad \textit{(Distribution)}$$

Discussion

Ultimately, this lab aided me in gaining experience with Karnaugh maps and reducing boolean expressions. The 3D representation of the K-maps in the documentation allowed for a simpler visualization of this in my own head. It was actually quite engaging and took a lot of carful attention to detail to each and every single value. I found myself having multiple transcription errors, but in doing this, I gained a lot more practice.

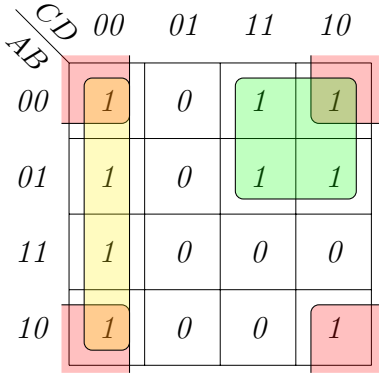
The introduction to the breadboard and having hands on real hardware was a nice change in pace for me. I have not worked with physical hardware since I was attached to Reactor Controls division on a nuclear fast attack submarine. Nevertheless, it was interesting to see how much more lenient the lab can be when only dealing with 5V coming from the transformers compared to the vast hoops I had to jump through with electrical safety in the Nuclear Navy.

Careful attention was placed on cable routing as this is paramount to allow for comprehensive troubleshooting down the line. Looking forward to the other labs, I want to learn more complex combinational logic and start gronking the sequential logic again that I was exposed to in Nuclear Field Electronics Technician 'A' School many years ago. The pace and military obligations during 'A' school were way too demanding to appreciate the subject and what it is that we learned, it was just a fire hose of information for 2 years straight 7am to frequently close to 8pm. The slower pace of a University course where more attention is given to everyone is a breath of fresh air as it allows me to really get into the weeds of what the specifics are. For this lab, I reviewed silicon doping and how a PN Junction works in order to understand (or better yet, remember) how a BJT's components react to different values of potential.

This sparked a lot of memories of troubleshooting various circuit cards on the boat and reading endless documentation until the problem was identified and the guilty components replaced, installed, and retested. It also allowed for use of some standardized lab equipment such as a digital multimeter and a logic probe, which I am very excited to continue working with.

Practice Questions

Example 8 ***Karnaugh Map for*** $\sum m(0, 2, 3, 4, 6, 7, 8, 10, 12)$



This produces:

$$F(A, B, C, D) = \overline{A}C + \overline{B}\,\overline{D} + \overline{C}\,\overline{D}$$

$$F(A, B, C, D) = \overline{A}C + \overline{D}(\overline{B} + \overline{C}) \quad \textit{(Distribution)}$$

Example 9 ***IEEE-754 Floating Point Conversion***

We are tasked with converting -19.5_{10} *into Single Precision IEEE-754 floating point format. We will show the sign bit, exponent, and first 8-bits of the mantissa.*

Step 1: Determine the sign bit (S)

Since the number is negative, the sign bit is:

$$S = 1$$

Step 2: Convert the magnitude $\mathbf{19.5_{10}}$ ***to binary***

First, we convert the integer part and the fractional part of 19.5_{10} *to binary:*

$$19_{10} = 10011_2 \quad \textit{and} \quad 0.5_{10} = 0.1_2$$

Therefore, the binary representation of 19.5_{10} *is:*

$$10011.1_2$$

Step 3: Normalize the binary number

We normalize 10011.1_2 *into the form* $1.M \times 2^E$ *by shifting the decimal point 4 places to the left:*

$$10011.1_2 = 1.00111_2 \times 2^4$$

Here, the mantissa M *is* 00111_2*, and the exponent* E *is* 4*.*

Step 4: Calculate the biased exponent

The exponent is biased by 127 in Single Precision IEEE-754. So, we add 127 to the actual exponent 4*:*

$$E = 127 + 4 = 131$$

Converting to binary, we get:

$$E = 10000011_2$$

Step 5: Assemble the IEEE-754 representation

Now we can assemble the components:

- *Sign bit* $S = 1$
- *Exponent* $E = 10000011_2$
- *Mantissa* $M = 00111_2$ *(we add trailing zeros to get the first 8 bits:* 00111000_2*)*

Thus, the first 17 bits of the IEEE-754 floating-point representation of -19.5_{10} *are:*

$$1\ 10000011\ 00111000_{IEEE-754}$$

Final Answer: *The IEEE-754 single-precision representation of* -19.5_{10} *(with the first 8 bits of the mantissa) is:*

$$1\ 10000011\ 00111000_{IEEE-754}$$