LAB 4 // Hardware
HARDWARE I/O AND KARNAUGH MAPS

INSTRUCTIONS and RUBRIC

CSE 2301 – Fall 2024

This is a continuation of the first week of the lab assignment. If you have not yet completed the construction of the I/O hardware, derivation of the POSTNET equations via Karnaugh maps, and construction of a LogicWorks mock-up, go back to week 3.

PART 4:

Protoboard Wiring

YOUR TASK – Implement the design you *successfully* tested in LogicWorks on your protoboard. Draw out your connections. Write down which variable each switch is associated with (these tasks are required for your deliverables). When you have finished the circuit and tested it exhaustively, demo to your TA. This concludes the lab.

Protoboard wiring can be arduous, and even very small mistakes can cause considerable frustration, so it is important to be methodical with your approach. First, look up the pin diagrams for components you will be using. Using this information, draw out your connections. This will not only serve as a guide when building the circuit, but also a reference when you inevitably misplace something and need to remember what each wire is connected to. If you have not, we strongly recommend you watch the module 5.5 videos to learn more troubleshooting techniques. Remember that your final outputs (D, C, B, and A) must be connected to the 7405 chip in your output subcircuit.

> NOTE: Try to stick to AND-2 and OR-2 gates, since your equations should be reduced anyway. The AND chip is a 7408, the INV/NOT chip is a 7404, and the OR chip is a 7432. The pin layouts of AND-2 and OR-2 chips are the same. The pin layout of a 7405 is the same as a 7404's.

SCORING

Demo Requirements [5 pts]:

- ✓ Draw a prototype diagram indicating where your wires will be connected and what all of your switches do.
- ✓ Wire the circuit onto your protoboard. You will receive 4 points for one implementation error, 3 points for two errors, but zero points for further issues. **Demo (5 pts).**

Report Requirements [3.5 pts]:

- ✓ [1.9] Theory:
  - [0.9] Display an understanding of minimizing equations with Karnaugh Maps in your own words. How are they set up and how do you use them? Why do we need "don't care" states (boxes marked with an X)?
  - [0.6] What are POSTNET (2 out of 5, 74210 weighting) and XS3? Keep it brief.
  - [0.4] How many non-valid input codes are in your circuit?
- ✓ [1.2] Deliverables:
  - [0.8] Attach the prototype diagram for all of your wires and switches.
  - [0.4] Make a POSTNET symbology bar code for your home area. If you'd rather not say, you can select any location.
- ✓ [0.4] Discussion section. Should conform to standard lab report guidelines.

Practice Questions [1.5 pts]:

- ✓ [0.5] Question 1:
  Convert unsigned binary 11010010_2 to ternary and hexadecimal.
- ✓ [0.5] Question 2:
  Convert the POSTNET (9) symbology bar code below into its decimal representation. Do not include the checksum.

- ✓ [0.5] Question 3:
  Use DeMorgan's theorem to simplify the formula below [0.2 points] then draw the circuit [0.3 points]. Make sure to only use AND-2, OR-2, and INV/NOT gates.
  Formula: $D'(CB' + A') + \overline{(D' + A)}$.