LAB 12 // Software
VHDL

INSTRUCTIONS and RUBRIC
CSE 2301 – Fall 2024

INTRODUCTION

Prerequisites
For this assignment it is expected that you are familiar with Hamming parity codes and the 2-bit ALU from lab 6.

Objectives
The objectives of this assignment are to gain an understanding of combinational VHDL and its applications.

Background
VHDL is a hardware description language with applications in digital design and PLA programming. We will be using it to reimplement basic combinational circuits which we have constructed in previous labs. LogicWorks includes tooling to create circuit components with VHDL.

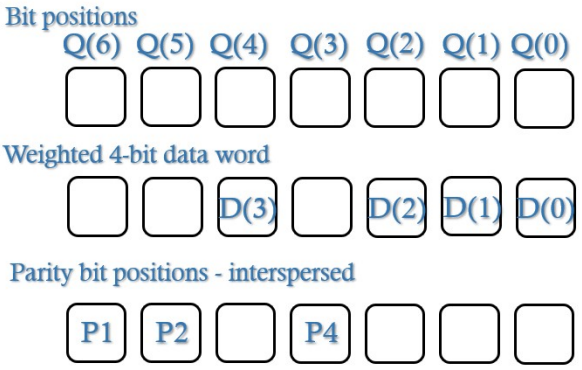
Please utilize the Starter Code provided with the assignment for both parts. The full implementation of these components is beyond the scope of this course.

PART 1:

Parity Generator

YOUR TASK – Follow the directions in the slide show to complete the starter VHDL code. The code should generate even Hamming parity bits for a 4-bit input. Please review the slide show and starter code for more detailed instructions.

Parity Bit	Based on Data Bits
P1	D(3), D(2), D(0)
P2	D(3), D(1), D(0)
P3	D(2), D(1), D(0)



PART 2:

2-bit ALU

YOUR TASK – Follow the directions in the slide show to complete the starter VHDL code. The circuit module should be capable of performing 4 operations depending on the state of the Op input bits. A and B are the 2-bit inputs which should be operated on. Q is the 4-bit output

OP	Q
00	A AND B (pad A/B with 0s to 4-bits)
01	A OR B (pad A/B with 0s to 4-bits)
10	A + B (pad A/B with 0s to 4-bits and convert to unsigned)
11	A * B (convert A/B to unsigned)

SCORING

Demo Requirements [5 pts]:

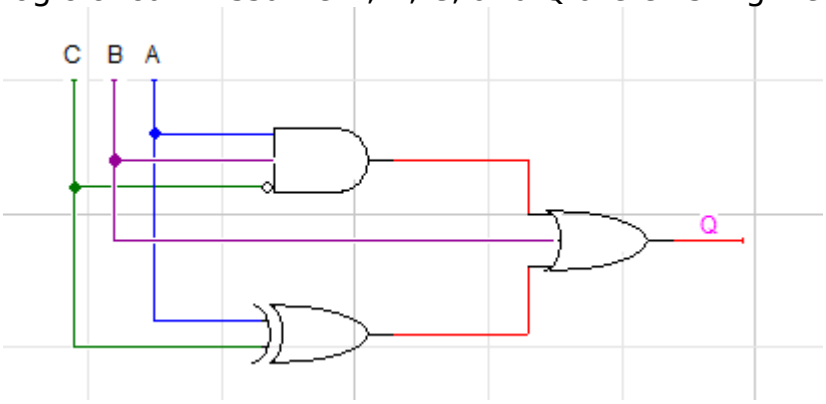
- ✓ Show TAs your finished Parity Generator circuit **(2.5 pts).**
- ✓ Show TAs your finished ALU_2 circuit **(2.5 pts).**

Report Requirements [3 pts]:

- ✓ [0.8] Theory:
  - [0.4] What is the purpose of the unsigned() function? How would the output of the ALU change if you used the signed() function instead?
  - [0.4] What circuit element are the If and Elsif statements emulating in the ALU?
- ✓ [1.6] Deliverables:
  - [0.6] Include your code for the parity bits of Part 1
  - [1.0] Include your code for the 2-bit ALU from Part 2
- ✓ [0.6] Discussion section. Should conform to standard lab report guidelines.

Practice Questions [2 pts]:

- ✓ [0.5] Question 1: Create a VHDL statement for the below combinational logic circuit. Assume A, B, C, and Q are existing well defined signals.



- ✓ [1.5] *Question 2:* Complete the starter code for the below combinational logic circuit. Assume A, B and Q are existing well defined signals. Assume sel is an existing well defined 2 bit vector. Ignore the enable pin.

```
process (A, B, sel)
begin
  if sel = "00" then
    Q <= '0';
  elsif sel = "01" then
    --enter code here

  elseif sel = "10" then
    --enter code here

  elseif sel = "11" then
    --enter code here


  end if;
end process;
```