FAIRCHILD

SEMICONDUCTOR™

June 1993
Revised April 1999

74VHC14
Hex Schmitt Inverter

General Description

The VHC14 is an advanced high speed CMOS Hex Schmitt Inverter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. Pin configuration and function are the same as the VHC04 but the inputs have hysteresis between the positive-going and negative-going input thresholds, which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals, thus providing greater noise margin than conventional inverters.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 5.5 ns (typ) at V_{CC} = 5V
- Low power dissipation: I_{CC} = 2 µA (Max) at T_A = 25°C
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (Min)
- Power down protection is provided on all inputs
- Low noise: V_{OLP} = 0.8V (Max)
- Pin and function compatible with 74HC14

Ordering Code:

Order Number	Package Number	Package Description
74VHC14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74VHC14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

IEEE/IEC
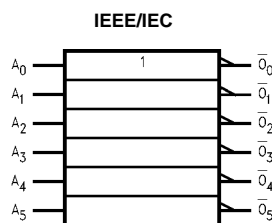
Connection Diagram
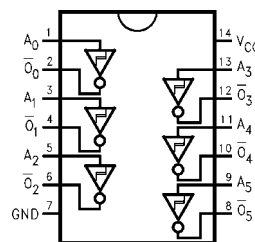
Pin Descriptions

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

A	O
L	H
H	L

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74VHC14

Absolute Maximum Ratings(Note 1)

Supply Voltage (V$_{CC}$)	−0.5V to +7.0V
DC Input Voltage (V$_{IN}$)	−0.5V to +7.0V
DC Output Voltage (V$_{OUT}$)	−0.5V to V$_{CC}$ + 0.5V
Input Diode Current (I$_{IK}$)	−20 mA
Output Diode Current (I$_{OK}$)	±20 mA
DC Output Current (I$_{OUT}$)	±25 mA
DC V$_{CC}$/GND Current (I$_{CC}$)	±50 mA
Storage Temperature (T$_{STG}$)	−65°C to +150°C
Lead Temperature (T$_L$)	
Soldering (10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V$_{CC}$)	+2.0V to +5.5V
Input Voltage (V$_{IN}$)	0V to +5.5V
Output Voltage (V$_{OUT}$)	0V to V$_{CC}$
Operating Temperature (T$_{OPR}$)	−40°C to +85°C

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The data book specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V$_{CC}$	T$_A$ = 25°C			T$_A$ = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V$_P$	Positive Threshold Voltage	3.0			2.20		2.20	V		
		4.5			3.15		3.15			
		5.5			3.85		3.85			
V$_N$	Negative Threshold Voltage	3.0	0.90			0.90		V		
		4.5	1.35			1.35				
		5.5	1.65			1.65				
V$_H$	Hysteresis Voltage	3.0	0.30		1.20	0.30	1.20	V		
		4.5	0.40		1.40	0.40	1.40			
		5.5	0.50		1.60	0.50	1.60			
V$_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	V$_{IN}$ = V$_{IL}$	I$_{OH}$ = −50 μA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I$_{OH}$ = −4 mA
		4.5	3.94			3.80				I$_{OH}$ = −8 mA
V$_{OL}$	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	V$_{IN}$ = V$_{IH}$	I$_{OL}$ = 50 μA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I$_{OL}$ = 4 mA
		4.5			0.36		0.44			I$_{OL}$ = 8 mA
I$_{IN}$	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V$_{IN}$ = 5.5V or GND	
I$_{CC}$	Quiescent Supply Current	5.5			2.0		20.0	μA	V$_{IN}$ = V$_{CC}$ or GND	

Noise Characteristics

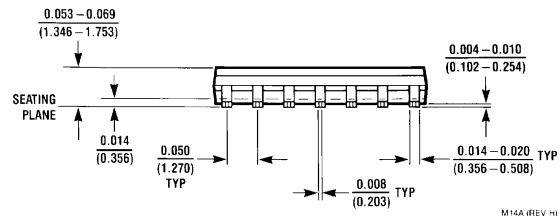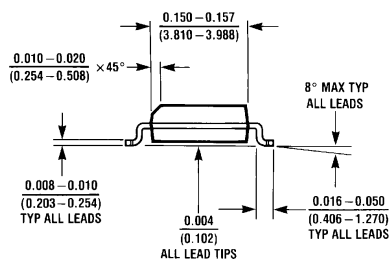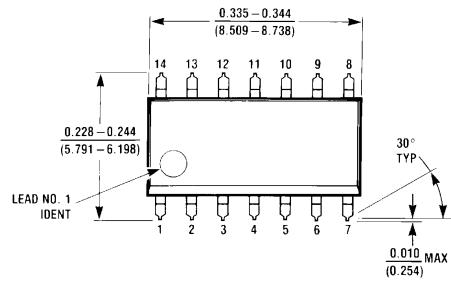| Symbol	Parameter	V$_{CC}$	T$_A$ = 25°C		Units	Conditions
			Typ	Limits		
V$_{OLP}$ (Note 3)	Quiet Output Maximum Dynamic V$_{OL}$	5.0	0.4	0.8	V	C$_L$ = 50 pF
V$_{OLV}$ (Note 3)	Quiet Output Minimum Dynamic V$_{OL}$	5.0	−0.4	−0.8	V	C$_L$ = 50 pF
V$_{IHD}$ (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C$_L$ = 50 pF
V$_{ILD}$ (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C$_L$ = 50 pF

Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

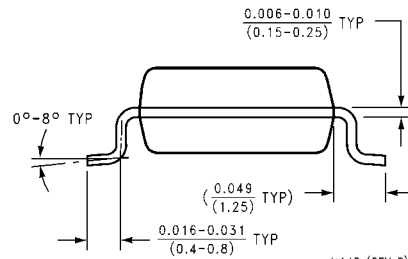| Symbol	Parameter	V$_{CC}$	T$_A$ = 25°C			T$_A$ = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t$_{PLH}$	Propagation Delay	3.3 ± 0.3		8.3	12.8	1.0	15.0	ns	C$_L$ = 15 pF
t$_{PHL}$	Time			10.8	16.3	1.0	18.5		C$_L$ = 50 pF
		5.0 ± 0.5		5.5	8.6	1.0	10.0	ns	C$_L$ = 15 pF
				7.0	10.6	1.0	12.0		C$_L$ = 50 pF
C$_{IN}$	Input Capacitance			4	10		10	pF	V$_{CC}$ = Open
C$_{PD}$	Power Dissipation Capacitance			21				pF	(Note 4)

Note 4: C$_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (Opr) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/6 (per Gate)

Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

0.010
(0.254) MAX

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) ×45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

14 8

0.295 − 0.319
(7.5 − 8.1)

0.205 − 0.213
(5.2 − 5.4)

1 7

0.394 − 0.402
(10.0 − 10.2)

(0.71
(1.8))

0.067 − 0.083
(1.7 − 2.1)

0.006 − 0.010
(0.15 − 0.25) TYP

0° − 8° TYP

0.006 (0.15)

SEATING PLANE

0.050
(1.27) TYP

0.014 − 0.020
(0.35 − 0.50) TYP

0.000 − 0.010
(0 − 0.25)

(0.049
(1.25) TYP)

0.016 − 0.031
(0.4 − 0.8) TYP
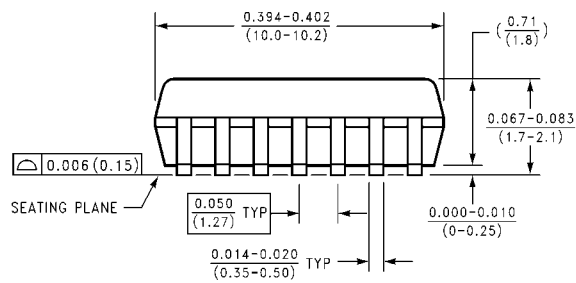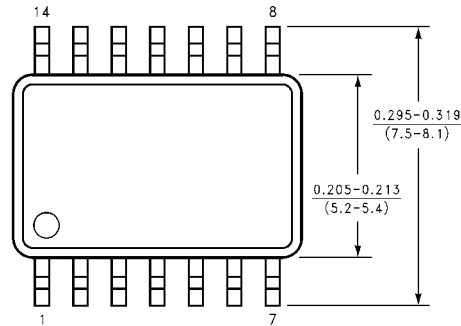
M14D (REV B)

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

5.0±0.1
-A-

0.43 TYP

14   8

6.4

3.2

4.4±0.1
-B-

1   7
ALL LEAD TIPS

◯ 0.2 C B A

PIN #1 IDENT.

7.72

4.16

1.78

0.65   0.42

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS

1.2 MAX

◯ 0.1 C

-C-

0.65

0.19 - 0.30

⊕ 0.13Ⓜ A BⓈ CⓈ

0.90 +0.15 -0.10

0.10±0.05

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTOM

R0.16

R0.31

0°-8°

GAGE PLANE

0.25

SEATING PLANE

0.6±0.1

1.00

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
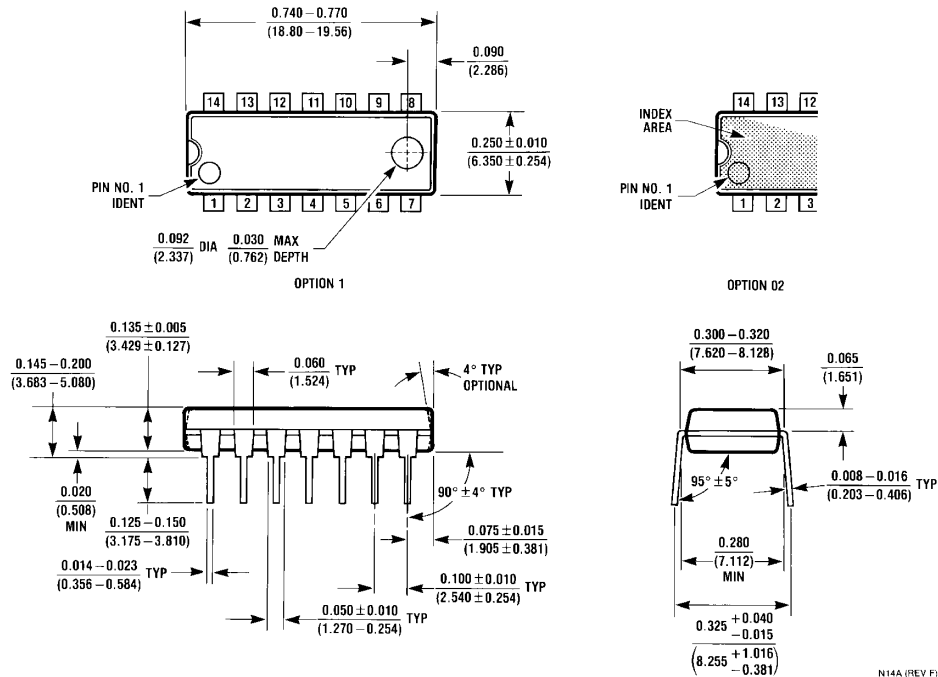   REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
   AND TIE BAR EXTRUSIONS

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.740 − 0.770
(18.80 − 19.56)

0.090
(2.286)

14 13 12 11 10 9 8

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7

0.092
(2.337) DIA   0.030
(0.762) MAX DEPTH

OPTION 1

INDEX
AREA

14 13 12

PIN NO. 1
IDENT

1 2 3

OPTION 02

0.135 ± 0.005
(3.429 ± 0.127)

0.145 − 0.200
(3.683 − 5.080)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.020
(0.508)
MIN

0.125 − 0.150
(3.175 − 3.810)

90° ± 4° TYP

0.014 − 0.023
(0.356 − 0.584) TYP

0.075 ± 0.015
(1.905 ± 0.381)

0.100 ± 0.010
(2.540 ± 0.254) TYP

0.050 ± 0.010
(1.270 − 0.254) TYP

0.300 − 0.320
(7.620 − 8.128)

0.065
(1.651)

95° ± 5°

0.008 − 0.016
(0.203 − 0.406) TYP

0.280
(7.112)
MIN

0.325 $^{+0.040}_{-0.015}$

$\left(8.255 ^{+1.016}_{-0.381}\right)$

N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A