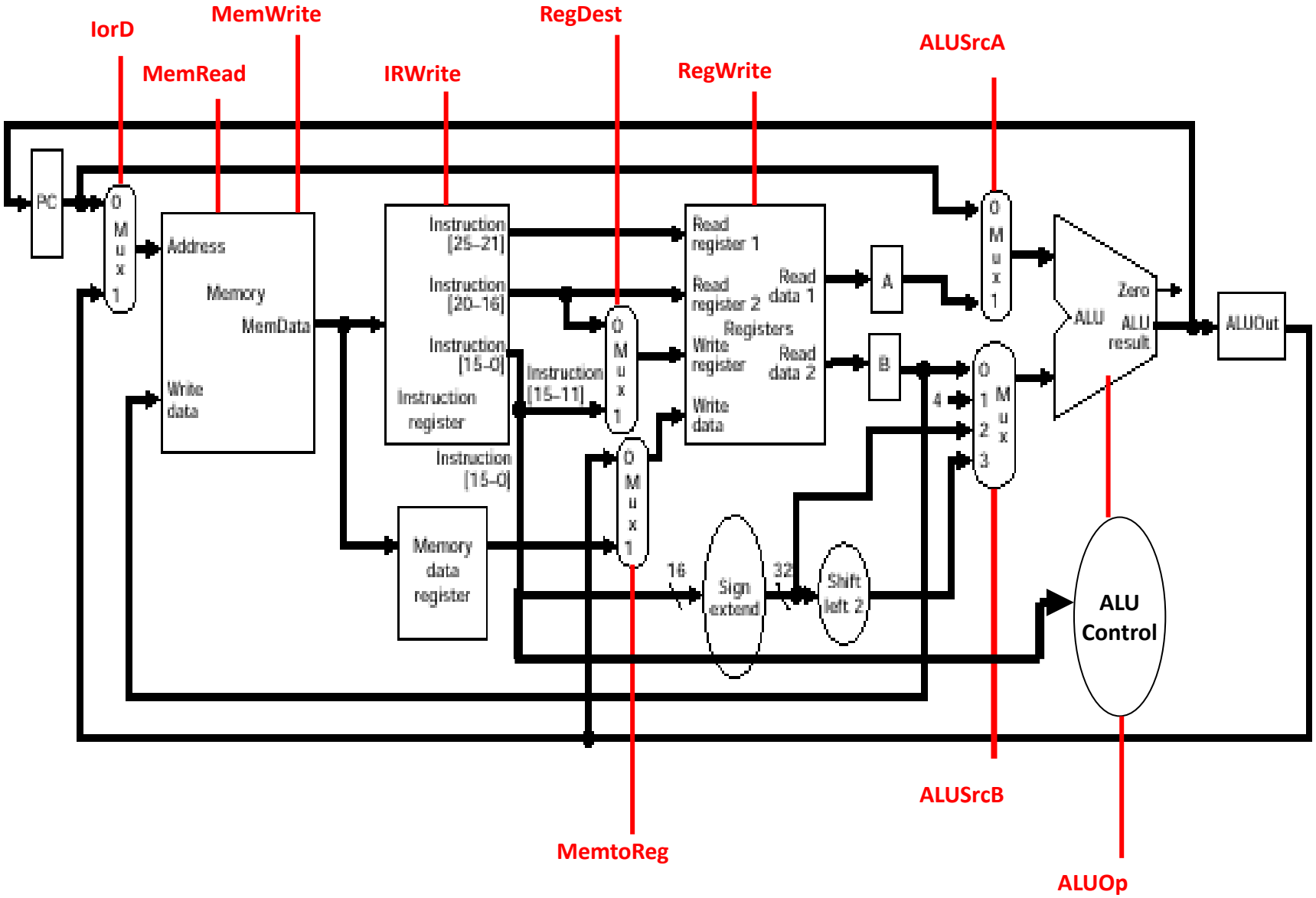
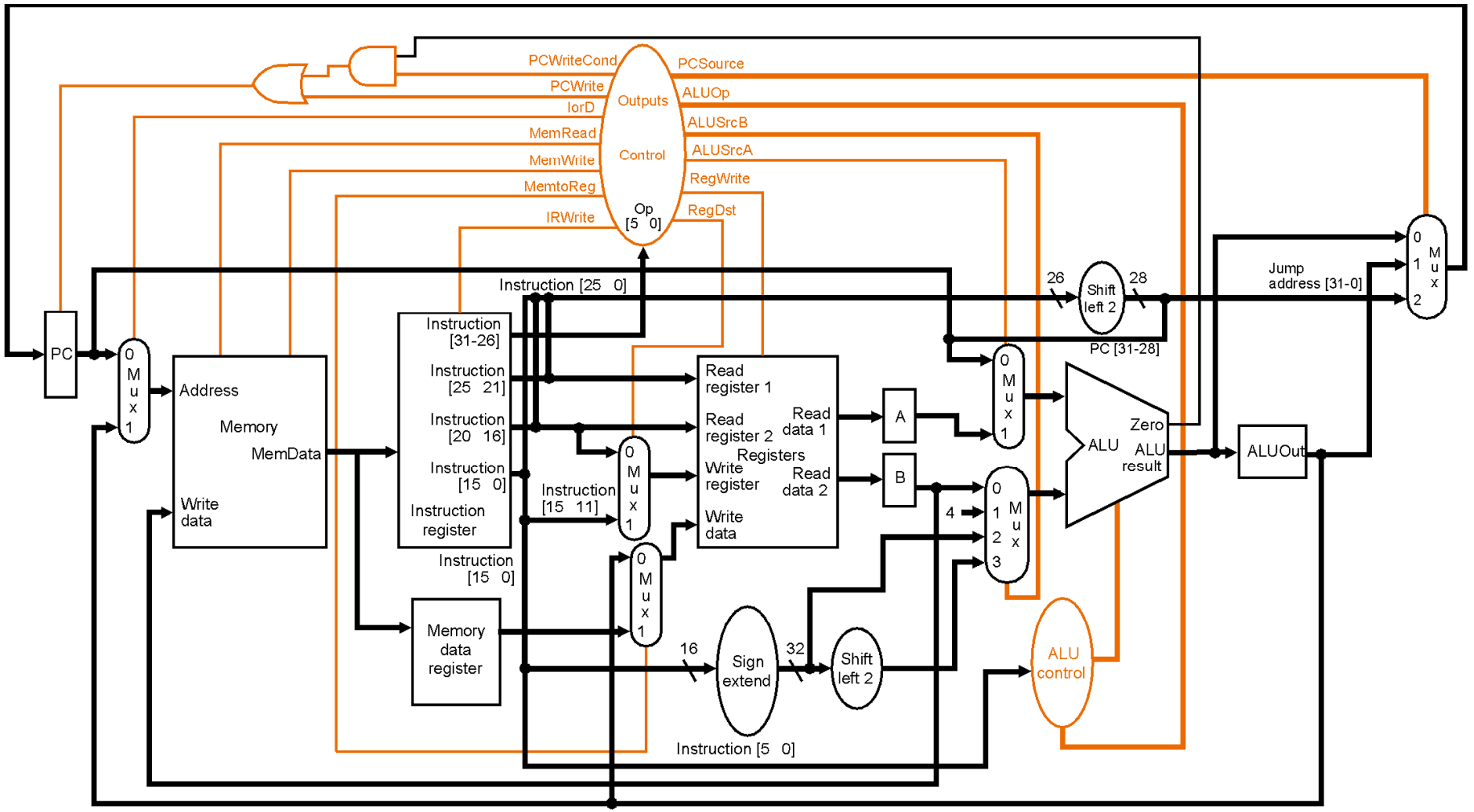
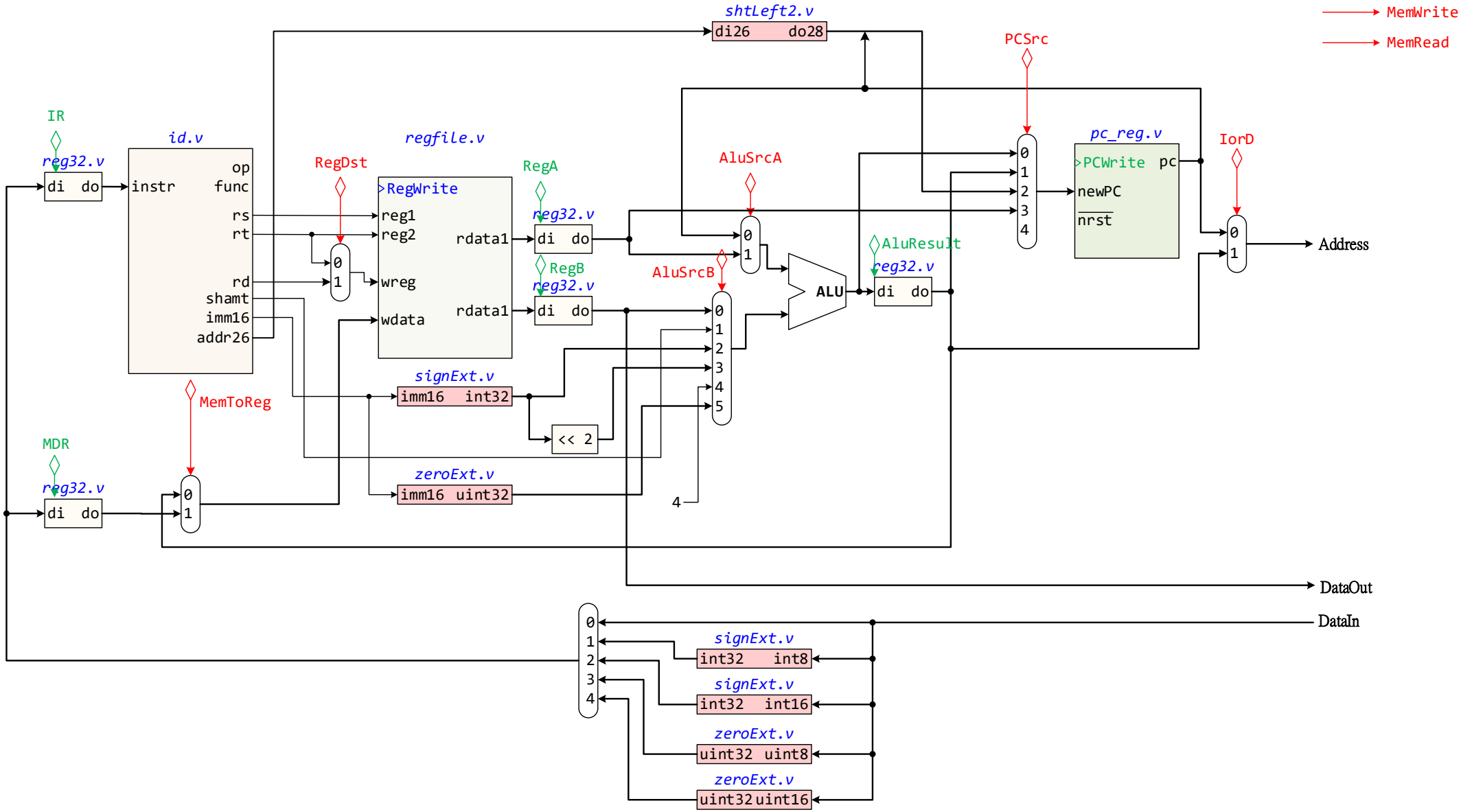
Project – MultiCycle Datapath for MIPS32

Multiple Cycle Datapath with Control



The Complete Multicycle Dataath




MemWrite
MemRead
shtLeft2.v
di26 do28
PCSrc
IR
reg32.v
di do
id.v
instr
op
func
rs
rt
rd
shamt
imm16
addr26
RegDst
regfile.v
RegWrite
reg1
reg2
wreg
wdata
rdata1
rdata1
RegA
reg32.v
di do
RegB
reg32.v
di do
AluSrcA
AluSrcB
ALU
AluResult
reg32.v
di do
pc_reg.v
PCWrite
pc
newPC
nrst
IorD
Address
signExt.v
imm16 int32
<< 2
MemToReg
MDR
reg32.v
di do
zeroExt.v
imm16 uint32
4
DataOut
DataIn
signExt.v
int32 int8
signExt.v
int32 int16
zeroExt.v
uint32 uint8
zeroExt.v
uint32 uint16

Defining the Control

- The control of the multicycle datapath must specify both the signals to be set in any step and the next step in the sequence

- Two techniques:
  - **Finite state machine**
    - **Each state (a circle) contains the valid control signals**
    - **Directional links point to next state**
    - **Each cycle corresponds to one state**
    - **FSM is the graphical representation of the control**
  - **Microprogramming**
    - **Assume the set of control signals that must be asserted in a state as an instruction to be executed by the datapath**
    - **Microprogram is a symbolic representation of the control that will be translated by a program to control logic**

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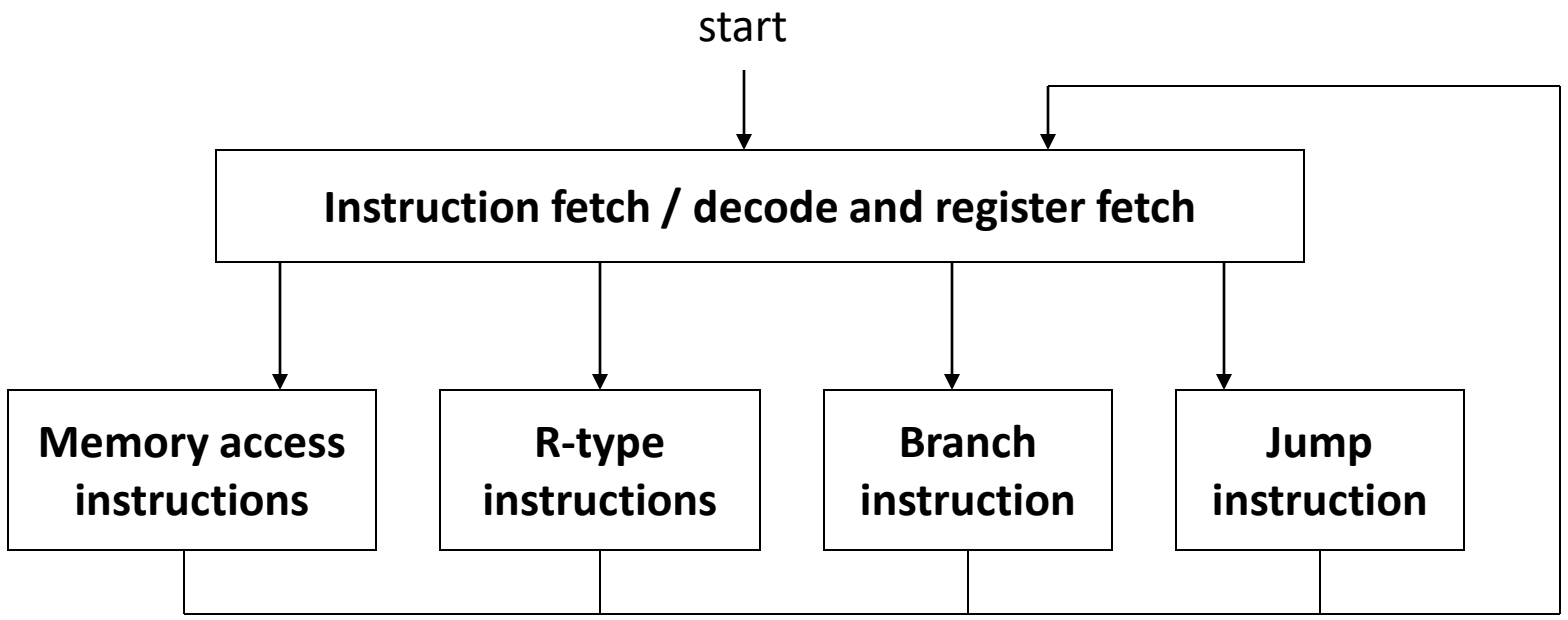
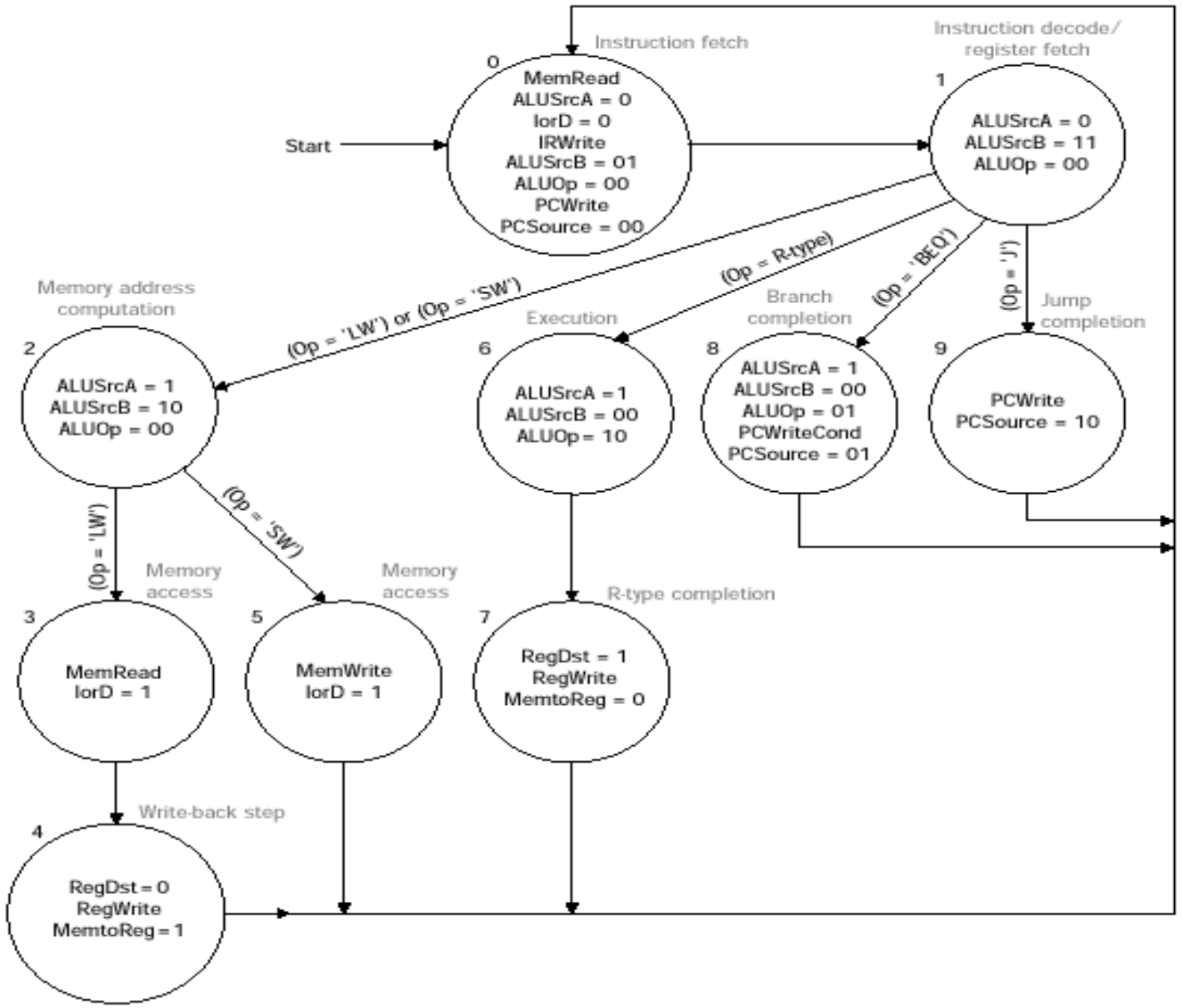
The high-level view of the FSM control



Finite State Machine Control



Implementation of the FSM Control