SYNOPSYS®

DesignWare IIP

Functional Specification

DWC_mshc/DWC_mshc_lite 1.70a-ea00 Functional spec

Revision: 1.0

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ABSTRACT

This document describes the enhancement in DWC_mshc/DWC_mshc_lite IP for muxing sampling clock in HS400 mode

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Document Revision History:

Version	Date	Author	Change Description
1.0	23/06/2017	Mobile Storage team	Preliminary version
2.0	30/06/2017	Mobile Storage team	1.70a-ea00 release version

Disclaimer

This is a preliminary version of the functional specification and is being shared for review. This specification is subject to change, based on the inputs from the reviewers. It should also be noted that Synopsys may adopt a phased approach for the implementation of the features and functionality, and thus not all features described here in this version of the document may be present in the first version of the product being developed.

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1. Introduction

1.70a-ea00 release introduces a new enhancement on muxing the sampling clock in HS400 mode, description of this new functionality is as described in this document.

1.1 Sampling clock muxing in 1.60a and below

The eMMC standard version 5.0 and above provides the data strobe interface signal that is driven by the device during read data output and write CRC status response output in HS400 mode. The enhanced data strobe (eMMC version 5.1 and above) is also driven during the CMD response in HS400 mode. In HS400 spped mode, DWC_mshc uses data strobes signal to sample the read data and write CRC status response. This signal is also used to sample the CMD response when enhanced strobe is enabled in DWC_mshc. The host system shall phase delay the data strobe so that it is center aligned. For other speed mode of operation, DWC_mshc controller used cclk_rx to sample the read data, write CRC response and CMD response.

To facilitate the sampling either with respect to data strobe or cclk_rx, DWC_mshc controller internally implement a clock mux. The mux control is generated based on the speed mode of operation. It is synchronous to rising edge of cclk_rx. Figure 1-1 represents the muxing of sampling clock based on speed of operation. However, cclk_rx is used as a test clock during scan mode.

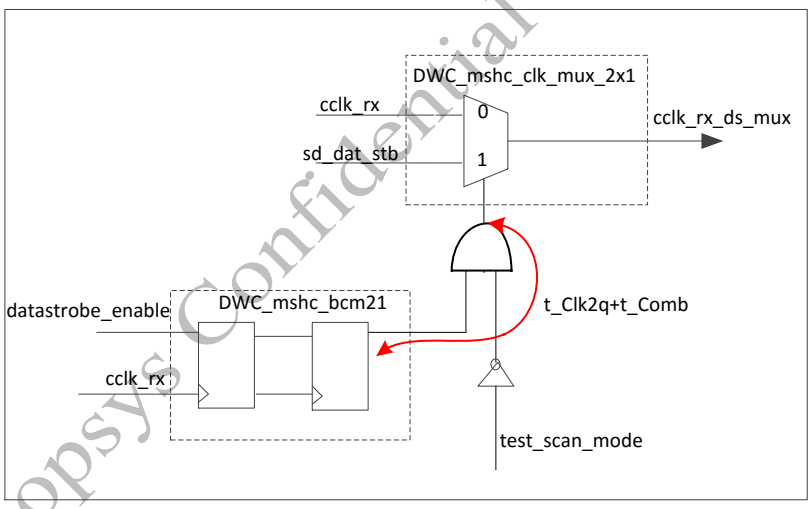

Figure 1-1 : Sampling clock muxing in 1.60a

Since data strobe is actively driven by eMMC device only during the transfer, data strobe is held low during the switching of sampling clock. However, the switching mux control is launched at rising edge of cclk_rx, a glitch may be observed on sampling clock if paths are not balanced i.e if (t_Clk2q + t_Comb) delay of the mux control is not compensated on the path delay of mux data. Figure 1-2 shows the glitch on sampling clock if cclk_rx to the DWC_mshc_clk_mux_2x1 is not balanced for (t_Clk2q + t_Comb).

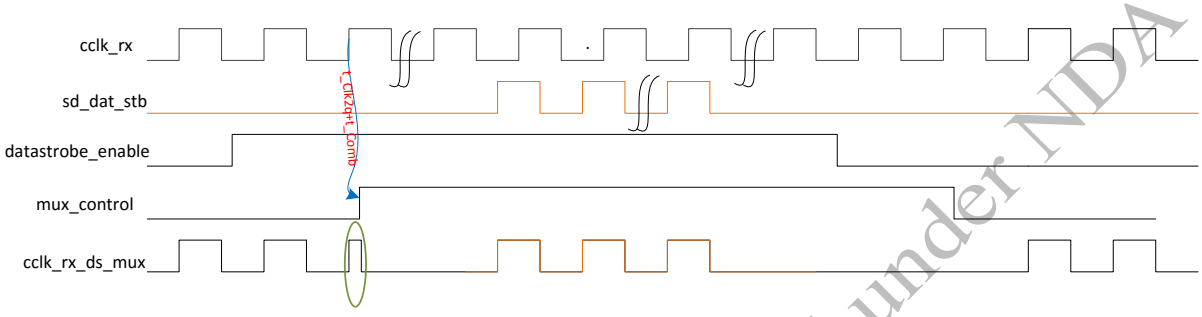

Figure 1-2 : Glitch on sampling clock

1.2 Proposed Enhancement

The enhancement is to change the mux control on the negative edge of cclk_rx so that no glitch is generated due to (t_Clk2q and t_Comb) delay on the mux control

1.3 Standards Compliance

The solution conforms to the following specifications.

- ✓ *SD Specifications Part A2 SD Host Controller Standard Specification Version 4.10, Sep 2013*
- ✓ *SD Specifications Part 1 Physical Layer Specification Version 6.0,*
- ✓ *eMMC JESDB51 Specification*

2. Enhancement Description

2.1 User Interface changes

No change

2.2 New Parameters

No change

2.3 Backward Compatibility with 1.60a and below

This enhancement always changes the mux control for sampling clock in HS400 mode with respect to negative edge of cclk_rx

2.4 New I/O Signal description

No New I/O signals added

3. Registers

No New Registers added

4. Functional Description

In this enhancement, the mux control to sampling clock mux changes with respect to negative edge of cclk_rx. Since data strobe and cclk_rx is held low during the change of mux control, a glitch is not generated without the need to compensate the path delay (t_Clk2q and T_Comb). The same circuitry is implemented for sampling the CMD response in enhanced strobe mode.

The enhancement brings in some negative edge triggered flops in functional mode. However, a scan mux is implemented so that all negative edge triggered flops in functional mode can be included in the single positive scan chain. Figure 4-1represents the new circuitry for muxing sample clock.

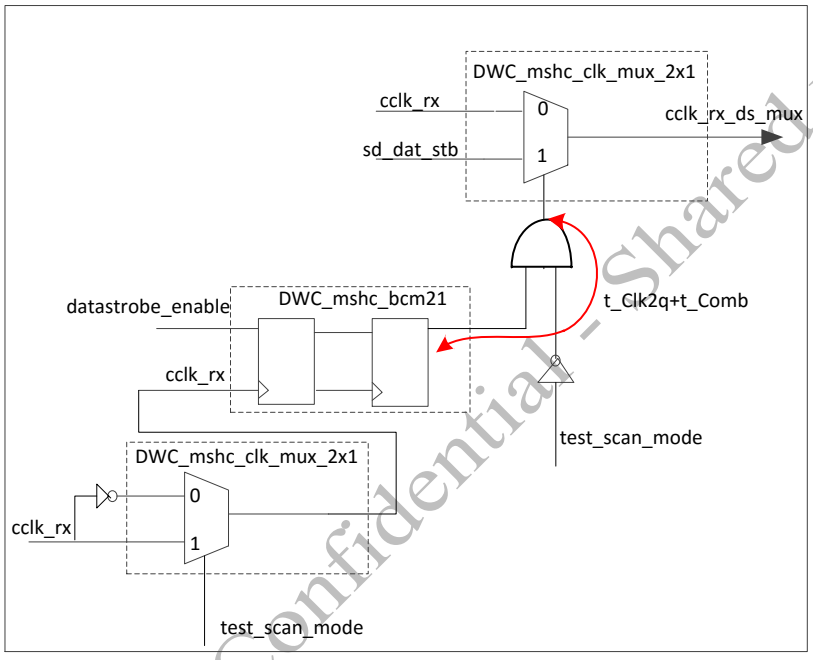

Figure 4-1 : Sampling clock mux control in 1.70a-ea00

Figure 4-2 shows the sampling clock without glitch. In this approach, the clock mux control changes while both the clocks are held low.

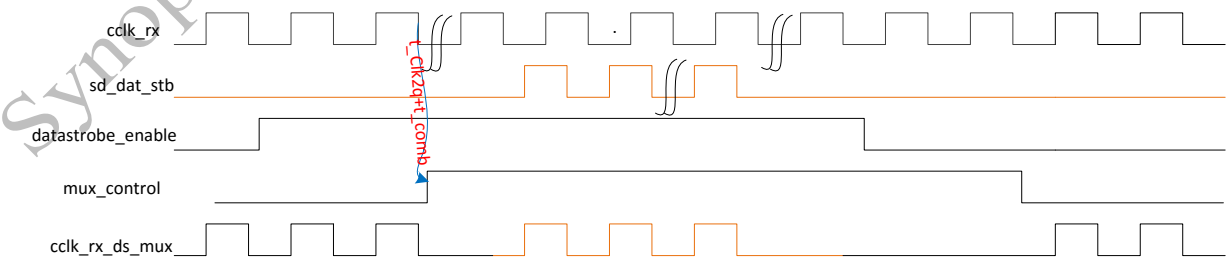

Figure 4-2 : No glitch on sampling clock

5. Implementation Guidelines

Add ¼ cycle max path delay synthesis constraint for clock mux control input as depicted below

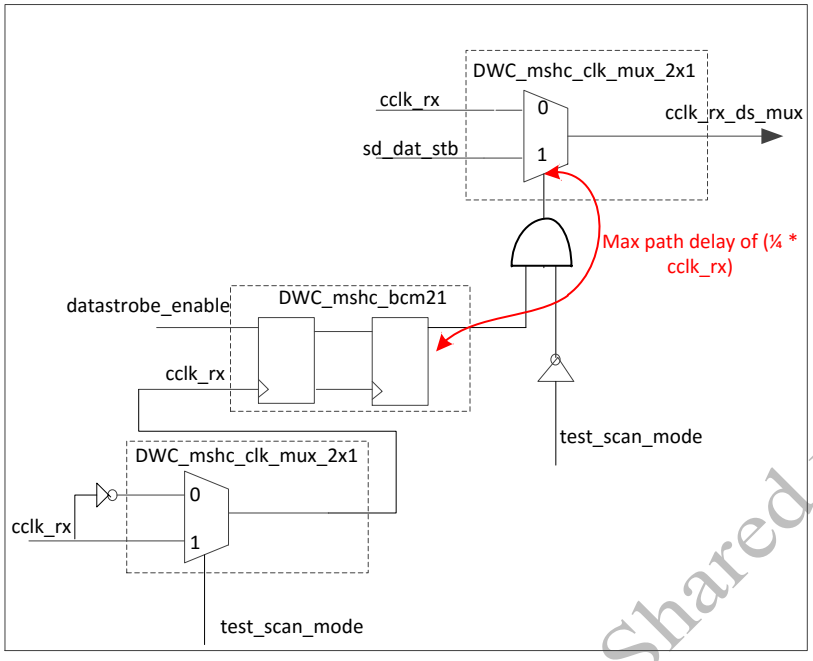

Figure 5-1 : Max path delay synthesis constraint on clock mux control input

6. Programming Sequence

No change

7. Documentation Impact

Databook and userguide will be updated and delivered as part of 1.70a-GA release

8. References

- SD Specifications Part A2 SD Host Controller Standard Specification Version 4.20
- DesignWare Cores Mobile Storage Host Controller Databook version 1.60a
- DesignWare Cores Mobile Storage Host Controller Userguide version 1.60a