Synopsys TS28HPC Logic Library

Sign-off Methodology and Recommendations
Vddnom=0.9V

15th Dec'2016

CONFIDENTIAL INFORMATION

The following material is confidential information of Synopsys and is being disclosed to you pursuant to a non-disclosure agreement between you or your employer and Synopsys. The material being disclosed may only be used as permitted under such non-disclosure agreement.

IMPORTANT NOTICE

In the event information in this presentation reflects Synopsys' future plans, such plans are as of the date of this presentation and are subject to change. Synopsys is not obligated to develop the software with the features and functionality discussed in these materials. In any event, Synopsys' products may be offered and purchased only pursuant to an authorized quote and purchase order or a mutually agreed upon written contract.

Revision History

DATE	DESCRIPTION
5-Jul	Initial
11-Oct	FFG to FF corner in flat OCV table
23-Sep	Added voltage/temp, on-chip wire, spatial margin, and register constraint details.
7-Oct	Added wire derates to flat OCV table, removed extra information
21-Oct	Added 3σ derate tables for local supply voltage variation given peak of this variation from 4mV to 40mV.
26-Oct	Consolidated supply OCV derates.
15-Dec	Added 0C and 125C voltage and temperature derates

Logic Sign-off Methodology & Margining

28HPC On Chip Variation Signoff Components

1. **Overview**
2. **On-Chip Process Variation Methods:**
   - Flat de-rate method, includes flat register setup and hold constraint margins
   - Advanced On Chip Variation method
3. **On-Chip Voltage Variation and Local Temperature Variation**
4. **On-Chip Wire Variation**
5. **On-Chip Spatial Margin**
6. **Register-Hold-Constraint-Margin for Local-Process Variation**
   - Flat margin
   - Liberty based

Sign-off Methods Guideline

- **Best known method**
  - Document describes method based on TSMC's method but applied to Synopsys libraries. Synopsys reserves right to update the document without prior notice when an improved, verified and approved OCV methodology becomes available.

- **Use this guideline appropriately**
  - Guideline is based on simulation using specified
    - SPICE model, LPE netlist, a pessimistic cell chain topology, cell Vth/size, transition times and PVT variation

- OCV customization available for designs which use weaker cells (eg. smaller size, higher Vth), larger slews or PVT conditions that can result in larger variability

- The guideline does not guarantee silicon viability, as the actual amount of timing margin required is still subject to specific design conditions not covered by this guideline

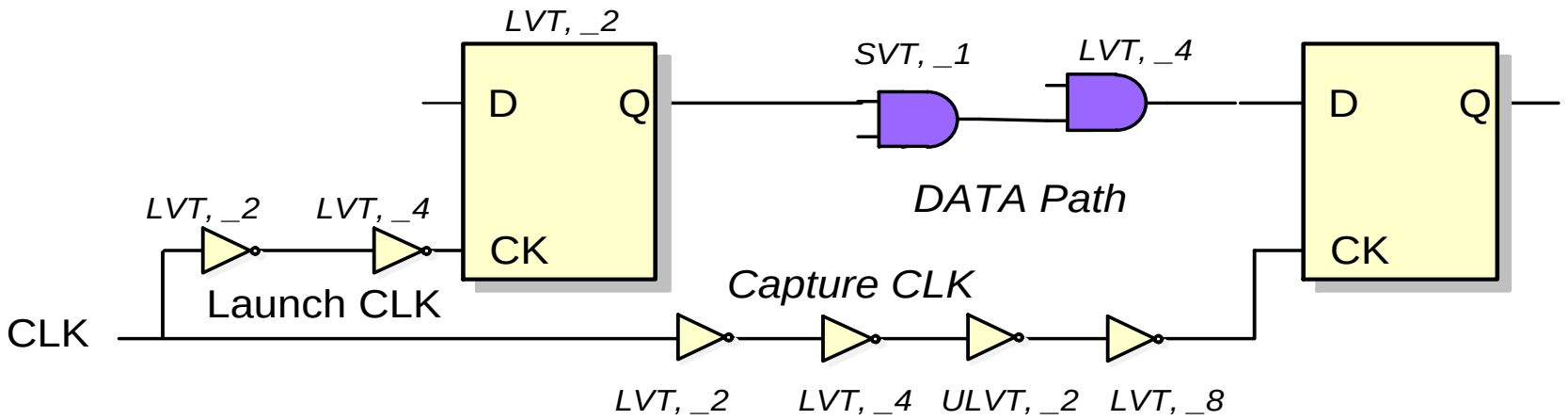
OCV Customization

- Synopsys can provide OCV customization for customer's design and sign-off conditions on a custom basis
  - Operating conditions: process, voltage, temperature, slew
  - Variation: IR-drop spec, process sigma
  - Cell library spec: size, Vth, gate length, track-height.

- Advise design adjustments to control variation
  - Example is to use larger-size and lower-Vth cells to control the rise in OCV when operating at lower Vdd

Using Conservative Design Spec. in OCV Determination

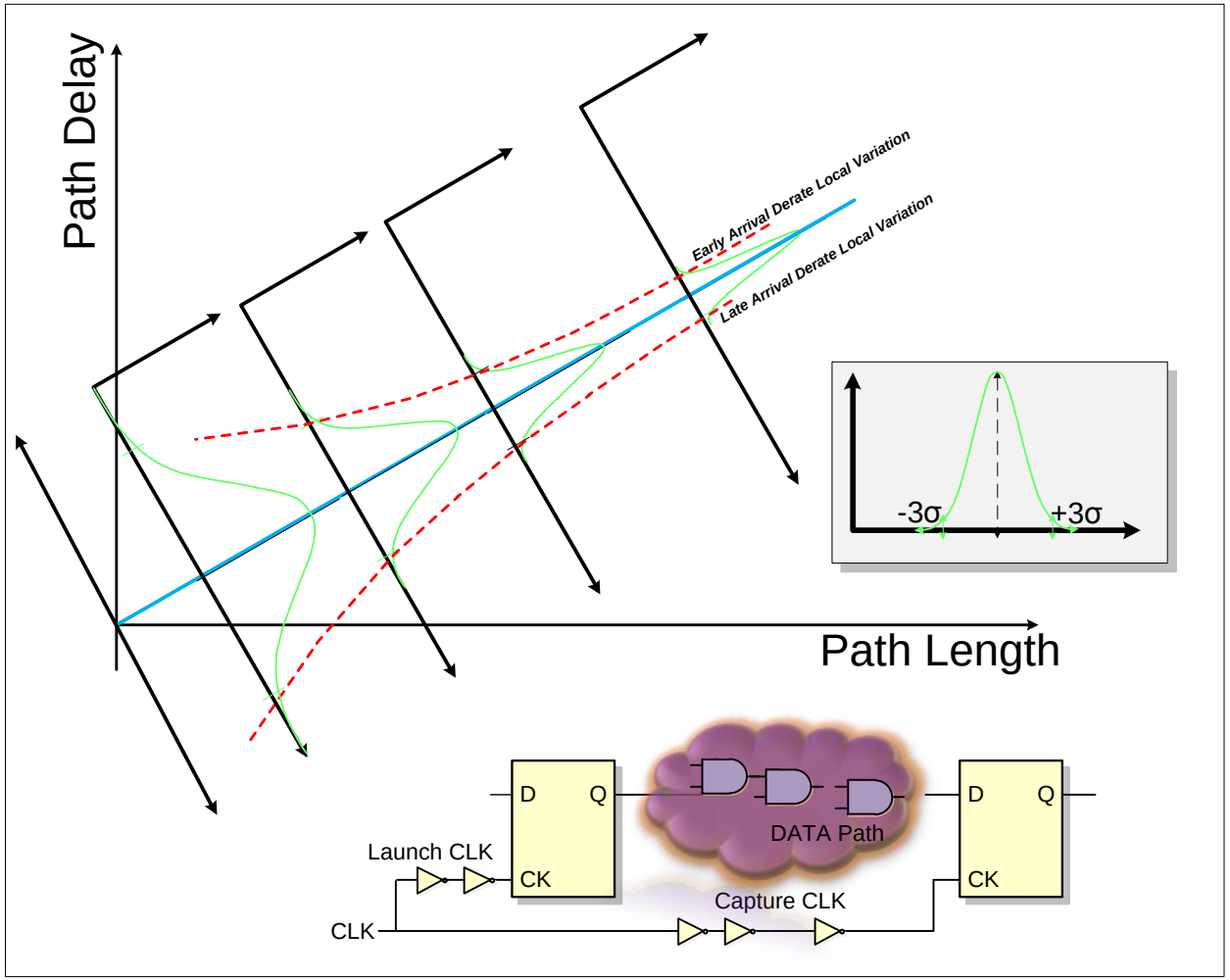
- Cells with larger variation tend to dominate path variation and one should use a conservative design spec when determining OCVs
  - Use conservative design spec in mixed cell usage
- The following spec usually result in larger OCV value
  - Large slew, Large IR_drop, smaller driving strength (<2x for clock and <1x for data), lower voltage, slower process, larger Vth
- But multiple tests on different spec to check which one is more conservative is strongly encouraged

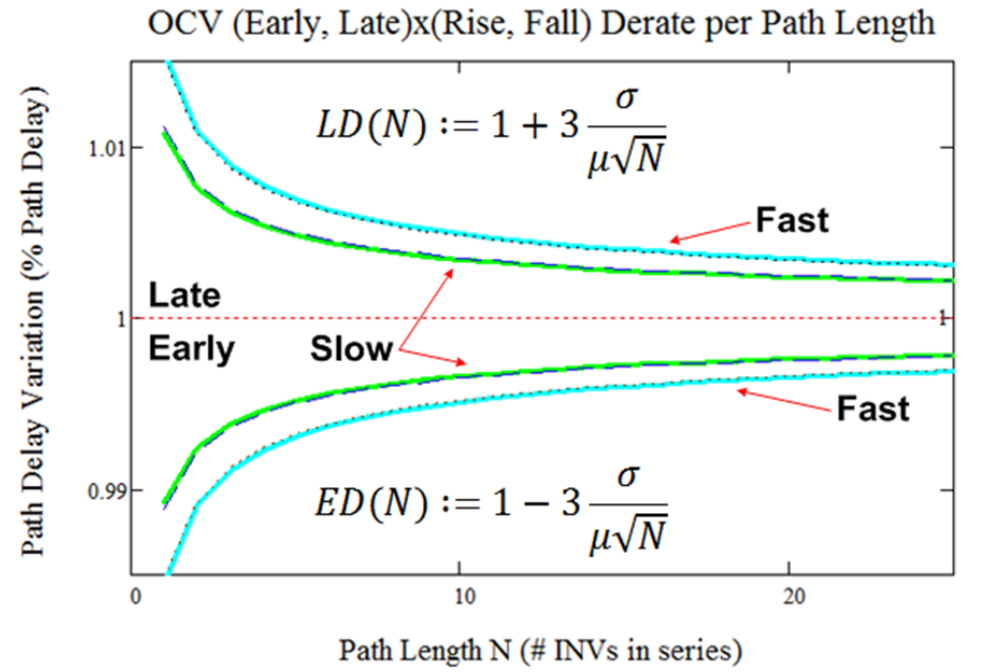


Example of Launch/Capture Clock & Data Paths

On-Chip Process Variation Methods

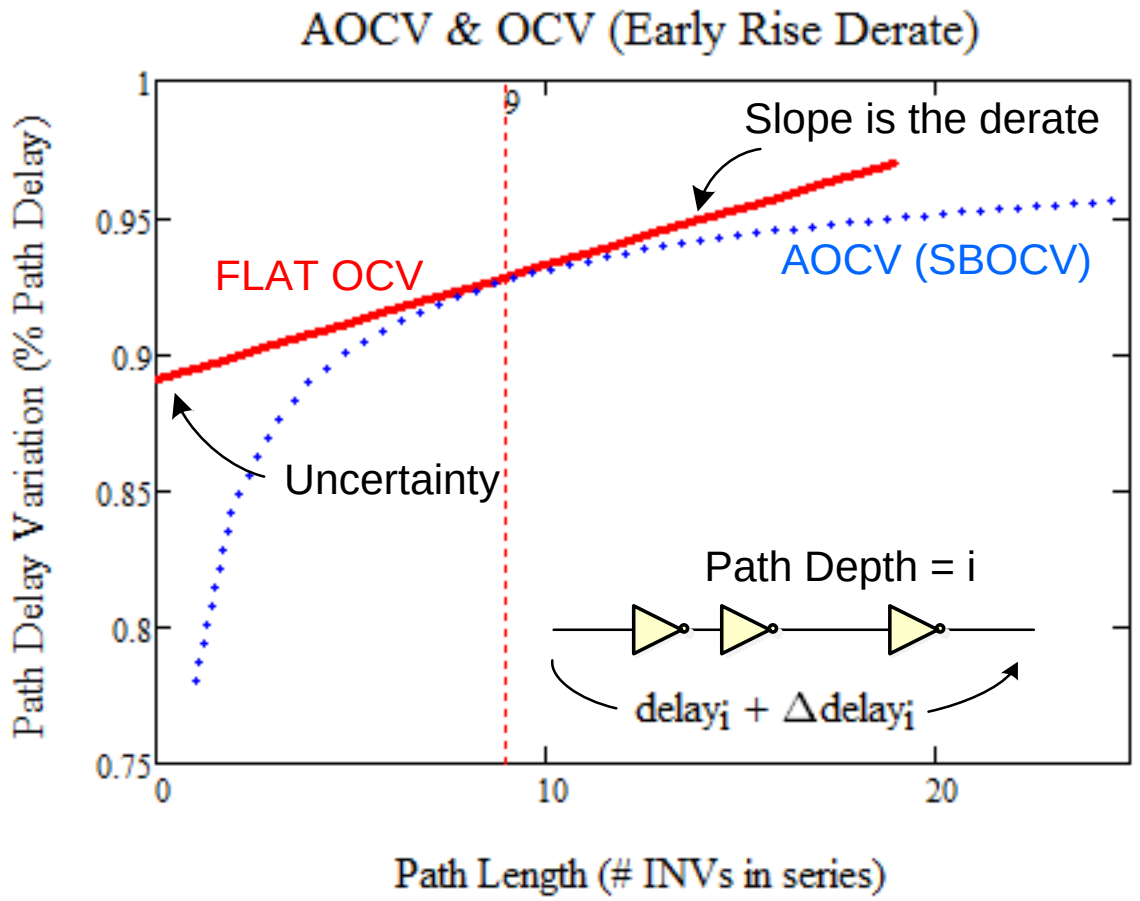
On-Chip Process Variation





- Statistical cancelation of process variation effects depends on logic-circuit path's stage depth.
- De-rates due to OCV therefore depend on # series-connected gates.

Advanced OCV (AOCV) vs FLAT OCV Path Delay



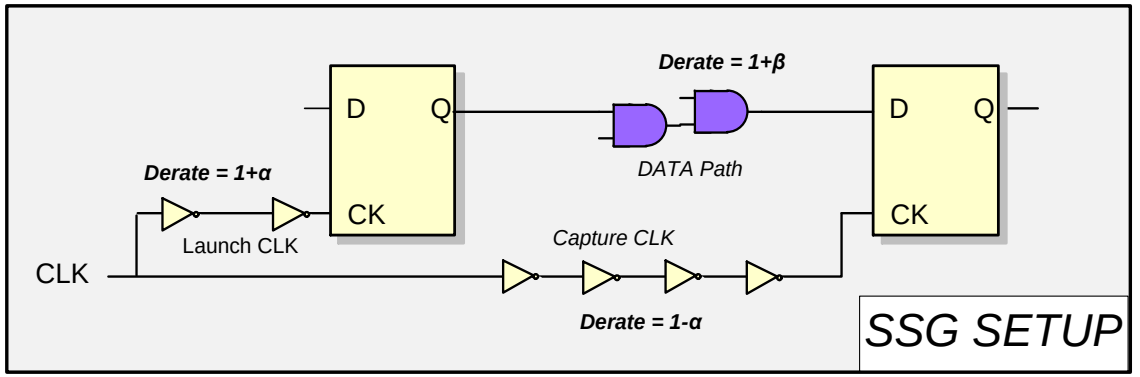
- Example of on-chip-process variation statistical cancelation on path delay for early, late de-rates for slow and fast corners.

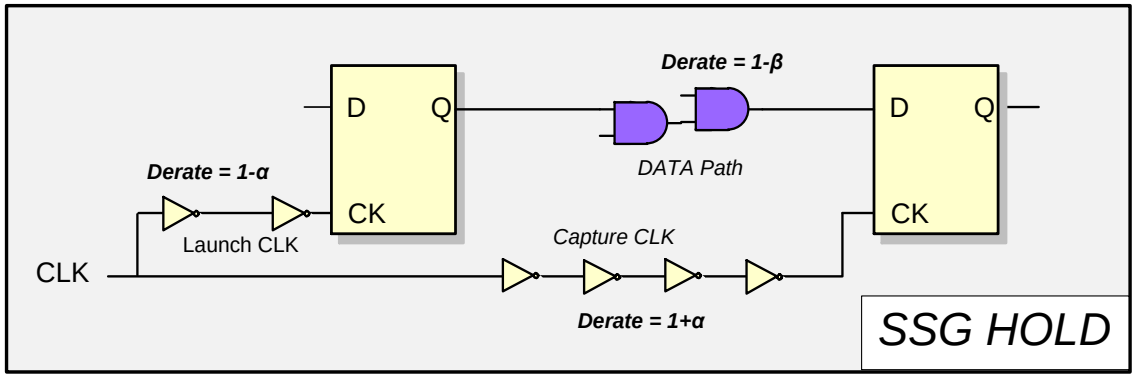
Flat OCV/AOCV Application

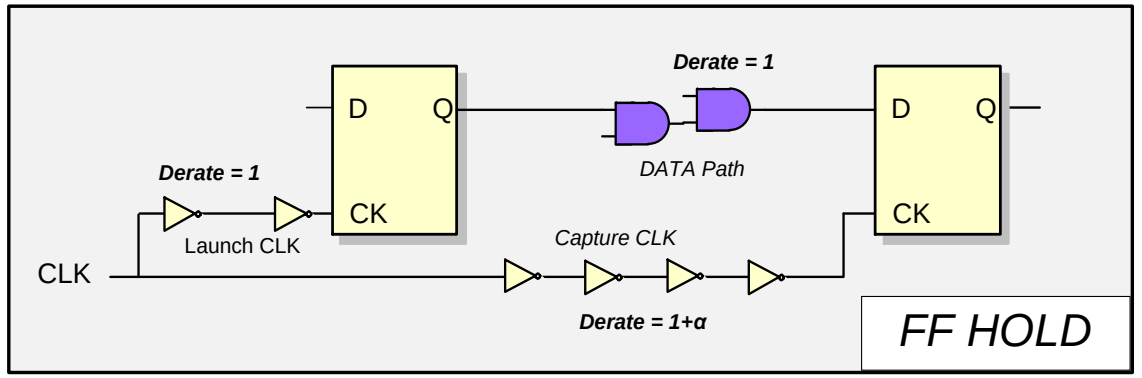
Process variation

- **Flat OCV STA recommend setting ****
  - **Setup (SSG)**
    - set_timing_derate –late –cell –clock (1+α)
    - set_timing_derate –late –cell –data (1+β)
    - set_timing_derate –early –cell (1-α)
  - **Hold (SSG)**
    - set_timing_derate –early –cell –clock (1-α)
    - set_timing_derate –early –cell –data (1-β)
    - set_timing_derate –late -cell (1+α)
  - **Hold (FF)**
    - set_timing_derate –late -cell (1+α)
- **AOCV STA recommend setting**
  - **Default given signoff PVT**
    - set timing_aocvm_enable_analysis #Enables AOCV analysis
    - set timing_aocvm_analysis_mode #Configures an AOCV analysis
    - set pba_aocvm_only_mode "" #Enables AOCV path-based analysis only
    - read_aocvm aocvm_file #Read AOCV derating tables from file.
  - **Additional setting for Hold (FF)**
    - set_timing_derate –early 1 –cell_delay #Launch Clock + Datapath

**** Note: α, β ≥ 0 represent clock- and data-OCV derate values, respectively**







Assumptions Used for OCV Generation for Vnom=0.9V

- Based on Synopsys TS28HPC library & c225-tsmc28hpc-1.8v/rel1.2 SPICE model
- PVT corner: SSG_0.81v_-40c & FF_0.99v_-40c
- Clock cells:

Device VT	Channel Length	Cell Height	Cell Name
HVT	35nm	7T	SVM_INV_S_2
SVT	35nm	7T	SVP_INV_S_2
LVT	35nm	7T	SVQ_INV_S_2
LVT	40nm	7T	SVJ_INV_S_2
LVT	30nm	7T	SVL_INV_S_2
eHVT	40nm	7T	SVD_INV_S_2
HVT	40nm	7T	SVF_INV_S_2
SVT	40nm	7T	SVG_INV_S_2

Data Cells:

Device VT	Channel Length	Cell Height	Cell Name
HVT	35nm	7T	SVM_INV_1
SVT	35nm	7T	SVP_INV_1
LVT	35nm	7T	SVQ_INV_1
LVT	40nm	7T	SVJ_INV_1
LVT	30nm	7T	SVL_INV_1
eHVT	40nm	7T	SVD_INV_1
HVT	40nm	7T	SVF_INV_1
SVT	40nm	7T	SVG_INV_1

- Max slew at SSG0.81Vn40C: 200ps for clock cells and 350ps for data cells for Flat OCV
- For AOCV ¼ max slew in delay table used
- IR drop (VDD-VSS variation) : 4 to 40mv
- OCV values based on assumptions different from the above may require larger de-rates. For example lower voltage corner, smaller cell, larger slew, larger IR drop
- No OCV sensitivity for track height was found, devices are sized far enough away from Wmin effects - these results for the 7T library can also be used for the 9T library

AOCV STA Application Note

- Extensive documentation for AOCV usage in Primetime can be found in the "Advanced On-Chip Variation Application Note" published in Solvnet (solvnet.synopsys.com):

https://solvnet.synopsys.com/retrieve/customer/application_notes/attached_files/019530/AOCVM_AppNote_6.0.pdf?1360132929551

Please note that some of the flows and attributes are optional.

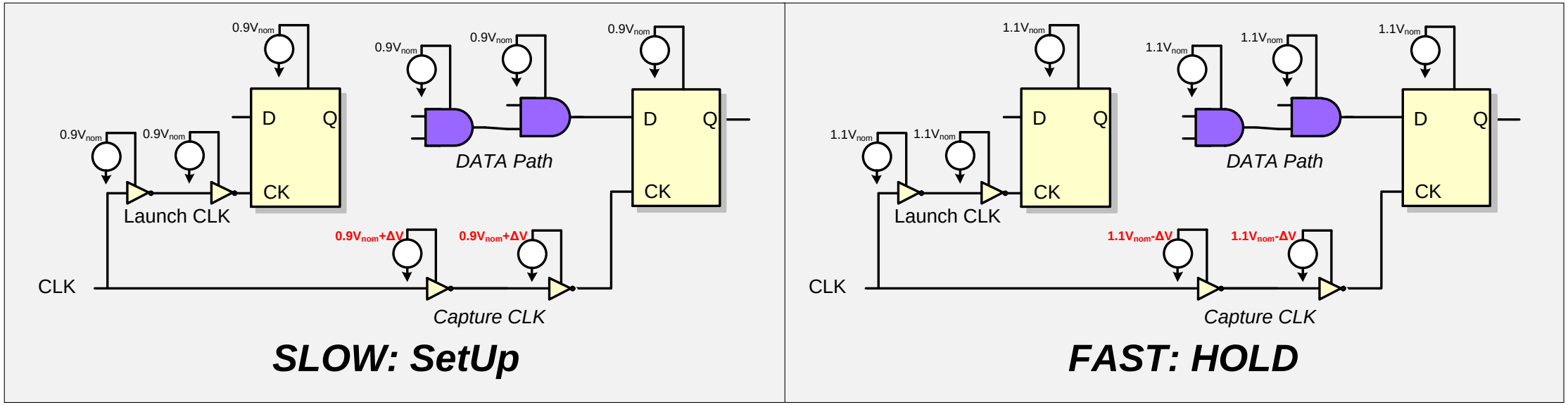
Summary of AOCV-related command in PrimeTime

```
set timing_aocvm_enable_analysis "" # Enables AOCV analysis
set timing_aocvm_analysis_mode "" # Configures an AOCV analysis
set pba_aocvm_only_mode "" # Enables AOCV path-based analysis only
read_aocvm aocvm_file # Read AOCV derating tables from an AOCV file
set_aocvm_coefficient # Specifies derating coefficient for AOCV
set_aocvm_table_group # Sets objects for named AOCV table set annotation
set_timing_derate -aocvm_guardband # Guard-banding in AOCV
report_aocvm # Reports AOCV deratings
report_timing_derate -aocvm_guardband # Reports AOCV guard-bands
report_timing –pba_mode # Path-based AOCV timing reports
get_timing_paths –pba_mode # Collection of path-based AOCV timing paths
write_binary_aocvm # Creates a binary AOCV file from an AOCV file
remove_aocvm # Removes AOCV information
reset_timing_derate -aocvm_guardband # Removes AOCV guard-bands
reset_aocvm_table_group # Resets the AOCV table set annotation for objects
```

On-Chip Voltage and Local Temperature Variation

Voltage/Temperature Variation Margin

- The voltage-supply variation is modeled as an identical supply difference between launch and capture paths applied through an additional flat derate to account for this launch- and capture-supply mismatch.
- IR-drop analysis should be checked against ΔV assumptions
- Temperature variation is measured by applying ΔT=10°C to all instances and observing delay differences.



3σ Voltage Variation Margin Table for Temperature=-40°C

Condition	ssg0p81V_-40								ff0p99V_-40							
Local ΔVdd (mV)	UHVT _INV_2		HVT _INV_2		SVT _INV_2		LVT _INV_2		UHVT _INV_2		HVT _INV_2		SVT _INV_2		LVT _INV_2	
	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
4	0.8%	0.8%	0.7%	0.9%	0.7%	0.8%	0.7%	0.8%	1.3%	1.3%	1.1%	1.1%	1.1%	1.1%	1.0%	1.1%
8	1.5%	1.5%	1.4%	1.4%	1.3%	1.3%	1.3%	1.2%	2.6%	2.4%	2.1%	2.0%	1.9%	1.7%	1.8%	1.7%
12	2.2%	2.1%	2.0%	2.0%	1.9%	1.9%	1.9%	1.7%	3.8%	3.5%	3.1%	2.9%	2.7%	2.5%	2.6%	2.5%
16	3.0%	2.8%	2.7%	2.6%	2.6%	2.5%	2.4%	2.3%	5.1%	4.6%	4.1%	3.8%	3.6%	3.3%	3.4%	3.2%
20	3.7%	3.5%	3.3%	3.3%	3.2%	3.0%	3.0%	2.8%	6.4%	5.8%	5.1%	4.7%	4.5%	4.1%	4.3%	3.9%
24	4.4%	4.2%	4.0%	3.9%	3.8%	3.6%	3.6%	3.4%	7.7%	7.0%	6.2%	5.7%	5.4%	4.9%	5.1%	4.7%
28	5.1%	4.9%	4.7%	4.5%	4.4%	4.2%	4.2%	3.9%	9.0%	8.2%	7.2%	6.6%	6.3%	5.7%	5.9%	5.5%
32	5.9%	5.6%	5.3%	5.2%	5.1%	4.8%	4.8%	4.5%	10.3%	9.3%	8.2%	7.6%	7.1%	6.5%	6.8%	6.2%
36	6.6%	6.3%	6.0%	5.8%	5.7%	5.4%	5.4%	5.0%	11.6%	10.5%	9.2%	8.5%	8.0%	7.3%	7.6%	7.0%
40	7.4%	7.0%	6.7%	6.5%	6.3%	6.0%	6.0%	5.6%	12.9%	11.7%	10.3%	9.5%	8.9%	8.1%	8.5%	7.8%

3σ Voltage Variation Margin Table for T=0°C and 125°C

Clock Cell and Operating Condition		Derate
SSG0p81V0C		%/mV
LVT40nm_7T_SVJ_INV_S_2	rise	0.1474%
	fall	0.1372%
SVT40nm_7T_SVG_INV_S_2	rise	0.1542%
	fall	0.1461%
HVT40nm_7T_SVF_INV_S_2	rise	0.1643%
	fall	0.1567%
UHVT40nm_7T_SVD_INV_S_2	rise	0.1794%
	fall	0.1716%
FF0p99V0C		%/mV
LVT40nm_7T_SVJ_INV_S_2	rise	0.2060%
	fall	0.1874%
SVT40nm_7T_SVG_INV_S_2	rise	0.2142%
	fall	0.1959%
HVT40nm_7T_SVF_INV_S_2	rise	0.2446%
	fall	0.2264%
UHVT40nm_7T_SVD_INV_S_2	rise	0.2962%
	fall	0.2724%

Clock Cell and Operating Condition		Derate
SSG0p81V125C		%/mV
LVT40nm_7T_SVJ_INV_S_2	rise	0.1394%
	fall	0.1325%
SVT40nm_7T_SVG_INV_S_2	rise	0.1433%
	fall	0.1357%
HVT40nm_7T_SVF_INV_S_2	rise	0.1505%
	fall	0.1439%
UHVT40nm_7T_SVD_INV_S_2	rise	0.1603%
	fall	0.1509%
FF0p99V125C		%/mV
LVT40nm_7T_SVJ_INV_S_2	rise	0.1927%
	fall	0.1796%
SVT40nm_7T_SVG_INV_S_2	rise	0.1932%
	fall	0.1790%
HVT40nm_7T_SVF_INV_S_2	rise	0.2135%
	fall	0.1986%
UHVT40nm_7T_SVD_INV_S_2	rise	0.2322%
	fall	0.2235%

Temperature Variation Margin Table

TSMC 28nm HPC				Temperature variation of 10C		Temperature variation of 10C		Temperature variation of 10C		Temperature variation of 10C		Temperature variation of 10C		Temperature variation of 10C	
				SSG0p81V-40C		FF0p99V-40C		SSG0p81V0C		FF0p99V0C		SSG0p81V125C		FF0p99V125C	
Library	VT	L (nm)	Cell Name	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
				σ/μ %	σ/μ %	σ/μ %	σ/μ %	σ/μ %	σ/μ %	σ/μ %	σ/μ %	σ/μ %	σ/μ %	σ/μ %	σ/μ %
ts28nchulogl40udl140f	UHVT	40	SVD_INV_S_2	3.71%	3.66%	0.50%	0.14%	2.99%	2.78%	0.43%	0.17%	1.87%	1.57%	0.05%	0.13%
ts28nchhlogl35udl140f	HVT	35	SVM_INV_S_2	2.06%	2.09%	0.11%	0.02%	1.76%	1.92%	0.09%	0.02%	1.10%	1.22%	0.05%	0.13%
ts28nchhlogl40udl140f	HVT	40	SVF_INV_S_2	2.06%	1.97%	0.02%	0.09%	1.82%	1.67%	0.03%	0.03%	1.03%	1.14%	0.09%	0.12%
ts28nchllogl30udl140f	LVT	30	SVL_INV_S_2	1.45%	1.76%	0.18%	0.09%	1.11%	1.42%	0.05%	0.03%	0.51%	0.81%	0.54%	0.13%
ts28nchllogl35udl140f	LVT	35	SVQ_INV_S_2	1.25%	1.35%	0.02%	0.09%	0.99%	1.08%	0.14%	0.16%	0.35%	0.62%	0.56%	0.24%
ts28nchllogl40udl140f	LVT	40	SVJ_INV_S_2	1.15%	1.25%	0.13%	0.34%	0.90%	1.13%	0.26%	0.19%	0.54%	0.53%	0.61%	0.34%
ts28nchslogl35udl140f	SVT	35	SVP_INV_S_2	1.59%	1.65%	0.09%	0.00%	1.43%	1.48%	0.02%	0.05%	1.15%	1.04%	0.39%	0.14%
ts28nchslogl40udl140f	SVT	40	SVG_INV_S_2	1.65%	1.52%	0.02%	0.18%	1.45%	1.30%	0.03%	0.10%	1.14%	1.02%	0.38%	0.17%

Flat OCV Application STA Recommended Settings

Voltage & Temperature Variation

- Setup (SSG) **
  - –[STA] set_timing_derate –early –cell –clock (1-α)
- Hold (FF)
  - –[STA] set_timing_derate –late –cell –clock (1+α)

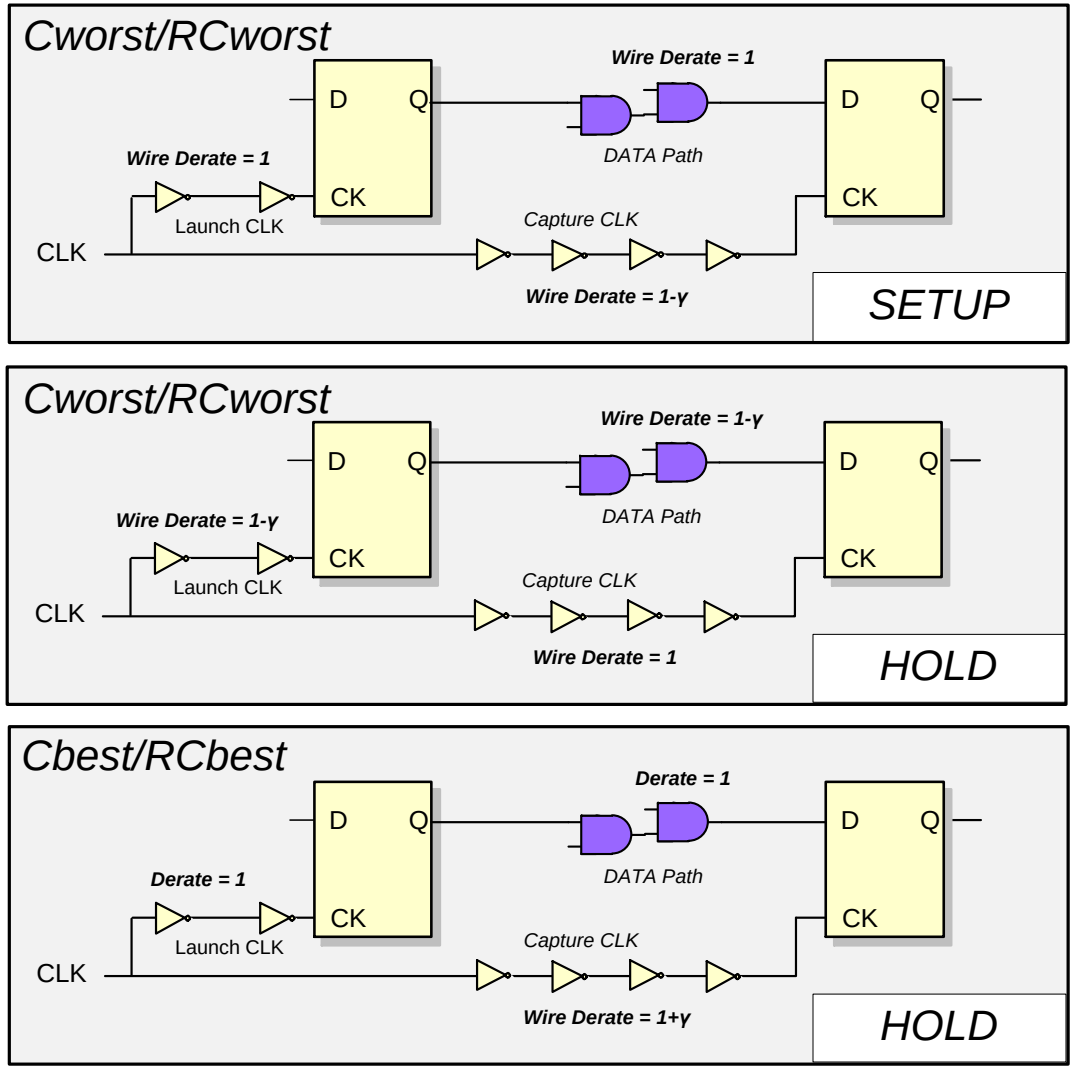
**** Note: α ≥ 0 represent clock derate values.**

On-Chip Wire Variation

On-Chip-Wire Variation for Total-RC Corner

- Apply wire OCV on one side because another side is already fastest/slowest
- Setup (Cworst/RCworst)
  - [STA] set_timing_derate –late –net –clock 1
  - [STA] set_timing_derate –late –net –data 1
  - [STA] set_timing_derate –early –net (1- γ)
- Hold (Cworst/RCworst)
  - [STA] set_timing_derate –early –net –clock (1- γ)
  - [STA] set_timing_derate –early –net –data (1- γ)
  - [STA] set_timing_derate –late –net 1
- Hold (Cbest/RCbest)
  - [STA] set_timing_derate –early –net –clock 1
  - [STA] set_timing_derate –early –net –data 1
  - [STA] set_timing_derate –late –net (1+γ)

**** Note: γ = 8.5% for TS28HPC process**

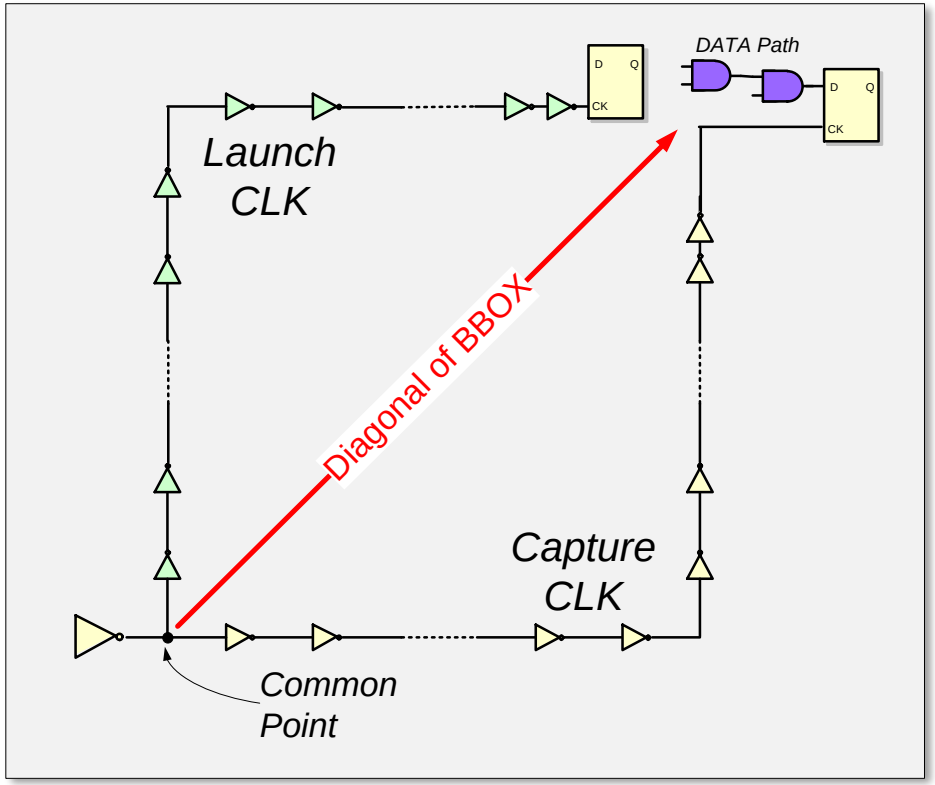


On-Chip Spatial Margin

Spatial Variation Margin (if applicable)

- Spatial Variation Margin (SVM) is added as a flat-OVC or AOCV when the diagonal of a bounding box enclosing the timing path is > 5mm. (See Diagram)
  - **SSG Early:** (OCV_{EARLY} ***or*** AOCV) – ½×$OCV_{SPATIAL}$
  - **SSG Late:** (OCV_{LATE} ***or*** AOCV) + ½×$OCV_{SPATIAL}$
  - **FF Late:** (OCV_{LATE} ***or*** AOCV) + $OCV_{SPATIAL}$

Diagnal of bbox	Spatial de-rate
bbox<5mm	0%
5mm ≤ bbox < 10mm	1.50%
10mm ≤ bbox	2.50%



- **Example: for a diagonal box 6mm, 28HPC**
  - SSG capture clock derate = -4.6% - ½*1.5% = -5.35%
  - SSG launch clock derate = +4.6% + ½*1.5% = 5.35%
  - SSG data derate = 6.3% + ½*1.5% = 7.05%

**AOCV spatial to be supported with AOCV 2.0

Register Constraint Margin for Local-Process Variation

Register Constraint Margin for Local-Process Variation

- **Setup time uncertainty**
  - Margin = clock jitter.

- **Hold time uncertainty**
  1. Use FLAT hold-constraint uncertainty margin**

     Example:

     set_clock_uncertainty -hold <flat hold margin> [get_pins -of [get_cells -hier -filter "ref_name =~ *ULVT*"] -filter "is_clock_pin == true"]

     OR

  2. Use hold constraint table in liberty [Please contact SNPS for details and PVT availability]

****Cell & pin based uncertainty will be overwritten by inter-clock uncertainty**

Chip Sign-off Corners

Chip Sign-Off Corners

TS28HPC, Vnom=0.9V

Timing Check	Library PVT Conditions	Chip Level RC Corner	FLAT OCV and Design Margin
Setup	SSG/0.81V/125C	Cworst	+4.6% on launch clock path, +6.3% on data path and -4.6% on capture path, -8.5% on capture net, and clock jitter +25ps setup margin.
		RCworst	
	SSG/0.81V/-40C	Cworst	
		RCworst	
Hold	SSG/0.81V/125C	Cworst	-5.5% on launch clock path, -8.2% on data path and +5.5% on capture path, -8.5% on launch clock net, -8.5% on data net, and +70ps hold margin
		RCworst	
	SSG/0.81V/-40C	Cworst	
		RCworst	
	FF/0.99V/125C	Cworst	+8.7% on capture cell, -8.5% on launch clock net, -8.5% on data net, and +50ps hold margin
		RCworst	
	FF/0.99V/-40C	Cworst	
		RCworst	
	FF/0.99V/125C	Cbest	+8.7% on capture cell, +8.5 on capture net, and +50ps hold margin
		RCbest	
	FF/0.99V/-40C	Cbest	
		RCbest	

