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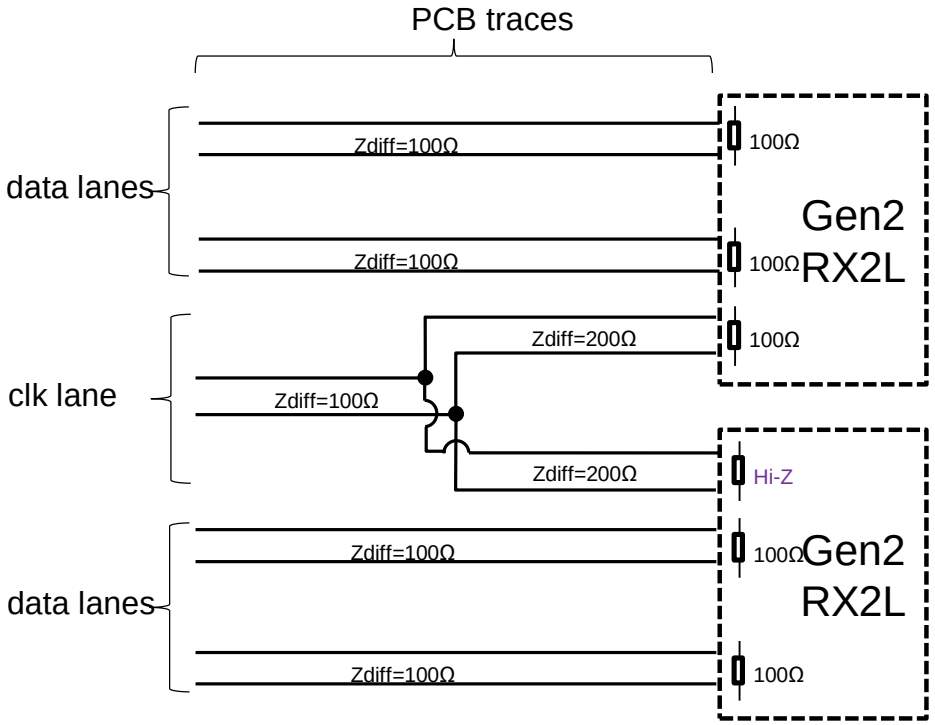
Dual RX DPHY GEN2 Aggregation: 2 x RX2L → 1 x RX4L

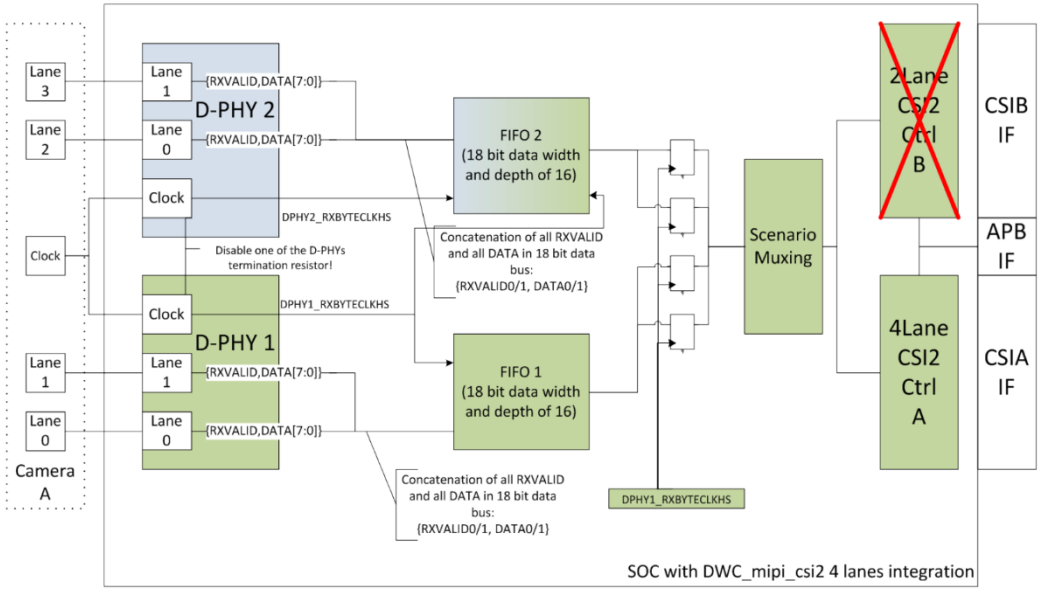
PCB Implementation

Gen2 DPHY Implementation

for 2 x RX2L → 1 x RX4L application scenario

- Two independent RX clock lanes used, single TX clock lane source
  - Silicon validated in-house and by customer on previous DPHY Generation (Gen2)
  - Input DDR clock is provided to two clock lanes





Previous DPHY generation – silicon validated

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Package Implementation

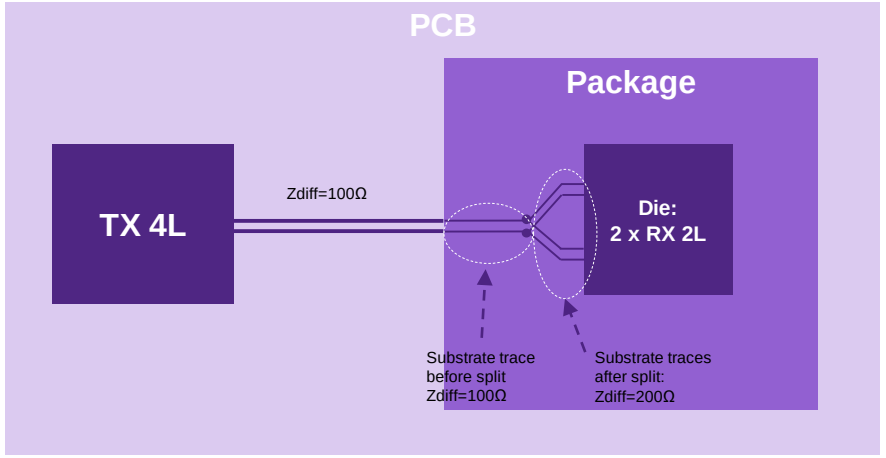
Workaround

- Adds PCB complexity and cost
  - Sets an inferior limit on cost efficiency of PCB: 200Ohm differential impedance translates to
    - Thin line width
    - Additional layer for thicker dielectric between signal plane and ground plane
    - Large line space
  - Needs careful analysis on SI issues
    - Clock Jitter → PHY performance
    - EMI
    - Noise
    - Cross-talk
- Consideration of cost efficiency may impede dual RX aggregation in practice

Package Implementation

Workaround

- Split clock lane on package substrate instead
  - Concept:
    - 100Ω differential impedance clock lane on PCB
    - Clock lane split to two 200Ω differential impedance traces for matched impedance
  - Pros: reduced PCB complexity and cost
  - Cons: increased package complexity and cost



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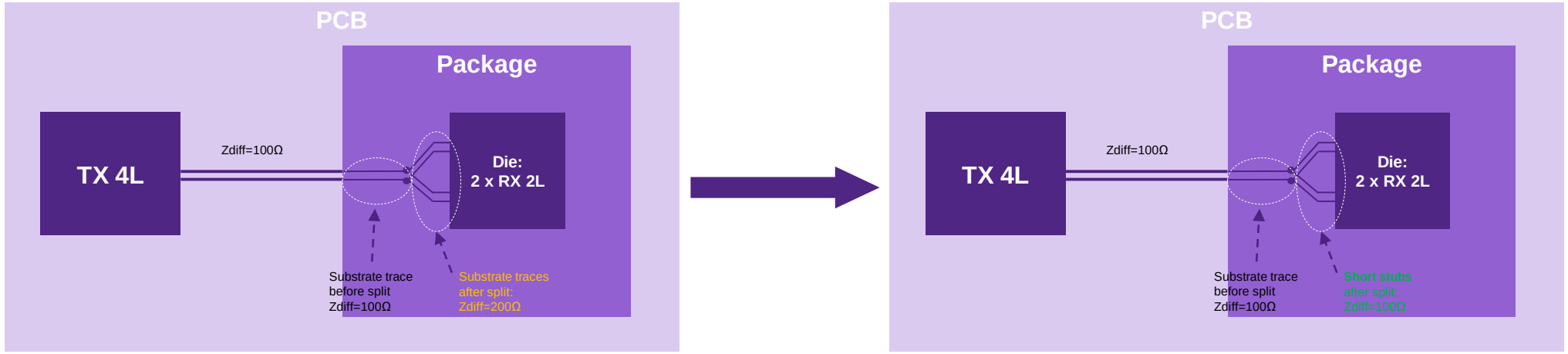
Package Implementation

Workaround

- To reduce complexity/cost furthermore
  - 200Ω differential impedance can be optional, if a stub < 5mm after clock split point
  - No showstopper impact is expected based on first-order analysis
  - SI simulation is still mandatory to give pass/fail result for assessment of IP performance



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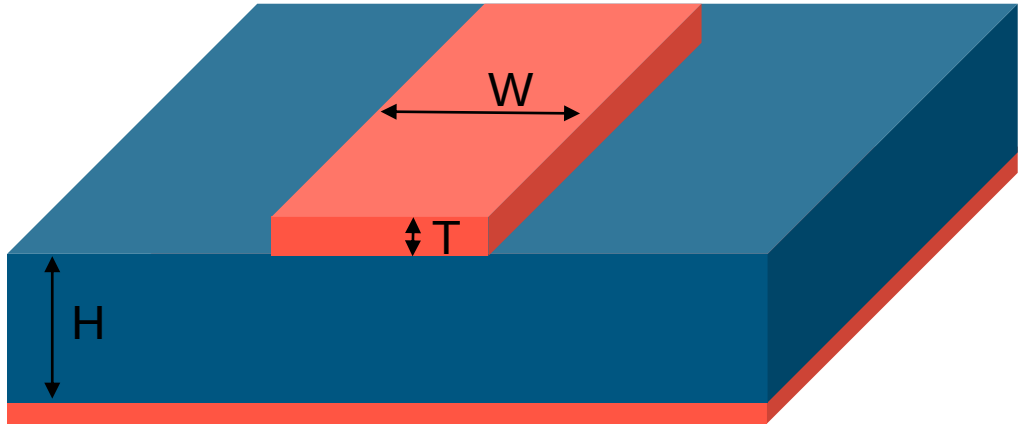
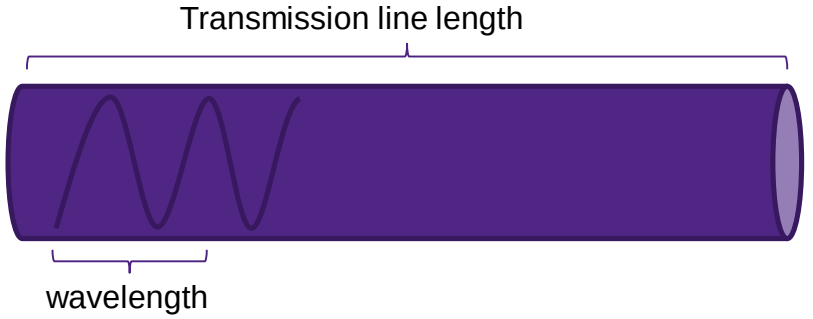
First-order Analysis

Impact of short stub



- Example: FR4 dielectric constant = 4.5
- tpd = $\frac{\sqrt{4.5}}{3\times10^{8}}$ = 7.07 ns/m
- In a typical microstrip configuration the dielectric constant is a “mix” between $\boldsymbol{\varepsilon_{air} = 1}$ and $\boldsymbol{\varepsilon r = 4.5}$

- In a typical transmission line the phase of the signal is not constant across the path:
  - signal wavelength << line length
  - There is a finite velocity for the propagation of the signal, usually specified as the propagation delay:
    - tpd = $\frac{\sqrt{\boldsymbol{\varepsilon} r}}{c}$, c = velocity of light
    - There is a characteristic impedance of the line that is “seen” by the signal. This impedance is real (purely resistive) and depends on the geometry of the lines.



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First-order Analysis

Impact of short stub

- Transmission lines can be simplified into a discrete element if the length is “electrically small”, i.e. the signal phase is constant across the element
  - Criteria 1 – **Rule of thumb** – stub should be smaller that ¼ wavelength of fmax (fmax up to 5th harmonic for high speed serial links):
    - Example: fclk= 0.75GHz → fmax = 3.75Ghz → period = 0.266ns
    - tpd = 5.6 ns/m
    - ¼ wavelength = 0.266/(4*5.6) = 11.8 mm
  - Criteria 2 – **Conservative estimate** – stub should be smaller than $^{1}/_{16}$ of signal “risetime”
    - Example: fclk= 0.75GHz → risetime = 333ps
    - tpd = 5.6 ns/m
    - risetime “length” = 0.333/5.6 = 59.6mm
    - 1/16 of risetime “length” = 3.7mm

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Thank You


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