Integration Design Reviews

Synopsys

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Integration Review Services Overview

- Offered by Synopsys as part of the Standard Core Support
- Visual implementation reviews focused on helping the customer improve the odds of SOC success
- Synopsys recommends customers to include time for the Reviews on their planning as they typically allow early detection of the most typical customer pitfalls
- Integration Review Services:

Logical Integration Review	Package Review
Post P&R Static Timing Review	PCB Review
GDS Physical Integration Review	ASIC level ESD Review
Reference Clock Review	

Process

Trigger

- Customer submits a SolvNet case requesting an Integration Review and uploads the necessary files

Offline Review

- Synopsys carefully reviews the data and provides review comments to customer

Final Review (Optionally Live)

- After customer implementation of the Offline Review recommendations a final review is carried to ensure all items were properly addressed
- Typical ETA: 5 to 7 business days

Logical Review

- **Prerequisite**
  - Verilog compiles successfully
  - At least 1 simulation test should have run successfully
- **Customer provides**
  - PHY + Controller integrated wrapper (showing connectivity)
  - Simulator Compile log / Synthesis log
  - PHY Parameter settings
  - VCD/VPD/FSDB waveforms for 1 simulation test run
- **Synopsys checklist**
  - run the recommended VTB tests provided in the controller package
  - PHY simulation model been integrated and tests passed
  - synthesis scripts about clock definitions and constraints
  - testability requirements are met

Post P&R Static Timing Review

- **Prerequisite**
  - Synthesis & PnR of SoftIPs complete
  - STA performed with IP timing models
- **Customer provides**
  - SDC file(s) for both functional and scan test mode
  - Verbose format timing reports of all violations
    - Switches to be used: “-capacitance”, “-transition_time”, “-full_clock_expanded”
    - Across all applicable PVT corners
- **Synopsys Checklist**
  - Timing closure
  - Any hold violation
  - Isolation cells/Bypass muxes on the PHY
  - Clock tree jitter on the reference clock and clock from the PHY

GDS Physical Integration Review

- **Prerequisite**
  - Physical integration of hard macro/IOs complete
  - DRC/LVS clean
- **Customer provides**
  - Completed Integration checklist
  - Integrated GDS (PHY + PADs)
  - Any custom modifications to PADs.
  - Snapshot of the placement of the hardmacro and soft-macro and I/Os.
- **Synopsys checklist**
  - Isolated powers and grounds
  - Clamp within ½ W of anti-parallel diodes
  - ESD/CDM protection on ASIC side pins
  - Minimum spacing to the PHY is met
  - JTAG access
  - Clock routing if alternate input is used
  - Understanding any XOR differences with the delivered GDS
  - Ref Clk Implementation.
  - Power / Ground Connection.

Package Review

- **Prerequisite**
  - Package layout with the PHY has been completed
  - Customer is able to bring up and display the package database
- **Customer provides**
  - Package file information in machine readable format such as Allegro MCM as well as the stack up and signal IO list for visual review
  - Signal Integrity analysis for TX, RX, and refclk signals
  - Power Distribution Network (PDN) Analysis for all supplies, checked against noise limits
- **Synopsys checklist**
  - Power Supply and Ground Connection
  - Impedance on high-speed data lines: 100Ohm differential
  - Reference Clock routing: Visual inspection of the reference clock routing to the PHY.
  - Crosstalk due to signal routing

Reference Clock Review

- **Prerequisite**
  - For reference clock in star package configuration
    - Package layout with the PHY has been completed
  - For reference clock with on-die distribution
    - Package layout with the PHY has been completed
    - On-die clock distribution implementation is completed
- **Customer provides**
  - Reference clock network diagram (schematic or sketch)
  - SPICE signal integrity simulation of refclk distribution
  - SPICE simulation and budgeting of additive jitter from buffers used in on-die distribution (if applicable)
- **Synopsys checklist**
  - Visual inspection of the reference clock routing to the PHY, including matching between differential signals
  - Review of additive jitter from on-due distribution (if applicable)
  - Review of reference clock signal integrity against specification requirements

PCB Review

- **Prerequisite**
  - Package layout with the PHY has been completed.
  - Customer is able to bring up and display the package database.
- **Customer provides**
  - schematics and PCB layout (BRD files) that will enable visual review of their system.
- **Synopsys checklist**
  - AC-coupling capacitors
  - Isolated power
  - Common ground
  - Reference resistor has been placed
  - JTAG pins brought out for test or debug
  - Reference clock
  - Power supply decoupling

ASIC Level ESD Review

- **Prerequisite**
  - Physical integration of all IPs complete
  - DRC/LVS clean
- **Customer provides**
  - ESD methodology and design diagram
- **Synopsys checklist**
  - IP IO Cross-domain protections
  - SoC ESD-ground


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