21 April 2017

Song Pan
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20000 Shanghai
China

Dear Song Pan:

In response to your request, the following JEDEC Manufacturer ID number has been assigned to your company:

47 decimal (bank 10)
0010 1111 binary
2F hex

This number is the next consecutive number on the list of numbers assigned to the system set-up by the JC-42 Committee on Memory devices of JEDEC and published in JEDEC Publication 106. The number is the next consecutive decimal number on the list. Your number is in bank 10. Note that there are 1134 numbers before you in banks one, two, three, four, five, six, seven, eight and nine. Your number is nine bytes of continuation code followed by the number itself. The continuation code is: 0111 1111 or 7F hex.

The binary is derived from the decimal and the parity bit (odd parity) added to it. The hex number comes from the binary including the parity; therefore, the numbers are not always directly convertible. A list of other numbers is attached for your information.

It should be noted that JTAG code described in IEEE-1149.1 standard is used a bit differently from the way JEDEC had originally intended these codes. The JEDEC number was originally created solely for EPROM manufacturers and the JTAG number was created for testing a wide range of items. The JEDEC number is now used in SPD for memory modules. Even though the use of the codes has changed over the years, it still works well in its original form. When using the number for JTAG, it is different in that it is an 11-bit number and the JEDEC one is 8-bits. Please see the attached JTAG information to find out how they use the other 3-bits.

Best regards,
Phileasher Tanner

JEDEC Manufacturer's ID Code

The JEDEC ID code has been in use since 1983 when JEP106 was first published. Over the years, it has been used in different ways for different purposes. It started out as something that could be read by an EPROM programming machine to read company names off a particular chip plugged into the machine. In later years, JTAG adopted it into their 1149.1 spec. JEDEC has also included it in their serial presence detect (SPD) used in memory modules. See descriptions below on different applications of the code for different uses.

IEEE 1149.1 JTAG Conversion

The JEDEC code in JEP106 and the IEEE 1149.1 JTAG Manufacturer's ID differ. This is an explanation of how they are different and how to do the conversions.

While the JEDEC code is shown decimal, binary and hex, most memory people use it as a hex number. Since the codes are assigned in banks of 126 numbers each, there are continuation codes that are used to separate them into their correct bank. Let's compare some similar codes and examine how they look different in different banks. Decimal code 14 in bank one is Motorola, decimal code 14 in bank 2 is VideoLogic, decimal code 14 in bank 3 is Novanet Semiconductor. The hex number for decimal code 14 is 0E. So the hex JEDEC code for Motorola is 0E, for Videologic it is 7F0E and for Novanet Semiconductor it is 7F7F0E.

The IEEE 1149.1 number uses the JEDEC ID Code as a binary number (not decimal) and modifies it. The JEDEC binary number is 8 bits odd parity, but the IEEE 1149.1 number is 11 bits. The JEDEC 8 bit number is modified in that the parity bit (MSB) is dropped, making 7 bits, and then four bits are added in front of that. The four bits added are used to indicate in binary which bank your code is in. So going back to our earlier examples above, the JEDEC binary number for Motorola is 00001110 in bank one. Converting this to IEEE 1149.1 would be 0001110 plus 0000 making 00000001110.

VideoLogic has the same binary code, but is in bank two, so the IEEE 1149.1 code for them is 0001110 plus 0001 making 00010001110. Novanet Semiconductor has the same binary code, but is in bank three, so the IEEE 1149.1 code for them is 0001110 plus 0010 making 00100001110.

JEDEC is now in bank ten, so the four bits added to the number are 1001.

Updated April 2016

DDR2 Memory Modules

The format in DDR2 did not easily accommodate bank numbers. This is the format as it was described for DDR2 SPDs:

Bytes 64-71: Module Manufacturer's JEDEC ID Code

Manufacturers of a given module may include their identifier according to JEDEC spec JEP106. The first byte is utilized, the second byte is filled with zeros. For example, a company whose value is hexadecimal CE would be coded as: "CE000000 00000000."

DDR3 and DDR 4 Memory Modules

For DDR3 modules, the format was updated to have two bytes clearly assigned. One byte is used to describe the ID code and the other byte is used to describe the bank number. Byte 118 is the ID code and Byte 117 is the bank number per the JEDEC SPD document:

Byte 117: Module Manufacturer ID Code, Least Significant Byte
Byte 118: Module Manufacturer ID Code, Most Significant Byte

This two-byte field indicates the manufacturer of the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

Byte 118, Bits 7 ~ 0	Byte 117, Bit 7	Byte 117, Bits 6 ~ 0
Last non-zero byte, Module Manufacturer	Odd Parity for Byte 117, bits 6 ~ 0	Number of continuation codes, Module Manufacturer
See JEP-106		See JEP-106

Examples:

Company	JEP-106		# continuation codes	SPD	
	Bank	Code		Byte 117	Byte 118
Fujitsu	1	04	0	0x80	0x04
US Modular	5	A8	4	0x04	0xA8

Codes assigned in bank ten (10) need nine (9) continuation codes for Byte 117, or 0001001 in bits 6~0.

In bank 10, you will need to add a 1 in bit 7 of Byte 117 to make it odd parity.

NOTE-The supplementary identification code is required only in cases where the component cannot be reprogrammed through the test logic defined by this standard. In cases where such reprogramming is possible, the ATE or master device controlling the operation of the component can ensure that it is programmed to the correct state at the start of the test sequence.

Since the bypass register (which is selected in the absence of a device identification register by the instruction loaded in the *Test-Logic-Reset* controller state) loads a logic 0 at the start of a scan cycle, whereas a device identification register will load a constant logic l into its LSB, examination of the first bit of data shifted out of a component during a test data scan sequence immediately following exit from the *Test-Logic-Reset* controller state will show whether a device identification register is included in the design.

A requirement of the *IDCODE* and *USERCODE* instructions is that, when they are used, the on-chip system logic shall continue its normal operation undisturbed. Rule 11.1.1b is included so that this requirement can be met. Note, however, that provided rule 11.1.1b is met, the shift-register stages may be shared resources used by several of the registers defined by this standard and also by any design-specific test data register.

11.2 Manufacturer Identity Code

11.2.1. Specifications

Rules

(a) The manufacturer identity code shall be a compressed form of the JEDEC Publication 106 [1][i] generated from the JEDEC (the Joint Electron Device Engineering Council) code as follows:

(i) Identification code bits 7·1. The seven LSBs are derived from the last byte of the JEDEC code by discarding the parity bit.

(ii) Identification code bits 11-8. The four MSBs provide a binary count of the number of bytes in the JEDEC code that contain the continuation character (hex 7F). Where the number of continuation characters exceeds 15, these four bits contain the modulo-16 count of the number of continuation characters.

(b) The manufacturer code 00001111111 shall not be used in components that are otherwise compatible with this standard.

Recommendations

(c) Where the component is an application-specific integrated circuit (ASIC), the manufacturer ID code should be that of the manufacturer of the component, rather than that of the designer.

11.2.2 Description

This scheme utilizes the manufacturer coding scheme administered by JEDEC.

[i]The number in brackets refers to those of the references listed in section 2.4.