The guideline of test vector generation

--for design engineer reference

Version 1.2

History

Rev	Revision History	Author	Date
0.0	Initial version	Athlon Zhang	May/05
1.0	Updated	Athlon Zhang	Aug/08
1.1	Update	Athlon Zhang	2/12/10
1.2	Update PLL enable pattern generation, PLL reset	Athlon Zhang	8/27/10
1.3	Update Spread Spectrum & PLL lock signal	Athlon Zhang	2010-9-10

1. **Title: Test guideline of test vector generation**
2. **Purpose**

   To define verisilicon function VCD file and Scan WGL/STIL format convert to test pattern flow.
3. **Scope**

This specification is applicable to all test pattern conversion of VeriSilicon turnkey projects.

4. Responsibility to generate test pattern

Front end design engineers are responsible for generate VCD/WGL/STIL simulation file, test engineers are responsible for convert simulation files to ATE tester vectors and generate test program.

5. Functional pattern Generate Guideline

VCD/EVCD files consist of device functional behavior. When generate VCD/EVCD files notice the following:

5.1. Cycle-based or WGL format function pattern is prefer, which can save debug time and avoid pattern conversion error.

5.2. Use several VCD files instead of one large VCD. Each VCD file will be translated to one tester pattern.

5.3. Only device external signals (top module) need to appear in the VCD, exclude power and ground pins.

5.4. Please only list output pins need to compared, this saves pattern conversion/ debug time.

5.5. For IO signals, make sure that the VCD also contains IO control signals. IO control signals are internal device signals, each IO signal should have a control signal to specify whether the IO signal is an input or an output at each point in the test., please specify output status when IO control signal equals 0 or 1.

5.6. The pins name and number should be consistent in all the Pattern (VCD and WGL).

5.7. There must not have any artificial jitter in the signal for the hardware limitation of tester.

5.8. For the input pins or io pins are in input mode, there must not have X state, replace X to Z if you have X.

5.9. For the output pins or io pins are in output mode, there must not have Z state, replace Z to X if you have Z.

5.10. There must not have any power pins in the pattern.

5.11. For the pins not used in the test, give them a logical 1 or logical 0; don't let them in float state.

5.12. EVCD file do not need to dump IO control signal.

5.13. If PLL output needs to compare, please set PLL by pass to avoid output shift due to different PLL lock time, or input stimulus until PLL is locked.

5.14. Avoid reset signal go through PLL. or input stimulus until PLL is locked

5.15. For VeriSilicon PLL, avoid use PLL lock time to trig reset as even in PLL bypass mode, Lock time is still available

5.16. If Spread Spectrum PLL is used, bypass mode has to be enable in the chip design

5.17. Signals/ clock need to be synchronized.

5.18. Please specify if there's multi-clock domain, set different clock period at same lease common multiple if possible.

5.19. The entire pattern should be delivered to Verisilicon at least three weeks before the conversion.