Introduction to Mali-V61

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Media Processing Group

Mali Video

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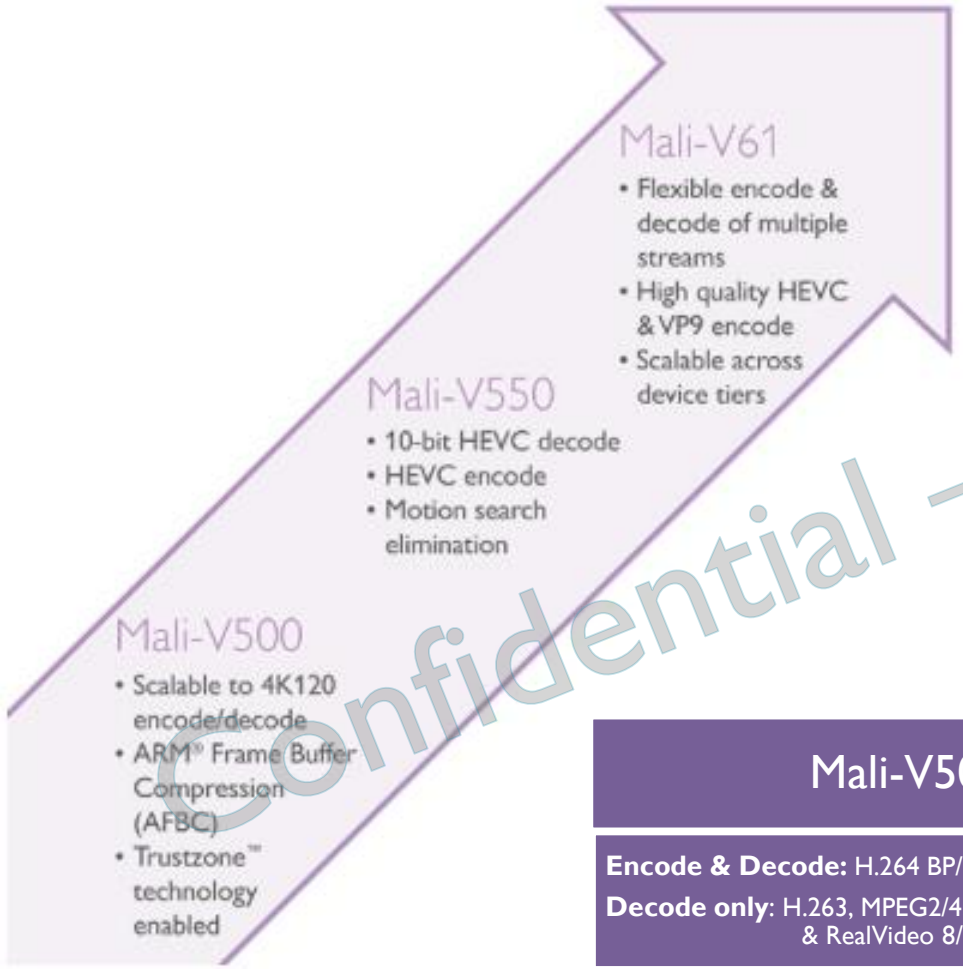
November 2016

Mali-V550 & Mali-V500

Current Video IP

Mali Video products

Flexible video IP for 'freedom of use'



- Multi-core, multi-codec, scalable solution
  - Single core supports 1080p60 pixel throughput (28HPM@600 MHz)
  - 4 cores support 4K60, 8 cores support 4K120
- Smallest area multi-standard codec, (28HPM)
  - Mali-V500: 1080p60 8-bit decode <1mm^2
  - Mali-V550: 1080p60 8-bit decode <1.3mm^2
  - Mali-V61: 1080p60 10-bit decode <1.6mm^2
- AFBC yields ~35% lower in-video bandwidth
- Integrated Android stack
  - Optimised for Mali Display, GPU and Video

Mali-V500	Mali-V550	Mali-V61
Encode & Decode: H.264 BP/MP/HP & VP8 **Decode only**: H.263, MPEG2/4, VC-1, DivX 4/5/6 & RealVideo 8/9/10	**Adds:** HEVC Main 10 Decode, HEVC Main Encode (Lite) Baseline JPEG Compliant	**Adds:** Full HEVC Main10 Encode VP9 10-bit P2 & 8-bit P0 Encode VP9 10-bit P2 & 8-bit P0 Decode

Mali-V550 PPA Estimates (28 HPM)

Operating Point	Cores	Freq (MHz)	8-bit V550 (mm^2)	10-bit V550 (mm^2)	Typ Encode Power (mW)	Typ Decode Power (mW)
1080p60	1	600	1.5 (1.3)	1.6 (1.4)	79	43
4K30 (2160p30)	2	600	2.9 (2.5)	3.0 (2.6)	158	86
4K60 (2160p60)	4	600	5.5 (4.8)	6.0 (5.2)	316	172

- Mali-V550 Decode only area numbers shown in brackets
- C35 transistor, 9 track library, 7-metal layers, SVT cells only, 600MHz timing closure, ~80% utilization
- Power data is for 28HPM, 85C, 0.9v, dynamic power only, gate level netlist simulation, measured on one stream using HEVC on a Mali-V550 MP1
  - Stream used is Tractor 1920x1080 with IPB frame pattern for decode and IPP pattern for encode
- Power numbers for MP2 & MP4 configurations are indicative, based on linear scaling of MP1 numbers

Mali-V500 PPA Estimates (28 HPM)

Operating Point	Cores	Freq (MHz)	Mali-V500 En/Decode (mm^2)	Mali-V500 Decode only (mm^2)	Typ Encode Power (mW)	Typ Decode Power (mW)
1080p60	1	600	1.14	0.97	78	62
4K30 (2160p30)	2	600	2.10	1.78	156	124
4K60 (2160p60)	4	600	4.22	3.42	312	248

- C35 transistor, 9 track library, 7-metal layers, SVT cells only, 600MHz timing closure, ~85% utilization
- Power data is for 28HPM, 85C, 0.9v, dynamic power only, gate level netlist simulation, measured on one stream using HEVC on a Mali-V500 MP1
- Power numbers for MP2 & MP4 configurations are indicative, based on linear scaling of MP1 numbers

Mali-V5x0 source and output frame formats

Format	VDMA Spec	Alias	Bit Depth	YUV	Planes	Mali-V500		Mali-V550	
						Dec	Enc	Dec	Enc
YUV420AFBC			8	420	AFBC	x	-	x	-
YUV420AFBC_10b			10	420	AFBC	-	-	x	-
YUV422AFBC			8	422	AFBC	-	-	x	-
YUV420Planar	YUV420_3P	I420	8	420	3	x	x	x	x
YUV420SemiPlanar	YUV420_2P_UV	NV12	8	420	2	x	x	x	x
YVU420SemiPlanar	YUV420_2P_VU	NV21	8	420	2	-	-	x	x
YUV422_1P	YUV422_1P_YUYV	YUY2	8	422	1	-	-	x	x
YVU422_1P	YUV422_1P_UYVY	UYVY	8	422	1	-	-	x	x
YUV420_10b_MS	YUV420_2P_10BIT	P010	10	420	2	-	-	x	-
YUV422_10b_MS	YUV422_2P_10BIT	Y210	10	422	2	-	-	x	-
YUYAAYVYAA_10b	YUV420_2x2_10BIT_0	Y0L2	10	420	1	-	-	x	-
AAYUYAAYVY_10b	YUV420_2x2_10BIT_1		10	420	1	-	-	x	-

Rotation 0, 90, 180 or 270 degrees:

- Rotation is not supported for any AFBC format
- Rotation is not supported for 422, needs conversion to 420
- Rotation supported for all 420 YUV formats
- Interlaced output for decode is supported for all formats

Cropping of the source frame before encoding is supported

For **decode**, the AFBC format always has to match the decoded stream

All YUV output can be downscaled by a factor of 2 or 4, no scaling for encode

9/10-bit ➔ 8-bit conversion for decode supported for all YUV formats

9/10-bit ➔ 8-bit conversion for encode supported for 2x2_10BIT formats

YUV422 ➔ YUV420 conversion is supported, both for decode & encode

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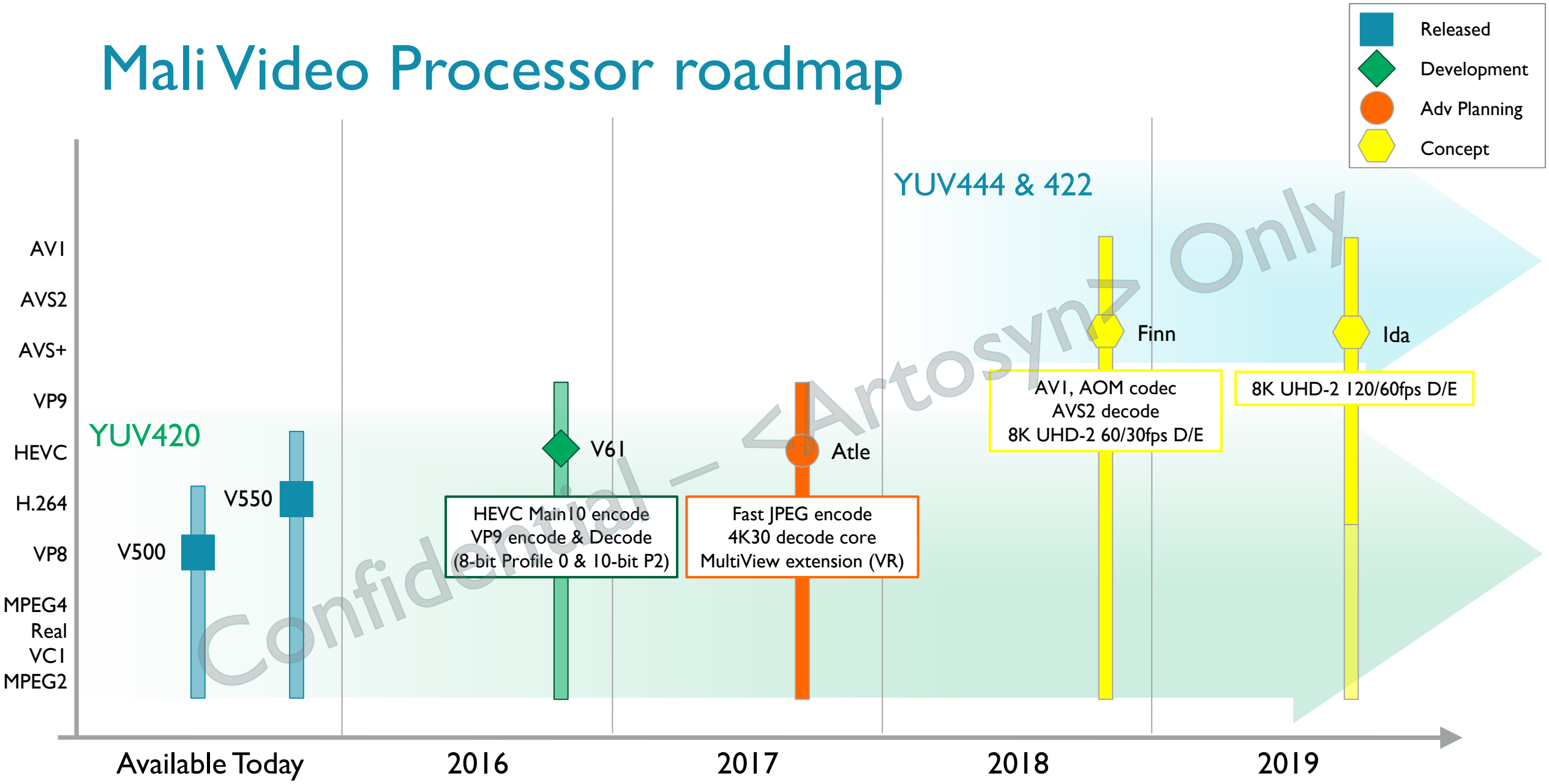
Roadmap

Mali Video Processor roadmap



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ARM a founder member of the AOM

The initial project will pursue a new, open patent royalty-free video codec specification and open-source implementation based on the contributions of members, along with binding specifications for media format, content encryption and adaptive streaming, thereby creating opportunities for next-generation media experiences.

"Customer expectations for media delivery continue to grow, and fulfilling their expectations requires the concerted energy of the entire ecosystem. The Alliance for Open Media brings together the leading experts in the entire video stack to work together in pursuit of open, royalty-free and interoperable solutions for the next generation of video delivery.

Gabe Frost, Executive Director
Alliance for Open Media

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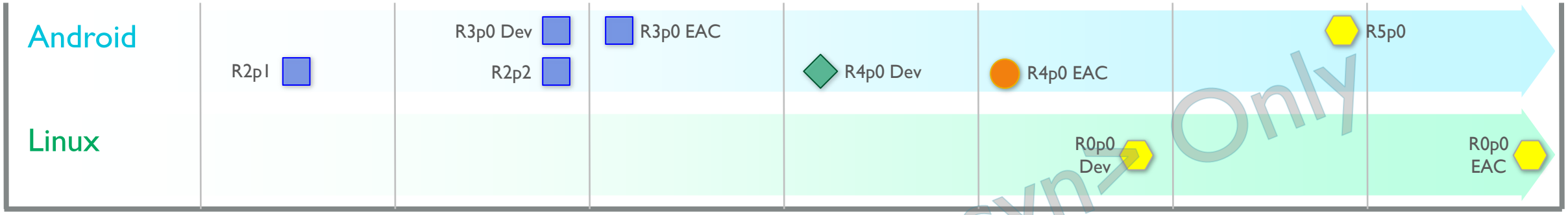
Mali-ViDDK roadmap

Roadmap subject to change

Released · Adv Planning · Planned · Concept



R1p0	R2p1	R3p0 Dev	R3p0 EAC	R4p0 Dev	R4p0 EAC	R5p0
V550 support added	Maintenance improvements	Android N support for V550	V550 EAC release	V61 Dev release VP9 encode/decode	V61 EAC release	Android O support
HEVC Support			Full Android N support CTS compliant	Android N support	Full Android N support CTS compliant	
Android L						

R2p0	R2p2
Android M support CTS compliant	Maintenance improvements

R0p0 Dev	R0p0 EAC
V61 Dev release	V61 Dev release
Video for Linux support	Video for Linux support

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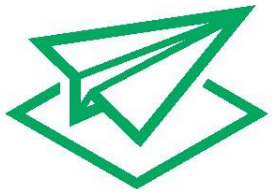
Introduction to Mali-V61

Mali-V61: 4K UHD Video Processor



Time to market

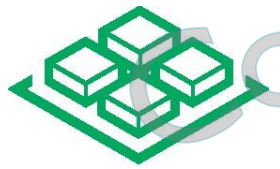
Unified IP – Mali Multimedia Suite

- The simplest way to unleash VP9 ready 4K multimedia
  - One scalable video solution to address mobile and home multimedia SoCs
  - Exceeds current premium mobile video requirements
    - Adds VP9 encode expected to be a requirement in 2018

Unified solution

~50% reduction in area

- Smallest multi video codec solution
  - OEM 'freedom of use' with simultaneous encode & decode of multiple streams
  - 50% silicon of our competitors with unified IP for all codecs, encode & decode



Multicore

Provides scalability

- Multi-standard, scalable, flexible video IP for encode and decode
  - To encode and/or decode video streams on mobile and home consumer devices
  - Supports HEVC, H.264, VP9, VP8, encode & decode and legacy decoders

EAC – December 2016

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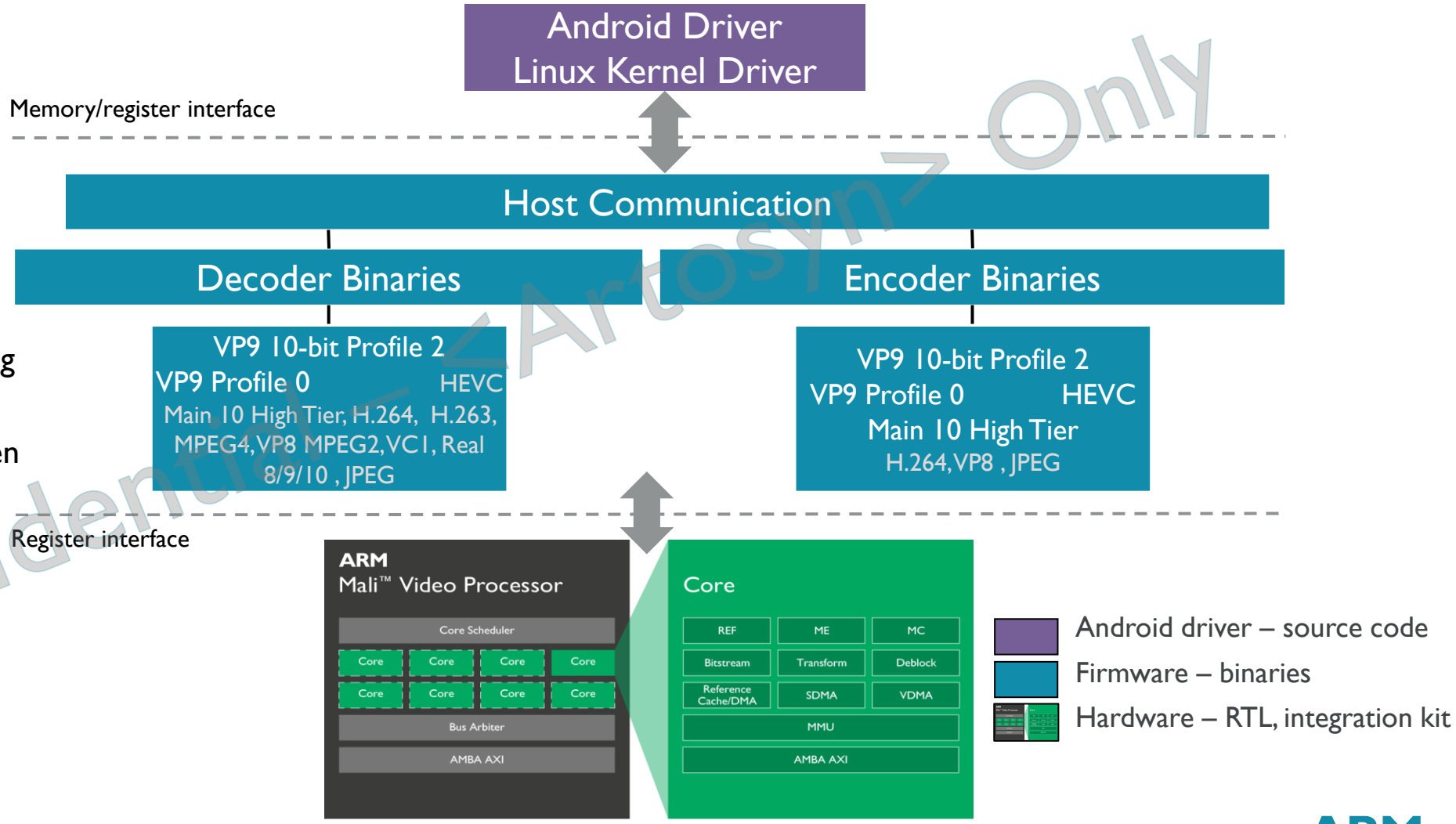
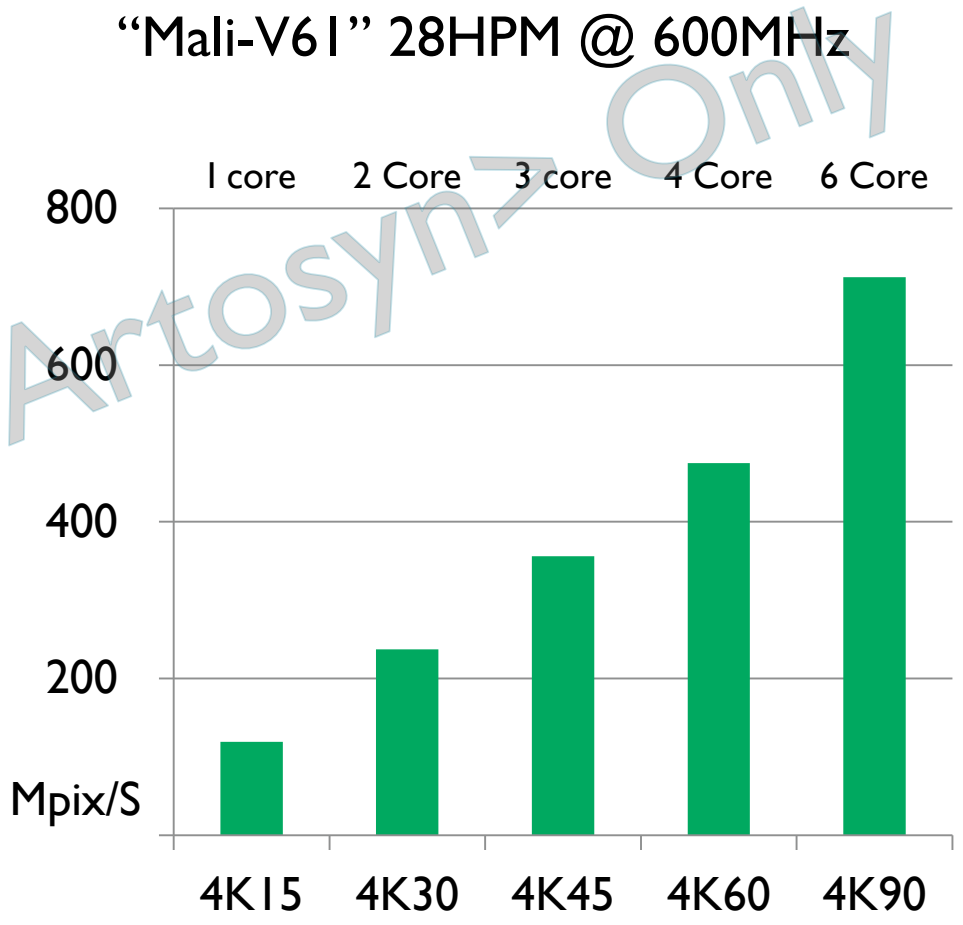
Mali-V61 flexibility

- Software:
  - Memory allocation
  - Scheduling
  - Power gating
- Firmware:
  - Codec implementation
  - Error concealment
  - Display frame reordering
  - Rate control
  - Communication between cores
- Hardware:
  - Fixed function blocks
  - Dedicated controllers
  - Control logic



Mali-V61 scalability examples

No. of Cores	28HPM @ 600MHz	Typical Displays
1	119Mpps	1080p60 WQXGAp30
2	237Mpps	4K UHDp30 1080p120
3	356Mpps	WQXGAp90 4K UHDp45
4	475Mpps	4K UHDp60



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Mali-V61 PPA, 28 HPM

Operating point	Cores	Freq [MHz]	8-bit [mm²]	10-bit [mm²]	Typical Encode Power [mW]	Typical Decode Power [mW]
1080p60	1	600	2.2 (1.5)	2.4 (1.6)	140	39
4K30 (2160p30)	2	600	4.1 (2.9)	4.4 (3.0)	280	78
4K45 (2160p45)	3	600	6.0 (4.3)	6.5 (4.5)	420	117
4K60 (2160p60)	4	600	7.9 (5.6)	8.5 (5.9)	560	156
4K90 (2160p90)	6	600	11.8(8.4)	12.6 (8.7)	840	254
4K120 (2160p120)	8	600	15.6(11.1)	16.7 (11.6)	1120	312

Mali-V61 decode only area numbers shown in brackets

- C35 transistor, 9 track library, 7-metal layers, SVT cells, 600MHz timing closure, ~80% utilization
- Power data is 28HPM, 85°C, 0.9v, dynamic power only, gate level netlist simulation, measured on one stream using HEVC on Mali-V61 MP1
  - Stream used: 8-bit Tractor 1920x1080, 50/50 P/B frame pattern for decode and encode
- Power numbers for MP2-MP8 configurations are indicative, based on scaling of the MP1 numbers

Power numbers updated 23rd November, 2016

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Mali-V61 PPA, 16 FinFet

Operating Point	Cores	Freq (MHz)	8-bit (mm^2)	10-bit (mm^2)	Typical Encode Power [mW]	Typical Decode Power [mW]
1080p80	1	800	1.3 (0.7)	1.4 (1.0)	130	39
4K40 (2160p40)	2	800	2.4 (1.7)	2.6 (1.8)	220	78
4K60 (2160p60)	3	800	3.6 (2.6)	3.8 (2.7)	390	117
4K80 (2160p80)	4	800	4.7 (3.4)	5.0 (3.5)	520	156
4K120(2160p120)	6	800	6.9 (5.0)	7.4 (5.2)	780	234

Mali-V61 decode only area numbers shown in brackets

- C16 transistor, 7.5 track library, 7-metal layers, LVT cells, 800MHz timing closure, ~80% utilization
- Power data is 16FF+, 85°C, 0.8v, dynamic power only, gate level netlist simulation, measured on one stream using HEVC on Mali-V61 MP1 using scaling from 28HPM.
  - *Stream used: 8-bit Tractor 1920x1080, 50/50 P/B frame pattern for decode and encode*
- Power numbers for MP2-MP6 configurations are indicative, based on scaling of the MP1 numbers
- 16FF+ scaling derived from 28HPM using netlist simulation

Power numbers updated 25th November, 2016

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Mali Video encode and decode

	Standard	Resolution	Mali-V500	Mali-V550	Mali-V61
Encode & Decode	HEVC Main 10 Profile up to Level 5.2 High Tier	720p/1080p/2160p			✓
	VP9 Profile 2, 10-bit, 4:2:0	720p/1080p/2160p			✓
	HEVC Main Profile up to Level 5.2 High Tier	720p/1080p/2160p		Encode Lite	✓
	VP9 Profile 0, 8-bit, 4:2:0	720p/1080p/2160p			✓
	H.264 BP/MP/HP MP1 @L4.2 - MP4 @L5.2	720p/1080p/1080i/2160p	✓	✓	✓
	VP8	720p/1080p/2160p	✓	✓	✓
	JPEG compliance (4:2:2 and 4:2:0)	8Kx8K pixels		✓	✓

Mali Video decode only

	Standard	Resolution	Mali-V500	Mali-V550	Mali-V61
Decode only	MPEG4 SP/ASP@L6	720p/1080p/1080i	✓	✓	✓
	DivX 4.x/5.x/6.x	720p/1080p/1080i/2160p	✓	✓	✓
	VC-1 SP/MP/AP@L4	720p/1080p/1080i	✓	✓	✓
	MPEG2 MP@HL	720p/1080p/1080i	✓	✓	✓
	H.263 profile0@L70	720p/1080p	✓	✓	✓
	RealVideo RV8/9/10	720p/1080p	✓	✓	✓

H.264 encoding tools

New elements/features in green

- CABAC/CAVLC entropy coding
- ME down to 1/4 pel (search window +/-128 horizontal, +/- 64 vertical)
- 8x8, 16x6 inter P modes supported
- 8x8,16x16 inter B modes supported with CABAC encoding
- Spatial direct supported for B frames with CABAC encoding
- Improved RDO based mode selection
- Support for 4x4, 8x8, 16x16 luma and chroma 8x8 intra modes
- Constrained intra prediction selectable
- Support for 4x4 and 8x8 transform
- Flexible rate control (CBR or VBR)
- In-built deblock filtering

HEVC encoding tools

New elements/features in green

- I, P and B-frame progressive encoding
- 8-bit and 10-bit sample depth
- Wavefront encoding
- Horizontal tiles
- 64x64 CTU size
- Support for all transform sizes
- ME down to 1/4 pel (search window +/-128 horizontal, +/- 64 vertical)
- Inter P splits down to 8x8
- Inter B splits down to 8x8
- Improved RDO based mode selection
- Constrained intra prediction selectable
- Flexible rate control (CBR or VBR)
- In-built deblock filtering

New in Mali-V61:VP9 encoding tools

All new for Mali Video

- 8-bit Profile 0 and Profile 2 at 10-bit sample depth
- Tile columns and tile rows
- Support for all transform sizes
- ME down to 1/4 pel (search window +/-128 horizontal, +/- 64 vertical)
- Single reference inter splits down to 8x8
- Reference Frame Scaling for both encode and decode
- RDO based mode selection
- Implicit probability update
- Explicit probability update and frame_parallel
- Flexible rate control (CBR or VBR)
- In-built deblock filtering

Mali-V61 C model

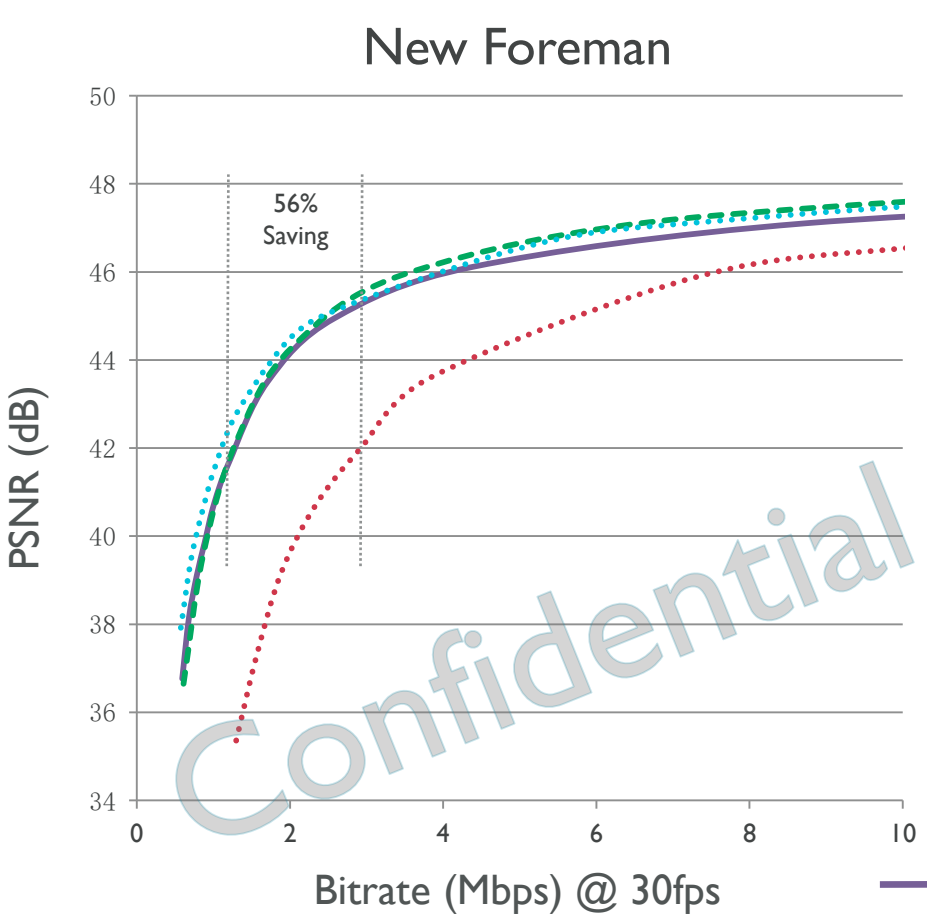
Available to Partners under LUL

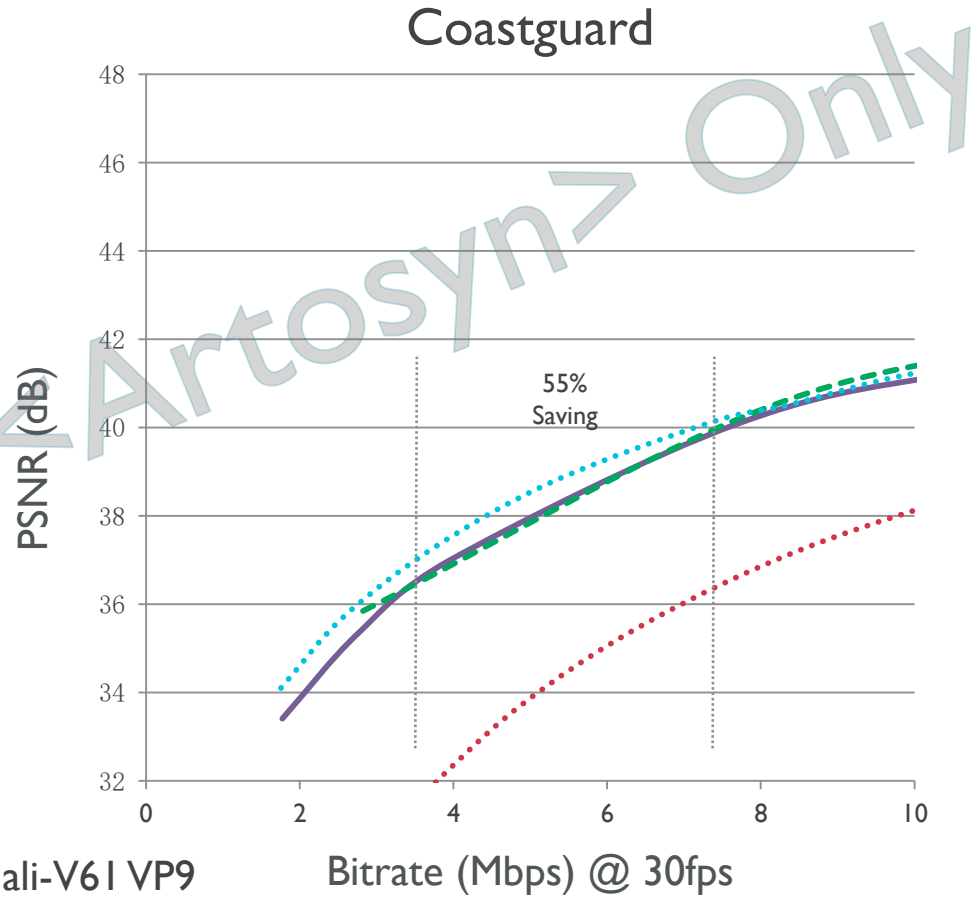
- Programs mve_decode and mve_encode are pre-built statically linked executables running on Linux, require at least GLIBC_2.3.2 to run
- Output is bit-exact to hardware/firmware implementation
- For decode a conformant bitstream is always decoded to the same output
- For encode, rate control adjustments can cause different output streams

- Does not directly provide PSNR or performance measurements
- Note:
  - Hardware model is Beta quality in October
    - There are quality and performance improvements being made between Hardware Beta and EAC
  - Firmware will not be Beta quality until December (HW EAC)
  - Rate Control, for example, will not be available before Firmware EAC in March 2017

Mali-V61 encode quality – 4K UHD 2160p

Based on bit exact alpha firmware model

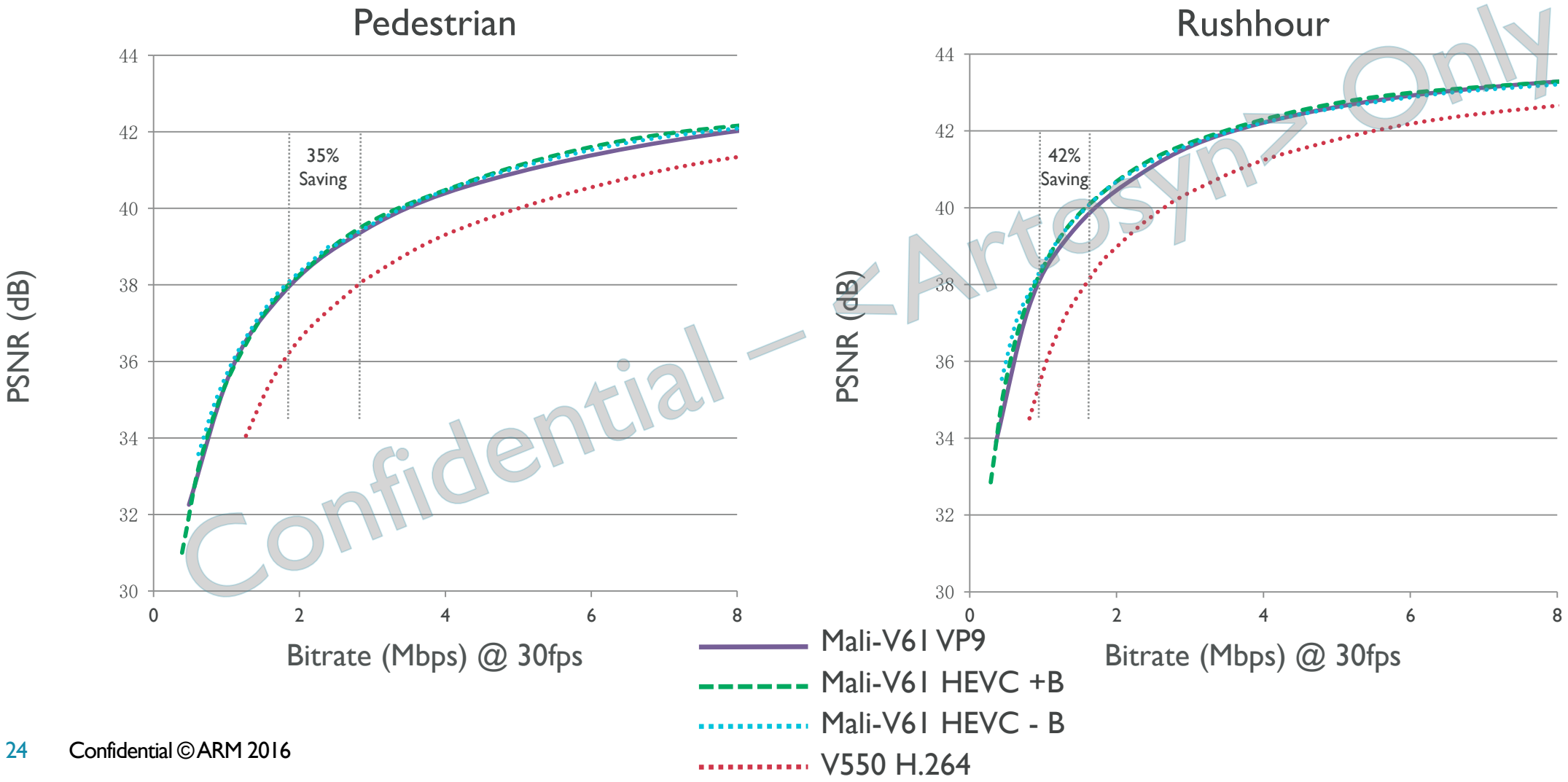




Mali-V61 VP9
Mali-V61 HEVC +B
Mali-V61 HEVC - B
V550 H.264

Mali-V61 encode quality – Full HD 1080p

Based on bit exact alpha firmware model



Mali-V61 decoder output formats

Frame Sample	Bit Depth	Memory Format
YUV420	8-bit	NV12: 2-plane, scan-line, Y and UV
YUV420	8-bit	NV21: 2-plane, scan-line, Y and VU
YUV420	8-bit	I420: 3-plane, scan-line Y, U, V
YUV420	8-bit	AFBC 1.0 Layout 1
YUV420	8-bit	AFBC 1.2 Layout 1
YUV420	10-bit	Y0L2: Single-plane block format YUYAAYVYAA
YUV420	10-bit	Single-plane block format AAYUYAAYVY
YUV420	10-bit	P010: 2-plane, scan-line, Y and UV, 10-bit in 16-bit, Microsoft format
YUV420	10-bit	AFBC 1.0 Layout 1
YUV420	10-bit	AFBC 1.2 Layout 1
YUV422 (JPEG only)	8-bit	YUY2: Single-plane, scan-line, YUYV order
YUV422 (JPEG only)	8-bit	UYVY: Single-plane, scan-line, UYVY order
YUV422 (JPEG only)	8-bit	AFBC 1.0 Layout 2
YUV422 (JPEG only)	8-bit	AFBC 1.2 Layout 2

- Limitations:
  - Rotation not supported for AFBC output
  - Cropping not supported for AFBC output
  - Rotation not supported for YUV422
    - unless converted to YUV420
  - For interlace the same rotation and scale may be used for each field
  - No color conversion support
  - No general scaling support
  - No general mip maps support
  - No deinterlacing support
  - No out of loop filtering support
  - No AFBC layout modes 5 and 6 (32x8) support
  - No AFBC block split mode support

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Mali-V61 output frame supported combinations

Output Frame Format	Crop	Downscale	Rotation	8 to B	10 to B	422 to 420
YUV420, 2 or 3 plane	Yes	1x1, 2x2, 4x4	0°, 90°, 180°, 270°	CFG10b	No	Yes
YUV420, Single plane (Y0L2)	Yes	1x1, 2x2, 4x4	0°, 90°, 180°, 270°	CFG10b	Any	Yes
YUV422, Single plane (JPEG only)	Yes	1x1, 2x2, 4x4	-	No	No	N/A
YUV420, AFBC	No	1x1, 2x2	-	CFG10b	No	Yes
YUV422, AFBC (JPEG only)	No	1x1, 2x2	-	No	No	N/A

- The reference frame output will always be in AFBC format of the bit-depth B determined by the bitstream without any post processing
  - Value of B is 8 or 10 dependent on codec support and configuration
- CFG10b: means this is supported if the 10-bit configuration is implemented

- NB an arbitrary crop could lead to less efficient AXI access if the picture is no longer burst aligned

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Mali-V61 encode source frame inputs

Frame Sample	Bit Depth	Memory Format
YUV420	8-bit	NV12: 2-plane, scan-line, Y and UV
YUV420	8-bit	NV21: 2-plane, scan-line, Y and VU
YUV420	8-bit	I420: 3-plane, scan-line Y, U, V
YUV420	8-bit	AFBC 1.2 16x16 and 32x8 block size
YUV420	10-bit	P010: 10 bits stored in 16-bit (Microsoft format)
YUV420	10-bit	Y0L2: 1-plane block format YUYAAYVYAA
YUV420	10-bit	1-plane block format AAYUYAAYVY
YUV420	10-bit	AFBC 1.2 16x16 and 32x8 block size
YUV422	8-bit	YUY2: 1-plane, scan-line, YUYV order
YUV422	8-bit	UYVY: 1-plane, scan-line, UYVY order
YUV422	8-bit	AFBC 1.2 16x16 and 32x8 block size
RGBA	8-bit	RGBA8888: 1-plane byte address order R,G,B,A
BGRA	8-bit	BGRA8888: 1-plane byte address order B,G,R,A
ARGB	8-bit	ARGB8888: 1-plane byte address order A,R,G,B
ABGR	8-bit	ABGR8888: 1-plane byte address order A,B,G,R

- Limitations:
  - The encoder may read data outside the crop region but shall not be affected by its contents and shall not go beyond a 4K page boundary
  - No interlaced input support
  - No scaled input support
  - No noise filtering support
  - No video stabilization support
  - AFBC input does not support cropping
  - AFBC input does not support rotation

Mali-V61 input source frame supported

Input Format	AFBC	Coded Format	Crop	Downscale	Rotation	Mirror	8 to B	10 to B
YUV420	No	YUV420	Yes	1x1	0°, 90°, 180°, 270°	0, X, Y	CFG10b	Any
YUV422	No	YUV420	Yes	1x1	0°, 90°, 180°, 270°	0, X, Y	No	No
YUV422	No	YUV422 (JPEG only)	Yes	1x1	0°, 180°	0, X, Y	No	No
YUV422	No	YUV440 (JPEG only)	Yes	1x1	90°, 270°	0, X, Y	No	No
RGB	No	YUV420	Yes	1x1	0°, 90°, 180°, 270°	0, X, Y	CFG10b	No
RGB	No	YUV422	Yes	1x1	0°, 180°	0, X, Y	No	No
RGB	No	YUV440	Yes	1x1	90°, 270°	0, X, Y	No	No
YUV420	Yes	YUV420	No	1x1	-	-	CFG10b	CFG10b
YUV422	Yes	YUV420	No	1x1	-	-	No	No
YUV422	Yes	YUV422 (JPEG only)	No	1x1	-	-	No	No

- Input frame is encoded at bit depth B
  - Value of B is 8 or 10 dependent on codec support and configuration
- CFG10b: means this is supported if the 10-bit configuration is implemented
- NB an arbitrary crop could lead to less efficient AXI access if the picture is no longer burst aligned

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JPEG Support

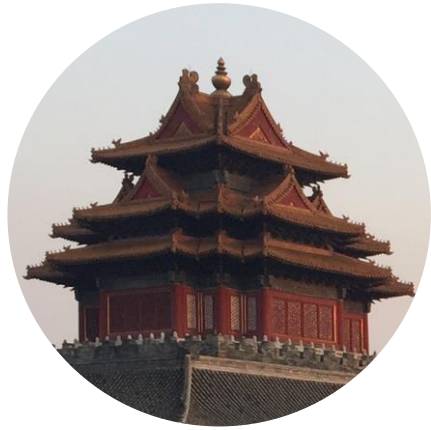
Mali-V61 JPEG encode capabilities

‘Freedom of use’ through flexible architecture

- YUV420 and YUV422 baseline sequential JPEG encode
- Multi-shot encoding
  - It is possible to encode Single or Multi-shot JPEG concurrently with encoding/decoding video
  - Performance implementation dependent
- Examples based on cores running at 450MHz

Four Cores
32MP
Multi-shot at
20 FPS

Single Core
8MP
Multi-shot at
20 FPS



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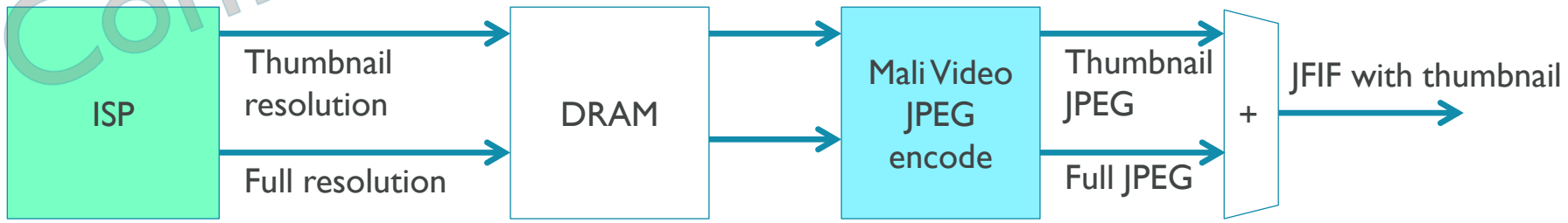
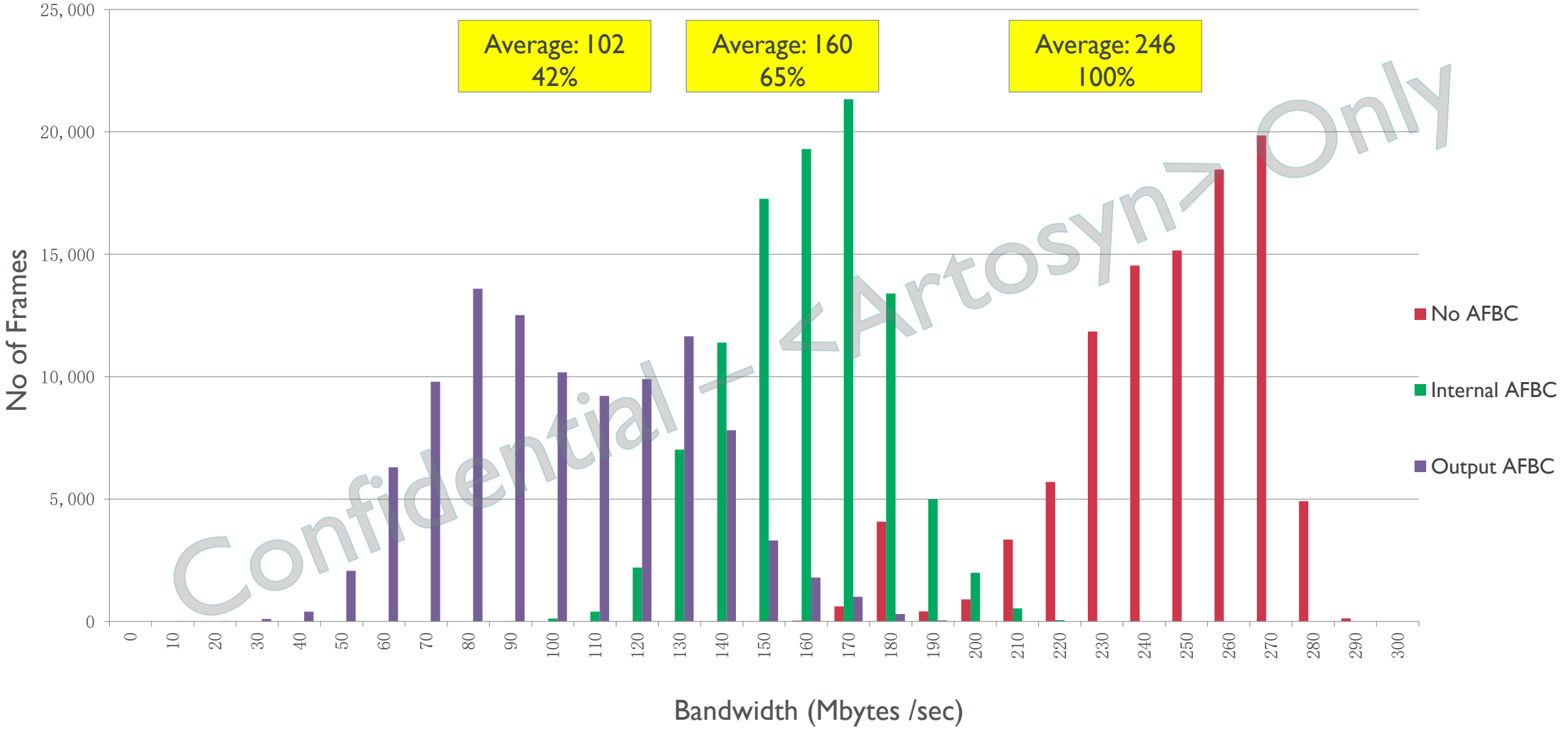
JPEG encode thumbnail support

- Status
  - No JPEG encode Thumbnail support is planned for Mali-V61 or Atle
- Reasoning
  - To support JPEG thumbnails requires an arbitrary scaler from Full-resolution to Thumbnail-resolution
  - The video encode path does not include an arbitrary scaler – this would be an additional complexity and area cost that would only be useful for JPEG
  - For ISPs that provide multi-channel output, a higher quality Thumbnail resolution image can be generated by the ISP
  - There is a software workaround to read every n'th row that has acceptable performance in current systems
- Recommended system:



AFBC in Mali-V6 I

Mali-V61 AFBC decode Casino Royale 1080p24



Testing

System testing – overview of tests

- Codecs
  - All supported codecs tested on system level
  - More than 4,000 test streams in total
- Conformance
  - Verifies that codecs conform to standards
  - Decode conformance tests streams from standard bodies
  - Encode syntax conformance checks
- Industry standard stress streams
  - Allegro (H.264) – AL-H264-ES
  - Argon (HEVC, VP9) – Argon Streams HEVC & VP9
  - Tektronix (VC-1, H.264, MPEG4)
- Bandwidth
  - Test against codec bandwidth requirements
- Error handling
  - Stress testing to ensure robustness and concealment
- Encode quality
  - Compare encode quality to reference encoders
  - Rate controller testing
- API test
  - Stress testing of the communication protocol between the driver and firmware
- Multicore
  - Verify that the performance scales with the number of cores and that the number of cores does not affect codec behavior in unexpected ways
- Multisession
  - Verify stability when several concurrent sessions run on the same hardware
- Features
  - Verifies that every supported feature behaves as expected
- Robustness testing
  - Decode of complete Blu-ray movies
- Performance – while varying external bus behavior
  - Frame rate
  - Frame lag
  - Encode latency

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Timelines

Mali-V61 timeline

- Binary model evaluation tool
  - Alpha available now
  - Beta release 14th December 2016
  - EAC release March 2017
- Hardware
  - Beta available now
  - EAC release 14th December 2016
- Firmware
  - Beta release 14th December 2016
  - EAC release March 2017
- Software
  - ViDDK r4p0 EAC release April 2017

ARM

Thank you