Customer Delivery Form

Version 1. 00
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Contents

Library	***Y/N***
STD	need OD library if Artosyn decide to signoff OD timing
STD ECO Kit	Artosyn to check
STD PMK kit	Artosyn to check with SNPS about LVL H/L transitor share nwell
IO	Y
IO PAD	Y
RDL BUMP	Artosyn to provide BUMP library
Memory	Y
Analog IP	Artosyn to provide ABB verilog simulation model
TCD/ICOVL	Artosyn to check
ESD clamp cell	Y
CDM buffer	Artosyn/VSI to check
Tech File	***Y/N***
ICC tech file	Y
ICC Tluplus/mapping file	Y
ICC gds2out layer mapping file	Y
Innovus tech lef	Artosyn to provide
Innovus gd2out layer mapping file	Artosyn to provide
QRC tech file	Artosyn to provide
STARC nxtgrd file	Artosyn to provide
virtuoso tech file/mapping file	Artosyn to provide
drc runset (keep VSI updated if any new version)	***Y/N***
ANT	Y
dummy metal	Y
dummy poly/OD	Y
DRC	Y
LVS	Y
bump	Y
Timing Signoff Creteria	***Y/N***
function mode signoff corner	Y
DFT mode signoff corner	VSI to decide
OCV derating	Y
setup uncertainty	Artosyn to decide
hold uncertainty	Y
Docs	***Y/N***
design rule	Y
bump design rule	Y
process design implementation guideline	Y
Data flow	***Y/N***
IP dataflow for floorplan	Artosyn to provide
full chip dataflow for floorplan	Artosyn to provide
Netlist	***Y/N***
netlist by block	Artosyn to provide
LVT pct requirements	Y
change names	Artosyn to check
unique instance names between blocks	Y
wand/wor in netlist	Artosyn to check
floating inputs	Artosyn to check
SDC	***Y/N***
clock structure diagram	Artosyn to provide
pre synthesis SDC (block, top-only, flatten)	Artosyn to provide
don't touch cell list	Artosyn to provide
delay chain instance list	Artosyn to provide
don't use cell list	Artosyn to provide
spare cell requirements	Artosyn to provide
special requirements	Artosyn to provide
prelayout timing clean with reasonable setup margin uncertainty and OCV in WCL corner	Artosyn to check
check prelayout timing in PT with WCL	Artosyn to check
UPF/CPF	***Y/N***
power state table	Artosyn to provide , Artosyn check CA7/ceva TOP power off or not
UPF (ca7 core, ca7 subsystem, ceva core, ceva subsystem, HEVC , ISP, top-only, flatten)	Artosyn to provide
Pin Assignments	***Y/N***
pin assignment file	Artosyn to provide
SiP requirements	Artosyn to decide
Power Estimatio/IR drop/EM	***Y/N***
estimated power consumption	Artosyn to check IP power consumption or toggle rate VCD
IR drop signoff creteria	Y
EM signoff creteria	Y
ROM code files	***Y/N***
update ROM code files and gds/cdl before tapeout	Artosyn to provide after finalize
Special physical requirement	***Y/N***
OTP bonding pad/CP test requirement	Artosyn to check
place PLL in digital core region	Artosyn to decide
use beachfrount DDR IO	Artosyn to check with SNPS about decap cell rows number and ESD penalty
Misc.	***Y/N***
Ceva Congesetion&Timing	Artosyn to check synthesis enviroment delivered from CEVA for congestion&timing