VeriSilicon

DFT Information Customer Form

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Contents

Test Mode	***Y/N***
dc scan	Y
IDDQ	Artosyn to control hard macro IP into sleep mode
ac scan	Y
ac mbist	Y
boundary scan	Y
IP test	covered by dedicated ATE mode
Test For OD mode	TBD
SPEC	***Y/N***
min dc scan test coverage	>96%, try to reach higher number
min ac scan test coverage	>80%
ATE memory limit	decided by VSI
scan chain length limit	decided by VSI
scan shift frequency	20M
speical MBIST algorithm	decided by VSI
MBIST diagnose	Y
MBIST repair	N
number of IO pins for DFT	130
Timing signoff creteria	Y
MBIST share bus	Y
Delivery Data	***Y/N***
IO pin assignment(NC pin list, SiP pin list)	Artosyn to check Sip Requirements
clock structure diagram	Artosyn to provide diagram together with detailed instance list
memory documents	Artosyn to provide memory related documents
soft IP documents(test related)	Artosyn to provide DFT guideline of soft IP (test interface, etc.)
hard IP documents	Y
OCC insertion points (Diagram+List)	Artosyn to provide
test mode config and hookupin list (scan, mbist, bsd)	Artosyn to provide test mode hookup pin
PLL/clock gen boot sequence in DFT mode	Artosyn to provide control pin name/pattern to enable OSC bypass mode(1.8v analog signal)
UPF files to define power switch/isolation enable hookup pin	Y
memory ROM code files	Artosyn to provide after finalize code
Check List/IO	***Y/N***
IO pin mux support DFT mode	owned by VSI
IO control pin(pu/pd, driving strength) stable in DFT mode	Artosyn to config
IO control pin(aplication voltage cfg) stable for multi-IO	Artosyn to config "MS" pin to enable 1.8v mode SD IO
Check List/clock	***Y/N***
clock gen support at speed scan/mbist mode (ref , PLL, gating, switch are sta	Artosyn to modify clock gen
at speed san/mbist clock frequency configuable	N
use TAP controller/scan chain to configure at speed clock frequency	N
OSC cell are not used as reference clock for PLL	20M
bypass IP output clock	Artosyn to add mux
bypass clock divider in soft IP	Artosyn to bypass divider in DFT mode
add don't touch buffer to prevent serial OCC insertion	Artosyn to add buffer
at speed san/mbist clock frequency same with function's	Artosyn to check
adjust at speed clock frequency for multicycle memory path in MBIST mode	Artosyn to add mux for CA7 in MBIST mode
at speed san/mbist clock frequency for OD application	Artosyn to check
PLL Clocks bootstrap	Y
Check List/reset	***Y/N***
clock gen divider reset controlled by IO pin	Y
PLL reset controlled by IO pin	Y
scan reset controller by IO pin	Artosyn to add mux
don't share clock gen/PLL/scan reset	Y
bypass reset synchronize logic	Y
Check List/memory	***Y/N***
memory EMA pin setting stable in MBIST mode	Artosyn to add
memory EMA pin setting in MBIST mode same as function mode	Artosyn to check
Check List/power switch	***Y/N***
power switch cell always turn on in DFT mode	Artosyn to add control
Check List/Misc.	***Y/N***
don't use scan DFF lib cell in synthesis	Y