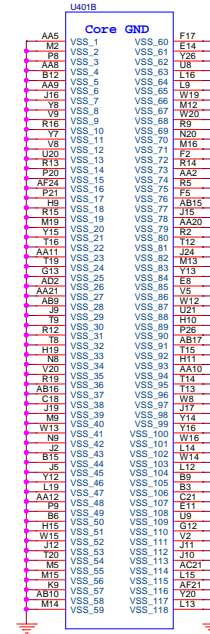
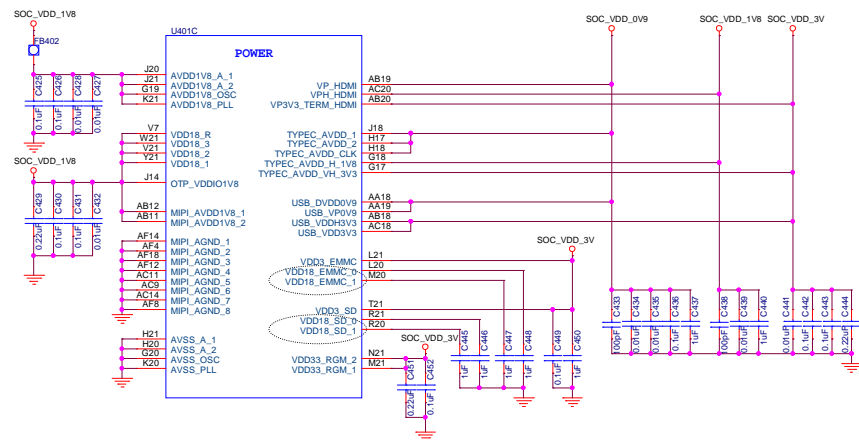
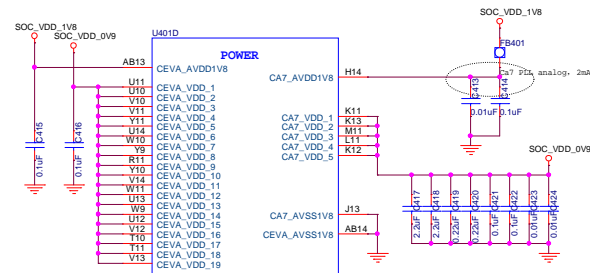
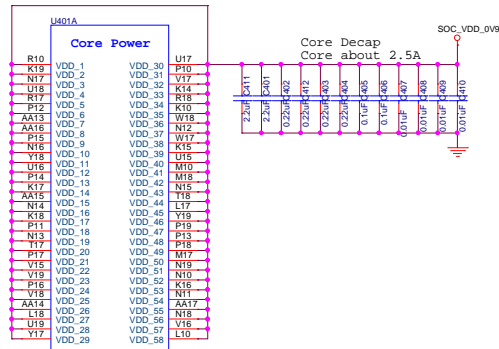


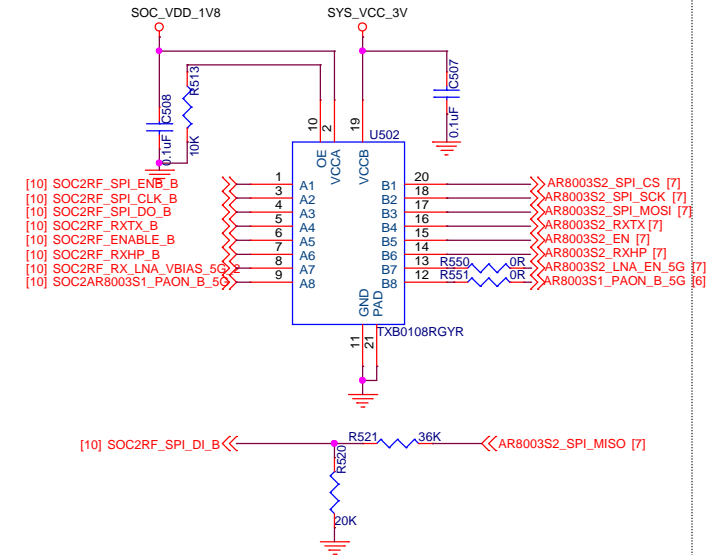


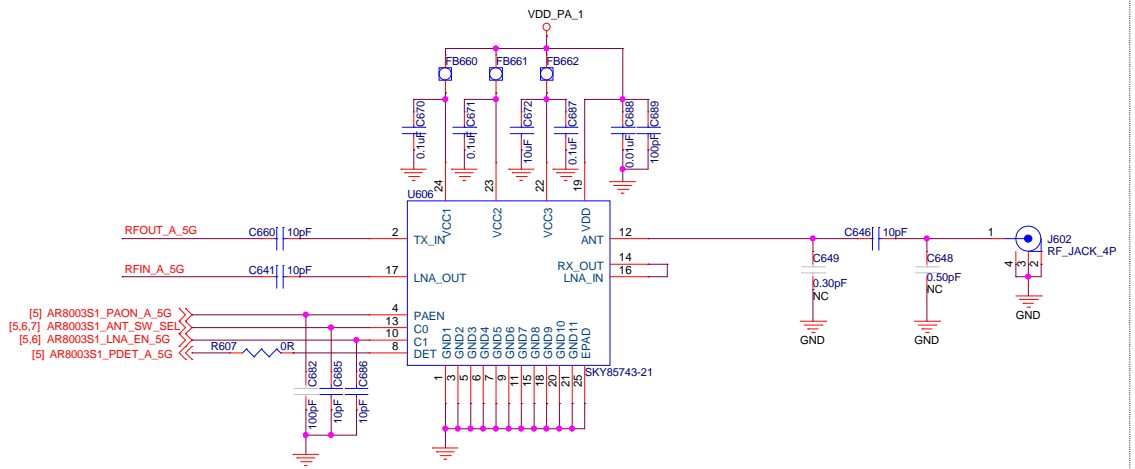
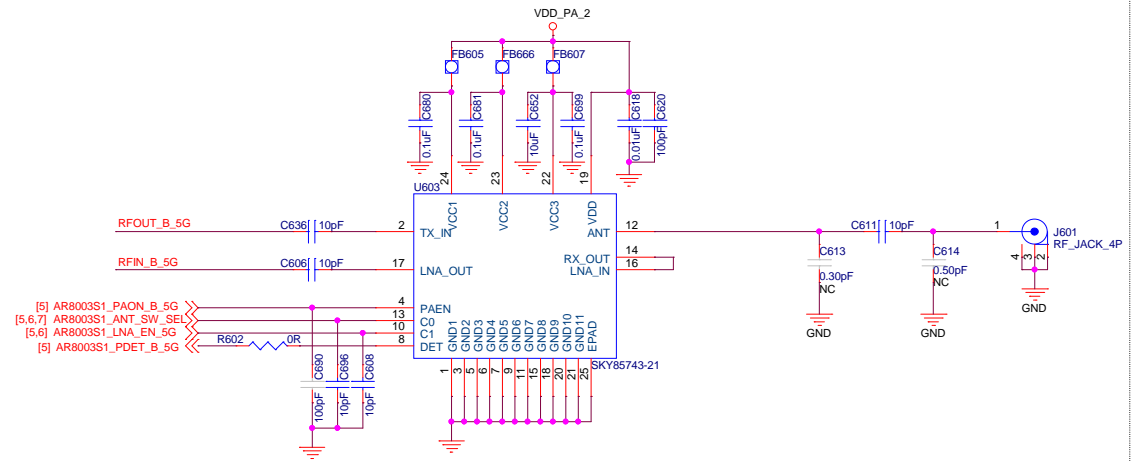
SIRIUS_LD_MB_V1.0.0

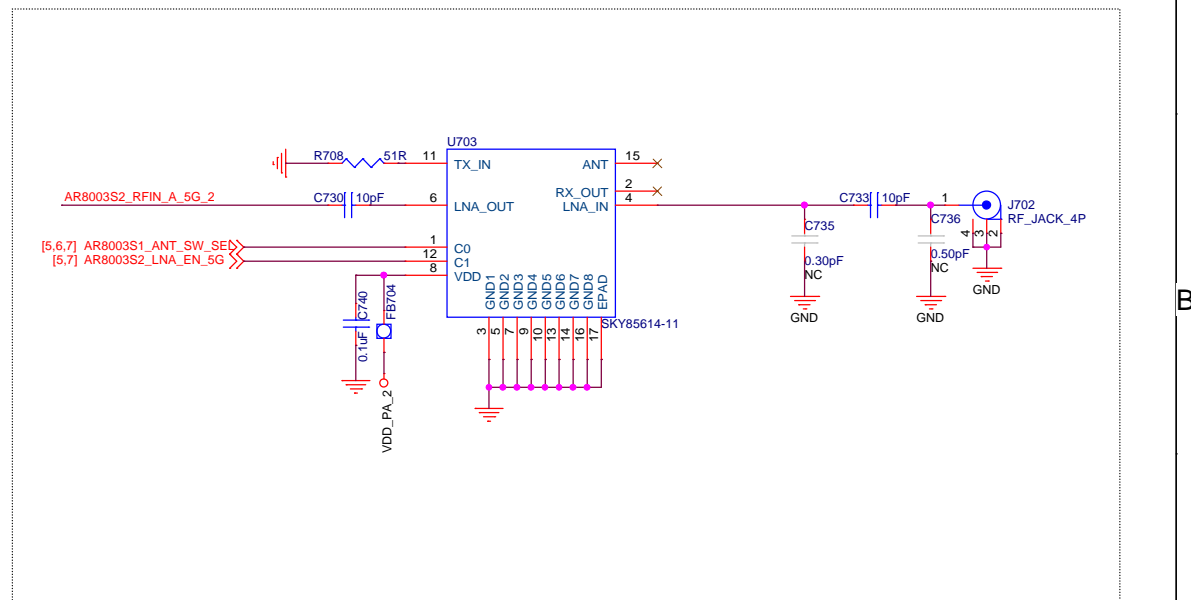
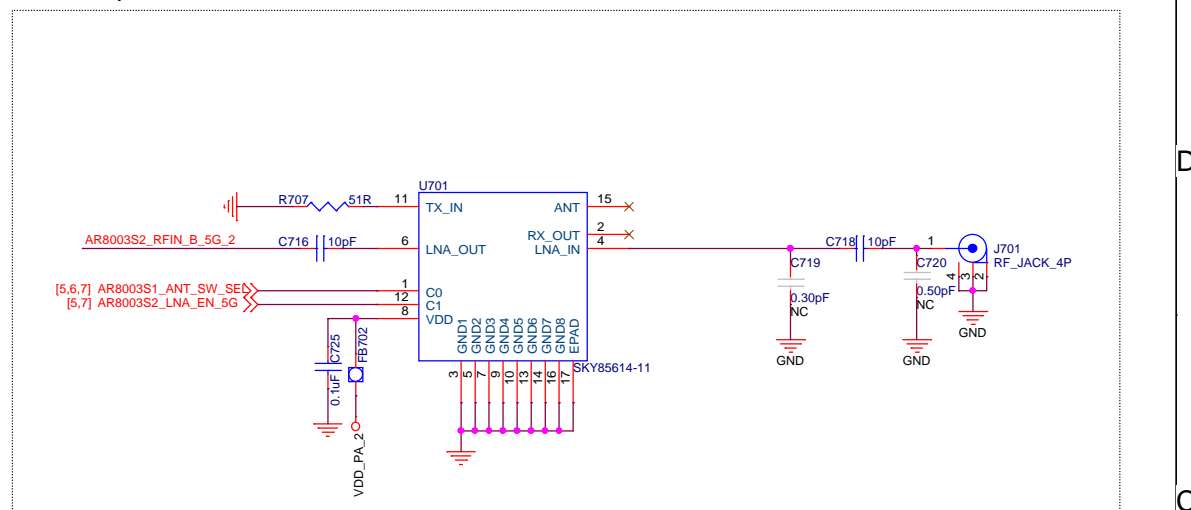
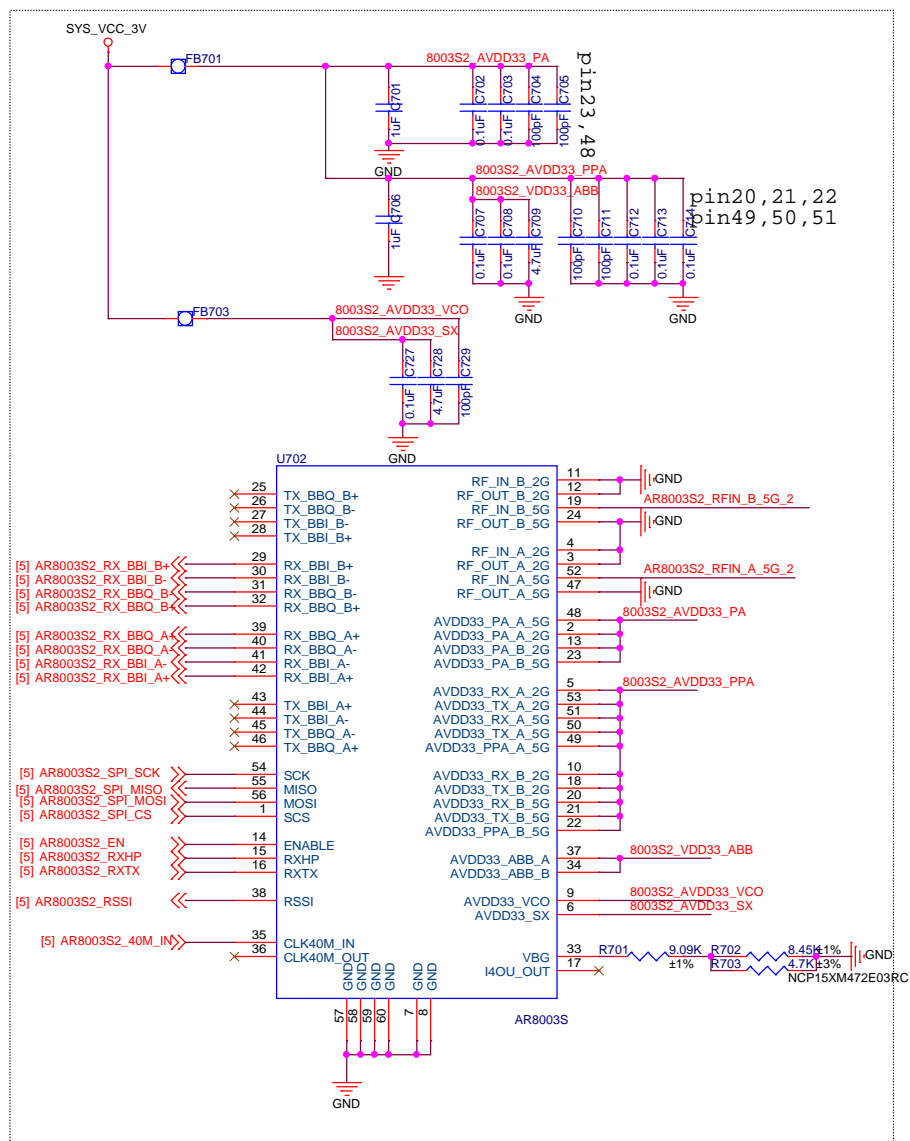
VERSION	Changelist	Created By	DATE
1.0.0	First Version	Wuping Wang Junfei Hu	27/02/2018

Wuping Wang	SIRIUS_LD_MB_V1.0.0	1.0.0
2018.02.27	B	P01_COVER
R&D, ARTOSYN		1 12

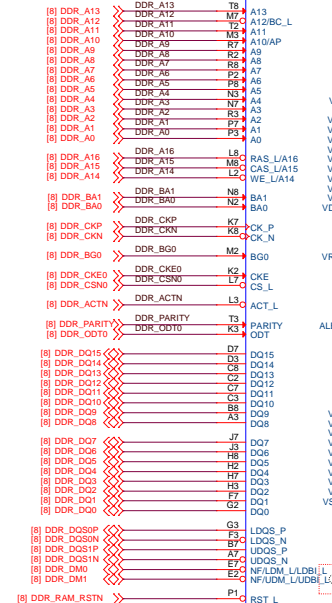
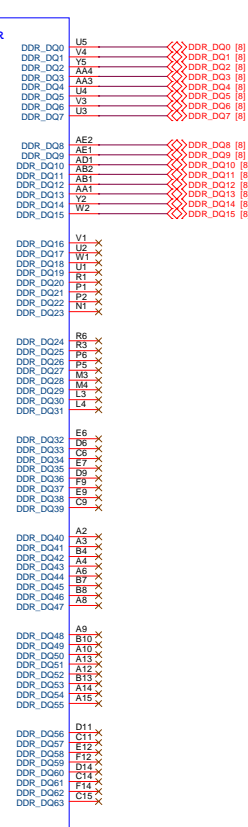








Wuping Wang	SIRIUS_LD_MB_V1.0.0		1.0.0
2018.02.27	B	P07_RF_RX_2	
R&D ARTOSYN		7 7 7	12 7

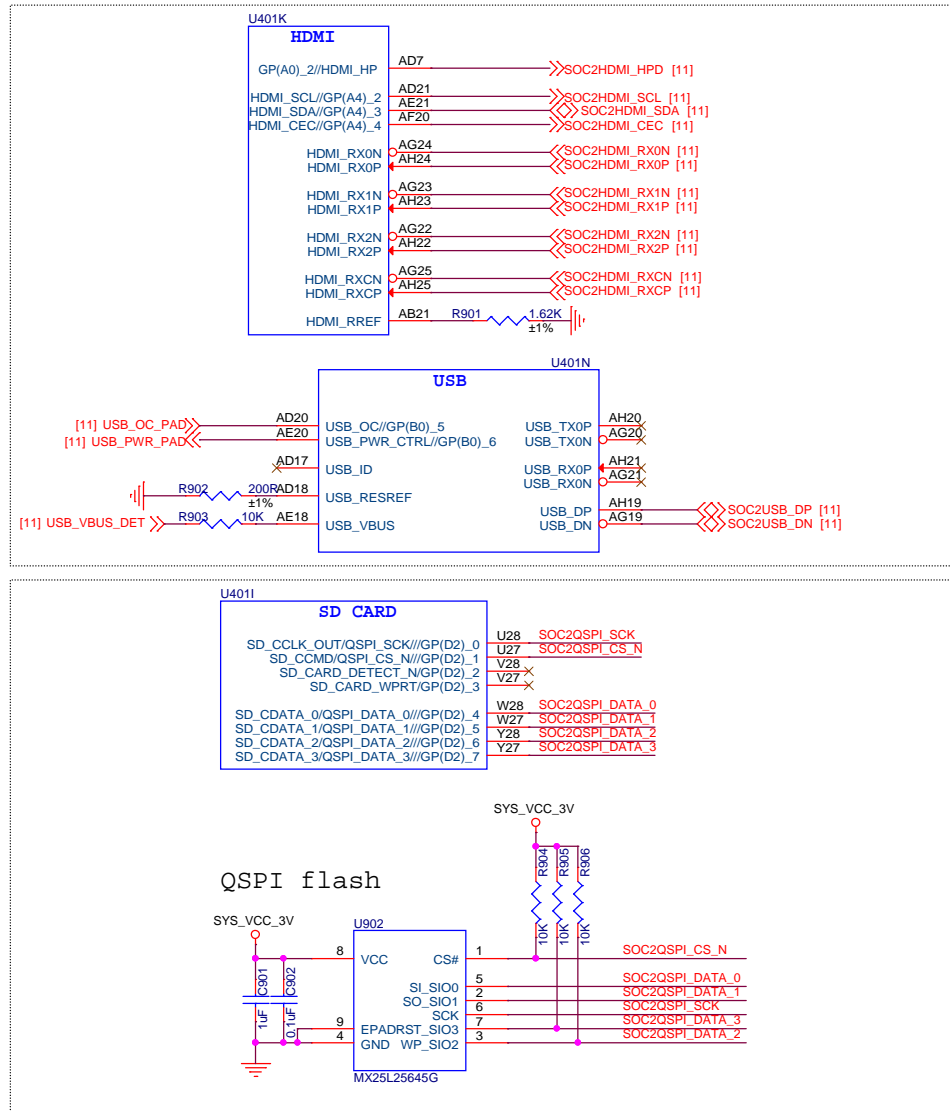


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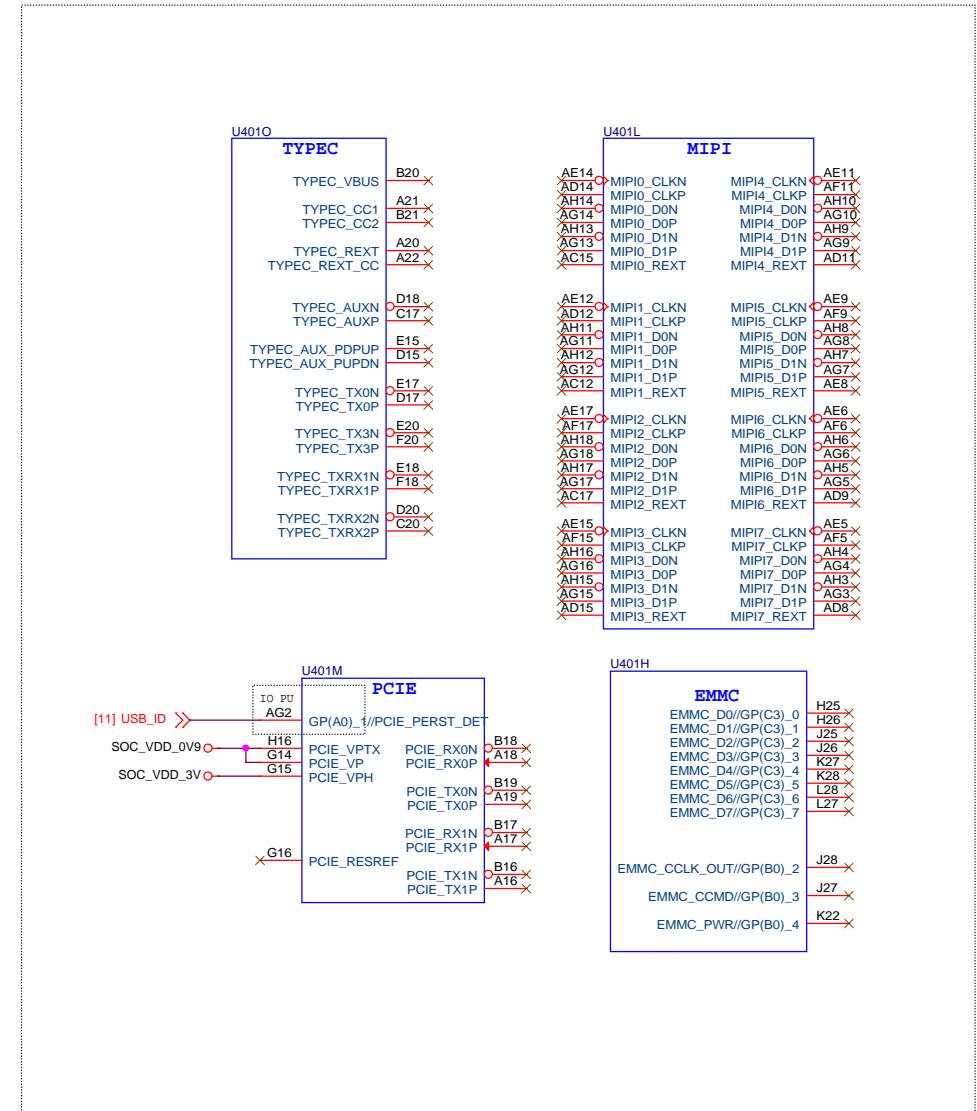
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artosun			
Wuping Wang	SIRIUS_ID_MB_V1.0.0		1.0.0
2018.02.27	B	P09_Sirius_Signal1	
R&D, ARTOSYN		9 12	

U401P

DVP

PCLK0//GP(A2)_6 AD26 >>> SOC2DVP_PCLK0 [11]
 DE0//GP(A2)_7 AD25 >>> SOC2DVP_DE0 [11]
 VSYNC0//GP(B0)_0 AF26 >>> SOC2DVP_VSYNC0 [11]
 HSYNC0//GP(B0)_1 AE26 >>> SOC2DVP_HSYNC0 [11]

QE0_0//GP(B3)_0 AG26 >>> SOC2DVP_QE0_0 [11]
 QE0_1//GP(B3)_1 AF25 >>> SOC2DVP_QE0_1 [11]
 QE0_2//GP(B3)_2 AD23 >>> SOC2DVP_QE0_2 [11]
 QE0_3//GP(B3)_3 AE24 >>> SOC2DVP_QE0_3 [11]
 QE0_4//GP(B3)_4 AC22 >>> SOC2DVP_QE0_4 [11]
 QE0_5//GP(B3)_5 AE23 >>> SOC2DVP_QE0_5 [11]
 QE0_6//GP(B3)_6 AF23 >>> SOC2DVP_QE0_6 [11]
 QE0_7//GP(B3)_7 AD22 >>> SOC2DVP_QE0_7 [11]

PCLK1//GP(A2)_2 AC28 >>> SOC2GPIO_0 [11]
 DE1//GP(A2)_3 AD28 >>> SOC2GPIO_1 [11]
 VSYNC1//GP(A2)_4 AC27 >>> SOC2GPIO_2 [11]
 HSYNC1//GP(A2)_5 AE28 >>> SOC2GPIO_3 [11]

QE1_0//GP(A3)_0 AF28 >>> SOC2DVP_QE1_0 [11]
 QE1_1//GP(A3)_1 AD27 >>> SOC2DVP_QE1_1 [11]
 QE1_2//GP(A3)_2 AG28 >>> SOC2DVP_QE1_2 [11]
 QE1_3//GP(A3)_3 AE27 >>> SOC2DVP_QE1_3 [11]
 QE1_4//GP(A3)_4 AH26 >>> SOC2DVP_QE1_4 [11]
 QE1_5//GP(A3)_5 AG27 >>> SOC2DVP_QE1_5 [11]
 QE1_6//GP(A3)_6 AH27 >>> SOC2DVP_QE1_6 [11]
 QE1_7//GP(A3)_7

1.8v digital IO

U401Q

I2S

I2S_WS_0//GP(B2)_0 AA27 >>> SOC2PMU_SLEEP [3]
 I2S_SDI_0//GP(B2)_1 AA26 >>> SOC2I2S_SDO_0 [11]
 I2S_SDO_0//GP(B2)_2 AB28 >>>
 I2S_CLK_0//GP(B2)_3 AA28 >>>

I2S_WS_1//GP(B2)_4 AA25 >>>
 I2S_SDI_1//GP(B2)_5 Y25 >>> SOC2I2S_SDO_1 [11]
 I2S_SDO_1//GP(B2)_6 AB27 >>>
 I2S_CLK_1//GP(B2)_7 AC26 >>>

I2S_WS_2//GP(C2)_0 Y24 >>>
 I2S_SDI_2//GP(C2)_1 AA23 >>> SOC2I2S_WS2 [11]
 I2S_SDO_2//GP(C2)_2 AA24 >>> SOC2I2S_SDO_2 [11]
 I2S_CLK_2//GP(C2)_3 AC22 >>> SOC2I2S_CLK2 [11]
 I2S_WS_3//GP(C2)_4 AB23 >>> SOC2I2S_SDO_3 [11]

I2S_SDI_3//GP(C2)_5 AB24 >>> SOC2RF_RXTX_B [5]
 I2S_SDO_3//GP(C2)_6 AC24 >>> SOC2RF_ENABLE_B [5]
 I2S_CLK_3//GP(C2)_7 AC25 >>> SOC2RF_RXHP_B [5]
 >>> SOC2RF_RX_LNA_VBIAS_5G_2 [5]

1.8v digital IO

U401S

I2C

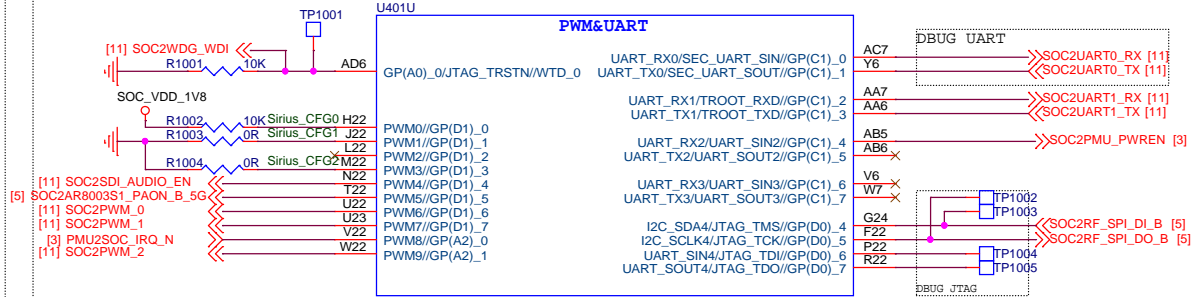
I2C_SDA0//GP(B1)_0 AE3 >>> SOC2PMU_I2C_SDA0 [3]
 I2C_SCLK0//GP(B1)_1 AD3 >>> SOC2PMU_I2C_SCLK0 [3]

I2C_SDA1//GP(B1)_2 AD4 >>>
 I2C_SCLK1//GP(B1)_3 AC4 >>>

I2C_SDA2//GP(B1)_4 AC5 >>> SOC2DVP_I2C_SDA [11]
 I2C_SCLK2//GP(B1)_5 AC3 >>> SOC2DVP_I2C_SCLK [11]

I2C_SDA3//GP(B1)_6 F24 >>> SOC2RF_SPI_ENB_B [5]
 I2C_SCLK3//GP(B1)_7 H24 >>> SOC2RF_SPI_CLK_B [5]

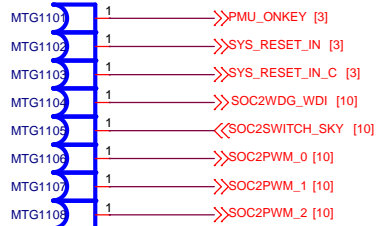
1.8v digital IO



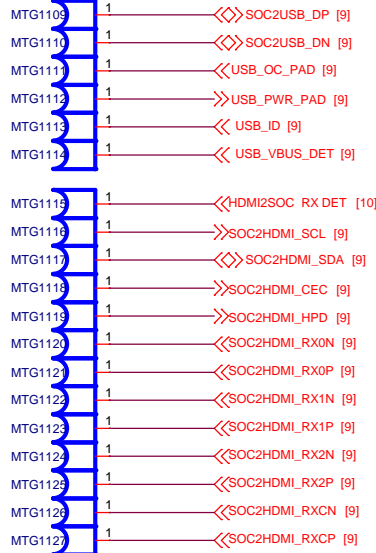
artosyn

Wuping Wang	SIRIUS_LD_MB_V1.0.0		1.0.0
2018.02.27	B	P10_Sirius_Signal2	
R&D, ARTOSYN		10 12	

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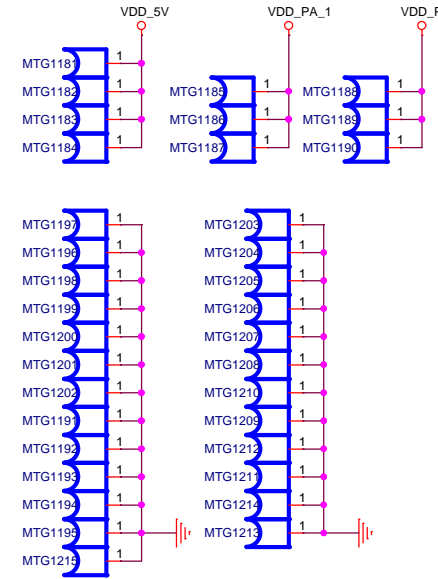
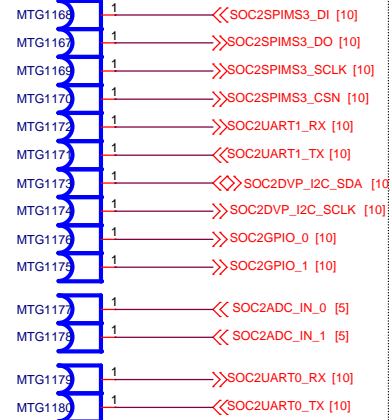
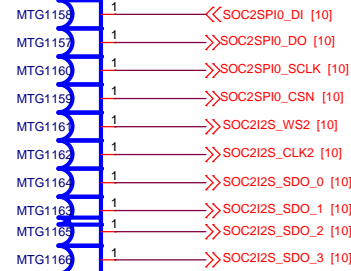
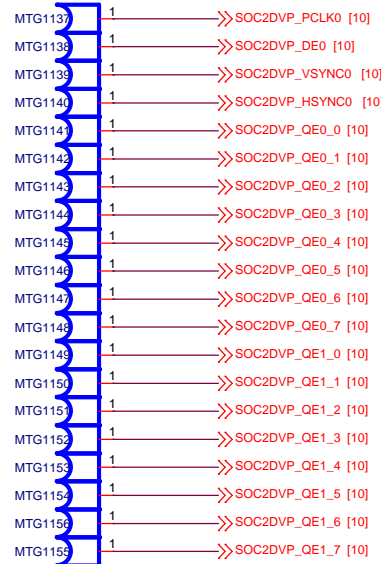
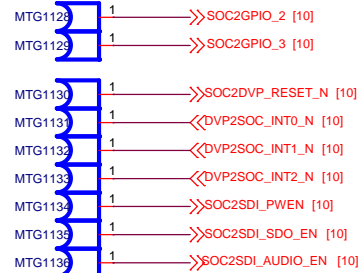


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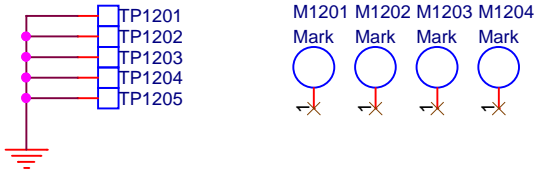
C


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artosun			
Wuping Wang	SIRIUS_LD_MB_V1.0.0		1.0.0
2018.02.27	B	P11_CONN_PORT	
R&D, ARTOSYN		11	12

MARK AND TEST



			
Wuping Wang	SIRIUS_EK_MB_V001		1.0.0
2018.02.27	A	SIRIUS_LD_MB_V1.0.0	
R&D, ARTOSYN		[12]	[12]