Security C - TSMC Secret

MT Form

Device Name: TMJX23

MT Version: MT-TMJX23-001 (Active)

1. Customer's Instruction

2. Project Information

Customer :	AN61 / SHICC		
Fab :	FAB15		
TSMC Product Name :	TMJX23	Customer Project Name :	LVTM0281703
Contact :	Rui Han	Tel :	021-61609878
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Editor :	AN61001	Update Date :	11/07/2017 19:52:30 (GMT/UTC+8)
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3. Technology Information

No	Question	Answer
1.	**Fab**	FAB15
2.	**TSMC Technology Selection**	
2.1	Geometry	28 nm
2.2	Technology	CL/CMOS LOGIC
	Device	HC/High Performance Compact Mobile Computing
	Process	ELK Cu
2.3	Voltage	0.9/1.8
2.4	Poly / metal layer quantity (Excluding RDL(MD) Layer)	1P / 8M
2.5	Poly gate material	HKMG
2.6	N-Buried Layer for EPI deposition	N
	Technology code(TL4)	CLN28HC41001 / 28 nm, CMOS LOGIC High Performance Compact Mobile Computing ELK Cu, 1P10M, HKMG, 0.9/1.8V
	Remark	CLN28HPC
3.	**Service Stage**	WF=>BP
3.1	Bump Type (FS: Front side; BS: Backside)	FS Lead free
	Backend Technology code(TL2)	N28BPL00012001 / 28 nm, Bumping FS Lead free, 12 inch
4.	**Product design for automotive**	N
4.1	Purchase tsmc automotive service	N

4. Mask Level & RFL Information

4.1 Mask Level Information

Customer Test Line : No

Special Scribe Line Width : No,use TSMC standard

Job View :

Request -- Yes
Place -- Internet E-jobview,
Hold Mask? Yes, Hold mask to wait Job View approval : All layer hold.
Notified Email List -- hanrui@icc.sh.cn

Form description :

Mask Combination : Completed

Metal Count(Scheme) = 8 (6_IME/2_TME)

No.	ID	Name	Ver.	Code/Option
1	120	OD1-ETCH	A	
2	121	ODR-ETCH	A	
3	191	WELL-P-CORE-IMP	A	
4	118	VT-N-CODE-LV-IMP	A	
5	193	WELL-P-I/O-IMP	A	
6	192	WELL-N-CORE-IMP	A	
7	194	WELL-N-I/O-IMP	A	
8	152	OD2-ETCH	A	
9	130	POLY-GATE-ETCH	A	
10	139	POLY-CUT-ETCH	A	
11	116	LDD-N-I/O-IMP	A	
12	113	LDD-P-CORE-IMP	A	
13	117	VT-P-CORE-LV-IMP	A	
14	11G	VT-P-PKT-HV-IMP	A	
15	199	VT-P-CELL-IMP	A	
16	123	SSD-ETCH	A	
17	115	LDD-P-I/O-IMP	A	
18	114	LDD-N-CORE-IMP	A	
19	11H	VT-N-CORE-HV-IMP	A	
20	112	VT-N-CELL-IMP	A	
21	197	S/D-P-IMP	A	
22	198	S/D-N-IMP	A	
23	111	ESD-P-IMP	A	
24	155	RPO-ETCH	A	
25	13A	SDS-HMR-SiGe-ETCH	A	
26	13D	MG-PM-HK-ETCH	A	
27	13F	MG-RESISTOR-HK-ETCH	A	
28	156	CONTACT-METAL-ETCH	A	
29	360	METAL1-CU-ETCH	A	
30	380	METAL2-CU-ETCH	A	
31	378	VIA1-CU-ETCH	A	
32	381	METAL3-CU-ETCH	A	
33	379	VIA2-CU-ETCH	A	
34	384	METAL4-CU-ETCH	A	
35	373	VIA3-CU-ETCH	A	
36	385	METAL5-CU-ETCH	A	
37	374	VIA4-CU-ETCH	A	
38	386	METAL6-CU-ETCH	A	
39	375	VIA5-CU-ETCH	A	
40	387	METAL7-CU-ETCH	A	
41	376	VIA6-CU-ETCH	A	
42	388	METAL8-CU-ETCH	A	
43	377	VIA7-CU-ETCH	A	
44	306	VIAR-AL-ETCH	A	
45	309	METALR-AL-ETCH	A	
46	308	PASSIVATION2-PAD-ETCH	A	

47	009	POLYIMIDE-NEGATIVE-PHO	A
48	020	UBM-BUMP-PHO	A

4.2 RFL Information

Confirm RFL : No

Layout Draft ID : No

FTP Server --

File Name --

User Name --

Password --

RFL special note :

5. Device Information

1. Basic Info.

1. Seal Ring

- (●) TSMC has to add seal ring
  - (●) TSMC standard
    - ( ) Rectangle (TSMC default seal ring shape for > 0.13 um technology)
    - (●) Octangle (TSMC default seal ring shape for <= 0.13 um technology)

      Specify the shape: Explanation of reserved area
      - ( ) Big CSR corner (For <= 0.13um and > 65nm technology)
      - ( ) Small CSR corner (For <= 0.13um and > 65nm technology)
      - (●) L-mark CSR corner (For <= 0.13um technology)
  - ( ) Approved customized seal ring. Please specify seal ring code :

    [ ]
- ( ) Customer added seal ring already
  - ( ) TSMC standard
  - ( ) Approved customized seal ring.

2. Tapeout database transfer method

DB check will be triggered automatically only if databases are ready in FTP server while MT submit

- (●) A single database under FTP server
- ( ) Separate to multiple databases under FTP server
- ( ) DB is not ready yet. Will FTP to tsmc server later (Please specify when the database will be ready in 'Customer Instruction')
- ( ) Load from old tapeout DB that mask was already made (please specify the old database source in 'Customer Instruction')

3. Database Information

FTP Server : ftp.tsmc.com.tw(HQ site) ▼ FTP User Name: iccan61 FTP User Password : [ ]

FTPed File Path/File Name : 2017.11.2.13.15.39/sirius_top_mrg_1101_1445.gds.gz.gpg

Uncomp GDS File Name : sirius_top_mrg_1101_1445.gds (case sensitive)

Uncomp GDS File Size : 96411854848 bytes (Please specify the size of the uncompressed file, not the compressed file.)

DB Format : (●) GDSII ( ) OASIS

SRAM Poly Gate direction on file for N45 and below only : (●) Vertical ( ) NONE

Gate Bias service : [ ] Sizing up [ ] Sizing down [x] None

TSMC IP Merge : Does this device need TSMC to merge any IP? ( ) Yes (●) No

Post Merge Database Information

File Path/File Name :

Uncompress File Name :

Uncompress File Size :

4. Window Description

1. GDS Data Window Coordinates :

X_Lower Left	0.0 um	Y_Lower Left	0.0 um
X_Upper Right	9450.0 um	Y_Upper Right	10000.0 um

2. Window Size : X = 9450.0 um Y = 10000.0 um

5. Shrink & Orientation

1. TSMC Applies Shrink : 90.0 % (100%=no shrink)
2. Database Scale : 1x
3. TSMC Rotation : (•) No ( ) 90 degree ( ) 180 degree ( ) 270 degree (Rotating counterclockwise)

6. Calma GDS-II Format

Structure Name : sirius_top (case sensitive. maximum: 127 characters)

7. Customer has completed DRC Design Rule Check

DRC Run by Customer : ( ) No (•) Yes

TSMC Command File Version : 22a

DRC Result : ( ) Pass (•) Fail

Have you informed customer service manager of the DRC errors and understood the risk level?

(•) Yes ( ) No

2. STI

1. IP

	Question	Answer	Mask code/CAD layer	Remark
1	OTP	Yes		
	OTP IP name (Exclude IP version)	KPTS28HPC128-R08W01-45C5PL-0V0		Pls seperate multiple IPs with a comma
	OTP vendor	Kilopass		
	OTP process category	STD		

2. COMMON

	Question	Answer	Mask code/CAD layer	Remark
1	Matching Circuit for MOS Array	MATCHING	MATCHING	MATCHING (205;8) is required for LVS and DRC CAD Layer.
		ANARRAY_M	ANARRAY_M	ANARRAY_M (255;21) is required for LVS and DRC CAD Layer.

3. FEOL

	Question	Answer	Mask code/CAD layer	Remark
1	1.8V under drive to 1.5V	(•) Yes	OD18_15	OD18_15 (16;4) is required for LVS and DRC CAD Layer.
		( ) No		
2	1.8V under drive to 1.2V	(•) Yes	OD18_12	OD18_12 (16;1) is required for LVS and DRC CAD Layer.
		( ) No		
3	SR_DPO	(•) Yes	SR_DPO	SR_DPO (17;7) is required for mask 13D,198,139,123,197,120,13A,130,156.

		○ No		
4	SR_DOD			SR_DOD layer is used for dummy od subject to logic bias and OPC.
		◉ Yes	SR_DOD	SR_DOD (6;7) is required for mask 198,120,130.
		○ No		
5	OD resistor	◉ Yes	RH_OD	RH_OD (117;1) is required for mask 116,114,115,113,123.
		○ No		
6	High-R resistor			High-R resistor is required both Mask 13Fand RH_PO(117;2) Non-High-R resistor is required RH_PO(117;2)
		◉ Yes	13F, RH_PO	Mask 13F is required. RH_PO (117;2) is required for mask 116,114,13D,115,113,123,120,155.
		○ No		
7	Inductor with NT_N			Inductor of TSMC PDK must use NT_N layer.
		○ Yes	NT_N	NT_N (11;0) is required for mask 116,114,191,193.
		◉ No		
8	Junction Diode	◉ Yes	DIODMY	DIODMY (119;0) is required for mask 198,123.
		○ No		
9	Low Leakage Diode	○ Yes	DIODMY_L	DIODMY_L (255;53) is required for mask 116,114,115,113.
		◉ No		
10	NMOS Ultra High VT	○ Yes	11B, VTUH_N	Mask 11B is required.
		◉ No		
11	PMOS Ultra High VT	○ Yes	11A, VTUH_P	Mask 11A is required.
		◉ No		
12	NMOS Ultra Low VT	○ Yes	11R, 118, VTUL_N, VTL_N	Mask 118 is required. Mask 11R is required.
		◉ No		
13	PMOS Ultra Low VT	○ Yes	11Q, VTUL_P	Mask 11Q is required.
		◉ No		
14	NMOS High VT	◉ Yes	11H, VTH_N	Mask 11H is required.
		○ No		
15	PMOS High VT	◉ Yes	11G, VTH_P	Mask 11G is required.
		○ No		
16	AVT mos device			AVT mos deivce (CORELDD_IO) tapeout or not
		○ Yes	AVT	AVT (207;10) is required for mask 116,114,191,193.
		◉ No		
17	HVNMOS	○ Yes	HVD_N	HVD_N (91;1) is required for mask 116,198,194,197,155,193.
		◉ No		
18	HVPMOS	○ Yes	HVD_P	HVD_P (91;2) is required for mask 115,198,194,197,155,193.
		◉ No		
19	Deep N-Well	○ Yes	119, DNW	DNW Mask 119 is required. DNW (1;0) is required for mask 119.

		◉ No		
20	NW resistor	○ Yes	NWDMY	NWDMY (114;0) is required for LVS and DRC CAD Layer.
		◉ No		
21	OD Dummy	◉ Yes	DOD	DOD (6;1) is required for dummy CAD layer.
		○ No		
22	POLY Dummy	◉ Yes	DPO	DPO (17;1) is required for dummy CAD layer.
		○ No		
23	Varactor	◉ Yes	VAR	VAR (143;0) is required for mask 116,114,115,113,123.
		○ No		
24	BJT device	◉ Yes	BJTDMY	BJTDMY (110;0) is required for mask 116,114,115,198,113,123.
		○ No		
25	SR_ESD			DRC dummy layer to waive RDR rules for ESD devices
		◉ Yes	SR_ESD	SR_ESD (121;0) is required for mask 123.
		○ No		
26	SRAM (0.9V)	Yes	112, 199, CO_12, CO_13, CO_16, PO_12, SRAMDMY;0, SRAMDMY;1, SRM, CO_15, CO_11, CO_14, PRBOUNDARY, RODMY	Mask 112 is required. Mask 199 is required. SRM (50;0) is required for mask 114,13D,198,113,139,123,197,120,130,156,192. SRAMDMY;0 (186;0) is required for mask 114,139,113,123,197,191,156,192,378,13D,198,120,130. PO_12 (17;12) is required for mask 139. CO_16 (30;16) is required for mask 156. CO_15 (30;15) is required for mask 156. CO_13 (30;13) is required for mask 156. CO_12 (30;12) is required for mask 156. SRAMDMY;1 (186;1) is required for mask 120,130. PRBOUNDARY (108;0) is required for LVS and DRC CAD Layer. RODMY (49;0) is required for LVS and DRC CAD Layer. CO_14 (30;14) is required for LVS and DRC CAD Layer. CO_11 (30;11) is required for OPC Blocking CAD layer.
	TSMC N28 GL SRAM bit cell	SP-HD 0.127 um^2 (drawing 0.156 um^2)	SRM_10	SRM_10 (50;10) is required for mask 198,123,197,120,191,130,156.
		SP-HC 0.155 um^2 (drawing 0.192 um^2)	SRM_11	SRM_11 (50;11) is required for mask 198,123,197,120,191.
		DP-HC 0.315 um^2 (drawing 0.389 um^2)	SRM_13	SRM_13 (50;13) is required for mask 120,130.
		TP-8T-HC-MUXN 0.24 um^2 (drawing 0.297um2)	SRM_18	SRM_18 (50;18) is required for mask 120,130,156.
	Other Bit cell	No		The SRAM in [others] will not be carried into logic operation for mask making at this moment. If you cannot find the bit cell you want in the options above, please contact tsmc.
	Memory size	52,622400?		
	SRAM Poly Orientation	Vertical Poly		All SRAM device (both N and P) requires Poly in single orientation
27	LL SRAM(1.0V)	No		
28	Native VT	◉ Yes	NT_N	NT_N (11;0) is required for mask 116,114,191,193.
		○ No		
29	NMOS Core Low VT	◉ Yes	118, VTL_N	Mask 118 is required.

		○ No		
30	PMOS Core Low VT	◉ Yes	117, VTL_P	Mask 117 is required.
		○ No		
31	ESD	◉ Yes	111, ESDIMP	ESDIMP Mask 111 is required. ESDIMP (189;0) is required for mask 111.
		○ No		
32	Dummy TCD insertion			Dummy TCD is a must. Pls refer to DRM if choose "No". Dummy TCD Cad layer [FEOL]: TCDDMY(165;1), TCDDMY_H(165;4), TCDDMY_V(165;5), TCDDMY_FH(165:6), TCDDMY_FV(165;7); [BEOL]:TCDDMY_M1(165;61), TCDDMY_FM1(165;31) are required to mark Dummy TCD area.
		◉ Yes	TCDDMY, TCDDMY_FH, TCDDMY_FV	TCDDMY_FH (165;6) is required for LVS and DRC CAD Layer. TCDDMY_FV (165;7) is required for LVS and DRC CAD Layer. TCDDMY (165;1) is required for LVS and DRC CAD Layer.
		○ No		
33	HIA Diode	◉ Yes	HIA_DUMMY, HIA_DUMMY	HIA_DUMMY (168;0) is required for mask 198. HIA_DUMMY (168;0) is required for LVS and DRC CAD Layer.
		○ No		
34	In-chip OVL Insertion			In-chip OVL is a must for the big die such as 1x1, 1x2, 2x1 and refers to DRM. In chip OVL Cad layer ICOVL(165;3) is required to mark in chip OVL area
		○ Yes	ICOVL, ICOVL	ICOVL (165;3) is required. ICOVL (165;3) is required for LVS and DRC CAD Layer.
		◉ No		

4. METAL

	Question	Answer	Mask code/CAD layer	Remark
	No. of metal layers (Excluding RDL(MD) Layer)	8		
	No. of std inter metal	6		Std inter metal includes M1
	M7/V6 feature	Std. thick Metal Mz-8XTM		
	M8/V7 feature	Std. thick Metal Mz-8XTM		

5. BEOL

	Question	Answer	Mask code/CAD layer	Remark
1	CO_VIRT			Currently, TSMC will request to tape out M1/CO masks both if Retool CO mask due to M1 OPC reference. If you wants to retool CO layer only for ROM revison, please provide CO_VIRT.
		○ Yes	CO_VIRT	CO_VIRT (30;30) is required for mask 360.
		◉ No		
2	Metal fuse by circuit trim	No		
3	Dummy Metal	Yes		
	Dummy Metal layer	M1	DM1	DM1 (31;1) is required for dummy CAD layer.
		M2	DM2	DM2 is required for dummy CAD layer.
		M3	DM3	DM3 is required for dummy CAD layer.

		M4	DM4	DM4 is required for dummy CAD layer.
		M5	DM5	DM5 is required for dummy CAD layer.
		M6	DM6	DM6 is required for dummy CAD layer.
		M7	DM7	DM7 is required for dummy CAD layer.
		M8	DM8	DM8 is required for dummy CAD layer.
4	Dummy Via (DVIAx)	Yes		DVIAx (dummy Via) is for VIAx only. And is must for flip-chip and WLCSP. Please have DVIAx in the gds..
	Dummy Via (DVIAx) layer	DVIA1	DVIA1	DVIA1 (51;1) is required for dummy CAD layer.
		DVIA2	DVIA2	DVIA2 (52;1) is required for dummy CAD layer.
		DVIA3	DVIA3	DVIA3 (53;1) is required for dummy CAD layer.
		DVIA4	DVIA4	DVIA4 (54;1) is required for dummy CAD layer.
		DVIA5	DVIA5	DVIA5 (55;1) is required for dummy CAD layer.
5	Virtual VIAx (VIAx_VIRT)	Yes		Virtual VIAx for Mx/x+1 mask OPC reference in ROM region. (Only for Vx, not Vy/Vz/Vr/Vu)
	Virtual VIAx (VIAx_VIRT) layer	VIA1_VIRT	VIA1_VIRT	VIA1_VIRT (51;200) is required for mask 380,360.
6	OPC Dummy metal	Yes		
	OPC Dummy Metal layer	M1	DM1_O	DM1_O (31;7) is required for mask 360.
		M2	DM2_O	DM2_O is required for mask 380.
		M3	DM3_O	DM3_O is required for mask 381.
		M4	DM4_O	DM4_O is required for mask 384.
		M5	DM5_O	DM5_O is required.
		M6	DM6_O	DM6_O is required.
7	MOM	Yes		
	If use TSMC MOM IP	◉ Yes		
		○ No		
	MOM Stacking metal layer (e.g: M1-M4)	M1-M6		

6. TOP MODULE

	Question	Answer	Mask code/CAD layer	Remark
1	CUP(Circuit under pad)	○ Yes	WBDMY	WBDMY (157;0) is required for LVS and DRC CAD Layer.
		◉ No		
2	Add Sealring by customer	○ Yes	SEALRING, SEALRING_ALL	SEALRING (162;0) is required for mask 123. SEALRING_ALL (162;2) is required for mask 123,307,309.
		◉ No		
3	RDL	AP RDL	306, 309	Mask 306,309 is required.
	Flip chip, Wire bond, WLCSP or CoWoS (Micro bump)			For WLCSP,please must inform TSMC for service supporting
		Flip chip	RV, AP, CB2_FC	RV (85;0) is required for mask 306. CB2_FC (86;0) is required for mask 308. AP (74;0) is required for mask 309.
	Ground-up pad	○ Yes	CBD	CBD (169;0) is required for mask 107,306.
		◉ No		

4	Polyimide (in Fab)	Yes	009, PM	PM Mask 009 is required. PM (5;0) is required for mask 009.
	Polyimide material	HD4104		

7. BP: Bumping

	Question	Answer	Mask code/CAD layer	Remark
1	Solder Type	Leadfree		
	Bump Ag composition (%)	TSMC STD 1.8%		
	Substrate type	Build up (BU, FCBGA)		Required total top metal thickness >= 1VIAz + 1Mz for N16~45 LF bump with Laminate substrate. Required total top metal thickness >= 1VIAz + 1Mz for N16~45 LF bump with BU substrate core thickness >= 800um and dies size =< 100mm2. Require total top metal thickness >= 2VIAz + 2Mz for N16~45 LF bump other than BU substrate core thickness >= 800um and dies size > 100mm2. Al Pad RDL thickness must = 28KA for N16~45 LF bump according to design rule define.
	Bump density	>= 9%		TSMC recommend LF bump density >=10% and <=26%.
	Bump Pitch (um)	150<=P<160		Please contact TSMC as die size > 400mm2.
	UBM Width (um)	80		Please contact TSMC as die size > 400mm2.
	Bump height (um)	75		Please contact TSMC as die size > 400mm2.
	No. of bumps per chip	2738		
	Bump site	TSMC in-house		1. "TSMC in-house" means that the bump processed in TSMC bump line; "Outsourcing" means that customer appoint tsmc to do bump process in other bump foundry 2. If need "Outsourcing" service, please contact TSMC Backend Turnkey team before product tape out
	BackLap after Bump			1. Include doing backlapping at TSMC or other company. 2. TSMC provide polyimide surface treatment process based on with or without backlapping process (tape/de-tape on wafer front side) after bump. Please confirm your product information if correct.
		○ Yes		
		◉ No		

3. MT Layers

No.	Tooling All tapeout All tapeout later All dry run	Process Layer ID	Name	Service Stage	Ver.	Code/ Option	Circuit Pattern CAD Layer Name	Drawing CAD Layer #	LOGO ○ Y ◉ N	Digitized Area Tone	TSMC applied bias/logic
1	tapeout	120	OD1-ETCH	WF	A		OD	6;0		D	TSMC standard
2	tapeout	121	ODR-ETCH	WF	A		OD_18	16;0		C	TSMC

										standard
3	tapeout	191	WELL-P-CORE-IMP	WF	A	LOGICAL OPR		D	TSMC standard
4	tapeout	118	VT-N-CODE-LV-IMP	WF	A	VTL_N	12;0	D	TSMC standard
5	tapeout	193	WELL-P-I/O-IMP	WF	A	LOGICAL OPR		C	TSMC standard
6	tapeout	192	WELL-N-CORE-IMP	WF	A	NW	3;0	C	TSMC standard
7	tapeout	194	WELL-N-I/O-IMP	WF	A	LOGICAL OPR		C	TSMC standard
8	tapeout	152	OD2-ETCH	WF	A	OD_18	16;0	D	TSMC standard
9	tapeout	130	POLY-GATE-ETCH	WF	A	PO	17;0	D	TSMC standard
10	tapeout	139	POLY-CUT-ETCH	WF	A	PO_11	17;11	C	TSMC standard
11	tapeout	116	LDD-N-I/O-IMP	WF	A	LOGICAL OPR		C	TSMC standard
12	tapeout	113	LDD-P-CORE-IMP	WF	A	LOGICAL OPR		C	TSMC standard
13	tapeout	117	VT-P-CORE-LV-IMP	WF	A	VTL_P	13;0	C	TSMC standard
14	tapeout	11G	VT-P-PKT-HV-IMP	WF	A	VTH_P	68;0	C	TSMC standard
15	tapeout	199	VT-P-CELL-IMP	WF	A	LOGICAL OPR		C	TSMC standard
16	tapeout	123	SSD-ETCH	WF	A	LOGICAL OPR		C	TSMC standard
17	tapeout	115	LDD-P-I/O-IMP	WF	A	LOGICAL OPR		C	TSMC standard
18	tapeout	114	LDD-N-CORE-IMP	WF	A	LOGICAL OPR		C	TSMC standard
19	tapeout	11H	VT-N-CORE-HV-IMP	WF	A	VTH_N	67;0	C	TSMC standard
20	tapeout	112	VT-N-CELL-IMP	WF	A	LOGICAL OPR		C	TSMC standard
21	tapeout	197	S/D-P-IMP	WF	A	PP	25;0	C	TSMC standard
22	tapeout	198	S/D-N-IMP	WF	A	NP	26;0	C	TSMC standard
23	tapeout	111	ESD-P-IMP	WF	A	ESDIMP	189;0	C	TSMC standard
24	tapeout	155	RPO-ETCH	WF	A	RPO	29;0	D	TSMC standard
25	tapeout	13A	SDS-HMR-SiGe-ETCH	WF	A	LOGICAL OPR		C	TSMC standard
26	tapeout	13D	MG-PM-HK-ETCH	WF	A	PMET_DRAW	205;6	D	TSMC standard
27	tapeout	13F	MG-RESISTOR-HK-ETCH	WF	A	LOGICAL OPR		C	TSMC standard
28	tapeout	156	CONTACT-METAL-ETCH	WF	A	CO	30;0	C	TSMC standard
29	tapeout	360	METAL1-CU-ETCH	WF	A	M1	31;0	C	TSMC standard
30	tapeout	380	METAL2-CU-ETCH	WF	A	M2	32;0	C	TSMC standard
31	tapeout	378	VIA1-CU-ETCH	WF	A	V1	51;0	C	TSMC standard
32	tapeout	381	METAL3-CU-ETCH	WF	A	M3	33;0	C	TSMC standard

33	tapeout	379	VIA2-CU-ETCH	WF	A	V2	52;0	C	TSMC standard
34	tapeout	384	METAL4-CU-ETCH	WF	A	M4	34;0	C	TSMC standard
35	tapeout	373	VIA3-CU-ETCH	WF	A	V3	53;0	C	TSMC standard
36	tapeout	385	METAL5-CU-ETCH	WF	A	M5	35;0	C	TSMC standard
37	tapeout	374	VIA4-CU-ETCH	WF	A	V4	54;0	C	TSMC standard
38	tapeout	386	METAL6-CU-ETCH	WF	A	M6	36;0	C	TSMC standard
39	tapeout	375	VIA5-CU-ETCH	WF	A	V5	55;0	C	TSMC standard
40	tapeout	387	METAL7-CU-ETCH	WF	A	M7	37;40	C	TSMC standard
41	tapeout	376	VIA6-CU-ETCH	WF	A	V6	56;40	C	TSMC standard
42	tapeout	388	METAL8-CU-ETCH	WF	A	M8	38;40	C	TSMC standard
43	tapeout	377	VIA7-CU-ETCH	WF	A	V7	57;40	C	TSMC standard
44	tapeout	306	VIAR-AL-ETCH	WF	A	RV	85;0	C	TSMC standard
45	tapeout	309	METALR-AL-ETCH	WF	A	AP	74;0	D	TSMC standard
46	tapeout	308	PASSIVATION2-PAD-ETCH	WF	A	CB2_FC	86;0	C	TSMC standard
47	tapeout	009	POLYIMIDE-NEGATIVE-PHO	WF	A	PM	5;0	D	TSMC standard
48	tapeout	020	UBM-BUMP-PHO	BP	A	UBM	170;0	D	TSMC standard

4. Tape-out Layer Usage

No	Tape Out Layer Usage	Circuit Layer
1	ANARRAY_M	255;21
2	AP	74;0
3	BJTDMY	110;0
4	CB2_FC	86;0
5	CO	30;0
6	CO_11	30;11
7	CO_12	30;12
8	CO_13	30;13
9	CO_14	30;14
10	CO_15	30;15
11	CO_16	30;16
12	DIODMY	119;0
13	DM1	31;1
14	DM1_O	31;7
15	DM2	32;1
16	DM2_O	32;7
17	DM3	33;1
18	DM3_O	33;7
19	DM4	34;1
20	DM4_O	34;7
21	DM5	35;1
22	DM5_O	35;7

23	DM6	36;1
24	DM6_O	36;7
25	DM7	37;41
26	DM8	38;41
27	DOD	6;1
28	DPO	17;1
29	DVIA1	51;1
30	DVIA2	52;1
31	DVIA3	53;1
32	DVIA4	54;1
33	DVIA5	55;1
34	ESDIMP	189;0
35	HIA_DUMMY	168;0
36	M1	31;0
37	M2	32;0
38	M3	33;0
39	M4	34;0
40	M5	35;0
41	M6	36;0
42	M7	37;40
43	M8	38;40
44	MATCHING	205;8
45	NP	26;0
46	NT_N	11;0
47	NW	3;0
48	OD	6;0
49	OD18_12	16;1
50	OD18_15	16;4
51	OD_18	16;0
52	PM	5;0
53	PMET_DRAW	205;6
54	PO	17;0
55	PO_11	17;11
56	PO_12	17;12
57	PP	25;0
58	PRBOUNDARY	108;0
59	RH_OD	117;1
60	RH_PO	117;2
61	RODMY	49;0
62	RPO	29;0
63	RV	85;0
64	SRAMDMY;0	186;0
65	SRAMDMY;1	186;1
66	SRM	50;0
67	SRM_10	50;10
68	SRM_11	50;11
69	SRM_13	50;13
70	SRM_18	50;18
71	SR_DOD	6;7
72	SR_DPO	17;7
73	SR_ESD	121;0
74	TCDDMY	165;1

75	TCDDMY_FH	165;6
76	TCDDMY_FV	165;7
77	UBM	170;0
78	V1	51;0
79	V2	52;0
80	V3	53;0
81	V4	54;0
82	V5	55;0
83	V6	56;40
84	V7	57;40
85	VAR	143;0
86	VIA1_VIRT	51;200
87	VTH_N	67;0
88	VTH_P	68;0
89	VTL_N	12;0
90	VTL_P	13;0