ARM® Mali™-Display Processors

ARM

Media Processing Group

March 2016

Mali-Display Products

Mali-DP650
- Split display mode
- Variable refresh rate
- Optimized for 2.5K

Mali-DP550
- 7 layer composition
- Co-processor interface
- Optimized for HD and Full HD

Mali-DP500
- Up to 4K display
- Secure display layer
- AFBC

- Composition, rotation, high quality scaling in a single pass
- Rich set of image processing functions
- Supports ARM Frame Buffer Compression (AFBC)
- Delivered with support for the latest version of Android™ optimized to work alongside Mali-GPU and Mali-Video drivers
- Display timing compatible with MIPI, VESA, CEA, HDMI
- Support for dual-display Android use-cases
- Support for secure video playback and trusted UI

Mali-DP550		Mali-DP650	
HD 720 1280 x 720p	Full HD 1920 x 1080p	WQHD/WQXGA 2560 x1440p/1600p	UHD (4K) 3840 x 2160p

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Mali-DP650: 4K mobile display processor

2x System Performance

Power efficiency

High Resolution

- Up to 4K UHD 2160p60 display performance
  - Enables composition use cases for resolutions beyond 1080p (Full HD) up to 4K(UHD)
  - Split-display mode enables MIPI D-PHY solutions to deliver 4K to mobile panels
- Significant system power reduction
  - >25% for 1440p/1600p; >50% at 4K, compared to Mali-DP550
  - Offloading complex presentation functions from the CPU, GPU and VPU
    - Composition, rotation, scaling, image processing, etc..
- Most efficient way to collect, enhance and deliver content to the panel
  - AndroidTM Software optimized to work alongside the Mali-GPU and Mali-VPU driver
  - ARM Frame Buffer Compression (AFBC) and TrustZone Media Protection (TZMP)
  - Co-processor interface enables further differentiation (HDR, CABC, LABC etc..)

Mali-DP550: Area efficient display processor

Area saving
25% to 40%

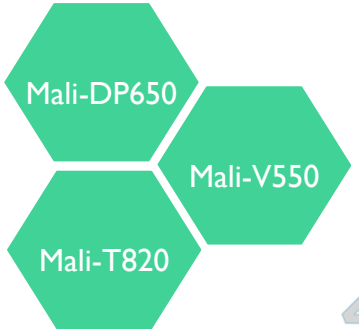
Power efficiency

Time to market

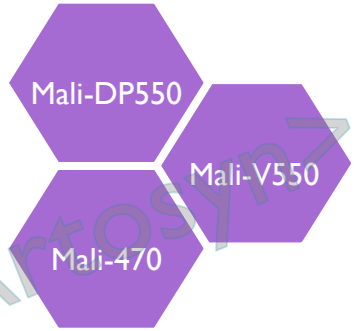
- Low cost display processor for 720p and 1080p panels
  - Targeting mobile and non-mobile (e.g. Industrial, IoT) applications
  - Enables efficient composition of up to 7 display layers
  - Display timing compatible with MIPI, VESA, CEA, HDMI
- Significant power reduction
  - Offloading complex presentation functions from the CPU, GPU and VPU
    - composition, rotation, scaling, image processing, etc..
- Most efficient way to collect, enhance and deliver to panels up to Full HD
  - Android™ Software optimized to work alongside the Mali-GPU and Mali-VPU driver
  - ARM Frame Buffer Compression (AFBC) and TrustZone Media Protection (TZMP)
  - Co-processor interface enables further differentiation (HDR, CABC, LABC etc..)

ARM Multimedia Suite: Better Together

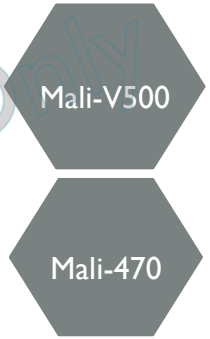
Premium mobile



Mass Market mobile



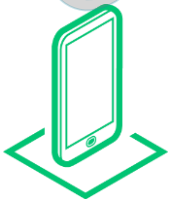
Entry level mobile



Wearables

Cortex, CoreLink, Physical IP, Tools

Highest performance
latest features



Balanced cost and
performance

Cost optimised
rich multimedia

Mobile experience
everywhere

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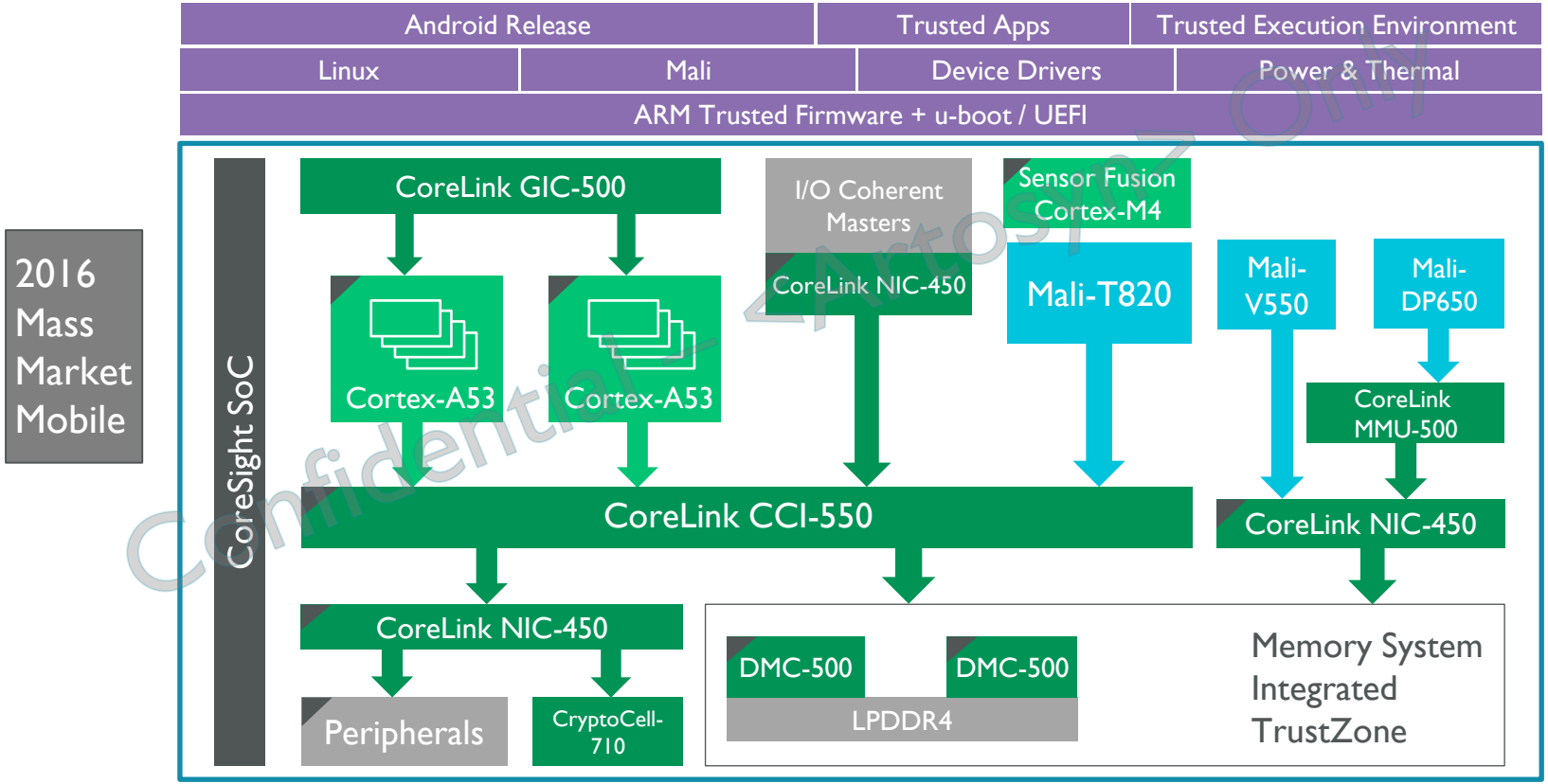
Mali-DP650 in an example Mass Market Mobile SoC



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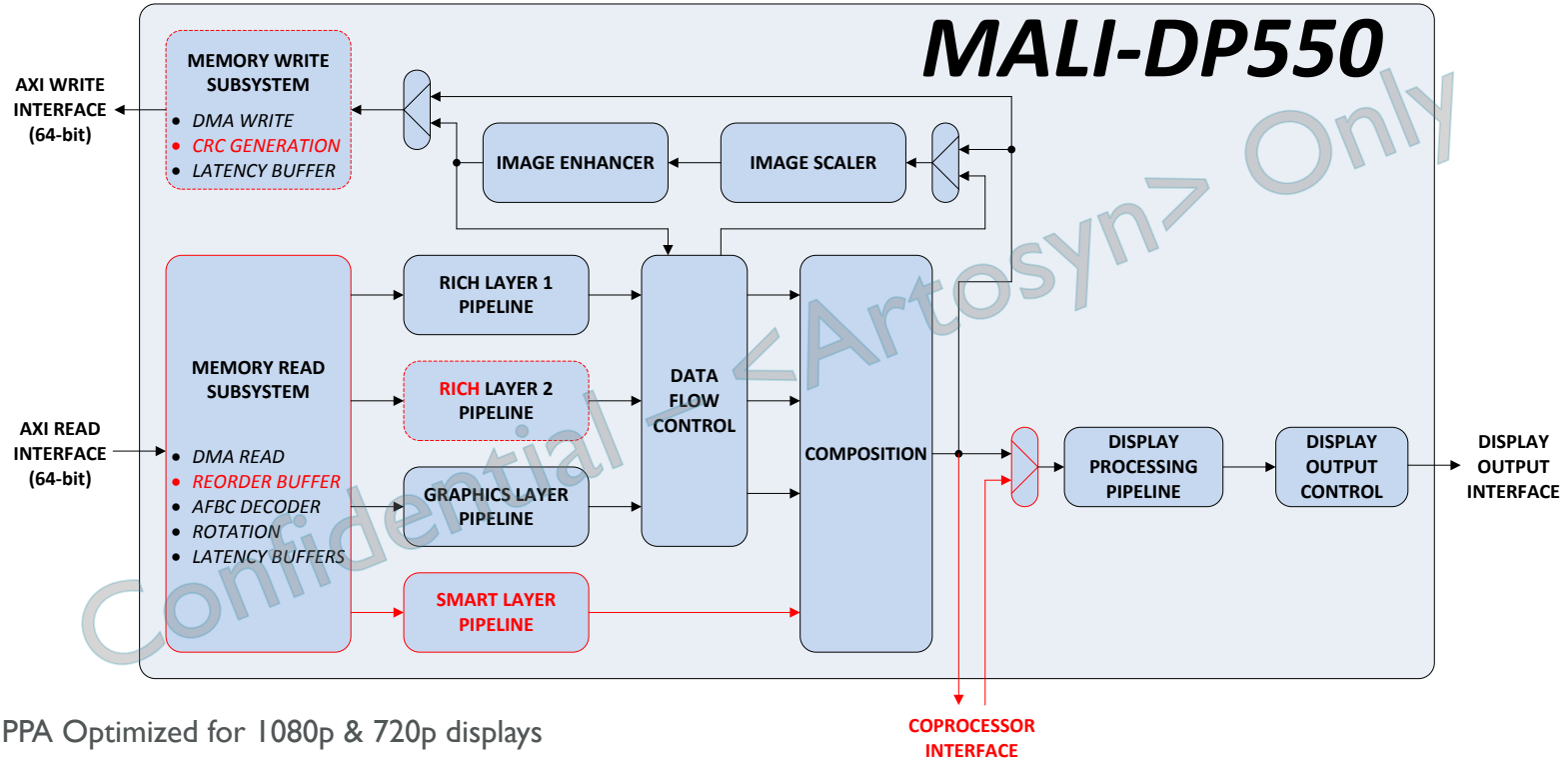
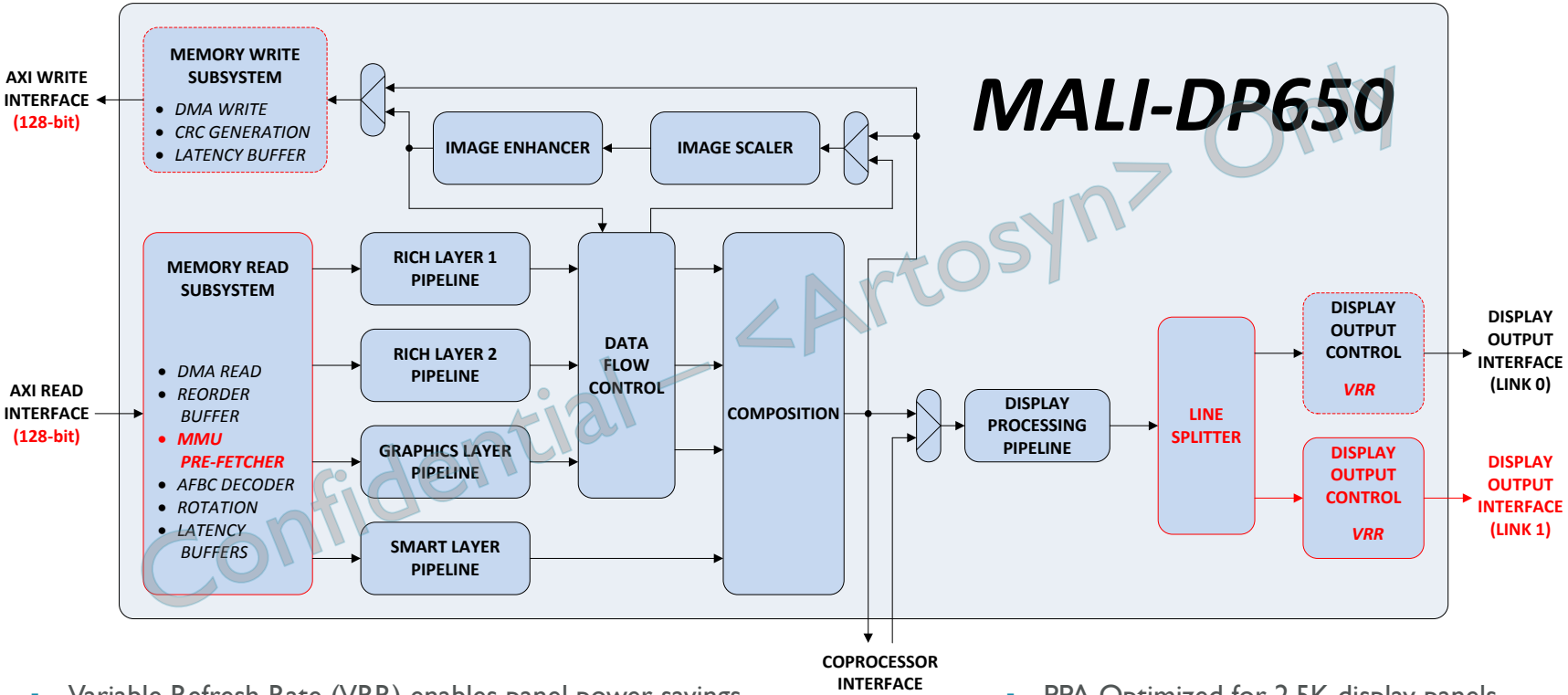
Mali-DP550 evolution



- PPA Optimized for 1080p & 720p displays
- Smart Layer enables efficient composition of up to 7 display layers
- Co-processor interface enables the insertion of 3rd party/proprietary IP to the display pipeline

Mali-DP650 evolution



- Variable Refresh Rate (VRR) enables panel power savings
- MMU pre-fetcher reduces impact of Page table walk latency
- 128-bit AXI enables up to 2x performance gains
- PPA Optimized for 2.5K display panels
- Line Splitter enables >1080p mobile displays

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Mali-Display processors die area

Configuration	*Line size*
HD	1280
2K	2048
QHD	2560
4K	4096

SD = Single Display Core

DD = Dual Display Core

- ***MALI-DP500 - TSMC 28HPM library:***

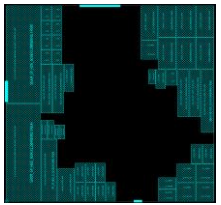
Configuration	SD_2K	SD_4K	DD_2K	DD_4K
Die area (mm^2)	0.78	1.01	1.78	2.25

- ***MALI-DP550 - TSMC 28HPM library:***

Configuration	SD_HD	SD_2K	SD_4K	DD_HD	DD_2K	DD_4K
Die area (mm^2)	0.98	1.18	1.6	1.97	2.43	3.16

- ***MALI-DP650 - TSMC 16FPLL library:***

Configuration	SD_QHD	SD_4K	DD_QHD	DD_4K
Die area (mm^2)	0.91	1.10	1.7	2.2



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Mali-DP550 r0p2 and Mali-DP650 r0p2 area comparison – SD 4K

TSMC 28HPM SVT C31 0.9V					
Design	**Std. cells area [mm²]**	**Memory area [mm²]**	**Design area [mm²]**	**Die area [mm²]**	**Overall RAM size [KB]**
Mali-DP550	0.48	0.93	1.41	**1.60**	571.5
Mali-DP650	0.61	1.04	1.65	**1.90**	639.25

TSCM 16FF+								
Design configuration	**Std. cells area [mm²]**		**Memory area [mm²]**		**Design area [mm²]**		**Die area [mm²]**		**Overall RAM size [KB]**
	LVT[1)]	**LVT UD[2)]**	**LVT**	**LVT UD**	**LVT**	**LVT UD**	**LVT**	**LVT UD**	
Mali-DP550	0.21	0.22	0.60	0.60	0.81	0.82	0.94	**0.95**	571.5
Mali-DP650	0.25	0.26	0.68	0.68	0.93	0.94	1.10	**1.11**	639.25

1) Library: TSMC 16FF+ LVT C16, 7.5-track, 9 metal layers, 0.8 V
2) Library: TSMC 16FF+ LVT C16, 7.5-track, 9 metal layers, 0.7 V (underdrive)

Mali-DP550 and Mali-DP650 power consumption

Operating point	Use-case(1)	ACLK(MHz)		Total power (mW)	
		DP550	DP650	DP550	DP650
1600p60	Min power	700	350	12.7	12.7
	Typical power	700	350	19.8	19.0
	Max power	700	350	52.9	**39.5**
2160p60	Min power	700	500	17.7	20.5
	Typical power	700	500	28.8	32.3
	Max power	700	500	102.3	**53.4**

- Analysed for TSMC 16FPLL, LVT UD, 0.7v, C16 library
- PVT corner = (tt, 0.7 V, 85 C), gate-level power analysis with switching activity taken from post place & route netlist simulation
- Mali-DP650 uses SD_QHD config for1600p60. Mali-DP550 uses SD_4K config for1600p60
- PXLCLK and MCLK frequency assumed 268.5MHz for 1600p60, 533.3MHz for 2160p60

(1)

Min Power	One full-screen graphics layer active, AFBC disabled, XRGB 8888 format
Typical Power	Graphics layer (full-screen) and smart layer (status bar + navigation bar) are active. Formats are ARGB 8888. Graphics layer is AFBC compressed.
Maximum Power	All layers are active. Video 1 in YUV 4:2:0 format is AFBC compressed and up-scaled. Video 2 is non-compressed and rotated. Smart layer consists of 2 rectangles. All processing functions enabled.

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Mali-Display processor – Types of layers

Graphics layer

- Single rectangle read from memory
- Only graphics formats supported
- AFBC supported
- Rotation and flips supported only for compressed layers
- Scaling supported

Smart layer

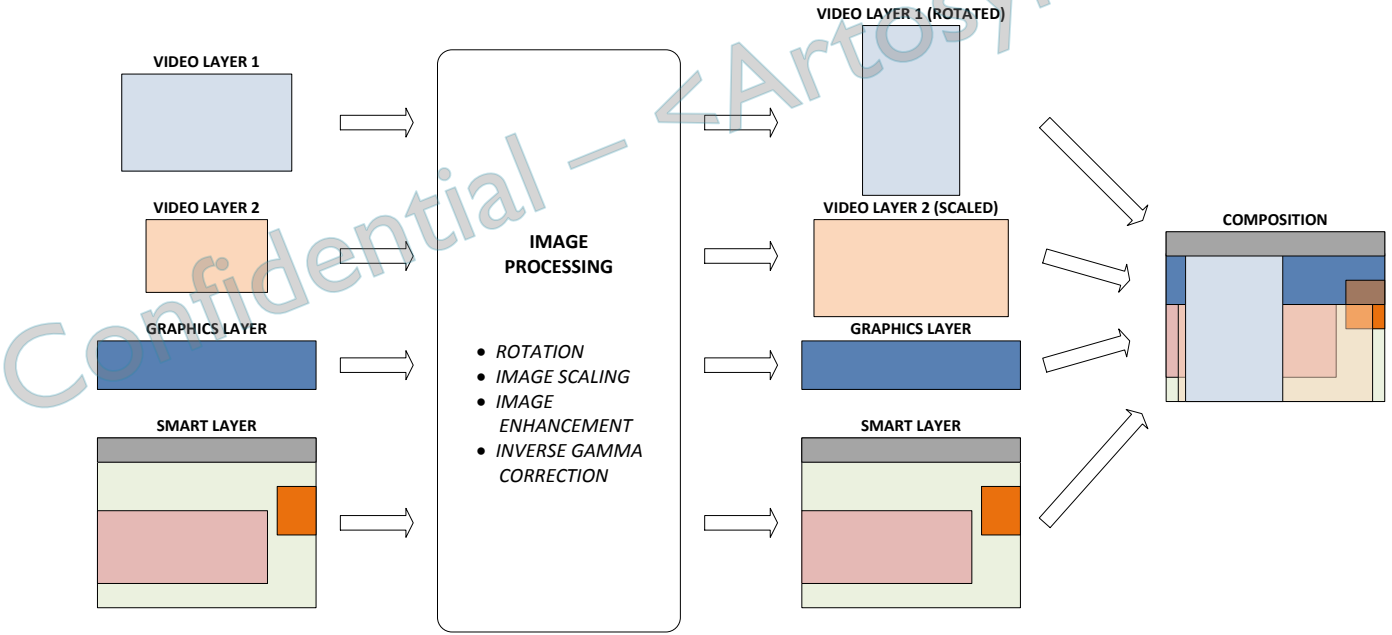
- Up to four rectangles read from memory and placed in smart layer bounding box
- Only 32-bit graphics formats supported
- AFBC not supported
- Rotation and flips not supported
- Scaling not supported

Rich layer

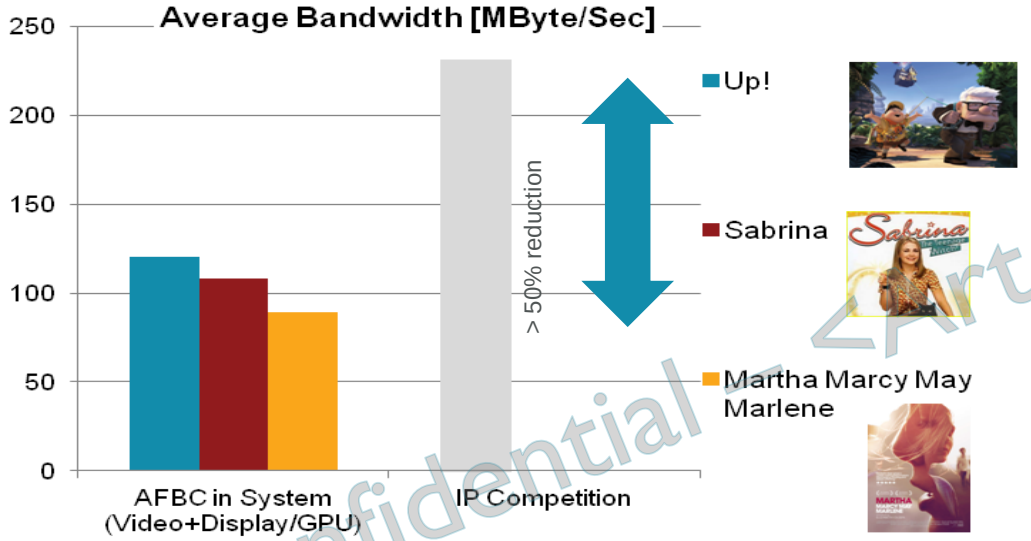
- Graphics layer with Video support
- Single rectangle read from memory
- AFBC supported
- Rotation and flips supported
- Scaling supported

Mali-Display composition

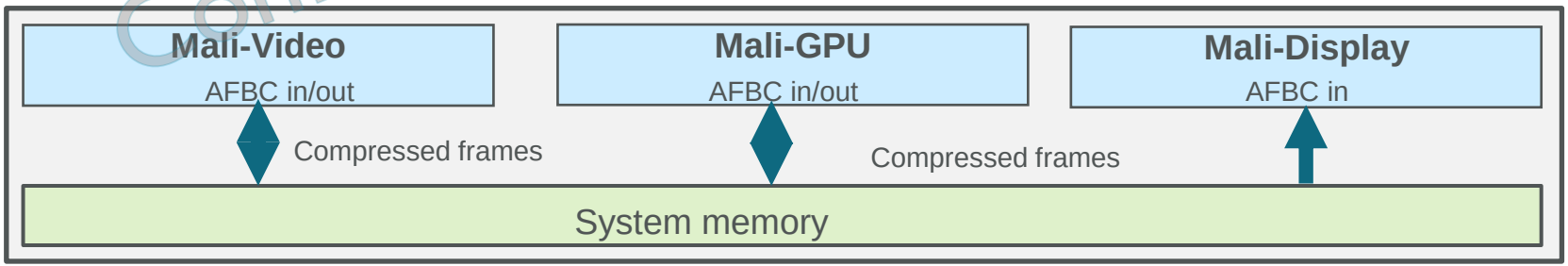
- Up to four layers
- Support for alpha blending
- Support for chroma keying
- Programmable composition offsets for each layer



System Bandwidth Reduction with AFBC



- Designed for video and graphics
- Lossless
- Real time compression
- Random access
- Block based (down to 4x4)



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Rotation

- *Rotation 90°, 180°, 270°*
- *Horizontal flip*
- *Vertical flip*

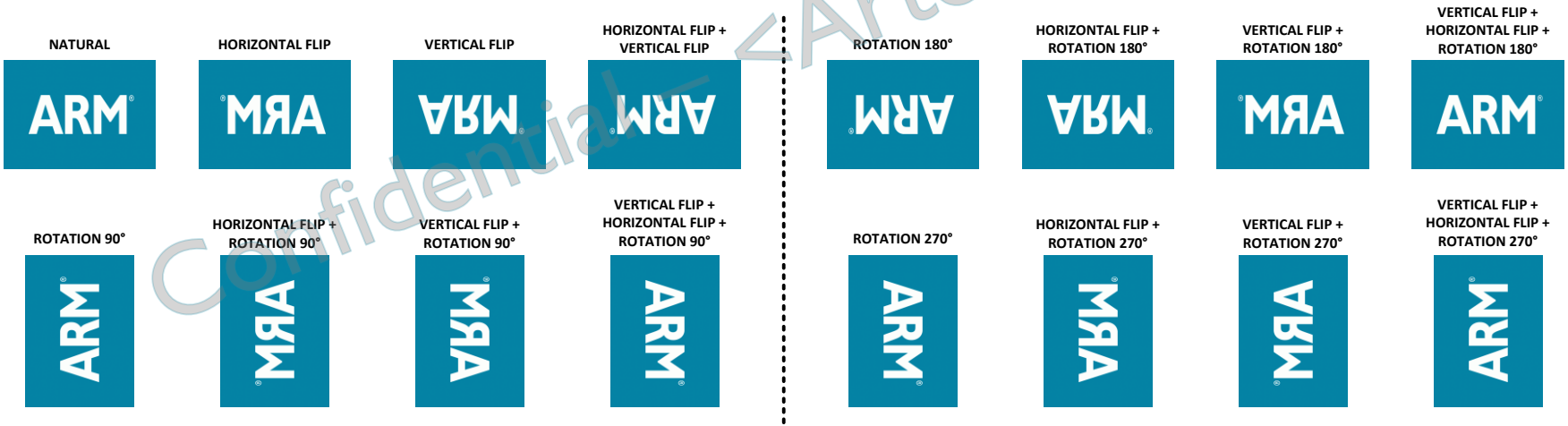
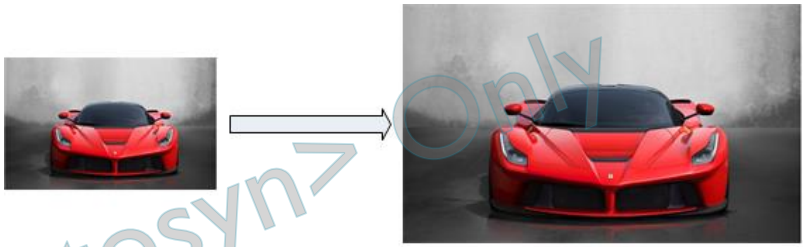


Image scaling / image enhancement

Image scaling

- High quality polyphase filtering algorithm
- Up-scaling limited by maximal display resolution
- Down-scaling up to 4x in each direction
- Scaling with single pixel accuracy
- Scaling of alpha component
- Programmable filter coefficients



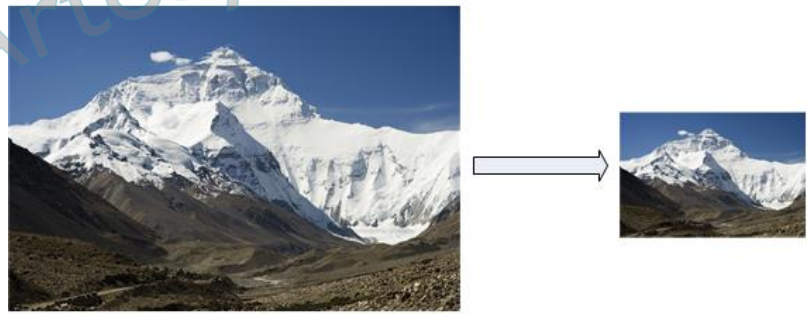
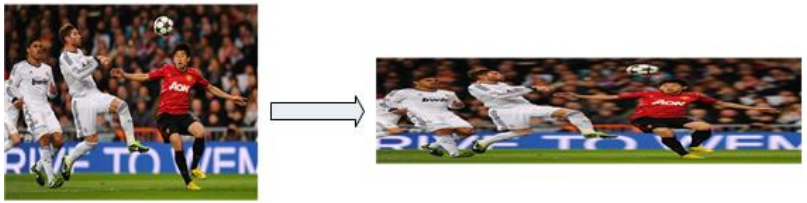


Image enhancement

- Detection of blurred edges
- Sharpening of the blurred edges
- Programmable filter coefficients



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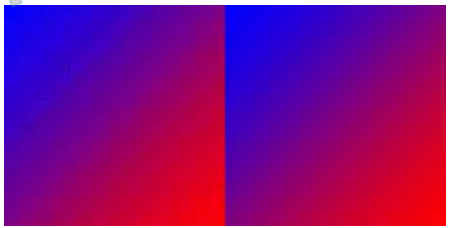
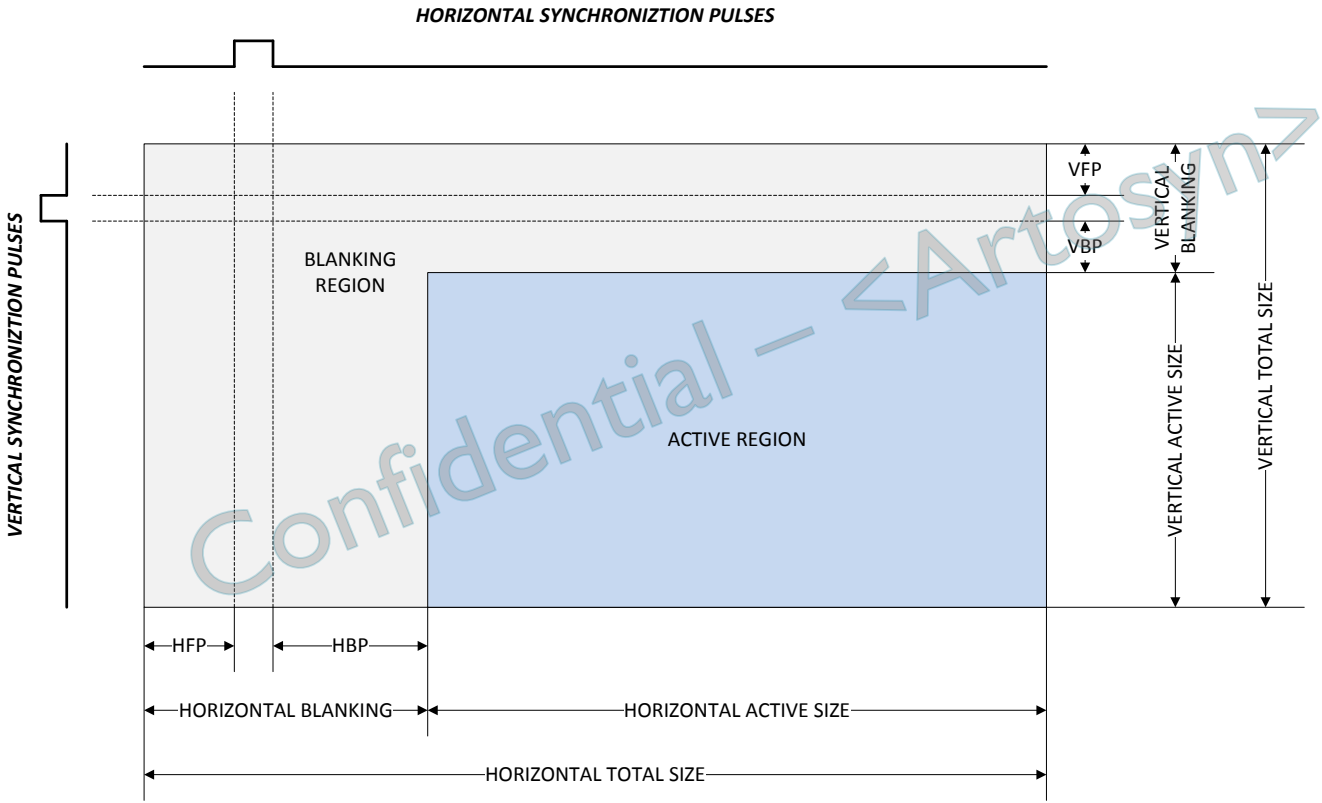
Other image processing functions

- Inverse gamma correction *(layer content)*
- YUV to RGB colour space conversion *(layer content)*
- Gamma correction *(display output content)*
- Colour adjustment *(display output content)*
- Dithering *(display output content)*
- RGB to YUV colour space conversion *(write-back content)*



Display timing generation



HFP - HORIZONTAL FRONT PORCH

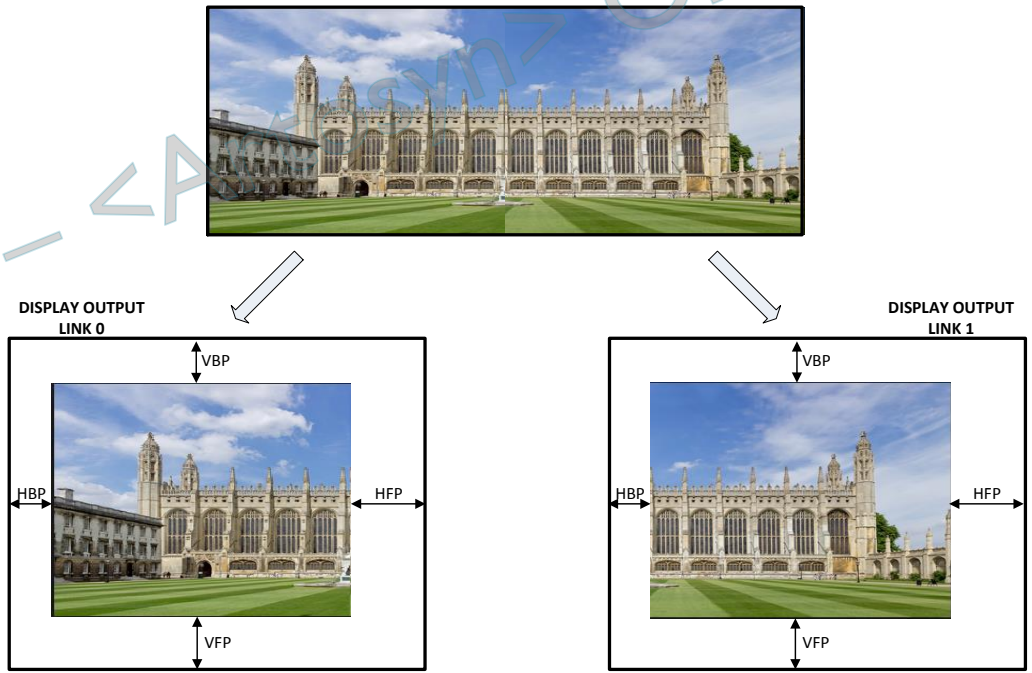
HBP - HORIZONTAL BACK PORCH

VFP - VERTICAL FRONT PORCH

VBP - VERTICAL BACK PORCH

Mali-DP650 Line splitter

- Allows two separate MIPI DSI transmitters to be driven in parallel by dividing the output line into two halves
- Full timing (porches, synchronization pulses) generated separately for each half
- Doubles the available data rate making display resolutions between 1080p and 4K a reality on a mobile or tablet devices



Mali-DP650 Variable Refresh Rate

- Sending output frames to the panel at 60Hz when displaying static content is detrimental to mobile battery life

- To counter that, Mali-DP650 supports Variable Refresh Rate (VRR) – where the frame rate can change dynamically through SW intervention
  - The software driver, when programming a scene, informs the hardware how long that particular frame should stay in VBLANK for by modifying the VFP values for the frame.
  - The VSYNC event provided by the driver to Android would be affected by whatever rate that particular frame was running at

- The lowest frame rate will depend on the panel itself but a typical target would be 30Hz, which contributes to a longer battery life

Mali-Display supported input pixel formats

Graphics formats	Video formats

• 32-bit RGB formats:
  • ARGB 2-10-10-10, ABGR 2-10-10-10, RGBA 10-10-10-2, BGRA 10-10-10-2
  • ARGB 8-8-8-8, ABGR 8-8-8-8, RGBA 8-8-8-8, BGRA 8-8-8-8
  • XRGB 8-8-8-8, XBGR 8-8-8-8, RGBX 8-8-8-8, BGRX 8-8-8-8
• 24-bit RGB formats:
  • RGB 8-8-8, BGR 8-8-8
• 16-bit RGB formats:
  • RGBA 5-5-5-1, ABGR 1-5-5-5
  • RGB 5-6-5, BGR 5-6-5
	• 8-bit per sample YUV formats:
	  • XYUV 444-P1-8
	  • YUV 422-P2-8
	  • VYUY 422-P1-8, YVYU 422-P1-8
	  • YUV 420-P1-8
	  • YUV 420-P2-8
	  • YUV 420-P3-8
	• 10-bit per sample YUV formats:
	  • XYUV 444-P1-10
	  • YUV 420-P1-10
	  • YUV 420-P2-10

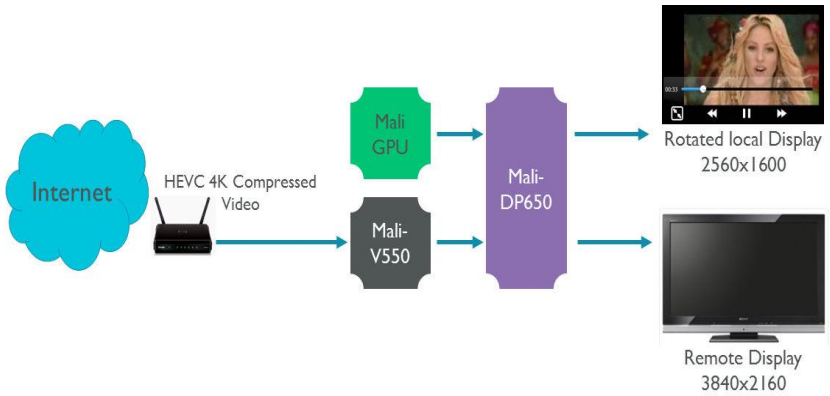
• AFBC formats:
  • 16 blocks of 4x4
	• AFBC formats:
	  • 20 blocks of 4x4 (planar YUV 4:2:0).
	  • 24 blocks of 4x4 (planar YUV 4:2:2)

Mali-Display write-back capability

- Mali-Display Write-Back (WB) enables the delivery of content to a second display core, a video encoder or any other dedicated multimedia function
  - An example use case could be to enable streaming content to external displays via either HDMI, USB-C or through Wi-Fi
- The Mali-Display processor supports one WB layer. This can either be:
  - A composited layer
  - A single layer (after internal processing, e.g. rotation, AFBC decoding or scaling)

WB graphics formats	*WB video formats*

• 32-bit RGB formats:
  • ARGB 2-10-10-10, ABGR 2-10-10-10, RGBA 10-10-10-2, BGRA 10-10-10-2
  • ARGB 8-8-8-8, ABGR 8-8-8-8, RGBA 8-8-8-8, BGRA 8-8-8-8
  • XRGB 8-8-8-8, XBGR 8-8-8-8, RGBX 8-8-8-8, BGRX 8-8-8-8
• 24-bit RGB formats:
  • RGB 8-8-8, BGR 8-8-8
	• 8-bit per sample YUV
	  • YUV 420-P2-8



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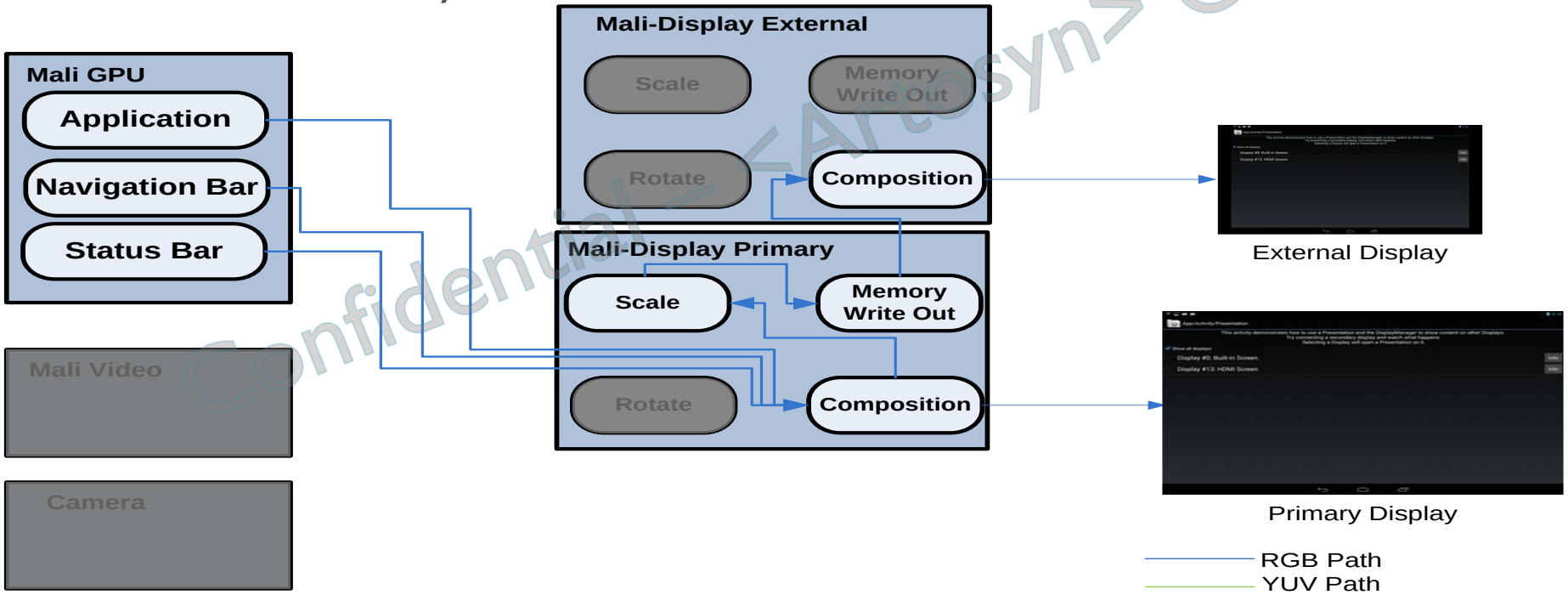
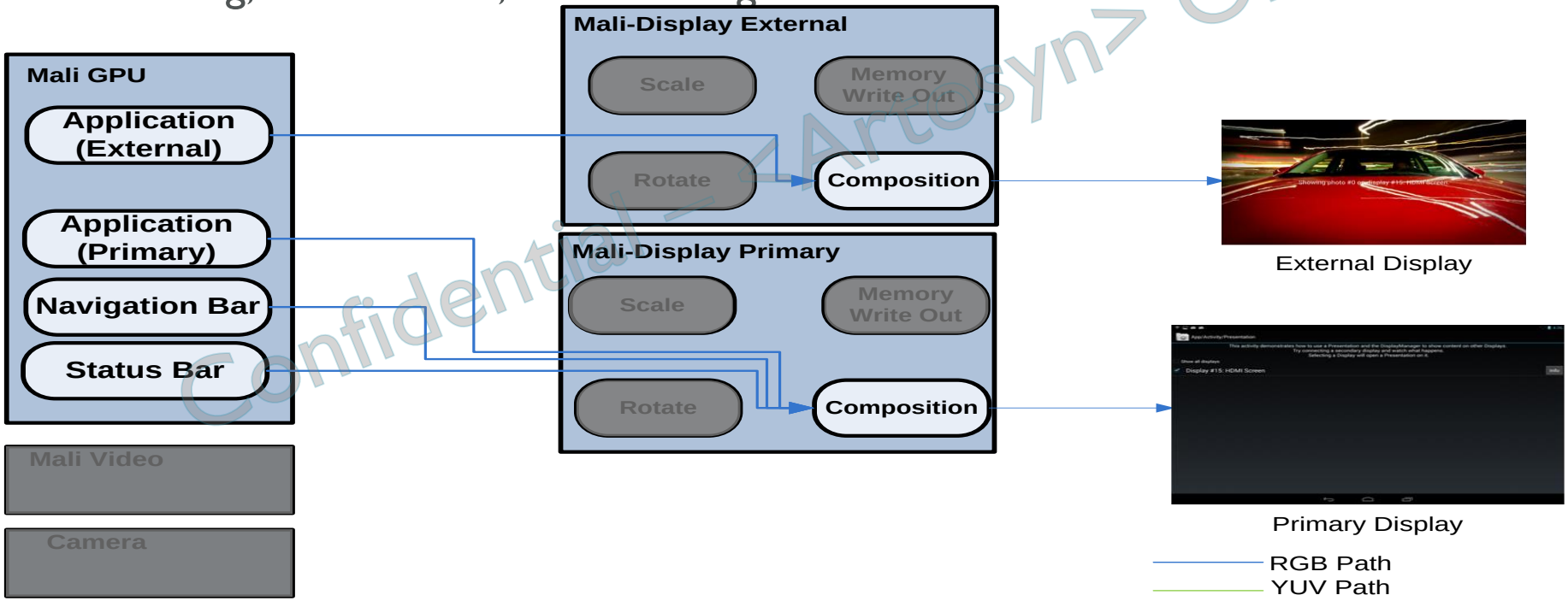
Dual Mali-Display Example: External Display (Clone mode)

- Clone – Same content displayed on both outputs
- Second screen usually scaled



Dual Mali-Display Example: External Display (Presentation)

- Presentation – Different content displayed on each output
- No scaling, No Rotation, No flattening



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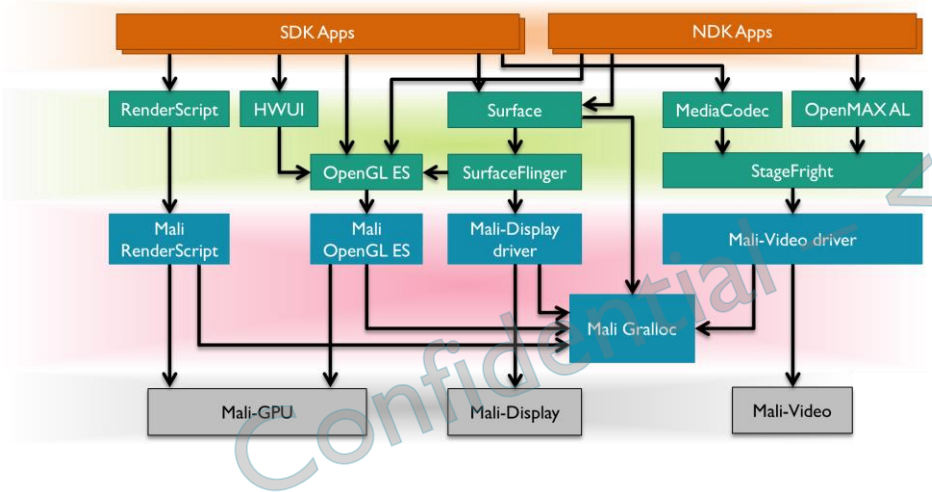
Mali drivers optimized to work together out of the box



- Maximize efficiency
- Faster time to market
- Minimum support issues

Zero copy sharing support

- dma_buf allows buffers allocated by ION to be shared between drivers
- Essential for efficient GPU/Video/Display

System Fence support (a.k.a. Android sync_pt)

- Represent a future event occurring
  - E.g. A GPU job completing
- Requires drivers to be synchronised
  - E.g. Display's "Compose" depends on GPU's "Render"
  - Reduces latency & improves user experience

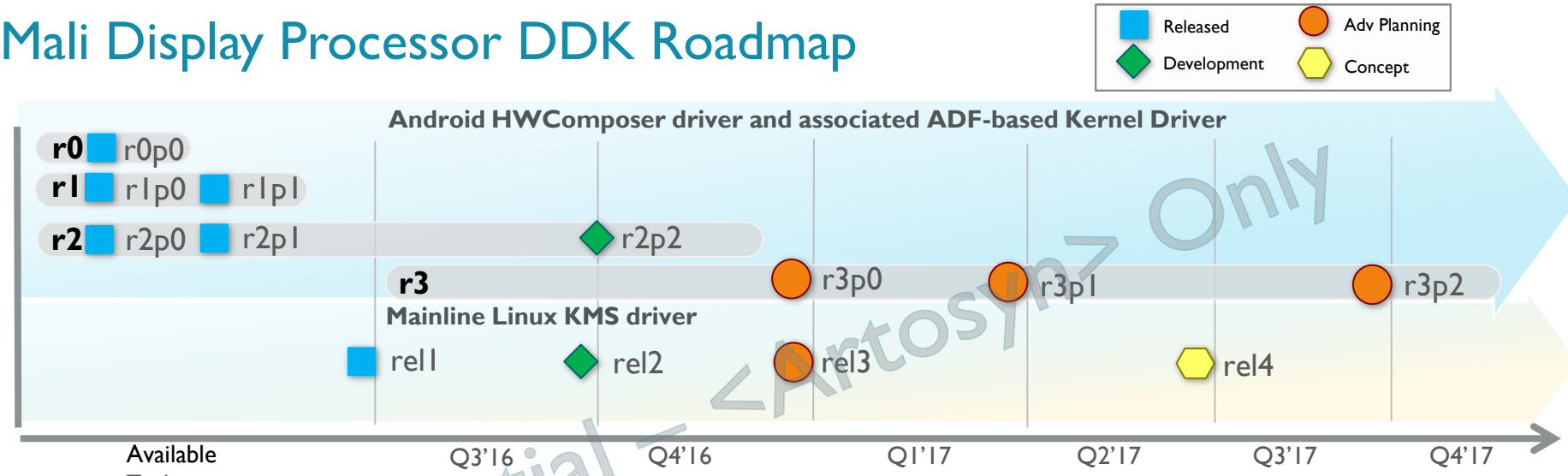
ARM reference Gralloc supported

- Allocates all buffer for graphics, display & video
  - Optimized for Mali GPU/Display/Video hardware (pixel format selection dependent on knowledge of HW)

Intelligent composition decisions

- Intelligent decisions on loading of Mali GPU and Display processors
- What to flatten on GPU and what to compose in Display
- Support for AFBC

Mali Display Processor DDK Roadmap



Roadmap subject to change

* Subject to external dependency

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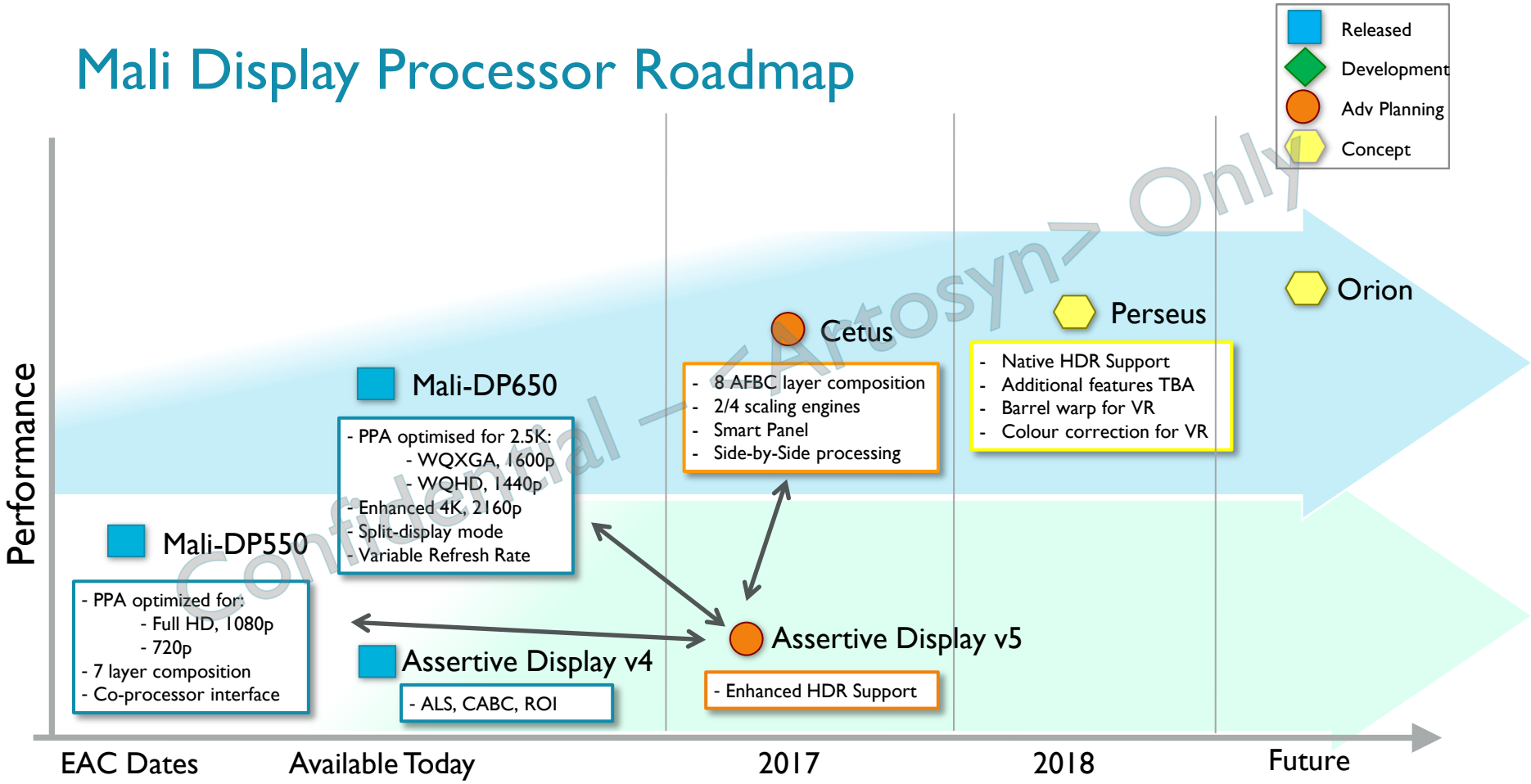
Mali Display Processor Roadmap



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Mali-Cetus Product Headline Features

- Support for 8 full frame AFBC layers on a single core with two display outputs
  - Capability of alpha blending of up to 4 video layers
  - Better use of display processor resources
- 2 or 4 high quality scaling engines for parallel window processing
  - Supports Android-N requirements for split-screen multi-window mode
- Smart Panel
  - Better support for display transmitter PHYs
  - Enhanced Command mode features such as self-refresh and partial update

Thank you

Mali-DP550 PPA results

Mali-DP550 r0p2 area – TSMC 28HPM, post place & route

Design configuration	Process	Std. cells area [mm²]	Memory area [mm²]	Design area [mm²]	Die area [mm²]	Overall RAM size [KB]
SD HD	SVT C38 0.9V	0.43	0.43	0.86	**0.98**	207
SD 2K	SVT C35 0.9V	0.45	0.57	1.02	**1.18**	306.5
SD 4K	SVT C31 0.9V	0.48	0.93	1.41	**1.60**	571.5
DD HD	SVT C38 0.9V	0.86	0.86	1.72	**1.97**	414
DD 2K	SVT C35 0.9V	0.96	1.14	2.10	**2.43**	613
DD 4K	SVT C31 0.9V	0.97	1.86	2.83	**3.16**	1143

Mali-DP550 r0p2 frequency targets – TSCM 28HPM, post place & route

Design configuration	Process	PCLK[1] [MHz]		ACLK[2] [MHz]		MCLK[3] [MHz]		PXLCLK[4] [MHz]	
		Target	Achieved	Target	Achieved	Target	Achieved	Target	Achieved
SD HD	SVT C38 0.9V	470	**470**	470	**470**	75	**75**	75	**75**
SD 2K	SVT C35 0.9V	600	**600**	600	**600**	150	**150**	150	**150**
SD 4K	SVT C31 0.9V	700	**700**	700	**695**	600	**600**	600	**600**
DD HD	SVT C38 0.9V	235	**235**	470	**470**	270	**270**	75	**75**
DD 2K	SVT C35 0.9V	700	**700**	700	**700**	600	**600**	600	**600**
DD 4K	SVT C31 0.9V	700	**657**	700	**700**	600	**600**	600	**600**

1) PCLK – APB slave and control registers clock
2) ACLK – Memory subsystem AXI clock, target derived based on worst case composition use case
3) MCLK – Main processing clock, target derived assuming no downscaling for SD configurations
4) PXLCLK – Pixel clock frequency target derived from VESA, CEA-861-F display timing

Mali-DP550 SD power analysis[1] results – TSMC 28HPM (tt, 0.9V, 85C)

Design config.	Operating point	Power vector	Leakage power [mW]	Dynamic power [mW]	Total power [mW]	Use case
SD HD	720p60	Minimum power	7.6	5.4	13.0	Only full-screen graphics layer active, AFBC disabled, XRGB 8888 format.
		Typical power	7.6	9.3	16.9	Graphics layer (full-screen) and smart layer (status bar + navigation bar) are active. Formats are ARGB 8888. Graphics layer is AFBC compressed.
		Maximum power	7.8	17.8	25.6	All layers are active. Video 1 in YUV 4:2:0 format is AFBC compressed and up-scaled. Video 2 is non-compressed and rotated. Smart layer consists of 2 rectangles. All processing functions enabled.
SD 2K	1080p60	Minimum power	12.1	9.3	21.4	Only full-screen graphics layer active, AFBC disabled, XRGB 8888 format.
		Typical power	12.2	16.7	28.9	Graphics layer (full-screen) and smart layer (status bar + navigation bar) are active. Formats are ARGB 8888. Graphics layer is AFBC compressed.
		Maximum power	12.4	35.3	47.7	All layers are active. Video 1 in YUV 4:2:0 format is AFBC compressed and up-scaled. Video 2 is non-compressed and rotated. Smart layer consists of 2 rectangles. All processing functions enabled.
SD 4K	1600p60	Minimum power	26.7	16.0	42.7	Only full-screen graphics layer active, AFBC disabled, XRGB 8888 format.
		Typical power	26.9	29.1	56.0	Graphics layer (full-screen) and smart layer (status bar + navigation bar) are active. Formats are ARGB 8888. Graphics layer is AFBC compressed.
		Maximum power	27.6	66.0	93.6	All layers are active. Video 1 in YUV 4:2:0 format is AFBC compressed and up-scaled. Video 2 is non-compressed and rotated. Smart layer consists of 2 rectangles. All processing functions are enabled.
SD 4K	2160p60	Minimum power	27.8	25.3	53.1	Only full-screen graphics layer active, AFBC disabled, XRGB 8888 format.
		Typical power	28.0	47.3	75.3	Graphics layer (full-screen) and smart layer (status bar + navigation bar) are active. Formats are ARGB 8888. Graphics layer is AFBC compressed.
		Maximum power	28.4	136.8	165.2	Video 1 layer (full-screen) and graphics layer (full-screen) are active. Formats are ARGB 8888 for video 1 and RGB 888 for graphics. Both layers are AFBC compressed.

1) Gate-level power analysis with switching activity taken from post place & route netlist simulation

Mali-DP550 vs. Mali-DP500 – main differences

Feature	Mali-DP500	Mali-DP550
Supported configurations	SD 2K – single display, maximum resolution 2048 x 2048 SD 4K – single display, maximum resolution 4096 x 4096	SD HD – single display, maximum resolution 1280 x 1280 SD 2K – single display, maximum resolution 2048 x 2048 SD 4K – single display, maximum resolution 4096 x 4096 DD HD – single display, maximum resolution 1280 x 1280 DD 2K – single display, maximum resolution 2048 x 2048 DD 4K – single display, maximum resolution 4096 x 4096
Number of display layers	3 – Video 1, Graphics 1, Graphics 2	4 (7) – Video 1, Video 2, Graphics, Smart Layer (up to 4 rectangles)
AXI interface	64-bit data bus, 40-bit address bus, 10-bit AXI ID	64-bit data bus, 40-bit address bus, 11-bit AXI ID
AXI parameters	Read and write OT: 1 – 32 (SW programmable) Burst length: 1, 2, 4, 8, 16, 32, 64, 128, 256-beat (SW programmable) Constant ID tags assigned for the layers – in order requirement for transactions corresponding to the same layer	Read OT: 1 – 32 (SW programmable) Burst length: 8, 16, 32, 64-beat (SW programmable) Each transaction has unique ID – full out of order support on the AXI read channel
Latency hiding buffers	No Reorder Buffer Input FIFO: 16 KB in 2K configuration, 32 KB in 4K config. – shared Output FIFO: 4 KB for plane 1 and 4KB for plane 2	Reorder Buffer: 16 KB (shared between read display layers) Input FIFO: 2.5 KB in HD config, 4 KB in 2K config, 8 KB in 4K config – per layer Output FIFO: 4 KB for plane 1, 2 KB for plane 2, 1 KB for CRC
CRC signatures	Not supported	Supported – 64-bit CRC calculated for 16x16 layer tiles
AFBC decoder and rotation	Supported layers: Video 1, Video 2 and Graphics Number of full-resolution AFBC / rotated layers per frame: 1 AFBC Output RAM: 64 KB in 2K config, 128 KB in 4K config	Supported layers: Video 1, Video 2 and Graphics Number of full-resolution AFBC / rotated layers per frame: 2 AFBC Output RAM: 80 KB in HD config,128 KB in 2K config, 256 KB in 4K config
Coprocessor interface	Not supported	Supported – parallel RGB interface exposed at the top-level. Enables 3rd party display processing IPs such as tone mapping
Power gating	Not supported	Supported – up to 2 power domains in a dual display configurations
External clock gating	Not supported	Support – ACLK0 and ACLK1 domains can be clock gated externally

Mali-DP650 PPA results

Mali-DP650 r0p1 area – TSMC 16FF+, post place & route

Design configuration	Std. cells area [mm²]			Memory area [mm²]			Design area [mm²]			Die area [mm²]			Overall RAM size [KB]
	LVT[1]	LVT UD[2]	SVT[3]	LVT	LVT UD	SVT	LVT	LVT UD	SVT	LVT	LVT UD	SVT	
SD QHD	0.25	0.26	-	0.48		-	0.73	0.74	-	**0.91**		-	410.83
SD 4K	0.25	0.26	0.27	0.68			0.93	0.94	0.95	**1.10**	**1.11**	**1.12**	639.25
DD QHD[4]	0.50	0.51	-	0.93		-	1.43	1.44	-	**1.70**		-	807.6
DD 4K	0.50	0.51	-	1.33		-	1.83	1.84	-	**2.20**		-	1256

1) Library: TSMC 16FF+ LVT C16, 7.5-track, 9 metal layers, 0.8 V
2) Library: TSCM 16FF+ LVT C16, 7.5-track, 9 metal layers, 0.7 V (underdrive)
3) Library: TSMC 16FF+ SVT C16, 7.5-track, 9 metal layers, 0.8 V
4) DD QHD area results are scaled from SD QHD

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Mali-DP550 r0p2 and Mali-DP650 r0p2 area comparison – SD 4K

TSMC 28HPM SVT C31 0.9V					
Design	**Std. cells area [mm²]**	**Memory area [mm²]**	**Design area [mm²]**	**Die area [mm²]**	**Overall RAM size [KB]**
Mali-DP550	0.48	0.93	1.41	**1.60**	571.5
Mali-DP650	0.61	1.04	1.65	**1.90**	639.25

TSCM 16FF+								
Design configuration	**Std. cells area [mm²]**		**Memory area [mm²]**		**Design area [mm²]**		**Die area [mm²]**		**Overall RAM size [KB]**
	LVT[1)]	**LVT UD[2)]**	**LVT**	**LVT UD**	**LVT**	**LVT UD**	**LVT**	**LVT UD**	
Mali-DP550	0.21	0.22	0.60	0.60	0.81	0.82	0.94	**0.95**	571.5
Mali-DP650	0.25	0.26	0.68	0.68	0.93	0.94	1.10	**1.11**	639.25

1) Library: TSMC 16FF+ LVT C16, 7.5-track, 9 metal layers, 0.8 V
2) Library: TSMC 16FF+ LVT C16, 7.5-track, 9 metal layers, 0.7 V (underdrive)

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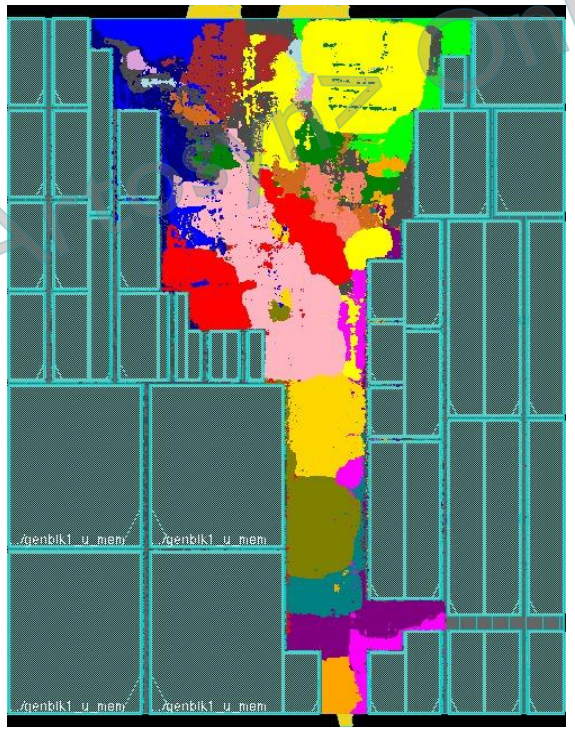
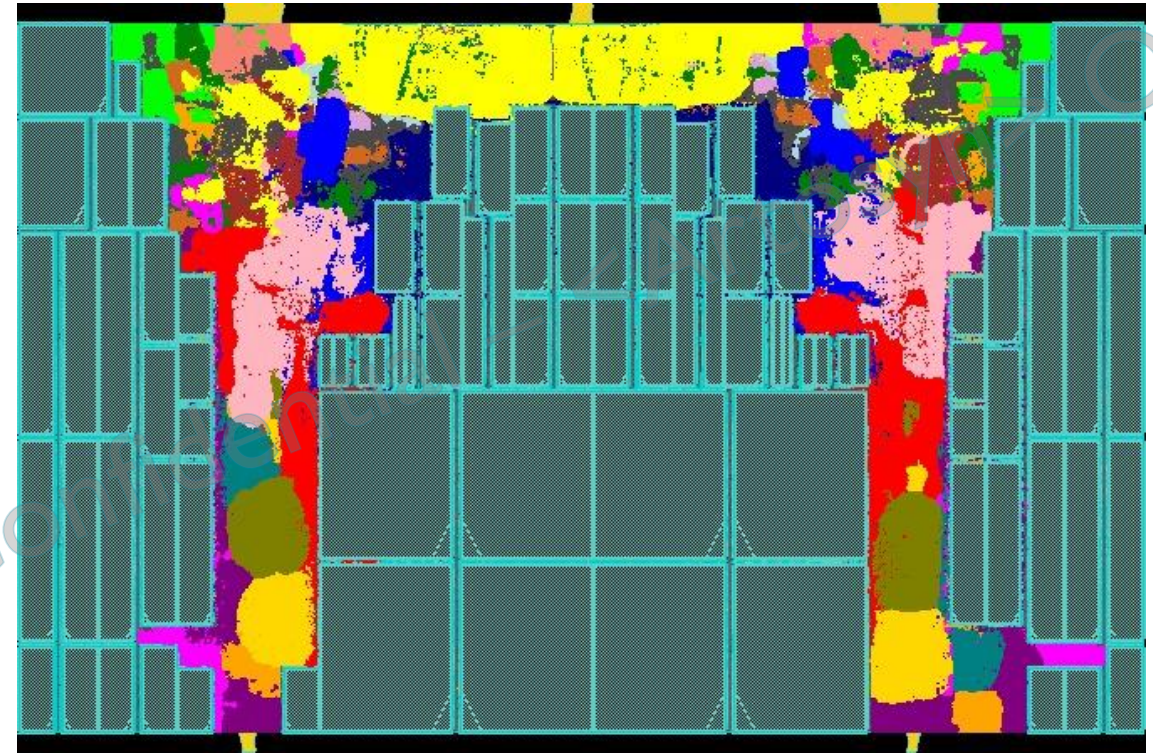
Mali-DP650 SD QHD and SD 4K floorplan images

SD QHD

SD 4K



Mali-DP650 DD 4K floorplan image



Mali-DP650 r0p2 frequency targets – TSMC 16FF+, post place & route

Design configuration	Process	PCLK[1] [MHz]		ACLK[2] [MHz]		MCLK[3] [MHz]		PXLCLK[4] [MHz]	
		Target	Achieved	Target	Achieved	Target	Achieved	Target	Achieved
SD QHD	LVT C16 UD	500	**500**	500	**500**	635	**635**	300	**300**
SD 4K	LVT C16 UD	650	**650**	650	**650**	635	**635**	600	**600**
DD 4K	LVT C16	650	**650**	650	**650**	635	**635**	600	**600**

1) PCLK frequency target is set the same as ACLK target, but in general these two clocks are asynchronous and PCLK can be slower
2) ACLK frequency target is set based on the most demanding composition use case at given resolution
3) MCLK frequency target is set assuming maximum downscaling factor of 2.5x for 1600p60 resolution
4) PXLCLK clock frequency target is derived from VESA, CEA-861-F display timing

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Latency tolerance – landscape scan, SD 4K configuration

Operating point [1]	Use cases [2]	ACLK clock requirement [MHz] [3]		Average latency tolerance [us]	
		Mali-DP550	Mali-DP650	Mali-DP550	Mali-DP650
1080p60 landscape scan	Two AFBC RGB 32bpp layers	500	350	2 us	8 us
	Two AFBC RGB 32bpp layers and one non-AFBC 8-bit YUV 4:2:0 layer	500	350	2 us	6.5 us
	Two AFBC RGB 32bpp layers and one non-AFBC 10-bit YUV 4:2:0 layer (P010)	500	350	2 us	5.5 us
	Three AFBC RGB 32bpp layers	500	350	1 us	4 us
1600p60 landscape scan	Two AFBC RGB 32bpp layers	650	500	1 us	4 us
	Two AFBC RGB 32bpp layers and one non-AFBC 8-bit YUV 4:2:0 layer	650	500	1 us	3.3 us
	Two AFBC RGB 32bpp layers and one non-AFBC 10-bit YUV 4:2:0 layer (P010)	650	500	1 us	2.7 us
	Two AFBC RGB 32bpp layers and one non-AFBC RGB 32bpp layer	650	500	1 us	2.5 us
2160p60 landscape scan	Two AFBC RGB 32bpp layers	Not supported	650	Not supported	2 us
	Two AFBC RGB 32bpp layers and one non-AFBC 8-bit YUV 4:2:0 layer	Not supported	650	Not supported	1.63 us
	Two AFBC RGB 32bpp layers and one non-AFBC 10-bit YUV 4:2:0 layer (P010)	Not supported	650	Not supported	1.33 us
	Two AFBC RGB 32bpp layers and one non-AFBC RGB 32bpp layer	Not supported	650	Not supported	1.25 us

1) Pixel clock frequency assumed: 1080p60 – 138.5 MHz, 1600p60 – 268.5 MHz, 2160p60 – 533.25 MHz
2) No downscaling and no rotation by 90/270 deg. in the composition use cases
3) Latency tolerance derived assuming: burst length = 16-beat, maximum OT = 32
4) AFBC compression ratio assumed = 50%

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Latency tolerance – portrait scan, SD 4K configuration

Operating point [1]	Use cases [2]	ACLK clock requirement [MHz] [3]		Average latency tolerance [us]	
		Mali-DP550	Mali-DP650	Mali-DP550	Mali-DP650
1080p60 portrait scan	Two AFBC RGB 32bpp layers	500	**350**	2 us	**8 us**
	Two AFBC RGB 32bpp layers and one non-AFBC 8-bit YUV 4:2:0 layer	500	**350**	2 us	**6.5 us**
	Two AFBC RGB 32bpp layers and one non-AFBC 10-bit YUV 4:2:0 layer (P010)	500	**350**	2 us	**5.5 us**
	Three AFBC RGB 32bpp layers	500	**350**	1 us	**4 us**
1440p60 portrait scan	Two AFBC RGB 32bpp layers	650	**500**	1.13 us	**4.5 us**
	Two AFBC RGB 32bpp layers and one non-AFBC 8-bit YUV 4:2:0 layer	650	**500**	1.13 us	**3.6 us**
	Two AFBC RGB 32bpp layers and one non-AFBC 10-bit YUV 4:2:0 layer (P010)	650	**500**	1.13 us	**3 us**
	Two AFBC RGB 32bpp layers and one non-AFBC RGB 32bpp layer	650	**500**	1.13 us	**2.8 us**
2160p60 portrait scan	Two AFBC RGB 32bpp layers	Not supported	**650**	Not supported	**2 us**
	Two AFBC RGB 32bpp layers and one non-AFBC 8-bit YUV 4:2:0 layer	Not supported	**650**	Not supported	**1.63 us**
	Two AFBC RGB 32bpp layers and one non-AFBC 10-bit YUV 4:2:0 layer (P010)	Not supported	**650**	Not supported	**1.33 us**
	Two AFBC RGB 32bpp layers and one non-AFBC RGB 32bpp layer	Not supported	**650**	Not supported	**1.25 us**

1) Pixel clock frequency assumed: 1080p60 – 137.5 MHz, 1440p60 – 252.75 MHz, 2160p60 – 549.5 MHz
2) No downscaling and no rotation by 90/270 deg. in the composition use cases
3) Latency tolerance derived assuming: burst length = 16-beat, maximum OT = 32
4) AFBC compression ratio assumed = 50%

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Latency tolerance and ACLK clock – important assumptions

- ACLK clock frequency for presented operating points is derived from the worst theoretical composition use cases, which are as follows:
  - 1080p60: Composition (alpha-blending) of four full-screen RGB 32bpp layers – ACLK = 350 MHz
  - 1440p60: Composition (alpha-blending) of four full-screen RGB 32bpp layers – ACLK = 500 MHz
  - 1600p60: Composition (alpha-blending) of four full-screen RGB 32bpp layers – ACLK = 500 MHz
  - 2160p60: Composition (alpha-blending) of three full-screen RGB 32bpp layers – ACLK = 600 MHz
- In practice, in Android window composition use cases we can see maximum 3 alpha-blended layers
  - e.g. Homescreen with StatusBar dragged down by a user
- As the result in a real system the ACLK frequency for DPU can be lower than the frequencies mentioned above. Assuming maximum three RGB 32bpp layers we could achieve as follows:
  - 1080p60: ACLK = 250 MHz
  - 1440p60: ACLK = 350 MHz
  - 1660p60: ACLK = 350 MHz
  - 2160p60: ACLK = 600 MHz (unchanged)
- In our performance validation flow we use worst case clocks for the use cases, and also we synthesise for the worst case clock

Mali-DP650 r0p1 vs. Mali-DP550 r0p2 – power at 16FF+ SVT C16, 0.8V [1)]

Power vector	Design configuration		Leakage power [mW]		Dynamic power [mW]		Total power [mW]		Power density [mW / mm²]	
	Mali-DP550	Mali-DP650	Mali-DP550	Mali-DP650 [2)]	Mali-DP550	Mali-DP650 [2)]	Mali-DP550	Mali-DP650	Mali-DP550	Mali-DP650
1080p60_min	SD 2K	SD QHD	1.6	2.5	7.1	5.6	**8.7**	**8.1**	12.4	9.0
1080p60_typ			1.6	2.5	12.3	11.3	**13.9**	**13.8**	19.9	15.3
1080p60_max1			1.6	2.5	28.0	25.7	**29.6**	**28.2**	42.3	31.3
1080p60_max2			-	2.5	-	22.7	**-**	**25.2**	-	28.0
1600p60_min	SD 4K	SD QHD	2.4	2.5	11.3	10.0	**13.7**	**12.5**	14.4	13.9
1600p60_typ			2.4	2.5	21.7	19.2	**24.1**	**21.7**	25.4	24.1
1600p60_max1			2.4	2.5	68.1	46.6	**70.6**	**49.1**	74.3	54.6
1600p60_max2			-	2.5	-	40.7	**-**	**43.2**	-	48.0
2160p60_min	SD 4K	SD 4K	2.4	2.8	17.1	18.8	**19.5**	**21.6**	20.5	19.6
2160p60_typ			2.4	2.8	33.3	34.2	**35.7**	**36.9**	39.7	33.5
2160p60_max1			2.4	2.8	128.3	62.2	**130.7**	**65.0**	137.6	59.1
2160p60_max2			-	2.8	-	77.5	**-**	**80.3**	-	73.0

1) PVT corner = (tt, 0.8 V, 85 C), gate-level power analysis with switching activity taken from post place & route netlist simulation

2) Mali-DP650 leakage and dynamic power numbers for 1080p and 1600p power vectors are scaled from LVT C16 results

Mali-DP650 r0p1 vs. Mali-DP550 r0p2 – power at 16FF+ LVT UD, 0.7 V [1)]

Power vector	Design configuration		Leakage power [mW]		Dynamic power [mW]		Total power [mW]		Power density [mW / mm²]	
	Mali-DP550	Mali-DP650	Mali-DP550	Mali-DP650	Mali-DP550	Mali-DP650	Mali-DP550	Mali-DP650	Mali-DP550	Mali-DP650
1080p60_min	SD 2K	SD QHD	4.2	5.6	4.5	4.0	**8.7**	**9.6**	13.0	10.7
1080p60_typ			4.2	5.6	8.5	8.0	**12.7**	**13.6**	19.0	15.1
1080p60_max1			4.2	5.6	20.4	18.8	**24.6**	**24.4**	36.7	27.1
1080p60_max2			-	5.6	-	16.6	-	**22.2**	-	24.7
1600p60_min	SD 4K	SD QHD	5.1	5.6	7.6	7.1	**12.7**	**12.7**	13.5	14.1
1600p60_typ			5.1	5.6	14.7	15.0	**19.8**	**19.0**	21.1	21.1
1600p60_max1			5.2	5.6	47.7	35.3	**52.9**	**39.5**	56.3	43.9
1600p60_max2			-	5.6	-	29.5	-	**35.1**	-	39.0
2160p60_min	SD 4K	SD 4K	5.11	6.3	12.6	14.3	**17.7**	**20.5**	18.8	18.6
2160p60_typ			5.13	6.3	23.7	26.0	**28.8**	**32.3**	30.6	29.4
2160p60_max1			5.17	6.3	97.1	47.1	**102.3**	**53.4**	108.8	48.5
2160p60_max2			-	6.3	-	58.9	-	**65.2**	-	59.3

1) PVT corner = (tt, 0.7 V, 85 C), gate-level power analysis with switching activity taken from post place & route netlist simulation

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Mali-DP650 r0p1 – power at 16FF+ SVT, LVT and LVT UD C16 [1)]

Power vector	Leakage power [mW]			Dynamic power [mW]			Total power [mW]		
	SVT[2)]	LVT[3)]	LVT UD[4)]	SVT	LVT	LVT UD	SVT	LVT	LVT UD
1080p60_min	2.50	6.28	5.55	5.57	5.07	4.03	8.07	11.4	**9.58**
1080p60_typ1	2.50	6.31	5.58	11.27	10.27	8.01	13.77	16.6	**13.60**
1080p60_typ2	2.50	6.31	5.58	12.49	11.49	8.95	14.99	17.8	**14.50**
1080p60_max1	2.50	6.37	5.63	25.69	24.19	18.77	28.19	30.6	**24.40**
1080p60_max2	2.50	6.32	5.58	22.72	21.22	16.61	25.22	27.5	**22.20**
1600p60_min	2.50	6.28	5.55	10.00	9.00	7.17	12.50	15.3	**12.70**
1600p60_typ1	2.50	6.31	5.58	19.2	17.2	13.40	21.70	23.5	**19.00**
1600p60_typ2	2.50	6.31	5.58	21.72	19.72	15.37	24.22	26.0	**20.90**
1600p60_max1	2.50	6.36	5.63	46.6	43.6	33.88	49.10	50.0	**39.50**
1600p60_max2	2.50	6.32	5.59	40.7	37.7	29.50	43.20	44.0	**35.10**
2160p60_min	2.76	6.90	6.28	18.78	17.9	14.3	21.6	24.9	**20.5**
2160p60_typ1	2.77	6.93	6.31	34.2	32.5	26.0	36.9	39.4	**32.3**
2160p60_typ2	2.77	6.93	6.31	36.9	35.1	28.1	39.7	42.0	**34.4**
2160p60_max1	2.78	6.95	6.32	62.2	59.8	47.1	65.0	66.7	**53.4**
2160p60_max2	2.78	6.94	6.32	77.5	74.4	58.9	80.3	81.4	**65.2**

1) Gate-level power analysis with switching activity taken from post place & route netlist simulation
2) PVT = (tt, 0.8 V, 85 C). Leakage and dynamic power numbers for 1080p and 1600p vectors are scaled from LVT C16 results
3) PVT = (tt, 0.8 V, 85 C)
4) PVT = (tt, 0.7 V, 85 C)

Mali-DP650 vs. Mali-DP550 – main differences

Feature	Mali-DP550	Gemini
Maximum line size configurations	1280 – HD configuration 2048 – 2K configuration 4096 – 4K configuration	2560 – QHD configuration 4096 – 4K configuration
AXI interface	64-bit data bus, 40-bit address bus, 11-bit AXI ID	128-bit data bus, 40-bit address bus, 12-bit AXI ID
AXI parameters	Read and write OT: 1 – 32 (SW programmable) Read and write burst length: 8, 16, 32, 64-beat (SW programmable)	Read OT: 1 – 32 (SW programmable) Write OT: 1 – 16 (SW programmable) Read and write burst length: 4, 8, 16, 32-beat (SW programmable)
Latency hiding buffers	Reorder Buffer: 16 KB (shared between read display layers) Input FIFO: 4 KB in 2K configuration, 8 KB in 4K configuration (per layer) Output FIFO: 4 KB for plane 1, 2 KB for plane 2, 1 KB for CRC	Reorder Buffer: 16 KB (shared between read display layers) Input FIFO: 10 KB in QHD configuration, 16 KB in 4K configuration (per layer) Output FIFO: 4 KB for plane 1, 2 KB for plane 2, 1 KB for CRC
MMU TLB prefetcher	Not supported	Supported
QoS	AXI-protocol based and basic side-band QOS	AXI-protocol based QOS
Rotation / flip of uncompressed layers	Supported rotated / flipped layers: Video 1, Video 2, Graphics Rotation Buffers size: 7 KB Maximum burst length for rotated layer: 8-beat (64 bytes) 10-bit YUV formats: YUV_444_P1_10, YUV_420_P2_10 (P010)	Supported rotated / flipped layers: Video 1, Video 2 No rotation buffers Maximum burst length for rotated layer: 4-beat (64 bytes) 10-bit YUV formats: YUV_444_P1_10, YUV_420_P2_10 (P010), YUV_420_P1_10 (Y0L2)
AFBC decoder	Supported layers: Video 1, Video 2 and Graphics Output data word size: 64-bit Number of 4x4 decoder blocks: 1 (shared between the layers) Header Buffer size: 4 KB in 2K configuration, 8 KB in 4K configuration Payload Buffer size: 8 KB AFBC output RAM: 128 KB in 2K configuration, 256 KB in 4K configuration	Supported layers: Video 1, Video 2 and Graphics Output data word size: 128-bit Number of 4x4 decoder blocks: 2 (shared between the layers) Header Buffer size: 5 KB in QHD configuration, 8 KB in 4K configuration Payload Buffer size: 2x8KB AFBC output RAM: 160 KB in 2K configuration, 256 KB in 4K configuration
Display outputs	Primary display output interface: 1 channel (36-bit RGB) Secondary display output interface: 1 channel (36-bit RGB)	Primary display output interface: 2 channels(30-bit RGB, support for 1:2 display line split) Secondary display output interface: 1 channel (30-bit RGB)
Variable refresh rate	Not supported	Supported through variable VFP (Vertical Front Porch)
Deinterlacing methods	Simple line replication (line doubling) 2x vertical scaling with programmable initial phase	2x vertical scaling with programmable initial phase