28nm Chip Implementation Guidelines

Agenda

- Specific Design Guidelines
  - Layout Effect
  - Design For Manufacturing
  - Process/Noise Aware CTS
- Physical Implementation Recommendation
  - Physical Sign-Off Recommendation
  - STA Sign-Off Recommendation
  - Power Sign-Off Recommendation
  - Signal Integrity
- N28 Integrated Sign-Off Flow

Technology Scaling Trend: Layout Dependent Effects (LDEs) Become Prominent

Layout Dependent Effects		Prior to 40nm	40nm	28nm and beyond
WPE	Well Proximity Effect			
PSE	Poly Spacing Effect			
LOD	Length of Diffusion			
OSE	OD to OD Spacing Effect			
OD/PO Density	OD/Poly Density			

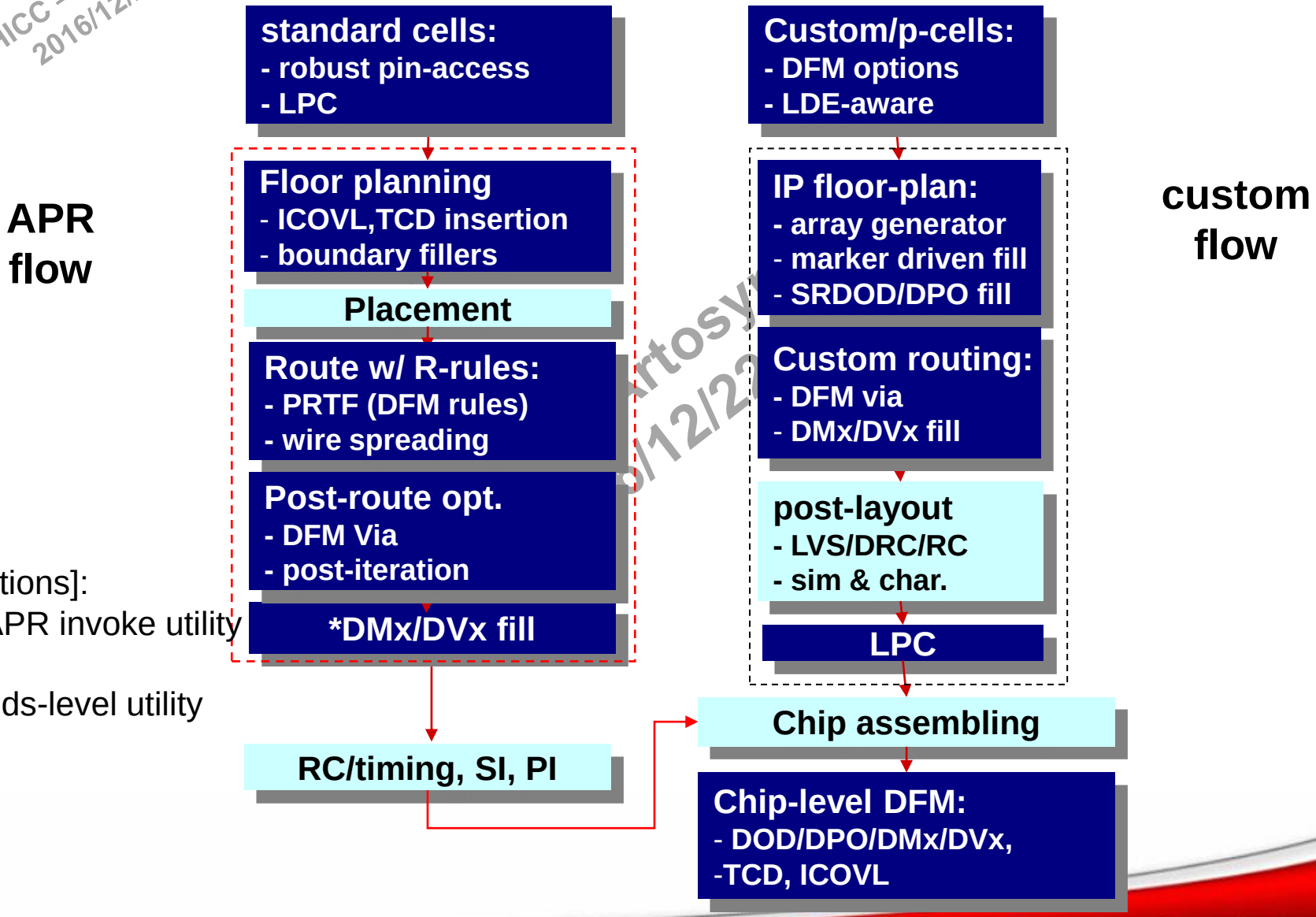
Layout Dependent Effects (LDE)

- **WPE (Well Proximity Effect)**
  - **V_t of MOS device is raised and the I_d is degraded when well edge and gate spacing gets smaller**
  - **Might cause timing inconsistency between timing library and silicon measurement for boundary cells**
- **OSE / PSE (OD / Poly Space Effect)**
  - **Reduce MOS characteristics differences between pre-simulation and post-simulation**
  - **No empty area in place-able area, FILLER cell is must**
  - **Add FILLER cell on both sides of the block**
  - **Insert Dummy OD**

N28 DFM Implementation Updates

- **Objectives**
  - Provide executable DFM solution to a) minimize yield excursion, b) CDU improvement for DRM v1.2
- **Major DFM enhancement items**
  - BEOL DFM prevention in APR techfile (updated)
  - BEOL DFM optimization in APR post-route (updated)
  - ICOVL and TCD insertion
  - FEOL and BEOL Dummy Fill
- **Support**
  - Regional FTS
  - Download "*N28 DFM Rollout Package* (T-N28-CL-RP-022)"

DFM Implementations @ Design Stages

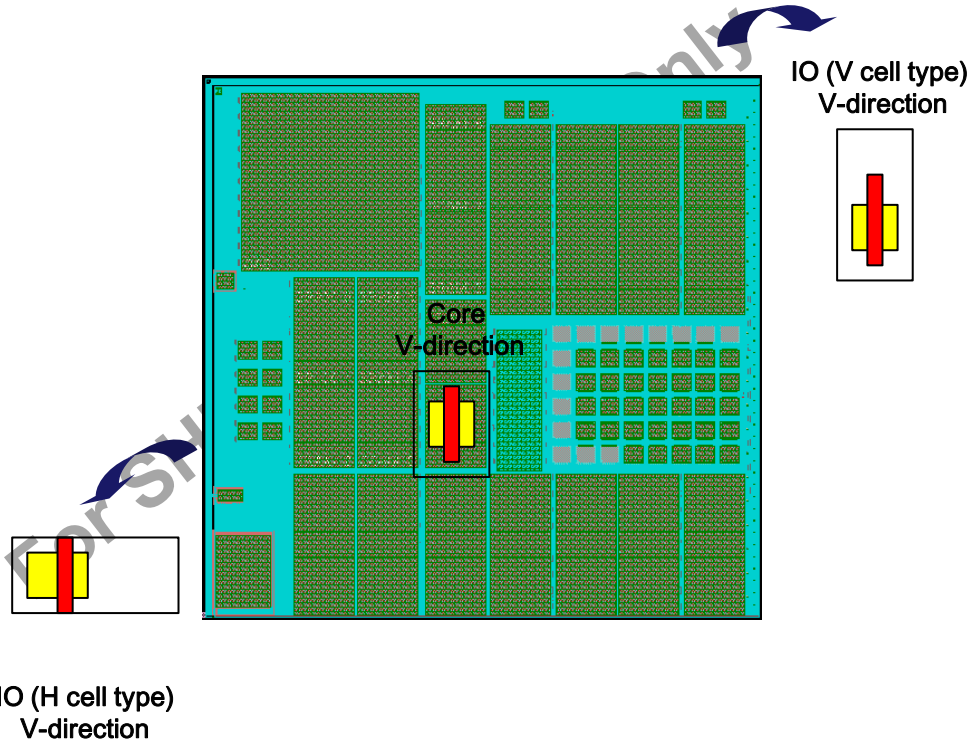


Physical Implementation Recommendation

- Physical Sign-Off recommendation
  - Floorplan guidelines
  - Placement and CTS guidelines
  - Dummy TCD/ICOVL insertion
  - DFM VIA insertion
- STA Sign-Off recommendation
  - Sign-Off corners
  - OCV, uncertainty and SBOCV
- Power Sign-Off recommendation
  - Sign-Off corner
  - PEM/SEM concern
- Signal Integrity

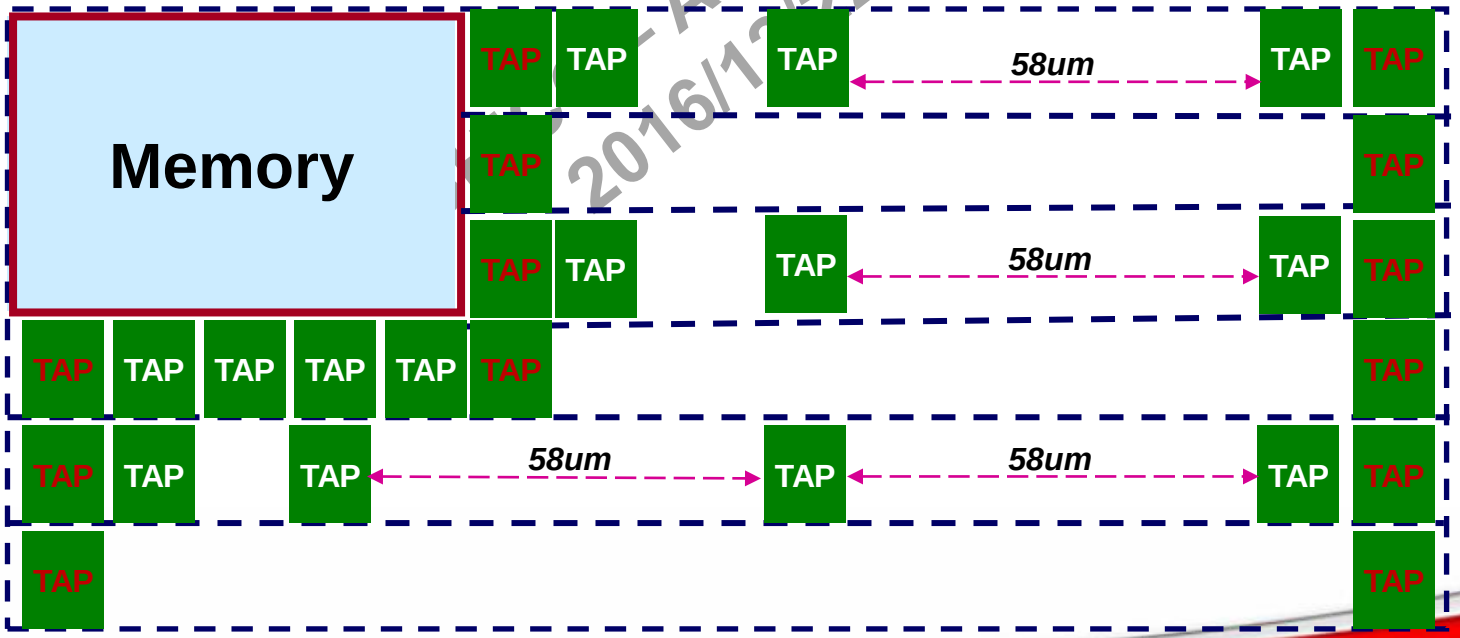
Physical Sign-Off Recommendation [Floorplan Guidelines]

- Poly uni-direction hard rule for all device
  - STD
  - SRAM
  - IO
  - TCD
  - ICOVL
  - IP



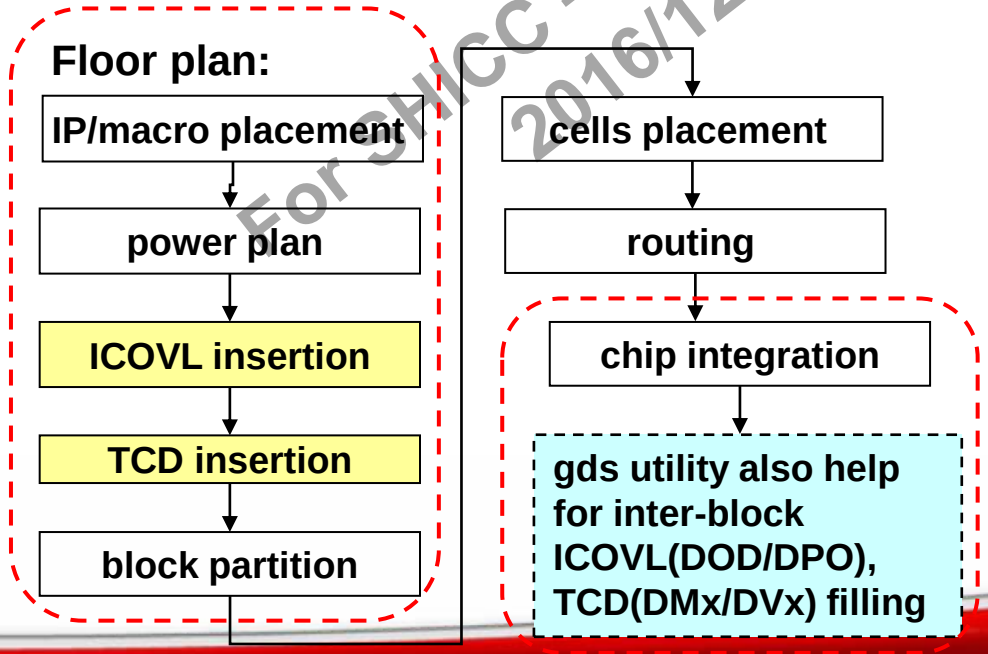
Physical Sign-Off Recommendation [Placement Guidelines]

- Same as N40, FILLER1 gap and FILLER1 are forbidden for OSE variation concern
- FILL1 cell has already been taken out from the standard cell libraries
- Row-End boundary cell
  - Use BOUNDARY_LEFT, BOUNDARY_RIGHT or at least TAPCELL



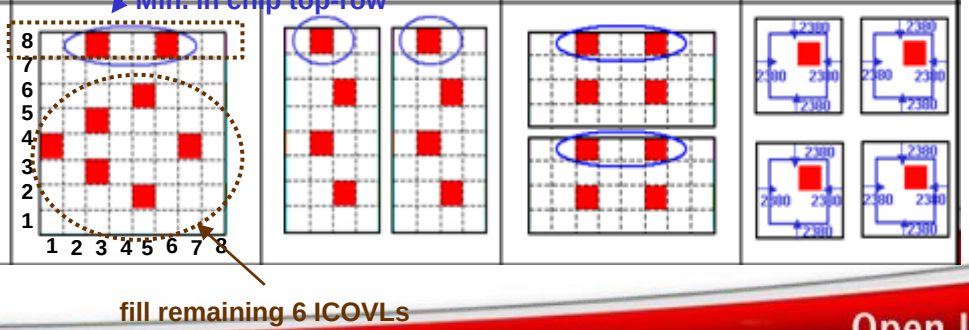
Dummy Pattern Insertion Flow

- **Two dummy patterns need to be inserted at floorplan stage**
  - ICOVL(In-chip Overlay)
  - Dummy TCD (Test-key for Critical Dimension)
- **Insertion guideline**
  - TCD: each TCD cell in a 2x2mm^2 tile; >50% inserted rate
  - ICOVL: 4~8 cells per die size & mask reticle (big design)
  - Consider dummy insertion in a hierarchical chip globally before block partitioning
  - Planning ICOVL sites before TCD cells
  - Align M1/M2 TCD with FEOL TCD cells to reduce area overhead



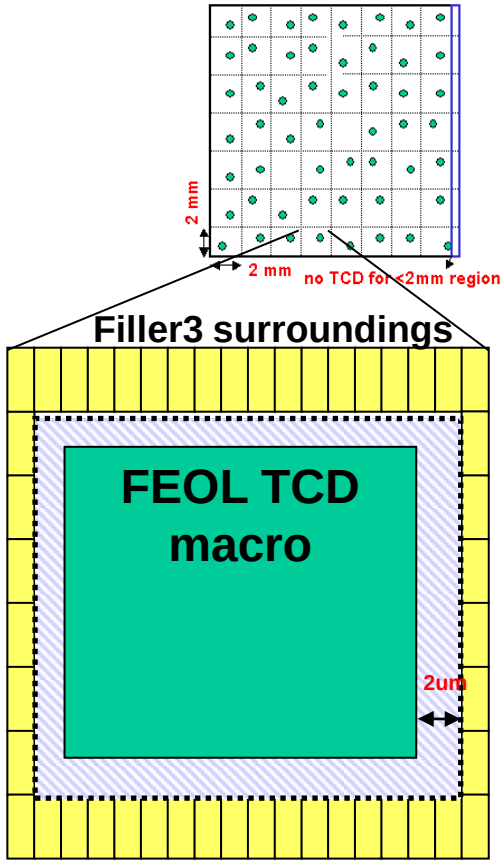
ICOVL Insertion

- **Benefit : Serves for better mask alignment**
- **Need to reserve space inside block for hierarchical designs**
- **Need to reserve enough ICOVL in top-raw (as blue circle), for U-fram litho.**
- **Implementation guideline**
  - **Insertion priority : ICOVL (combo> single) > TCD**
  - **Use Gross-Die Advisor (GDA) to estimate the mask reticle planning**
    - ***tsmc-online/DesignPortal2.0/TechnologySelection/GDA***

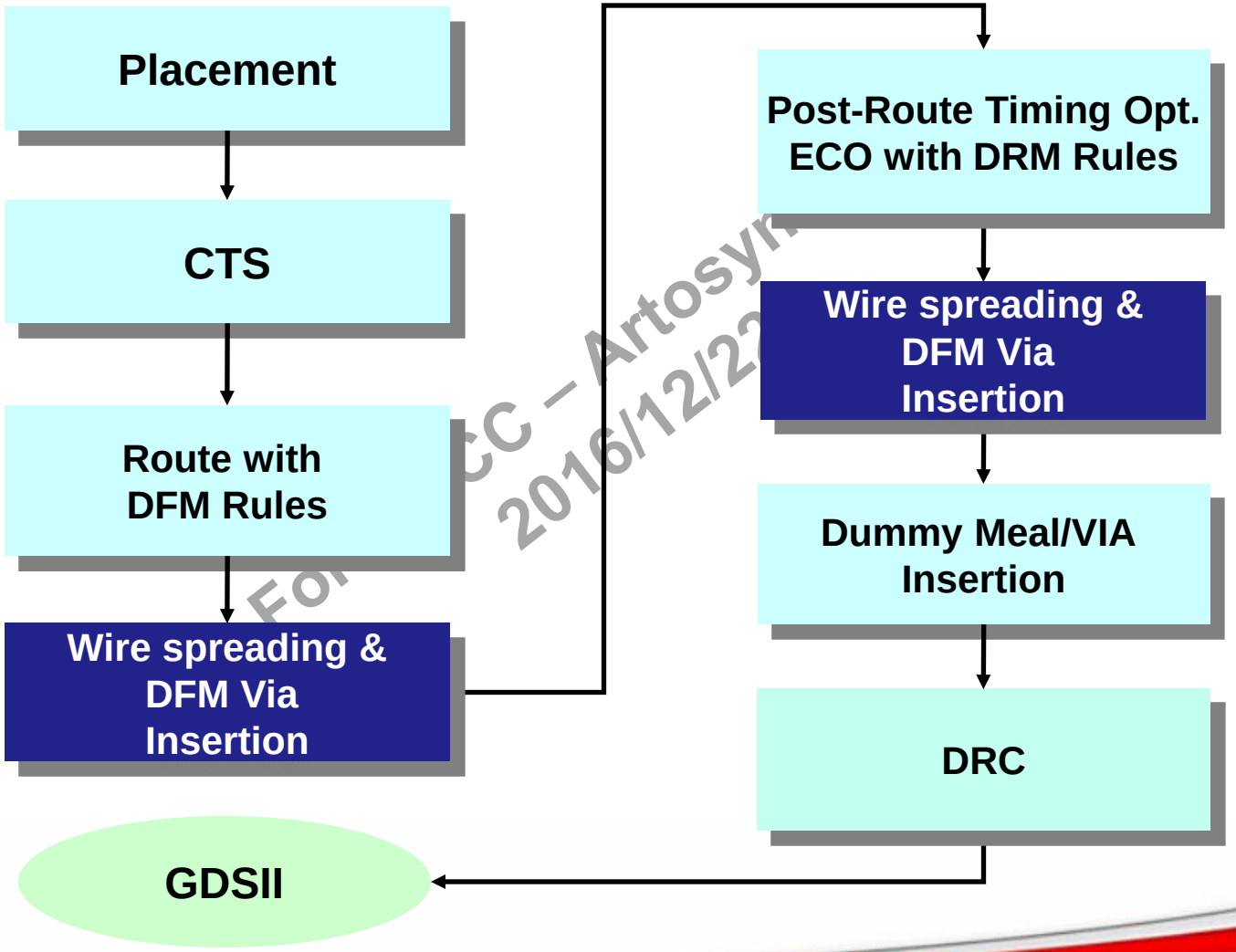
Die size & reticle	1x1 reticle	2x1 reticle	1x2 reticle	2x2 reticle
Die-X (mm)	> 14.31	9.51 < X <=14.31	> 14.31	9.51 < X <=14.31
Die-Y (mm)	> 18.24	> 18.24	12.13 < Y <=18.24	12.13 < Y <=18.24
grid partition	8x8	4x8	8x4	-
required ICOVL counts / # in chip top-row	8 / 2	4 / 1	4 / 2	1® / 0
Examples for ICOVL insertion				

Dummy TCD Insertion

- **Benefit:**
  - FEOL dummy TCD: improve PO CDU (Critical Dimension Uniformity) by 30~40%
  - BEOL dummy TCD: metal mask CD control
- Inserting TCD dummy in chip design planning stage is recommended to meet design requirements like uniform distribution
- Post-route TCD dummy insertion is only supplemental for uniform distribution improvement

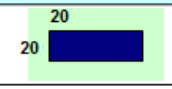
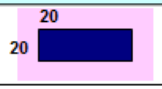
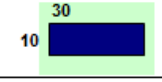
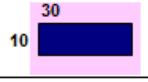
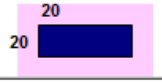
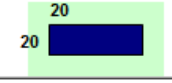
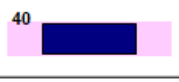
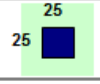
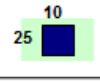
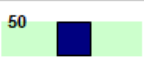


N28 DFM Routing Flow

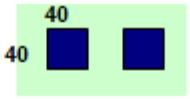
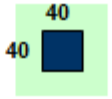
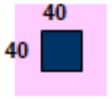
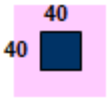
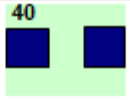
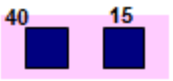
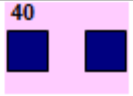
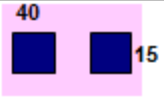


Wire Spreading and DFM Via Swapping

- Reduce systematic defects in early phase of the technology ramp
- Tech. file is by request and definitions could be changed

Sequence	Vx enclosure by Mx+1	Vx enclosure by Mx	Mx+1/Vx	Vx/Mx
1	20nm/20nm	20nm/20nm		
2	30nm/10nm	30nm/10nm		
3	0nm/40nm	20nm/20nm		
4	20nm/20nm	0nm/40nm		
5	0nm/40nm	0nm/40nm		
6	25nm/25nm	25nm/25nm		
7	0nm/30nm	10nm/25nm		
8	10nm/25nm	0nm/30nm		
9	0nm/50nm	0nm/50nm		

N28 DFM Via Definition – My/Vy

Sequence	Vy enclosure by My+1	Vy enclosure by My	My+1/Vy	Vy/My	Vy/Mx
1	40nm/40nm	40nm/40nm			
2	40nm/40nm	40nm/40nm			
3	40nm/0nm	0nm/40nm			
	0nm/40nm	40nm/0nm			
4	0nm/65nm	0nm/65nm			

DFM VIA Swapping Template in Cadence EDI

```
#--- Wire Spreading ---#
setNanoRouteMode –droutePostRouteSpreadWire true
detailRoute

#--- Define DFM Via Priority ---#
setNanoRouteMode –droutePostRouteSpreadWire false
setNanoRouteMode –dbViaWeight {*FBD* 8, *FBS* 7, *PBD* 6, *PBS* 5, *2cut_p1* 4,
*2cut_p2* 3, *2cut_p3* 2, *FAT* 1}
setNanoRouteMode –routeWithTimingDriven false
setNanoRouteMode –drouteUseMultiCutViaEffort high
setNanoRouteMode –drouteExpFixMar true
setNanoRouteMode –drouteExpAllowNonPreferApa true
setNanoRouteMode –droutePostRouteSwapVia true

detailRoute
```

DFM VIA Swapping Template in Synopsys ICC

```
#--- Wire Spreading ---#
spread_zrt_wires

#---DFM VIA Insertion ---#
define_zrt_redundant_vias \
 -from_via { VIA12_1cut VIA12_1cut VIA12_1cut VIA12_1cut VIA12_1cut VIA12_1cut VIA12_1cut VIA12_1cut     \
          VIA12_1cut_V VIA12_1cut_V VIA12_1cut_V VIA12_1cut_V VIA12_1cut_V VIA12_1cut_V VIA12_1cut_V  \
          VIA12_1cut_V VIA12_LONG_H VIA12_LONG_H VIA12_LONG_H VIA12_LONG_H VIA12_LONG_H \
          VIA12_LONG_V VIA12_LONG_V VIA12_LONG_V VIA12_LONG_V VIA12_LONG_V \
          VIA12_LONG_HH VIA12_LONG_HH VIA12_LONG_HH VIA12_LONG_HH VIA12_LONG_HH }\
 -to_via { VIA12_FBD VIA12_FBS VIA12_PBD VIA12_PBS VIA12_2cut_P1 VIA12_2cut_P2_BLC VIA12_2cut_P3  \
         VIA12_1cut_FAT_V  VIA12_FBD VIA12_FBS VIA12_PBD VIA12_PBS VIA12_2cut_P1 VIA12_2cut_P2_BLC  \
         VIA12_2cut_P3 VIA12_1cut_FAT_V  VIA12_FBD VIA12_PBD VIA12_2cut_P1 VIA12_2cut_P2_BLC VIA12_2cut_P3 \
         VIA12_FBD VIA12_PBD VIA12_2cut_P1 VIA12_2cut_P2_BLC VIA12_2cut_P3 \
         VIA12_FBD VIA12_PBD VIA12_2cut_P1 VIA12_2cut_P2_BLC VIA12_2cut_P3 }\
 -to_via_x_size  { 1 1 1 1 1 1 1 1  1 1 1 1 1 1 1 1  1 1 1 1 1  1 1 1 1 1  1 1 1 1 1 } \
 -to_via_y_size  { 1 1 1 1 1 1 1 1  1 1 1 1 1 1 1 1  1 1 1 1 1  1 1 1 1 1  1 1 1 1 1 } \
 -to_via_weights { 8 7 6 5 4 3 2 1  8 7 6 5 4 3 2 1  8 6 4 3 2  8 6 4 3 2  8 6 4 3 2 }

Insert_zrt_redundant_vias –effort high
```

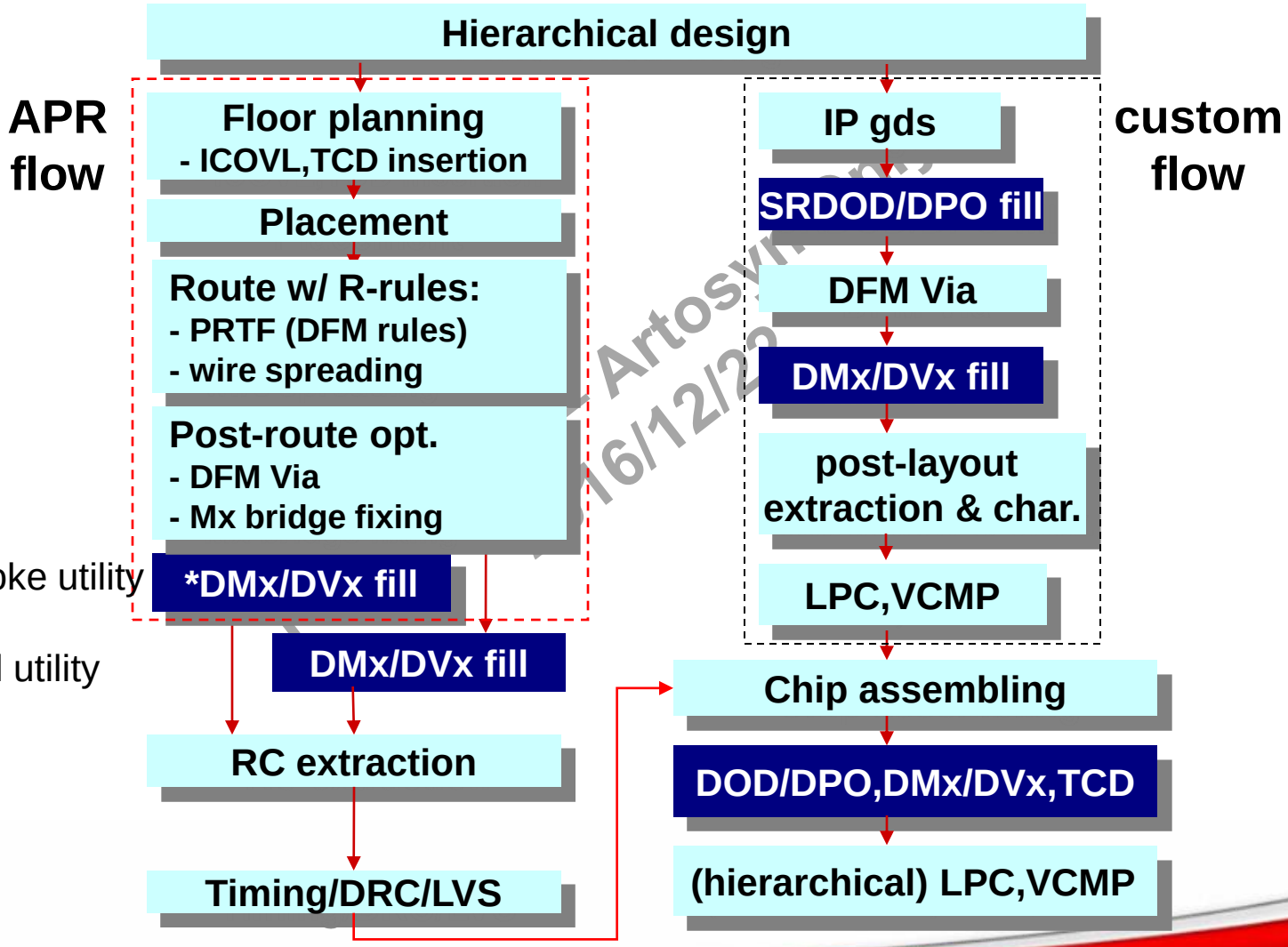
DFM VIA Swapping Template in Mentor Olympus


```
#--- Wire Spreading ---#
spread_wires

#--- Define DFM Via Priority ---#
set_property –name dfm_weight –value 9 –objects [get_lib_vias –of_objects [get_objects –type lib] *FBD*]
set_property –name dfm_weight –value 8 –objects [get_lib_vias –of_objects [get_objects –type lib] *FBS*]
set_property –name dfm_weight –value 7 –objects [get_lib_vias –of_objects [get_objects –type lib] *PBD*]
set_property –name dfm_weight –value 6 –objects [get_lib_vias –of_objects [get_objects –type lib] *PBS*]
set_property –name dfm_weight –value 5 –objects [get_lib_vias –of_objects [get_objects –type lib] *P1*]
set_property –name dfm_weight –value 4 –objects [get_lib_vias –of_objects [get_objects –type lib] *P2*]
set_property –name dfm_weight –value 3 –objects [get_lib_vias –of_objects [get_objects –type lib] *P3*]
set_property –name dfm_weight –value 2 –objects [get_lib_vias –of_objects [get_objects –type lib] *FAT*]
config_lib_vias –use_generated false
replace_vias –type dfm
```

DFM Implementation @ Design Stages

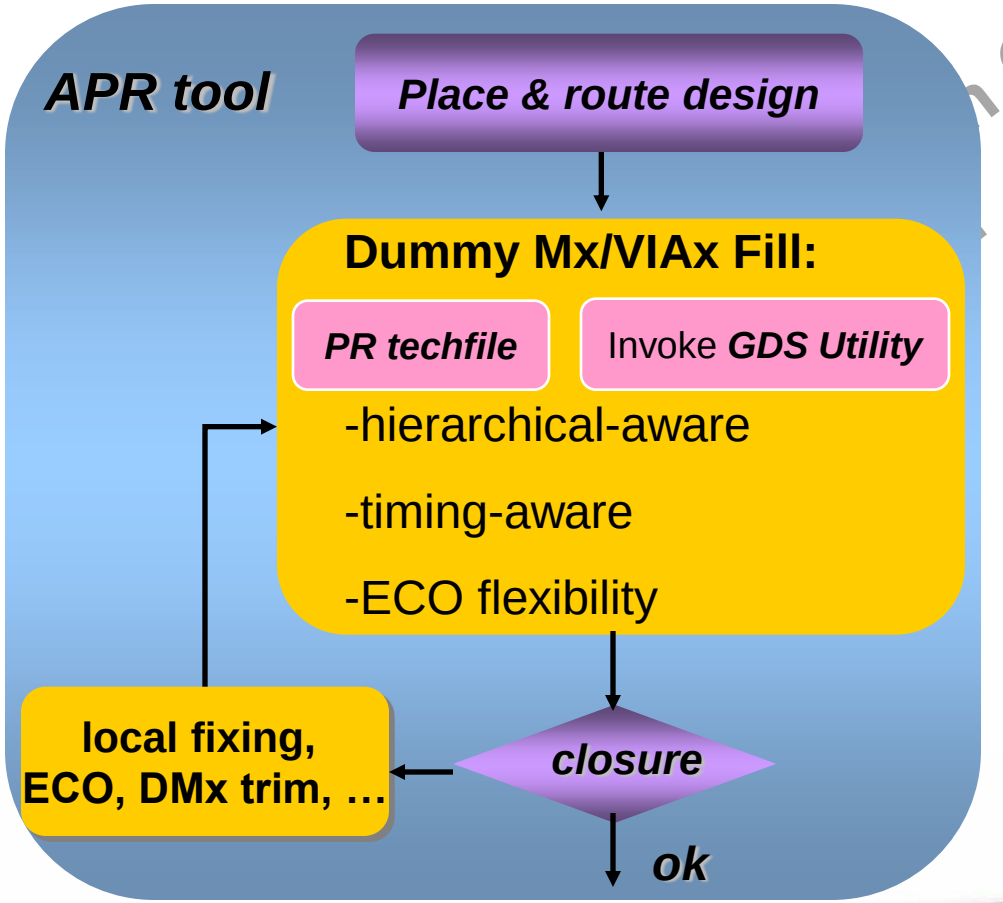
- DFM implementation in both APR, IP and chip-assembly flows

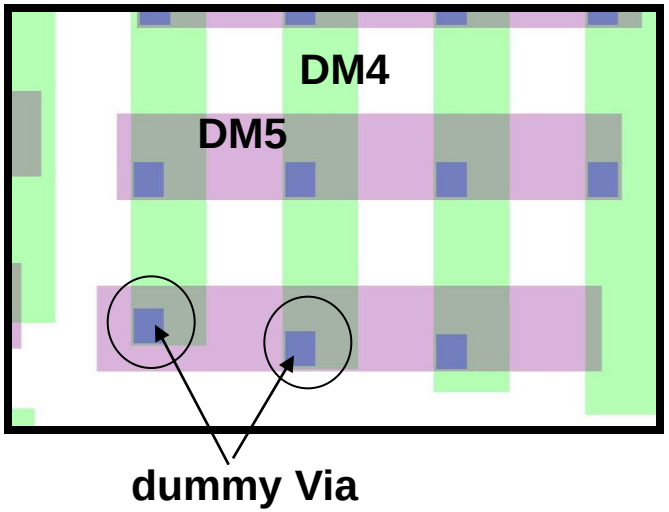


[Options]:
1. APR invoke utility
or
2. gds-level utility

APR to Integrate DMx/DVx Utility

- The integrated APR+DMx/DVx flow stay in the same APR stage, with advantages and improve the design iterations
- Dummy via is must for backend process/reliability





Commands for APR + Mx/VIAx Utility

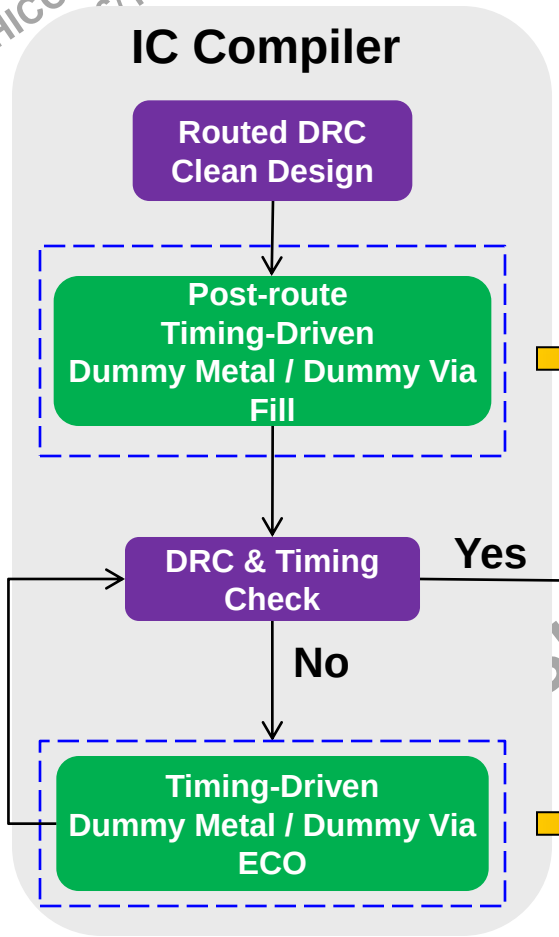
Olympus + Calibre Flow:

```
#---specify the calibre dummy utility---#
config_calibre_mfill -rule_file Dummy_Metal_Via_Calibre_28nm.11a.encrypt
-rule_map $mfill_map -model_based false
#--- select the layers to insert dummy metal/vias ---#
select_calibre_mfill -by_names {DM1_FILL ODM1_FILL DM2_FILL ODM2_FILL DM3_FILL ODM3_FILL
DM4_FILL ODM4_FILL DM5_FILL ODM5_FILL DM6_FILL ODM6_FILL DVIA2_FILL DVIA3_FILL DVIA4_FILL
DVIA5_FILL}
#--- insert dummy metal/vias ---#
insert_metal_fill –mode calibre
```

ICC + ICV Flow:

```
#---specify the ICV dummy utility---#
set_physical_signoff_options -exec_cmd icv -fill_runset Dummy_Metal_Via_ICV_28nm.11a.encrypt
#--- insert dummy metal/vias ---#
signoff_metal_fill
– mode flat
– select_layers {m1 m2 v2 m3 v3 m4 v4 m5 v5 m6}
– allowed_floating_via_type none        #to remove the floating dummy via
```

Commands for ECO Flow: ICC+ICV



done

Command example:
signoff_metal_fill
– mode flat
– timing_preserve_setup_slace_threshold 0.1
–allowed_floating_via_type none *

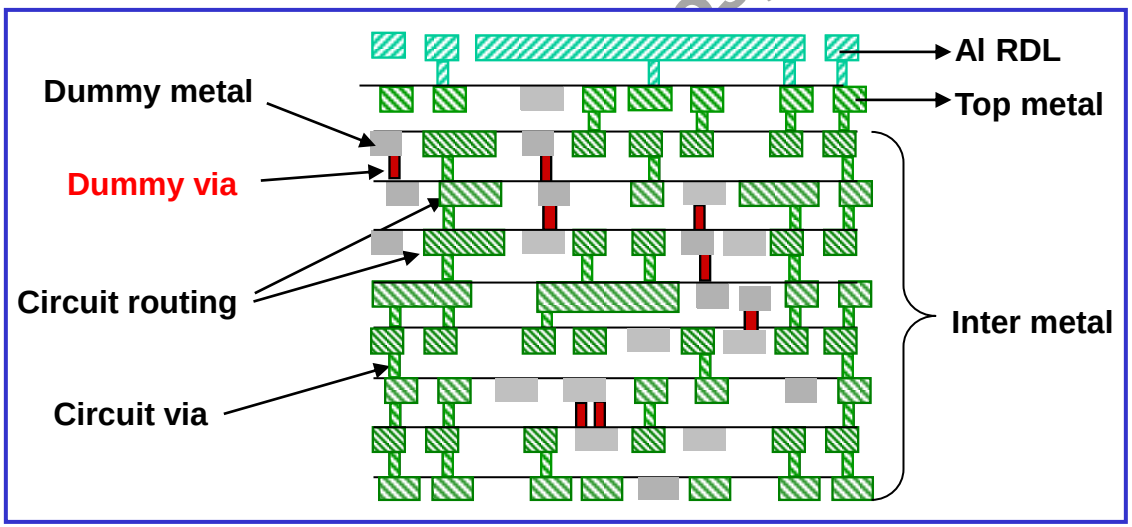
Command example (2 steps):
1) signoff_metal_fill
–remove_overlap_with_nets {get_flat_nets -all}

2) signoff_metal_fill
– mode flat
– timing_preserve_setup_slace_threshold 0.1
–allowed_floating_via_type none *
–eco

***" –allowed_floating_via_type none" will remove the floating DVIAx for timing driven flow**

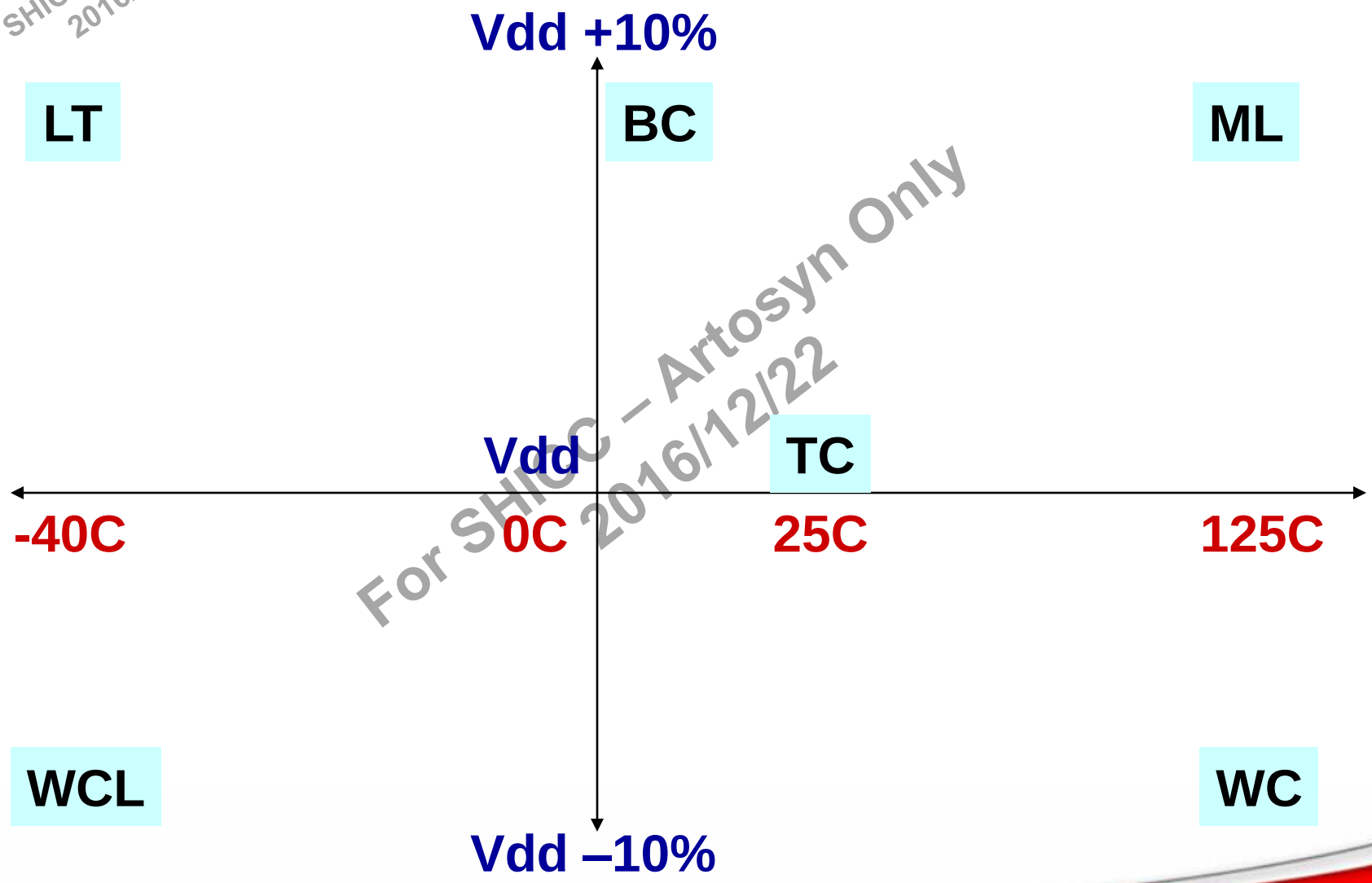
Dummy Via Insert Over Dummy Metal

- Flip chip package requires inter-layer dummy via insert between two dummy metal at adjacent metal layers when there's a sufficient overlap area of dummy metal. In other words, inter-layer dummy VIAx (datatypeL1) is required to be inserted between the overlap of two dummy metal at Mx and Mx+1



- Dummy via algorithm was integrated into TSMC dummy utility

PVT Corner Abbreviations



Temperature Inversion Effect (1)

- Before 65nm, gate delay always increases with temperature increasing
  - It can be synthesized and analyzed by conventional ASIC tools and flows
- Started from 65nm, gate delay is no longer increases with temperature increasing
  - The gate delay might increase with temperature decreasing
- In N40 technology, temperature inversion only happens at SS corner
- In N28 technology, temperature inversion happens at both SS and FF corners

Temperature Inversion Effect (2)

CKND8 in ML corner

```
cell_rise (delay_template_8x8_0) {
  index_1 ("0.0016, 0.0046, 0.0107, 0.0229, 0.0473, 0.0959, 0.1933, 0.3881");
  index_2 ("0.0005, 0.00349, 0.00947, 0.02144, 0.04536, 0.09321, 0.1889, 0.3803");
  values ( \
    "0.002223, 0.003097, 0.004689, 0.007747, 0.01381, 0.02595, 0.05006, 0.09804", \
    "0.00275, 0.003728, 0.00544, 0.008618, 0.01472, 0.02675, 0.05089, 0.099", \
    "0.003319, 0.004642, 0.006749, 0.01015, 0.01651, 0.02871, 0.05281, 0.1009", \
    "0.003951, 0.00569, 0.008436, 0.01272, 0.01957, 0.03229, 0.05671, 0.1049", \
    "0.004709, 0.006917, 0.01044, 0.01598, 0.02466, 0.03846, 0.06386, 0.1127", \
    "0.00548, 0.008257, 0.01275, 0.01995, 0.03109, 0.04848, 0.07609, 0.1269", \
    "0.006112, 0.009655, 0.01532, 0.02449, 0.03896, 0.06138, 0.09615, 0.1515", \
    "0.006676, 0.01074, 0.01797, 0.02962, 0.0479, 0.07671, 0.122, 0.1916" \
  );
}
```

CKND8 in LT corner

```
cell_rise (delay_template_8x8_0) {
  index_1 ("0.0014, 0.0044, 0.0104, 0.0224, 0.0464, 0.0943, 0.1902, 0.3819");
  index_2 ("0.0005, 0.00349, 0.00947, 0.02144, 0.04536, 0.09321, 0.1889, 0.3803");
  values ( \
    "0.002112, 0.002917, 0.004361, 0.00712, 0.01259, 0.02347, 0.04528, 0.08882", \
    "0.002809, 0.003714, 0.005302, 0.008206, 0.01374, 0.02465, 0.04646, 0.09003", \
    "0.003633, 0.004932, 0.006911, 0.01007, 0.0159, 0.027, 0.04878, 0.09234", \
    "0.004651, 0.006448, 0.00916, 0.01323, 0.01958, 0.03127, 0.05349, 0.0971", \
    "0.005965, 0.008342, 0.01206, 0.01758, 0.02588, 0.03864, 0.06206, 0.1066", \
    "0.007703, 0.01077, 0.01569, 0.02321, 0.03446, 0.05103, 0.07665, 0.1235", \
    "0.01021, 0.01418, 0.0206, 0.03033, 0.04552, 0.06797, 0.1015, 0.1527", \
    "0.01405, 0.0189, 0.02702, 0.03987, 0.05973, 0.09005, 0.1352, 0.2023" \
  );
}
```

Temperature Inversion Effect (3)

CKND8 in WC corner

```
cell_rise (delay_template_8x8_0) {
  index_1 ("0.0032, 0.0063, 0.0123, 0.0245, 0.0488, 0.0974, 0.1947, 0.3892");
  index_2 ("0.0005, 0.00349, 0.00947, 0.02144, 0.04536, 0.09321, 0.1889, 0.3803");
  values ( \
    "0.004812, 0.006571, 0.009765, 0.01592, 0.02815, 0.05262, 0.1017, 0.1988", \
    "0.005911, 0.007826, 0.0112, 0.0175, 0.02977, 0.05419, 0.1033, 0.2005", \
    "0.007911, 0.009987, 0.01368, 0.02035, 0.03287, 0.05731, 0.1061, 0.2037", \
    "0.01089, 0.01386, 0.01809, 0.0254, 0.03867, 0.06364, 0.1125, 0.21", \
    "0.01503, 0.01942, 0.02556, 0.03423, 0.04873, 0.07522, 0.1252, 0.2229", \
    "0.02031, 0.02706, 0.03626, 0.04892, 0.06648, 0.09545, 0.1484, 0.2483", \
    "0.02703, 0.03686, 0.05092, 0.06994, 0.09571, 0.131, 0.1888, 0.2947", \
    "0.03558, 0.04904, 0.06967, 0.09845, 0.1372, 0.1889, 0.26, 0.3755" \
  );
}
```

CKND8 in WCL corner

```
cell_rise (delay_template_8x8_0) {
  index_1 ("0.0036, 0.007, 0.0139, 0.0275, 0.0547, 0.1092, 0.2182, 0.4362");
  index_2 ("0.0005, 0.00349, 0.00947, 0.02144, 0.04536, 0.09321, 0.1889, 0.3803");
  values ( \
    "0.006072, 0.008164, 0.01195, 0.01925, 0.03382, 0.06278, 0.1209, 0.2367", \
    "0.007795, 0.01008, 0.01409, 0.02156, 0.0361, 0.06508, 0.123, 0.2391", \
    "0.01096, 0.01355, 0.01802, 0.02596, 0.04083, 0.06988, 0.1278, 0.2437", \
    "0.01687, 0.01978, 0.02483, 0.03368, 0.04951, 0.07926, 0.1373, 0.2532", \
    "0.02678, 0.03121, 0.03736, 0.04726, 0.06491, 0.09653, 0.156, 0.2719", \
    "0.04329, 0.05038, 0.05987, 0.07235, 0.09209, 0.1274, 0.1907, 0.3096", \
    "0.07095, 0.08235, 0.09719, 0.1167, 0.1423, 0.1819, 0.2525, 0.3791", \
    "0.1162, 0.1357, 0.16, 0.1908, 0.2309, 0.2821, 0.3612, 0.5025" \
  );
}
```

Default OCV Generation Assumptions (Nominal Voltage=0.9v)

- Based on N28HPC+ 110a library & v1.0_2p1 SPICE model
- PVT corner: SSG_0.81v_m40c & FFG_0p99v_m40c
- Clock cell: CKND2BWP7T30P140
- Max clock slew at SSG_0.81_m40C: 150ps
- Data cell: INVD1BWP7T30P140
- Max data slew at SSG_0.81v_m40C: 250ps
- IR drop (VDD-VSS variation) : +/-2.5% for SSG, +/-5% for FFG
- [NOTE!] Applying default OCV on looser design spec may cause design risk
  - EX: lower voltage corner, smaller cell, larger slew, larger IR drop
  - Please consult TSMC for OCV customization support

28HPC+ STA Timing Recommendations (Sample only)

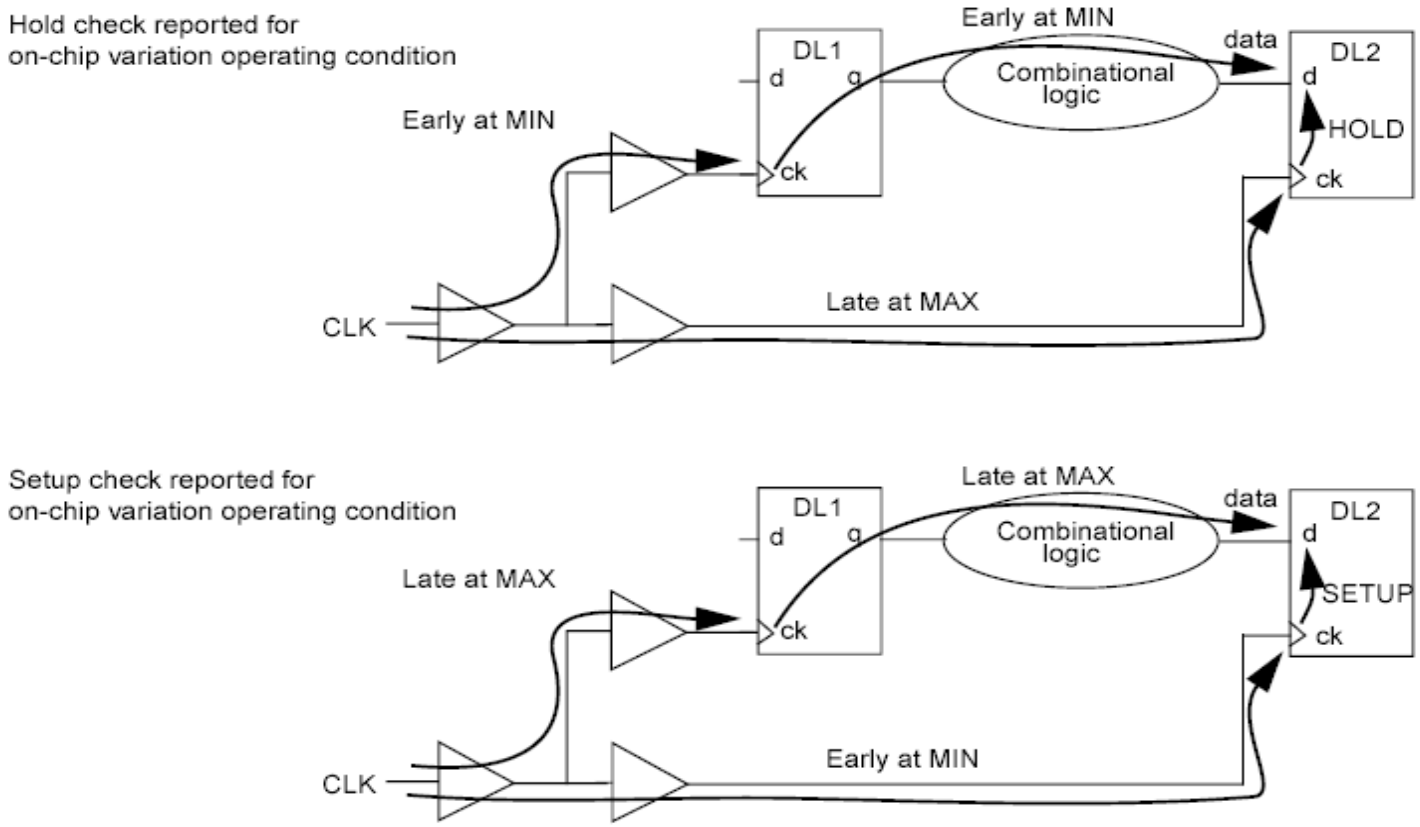
Timing Check	Library PVT Conditions	RC Corner	OCV and Design Margin
Setup	SSG/0.81/125C	Cworst_T	(a) +3.2% on launch clock cell, +7.1% on data cell and -3.2% on capture cell (b) +6% on launch clock net, +6% on data net and -6% on capture net (c) Clock jitter + 25ps setup margin
		Rcworst_T	
	SSG/0.81/-40C	Cworst_T	
		Rcworst_T	
Hold	SSG/0.81/125C	Cworst	(a) -4.6% on launch clock cell, -9.6% on data cell and +4.6% on capture cell (b) -8.5% on launch clock net, -8.5% on data net (c) 50ps hold margin
		Rcworst	
	SSG/0.81/-40C	Cworst	
		Rcworst	
	FFG/0.99/125C	Cworst	(a) -7.2% on launch clock cell, -12.1% on data cell and +7.2% on capture cell (b) -8.5% on launch clock net, -8.5% on data net (c) 40ps hold margin
		Rcworst	
	FFG/0.99/-40C	Cworst	
		Rcworst	
	FFG/0.99/125C	Cbest	(a) -7.2% on launch clock cell, -12.1% on data cell and +7.2% on capture cell (b) +8.5% on capture net (c) 40ps hold margin
		Rcbest	
	FFG/0.99/-40C	Cbest	
		Rcbest	

OCV Setting in STA

- Only set OCV on clock except hold check in FF corner
- OCV is process and design dependent
  - Depending on intra die process and RC variation
  - Depending on clock tree size, routing layers, voltage drop and chip temperature
- Focus on on-chip clock latency variation
- For example: 28HPM OCV setting in Prime Time
  - WCL -8%, BC +14%

```
set_operating_condition -analysis_type on_chip_variation
set timing_remove_clock_reconvergence_pessimism true
SS corner for setup check                FF corner for hold check
set_timing_ferate -early 0.92            set_timing_derate -early 1.0
set_timing_derate -late 1.0              set_timing_derate -late  1.14
```

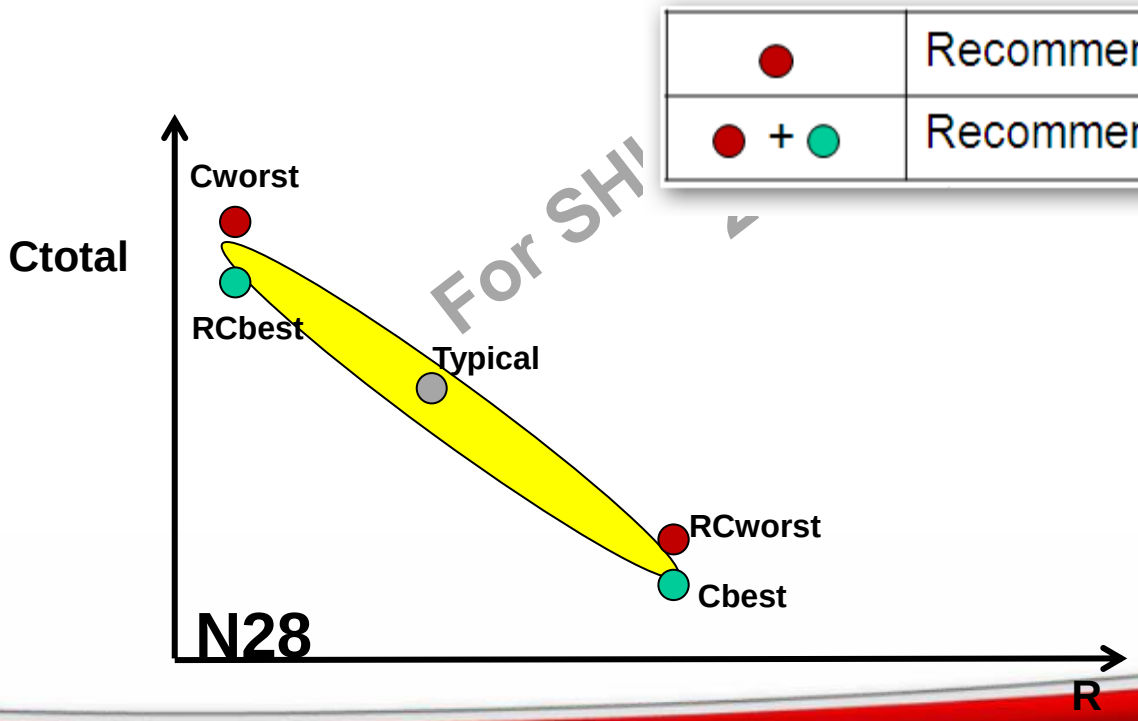
What is On Chip Variation (OCV)



Overly optimistic OCV – Not enough margins to cover PVT variation
Overly pessimistic OCV – Too conservative to make timing closure

N28 RC Corners

- 5 RC corners to cover all RC variations
- From resistance (*R*) point of view
  - R_{max} in Cbest corner is similar to R_{max} in RCworst corner
  - R_{min} in Cworst corner is similar to R_{min} in RCbest corner

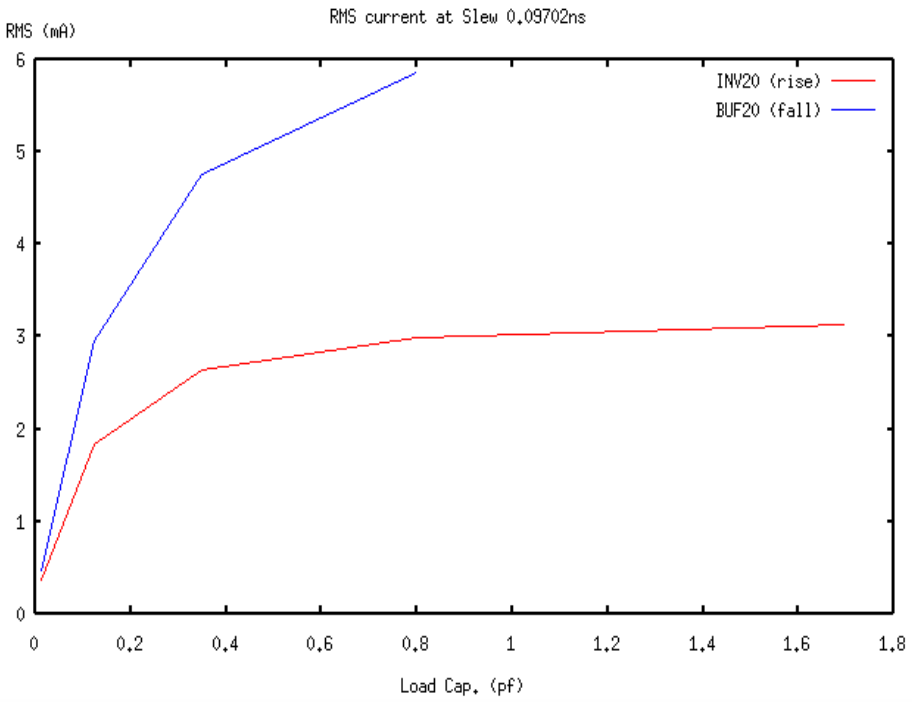


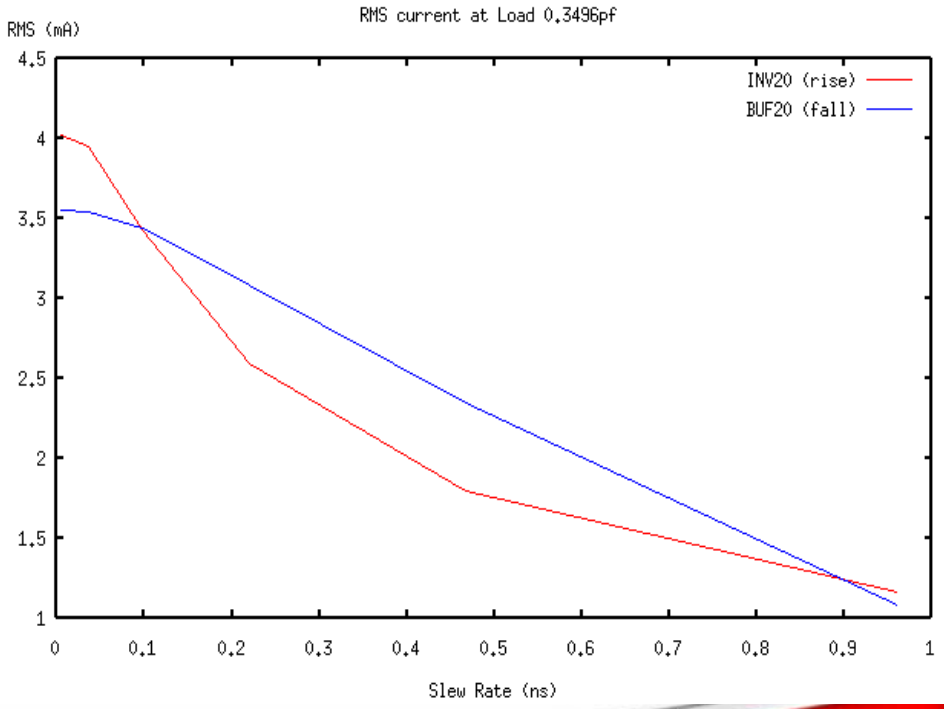
Process/Noise Aware CTS

- Double spacing/width spec for clock nets
  - Minimize crosstalk (coupling capacitance) effect
- Restrict clock buffer types to CKND8, CKND12 and CKND16 only
  - Minimize process variation effect on different types of cells
  - Use clock inverter for better duty cycle
- Use only ‘stronger’ VT cells for CTS when doing mixed VT design
  - For example, use LVT for LVT/SVT mixed designs
  - Simply speaking, no HVT for CTS and flip-flops
- Avoid of CKND20, CKND24 cells for SEM concerns
- Avoid of CK cell types under CKND2 for process variation and OCV concerns

Sources of Signal EM Violations

- Fast slew rate
- Large output loading
- Short clock period



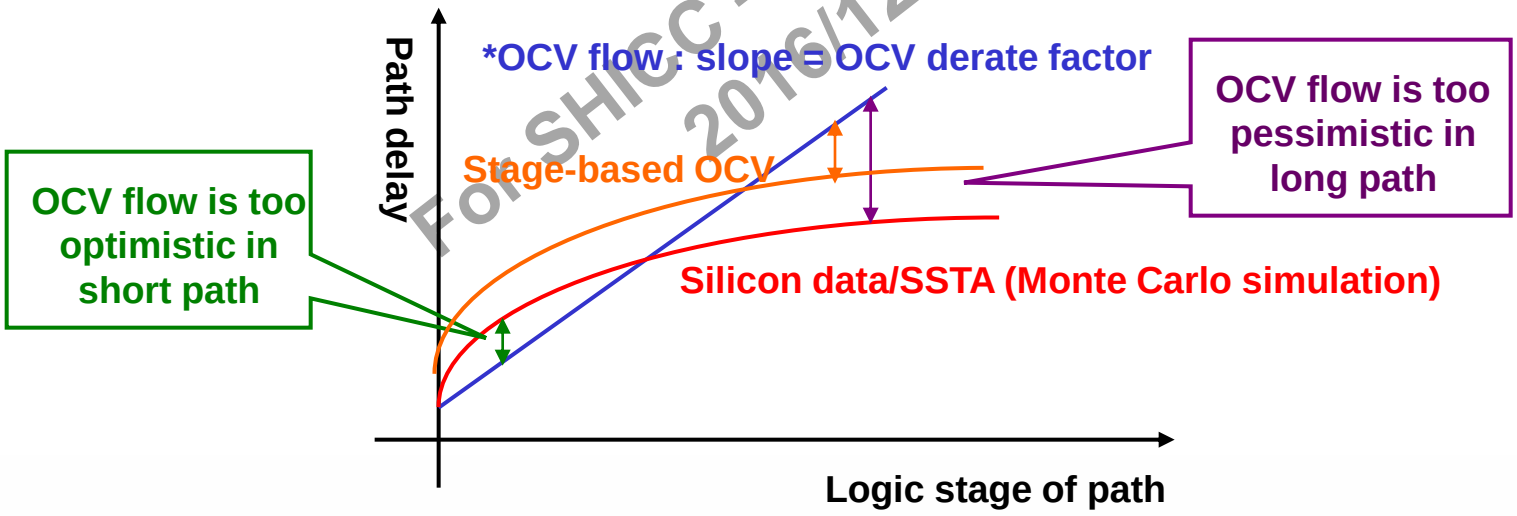


EM on Clock Nets

- Clock buffers often drive lots of cells with fast slew rates and large toggle rates
- However, fixing EM violations on clock nets after detailed route will affect clock latencies and skews
- Users can set maximum capacitance or length constraints for clock buffers to prevent EM violations

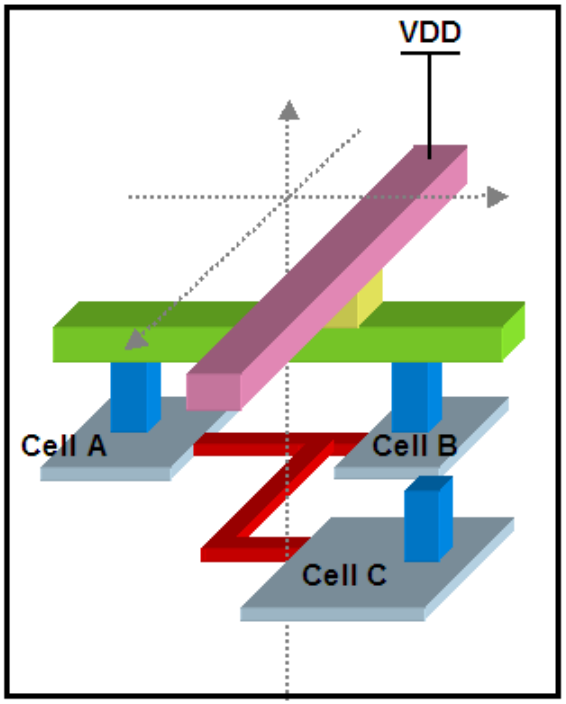
Stage-Based OCV

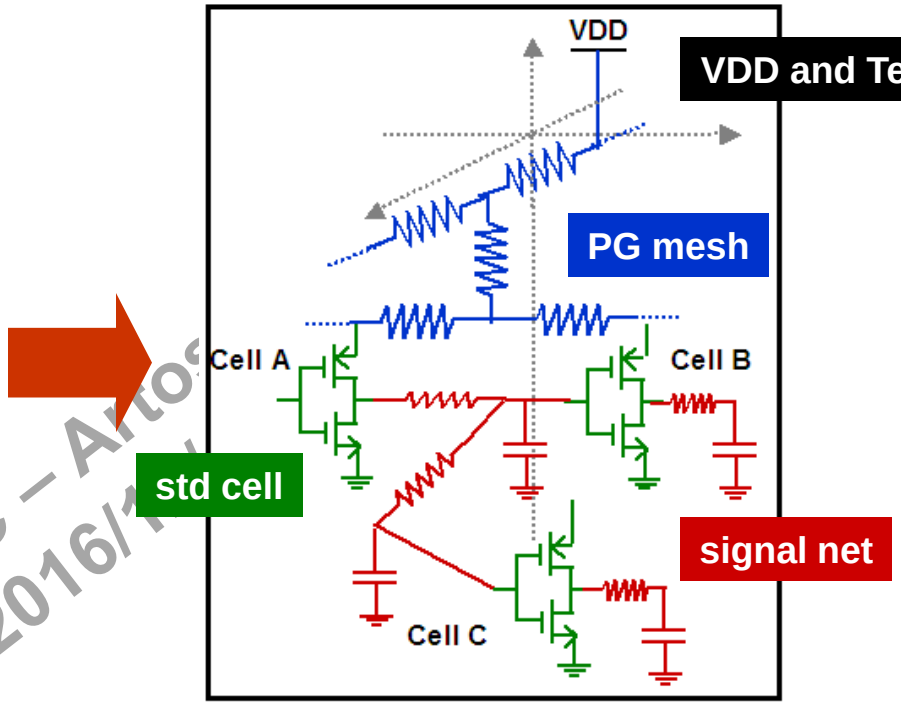
- **Purpose: To reduce pessimism of assuming all devices in worst case corner - remove redundant margin**
- **Methodology: Use local canceling effect to make OCV factor depend on the depth of cells in a timing path**
  - **Small OCV factor for long stages**
  - **Large OCV factor for short stages**



*OCV is derived by using CKND2 with 15 stages.

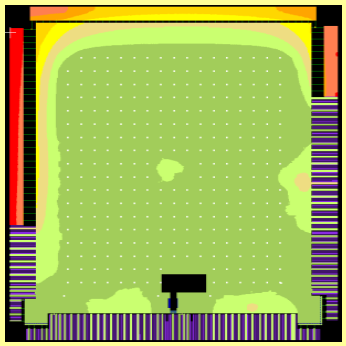
Power/IR Calculation Setup





Std cell library	**ML corner** for maximum leakage
VDD and Temperature	**High VDD** and **High Temp** to be consistent with **ML corner**
Signal net extraction	**Cworst** for maximum switching power
PG mesh extraction	**Typical corner** considering less variation in wider/thicker metal

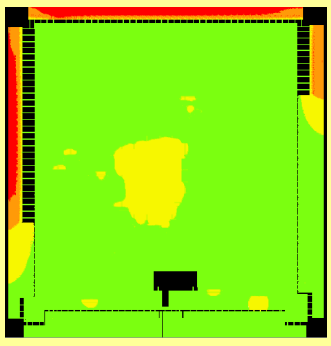
Static vs. Dynamic IR Drop



Static IR

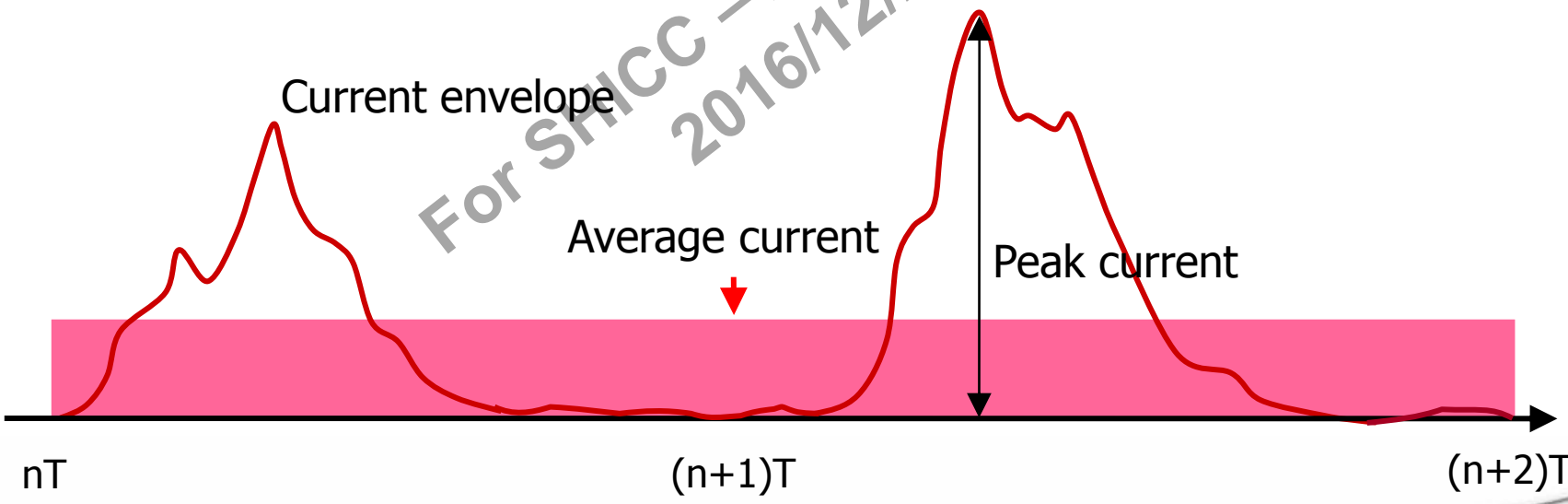
Max IR-drop: 33mV

VS



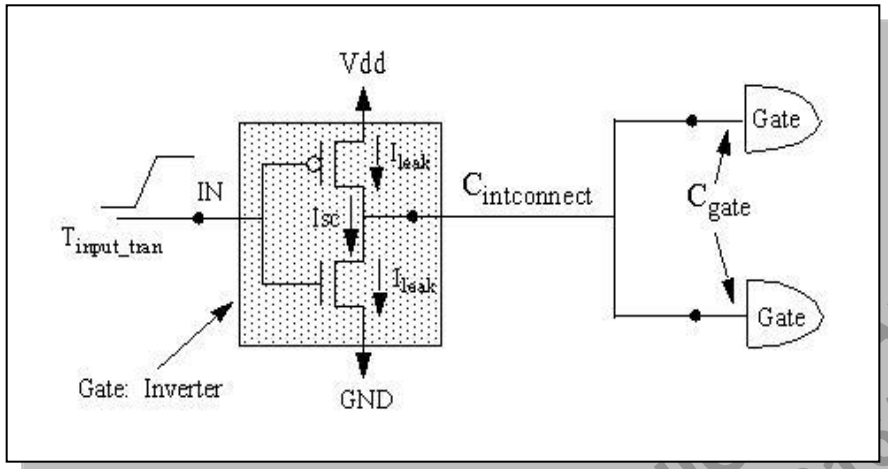
Dynamic IR

Max IR-drop: 230mV



Gate-level Static Power and IR Drop

$$P_{avg} = P_{leakage} + P_{internal} + P_{switching}$$



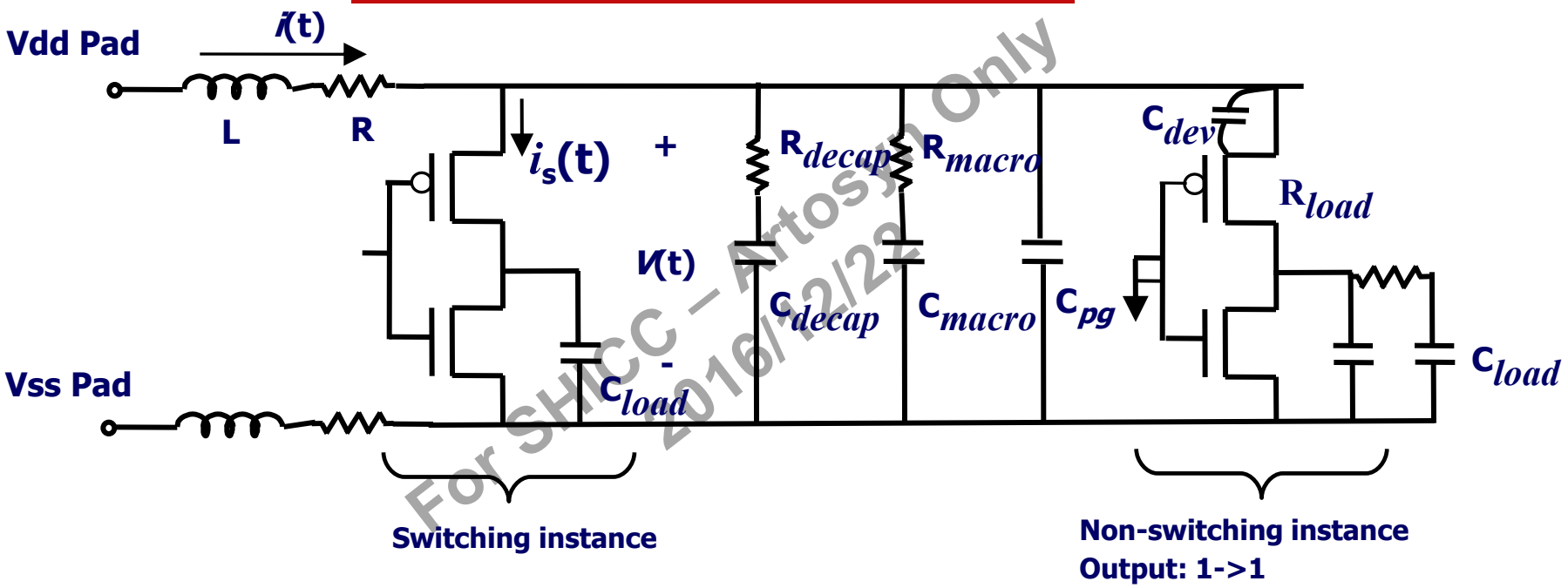
Gate Active Average Power is function of input slew, output load (.lib power tables) linearly proportional to frequency and toggle rate

- Static voltage drop, V_{static} :
  - ***I*** : Average current
  - ***R*** : P/G resistance mesh networks
- V_{static} is computed at every node by matrix inversion

Static Voltage Drop Analysis Gives You A Good Indication of Power Plan Robustness

Dynamic Voltage Drop –The Complete Picture

On-chip power/ground network



- On-chip power/ground network → R,L,C mesh
- Switching instances → PWL current sources
- Non-switching instances → Equivalent decaps

Dynamic Voltage Drop

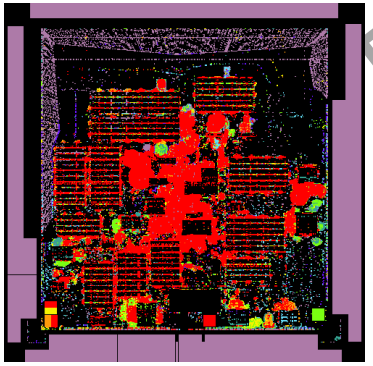
- Dynamic IR analysis checks the temporal relationships between
  - Simultaneous switching events
  - The impact of intrinsic and intentional decoupling capacitance
  - The impact of on-chip and off-chip inductive noise (*Ldi/dt* and LC resonance)
- Dynamic peak contribution to IR drop [*i(t)R* and *Ldi/dt*] can exceed static IR by more than 3~5X on high frequency chips for designs under 90nm
  - Impact on timing and functional failure

Spike Current Causing Chip Failure Can Only be Identified by Dynamic Voltage Drop Analysis

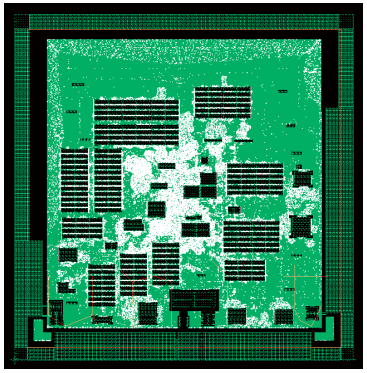
DCAP Insertion

- Evenly spread DCAP after routing stage in the flow
- Place DCAP close to localized hot spot because of dynamic voltage drop
- Use DCAP abutted approach for clock cells
  - If no DCCK cells in the library for CTS

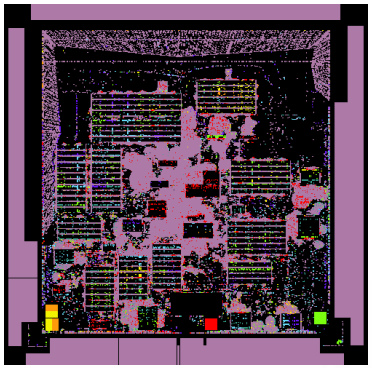
Max IR-drop in the original design: 276mv



DCAP Insertion

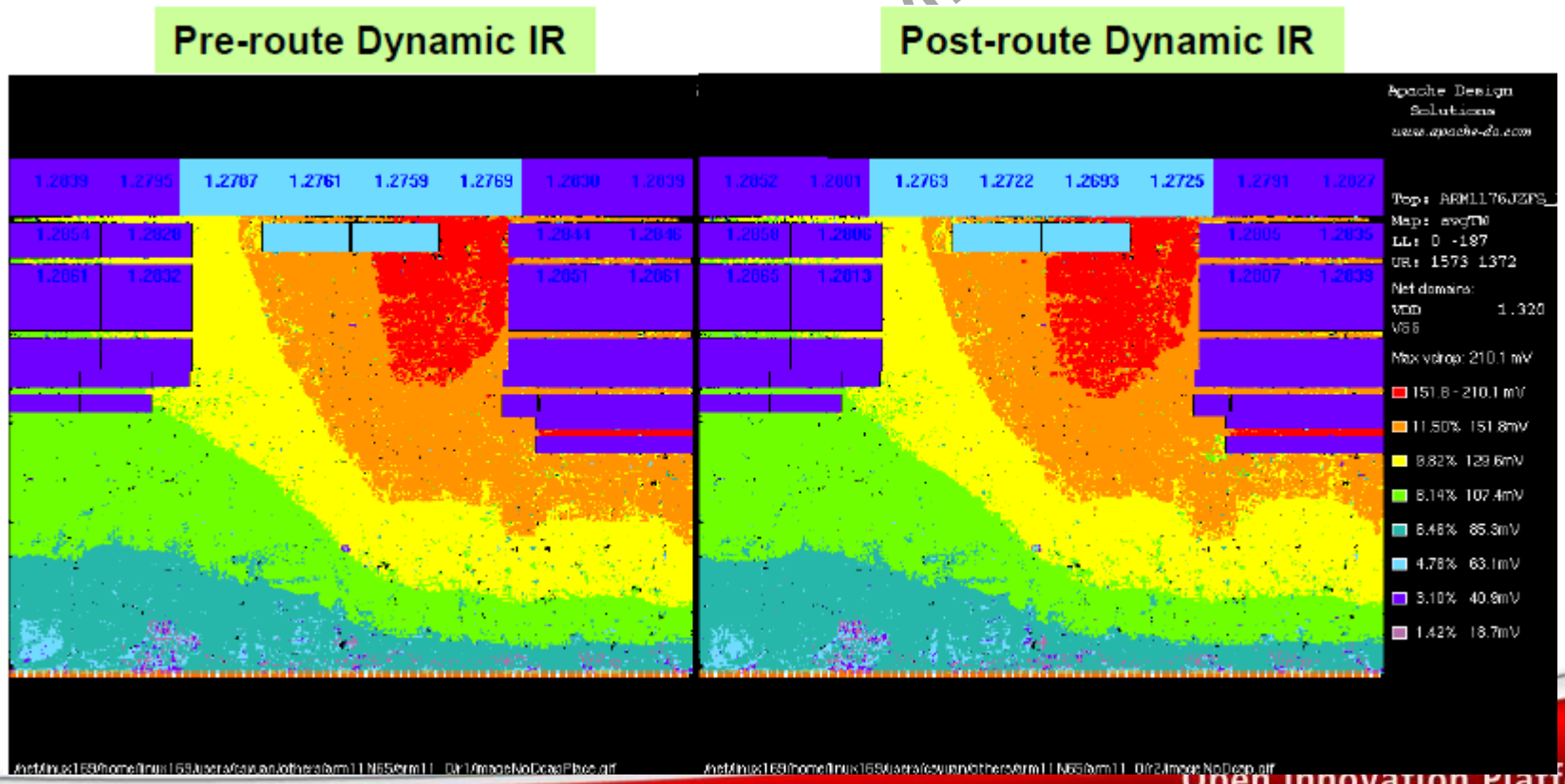


Max IR-drop after DCAP Insertion: 202mv



Analyze Dynamic IR in Pre-Route Stage

- **Dynamic IR correlation between pre-route and post-route stages**
  - **Global route SPEF vs detailed route SPEF**

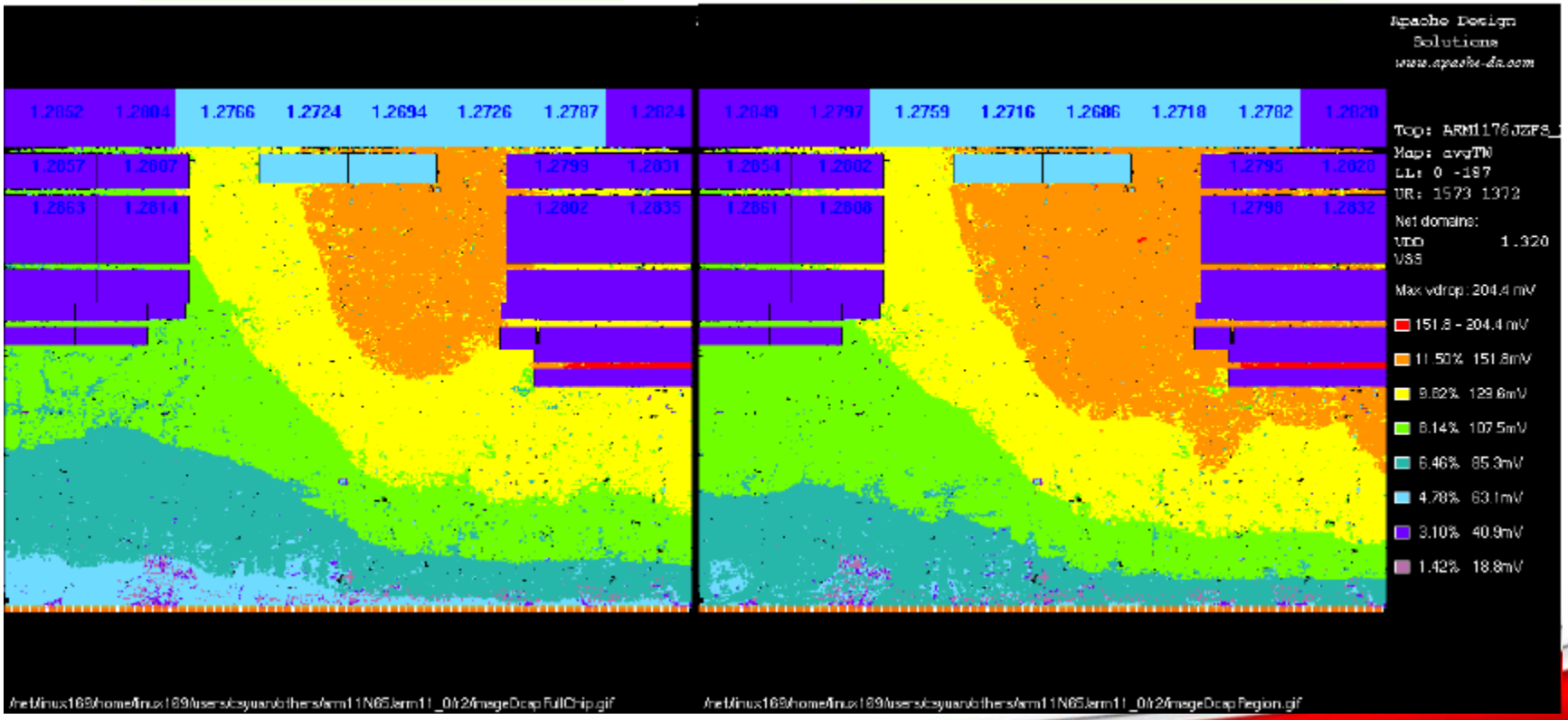


Full Chip v.s. Regional DCAP Insertion

- If no leakage concern, full chip insertion can gain more IR enhancement

Full Chip DCAP Insertion

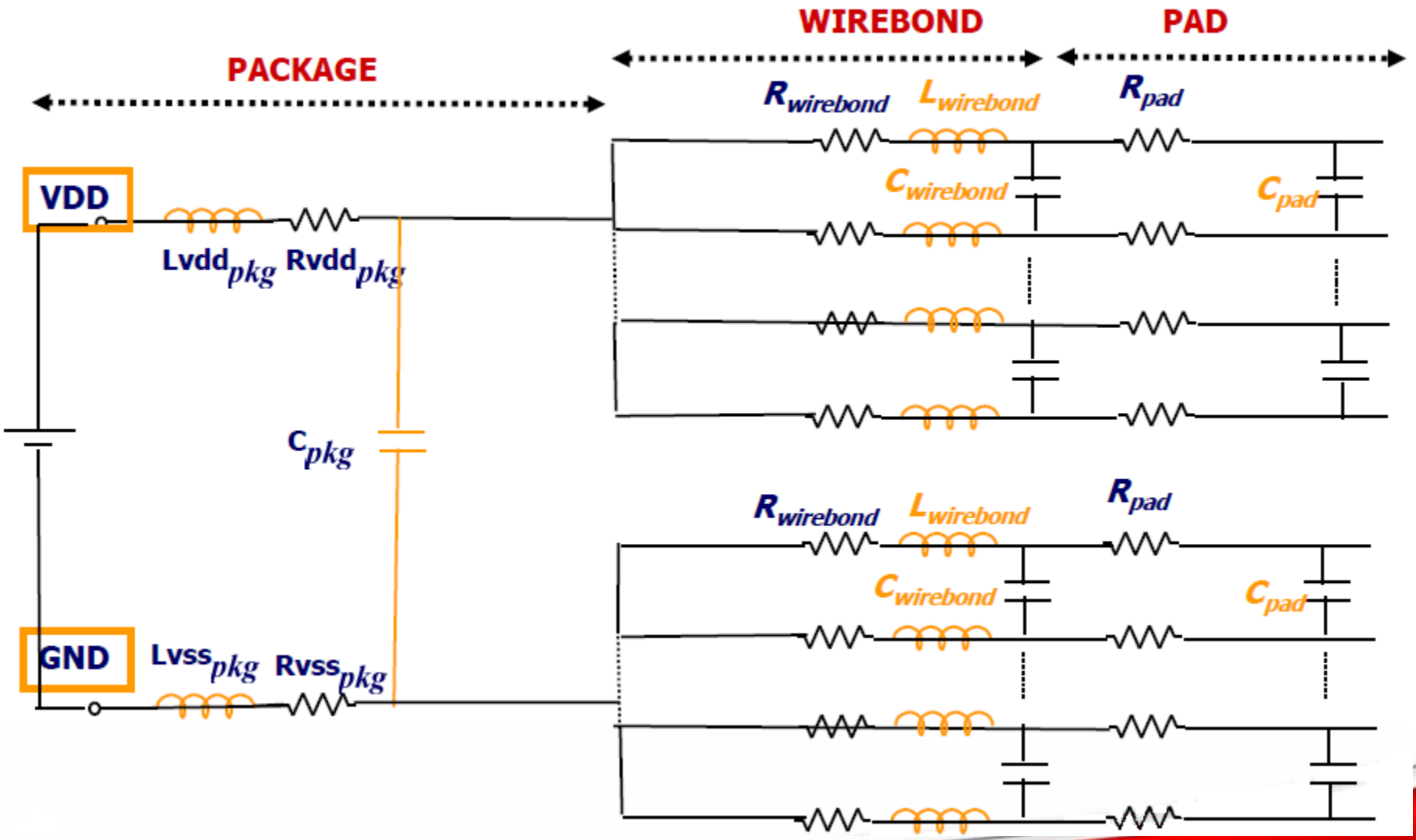
Regional DCAP Insertion



Power Integrity Recommendations

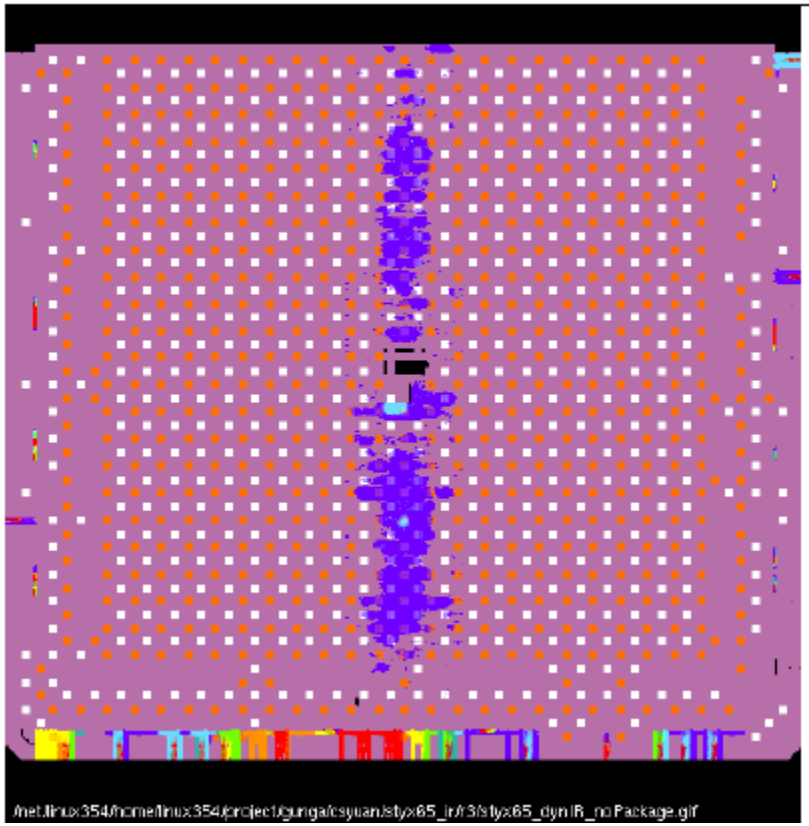
- **Power integrity sign-off in several modes**
  - **Power calculation corner: ML + Cworst RC**
  - **Power integrity analysis corner: TC(RC of PG mesh) with total average power from power calculation**
  - **Static IR drop**
    - **3% for VDD + VSS (Flip chip)**
    - **5% for VDD + VSS (Package type is wire bond)**
    - **Average power IR drop**
  - **Dynamic IR drop**
    - **Around 3~5X in signoff constraint, avoid of local hotspot**
    - **Scan Mode IR drop**
      - Peak power usually around clock-edge
      - Analyzing IR drop during small timing window when flops are switching at the same time

Going Beyond Chip ItselfPackage Model in Dynamic IR



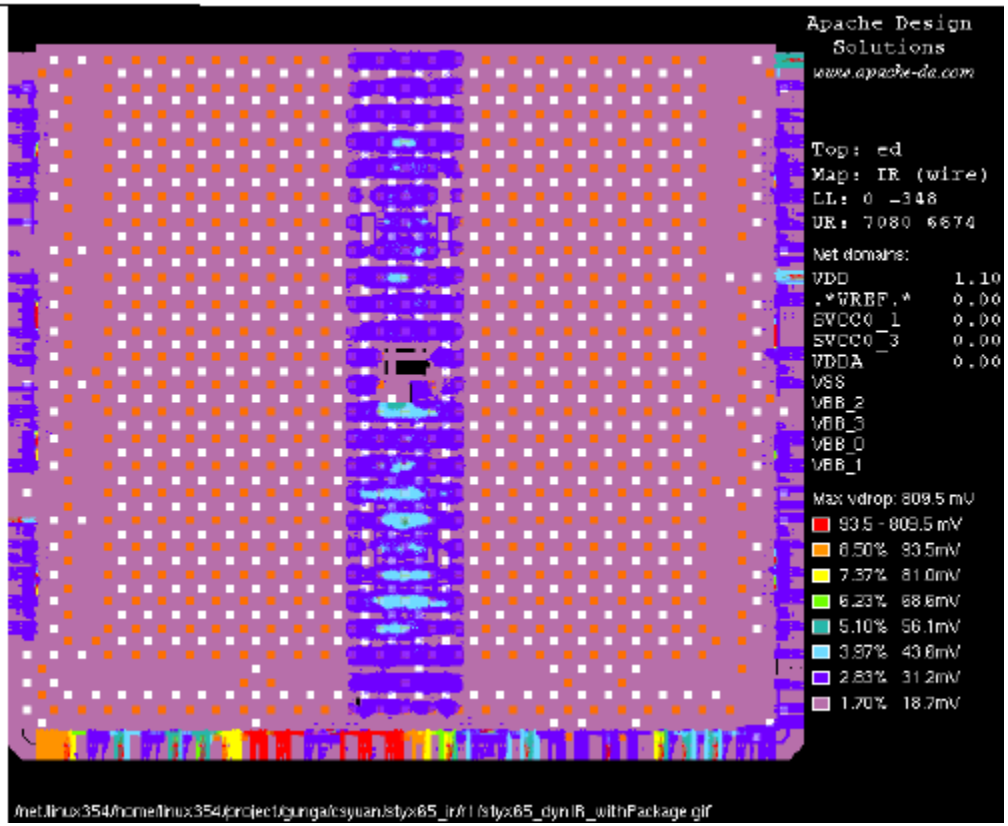
Dynamic IR W/Wo Package R Spice Model

Without package model



Max Voltage Drop – 35mV in core area

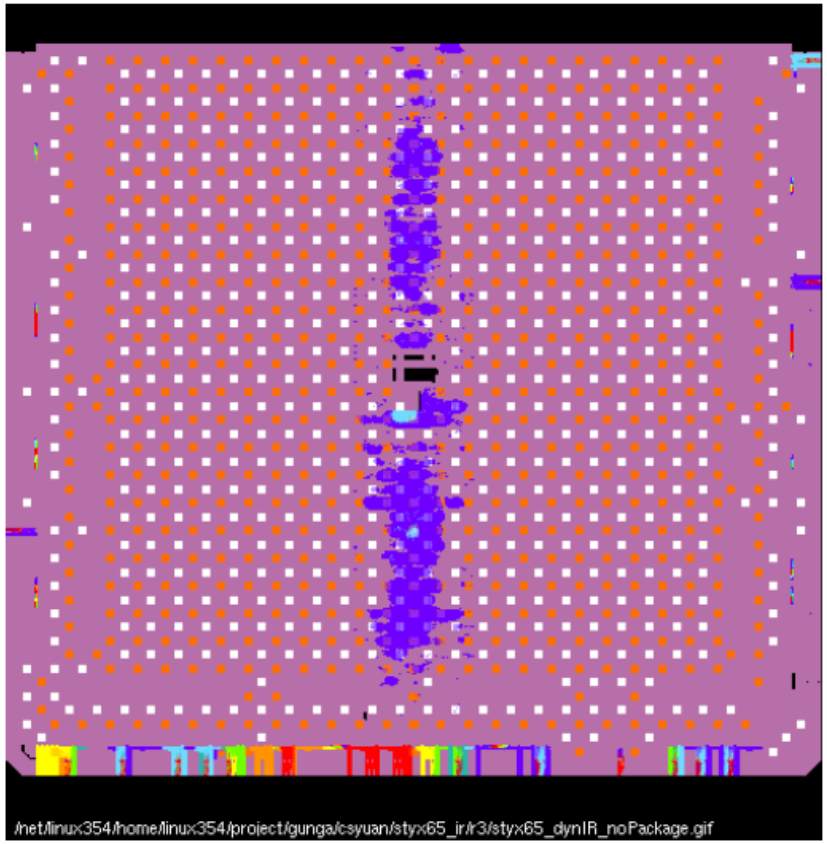
With package R model



Max Voltage Drop – 45mV in core area

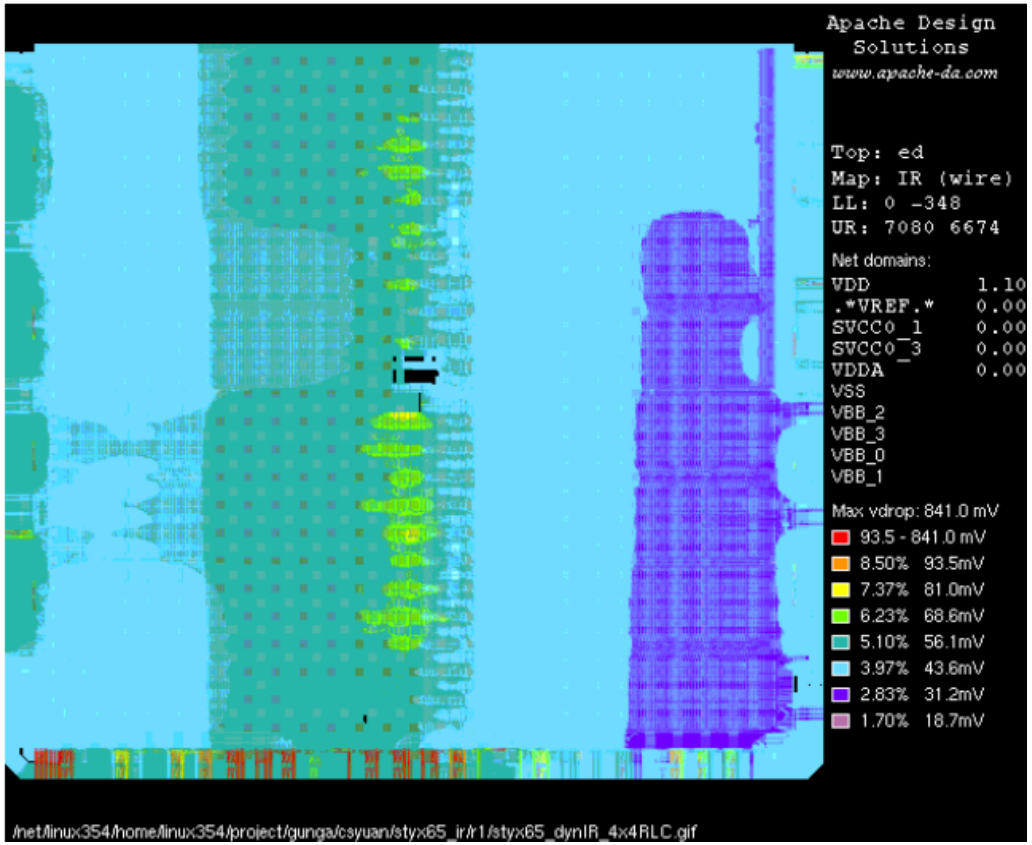
Dynamic IR W/Wo Package RLC Spice Model (4x4 RLC Matrix)

Without package model



Max Voltage Drop – 35mV in core area

With package RLC model

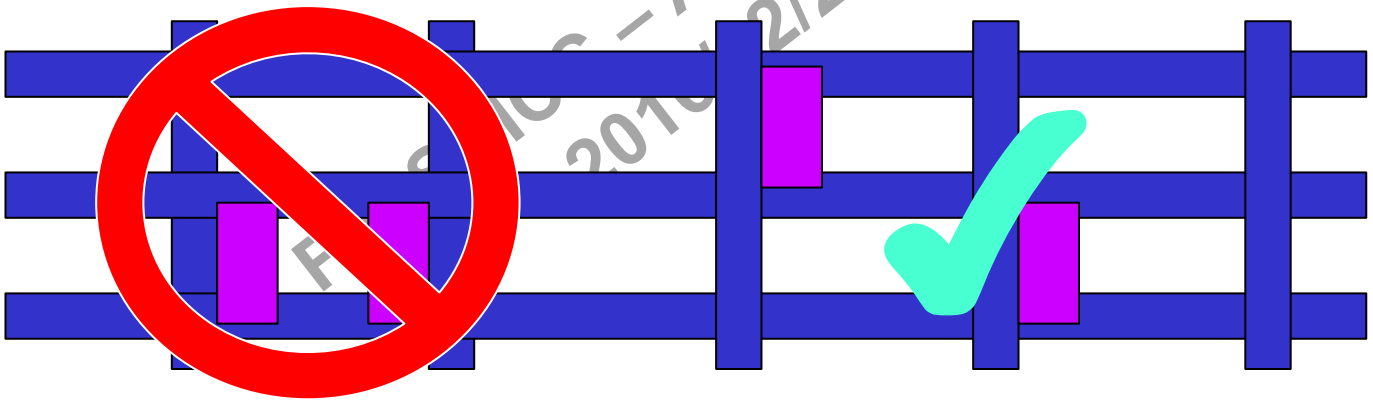


Max Voltage Drop – 73 mV in core area

Power EM Concerns

	Foumula	Imax (mA)
DC I_{max}@110C	2 * 0.996 * (w * 0.9 - 0.003)	**0.4422**

- **EM will be a problem**
  - **If using high driving cells (>= D16) at clock tree**
  - **If clock tree cells placed in adjacent row**
  - **If high output capacitance loading in clock tree**

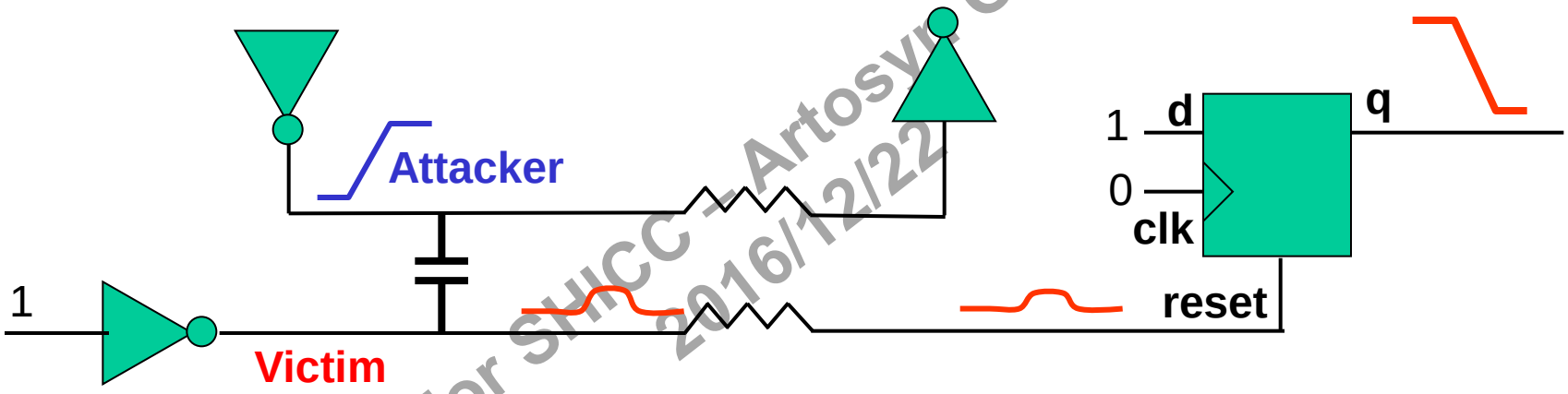


Analyze Crosstalk Effect (SI)

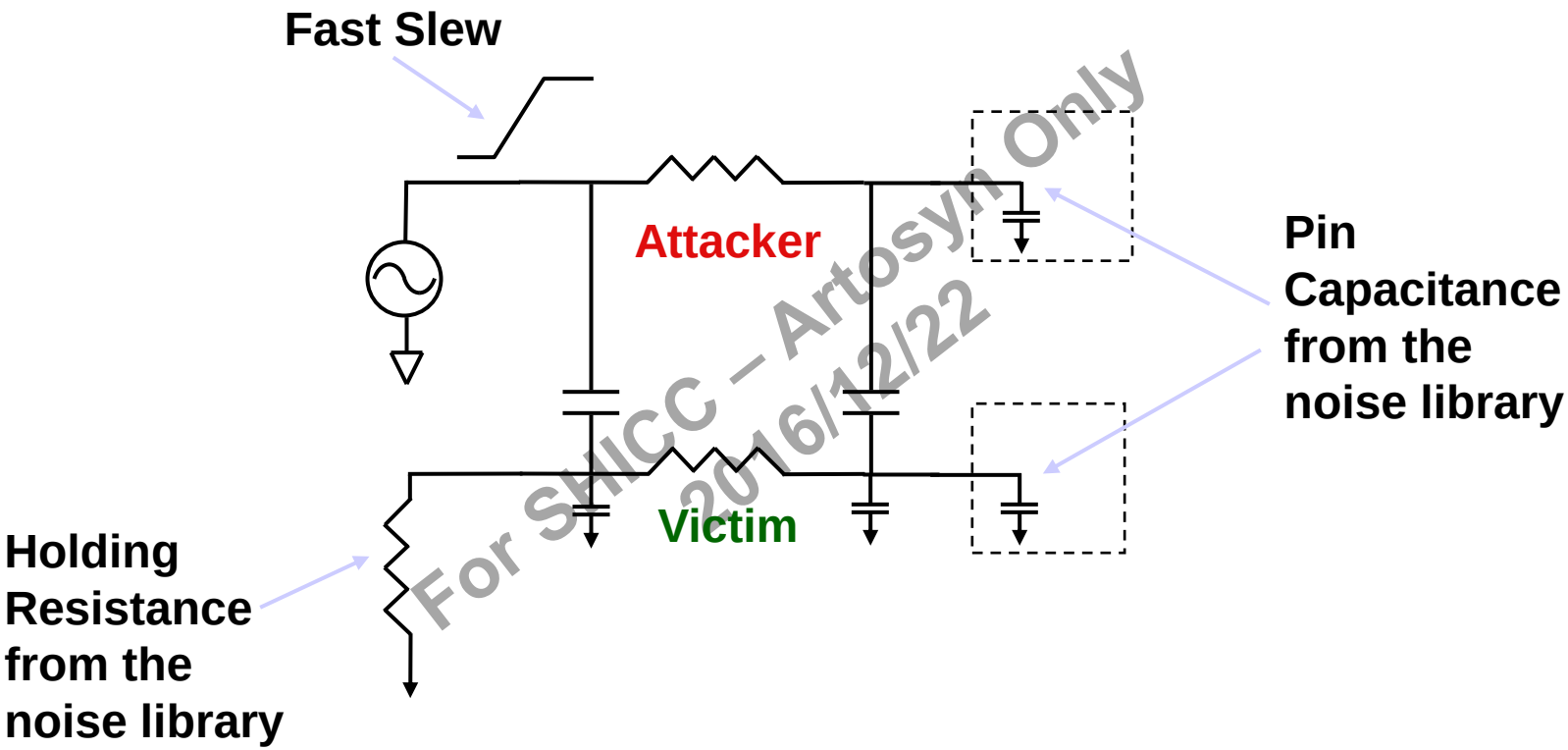
- Calculates coupling noise for nets with coupling capacitance
- Performs noise immunity (sensitivity) analysis on nets exceeding noise threshold
- Performs delay uncertainty analysis on nets exceeding noise threshold
- Different thresholds are specified in the noise library for different cell pins

Impact of Noise on Functionality

- Coupling noise can cause functional failures

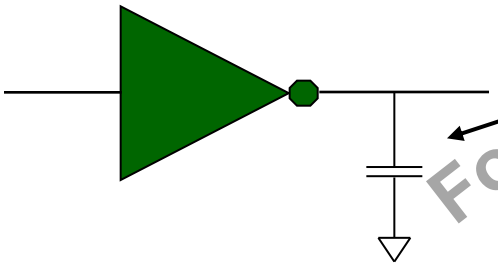


Noise Induced Delay Calculation

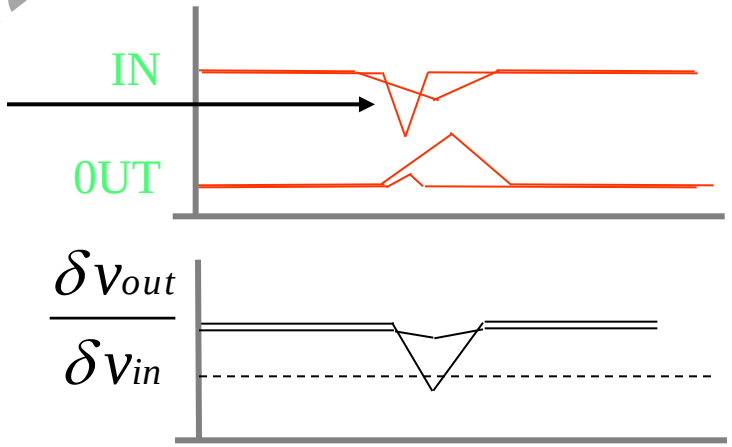


Noise Immunity Analysis

- Calculates the sensitivity for each receiver to worst-case coupling noise
- Accounts for the transient effects of noise

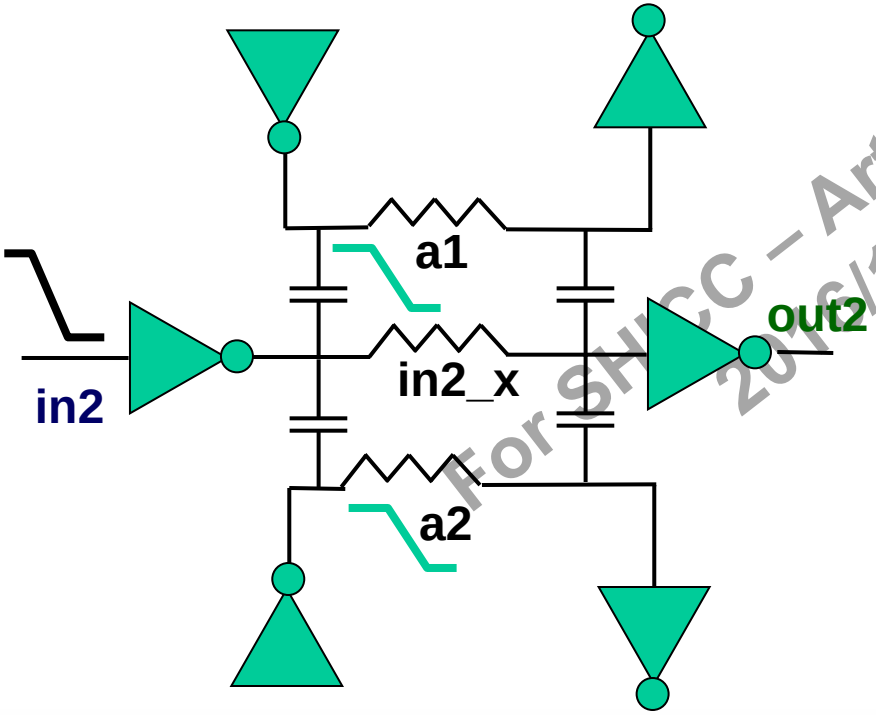


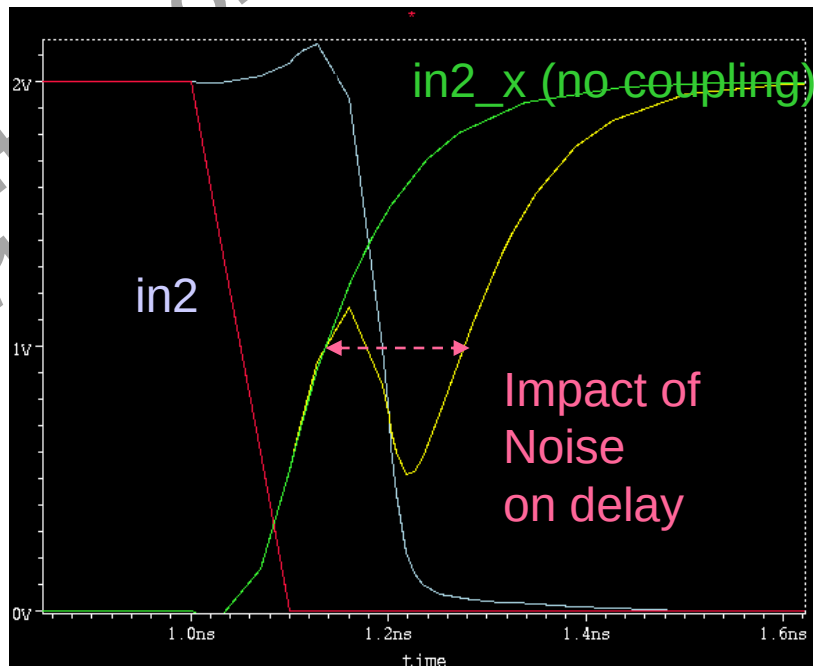
Noise sensitivity is dependent on input waveform shape and output loading



Impact of Noise on Delay

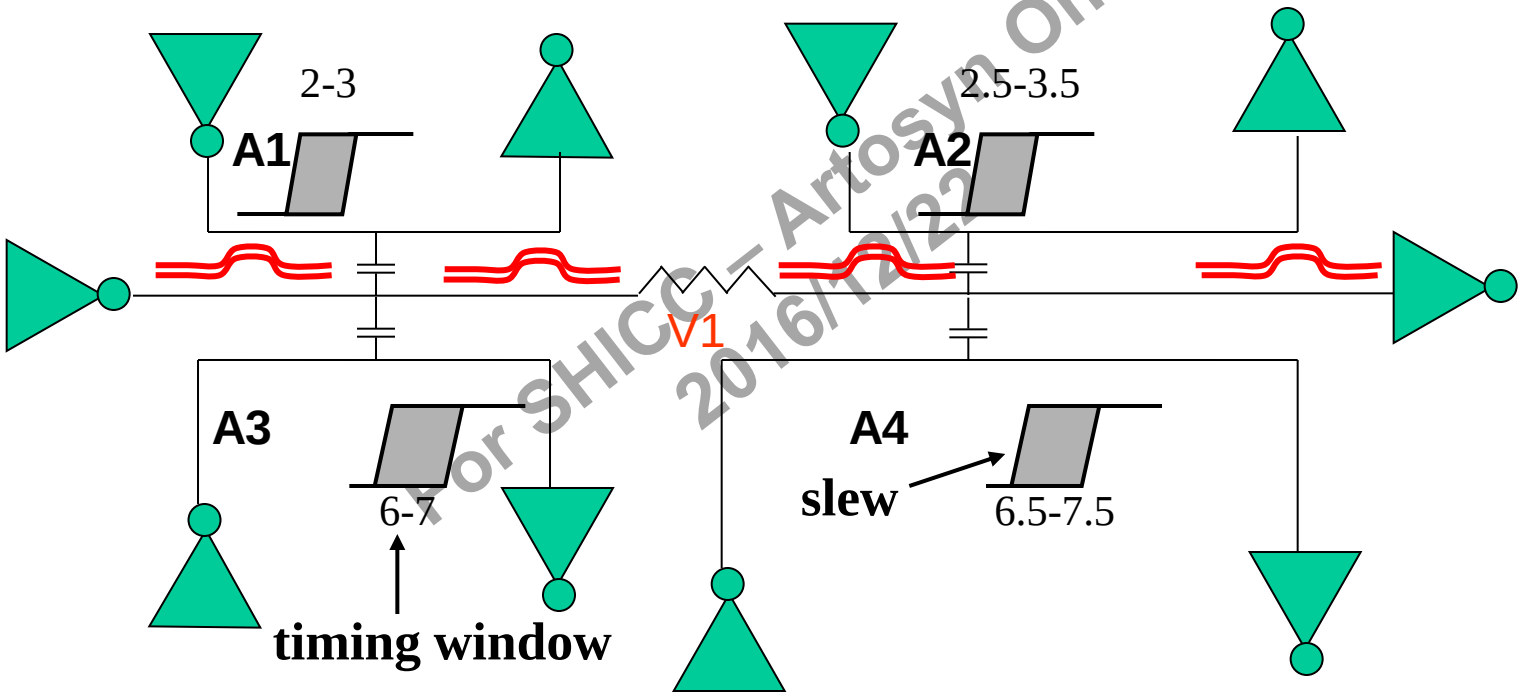
- Coupling noise can impact delay





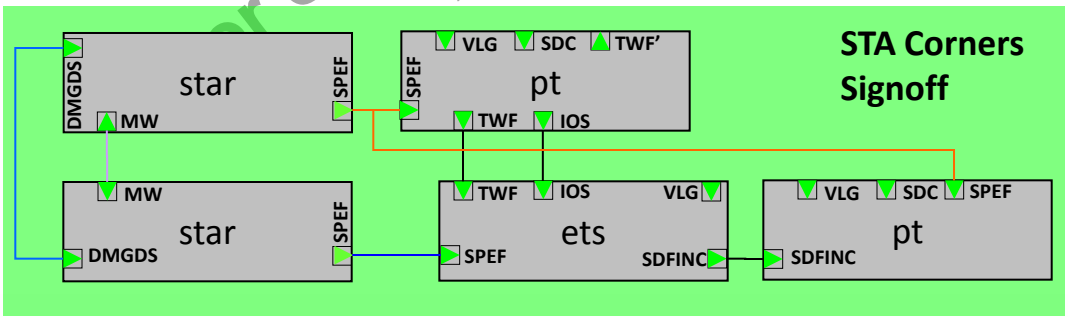
Timing Windows and Slews

- Use timing windows and slews from STA

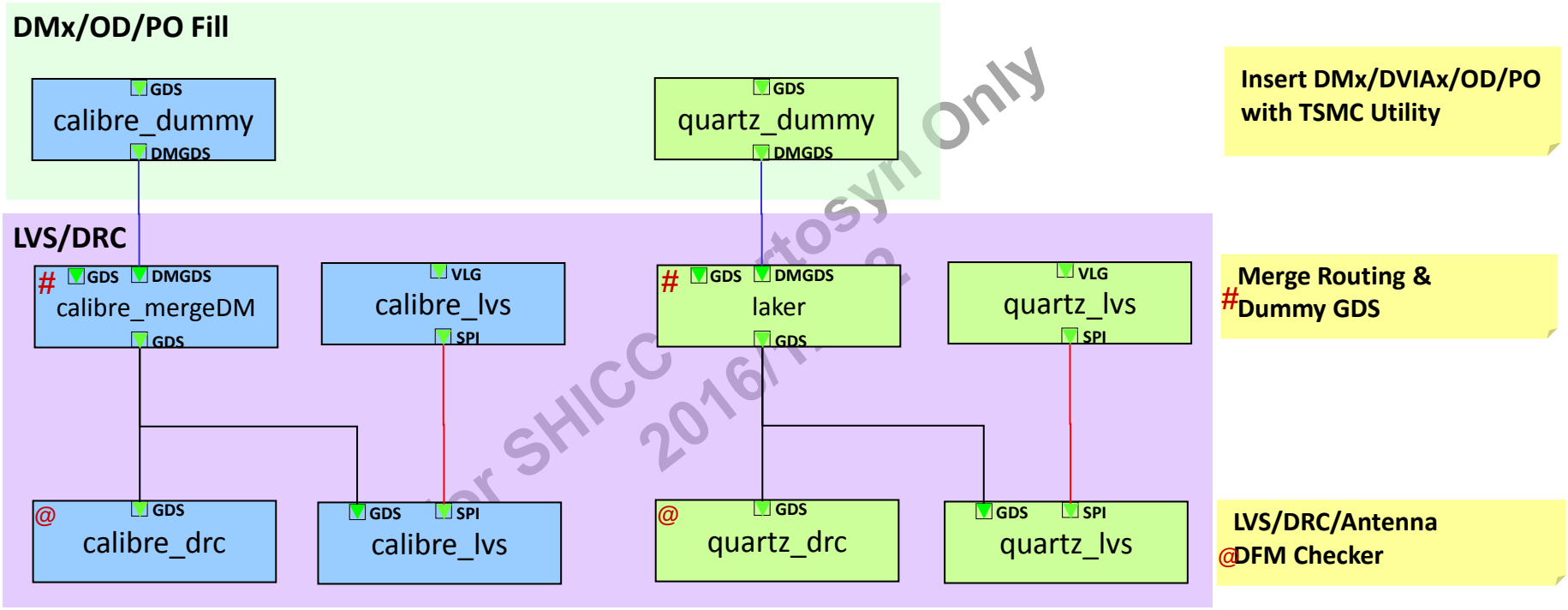


Delay Uncertainty Analysis

- Calculates the change in delay due to coupling noise acting both with and against a transitioning signal
  - Outputs a delay uncertainty report
- Outputs incremental SDF for impacted nets
  - Back-annotated incremental SDF to PrimeTime
  - For example, PrimeTime + ETS_SI for noise timing closure



DMx/DVIAx/OD/PO Fill & Physical Verification



Summary

- 28nm Design Flow Overview
- Specific Guideline in 28nm
  - LDE, DFM, CTS
- Timing Sign-off Recommendations of Corner Selections and OCV Ratio
- Power Sign-Offf & Signal Integrity Recommendations