Selecting the Optimum PCI Express Clock Source

PCI Express (PCIe) is a serial point-to-point interconnect standard developed by the Peripheral Component Interconnect Special Interest Group (PCI-SIG). Although originally designed for desktop personal computers, the PCIe standard has been widely adopted in a broad range of applications including blade servers, storage, embedded computing, and networking and communications. Not only is the PCIe interface supported by a wide base of commercially available devices, it is also becoming more readily available in FPGAs and SoCs, providing designers with flexible solutions for transferring data within their systems. One of the key advantages of using PCIe is its scalable data bandwidth and flexible clocking solutions. Let's explore some of the standard clocking architectures for PCIe and consider their benefits for typical system applications.

The PCIe Link

Before considering clocking architectures, let's examine a PCIe data link. It consists of one or more lanes that provide a transmit (Tx) and receive (Rx) differential pair. Figure 1 shows two devices that need to transfer data. One of the key advantages of PCIe is its bandwidth scalability enabling up to 32 lanes to be configured on a single link. With the recent introduction of PCIe 3.0, each lane can accommodate 8 Gbits per second (Gbps) per direction for a maximum data throughput of 64 Gbps of data transfer. Applications that need less data bandwidth can simply be configured with fewer lanes. Previous PCIe 1.1 and 2.1 standards offer 2.5 Gbps and 5.0 Gbps per lane respectively. Choosing a PCIe standard with higher data rates ultimately means using less lanes or connection wires between devices, but it also places additional requirements on the clocking performance. We will examine these requirements in the following sections.

	Nominal Bit Rate	Data Throughput Per Lane	Max Data Throughput (32 Lanes)	Year Released
PCIe 1.1	2.5 Gbits/s	500 MBytes/s	16 GBytes/s	2003
PCIe 2.1	5.0 Gbits/s	1.0 GBytes/s	32 GBytes/s	2007
PCIe 3.0	8.0 Gbits/s	2.0 GBytes/s	64 GBytes/s	2010

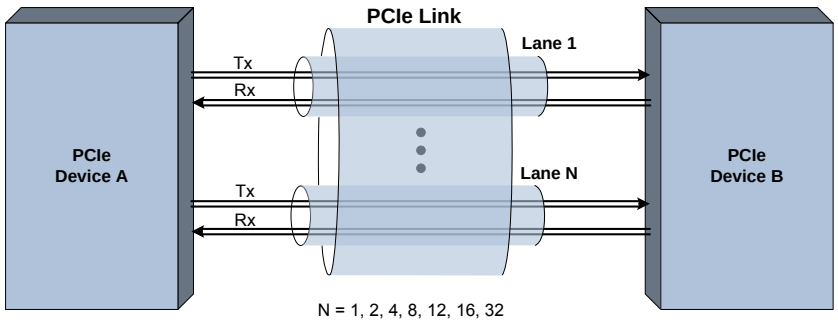


Figure 1. The PCI Express Link

PCIe Applications

Because of the popularity of PCIe, growing numbers of application-specific devices (e.g., ASICs and SoCs) are adopting the PCIe interface as a common interconnect with other devices that are readily available on the market. Even today's field-programmable grid arrays (FPGAs) offer built-in PCIe protocol stacks and physical layer interfaces to help simplify system-level design. Figure 2 illustrates a few examples of system-level solutions using PCIe interconnects. It is important to note that reliable data transmission over a PCIe link requires a stable clock reference at both the transmitting and receiving ends.

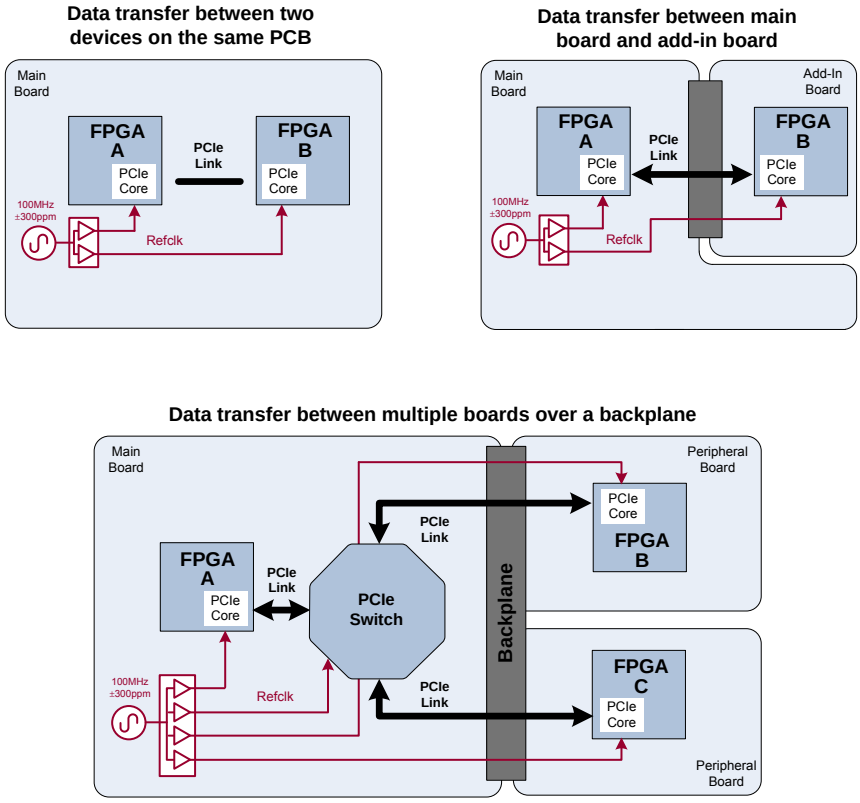


Figure 2. System Applications of PCIe Interconnects

PCIe Clocking Architectures

The PCIe standard specifies a 100 MHz clock (Refclk) with greater than ±300 ppm frequency stability at both the transmitting and receiving devices. It also specifies support for three distinct clocking architectures: *Common Refclk*, *Separate Refclk* and *Data Clocked Refclk*. Figure 3 shows a block diagram of each architecture. Of the three, the *Common Refclk* architecture is the most widely supported clocking method used by commercially available devices. An advantage of this clocking architecture is that it supports spread spectrum clocking (SSC) which can be very useful in reducing electromagnetic interference (EMI). A disadvantage is that the same clock source must be distributed to every PCIe device while keeping the clock-to-clock skew to less than 12 ns between devices. This can be a challenge for large circuit boards or when crossing over a backplane connector to another circuit board. Examples of applications using the Common Refclk architecture are also shown in Figure 2.

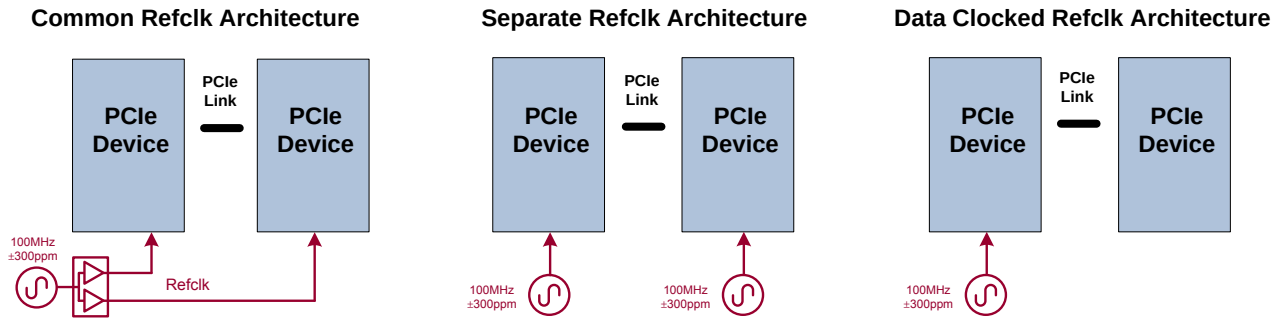


Figure 3. PCIe Clocking Architectures

An alternative is to use the *Separate Refclk architecture* where a different clock source is used at each end of the PCIe link. Both clock sources can still have a frequency accuracy of ±300 ppm since the PCI Express standard allows for a total frequency deviation of 600 ppm between the transmitter and receiver, but it leaves no extra frequency margin for enabling spread spectrum clocking. The advantage of this architecture is that tightly-controlled clock distribution is no longer required over connectors and backplanes. The *Data Clocked Refclk* architecture is the simplest to implement since it only requires one clock source located at the transmitter. In this case, the receiver simply extracts the embedded clock from the transmitter. The data clocked architecture was introduced when the PCIe 2.0 standard was released in 2007, so it is still a relatively new clocking scheme with fewer commercially available devices that support it.

Refclk Frequency and Jitter Requirements

The industry-standard reference clock frequency used for devices supporting PCIe 1.1, 2.1 and 3.0 is 100 MHz (±300 ppm generated using an HCSL signal format). It is common for embedded processors, system controllers and SoC-based designs to use 100 MHz HCSL format as the reference clock for the PCIe bus interface circuitry.

However, in applications that use FPGAs, the PCIe reference clock requirements can deviate from the standard 100 MHz HCSL format to other frequencies and formats such as 125 MHz, 200 MHz or 250 MHz in LVCMOS, LVDS or LVPECL. A typical example is an FPGA that supports both PCIe and Ethernet functions. Using a common reference clock frequency of 125 MHz to clock both functions helps to reduce clocking domains or timing islands in the FPGA. Internally the FPGA multiplies this reference to the required PCIe lane rate (e.g. 125 MHz x64 for PCIe 3.0). Depending on the mix of ICs used in a design, the PCIe clock strategy may vary from one of generating multiple 100 MHz HCSL clocks to generating a mix of different frequencies and output formats.

The jitter performance of the reference clock is also an important consideration. While the higher data throughput of PCIe 3.0 is intended to reduce the number of interconnect wires between two devices, it also requires a higher performance reference clock. Clock sources that meet the jitter requirements of PCIe 1.1 and 2.1 may not meet the needs of a device that supports PCIe 3.0. Table 1 summarizes the jitter requirements for all PCI Express standards. For a detailed discussion on clock source or Refclk jitter requirements for each of the PCIe standards, refer to application note AN562 available from www.silabs.com/timing.

Table 1. PCIe Clocking Architectures

	Description	Symbol	Limit	Units
Common Refclk Architecture				
PCIe 1.1	Random Jitter	Rj	4.7	ps pk-pk
	Deterministic Jitter	Dj	41.9	ps pk-pk
	Total Jitter Where Tj = Dj + 14.069 x Rj (for BER 10^{-12})	Tj	108	ps pk-pk
PCIe 2.1	High Frequency RMS Jitter Measured from 1.5 MHz to Nyquist (or $f_{REFCLK/2}$)	J_{RMS-HF}	3.1	ps RMS
	Low Frequency RMS Jitter Measured from 10 kHz to 1.5 MHz	J_{RMS-LF}	3.0	ps RMS
PCIe 3.0	Random Jitter	J_{RMS}	1.0	ps RMS
Data Clocked Refclk Architecture				
PCIe 1.1	Not defined in PCIe standards			
PCIe 2.1	High Frequency RMS Jitter Measured from 1.5 MHz to Nyquist (or $f_{REFCLK/2}$)	J_{RMS-HF}	4.0	ps RMS
	Low Frequency RMS Jitter Measured from 10 kHz to 1.5 MHz	J_{RMS-LF}	7.5	ps RMS
PCIe 3.0	Random Jitter	J_{RMS}	1.0	ps RMS
Separate Refclk Architecture				
PCIe 1.1	Device dependent. Not defined in PCIe standards.			
PCIe 2.1				
PCIe 3.0				

Spread Spectrum Clocking (SSC)

The use of spread spectrum clocking is also an important consideration when selecting a PCIe clock source since it is an effective method of lowering the amount of radiated electromagnetic interference (EMI) that is generated from high speed clock and datapath signals. Spread spectrum clocks use low frequency modulation of the carrier frequency to spread out the radiated energy across a broader range of frequencies. Radiation from data lines transmitted with a device using a spread spectrum clock reference will also benefit from the same EMI reduction. PCIe devices are specified to reliably transmit data when using a Refclk with a spread spectrum modulation rate of 30 to 33 kHz and modulation amplitude of 0 to -0.5%. Because each PCIe device must transmit within a bit rate of ±300 ppm of each other, the same Refclk must be supplied to both devices if SSC is enabled. Therefore Separate Clocking Architecture is not recommended when SSC is required unless both clocks are synchronized to a common source. System level shielding may be required to meet EMI compliance standards when SSC is disabled.

Choosing the Optimum PCIe Clock Source

As we have seen, several factors should be considered when choosing the optimal PCIe clock source. Ideally, the clock should support features that provide performance good enough to meet all PCIe data rates, spread spectrum clocking and adjustable output-output skew. Standard off-the-shelf PCIe clock devices with 100 MHz HCSL format typically can address a majority of PCIe applications. In some cases, flexible output frequencies and flexible output signal formats are required. Single clock oscillators and buffers have traditionally been used for simple PCIe clocking applications, but frequency and format-flexible clock generators are now becoming widely used in complex timing applications requiring reference clock generation of different frequencies and output formats such as LVDS and LVPECL.

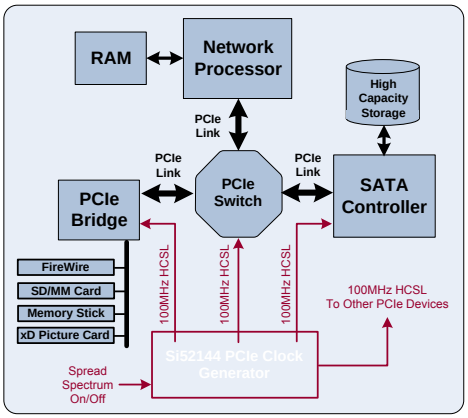
Figure 4 shows two PCIe clocking solutions. One uses Silicon Labs' Si52144 clock generator as a single-chip PCIe clock tree solution. This clock generator is ideal for off-the-shelf PCIe devices that require standard 100 MHz HCSL clocks. The clock generator also provides an additional pin-controlled spread spectrum feature for easy SSC on/off access during electromagnetic interference (EMI) compliance testing.

Another solution using Silicon Labs' web-customizable Si5335 clock generator provides greater flexibility often required with FPGA or custom ASIC and SoC designs. In addition to generating clocks other than the standard 100 MHz HCSL format, it provides output-to-output skew adjustments to compensate for large differences in PCB trace lengths and supports spread spectrum on a per output basis, enabling developers to target EMI reduction in areas of the board that need it the most. Providing this functionality in a single clock generator device simplifies system design and reduces the component count and bill of materials cost. This flexibility also enables developers to make changes when prototyping in the lab and helps guarantee a successful first-pass design.

Si5214x and Si5315x PCI Express HCSL Clock Generators& Buffers

- High clock density – 2 to 9 output HCSL outputs
- PCIe 2.1 and PCIe 3.0 compliant
- Integrated output clock terminations
- Up to 50% lower power than competing solutions
- Dedicated output enable pins
- Pin selectable Spread Spectrum

Pre-Configured Fixed Frequency PCIe Clock Solution



Si5335 Low Jitter HCSL/LVDS/LVPECL Clock Generator

- Four differential outputs up to 350 MHz
- Low phase jitter: <1 ps RMS (12kHz – 20MHz)
- 70% lower jitter than PCIe 3.0 requirements
- Any signal format on any output: HCSL, LVDS, LVPECL, LVCMOS
- Flexible PCIe compliant SSC on any output
- Web customizable: frequency, signal format, spread spectrum, output delay

Flexible PCIe Clock Solution Using Web-Customizable Clock Generator

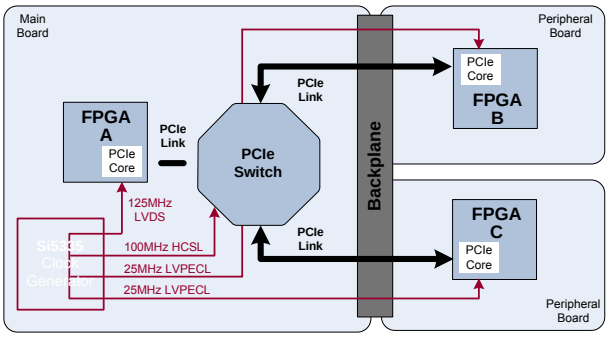


Figure 4. PCI Express Clock Generation Solutions

Summary

To ensure proper compliance with the PCIe standard, systems that use the PCIe interface require careful attention to the timing subsystem and architecture. Designers must consider which of the three PCIe specified reference clock architectures – common, separate or data clocked – will meet their application's functional and performance goals. Due to the diversity of ICs such as FPGAs, processors and switches that integrate PCIe cores, developers may want to use timing solutions that support multiple I/O voltage and formats, as well as spread spectrum clocking technology. Silicon Labs provides single and dual output clock oscillators, buffers and a wide portfolio of frequency programmable, multi-output clock generators that meet the requirements of today's most demanding PCIe 3.0/2.1 and 1.1 applications.

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