N28HPC Sign-off Methodology and Recommendations

DFD/DMKD

Revision History

Date	Description
2014/04/08	First version
2014/04/17	Add 9T OCV and guideline of mixed 9T & 7T design
2014/05/21	Update the hold-uncertainty with N28HPC model Add mix-OCV/SBOCV guideline
2014/06/05	Redesigned methodology based on flattened blocks; reduced margin required for mixing blocks with cells of different track heights
2014/06/23	Revised FF corner derating with relaxed methodology Enforce derating also on hardened macro
2014/09/30	Revise OCV values based on OCV calculator Add description of OCV calculator Add description of Spatial variation Add description of SBOCV variation components Update hold-uncertainty of SBOCV flow Revise the margin method of 7T/9T interface Revise the demo-case of mix-corner

Revision History

Date	Description
2014/10/08	Revise the technology-migration ratio. Ori: 0.7(early) / 1.0(late). Update: 0.7(early) / 0.9(late)
2014/12/12	Revise recommend OCV values Revise SBOCV IR drop spec Add wire OCV Remove 7T/9T interface margin
2015/01/08	Revise description of OCV customization
2015/01/23	Revise description of wire SBOCV
2015/03/30	Revise description of OCV customization
2015/09/15	Revise the example at page 22 Remove mix block page
2015/09/25	Revise hold margin for U/HVT flops to eliminate characterization inaccuracies caused by flop's internal glitch

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N28HPC Sign-off Methodology Update

- **Use global corner for slow (SSG) and total corner for fast (FF)**
- **Recommend SBOCV-based sign-off to maximize timing gains**
  - **Flat OCV provided here for reference in APR and margin adjustments for mixed HPC/HPM sign-off**

Corner	Original	Update
Performance corner	Total corner SS+OCV or SS+SBOCV OCV: Fixed setup margin to cover shorter stage SBOCV: setup margin = clock jitter	Global corner SSG+OCV or SSG+SBOCV OCV: Fixed setup margin to cover shorter stage SBOCV: Setup margin = clock jitter
Hold corner	Faster corner hold: FF+OCV or FF+SBOCV Slower corner hold: SS+OCV or SS+SBOCV OCV: Fixed hold margin to cover shorter stage SBOCV: Hold constraint variation margin per PVT corner	Faster corner hold (same): FF+OCV or FF+SBOCV Slower corner hold : SSG+OCV or SSG+SBOCV OCV: Hold constraint variation margin per PVT corner SBOCV: Hold constraint variation margin per PVT corner

Default OCV Generation Assumptions

- PVT corner: SSG_0.81v_m40c & FF_0p99v_m40c
- Clock cell: CKND2BWP7T30P140 (7T)
- Max clock slew at SSG_0.81_m40C: 200ps
- Data cell: INVD1BWP7T30P140 (7T)
- Max data slew at SSG_0.81v_m40C: 350ps
- IR drop (VDD-VSS variation) : +/-2.5% for SSG, +/-5% for FF
- [NOTE!] Applying default OCV on looser design spec may cause design risk
  - EX: lower voltage corner, smaller cell, larger slew, larger IR drop
  - Please consult DFD for OCV customization support

N28HPC Chip Sign-Off Corners

Timing Check	Library PVT Conditions	RC Corner	OCV and Design Margin
Setup	SSG/0.81/125C	Cworst	(1a) SBOCV on launch+data /capture clock (1b) Clock jitter OR (2a) +3.9% on launch clock cell, +7.7% on data clock cell and -3.9% on capture cell (2b) -8.5% on capture net (2c) Clock jitter + 25ps setup margin
		Rcworst	
	SSG/0.81/-40C**	Cworst	
		Rcworst	
Hold	SSG/0.81/125C	Cworst	(1a) SBOCV on launch+data/capture clock (1b) Flop hold constraint variation margin OR (2a) -4.9% on launch clock cell, -12.7% on data cell and +4.9% on capture cell (2b) -8.5% on launch clock net, -8.5% on data net (2c) 70ps hold margin
		Rcworst	
	SSG/0.81/-40C**	Cworst	
		Rcworst	
	FF/0.99/125C	Cworst	(1a) SBOCV on capture clock (1b) Flop hold constraint variation margin per PVT OR (2a) +13.9% on capture cell (2b) -8.5% on launch clock net, -8.5% on data net (2c) 50ps hold margin
		Rcworst	
	FF/0.99/-40C**	Cworst	
		Rcworst	
	FF/0.99/125C	Cbest	(1a) SBOCV on capture clock (1b) Flop hold constraint variation margin per PVT OR (2a) +13.9% on capture cell (2b) +8.5% on capture net (2c) 50ps hold margin
		Rcbest	
	FF/0.99/-40C**	Cbest	
		Rcbest	

•Based on TSMC internal experiences on N28HPC 100a library & **v1.0_2p1 SPICE** model

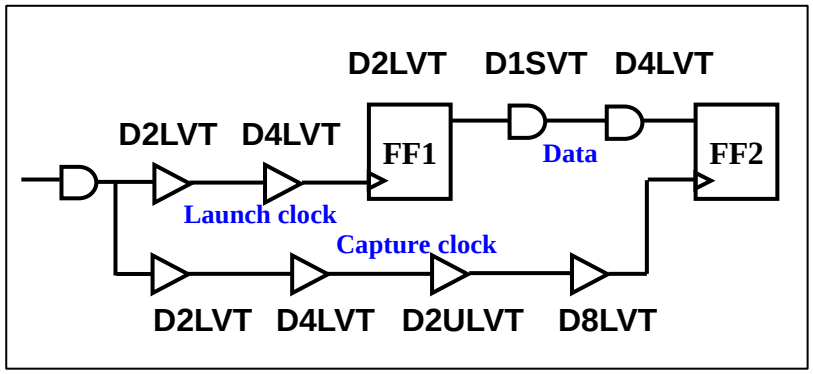
** Low temperature setting (like -40C, -25C, 0C, …) is design application dependent

OCV Customization

- **TSMC provide OCV customization for customer's design and sign-off conditions**
  - **Operating conditions: process, voltage, temperature, slew**
  - **Variation: IR-drop spec, process sigma**
  - **Cell library spec: size, Vth, gate length, track-height**
- **Advise design adjustments to control variation**
  - **Eg. use larger-size and lower-Vth cells to control the rise in OCV when operating at lower Vdd**

Always Use Conservative Design Spec in OCV Determination

- Cells with larger variation tend to dominate path variation → should use conservative design spec when determining OCVs
- Use conservative design spec in mixed cell usage
  - The following spec usually result in larger OCV value
    - Large slew, Large IR_drop, smaller driving strength, lower voltage, slower process, larger Vth
  - But multiple tests on different spec to check which one is more conservative is strongly encouraged

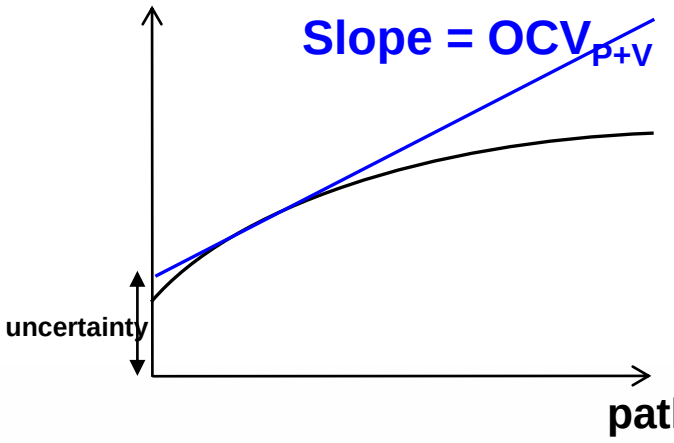


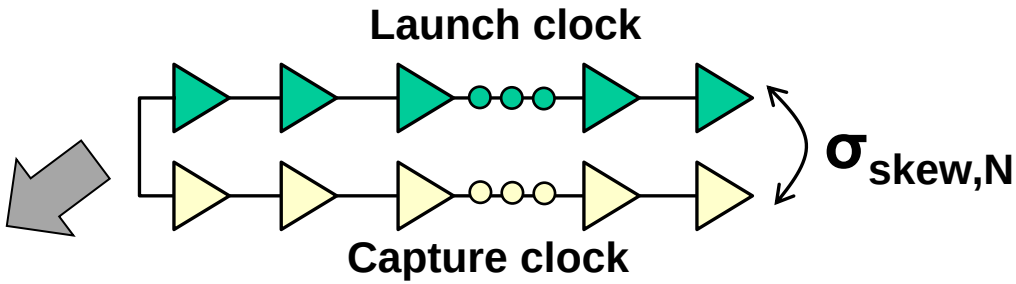
<Recommend spec>
Clock: D2 LVT
Data: D1 SVT

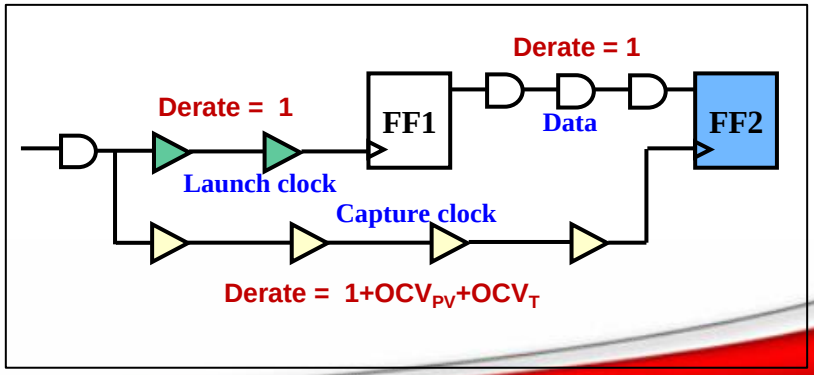
Flat OCV Methodology (FF Corner)

- $OCV = OCV_{P+V} + OCV_{temperature}$
  - $OCV_{temperature} = abs(1-delay_{-30C}/delay_{-40C})$
- $Delay_{capture}*OCV+clock\_uncertainty >= skew\ variation + flop\ variation$

path variation =
$3*(\sigma_{skew,p}^{2}+\sigma_{skew,v}^{2})^{1/2} +3*\sigma_{constraint}$

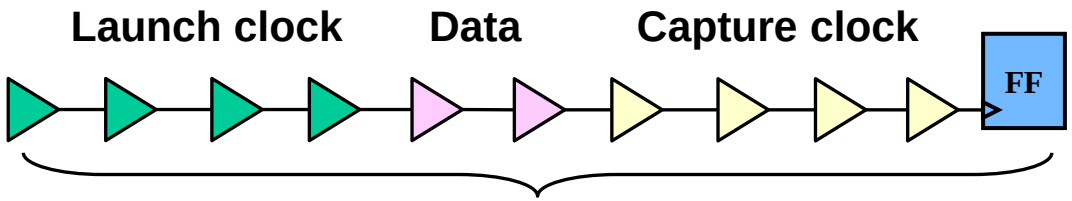






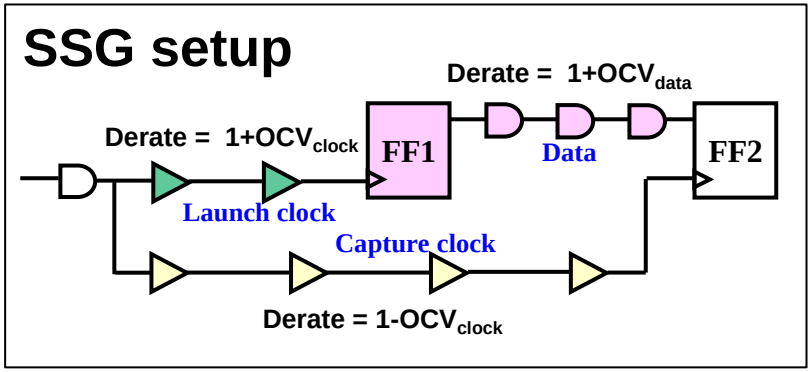
Flat OCV Methodology (SSG Corner)

- $delay_{capture}*OCV_{clock}+delay_{launch}*OCV_{clock}+delay_{data}*OCV_{data}+uncertainty >=$ Slack variation



Setup: $\sigma_{slack}= (\sigma_{launch}^2 +\sigma_{data}^2 +\sigma_{capture}^2)^{1/2}$

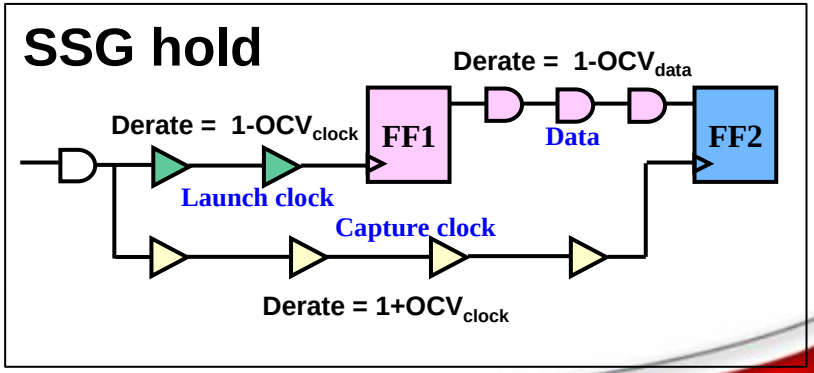
Hold: $\sigma_{slack}= (\sigma_{launch}^2 +\sigma_{data}^2 +\sigma_{capture}^2)^{1/2} +\sigma_{constraint}$



Math solver:

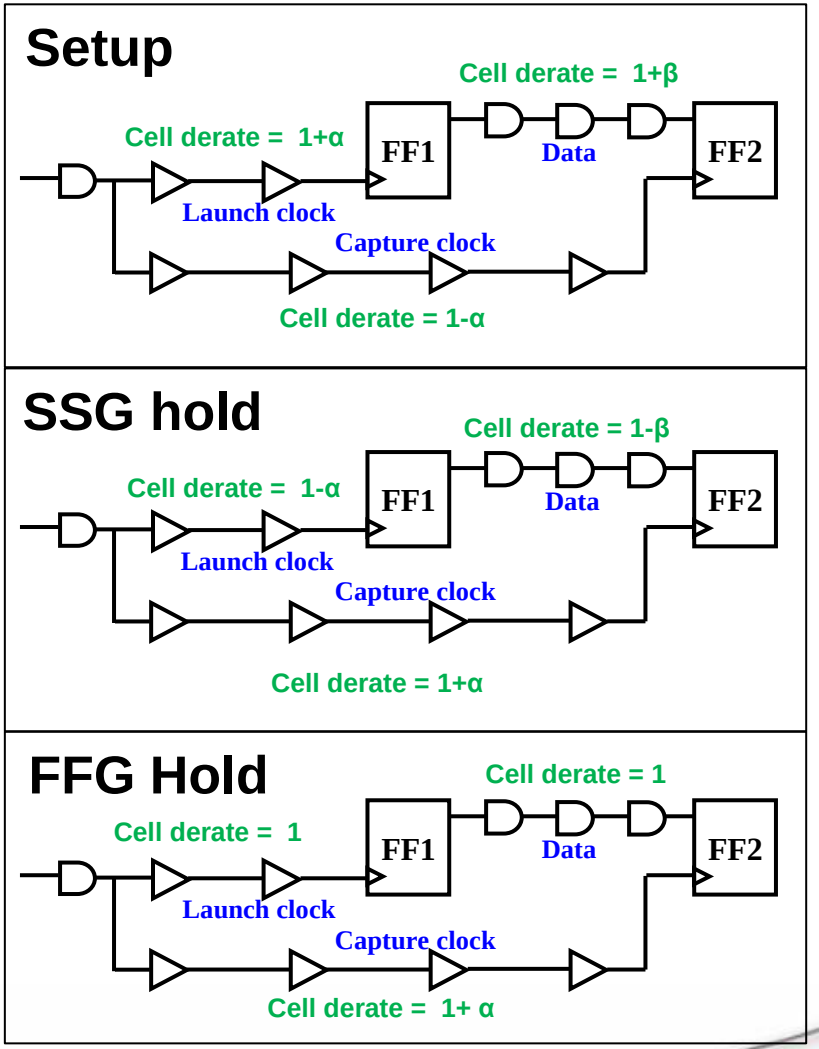
Find OCV_{clock} & OCV_{data}

s.t. $D_{capture}*OCV_{clock}+ D_{launch}*OCV_{clock}+ D_{data}*OCV_{data}+$ uncertainty $\geq 3*\sigma_{slack}$



Flat OCV Application

- Apply on both side because library delay is at average(global) delay
- OCV (fitted by global OCV method)
  - Setup (SSG)
    - [STA] set_timing_derate –late –cell –clock (1+α)
    - [STA] set_timing_derate –late –cell –data (1+β)
    - [STA] set_timing_derate –early –cell (1-α)
  - Hold (SSG)
    - [STA] set_timing_derate –early –cell –clock (1-α)
    - [STA] set_timing_derate –early –cell –data (1-β)
    - [STA] set_timing_derate –late –cell (1+α)
  - Hold (FF)
    - [STA] set_timing_derate –late –cell (1+α)

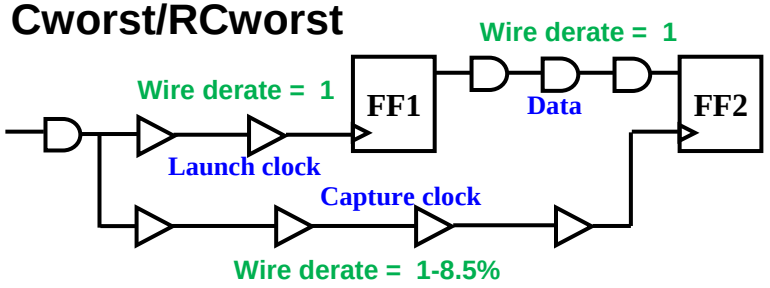


ps: α, β, γ ≧ 0, stand for clock/data OCV values

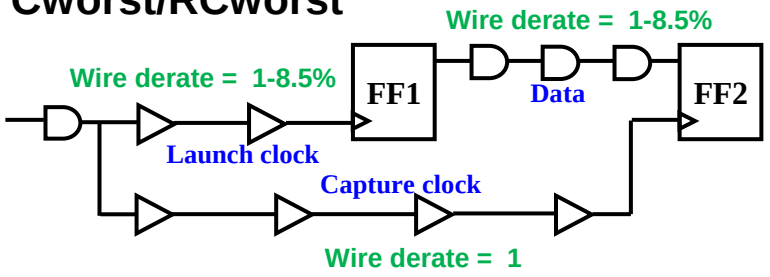
Wire OCV Application for Total-RC corner

- Apply wire OCV on one side because another side is already fastest/slowest
  - Setup (Cworst/RCworst)
    - [STA] set_timing_derate –late –net –clock 1
    - [STA] set_timing_derate –late –net –data 1
    - [STA] set_timing_derate –early –net (1-8.5%)
  - Hold (Cworst/RCworst)
    - [STA] set_timing_derate –early –net –clock (1-8.5%)
    - [STA] set_timing_derate –early –net –data (1-8.5%)
    - [STA] set_timing_derate –late –net 1
  - Hold (Cbest/RCbest)
    - [STA] set_timing_derate –early –net –clock 1
    - [STA] set_timing_derate –early –net –data 1
    - [STA] set_timing_derate –late –net (1+8.5%)

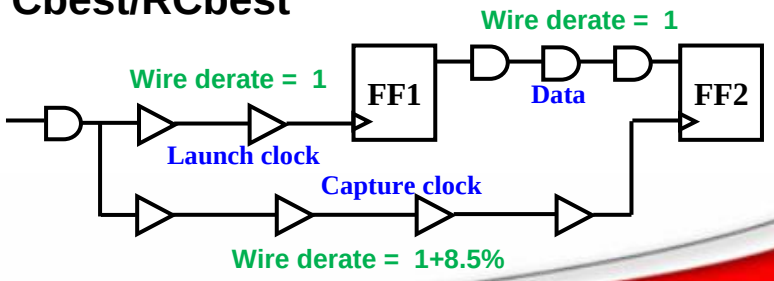
Setup for Cworst/RCworst



Hold for Cworst/RCworst

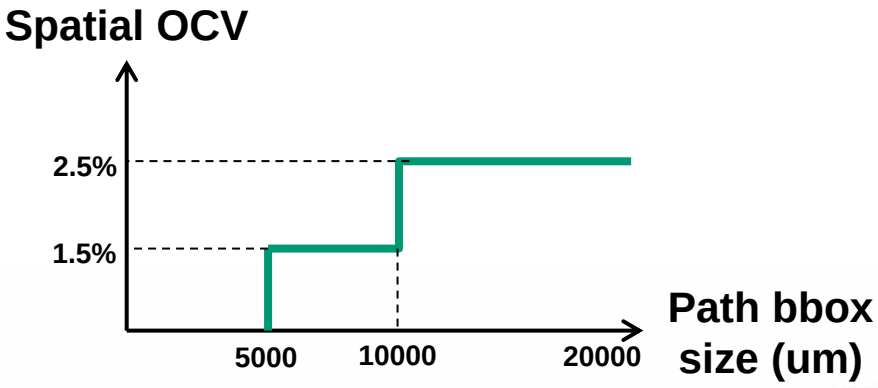


Hold for Cbest/RCbest



Spatial Variation Margin (if applicable)

- Spatial variation margin is added to flat-OCV or SBOCV when diagonal of bounding box encompass the timing path is larger than 5000um
  - SSG early: (OCV$_{early}$ or SBOCV) - ½*OCV$_{spatial}$
  - SSG late: (OCV$_{late}$ or SBOCV) + ½*OCV$_{spatial}$
  - FF late: (OCV$_{late}$ or SBOCV) + OCV$_{spatial}$
- EX: For a path contain all 9T cells in SSG corner, bbox diagonal = 6000um, in setup check
  - SSG capture clock derate = -3.9% - ½*1.5% = -4.65%
  - SSG launch clock derate = +3.9% + ½*1.5% = 4.65%
  - SSG data derate = 7.7% + ½*1.5% = 8.45%



SBOCV Signoff

SBOCV Variation Component

- **SBOCV should cover at least these independent sources**
  - **FEOL: delay variation by Monte Carlo simulation at global corner**
    - **TSMC apply additional LDE factor multiplied to FEOL variation to account for local layout variation**
  - **BEOL: delay variation from wire Res. & Cap. Variation**
    - **TSMC provide wire SBOCV table, please contact FTS**
  - **V: delay variation from VDD & VSS variation**
  - **T: delay variation due to temperature difference between launch/capture paths**
- **Customers/designers shall determine their margin for PVT**

TSMC's SBOCV	FEOL	BEOL	V	T
Margin assumption	3σ*LDE†	+/-3σ_R & -/+3σ_C	Slow corner: +/-2.5% Fast corner: +/-5%	10°C
Type	Random (Gaussian)	Flat	Random (Gaussian)	Flat
Applied in	Data, Clock	Data, Clock	Clock	Clock

† LDE factor is 1.18 for N28HPC

Wire SBOCV

- **TSMC provide 2 stand-alone wire SBOCV tables**
  - **N28_wire_worstrc.aocvm: Cworst & Rcworst**
  - **N28_wire_bestrc.aocvm: Cbest & Rcbest**
- **Read best-RC(worst-RC) wire SBOCV after reading all other tables when signoff under best-RC(worst-RC) corner to overwrite other wire SBOCVs in stdcell tables**

```
Example for worst-RC corner (Cworst & RCworst):
read_aocvm xxxxx.aocvm
read_aocvm xxxxx.aocvm
read_aocvm  ./N28_wire_worstrc.aocvm
…
update_timing
```

```
Example for best-RC corner (Cbest & RCbest)
read_aocvm xxxxx.aocvm
read_aocvm xxxxx.aocvm
read_aocvm  ./N28_wire_bestrc.aocvm
…
update_timing
```

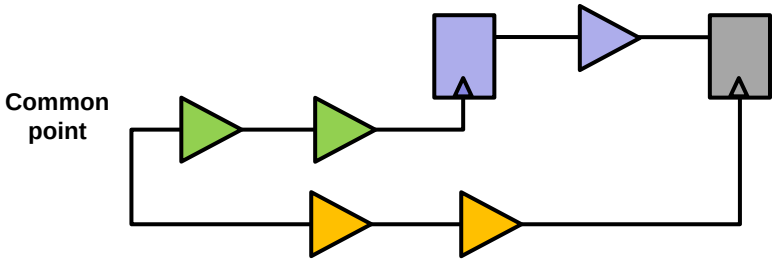
TSMC's SBOCV Deliverable

- TSMC provide 4 types of SBOCV tables based on different scenarios
- Clock_pvt_data_p is recommended for setup & hold analysis
  - Provide other 3 types for customer's specific purpose

POR SBOCV table type	Variation source in clock path	Variation source in data path
clock_p_data_p	P	P
clock_pvt_data_p	**P+V+T**	**P**
clock_pv_data_pv	P+V	P+V
clock_pvt_data_pv	P+V+T	P+V

Global SBOCV Method

- In global corner SBOCV, path slack variation is characterized by a single delay chain consist of capture, launch & data because they are statistically same
  - $\sigma(X-Y) = \sigma(X+Y) = \text{sqrt}(\sigma_X^2 + \sigma_Y^2)$
- Thus user need to lookup SBOCV by total stage of capture, launch & data
- Flat OCV is also generated by same concept

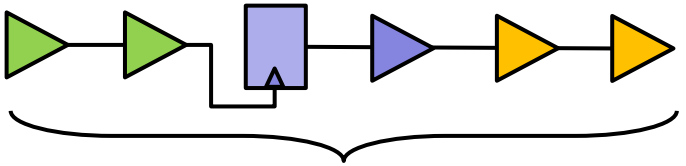


Slack = clk_period + capture – launch – data

σ_{slack} = σ(capture – launch – data)

= sqrt($\sigma_{capture}$^2 +σ_{launch}^2+σ_{data}^2)

Equal to



Delay = capture + launch + data

σ(capture + launch + data)

= sqrt($\sigma_{capture}$^2 +σ_{launch}^2+σ_{data}^2)

Derate = $3\sigma_{slack}/(\mu_{capture} + \mu_{launch} + \mu_{data})$

SBOCV Register Constraint Uncertainty

- **Setup time uncertainty**
  - **Margin = clock jitter**
- **Hold time uncertainty**
  - **Consider the process variation impact to capture flop**
  - **Margin = register constraint variation (D & SI uncertainty are separate in below table)**

N28HPC CP->D / CP-> SI hold uncertainty (ps)	9T ff0p99v	7T ff0p99v	9T ssg0p81v	7T ssg0p81v
Clk slew	<120ps		<200ps	
D & SI slew	<220ps		<350ps	
ULVT	17/25	24/25	36/53	53/54
LVT	17/26	25/26	41/57	56/58
SVT	19/28	27/28	43/64	60/65
HVT	23/31	31/32	48/90	77/91
UHVT	28/32	33/34	63/142	120/135

a. Based on simulation with TSMC 28HPC v1d0_2p1 SPICE model & 100a LPE netlist for 9T & 7T SDFQD1

b. Uncertainty is calculated by 3σ. σ is the constraint variation due to local-process variation.

c. Lower voltage corner & larger pin slew needs larger uncertainty to cover variation

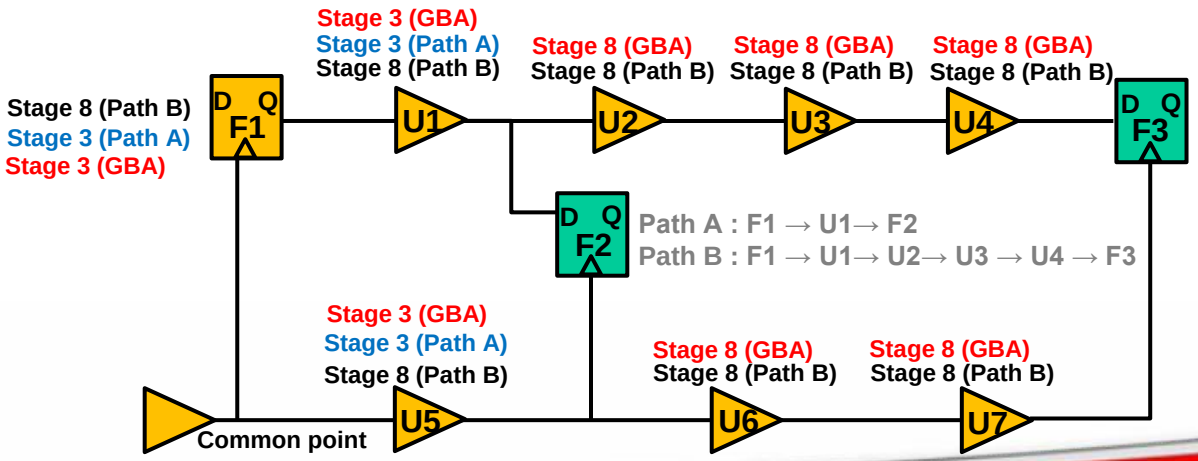
Hold-Constraint Uncertainty in STA

- **Hold uncertainty can be set by either way**
  1. **Insert into hold-constraint table of .lib (Please contact TSMC for the script)**
  2. **Use SDC command in tool**
     - **Ex:** ***set_clock_uncertainty -hold 0.051 [get_pins -of [get_cells -hier -filter "ref_name =~ *ULVT*"] -filter "is_clock_pin == true"]***
     - **Note!! Cell & pin based uncertainty will be overwritten by inter-clock uncertainty**

SBOCV STA Settings

	PrimeTime (v13.12-SP3-1 or after)	Tempus (14.1 or after)
Enable SBOCV analysis	set timing_aocvm_enable_analysis true	set_analysis_mode -aocv true -analysisType onChipVariation -cppr both
Stage counting mode for SSG	set timing_aocvm_analysis_mode combined_launch_capture_depth	set_global timing_aocv_analysis_mode combine_launch_capture
Stage counting mode for FF	set timing_aocvm_analysis_mode separate_data_clock_metrics	set_global timing_aocv_analysis_mode separate_data_clock
PBA timing report	report_timing -pba_mode path	report_timing –retime aocv_path_slew_propagation

- **Must use PBA reporting for SBOCV derate**
  - **Using GBA in report_timing will result in very pessimistic derating due to GBA's worst-case stage counting**



PBA vs GBA stage counting on Path B (from F1 to F3)		
Inst	PBA	GBA
F1	8	3
U1	8	3
U2	8	8
U3	8	8
U4	8	8
U5	8	3
U6	8	8
U7	8	8

* Stage couting in this example is using combine_launch_capture mode

SBOCV ICC Setting

- **Command to analyze SBOCV in ICC**
  - ***set timing_aocvm_enable_analysis true***
  - ***set timing_aocvm_analysis_mode separate_data_and_clock_metrics****
  - ***read_aocvm <sbocv_file>***
  - ***set_fast_pba_analysis_options -num_endpoints 1000***
  - ***apply_fast_pba_analysis***
  - **Fast PBA supported after ICC 2013.03-SP4**

*There is currently no support for combined clock and data stage counting; timing may be pessimistic

SBOCV EDI Setting

- **Create "library set" with corresponding SBOCV table**
  - ***create_library_set -name LIB1 -timing {LIB1.lib} -aocv {LIB1.aocvm}***
- **Enable SBOCV analysis before optimization**
  - ***setAnalysisMode –aocv true***
  - ***set_global timing_aocv_analysis_mode separate_data_clock****
  - ***set_global timing_enable_aocv_slack_based true***
  - ***set_global timing_aocv_slack_threshold 0.0***
  - **Slack-based AOCV supported after EDI 13.20–b060**

*There is currently no support for combined clock and data stage counting; timing may be pessimistic