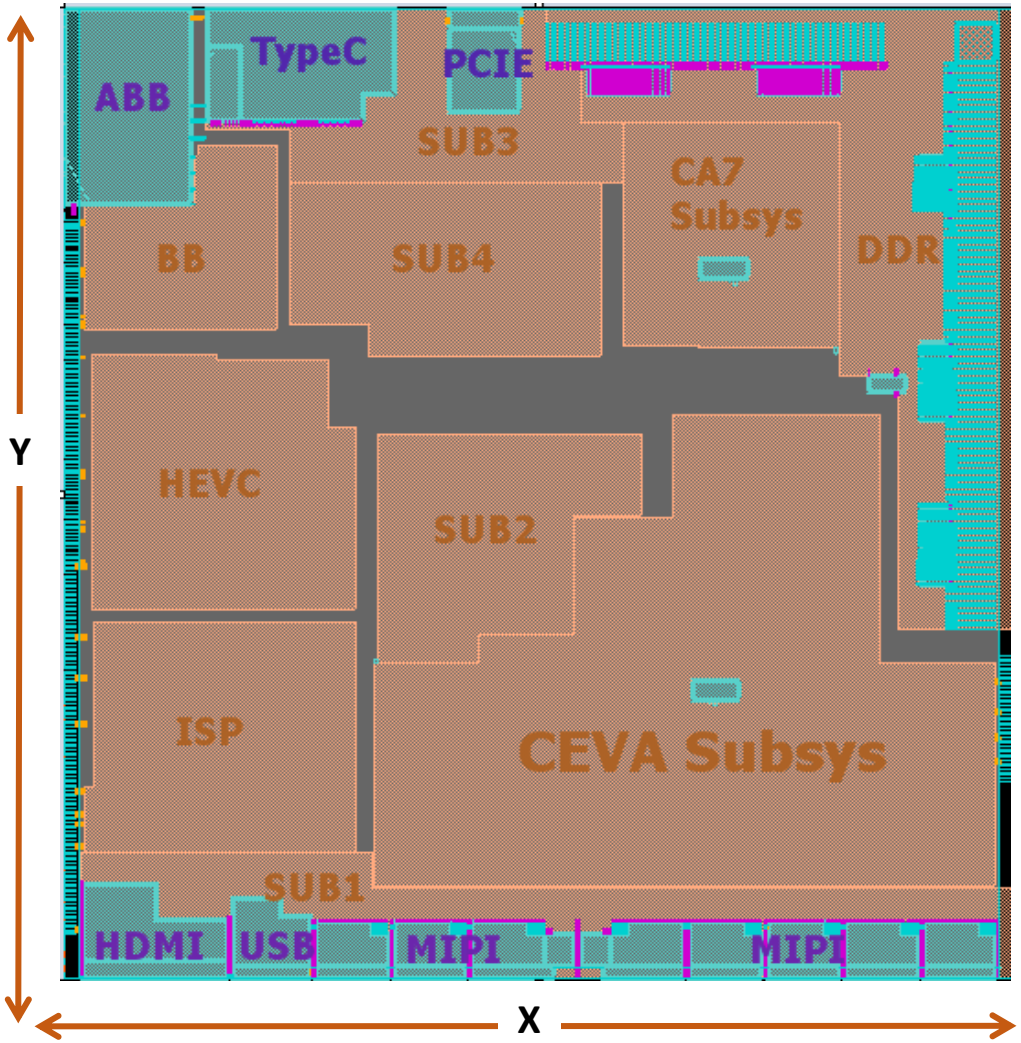
Artosyn Sirius Tapeout Review

Oct 17th, 2017

VeriSilicon Microelectronics (Shanghai) Co., Ltd.

Design Overview



▲ Process: TSMC 28HPC 1P8M+UT-ALRDL_5X2Z

drawn size	X[um]	Y[um]
Chip size (w S.Ring)	?	?
Layout size (W/O S.R)	9450	10000
silicon size	**X[um]**	**Y[um]**
Chip size (w S.R.)	?	?
Layout size (W/O S.R)	8505	9000

#	partitions	Track	Low Power Feature
1	ceva subsys	7T	
2	ceva harden	12T	OD
3	ceva core	12T	OD + Shut Down
4	ca7 subsys	7T	
5	ca7 harden	12T	OD
6	ca7 core	12T	OD + Shut Down
7	DDR	9T	
8	HEVC	7T	Shut Down + Always-on
9	ISP	7T	Shut Down + Always-on
10	BaseBand	7T	
11	SUB1	7T	
12	SUB2	7T	
13	SUB3	7T	
14	SUB4	7T	
15	Top	7T	

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Power Consumption Estimation By Power Domain (TT85)

- TT@85℃
- Toggle rate: data 0.1, clock 1.5

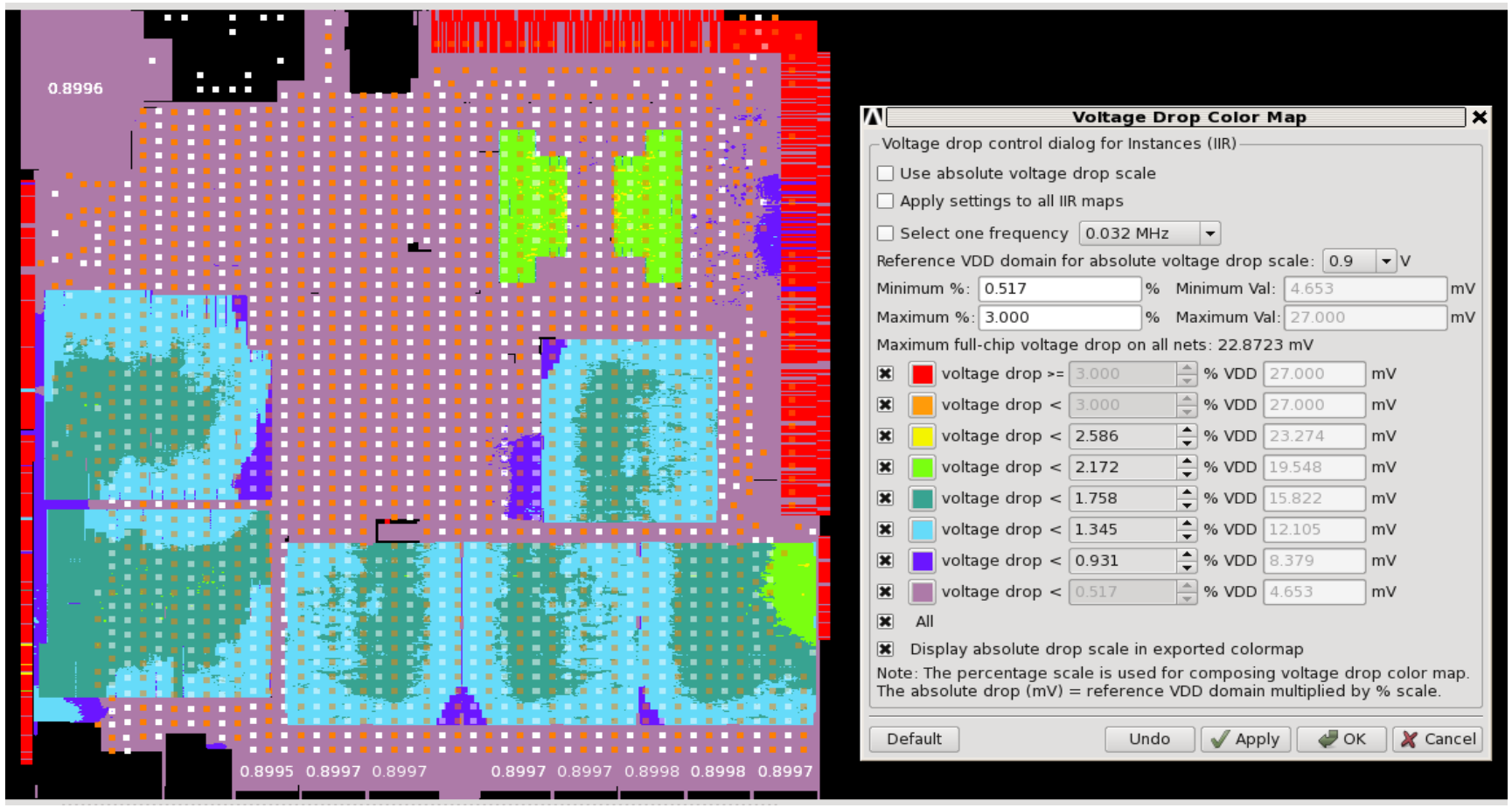
Vdd_domain	total_pwr	leakage_pwr	internal_pwr	switching_pwr	%_total_pwr	#inst_count
VDD (0.9V)	6.2774	0.26328	3.8077	2.2064	35.909	26171444
VDD_CEVA (0.9V)	0.45416	0.016112	0.35663	0.081415	2.598	10473261
VDD_CA7 (0.9V)	0.57422	0.034809	0.35977	0.17965	3.2848	1289492
VDD_HEVC_SW (0.9V)	1.6158	0.056163	0.93271	0.62694	9.2432	4690570
VDD_ISP_SW (0.9V)	1.3694	0.046206	0.83906	0.48418	7.8338	3119735
cortexa7core_0/VDD_CA7_SW (0.9V)	0.30843	0.023901	0.18818	0.096351	1.7643	232849
cortexa7core_1/VDD_CA7_SW (0.9V)	0.30782	0.023901	0.18817	0.095744	1.7608	232849
cortexa7core_2/VDD_CA7_SW (0.9V)	0.30781	0.023901	0.18817	0.095736	1.7608	232849
cortexa7core_3/VDD_CA7_SW (0.9V)	0.30788	0.023901	0.18817	0.095805	1.7612	232849
cevaxm4_core_0/VDD_CEVA_SW (0.9V)	1.4105	0.075091	0.67427	0.66113	8.0686	2510392
cevaxm4_core_1/VDD_CEVA_SW (0.9V)	1.4105	0.075091	0.67428	0.66113	8.0687	2510392
cevaxm4_core_2/VDD_CEVA_SW (0.9V)	1.4105	0.075091	0.67428	0.66113	8.0687	2510392
cevaxm4_core_3/VDD_CEVA_SW (0.9V)	1.4105	0.075091	0.67428	0.66113	8.0687	2510392

Power Consumption Estimation By Cell Type (TT85)

cell_type	total_pwr	leakage_pwr	internal_pwr	switching_pwr	%_total_pwr	#inst_count
combinational	7.5834	0.4395	1.9478	5.1961	43.692	23354007
latch_and_FF	5.9439	0.13332	5.3329	0.47775	34.246	3970390
memory	0.7812	0.18649	0.56646	0.028247	4.5008	1280
I/O	0.17772	0.00060987	0.14745	0.029657	1.0239	644
misc_seq	2.8701	0.046093	1.6755	1.1485	16.536	123991
decap	0.000341	0.000341	0	0	0.0019647	8596190
Total	17.357	0.80636	9.6702	6.8802	100	36046502

IR Drop

- IR drop simulation env: TT@85℃
- Toggle rate: data 0.1, clock 1.5
- Max Instance IR drop: 2.54%



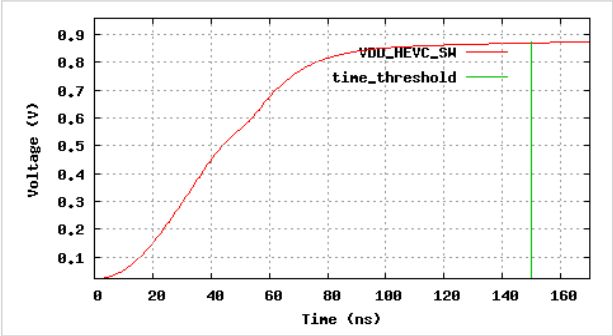
Power Ramp Up (HEVC, TT85)

- Peak Rampup Current: 475.962mA
- Worst Rampup time: 79.0ns

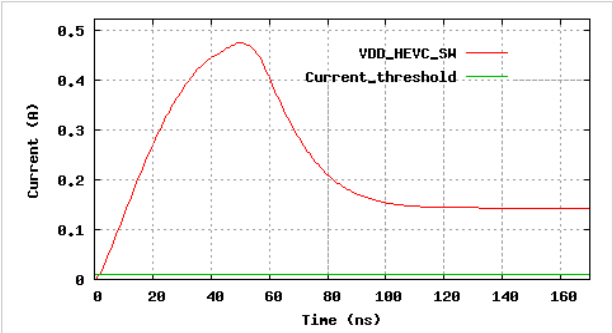
Low Power Analysis Summary

Summary | Waveforms | Switch Turnon Histogram

Worst ramp up/down switch

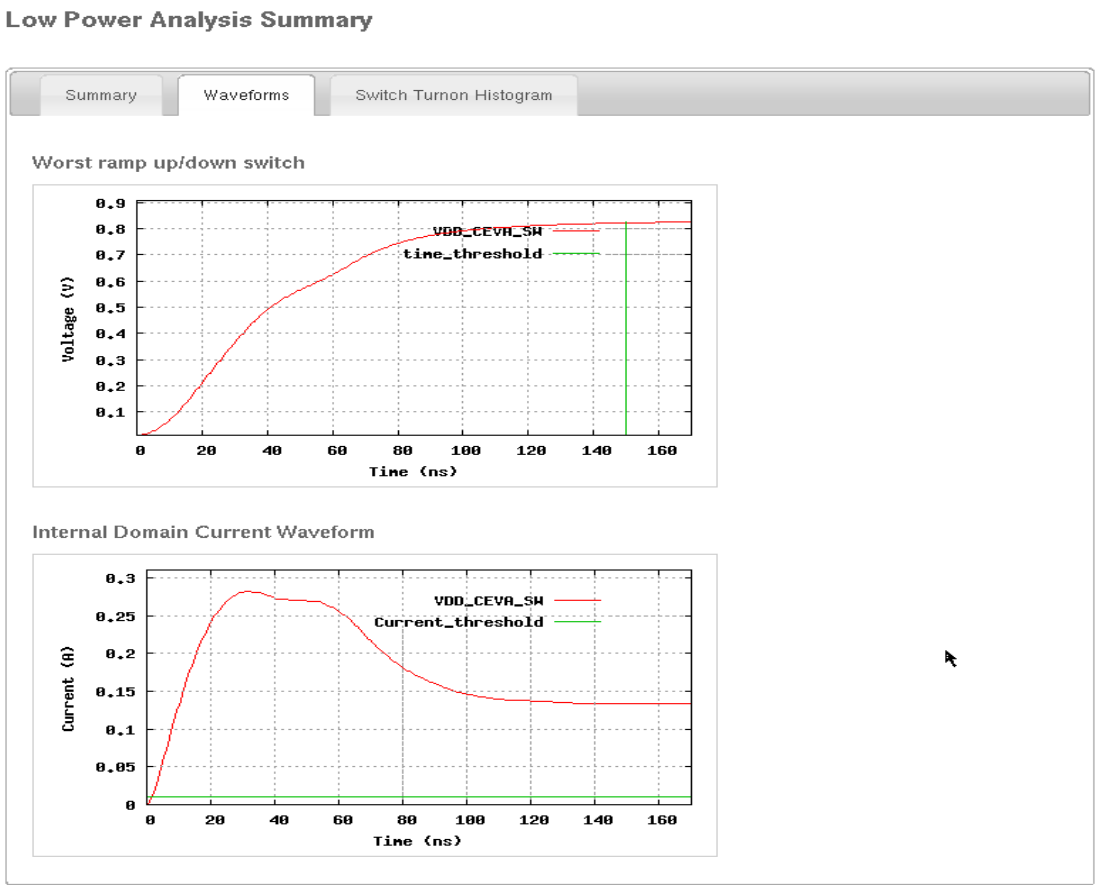


Internal Domain Current Waveform



Power Ramp Up (CEVA core, TT85)

- Peak Rampup Current: 281.933mA
- Worst Rampup time: 119ns



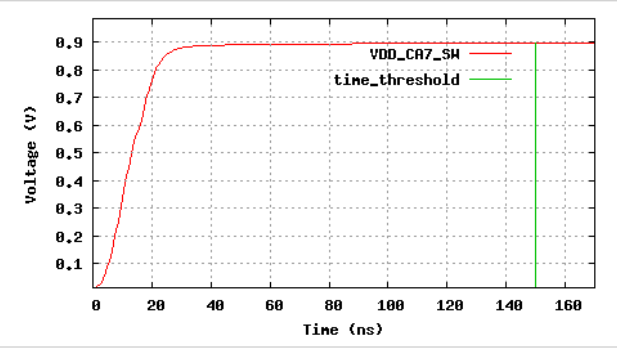
Power Ramp Up (CA7 core, TT85)

- Peak Rampup Current: 135.206mA
- Worst Rampup time: 22.0ns

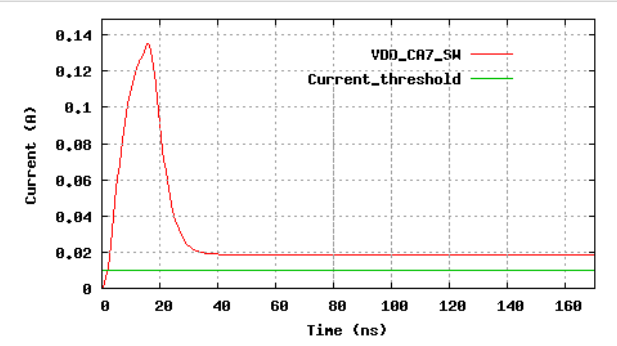
Low Power Analysis Summary

Summary | Waveforms | Switch Turnon Histogram

Worst ramp up/down switch



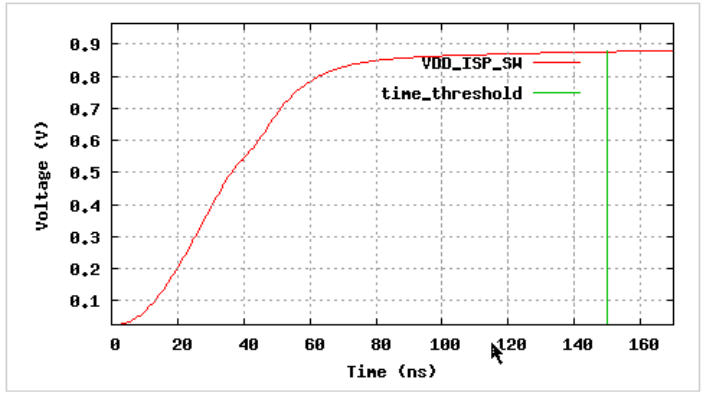
Internal Domain Current Waveform



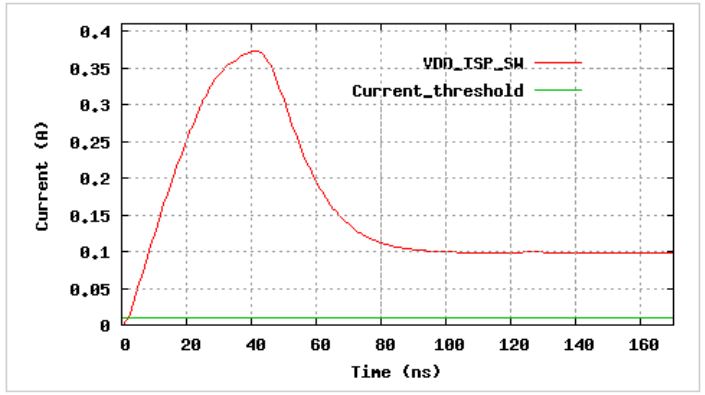
Power Ramp Up (ISP, TT85)

- Peak Rampup Current: 372.902mA
- Worst Rampup time: 65.0ns

Worst ramp up/down switch



Internal Domain Current Waveform



STD Inst Number by Library

partition	PTM	PTP	PVM	PVP	PVQ	SEF	SEG	SEJ	SEM	SEP	SEQ	STF	STG	STJ	STM	STP	STQ	SVF	SVG	SVJ	SVM	SVN	SVP	SVQ	Total
sirius_sub_3_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	409822	57076	255	28203	0	602546	17046	1114948
DDR_TOP_inst	0	0	0	0	0	707	426	147	732342	399441	144750	0	0	0	0	0	0	0	0	0	0	0	0	0	1277813
hevc_top_inst	0	0	25520	283	342	0	0	0	0	0	0	0	0	0	0	0	0	915122	249193	15310	235220	0	2559548	43788	4044326
sirius_sub_ca7_inst	5408	4736	0	4056	0	0	0	0	0	0	0	225097	156418	232	109010	595880	80905	101445	32960	2403	8766	0	178871	3961	1510148
sirius_sub_1_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	32028	7335	574	36568	205	846051	9565	932326
luxury_isp_top_inst	0	0	21011	181	320	0	0	0	0	0	0	0	0	0	0	0	0	338906	167073	0	117466	0	1877044	25957	2547958
sirius_sub_4_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	273674	95892	0	22661	0	436381	3264	831872
sirius_sub_2_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	706774	186325	110	63791	0	1220688	13383	2191071
sirius_asic_top_baseband_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	427764	85590	8	2572	0	811962	2878	1330774
sirius_sub_ceva_inst	45612	5829	0	2089	0	0	0	0	0	0	0	100331	727117	16595	458683	7508498	287021	6697	126145	594	84265	0	411500	11432	9792408
sirius_sub_top_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	55883	63665	757	159266	0	1475564	55962	1811097
full_chip	51020	10565	46531	6609	662	707	426	147	732342	399441	144750	325428	883535	16827	567693	8104378	367926	3269348	1071702	20086	759843	205	10461209	204449	27445829

STD Area by Library (unit: um^2)

partition	PTM	PTP	PVM	PVP	PVQ	SEF	SEG	SEJ	SEM	SEP	SEQ	STF	STG	STJ	STM	STP	STQ	SVF	SVG	SVJ	SVM	SVN	SVP	SVQ	Total
sirius_sub_3_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	227475.74	57143.31	161.504	14767.424	0	617217.33	22886.136	939651.44
DDR_TOP_inst	0	0	0	0	0	542.178	321.552	183.708	1159049.7	363343.05	234978.66	0	0	0	0	0	0	0	0	0	0	0	0	0	1758418.8
hevc_top_inst	0	0	65024.96	144.06	167.58	0	0	0	0	0	0	0	0	0	0	0	0	415540.78	137621.4	16726.738	299701.15	0	224587.6	38965.192	3219771.5
sirius_sub_ca7_inst	21805.056	7817.88	0	1197.364	0	0	0	0	0	0	0	162261.46	167420.23	294.672	152663.11	903825.89	170165.02	43206.534	29785.826	2653.84	5703.012	0	169786.86	3764.964	1842351.7
sirius_sub_1_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15012.424	4707.822	391.902	42898.912	1325.94	658852.63	9823.716	733013.34
luxury_isp_top_inst	0	0	53536.028	98.196	156.8	0	0	0	0	0	0	0	0	0	0	0	0	282746.37	142267.38	0	54510.246	0	1470164.9	32782.666	2036262.6
sirius_sub_4_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	143041.68	112506.94	0	14730.576	0	420297.6	3233.412	693810.21
sirius_sub_2_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	343316.25	109510.79	111.818	28680.484	0	1258699.3	17544.352	1757862.9
sirius_asic_top_baseband_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	207715.17	96297.152	5.978	4764.564	0	804108.52	2251.452	1115143.4
sirius_sub_ceva_inst	183907.58	9815.904	0	614.166	0	0	0	0	0	0	0	257497.13	870994.49	19138.392	876198.96	898494.3.9	463540.22	6695.458	185239.6	554.68	26054.378	0	304783.43	23718.156	1221369 6
sirius_sub_top_inst	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	23883.972	41787.396	631.218	48828.5	0	1391821.5	101700.58	1608653.1
full_chip	205712.764	17633.784	118560.996	2053.786	324.38	542.178	321.552	183.708	1159049.7	363343.05	234978.66	419758.58	1038414.7	19433.064	1028862.1	9888769.8	633705.24	1709076.1	917222.77	21273.154	540997.53	1325.94	9366526.3	275293.66	2796336 3

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DFM Via Rate

	block	M1	M2	M3	M4	M5
1	ceva subsys	43.04%	94.00%	93.58%	93.41%	93.72%
2	ceva harden	86.46%	91.46%	88.53%	88.90%	90.74%
3	ceva core	80.99%	81.23%	80.87%	78.92%	80.03%
4	ca7 subsys	25.10%	67.50%	73.00%	75.10%	79.10%
5	ca7 harden	91%	93.52%	91.48%	94.42%	93.61%
6	ca7 core	69.22%	96.73%	83.72%	80.39%	93.97%
7	DDR	28.11%	72.61%	73.41%	67.22%	64.12%
8	HEVC	27.20%	73.00%	79.00%	80.50%	80.50%
9	ISP	30.60%	72.70%	80.20%	83.50%	89.00%
10	BaseBand	27.90%	84.50%	91.20%	90.90%	90.40%
11	SUB1	33.20%	93.10%	97.40%	97.90%	97.50%
12	SUB2	33.80%	90.40%	96.50%	96.10%	96.30%
13	SUB3	32.60%	91.80%	97.70%	97.50%	96.70%
14	SUB4	26.60%	80.10%	87.70%	87.40%	90.90%
15	Top	50.10%	80.90%	84.80%	87.40%	90.70%

DRC Violation to be waived (CLN28HP_8M_5X2Z_002.17b.encrypt)

Check	Results	Comments
ESD.3g	4	HDMI(4)
ESD.6g	816	DDRIO(816)
ESD.7g	3	ABB(3)
ESD.18g	8	HDMI(8)
ESD.31g	4	USB IO (4)
ESD.52g	3	HDMI(3)
HIA.3g	91	TypeC(56);PCIe(21);USB(14)
HIA.4g	176	TypeC(176);
HIA.5g	320	TypeC(176); MIPI-IO(34*2);PCIe(76)
NW.S.2	5	OTP(5)
NW.S.3	9	OTP(9)
NW.S.4	61	OTP(61)
NW.S.3__NW.S.4:SUGGESTED	71	OTP(71)
PO.A.3	536	OTP(6)
PO.L.3	49	OTP(49)
PO.R.12	2	OTP(2)
PO.W.17	1092	OTP(1092)
PO.DN.3.1	1	Between DDR IO and core, Dummy exclude cover DDR-IO, can't add PO dummy at that area. Confirming with Artosyn/Synopsys
DIODMY_L:WARNING	1	Full chip(1), need Artosyn waive { @ Each low leakage concern diode must be covered by DIODMY_L.@ If there's no low leakage diode concern cell in the chip, the violation can be ignored.}
MFU.R.1	1	Full chip(1), need Artosyn waive {@ Mask Field Utilization (MFU) is a ratio of mask utilized region which is calculated by (multiple die area + scribe_line area) / (scanner maximum field area) >= 80%}
SRAM.WARN.1	1	Full chip(1), need Artosyn waive memory redundancy missing
Total	3255	

DRC Violation to be waived (CN28_LEADFREE_BUILD_UP_BUMP_8M_5X2Z.12a)

Checks	Results	Comments
PM.W.4	23	OTP(23)
PM.S.2	2	OTP(2)
PM.EN.2	23	OTP(23)
Total	48	

ERC Violation to be waived

Check	Results	Comments
floating.nxwell_float	4392 (11098)	ABB, TypeC, PCIE/PAD, DDRIO, HDMI/PAD, USB3/PAD, MIPI/PAD, pll_ddr, pll_arm, bjt_sensor, IO
floating.psub	987 (2220)	ABB, TypeC, USB3, MIPI/PAD, mipi_pll
mnpg	7339 (87967)	TypeC, PCIE_PAD, DDRIO, pll_arm, pll_ddr, HDMI_PAD, USB3_PAD, MIPI_ PAD, IO
npvss49	232 (20665)	ABB, TypeC, PCIE/PAD, DDRIO, pll_arm, pll_ddr, HDMI/PAD, USB3/PAD, MIPI/PAD, IO
npvss150	320 (396)	USB3
ppvdd150	16 (16)	USB3

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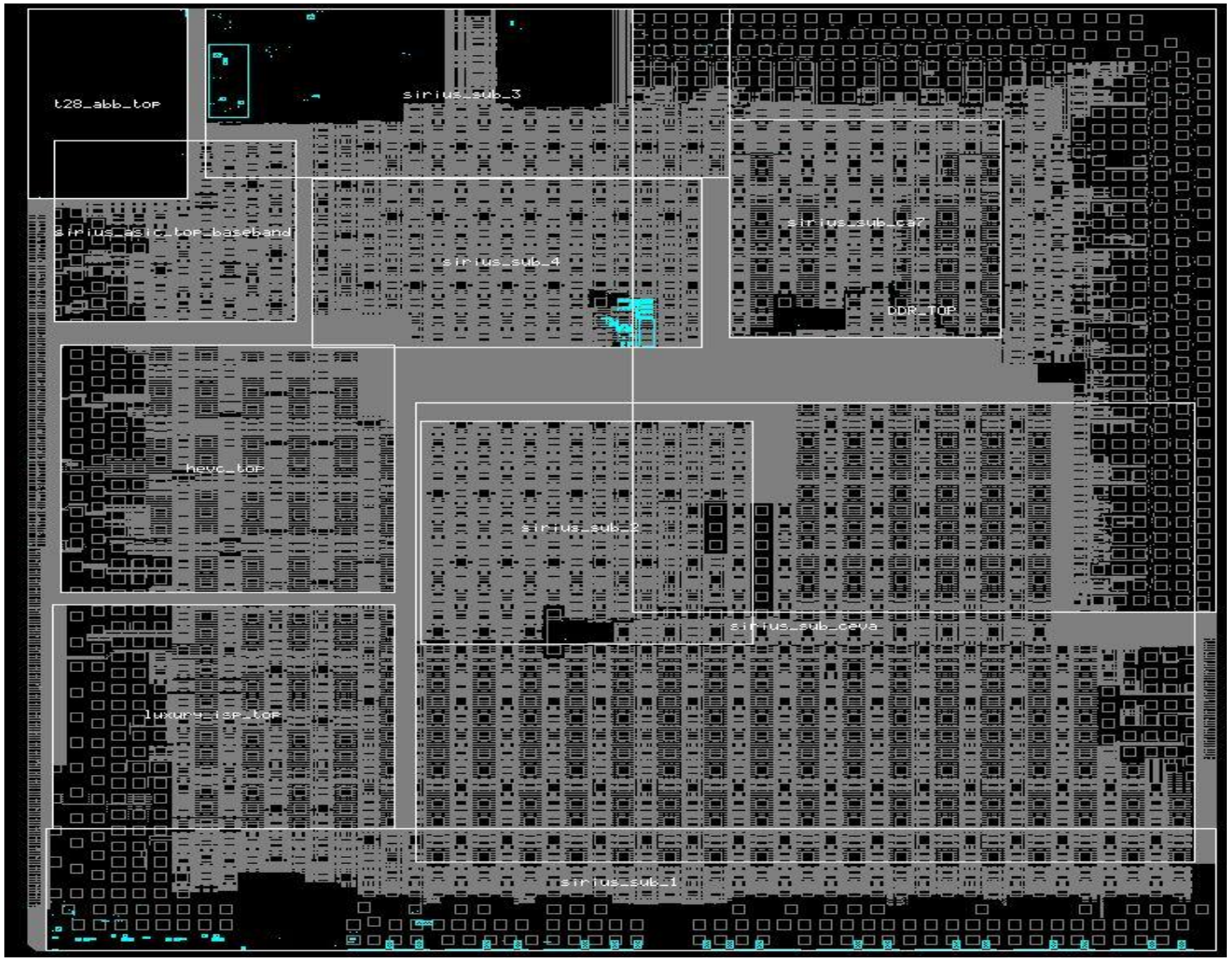
ERC : floating.nxwell_float



floating.nxwell_float

Cell / Check	Results
Cell sirius_top	13294
Check floating.nxwell_float	4392
Check floating.psub	987
Check mnpg	7339
Check mppg	8
Check npvss49	232
Check npvss150	320
Check ppvdd150	16

7348	7349	7350	7351
7369	7370	7371	7372
7390	7391	7392	7393
7411	7412	7413	7414
7432	7433	7434	7435
7453	7454	7455	7456
7474	7475	7476	7477
7495	7496	7497	7498
7516	7517	7518	7519

Rule File Pathname: tmp_rule
nxwell_float is not connected to POWER

sdtc01cap_t28hpc_4t2r_vf180_6020
sdtc01pdp_t28hpc_xx_vf180_6020
dwc_pcie2_x2_ns
dwc_pcie2_pads_x2_ns
dwc_hdmi_20_rx_1p_phy_ns
dwc_hdmi1rxio
dwc_usb3_sspx1_hspx1_ns
dwc_usb3_pads_sspx1_hspx1_ns
dwc_mipi_2_bidir_dphy_ns_core
dwc_dphy2sio
dwc_dphy2bio
t28_abb_top
pll_ddr_top
t28_pll_arm_top
t28_ts_bjt_sensor
DDRIO
IO

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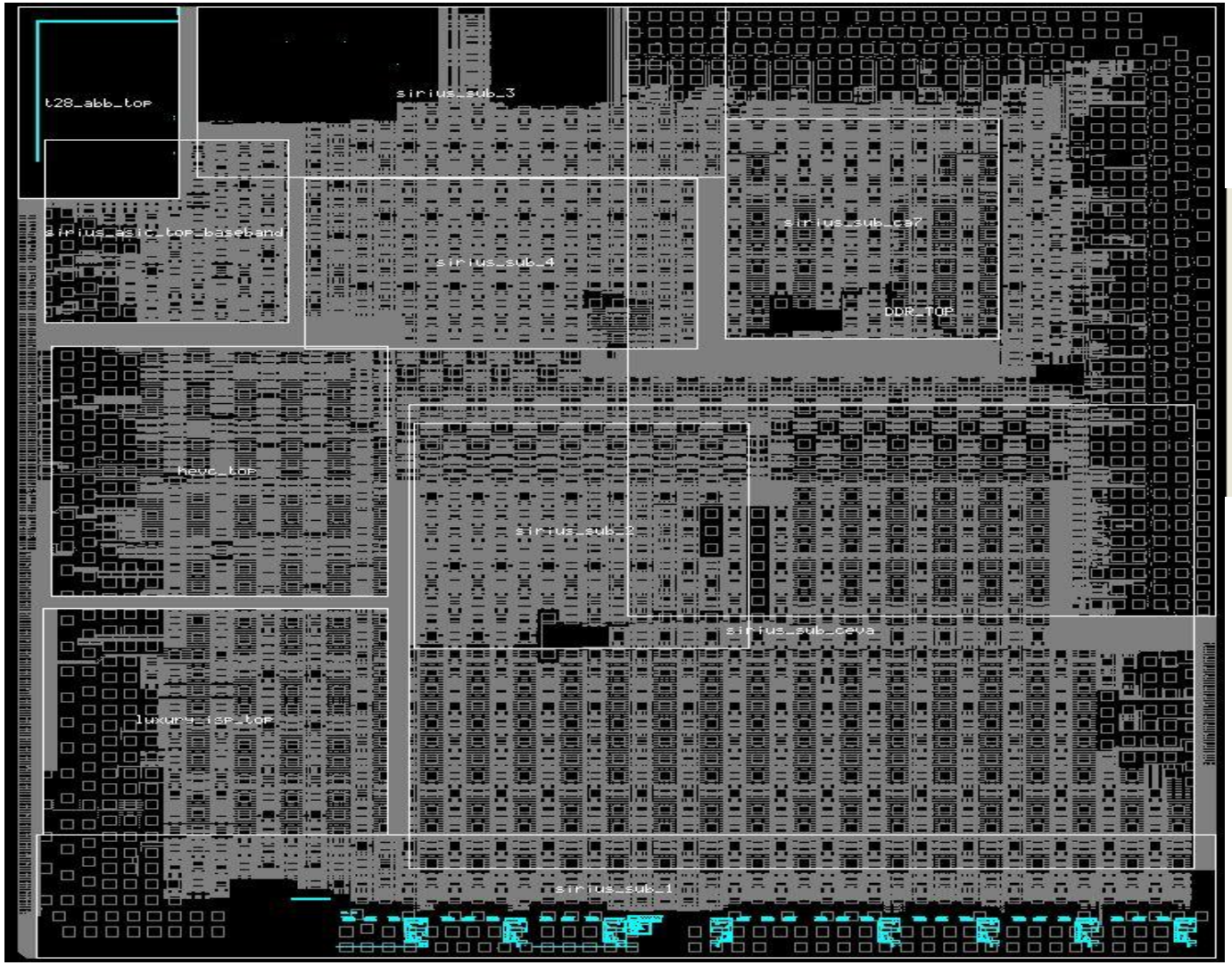
ERC floating.psub



floating.psub

Cell / Check	Results
Cell sirius_top	13294
Check floating.nxwell_float	4392
Check floating.psub	987
Check mnpg	7339
Check mppg	8
Check npvss49	232
Check npvss150	320
Check ppvdd150	16

11740	11741	11742	11743
11761	11762	11763	11764
11782	11783	11784	11785
11803	11804	11805	11806
11824	11825	11826	11827
11845	11846	11847	11848
11866	11867	11868	11869
11887	11888	11889	11890
11908	11909	11910	11911

```
Rule File Pathname: tmp_rule
psub is not connected to GROUND
```

t28_abb_top
sdtc01cap_t28hpc_4t2r_vf180_6020
dwc_usb3_sspx1_hspx1_ns
dwc_mipi_2_bidir_dphy_ns_core
dwc_dphy2sio
dwc_dphy2bio:
dwc_mipi_pll_dphy_ns

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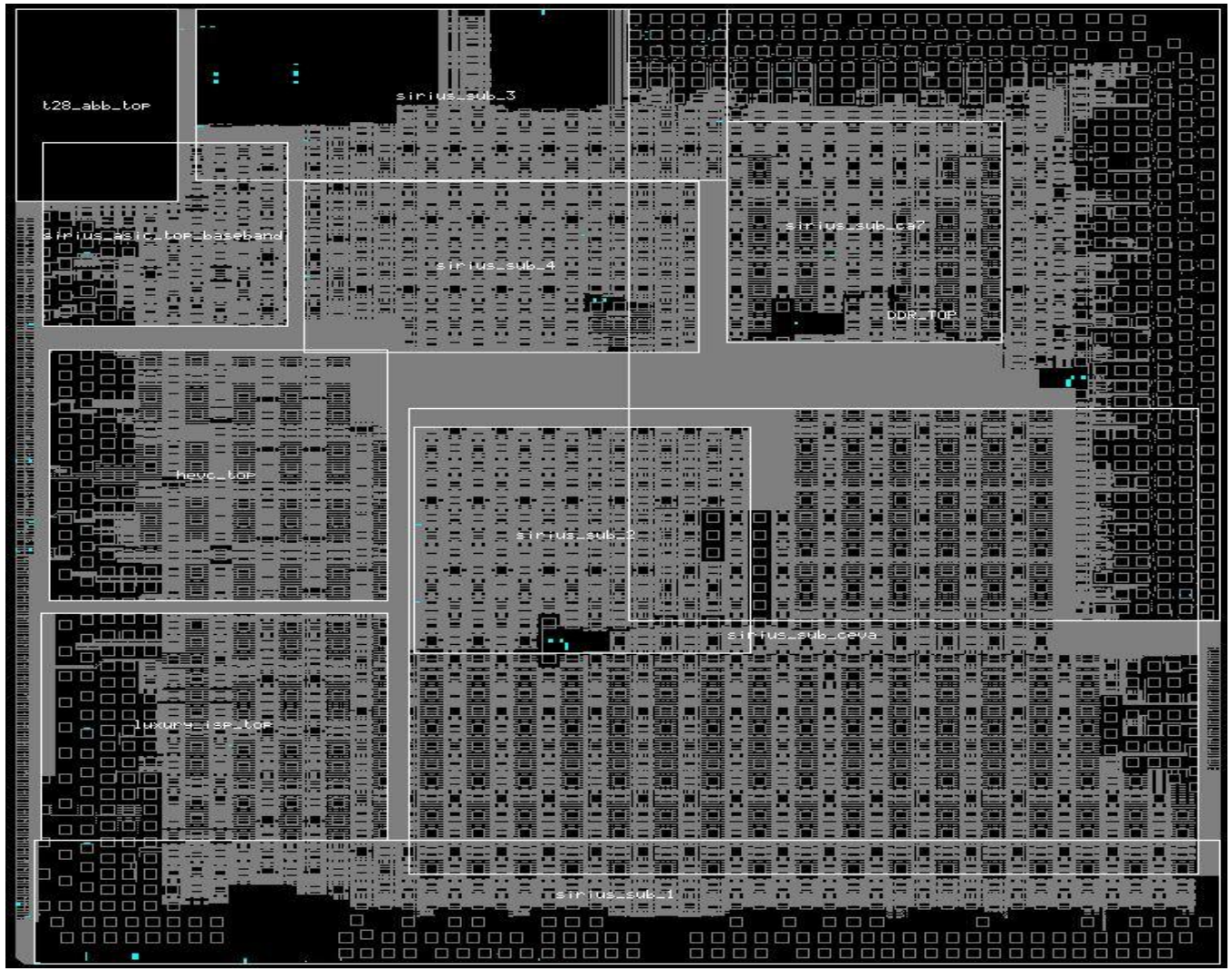
ERC floating.mnpg



mnpg

Cell / Check	Results
Cell sirius_top	13294
Check floating.nxwell_float	4392
Check floating.psub	987
Check mnpg	7339
Check mppg	8
Check npvss49	232
Check npvss150	320
Check ppvdd150	16

1	2	3	4
22	23	24	25
43	44	45	46
64	65	66	67
85	86	87	88
106	107	108	109
127	128	129	130
148	149	150	151
169	170	171	172

```
Rule File Pathname: tmp_rule
MOS connected to both power and ground
```

sdtc01cap_t28hpc_4t2r_vf180_6020
sdtc01pdp_t28hpc_xx_vf180_6020
dwc_pcie2_pads_x2_ns
dwc_hdmi1rxio
dwc_usb3_pads_sspx1_hspx1_ns
dwc_dphy2sio
dwc_dphy2bio
t28_pll_arm_top
pll_ddr_top
DDRIO
IO

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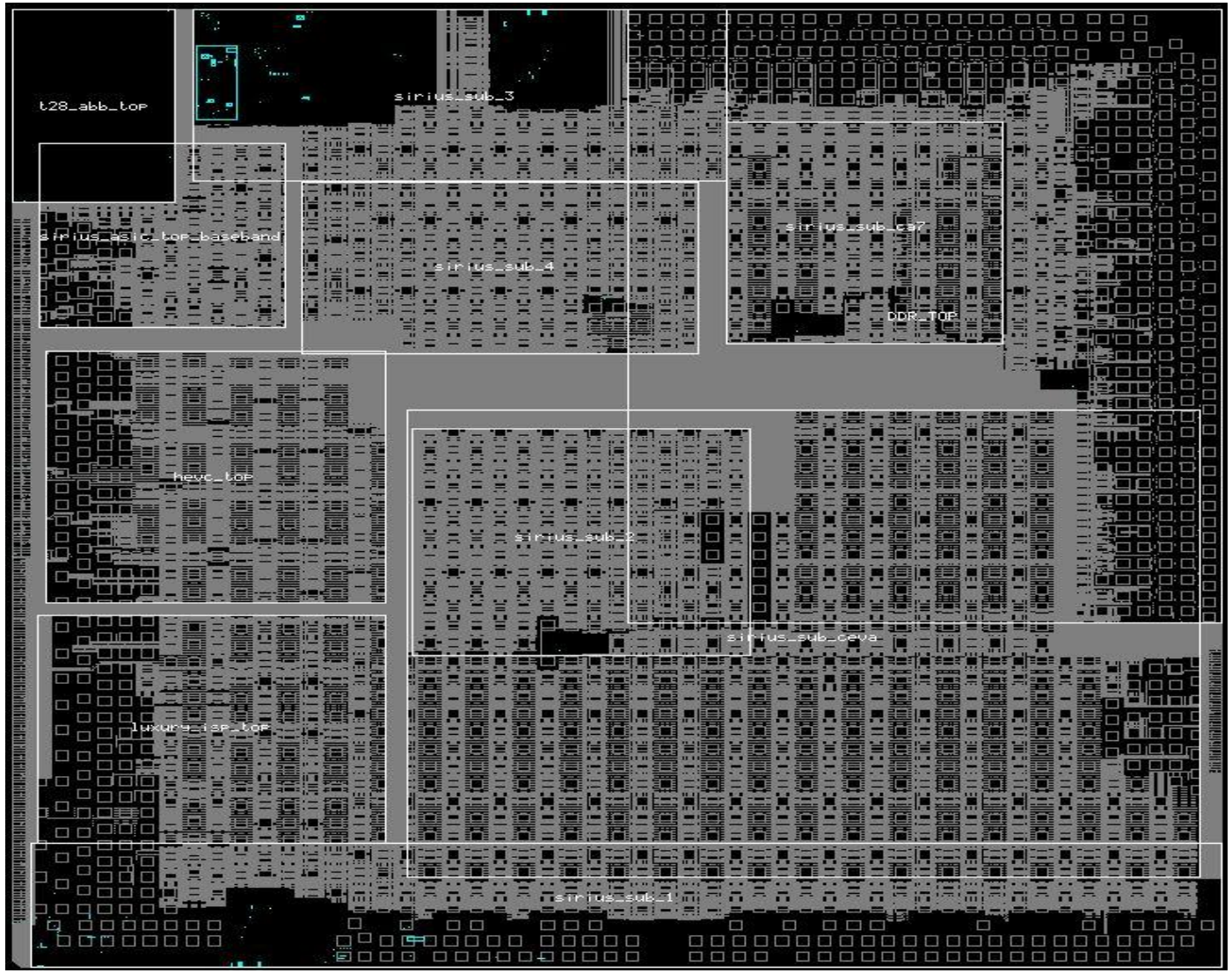
ERC npvss49



npvss49

Cell / Check	Results
Cell sirius_top	13294
Check floating.nxwell_float	4392
Check floating.psub	987
Check mnpg	7339
Check mppg	8
Check npvss49	232
Check npvss150	320
Check ppvdd150	16

13063	13064	13065	13066
13084	13085	13086	13087
13105	13106	13107	13108
13126	13127	13128	13129
13147	13148	13149	13150
13168	13169	13170	13171
13189	13190	13191	13192
13210	13211	13212	13213
13231	13232	13233	13234

```
Rule File Pathname: tmp_rule
ntap connected to GROUND
```

sdtc01cap_t28hpc_4t2r_vf180_6020
sdtc01pdp_t28hpc_xx_vf180_6020
dwc_pcie2_x2_ns
dwc_pcie2_pads_x2_ns
dwc_hdmi_20_rx_1p_phy_ns
dwc_hdmi1rxio
dwc_usb3_sspx1_hspx1_ns
dwc_usb3_pads_sspx1_hspx1_ns
dwc_mipi_2_bidir_dphy_ns_core
dwc_dphy2sio
dwc_dphy2bio
t28_abb_top
t28_pll_arm_top
pll_ddr_top
DDRIO
IO

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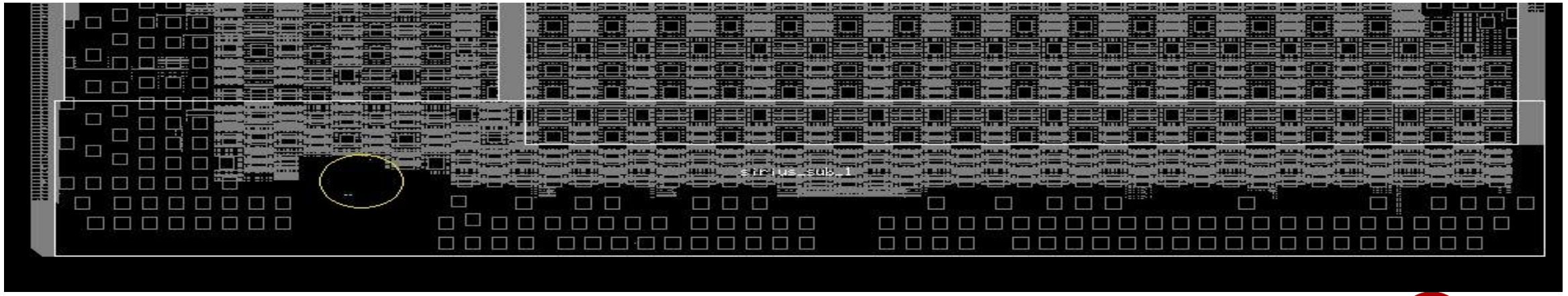
ERC NPVSS150

Cell / Check	Results
Cell sirius_top	13294
Check floating.nxwell_float	4392
Check floating.psub	987
Check mnpg	7339
Check mppg	8
Check npvss49	232
Check npvss150	320
Check ppvdd150	16

12743	12744	12745	12746
12764	12765	12766	12767
12785	12786	12787	12788
12806	12807	12808	12809
12827	12828	12829	12830
12848	12849	12850	12851
12869	12870	12871	12872
12890	12891	12892	12893
12911	12912	12913	12914

```
Rule File Pathname: tmp_rule
gate1_not_I02 connected to GROUND
```

dwc_usb3_sspx1_hspx1_ns



VeriSilicon

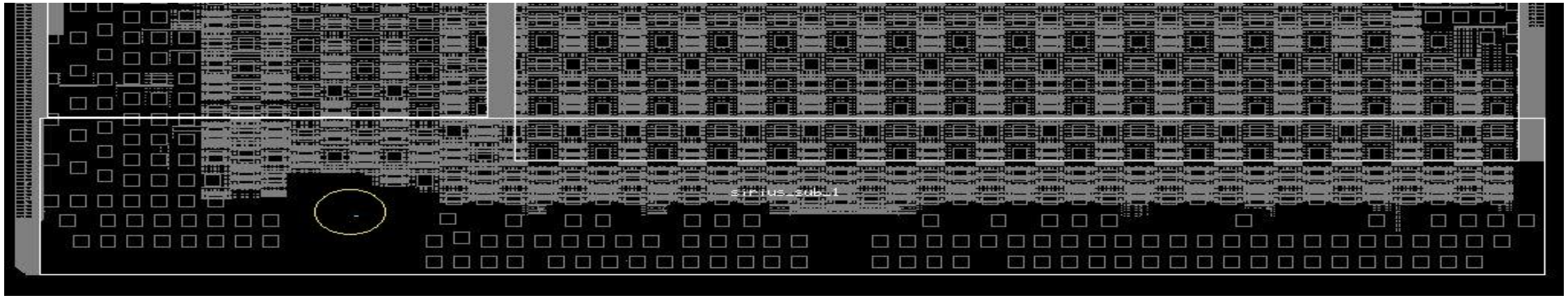
ERC NPVDD150

Cell / Check	Results
Cell sirius_top	13294
Check floating.nxwell_float	4392
Check floating.psub	987
Check mnpg	7339
Check mppg	8
Check npvss49	232
Check npvss150	320
Check ppvdd150	16

12727 12728 12729

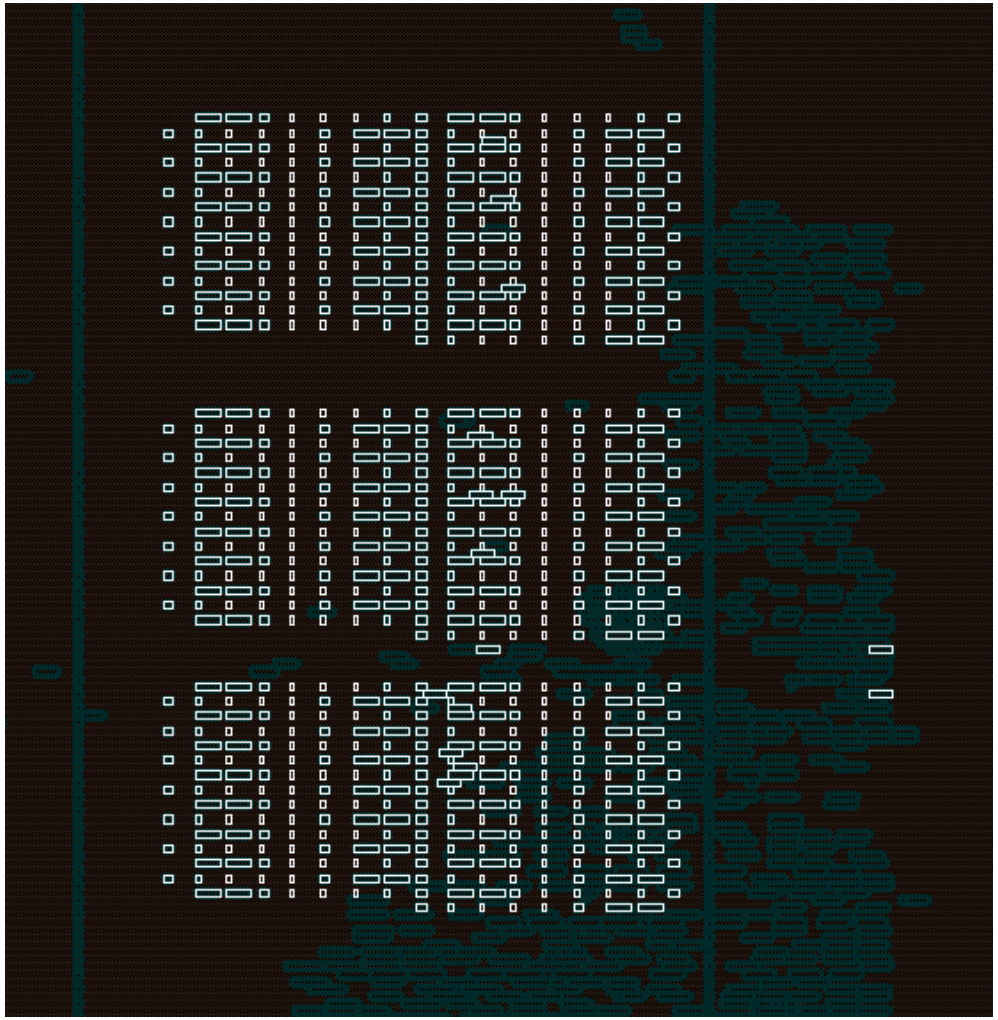
```
Rule File Pathname: tmp_rule
gate1_not_I02 connected to POWER
```

dwc_usb3_sspx1_hspx1_ns



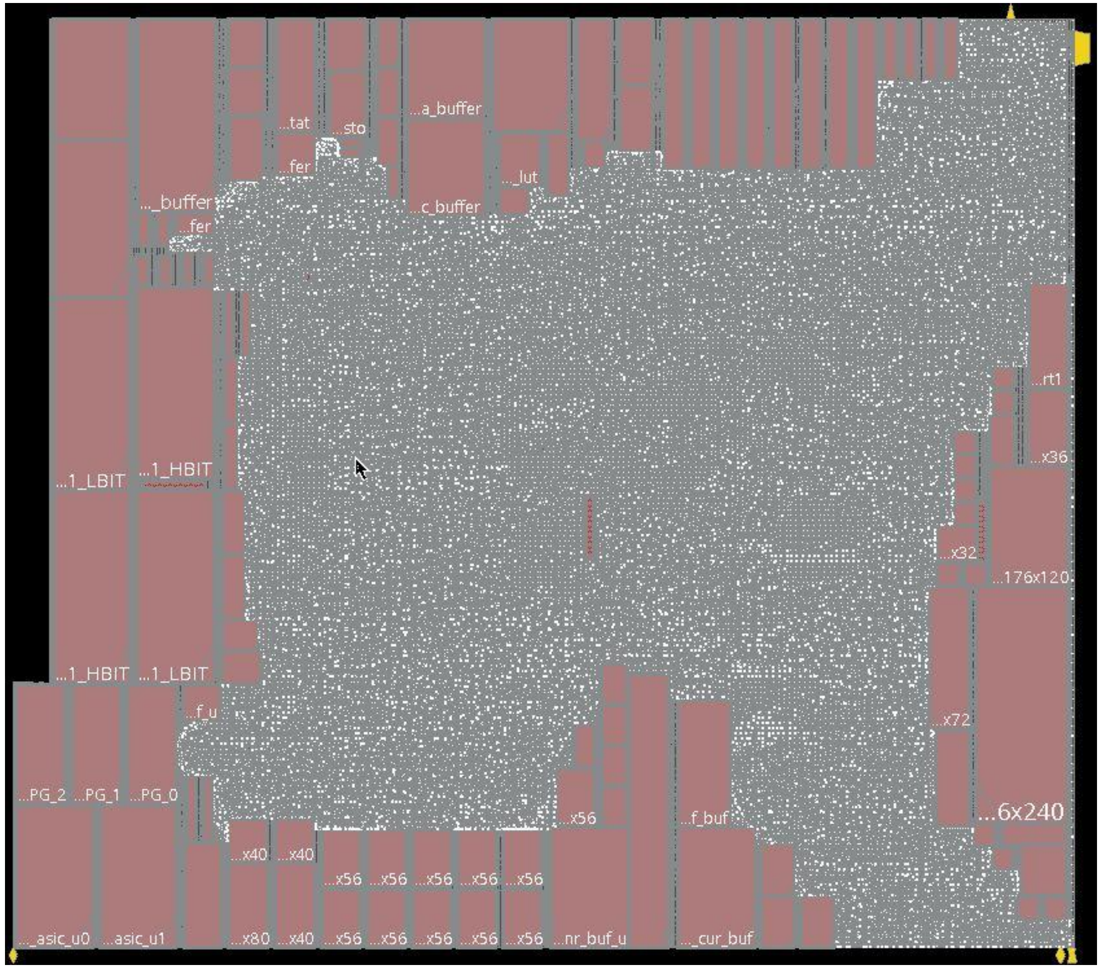
VeriSilicon

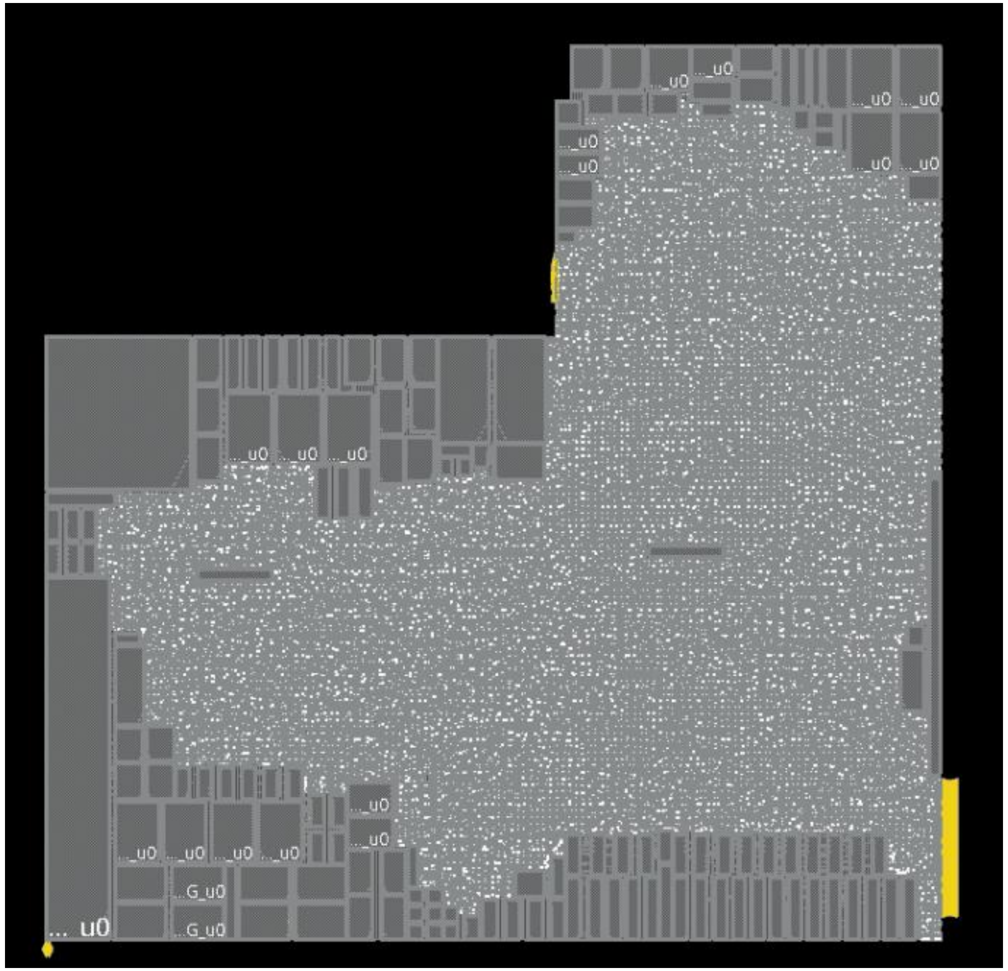
DVP delay line



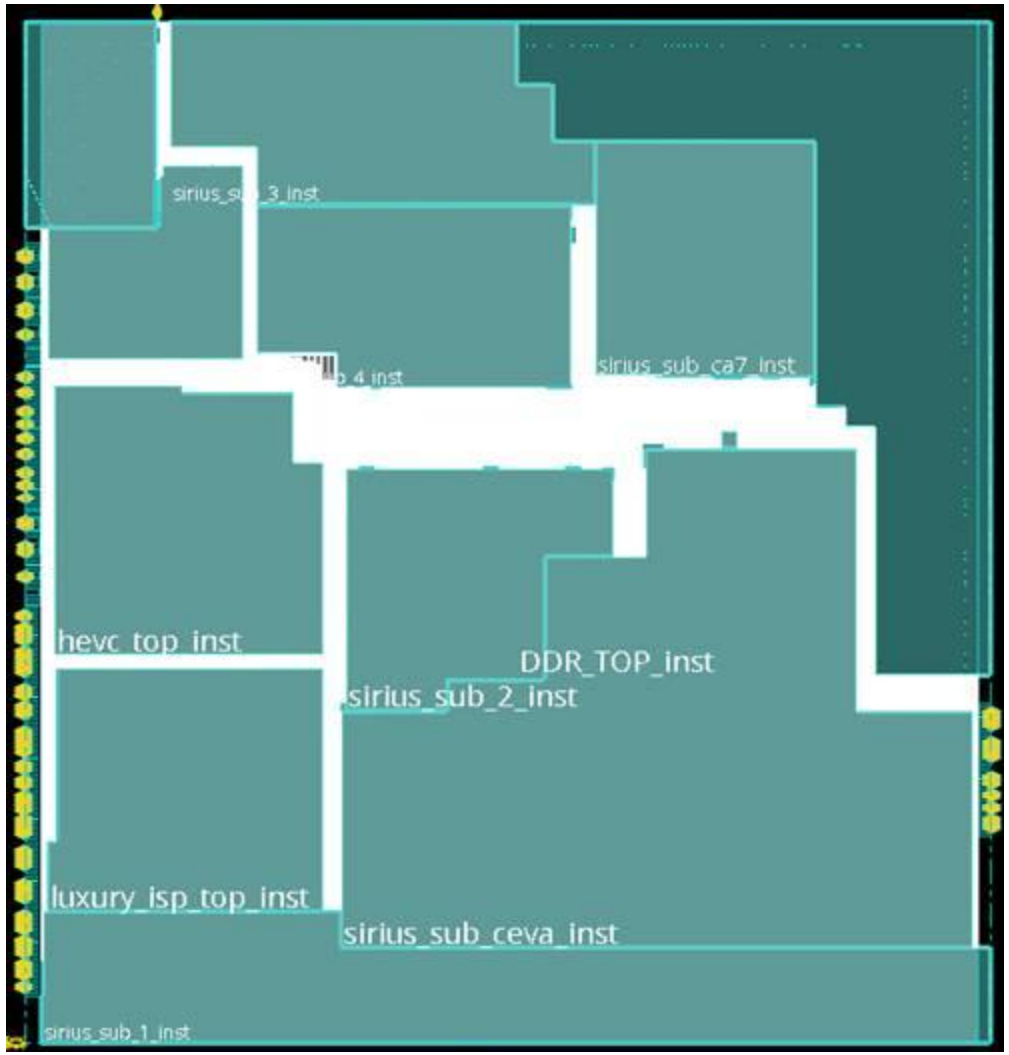
TRNG delay line

BB&ISP spare gates

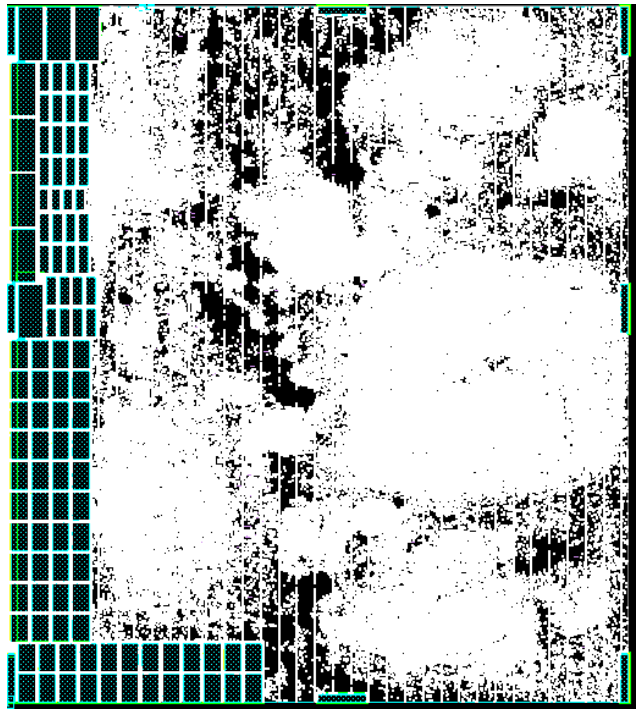


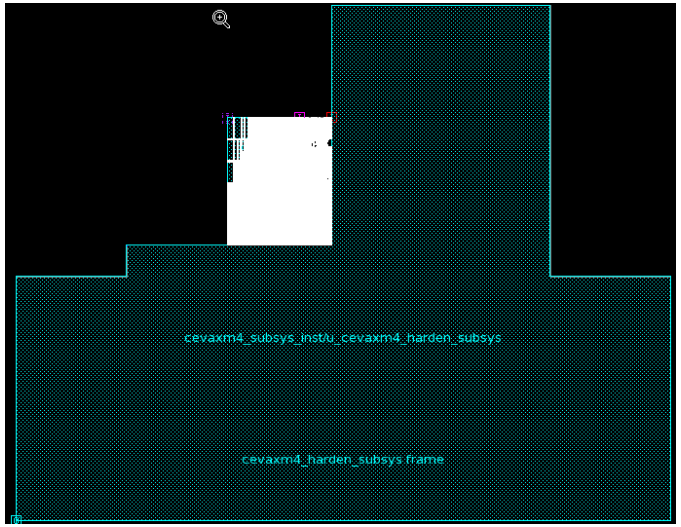


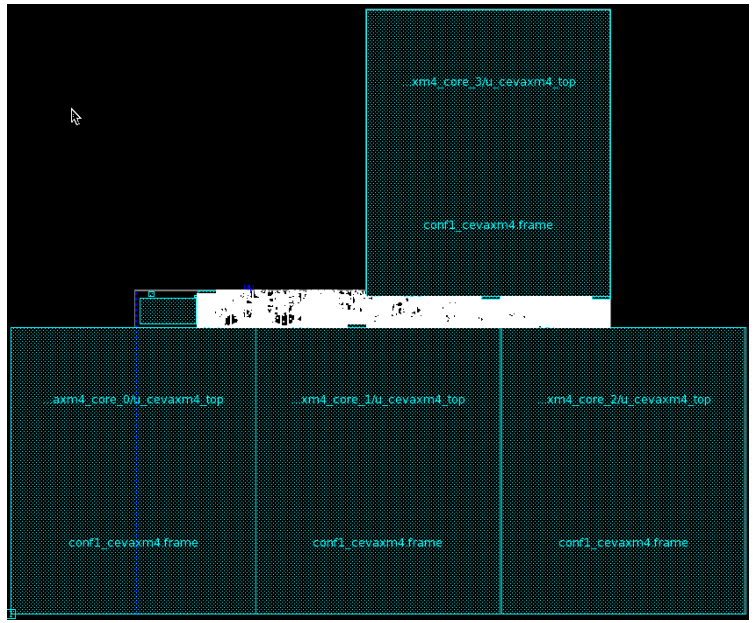
TOP DECAP


sirius_sub_3_inst
sirius_sub_ca7_inst
hevc_top_inst
DDR_TOP_inst
sirius_sub_2_inst
luxury_isp_top_inst
sirius_sub_ceva_inst
sirius_sub_1_inst

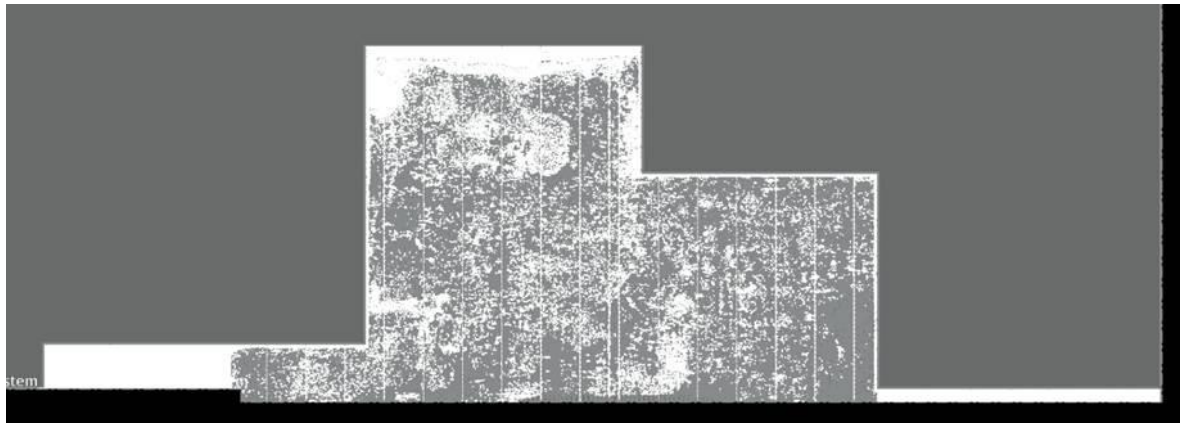
SUB CEVA ECO DECAP

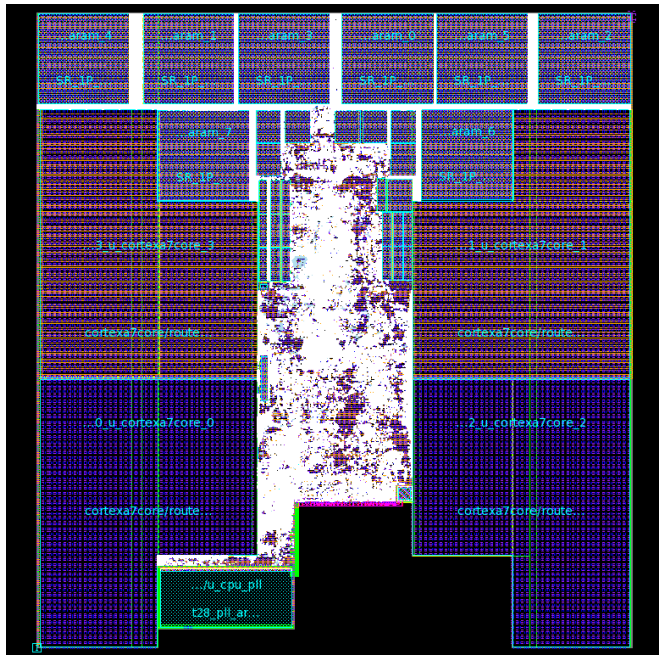


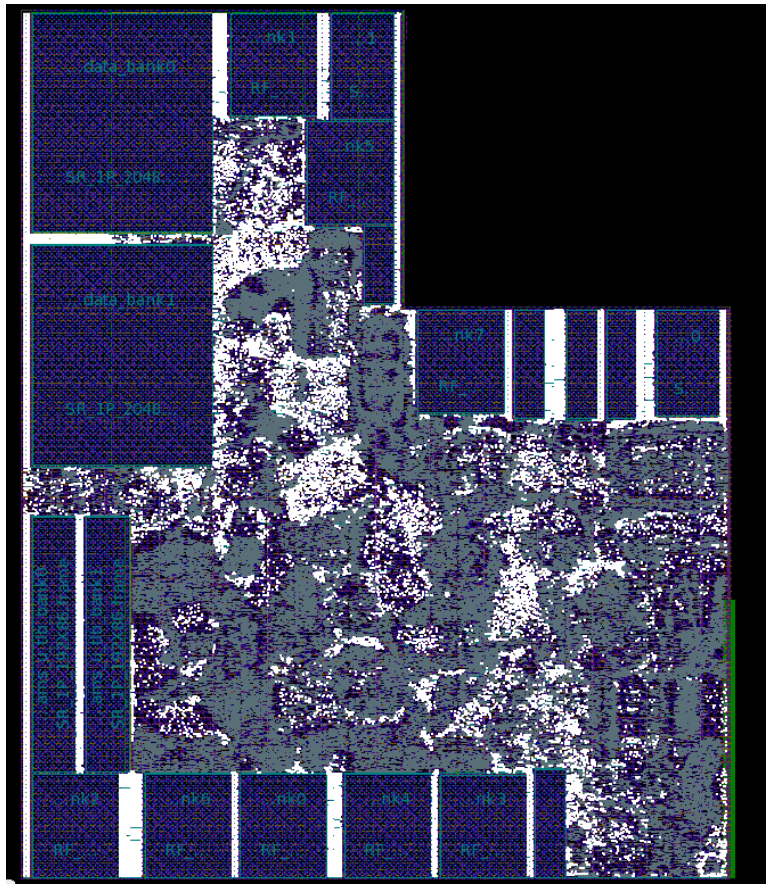




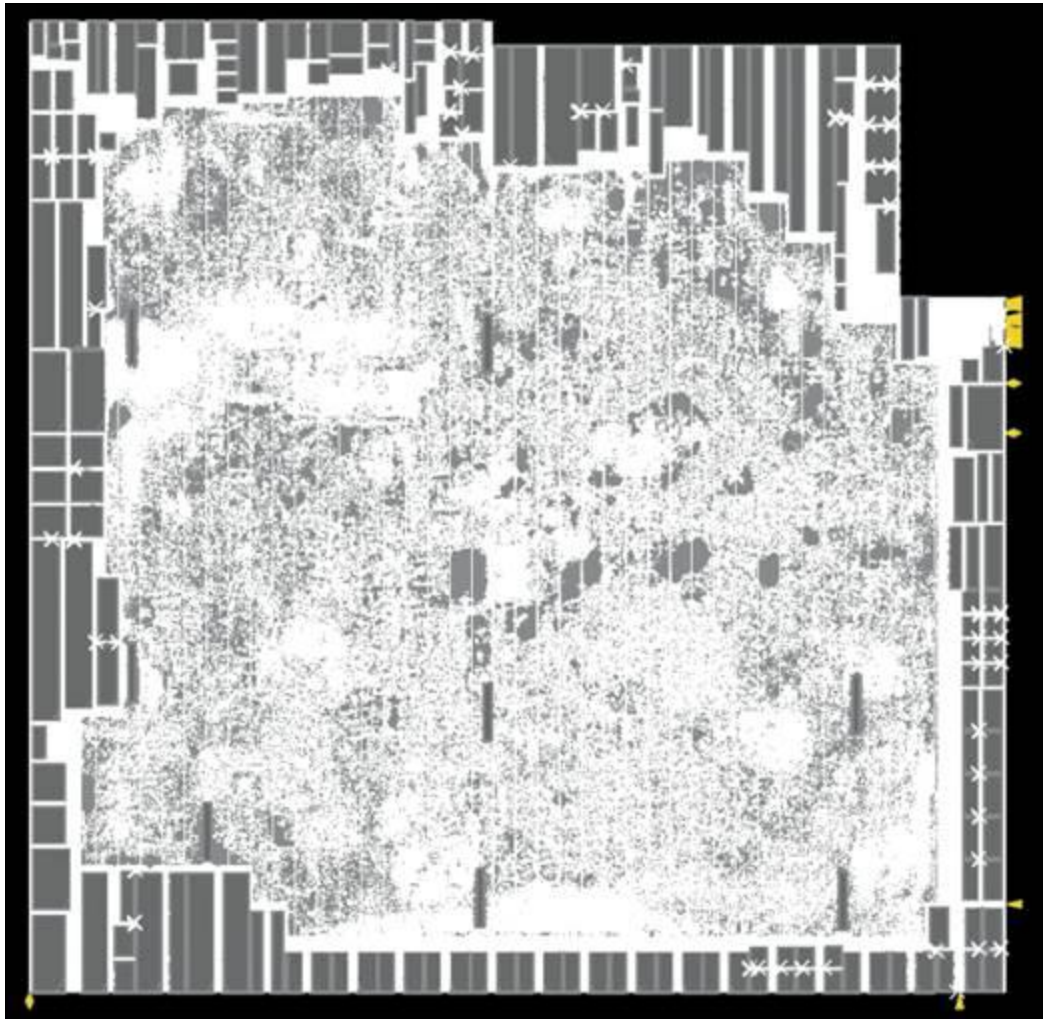
SUB CA7 ECO DECAP



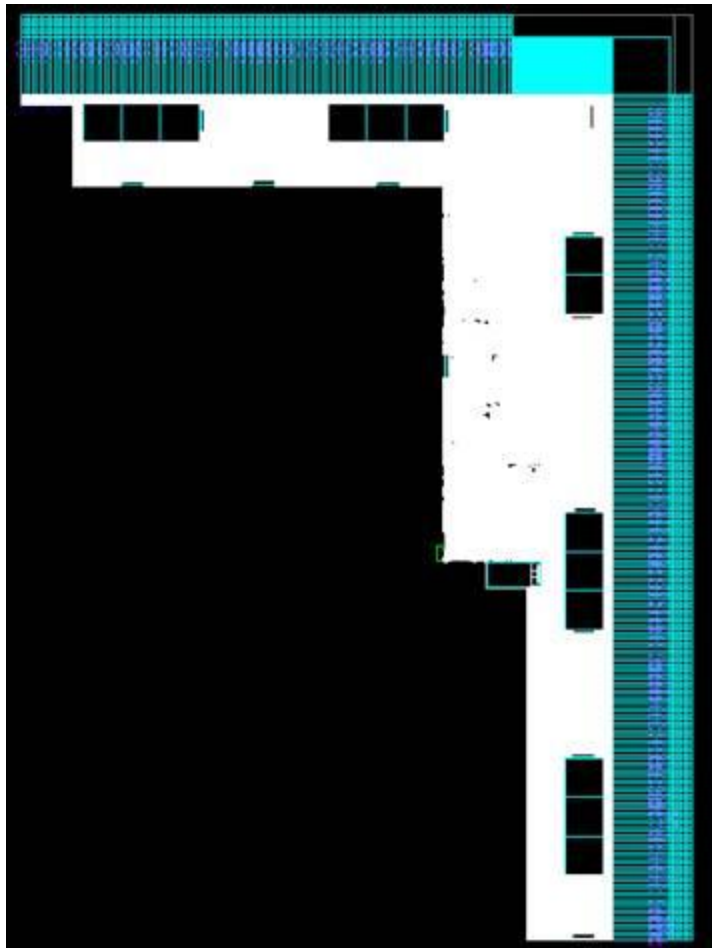




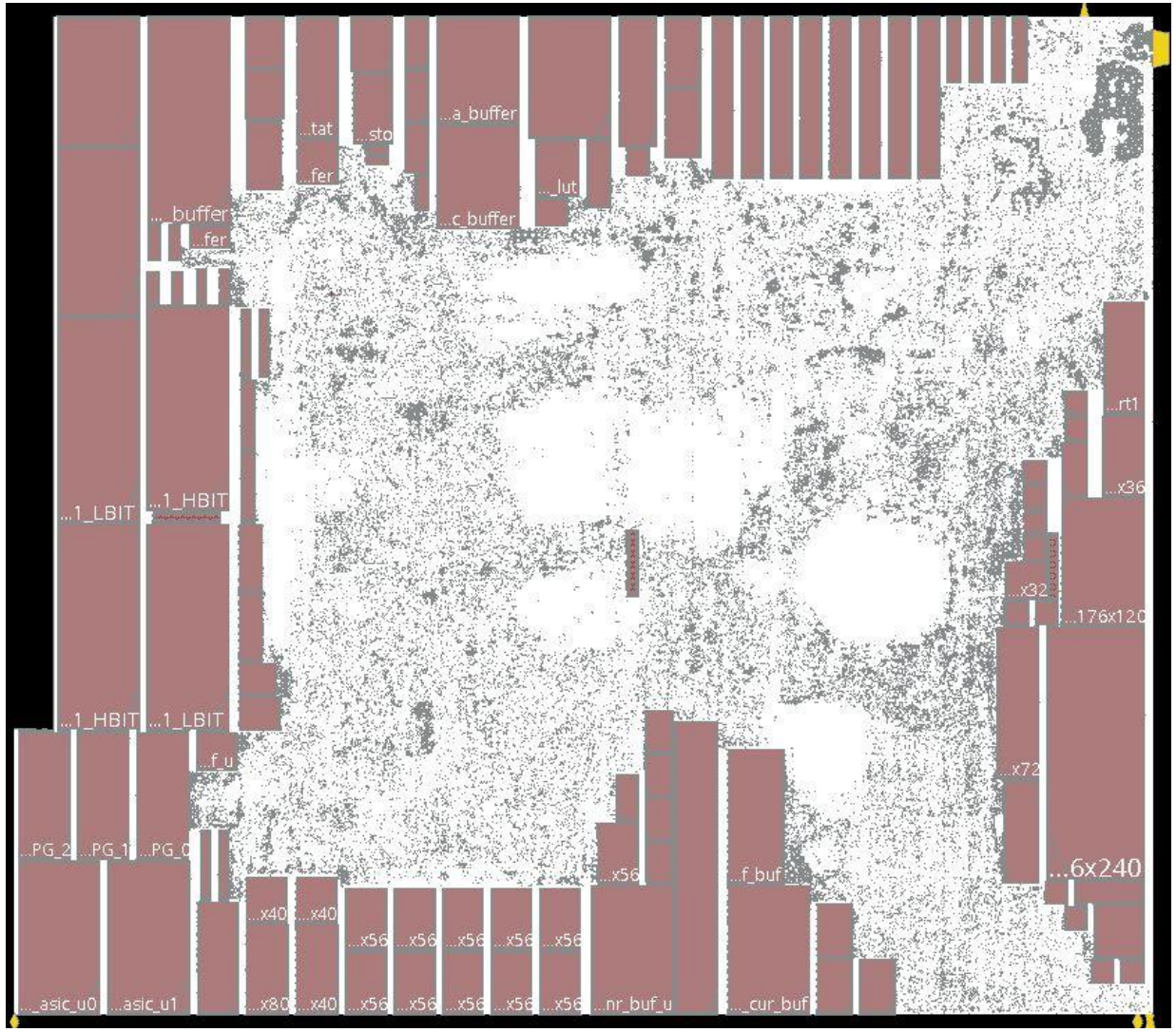
HEVC ECO DECAP



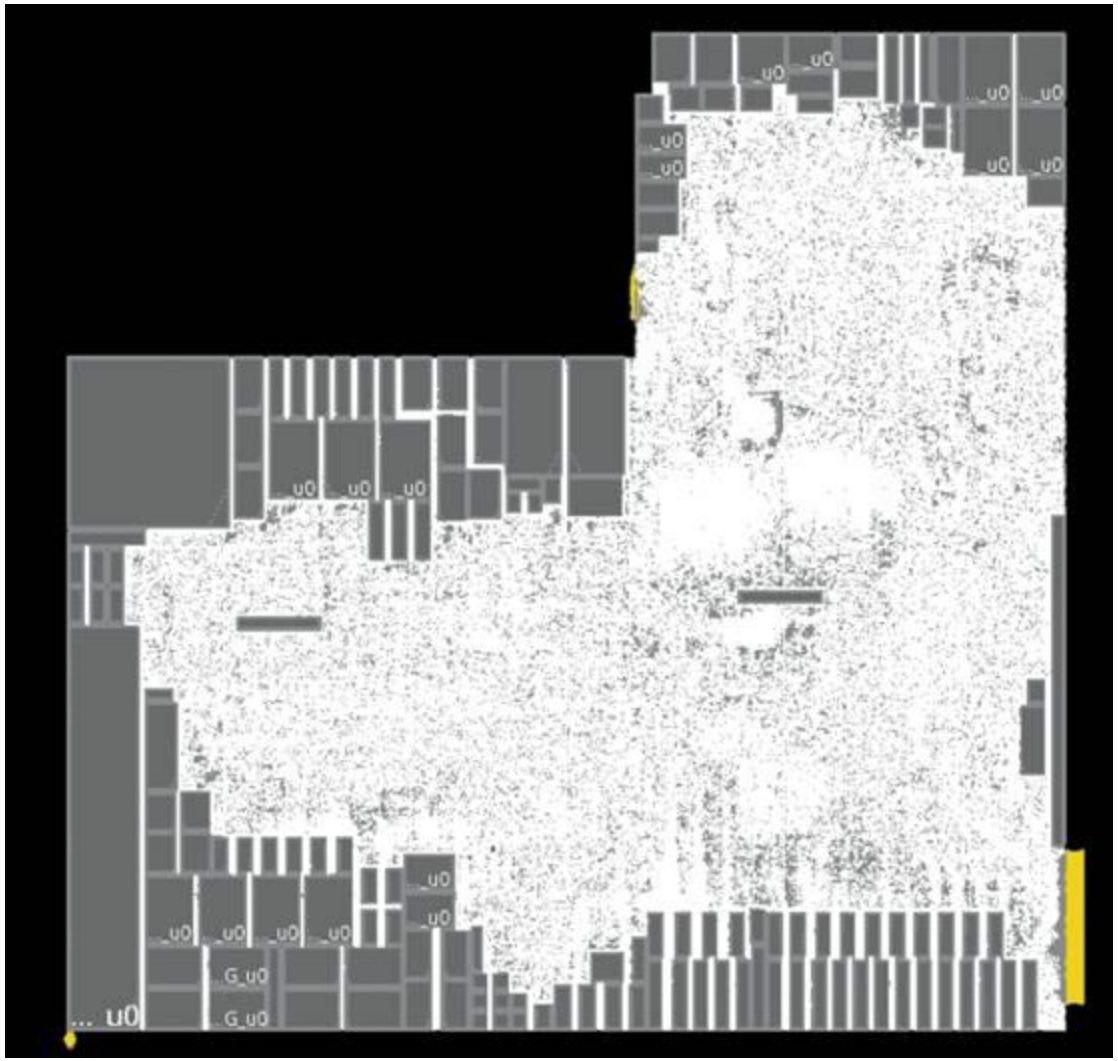
DDR ECO DECAP



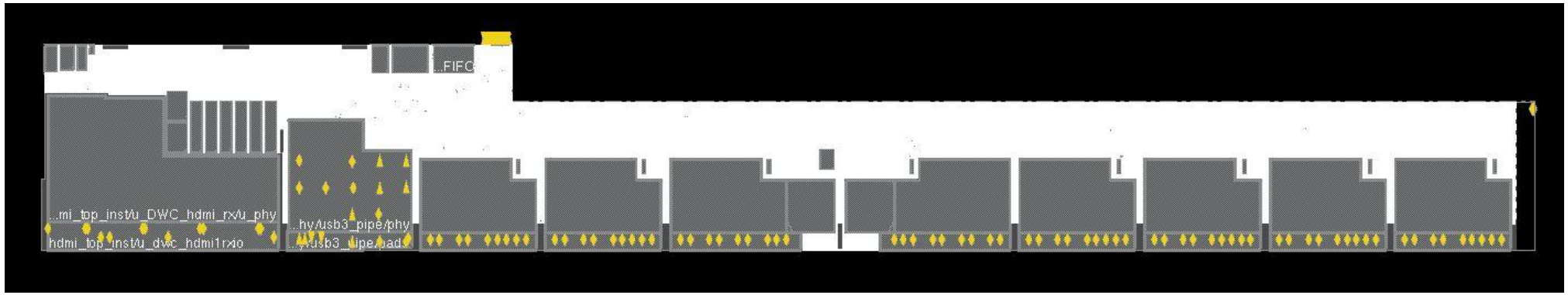
ISP ECO DECAP



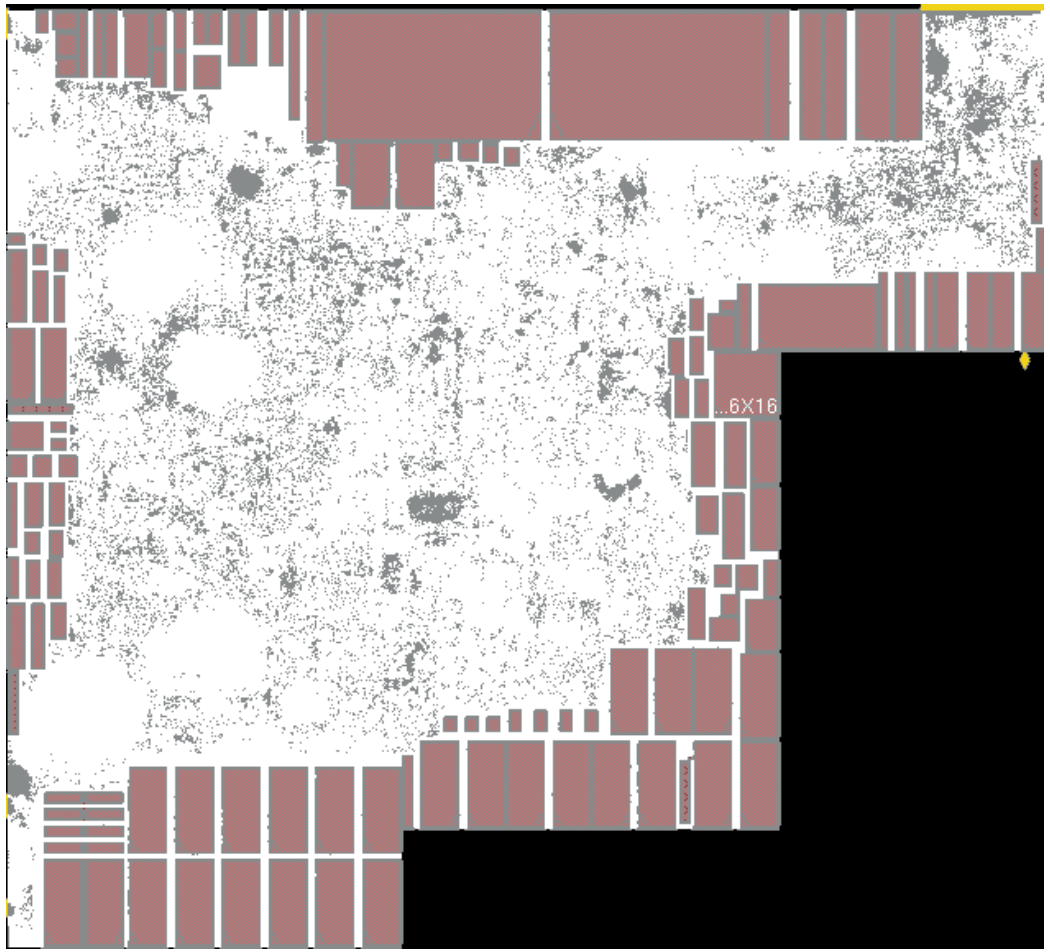
BB ECO DECAP



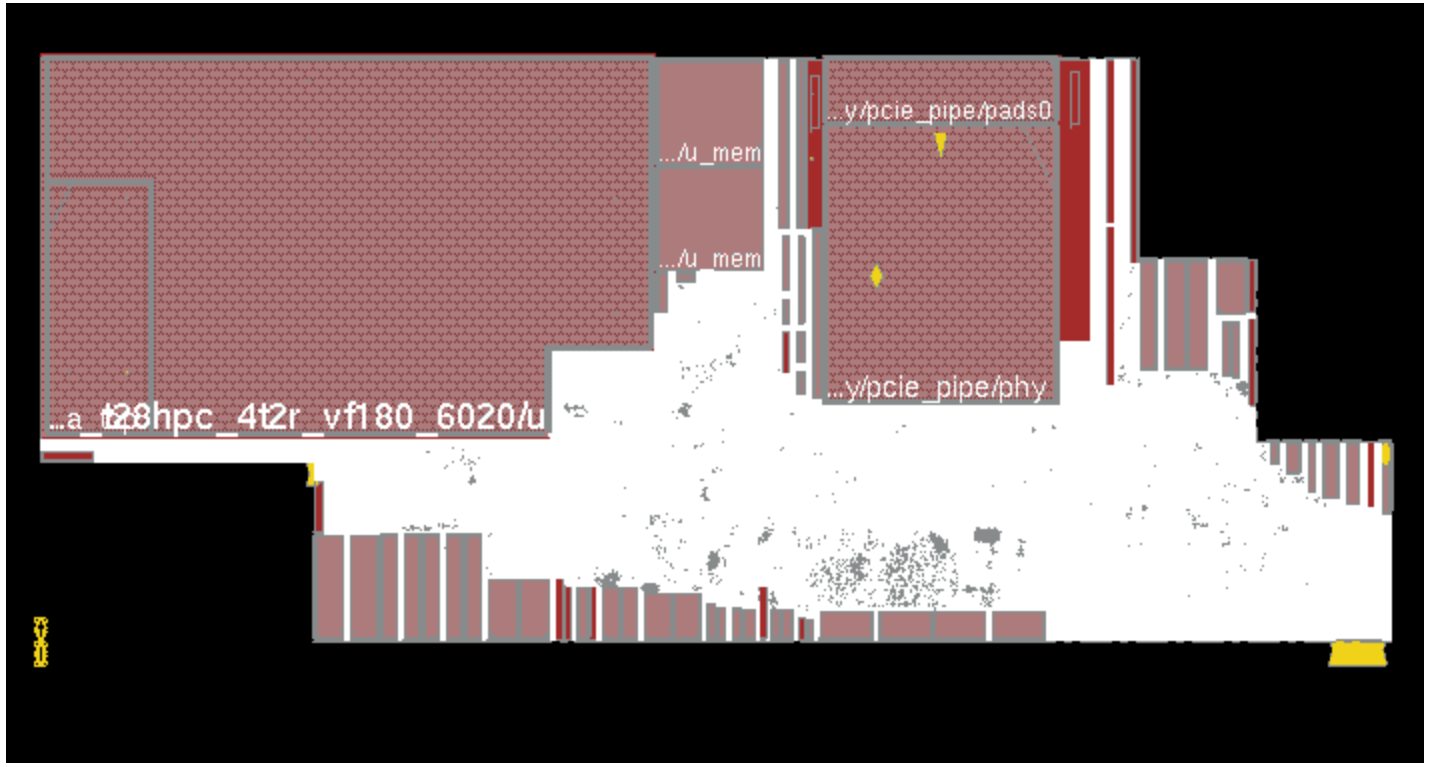
SUB1 ECO DECAP



SUB2 ECO DECAP



SUB3 ECO DECAP



SUB4 ECO DECAP

TSMC recommended Timing signoff criteria

Timing Check	Library PVT Conditions	RC Corner	OCV and Design Margin
Setup	SSG/0.81/125C	Cworst	(1a) SBOCV on launch+data /capture clock (1b) Clock jitter OR (2a) +3.9% on launch clock cell, +7.7% on data clock cell and -3.9% on capture cell (2b) -8.5% on capture net (2c) Clock jitter + 25ps setup margin
		Rcworst	
	SSG/0.81/-40C**	Cworst	
		Rcworst	
Hold	SSG/0.81/125C	Cworst	(1a) SBOCV on launch+data/capture clock (1b) Flop hold constraint variation margin OR (2a) -4.9% on launch clock cell, -12.7% on data cell and +4.9% on capture cell (2b) -8.5% on launch clock net, -8.5% on data net (2c) 70ps hold margin
		Rcworst	
	SSG/0.81/-40C**	Cworst	
		Rcworst	
	FF/0.99/125C	Cworst	(1a) SBOCV on capture clock (1b) Flop hold constraint variation margin per PVT OR (2a) +13.9% on capture cell (2b) -8.5% on launch clock net, -8.5% on data net (2c) 50ps hold margin
		Rcworst	
	FF/0.99/-40C**	Cworst	
		Rcworst	
	FF/0.99/125C	Cbest	(1a) SBOCV on capture clock (1b) Flop hold constraint variation margin per PVT OR (2a) +13.9% on capture cell (2b) +8.5% on capture net (2c) 50ps hold margin
		Rcbest	
	FF/0.99/-40C**	Cbest	
		Rcbest	

VeriSilicon

Timing signoff criteria for Artosyn Sirius

				1.8v@EMMC/SD IO	3.3V@ EMMC/SD IO			
Type	Core Voltage	LIB	RC	function	MBIST	AC scan capture	DC scan	scan shift
setup	Normal	WC (SS125)	Cworst	√	√	√	√	√
		WC (SS125)	RCworst	√	√	√	√	√
		WCL (SSm40)	Cworst	√	√	√	√	√
		WCL (SSm40)	RCworst	√	√	√	√	√
hold	Normal Voltage @ CEVA/CA7 core	WC (SS125)	Cworst	√	√	√	√	√
		WC (SS125)	RCworst	√	√	√	√	√
		WCL (SSm40)	Cworst	√	√	√	√	√
		WCL (SSm40)	RCworst	√	√	√	√	√
		ML(FF125)	Cbest	√	√	√	√	√
		ML(FF125)	RCbest	√	√	√	√	√
		LT(FFm40)	Cbest	√	√	√	√	√
		LT(FFm40)	RCbest	√	√	√	√	√
	Over Drive @ CEVA/CA7 core	WC (SS125)	Cworst	√				
		WC (SS125)	RCworst	√				
		WCL (SSm40)	Cworst	√				
		WCL (SSm40)	RCworst	√				
		OD_ML(FF125)	Cbest	√				
		OD_ML(FF125)	RCbest	√				
		OD_LT(FFm40)	Cbest	√				
		OD_LT(FFm40)	RCbest	√				

No OCV derating on IO instances

VeriSilicon

Clock Uncertainty@Function Mode

clock period	clock name	setup uncertainty	hold uncertainty (FF)	hold uncertainty (SS)
>= 800M	a7pll_clk, cortexa7_clk, l2_clk	50ps	40ps	70ps
< 800M		75PS	40PS	70PS
ceva	*cevaxm4_core*_clk	30ps	40ps	70ps
DDR PHY clocks	set_clock_uncertainty -setup 0.12 -from [get_clocks {AC_CTL_CLK DX*_CTL_CLK}] -to [get_clocks ddr_pll_clk] set_clock_uncertainty -setup 0.12 -from [get_clocks ddr_pll_clk] -to [get_clocks {AC_CTL_CLK DX*_CTL_CLK}] set_clock_uncertainty -setup 0.12 -from [get_clocks ddr_pll_clk] -to [get_clocks DX*_DDR_CLK] set_clock_uncertainty -setup 0.12 -from [get_clocks DX*_DDR_CLK] -to [get_clocks ddr_pll_clk] set_clock_uncertainty -hold 0.16 -from [get_clocks {AC_CTL_CLK DX*_CTL_CLK}] -to [get_clocks ddr_pll_clk] set_clock_uncertainty -hold 0.16 -from [get_clocks ddr_pll_clk] -to [get_clocks {AC_CTL_CLK DX*_CTL_CLK}] set_clock_uncertainty -hold 0.16 -from [get_clocks ddr_pll_clk] -to [get_clocks DX*_DDR_CLK] set_clock_uncertainty -hold 0.16 -from [get_clocks DX*_DDR_CLK] -to [get_clocks ddr_pll_clk]	120ps	160ps	160ps
usb clocks	sirius_sub_1_inst/usb3_top_inst/phy/hspx1_div8clk \ sirius_sub_1_inst/usb3_top_inst/phy/hspx1_div10clk \ sirius_sub_1_inst/usb3_top_inst/phy/hspx1_div40clk \ sirius_sub_1_inst/usb3_top_inst/phy/hspx1_div16clk \ sirius_sub_1_inst/usb3_top_inst/phy/sspx1_mpll_ana_word_clk \ sirius_sub_1_inst/usb3_top_inst/phy/sspx1_mpll_ana_dword_clk \ sirius_sub_1_inst/usb3_top_inst/phy/sspx1_mpll_ana_qword_clk \ sirius_sub_1_inst/usb3_top_inst/phy/sspx1_mpll_ana_refssc_clk \ sirius_sub_1_inst/usb3_top_inst/phy/sspx1_tx0_out_word_clk \ sirius_sub_1_inst/usb3_top_inst/phy/sspx1_rx0_ana_word_clk \ sirius_sub_1_inst/usb3_top_inst/phy/sspx1_rx0_out_clk \ sirius_sub_1_inst/usb3_top_inst/phy/RX0CLK \ usb3_top_inst_mpll_word_clk \ usb3_top_inst_phy_ref_clk \ usb3_top_inst_rx0_clk \ sirius_sub_1_inst/usb3_top_inst/phy/MPLLWORDCLK \ sirius_sub_1_inst/usb3_top_inst/phy/MPLLDWORDCLK \ sirius_sub_1_inst/usb3_top_inst/phy/MPLLQWORDCLK \ sirius_sub_1_inst/usb3_top_inst/phy/REFOUTPUTCLK \ sirius_sub_1_inst/usb3_top_inst/phy/pll_480m_clk_in \ usb3_top_inst_PHYCLOCK0 \ usb3_top_inst_FREECLK \ sirius_sub_1_inst/usb3_top_inst/phy/int_sspx1_480m_clk \ usb3_top_inst_CLK480M \ usb3_top_inst_CLK48MOHCI \ usb3_top_inst_CLK12MOHCI \	200ps	100ps	100ps

Full Chip Hold Timing Violation Summary (PBA mode)

No OCV derating on IO instances

				1.8v@EMMC/SD IO
Type	Core Voltage	LIB	RC	function
hold	Normal Voltage @ CEVA/CA7 core	WC (SS125)	Cworst	- 0.0006 (1)
		WC (SS125)	RCworst	clean
		WCL (SSm40)	Cworst	clean
		WCL (SSm40)	RCworst	clean
		ML(FF125)	Cbest	-0.001 (27)
		ML(FF125)	RCbest	-0.005 (31)
		LT(FFm40)	Cbest	-0.0008 (14)
		LT(FFm40)	RCbest	-0.008 (79)
	Over Drive @ CEVA/CA7 core	WC (SS125)	Cworst	- 0.0006 (1)
		WC (SS125)	RCworst	-0.0003 （1）
		WCL (SSm40)	Cworst	-0.0036 （9）
		WCL (SSm40)	RCworst	-0.0018 （1）
		OD_ML(FF125)	Cbest	-0.002 (32)
		OD_ML(FF125)	RCbest	-0.005 （31）
		OD_LT(FFm40)	Cbest	-0.0008 (14)
		OD_LT(FFm40)	RCbest	-0.008 (82)

Setup Timing Violation Summary (PBA mode)

▲ Full Chip (exclude CEVA/DDR)

				1.8v@EMMC/SD IO
Type	Core Voltage	LIB	RC	function
setup	Normal	WC (SS125)	Cworst	clean
		WC (SS125)	RCworst	clean
		WCL (SSm40)	Cworst	-0.002 (2)
		WCL (SSm40)	RCworst	clean

▲ DDR (500M)

				1.8v@EMMC/SD IO
Type	Core Voltage	LIB	RC	function
setup	Normal	WC (SS125)	Cworst	clean
		WC (SS125)	RCworst	clean
		WCL (SSm40)	Cworst	clean
		WCL (SSm40)	RCworst	clean

▲ CEVA (600M, non-OD)

				1.8v@EMMC/SD IO
Type	Core Voltage	LIB	RC	function
setup	Normal	WC (SS125)	Cworst	clean
		WC (SS125)	RCworst	clean
		WCL (SSm40)	Cworst	-0.015 (24)
		WCL (SSm40)	RCworst	clean

▲ DDR (533M)

				1.8v@EMMC/SD IO
Type	Core Voltage	LIB	RC	function
setup	Normal	WC (SS125)	Cworst	clean
		WC (SS125)	RCworst	-0.006 (1)
		WCL (SSm40)	Cworst	-0.0859 (65) , 120ps uncertainty
		WCL (SSm40)	RCworst	-0.0276 (2), 120ps uncertainty

IO Timing

IO INPUT	constraint		wc_cworst_125		wc_rcworst_125		wcl_cworst_m40		wcl_rcworst_m40		ml_cbest_125		ml_rcbest_125		lt_cbest_m40		lt_rcbest_m40	
	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew
DVP	2.1	0.5	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet
SD	N/A	0.2	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet
EMMC	N/A	0.5	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet
ETH	N/A	0.5	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet	N/A	meet
FLASH	0.2	0.2	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet

IO OUTPUT	constraint		wc_cworst_125		wc_rcworst_125		wcl_cworst_m40		wcl_rcworst_m40		ml_cbest_125		ml_rcbest_125		lt_cbest_m40		lt_rcbest_m40	
	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew	clk skew	data skew
EMMC	0.5	0.2	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet
SD	0.5	0.5	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet
TRACE	1	0.65	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet
ETH	0.3	0.2	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet
DVP	1.2	0.8	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet
FLASH	0.5	0.5	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet
I2S GBE_PAD	1	1	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet
I2S I2S_PAD	1	1	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet
HDMI GBE_PAD	1	1	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet
HDMI I2S_PAD	1	1	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet	meet

No OCV derating on IO instances

TypeC Clock Skew Violations

- TypeC clock skew violation due to OCV
- WCL Cworst clock skew listed as below

pin	rise_tran_max	rise_tran_min	fall_tran_max	fall_tran_min
sirius_sub_3_inst/cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/cmn_psm_clk_in	0.083723	0.083458	0.079206	0.078442
sirius_sub_3_inst/cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/xcvr_psm_clk_ln_2	0.109012	0.108966	0.099471	0.099634
sirius_sub_3_inst/cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/xcvr_psm_clk_ln_1	0.099122	0.099059	0.090591	0.090674
sirius_sub_3_inst/cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/xcvr_psm_clk_ln_0	0.098405	0.098341	0.089871	0.089975
sirius_sub_3_inst/cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/xcvr_psm_clk_ln_3	0.11093	0.110884	0.101314	0.101439

pin	max_rise_arrival	min_rise_arrival	max_fall_arrival	min_fall_arrival
sirius_sub_3_inst/cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/cmn_psm_clk_in	2.732111	2.44608	2.681993	2.403781
sirius_sub_3_inst/cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/xcvr_psm_clk_ln_2	2.690405	2.408958	2.640404	2.368251
sirius_sub_3_inst/cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/xcvr_psm_clk_ln_1	2.617184	2.341162	2.564248	2.297656
sirius_sub_3_inst/cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/xcvr_psm_clk_ln_0	2.616337	2.340403	2.563539	2.296978
sirius_sub_3_inst/cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/xcvr_psm_clk_ln_3	2.691041	2.409555	2.640919	2.368721

Floating Macro Pins

floating InOut
Warning: InOut term >>>>> hdmi_top_inst/u_DWC_hdmi_rx/u_phy/VREF_SE_TOARC <<<<< have no drive.
Warning: InOut term >>>>> hdmi_top_inst/u_DWC_hdmi_rx/u_phy/VREF_CM_TOARC <<<<< have no drive.
Warning: InOut term >>>>> pcie_iip_device_inst/u_subsystem/u_phy/pcie_pipe/pads0/resref_s <<<<< have no drive
Warning: InOut term >>>>> cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/cmn_atb_core_0 <<<<< have no drive.
Warning: InOut term >>>>> cdn_typec_subsystem_top_inst/u_cdnsusbss_drd_ips/u_cdnsusbss_drd_phy/u_sdtc01cay_t28hpc_4t2r_vf180_6020/u_pma/cmn_atb_core_1 <<<<< have no drive.
floating Input
Error: Input term >>>>> hdmi_top_inst/u_dwc_hdmi1rxio/TRIGB <<<<< have no drive!
Error: Input term >>>>> hdmi_top_inst/u_dwc_hdmi1rxio/TRIGA <<<<< have no drive!
Error: Input term >>>>> hdmi_top_inst/u_dwc_hdmi1rxio/OVDD <<<<< have no drive!
Error: Input term >>>>> hdmi_top_inst/u_dwc_hdmi1rxio/BOOST <<<<< have no drive!
Error: Input term >>>>> usb3_top_inst/U_usb3_ssphy/usb3_pipe/phy/ATBSP <<<<< have no drive!
Error: Input term >>>>> usb3_top_inst/U_usb3_ssphy/usb3_pipe/phy/ATBSM <<<<< have no drive!
Error: Input term >>>>> usb3_top_inst/U_usb3_ssphy/usb3_pipe/phy/ATBFP <<<<< have no drive!
Error: Input term >>>>> usb3_top_inst/U_usb3_ssphy/usb3_pipe/phy/ATBFM <<<<< have no drive!
Error: Input term >>>>> pcie_iip_device_inst/u_subsystem/u_phy/pcie_pipe/phy/atb_f_p <<<<< have no drive!
Error: Input term >>>>> pcie_iip_device_inst/u_subsystem/u_phy/pcie_pipe/phy/atb_f_m <<<<< have no drive!
Error: Input term >>>>> pcie_iip_device_inst/u_subsystem/u_phy/pcie_pipe/phy/atest <<<<< have no drive!
Error: Input term >>>>> pcie_iip_device_inst/u_subsystem/u_phy/pcie_pipe/phy/atb_s_p <<<<< have no drive!
Error: Input term >>>>> pcie_iip_device_inst/u_subsystem/u_phy/pcie_pipe/phy/atb_s_m <<<<< have no drive!

MBIST Controller Distribution

▲There are 139 MBIST controllers

Block	MBIST Controller Num
baseband	23
ca7 core	none
ca7 harden	1 (share bus)
ca7 sub subsystem	none
ceva harden	none
ceva subsystem	2
ceva core	6
DDR	none
HEVC	26
ISP	15
SUB1	9
SUB2	18
SUB3	17
SUB4	17
TOP	5

Scan Test Coverage

▲Stuck-At Test Coverage:

- ▶ Domain1 (ceva_harden, ceva_core*4, sub2, hevc): 99.3%
- ▶ Domain2 (The left): 98.5%

▲Transition Test Coverage:

- ▶ Domain1: 84.0%
- ▶ Domain2: 81.8%

Other reports

- Transition Violation Summary:

  transition_violation_reports_20171024.tar.gz

- Noise Violation Summary:

  noise_violation_reports.20171024.rpt.tar.gz

- VCLP Violation Summary:

  20171022_vclprpt.tar.gz

- Formal Verification Summary:

  formal_verifcation_reports.20171024.tar.gz

- TypeC clock Skew Violations:

  typec_skew_20171020.rpt

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