AR9201 Databook

New Generation HD AI SOC

v1.0

(ARTOSYN)

Version	Writer	Date	Description
v1.0	Song Pan	2018/2/8	Initial

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1. Introduction

AR9201 is one all-in-one SOC chip designed for various applications such as drone, intelligent surveillance, ADAS and car driving recorder, integrates ARM Cortex-A7 based CPU subsystem for application and Cortex-M7 based MCU subsystem for real-time system control, high performance computing array for machine vision, multi-standard 4K image/video codec and high performance COFDM based wireless transceiver for wireless audio/video streaming.

The quad-core ARM Cortex-A7 CPU together with quad CEVA XM4 DSP cores build up a high performance computing array. Two AR9201 chips can also be connected via PCIe interface and form a bigger computing array if higher performance is desired. Customized OpenCV API and various basic building blocks inside deep neuro networks (like Faster-RCNN or YOLO) are ported on this computing array. Intelligent machine vision applications can be easily implemented by using the SDK associated with AR9201 hardware platform.

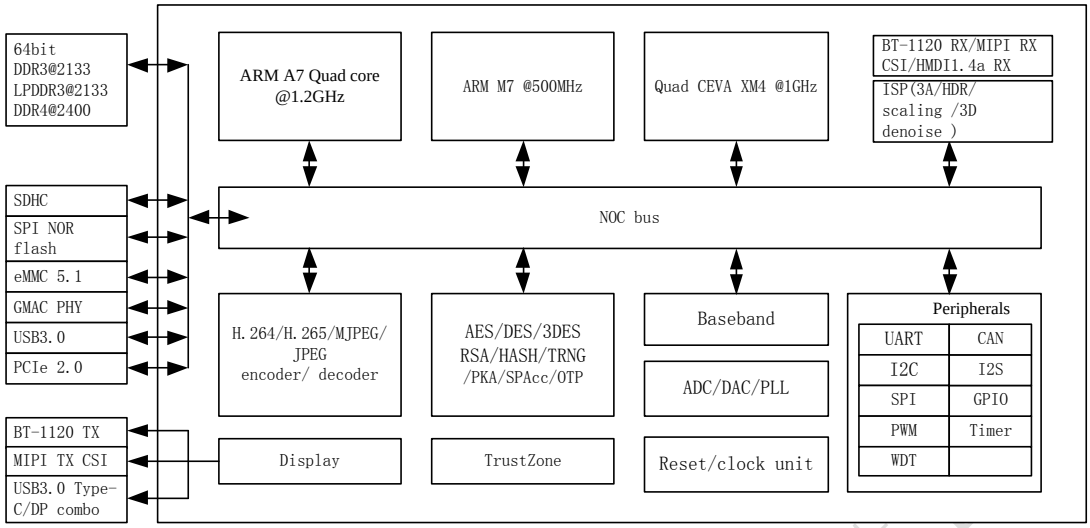
Cortex-M7 TCM (Tightly Coupled Memory) and all the common peripherals are integrated in the MCU subsystem. All these abundant features can meet the most industrial control system such as drone flight control, robot control and etc.

The video subsystem is comprised of 8-way MIPI clock ports, a 4K UHD ISP (Image Signal Processor), multi-standard video codecs, one video display module and various video/audio output ports such as DisplayPort, MIPI or BT-1120. The powerful ISP module can handle 8 1080p@30fps or 2 4Kx2K@30fps Bayer RAW 14-bit input data in real-time. Three types of image/video standard are supported by three dedicated hardware codecs: MJPEG/JPEG, H.264 and H.265.

The in-house baseband modem is a bi-directional communication IP for the purpose of remote control and high definition video transmission or bi-directional high definition video transmission. One AP can support max to four nodes for the bi-directional reliable transmission with long distance and high throughput. This IP supports RF transceiver named AR8003s provided by Artosyn which can support 2.4G and 5G bands.

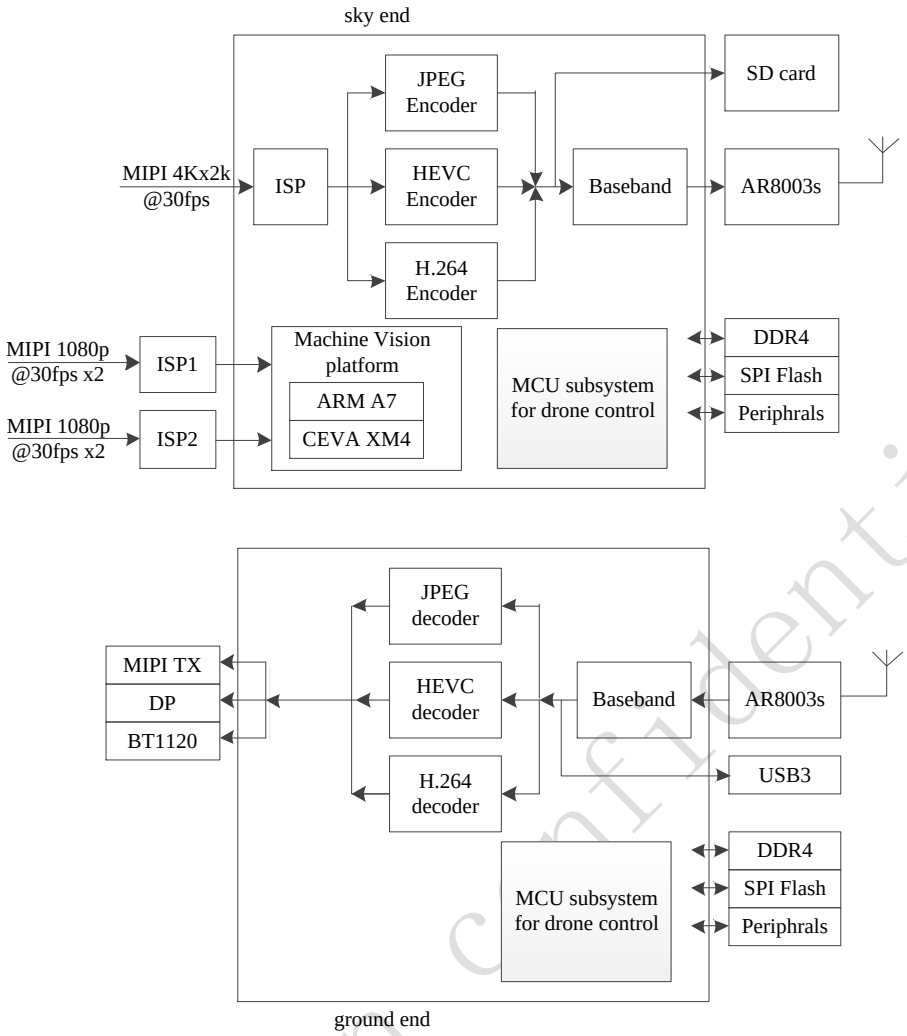
In house image signal processor (ISP) design can support standard sensor data processing and provide basic function such as auto white balance(AWB),automatic exposure(AE),de-mosaic, defected pixel correction(DPC) as well as advanced functions such as wide dynamic range(WDR),dynamic range compression(DRC),both RAW de-noise and 3D de-noise.

2. Block Diagram

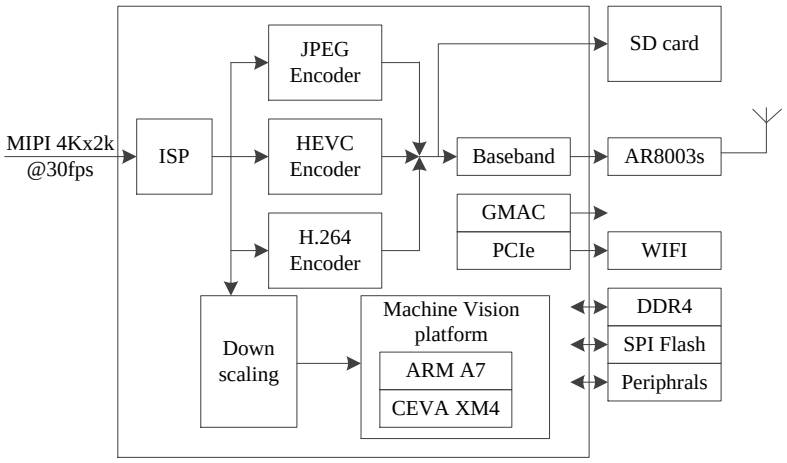


3. Example Application Solution

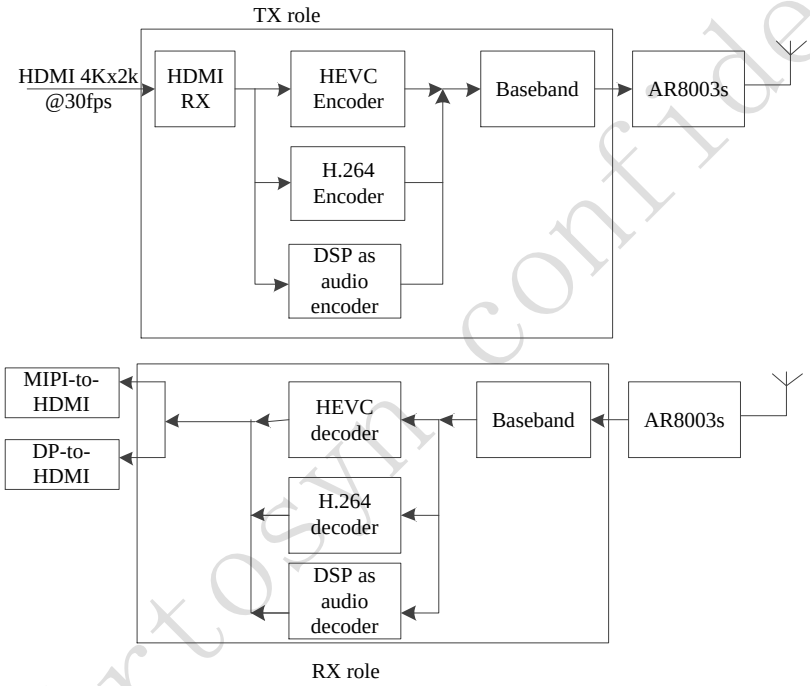
- All-in-one Drone solution for remote control, wireless UHD video streaming and intelligent machine vision for automatic object detection and obstacle avoidance



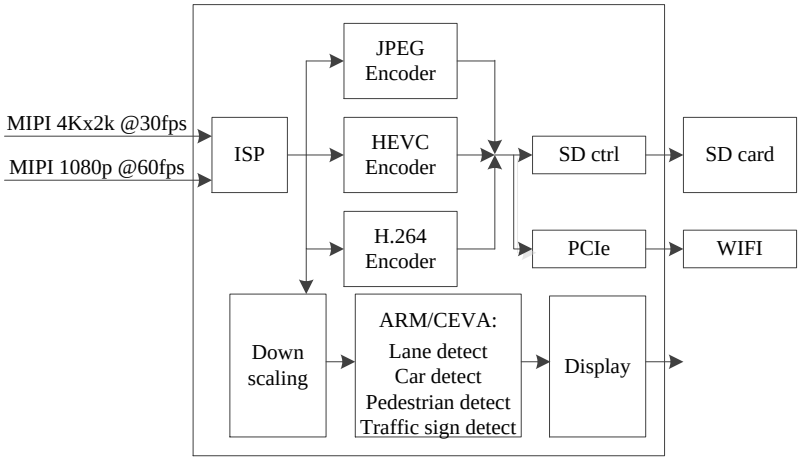
- UHD (4Kx2K@30fps) wired/wireless security camera



- Wireless HDMI transmitter/receiver dongle



- High end car driving recorder



4. Features

- **Application Processor Core**
  - 1.2GHz ARM Cortex-A7 quad-core, each core with 32KB I-cache, 32KB D-cache
  - 512KB L2 cache
  - Neon acceleration and double precision FPU
  - Embedded Trace data interface (16KB ETB) for ARM-DS5 debugger
  - DVFS control
- **MCU core**
  - 500MHz ARM Cortex-M7 CPU, 16Kbyte I-cache, 16KB D-cache
  - 128KB ITCM and 64KB DTCM
  - Double precision FPU
- **CEVA DSP core**
  - 4 x high performance CEVA XM4 Cores at 1000MHz
  - 32KB PTCM, 32KB I-Cache and 128K DTCM for each DSP core
  - 2M-Byte shared on-chip SRAM
- **Video Codec Format**
  - H.264 BP/MP/HP encoding and decoding
  - H.265 MAIN/MAIN10 @L5.0 High-tier encoding and decoding
  - MJPEG/JPEG Extended Sequential encoding and decoding
- **Video Codec Performance**
  - Software configurable video codec, either as encoder or as decoder
  - Real-time multi-stream H.264/H.265 encoding or decoding:
    - H.264: 1080P@60fps
    - 4Kx2K@30fps+1080p@30fps
  - MJPEG/JPEG encoding/decoding at 4Kx2K@30fps
  - MJPEG/JPEG encoding and decoding
- **ISP**
  - Input Video resolution ranging from 4152x2174@ 60fps to 480x240
  - Both spatial denoising and temporal denoising
  - Adjustable 3A functions
  - Digital WDR and tone mapping support
  - Lens Shading correction
  - Green Imbalance correction
  - Bayer RAW data input with max 20bit-width
  - 3 different resolution video outputs from the single source
- **Audio Encoding/Decoding**
  - I2S interface for external audio input
  - Software support for Voice/music encoding/decoding complying with multiple protocols such as G.711, ADPCM, G.726 and MP3.
- **Security Engine**
  - AES and DES encryption and decryption algorithms implemented by using hardware

- RSA1024/2048/4096 signature verification algorithm implemented by using hardware
- Hash MD5, SHA-1, SHA-256, SHA-512 and SHA-512/256 tamper proofing algorithms implemented by using hardware
- ARM TrustZone solution for hardware-based security
- Security CPU solution for secure boot and secure storage.

Video Interfaces

Video input

- 2 BT-656 or BT-1120 digital parallel input interfaces, up to 1080p@60fps
- 8 MIPI CSI-RX input ports, 2 data-lane for each port, up to 4Kx2K@30fps
- 1 HDMI 1.4 RX interface up to 4Kx2K@30fps

Video output

- 1 DisplayPort output interface up to 4Kx2K@30fps
- 1 BT-1120 digital parallel output interface up to 1080p@60fps, sharing pins with BT-1120 input interface
- 1 MIPI CSI-TX output interface up to 4Kx2K@30fps

Baseband

- 2T4R with 2.5MHz/5MHz/10MHz/20MHz/40MHz bandwidth
- BPSK/QPSK/16QAM/64QAM/256QAM modulation
- LDPC encoder with 1/2, 2/3, 3/4 code rate
- Max down link rate at 100Mbps
- 2.4G/5.8G uplink/downlink communication
- One AP support max to four nodes

Analog

- One 8-1 10bit SAR ADC
- Two 10bit SAR ADCs
- Four 12bit DACs
- Eight 12bit ADCs

Peripherals

- 9 UARTs
- 2 Watch dog timers
- 20 timers，10 of which have PWM output
- 4 CAN bus interface
- 5 I2C interfaces, can be configured as either master or slave by software
- 4 SPI masters(2x1-1, 2x1-5), 2 SPI slave
- 4 I2S 4bit interfaces
- 147 GPIO, shared with other functions.
- 2 AXI DMA controller
- One AHB DMA controller
- USB 3.0 DRD controller and PHY.
- USB 3.0 /Type-C / DisplayPort combo interface
- 10/100/1000M Ethernet RGMII interface
- 2-lane PCIe 2.0, can be configured as EP or RC mode

External Memory Interfaces

DDR4/DDR3/LPDDR3 interface

- 32/64-bit DDR4 interface up to DDR4 2400
- 32/64-bit DDR3 interface up to DDR3 2133
- 32/64-bit LPDDR3 interface up to LPDDR3 2133
- **SPI NOR flash interface**
- 1-/2-/4-wire mode
- 3-byte or 4-byte address mode
- Maximum capacity of 256 MB
- **eMMC 5.1 interface with 64GB max capacity**
- **Secure Boot from internal ROM with eMMC flash or SPI NOR flash.**

Physical Specification

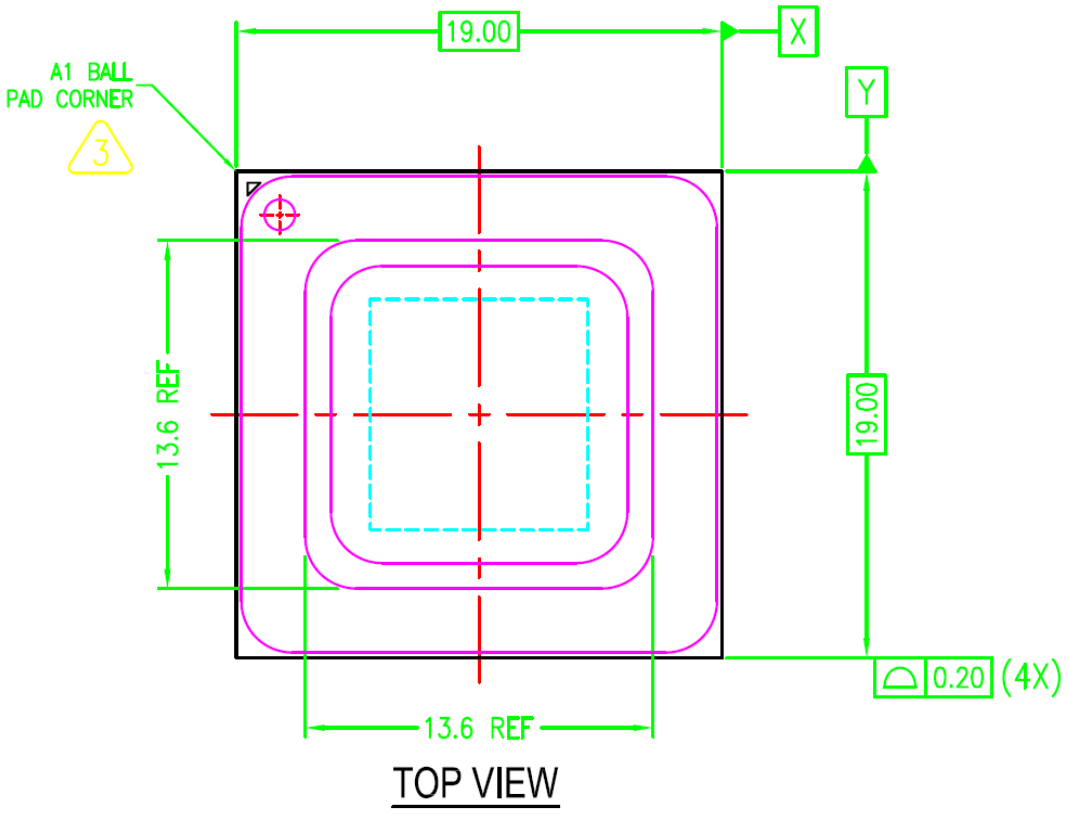
- **Power consumption**
- 3W typical power consumption in the 4Kx2K scenario
- Multiple power domains for power saving
- **Operating voltages**
- 0.9V core voltage
- 1.8V I/O voltage
- 1.2V/1.2V/1.5V for DDR4/LPDDR3/DDR3
- 3.3V I/O voltage
- **Package**
- FCBGA
- Body size of 19mm x19mm
- Ball pitch of 0.65mm

5. Package Information

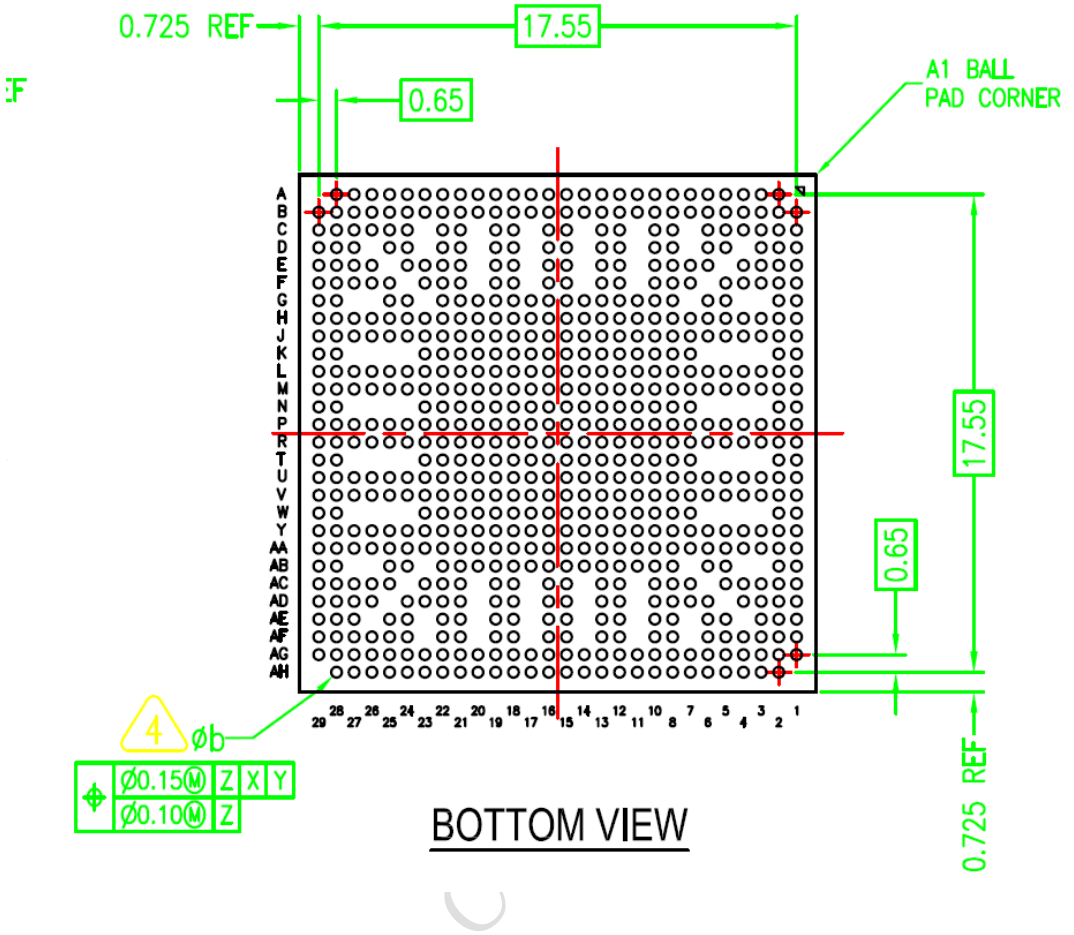
5.1 Ordering information

Part No	Package	Device special feature
AR9201	19X19 mm^2 Ball pitch 0.65mm FCBGA684	

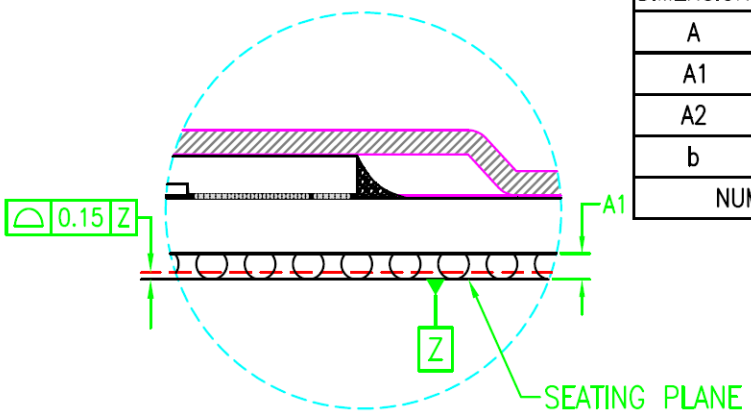
5.2 Dimension



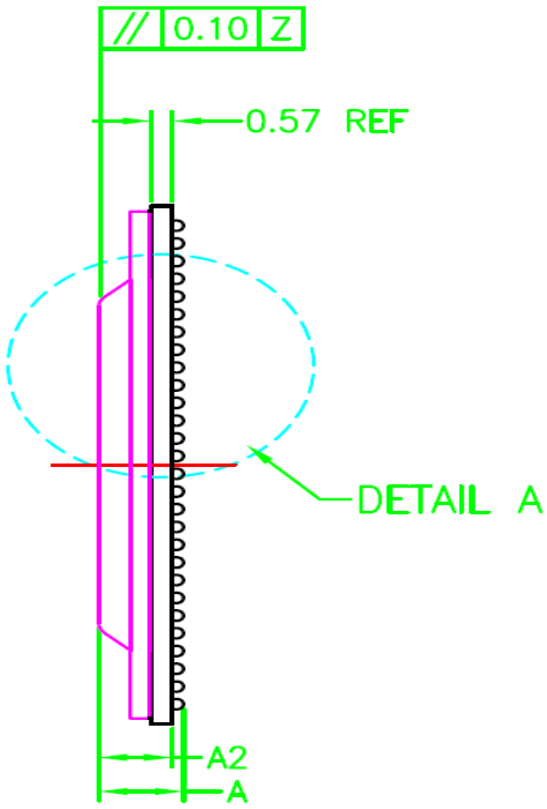
TOP VIEW



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	2.061	2.277	2.492
A1	0.257	0.307	0.357
A2	1.804	1.970	2.135
b	0.350	0.400	0.450
NUMBER OF BALLS 684			



DETAIL A
ROTATED 90°



SIDE VIEW

NOTES:

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M–1994.
2. TERMINAL POSITIONS DESIGNATION PER JESD 95–1, SPP–010.
3. CORNER DETAILS PER STATS ChipPAC OPTION.
4. REFLOW BALL DIAMETER.
5. COMPLIANT TO JEDEC REGISTERED OUTLINE MS–034, NO EXACT VARIATION AND WITH EXCEPTION TO DIM 'A'.
6. RAW SOLDER BALL SIZE DURING ASSEMBLY IS ø0.400MM.

5.3 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		DDR_DQ40	DDR_DQ41	DDR_DQ43	DDR_DQS5N	DDR_DQ44	DDR_DM5	DDR_DQ47	DDR_DQ48	DDR_DQ50	DDR_DQS6N	DDR_DQ52	DDR_DQ51	DDR_DQ54

B	DDR_CK	DDR_CKN	VSS	DDR_DQ42	DDR_DQS5	VSS	DDR_DQ45	DDR_DQ46	VSS	DDR_DQ49	DDR_DQS6	VSS	DDR_DQ53	DDR_DM6
C	DDR_A17	DDR_A16	DDR_CKE1	DDR_RAM_RSTN	DDR_ATO	DDR_DQ34		DDR_DQS4	DDR_DQ39		DDR_DQ57	DDR_DQS7N		DDR_DQ61
D	DDR_A14	DDR_A15	DDR_CKE0		DDR_DTO0	DDR_DQ33		DDR_DQS4N	DDR_DQ36		DDR_DQ56	DDR_DQS7		DDR_DQ60
E	DDR_A12	DDR_A13	DDR_CSN0	DDR_CSN1		DDR_DQ32	DDR_DQ35	VSS	DDR_DQ38		VSS	DDR_DQ58		VSS
F	DDR_A10	VSS	DDR_BG1	DDR_BG0	VSS		DDR_DTO1	DDR_PLL_VDD	DDR_DQ37		DDR_DM4	DDR_DQ59		DDR_DQ62
G	DDR_A11	DDR_A9			DDR_ODT0	DDR_ALERTN		DDR_PLL_VDD	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	VSS	VSS	PCIE_VP
H	DDR_A7	DDR_A6	DDR_BA0	DDR_PARITY	DDR_ODT1	DDR_VREFI	DDR_VDDQ	DDR_VDDQ	VSS	VSS	VSS	DDR_AVSS1V8	DDR_AVDD18	CA7_AVDD1V8
J	DDR_A2	VSS	DDR_A8	DDR_BA1	VSS	DDR_ACTN	DDR_VDDQ	DDR_VDDQ	VSS	VSS	VSS	VSS	CA7_AVSS1V8	OTP_VDDIO1V8
K	DDR_A3	DDR_A5					DDR_VREFO_0	DDR_VDDQ	VSS	VDD	CA7_VDD	CA7_VDD	CA7_VDD	VDD
L	DDR_A4	DDR_A1	DDR_DQ30	DDR_DQ31	DDR_DM3	DDR_ZQ	DDR_VDDQ	DDR_VDDQ	VSS	VDD	CA7_VDD	VSS	VSS	VSS
M	DDR_A0	VSS	DDR_DQ28	DDR_DQ29	VSS	DDR_VREFI_ZQ	DDR_VREFO_1	DDR_VDDQ	VSS	VDD	CA7_VDD	VSS	VSS	VSS
N	DDR_DQ23	DDR_DM2					DDR_VDDQ	VSS	VSS	VDD	VDD	VDD	VDD	VDD
P	DDR_DQ21	DDR_DQ22	DDR_DQS3N	DDR_DQS3	DDR_DQ27	DDR_DQ26	DDR_VDDQ	VSS	VSS	VDD	VDD	VDD	VDD	VDD

15	16	17	18	19	20	21	22	23	24	25	26	27	28	
DDR_DQ55	PCIE_TX1P	PCIE_RX1P	PCIE_RX0P	PCIE_TX0P	TYPEC_REXT	TYPEC_CC1	TYPEC_REXT_CC	XTAL1	QDAC_OUTN_A	IDAC_OUTN_A	IADC_VINN_A	QADC_VINN_A		A
VSS	PCIE_TX1N	PCIE_RX1N	PCIE_RX0N	PCIE_TX0N	TYPEC_VBUS	TYPEC_CC2	CLKREF_SEL_PAD	XTAL2	QDAC_OUTP_A	IDAC_OUTP_A	IADC_VINP_A	QADC_VINP_A	AD_IN_2	B
DDR_DQ63		TYPEC_AUXP	VSS		TYPEC_TXRX2P	VSS		RSSI_2	PDET_A_5G	PDET_A_2G	AD_IN_3	QADC_VINP_B	QADC_VINN_B	C

TYPEC_AUX_PUPDN		TYPEC_TX0P	TYPEC_AUXN		TYPEC_TXRX2N	AD_IN_5		PDET_B_5G	PDET_B_2G		RSSI_1	IADC_VINP_B	IADC_VINN_B	D
TYPEC_AUX_PDPUP		TYPEC_TX0N	TYPEC_TXRX1N		TYPEC_TX3N	AD_IN_6	AD_IN_1	AD_IN_0		IADC_VINP_C	IADC_VINN_C	IDAC_OUTP_B	IDAC_OUTN_B	E
DDR_DM7		VSS	TYPEC_TXRX1P		TYPEC_TX3P	AD_IN_4	I2C_SCLK4_PAD		I2C_SDA3_PAD	QADC_VINP_C	QADC_VINN_C	QDAC_OUTP_B	QDAC_OUTN_B	F
PCIE_VPH	PCIE_RESREF	TYPEC_AVDD_VH_3V3	TYPEC_AVDD_H_1V8	AVDD1V8_OSC	AVSS_OSC	AD_IN_7		GBE_RST_PAD	I2C_SDA4_PAD			IADC_VINP_D	IADC_VINN_D	G
VSS	PCIE_VPTX	TYPEC_AVDD	TYPEC_AVDD_CLK	VSS	AVSS_A	AVSS_A	PWM0_PAD	GBE_INT_PAD	I2C_SCLK3_PAD	EMMC_D0_PAD	EMMC_D1_PAD	QADC_VINP_D	QADC_VINN_D	H
VSS	VSS	VSS	TYPEC_AVDD	VSS	AVDD1V8_A	AVDD1V8_A	PWM1_PAD	GBE_CLK_PAD	VSS	EMMC_D2_PAD	EMMC_D3_PAD	EMMC_CCMD_PAD	EMMC_CLKOUT_PAD	J
VDD	VDD	VDD	VDD	VDD	AVSS_PLL	AVDD1V8_PLL	EMMC_PWR_PAD					EMMC_D4_PAD	EMMC_D5_PAD	K
VSS	VSS	VDD	VDD	VSS	VDD18_EMMC_0	VDD3_EMMC	PWM2_PAD	SPI_M1_DO_PAD	SPI_M1_DI_PAD	GBE_MDC_PAD	GBE_TXC_PAD	EMMC_D7_PAD	EMMC_D6_PAD	L
VSS	VSS	VDD	VDD	VSS	VDD18_EMMC_1	VDD3_3_RGM	PWM3_PAD	SPI_M1_SCLK_PAD	SPI_M1_CSN_PAD	GBE_MDIO_PAD	GBE_TXEN_PAD	GBE_TXD1_PAD	GBE_TXD0_PAD	M
VDD	VDD	VDD	VDD	VDD	VSS	VDD3_3_RGM	PWM4_PAD					GBE_TXD2_PAD	GBE_TXD3_PAD	N
VDD	VDD	VDD	VDD	VDD	VSS	VSS	UART_SIN4_PAD	SPI_M2_CS0N_PAD	SPI_M2_DI_PAD	SPI_M0_CSN_PAD	VSS	GBE_RXEN_PAD	GBE_RXC_PAD	P

R	DDR_DQ20	VSS	DDR_DQ25	DDR_DM0	VSS	DDR_DQ24	DDR_VDDQ	DDR_VDDQ	VSS	VDD	CEVA_VDD	VSS	VSS	VSS
T	DDR_DQS2N	DDR_DQS2					DDR_VDDQ	VSS	VSS	CEVA_VDD	CEVA_VDD	VSS	VSS	VSS

U	DDR_DQ19	DDR_DQ17	DDR_DQ7	DDR_DQ5	DDR_DQ0	DDR_VDDQ	DDR_VDDQ	VSS	VSS	CEVA_VDD	CEVA_VDD	CEVA_VDD	CEVA_VDD	CEVA_VDD
V	DDR_DQ16	VSS	DDR_DQ6	DDR_DQ1	VSS	UART_RX3_PAD	VDD18_R	VSS	VSS	CEVA_VDD	CEVA_VDD	CEVA_VDD	CEVA_VDD	CEVA_VDD
W	DDR_DQ18	DDR_DQ15					UART_TX3_PAD	VSS	CEVA_VDD	CEVA_VDD	CEVA_VDD	VSS	VSS	VSS
Y	DDR_DM1	DDR_DQ14	DDR_DQS0N	DDR_DQS0	DDR_DQ2	UART_TX0_PAD	VSS	VSS	CEVA_VDD	CEVA_VDD	CEVA_VDD	VSS	VSS	VSS
AA	DDR_DQ13	VSS	DDR_DQ4	DDR_DQ3	VSS	UART_TX1_PAD	UART_RX1_PAD	VSS	VSS	VSS	VSS	VSS	VDD	VDD
AB	DDR_DQ12	DDR_DQ11			UART_RX2_PAD	UART_TX2_PAD		TEST_MODE_EN_PAD	VSS	VSS	MIPI_AVDD1V8	MIPI_AVDD1V8	CEVA_AVDD1V8	CEVA_AVSS1V8
AC	DDR_DQS1N	DDR_DQS1	I2C_SCLK2_PAD	I2C_SCLK1_PAD	I2C_SDA2_PAD		UART_RX0_PAD	RSTN_PAD	MIPI_AGND		MIPI_AGND	MIPI1_REXT		MIPI_AGND
AD	DDR_DQ10	VSS	I2C_SCLK0_PAD	I2C_SDA1_PAD		GP0_PAD	GP2_PAD	MIPI7_REXT	MIPI6_REXT		MIPI4_REXT	MIPI1_CLKP		MIPI0_CLKP
AE	DDR_DQ9	DDR_DQ8	I2C_SDA0_PAD		MIPI7_CLKN	MIPI6_CLKN		MIPI5_REXT	MIPI5_CLKN		MIPI4_CLKN	MIPI1_CLKN		MIPI0_CLKN
AF	GP5_PAD	GP4_PAD	GP7_PAD	MIPI_AGND	MIPI7_CLKP	MIPI6_CLKP		MIPI_AGND	MIPI5_CLKP		MIPI4_CLKP	MIPI_AGND		MIPI_AGND
AG	GP6_PAD	GP1_PAD	MIPI7_D1P	MIPI7_D0P	MIPI6_D1P	MIPI6_D0P	MIPI5_D1P	MIPI5_D0P	MIPI4_D1P	MIPI4_D0P	MIPI1_D0P	MIPI1_D1P	MIPI0_D1P	MIPI0_D0P
AH		GP3_PAD	MIPI7_D1N	MIPI7_D0N	MIPI6_D1N	MIPI6_D0N	MIPI5_D1N	MIPI5_D0N	MIPI4_D1N	MIPI4_D0N	MIPI1_D0N	MIPI1_D1N	MIPI0_D1N	MIPI0_D0N
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

VSS	VSS	VDD	VDD	VSS	VDD18_SD_1	VDD18_SD_0	UART_SOUT4_PAD	SPI_M2_SCLK_PAD	SPI_M2_DO_PAD	SPI_M0_DI_PAD	SPI_M0_SCLK_PAD	GBE_RXD1_PAD	GBE_RXD0_PAD	R
VSS	VSS	VDD	VDD	VSS	VSS	VDD3_	PWM5_P					GBE_RX	GBE_RXD2	T

						SD	AD					D3_PAD	_PAD	
VDD	VDD	VDD	VDD	VDD	VSS	VSS	PWM6_PAD	PWM7_PAD	SPI_MS3_DI_PAD	SPI_M0_DO_PAD	SPI_MS3_SCLK_PAD	SD_CCMD_PAD	SD_CCLK_OUT_PAD	U
VDD	VDD	VDD	VDD	VDD	VSS	VDD18	PWM8_PAD	SPI_MS3_DO_PAD	SPI_MS3_CS1N_PAD	SPI_MS3_CS3N_PAD	SPI_MS3_CS2N_PAD	SD_CARD_WPRT_PAD	SD_CARD_DETECT_N_PAD	V
VSS	VSS	VDD	VDD	VSS	VSS	VDD18	PWM9_PAD					SD_CDATA_1_PAD	SD_CDATA_0_PAD	W
VSS	VSS	VDD	VDD	VDD	VSS	VDD18	SPI_MS3_CS0N_PAD	SPI_MS3_CS4N_PAD	I2S_WS2_PAD	I2S_SDI1_PAD	VSS	SD_CDATA_3_PAD	SD_CDATA_2_PAD	Y
VDD	VDD	VDD	USB_DVDD0V9	USB_VP0V9	VSS	VSS	I2S_CLK2_PAD	I2S_SDI2_PAD	I2S_SDO2_PAD	I2S_WS1_PAD	I2S_SDI0_PAD	I2S_WS0_PAD	I2S_CLK0_PAD	AA
VSS	VSS	VSS	USB_VDDH3V3	VP_HDMI	VP3V3_TERM_HDMI	HDMI_RREF		I2S_WS3_PAD	I2S_SDI3_PAD			I2S_SDO1_PAD	I2S_SDO0_PAD	AB
MIPI0_REXT		MIPI2_REXT	USB_VDD3V3		VPH_HDMI	VSS	QE0_4_PAD		I2S_SDO3_PAD	I2S_CLK3_PAD	I2S_CLK1_PAD	VSYNC1_PAD	PCLK1_PAD	AC
MIPI3_REXT		USB_ID	USB_RESREF		USB_OC_PAD	HDMI_SCL_PAD	QE0_7_PAD	QE0_2_PAD		DE0_PAD	PCLK0_PAD	QE1_1_PAD	DE1_PAD	AD
MIPI3_CLKN		MIPI2_CLKN	USB_VBUS		USB_PWR_PAD	HDMI_SDA_PAD		QE0_5_PAD	QE0_3_PAD		HSYNC0_PAD	QE1_3_PAD	HSYNC1_PAD	AE
MIPI3_CLKP		MIPI2_CLKP	MIPI_AGND		HDMI_CEC_PAD	VSS		QE0_6_PAD	VSS	QE0_1_PAD	VSYNC0_PAD	QE1_5_PAD	QE1_0_PAD	AF
MIPI3_D1P	MIPI3_D0P	MIPI2_D1P	MIPI2_D0P	USB_DN	USB_TX0N	USB_RX0N	HDMI_RX2N	HDMI_RX1N	HDMI_RX0N	HDMI_RXCN	QE0_0_PAD	QE1_6_PAD	QE1_2_PAD	AG
MIPI3_D1N	MIPI3_D0N	MIPI2_D1N	MIPI2_D0N	USB_DP	USB_TX0P	USB_RX0P	HDMI_RX2P	HDMI_RX1P	HDMI_RX0P	HDMI_RXCP	QE1_4_PAD	QE1_7_PAD		AH
15	16	17	18	19	20	21	22	23	24	25	26	27	28	

5.4 Pin Order

Total: 684 pins.

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A10	DDR_DQ50	AE6	MIPI6_CLKN	D20	TYPEC_TXRX2N	K12	CA7_VDD	R24	SPI_M2_DO_PAD
A11	DDR_DQS6N	AE8	MIPI5_REXT	D21	AD_IN_5	K13	CA7_VDD	R25	SPI_M0_DI_PAD
A12	DDR_DQ52	AE9	MIPI5_CLKN	D23	PDET_B_5G	K14	VDD	R26	SPI_M0_SCLK_PAD
A13	DDR_DQ51	AF1	GP5_PAD	D24	PDET_B_2G	K15	VDD	R27	GBE_RXD1_PAD
A14	DDR_DQ54	AF11	MIPI4_CLKP	D26	RSSI_1	K16	VDD	R28	GBE_RXD0_PAD
A15	DDR_DQ55	AF12	MIPI_AGND	D27	IADC_VINP_B	K17	VDD	R3	DDR_DQ25
A16	PCIE_TX1P	AF14	MIPI_AGND	D28	IADC_VINN_B	K18	VDD	R4	DDR_DM0
A17	PCIE_RX1P	AF15	MIPI3_CLKP	D3	DDR_CKE0	K19	VDD	R5	VSS
A18	PCIE_RX0P	AF17	MIPI2_CLKP	D5	DDR_DTO0	K2	DDR_A5	R6	DDR_DQ24
A19	PCIE_TX0P	AF18	MIPI_AGND	D6	DDR_DQ33	K20	AVSS_PLL	R7	DDR_VDDQ
A2	DDR_DQ40	AF2	GP4_PAD	D8	DDR_DQS4N	K21	AVDD1V8_PLL	R8	DDR_VDDQ
A20	TYPEC_REXT	AF20	HDMI_CEC_PAD	D9	DDR_DQ36	K22	EMMC_PWR_PAD	R9	VSS
A21	TYPEC_CC1	AF21	VSS	E1	DDR_A12	K27	EMMC_D4_PAD	T1	DDR_DQS2N
A22	TYPEC_REXT_CC	AF23	QE0_6_PAD	E11	VSS	K28	EMMC_D5_PAD	T10	CEVA_VDD
A23	XTAL1	AF24	VSS	E12	DDR_DQ58	K7	DDR_VREFO_0	T11	CEVA_VDD
A24	QDAC_OUTN_A	AF25	QE0_1_PAD	E14	VSS	K8	DDR_VDDQ	T12	VSS
A25	IDAC_OUTN_A	AF26	VSYNC0_PAD	E15	TYPEC_AUX_PDPUP	K9	VSS	T13	VSS
A26	IADC_VINN_A	AF27	QE1_5_PAD	E17	TYPEC_TX0N	L1	DDR_A4	T14	VSS
A27	QADC_VINN_A	AF28	QE1_0_PAD	E18	TYPEC_TXRX1N	L10	VDD	T15	VSS
A3	DDR_DQ41	AF3	GP7_PAD	E2	DDR_A13	L11	CA7_VDD	T16	VSS
A4	DDR_DQ43	AF4	MIPI_AGND	E20	TYPEC_TX3N	L12	VSS	T17	VDD
A5	DDR_DQS5N	AF5	MIPI7_CLKP	E21	AD_IN_6	L13	VSS	T18	VDD
A6	DDR_DQ44	AF6	MIPI6_CLKP	E22	AD_IN_1	L14	VSS	T19	VSS
A7	DDR_DM5	AF8	MIPI_AGND	E23	AD_IN_0	L15	VSS	T2	DDR_DQS2
A8	DDR_DQ47	AF9	MIPI5_CLKP	E25	IADC_VINP_C	L16	VSS	T20	VSS
A9	DDR_DQ48	AG1	GP6_PAD	E26	IADC_VINN_C	L17	VDD	T21	VDD3_SD

AA1	DDR_DQ13	AG10	MIPI4_D0P	E27	IDAC_OUTP_B	L18	VDD	T22	PWM5_PAD
AA10	VSS	AG11	MIPI1_D0P	E28	IDAC_OUTN_B	L19	VSS	T27	GBE_RXD3_PAD
AA11	VSS	AG12	MIPI1_D1P	E3	DDR_CSN0	L2	DDR_A1	T28	GBE_RXD2_PAD
AA12	VSS	AG13	MIPI0_D1P	E4	DDR_CSN1	L20	VDD18_EMMC_0	T7	DDR_VDDQ
AA13	VDD	AG14	MIPI0_D0P	E6	DDR_DQ32	L21	VDD3_EMMC	T8	VSS
AA14	VDD	AG15	MIPI3_D1P	E7	DDR_DQ35	L22	PWM2_PAD	T9	VSS
AA15	VDD	AG16	MIPI3_D0P	E8	VSS	L23	SPI_M1_DO_PAD	U1	DDR_DQ19
AA16	VDD	AG17	MIPI2_D1P	E9	DDR_DQ38	L24	SPI_M1_DI_PAD	U10	CEVA_VDD
AA17	VDD	AG18	MIPI2_D0P	F1	DDR_A10	L25	GBE_MDC_PAD	U11	CEVA_VDD
AA18	USB_DVDD0V9	AG19	USB_DN	F11	DDR_DM4	L26	GBE_TXC_PAD	U12	CEVA_VDD
AA19	USB_VP0V9	AG2	GP1_PAD	F12	DDR_DQ59	L27	EMMC_D7_PAD	U13	CEVA_VDD
AA2	VSS	AG20	USB_TX0N	F14	DDR_DQ62	L28	EMMC_D6_PAD	U14	CEVA_VDD
AA20	VSS	AG21	USB_RX0N	F15	DDR_DM7	L3	DDR_DQ30	U15	VDD
AA21	VSS	AG22	HDMI_RX2N	F17	VSS	L4	DDR_DQ31	U16	VDD
AA22	I2S_CLK2_PAD	AG23	HDMI_RX1N	F18	TYPEC_TXRX1P	L5	DDR_DM3	U17	VDD
AA23	I2S_SDI2_PAD	AG24	HDMI_RX0N	F2	VSS	L6	DDR_ZQ	U18	VDD
AA24	I2S_SDO2_PAD	AG25	HDMI_RXCN	F20	TYPEC_TX3P	L7	DDR_VDDQ	U19	VDD
AA25	I2S_WS1_PAD	AG26	QE0_0_PAD	F21	AD_IN_4	L8	DDR_VDDQ	U2	DDR_DQ17
AA26	I2S_SDI0_PAD	AG27	QE1_6_PAD	F22	I2C_SCLK4_PAD	L9	VSS	U20	VSS
AA27	I2S_WS0_PAD	AG28	QE1_2_PAD	F24	I2C_SDA3_PAD	M1	DDR_A0	U21	VSS
AA28	I2S_CLK0_PAD	AG3	MIPI7_D1P	F25	QADC_VINP_C	M10	VDD	U22	PWM6_PAD
AA3	DDR_DQ4	AG4	MIPI7_D0P	F26	QADC_VINN_C	M11	CA7_VDD	U23	PWM7_PAD
AA4	DDR_DQ3	AG5	MIPI6_D1P	F27	QDAC_OUTP_B	M12	VSS	U24	SPI_MS3_DI_PAD
AA5	VSS	AG6	MIPI6_D0P	F28	QDAC_OUTN_B	M13	VSS	U25	SPI_M0_DO_PAD
AA6	UART_TX1_PAD	AG7	MIPI5_D1P	F3	DDR_BG1	M14	VSS	U26	SPI_MS3_SCLK_PAD
AA7	UART_RX1_PAD	AG8	MIPI5_D0P	F4	DDR_BG0	M15	VSS	U27	SD_CCMD_PAD
AA8	VSS	AG9	MIPI4_D1P	F5	VSS	M16	VSS	U28	SD_CCLK_OUT_PAD
AA9	VSS	AH10	MIPI4_D0N	F7	DDR_DTO1	M17	VDD	U3	DDR_DQ7
AB1	DDR_DQ12	AH11	MIPI1_D0N	F8	DDR_PLL_VDD	M18	VDD	U4	DDR_DQ5

AB10	VSS	AH12	MIPI1_D1N	F9	DDR_DQ37	M19	VSS	U5	DDR_DQ0
AB11	MIPI_AVDD1V8	AH13	MIPI0_D1N	G1	DDR_A11	M2	VSS	U6	DDR_VDDQ
AB12	MIPI_AVDD1V8	AH14	MIPI0_D0N	G10	DDR_VDDQ	M20	VDD18_EMMC_1	U7	DDR_VDDQ
AB13	CEVA_AVDD1V8	AH15	MIPI3_D1N	G11	DDR_VDDQ	M21	VDD33_RGM	U8	VSS
AB14	CEVA_AVSS1V8	AH16	MIPI3_D0N	G12	VSS	M22	PWM3_PAD	U9	VSS
AB15	VSS	AH17	MIPI2_D1N	G13	VSS	M23	SPI_M1_SCLK_PAD	V1	DDR_DQ16
AB16	VSS	AH18	MIPI2_D0N	G14	PCIE_VP	M24	SPI_M1_CSN_PAD	V10	CEVA_VDD
AB17	VSS	AH19	USB_DP	G15	PCIE_VPH	M25	GBE_MDIO_PAD	V11	CEVA_VDD
AB18	USB_VDDH3V3	AH2	GP3_PAD	G16	PCIE_RESREF	M26	GBE_TXEN_PAD	V12	CEVA_VDD
AB19	VP_HDMI	AH20	USB_TX0P	G17	TYPEC_AVDD_VH_3V3	M27	GBE_TXD1_PAD	V13	CEVA_VDD
AB2	DDR_DQ11	AH21	USB_RX0P	G18	TYPEC_AVDD_H_1V8	M28	GBE_TXD0_PAD	V14	CEVA_VDD
AB20	VP3V3_TERM_HDMI	AH22	HDMI_RX2P	G19	AVDD1V8_OSC	M3	DDR_DQ28	V15	VDD
AB21	HDMI_RREF	AH23	HDMI_RX1P	G2	DDR_A9	M4	DDR_DQ29	V16	VDD
AB23	I2S_WS3_PAD	AH24	HDMI_RX0P	G20	AVSS_OSC	M5	VSS	V17	VDD
AB24	I2S_SDI3_PAD	AH25	HDMI_RXCP	G21	AD_IN_7	M6	DDR_VREFI_ZQ	V18	VDD
AB27	I2S_SDO1_PAD	AH26	QE1_4_PAD	G23	GBE_RST_PAD	M7	DDR_VREFO_1	V19	VDD
AB28	I2S_SDO0_PAD	AH27	QE1_7_PAD	G24	I2C_SDA4_PAD	M8	DDR_VDDQ	V2	VSS
AB5	UART_RX2_PAD	AH3	MIPI7_D1N	G27	IADC_VINP_D	M9	VSS	V20	VSS
AB6	UART_TX2_PAD	AH4	MIPI7_D0N	G28	IADC_VINN_D	N1	DDR_DQ23	V21	VDD18
AB8	TEST_MODE_EN_PAD	AH5	MIPI6_D1N	G5	DDR_ODT0	N10	VDD	V22	PWM8_PAD
AB9	VSS	AH6	MIPI6_D0N	G6	DDR_ALERTN	N11	VDD	V23	SPI_MS3_DO_PAD
AC1	DDR_DQS1N	AH7	MIPI5_D1N	G8	DDR_PLL_VDD	N12	VDD	V24	SPI_MS3_CS1N_PAD
AC11	MIPI_AGND	AH8	MIPI5_D0N	G9	DDR_VDDQ	N13	VDD	V25	SPI_MS3_CS3N_PAD

AC12	MIPI1_REXT	AH9	MIPI4_D1N	H1	DDR_A7	N14	VDD	V26	SPI_MS3_CS2N_PAD
AC14	MIPI_AGND	B1	DDR_CK	H10	VSS	N15	VDD	V27	SD_CARD_WPRT_PAD
AC15	MIPI0_REXT	B10	DDR_DQ49	H11	VSS	N16	VDD	V28	SD_CARD_DETECT_N_PAD
AC17	MIPI2_REXT	B11	DDR_DQS6	H12	DDR_AVSS1V8	N17	VDD	V3	DDR_DQ6
AC18	USB_VDD3V3	B12	VSS	H13	DDR_AVDD18	N18	VDD	V4	DDR_DQ1
AC2	DDR_DQS1	B13	DDR_DQ53	H14	CA7_AVDD1V8	N19	VDD	V5	VSS
AC20	VPH_HDMI	B14	DDR_DM6	H15	VSS	N2	DDR_DM2	V6	UART_RX3_PAD
AC21	VSS	B15	VSS	H16	PCIE_VPTX	N20	VSS	V7	VDD18_R
AC22	QE0_4_PAD	B16	PCIE_TX1N	H17	TYPEC_AVDD	N21	VDD33_RGM	V8	VSS
AC24	I2S_SDO3_PAD	B17	PCIE_RX1N	H18	TYPEC_AVDD_CLK	N22	PWM4_PAD	V9	VSS
AC25	I2S_CLK3_PAD	B18	PCIE_RX0N	H19	VSS	N27	GBE_TXD2_PAD	W1	DDR_DQ18
AC26	I2S_CLK1_PAD	B19	PCIE_TX0N	H2	DDR_A6	N28	GBE_TXD3_PAD	W10	CEVA_VDD
AC27	VSYNC1_PAD	B2	DDR_CKN	H20	AVSS_A	N7	DDR_VDDQ	W11	CEVA_VDD
AC28	PCLK1_PAD	B20	TYPEC_VBUS	H21	AVSS_A	N8	VSS	W12	VSS
AC3	I2C_SCLK2_PAD	B21	TYPEC_CC2	H22	PWM0_PAD	N9	VSS	W13	VSS
AC4	I2C_SCLK1_PAD	B22	CLKREF_SEL_PAD	H23	GBE_INT_PAD	P1	DDR_DQ21	W14	VSS
AC5	I2C_SDA2_PAD	B23	XTAL2	H24	I2C_SCLK3_PAD	P10	VDD	W15	VSS
AC7	UART_RX0_PAD	B24	QDAC_OUTP_A	H25	EMMC_D0_PAD	P11	VDD	W16	VSS
AC8	RSTN_PAD	B25	IDAC_OUTP_A	H26	EMMC_D1_PAD	P12	VDD	W17	VDD
AC9	MIPI_AGND	B26	IADC_VINP_A	H27	QADC_VINP_D	P13	VDD	W18	VDD
AD1	DDR_DQ10	B27	QADC_VINP_A	H28	QADC_VINN_D	P14	VDD	W19	VSS
AD11	MIPI4_REXT	B28	AD_IN_2	H3	DDR_BA0	P15	VDD	W2	DDR_DQ15
AD12	MIPI1_CLKP	B3	VSS	H4	DDR_PARITY	P16	VDD	W20	VSS
AD14	MIPI0_CLKP	B4	DDR_DQ42	H5	DDR_ODT1	P17	VDD	W21	VDD18
AD15	MIPI3_REXT	B5	DDR_DQS5	H6	DDR_VREFI	P18	VDD	W22	PWM9_PAD
AD17	USB_ID	B6	VSS	H7	DDR_VDDQ	P19	VDD	W27	SD_CDATA_1_PAD
AD18	USB_RESREF	B7	DDR_DQ45	H8	DDR_VDDQ	P2	DDR_DQ22	W28	SD_CDATA_0_PAD
AD2	VSS	B8	DDR_DQ46	H9	VSS	P20	VSS	W7	UART_TX3_PAD
AD20	USB_OC_PAD	B9	VSS	J1	DDR_A2	P21	VSS	W8	VSS
AD21	HDMI_SCL_PA	C1	DDR_A17	J10	VSS	P22	UART_SIN4_P	W9	CEVA_VDD

	D						AD		
AD22	QE0_7_PAD	C11	DDR_DQ57	J11	VSS	P23	SPI_M2_CS0N_PAD	Y1	DDR_DM1
AD23	QE0_2_PAD	C12	DDR_DQS7N	J12	VSS	P24	SPI_M2_DI_PAD	Y10	CEVA_VDD
AD25	DE0_PAD	C14	DDR_DQ61	J13	CA7_AVSS1V8	P25	SPI_M0_CSN_PAD	Y11	CEVA_VDD
AD26	PCLK0_PAD	C15	DDR_DQ63	J14	OTP_VDDIO1V8	P26	VSS	Y12	VSS
AD27	QE1_1_PAD	C17	TYPEC_AUXP	J15	VSS	P27	GBE_RXEN_PAD	Y13	VSS
AD28	DE1_PAD	C18	VSS	J16	VSS	P28	GBE_RXC_PAD	Y14	VSS
AD3	I2C_SCLK0_PAD	C2	DDR_A16	J17	VSS	P3	DDR_DQS3N	Y15	VSS
AD4	I2C_SDA1_PAD	C20	TYPEC_TXRX2P	J18	TYPEC_AVDD	P4	DDR_DQS3	Y16	VSS
AD6	GP0_PAD	C21	VSS	J19	VSS	P5	DDR_DQ27	Y17	VDD
AD7	GP2_PAD	C23	RSSI_2	J2	VSS	P6	DDR_DQ26	Y18	VDD
AD8	MIPI7_REXT	C24	PDET_A_5G	J20	AVDD1V8_A	P7	DDR_VDDQ	Y19	VDD
AD9	MIPI6_REXT	C25	PDET_A_2G	J21	AVDD1V8_A	P8	VSS	Y2	DDR_DQ14
AE1	DDR_DQ9	C26	AD_IN_3	J22	PWM1_PAD	P9	VSS	Y20	VSS
AE11	MIPI4_CLKN	C27	QADC_VINP_B	J23	GBE_CLK_PAD	R1	DDR_DQ20	Y21	VDD18
AE12	MIPI1_CLKN	C28	QADC_VINN_B	J24	VSS	R10	VDD	Y22	SPI_MS3_CS0N_PAD
AE14	MIPI0_CLKN	C3	DDR_CKE1	J25	EMMC_D2_PAD	R11	CEVA_VDD	Y23	SPI_MS3_CS4N_PAD
AE15	MIPI3_CLKN	C4	DDR_RAM_RSTN	J26	EMMC_D3_PAD	R12	VSS	Y24	I2S_WS2_PAD
AE17	MIPI2_CLKN	C5	DDR_ATO	J27	EMMC_CCMD_PAD	R13	VSS	Y25	I2S_SDI1_PAD
AE18	USB_VBUS	C6	DDR_DQ34	J28	EMMC_CLKOUT_PAD	R14	VSS	Y26	VSS
AE2	DDR_DQ8	C8	DDR_DQS4	J3	DDR_A8	R15	VSS	Y27	SD_CDATA_3_PAD
AE20	USB_PWR_PAD	C9	DDR_DQ39	J4	DDR_BA1	R16	VSS	Y28	SD_CDATA_2_PAD
AE21	HDMI_SDA_PAD	D1	DDR_A14	J5	VSS	R17	VDD	Y3	DDR_DQS0N
AE23	QE0_5_PAD	D11	DDR_DQ56	J6	DDR_ACTN	R18	VDD	Y4	DDR_DQS0
AE24	QE0_3_PAD	D12	DDR_DQS7	J7	DDR_VDDQ	R19	VSS	Y5	DDR_DQ2
AE26	HSYNC0_PAD	D14	DDR_DQ60	J8	DDR_VDDQ	R2	VSS	Y6	UART_TX0_PAD
AE27	QE1_3_PAD	D15	TYPEC_AUX_P	J9	VSS	R20	VDD18_SD_1	Y7	VSS

			UPDN						
AE28	HSYNC1_PAD	D17	TYPEC_TX0P	K1	DDR_A3	R21	VDD18_SD_0	Y8	VSS
AE3	I2C_SDA0_PAD	D18	TYPEC_AUXN	K10	VDD	R22	UART_SOUT4 _PAD	Y9	CEVA_VDD
AE5	MIPI7_CLKN	D2	DDR_A15	K11	CA7_VDD	R23	SPI_M2_SCLK _PAD		

5.5 Pin Descriptions

5.5.1 System/GPIO interface (10)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
AC8	RSTN	in	N/A	1.8v digital IO	RSTN
AB8	TEST_MODE_EN	in	N/A	1.8v digital IO	TEST_MODE_EN
AD6	GP0	inout	PD	1.8v digital IO	JTAG_TRSTN/WTD_0/GPIO_A0_0
AG2	GP1	inout	PU	1.8v digital IO	GPIO_A0_1/PCIE_PERST_DET
AD7	GP2	inout	PU	1.8v digital IO	GPIO_A0_2/HDMI_HP
AH2	GP3	inout	PU	1.8v digital IO	GPIO_A0_3/UART_SIN5/SPI_M2_CS1N
AF2	GP4	inout	PU	1.8v digital IO	GPIO_A0_4/UART_SOUT5/SPI_M2_CS2N/ BB_SPI_~~DO~~ MOSI_A
AF1	GP5	inout	PU	1.8v digital IO	GPIO_A0_5/WTD_1/BB_SPI_ENB_A
AG1	GP6	inout	PU	1.8v digital IO	GPIO_A0_6/UART_SIN1/SPI_M2_CS3N/I2C_SDA4/BB_SPI_~~DI~~ MISO_A
AF3	GP7	inout	PU	1.8v digital IO	GPIO_A0_7/UART_SOUT1/SPI_M2_CS4N/I2C_SCLK4/BB_SPI_CLK_A

Share function

Name	Function_0	Function_1	Function_2	Function_3	Function_4	Function_5
GP0	JTAG_TRSTN	WTD_0			GPIO_A0_0	ATE_TEST _IN_16

GP1	GPIO_A0_1	PCIE_PERST_DET				ATE_TEST _IN_17
GP2	GPIO_A0_2	HDMI_HP				ATE_TEST _IN_18
GP3	GPIO_A0_3	UART_SIN5	SPI_M2_CS1N			ATE_TEST _IN_19
GP4	GPIO_A0_4	UART_SOUT5	SPI_M2_CS2N		BB_SPI_~~DO~~ MOSI_A	ATE_TEST _IN_20
GP5	GPIO_A0_5	WTD_1			BB_SPI_ENB_A	ATE_TEST _IN_21
GP6	GPIO_A0_6	UART_SIN1	SPI_M2_CS3N	I2C_SDA4	BB_SPI_~~DI~~ MISO_A	ATE_TEST _IN_22
GP7	GPIO_A0_7	UART_SOUT1	SPI_M2_CS4N	I2C_SCLK4	BB_SPI_CLK_A	ATE_TEST _IN_23

5.5.2 SPI Interface (20)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
P25	SPI_M0_DI	INOUT	PU	1.8v digital IO	SPI_M0_DI/GPIO_C0_0
R25	SPI_M0_DO	INOUT	N/A	1.8v digital IO	SPI_M0_DO/GPIO_C0_1
U25	SPI_M0_SCLK	INOUT	N/A	1.8v digital IO	SPI_M0_SCLK/GPIO_C0_2
R26	SPI_M0_CSN	INOUT	N/A	1.8v digital IO	SPI_M0_CSN/GPIO_C0_3
M24	SPI_M1_DI	INOUT	PU	1.8v digital IO	SPI_M1_DI/GPIO_C0_4/CAN_RXD2
L24	SPI_M1_DO	INOUT	PU	1.8v digital IO	SPI_M1_DO/GPIO_C0_5/CAN_TXD2
L23	SPI_M1_SCLK	INOUT	PU	1.8v digital IO	SPI_M1_SCLK/GPIO_C0_6/CAN_RXD3/TEST_JTAG_RTCK
M23	SPI_M1_CSN	INOUT	PU	1.8v digital IO	SPI_M1_CSN/GPIO_C0_7/CAN_TXD3/TEST_JTAG_TRSTN
P23	SPI_M2_DI	INOUT	PU	1.8v digital IO	SPI_M2_DI/GPIO_D0_0/BB_ANT_SW_SEL/TEST_JTAG_TDI
P24	SPI_M2_DO	INOUT	PU	1.8v digital IO	SPI_M2_DO/GPIO_D0_1/BB_ANT_SW_SEL_N/TEST_JTAG_TDO
R24	SPI_M2_SCLK	INOUT	PD	1.8v digital IO	SPI_M2_SCLK/GPIO_D0_2/BS_SEL/TEST_JTAG_TCK

R23	SPI_M2_CS0N	INOUT	PU	1.8v digital IO	SPI_M2_CS0N/GPIO_D0_3/BS_SEL_N/TEST_JTAG_TMS
Y22	SPI_MS3_DI	INOUT	PU	1.8v digital IO	SPI_DBG_DI/GPIO_A1_0/SPI_M3_DI/CAN_RXD0/SPI_S0_DI
V24	SPI_MS3_DO	INOUT	N/A	1.8v digital IO	SPI_DBG_DO/GPIO_A1_1/SPI_M3_DO/CAN_TXD0/SPI_S0_DO
V26	SPI_MS3_SCLK	INOUT	PU	1.8v digital IO	SPI_DBG_CLK/GPIO_A1_2/SPI_M3_SCLK/CAN_RXD1/SPI_S0_SCK
V25	SPI_MS3_CS0N	INOUT	PU	1.8v digital IO	SPI_DBG_CSN/GPIO_A1_3/SPI_M3_CS0N/CAN_TXD1/SPI_S0_CSN
Y23	SPI_MS3_CS1N	INOUT	PU	1.8v digital IO	BB_DEBUG_MOSI/GPIO_A1_4/SPI_M3_CS1N/CAN_STBY0/SPI_S1_DI
U24	SPI_MS3_CS2N	INOUT	N/A	1.8v digital IO	BB_DEBUG_MISO/GPIO_A1_5/SPI_M3_CS2N/CAN_STBY1/SPI_S1_DO
V23	SPI_MS3_CS3N	INOUT	PU	1.8v digital IO	BB_DEBUG_SCK/GPIO_A1_6/SPI_M3_CS3N/CAN_STBY2/SPI_S1_SCK
U26	SPI_MS3_CS4N	INOUT	PU	1.8v digital IO	BB_DEBUG_CSN/GPIO_A1_7/SPI_M3_CS4N/CAN_STBY3/SPI_S1_CSN

Share function

Name	Function_0	Function_1	Function_2	Function_3	Function_4
SPI_M0_DI	SPI_M0_DI	GPIO_C0_0			
SPI_M0_DO	SPI_M0_DO	GPIO_C0_1			
SPI_M0_SCLK	SPI_M0_SCLK	GPIO_C0_2			
SPI_M0_CSN	SPI_M0_CSN	GPIO_C0_3			
SPI_M1_DI	SPI_M1_DI	GPIO_C0_4	CAN_RXD2		
SPI_M1_DO	SPI_M1_DO	GPIO_C0_5	CAN_TXD2		
SPI_M1_SCLK	SPI_M1_SCLK	GPIO_C0_6	CAN_RXD3	TEST_JTAG_RTCK	
SPI_M1_CSN	SPI_M1_CSN	GPIO_C0_7	CAN_TXD3	TEST_JTAG_TRSTN	
SPI_M2_DI	SPI_M2_DI	GPIO_D0_0	BB_ANT_SW_SEL	TEST_JTAG_TDI	
SPI_M2_DO	SPI_M2_DO	GPIO_D0_1	BB_ANT_SW_SEL_N	TEST_JTAG_TDO	
SPI_M2_SCLK	SPI_M2_SCLK	GPIO_D0_2	BS_SEL	TEST_JTAG_TCK	
SPI_M2_CS0N	SPI_M2_CS0N	GPIO_D0_3	BS_SEL_N	TEST_JTAG_TMS	
SPI_MS3_DI	SPI_DBG_DI	GPIO_A1_0	SPI_M3_DI	CAN_RXD0	SPI_S0_DI
SPI_MS3_DO	SPI_DBG_DO	GPIO_A1_1	SPI_M3_DO	CAN_TXD0	SPI_S0_DO
SPI_MS3_SCLK	SPI_DBG_CLK	GPIO_A1_2	SPI_M3_SCLK	CAN_RXD1	SPI_S0_SCK
SPI_MS3_CS0N	SPI_DBG_CSN	GPIO_A1_3	SPI_M3_CS0N	CAN_TXD1	SPI_S0_CSN
SPI_MS3_CS1N	BB_DEBUG_MOSI	GPIO_A1_4	SPI_M3_CS1N	CAN_STBY0	SPI_S1_DI
SPI_MS3_CS2N	BB_DEBUG_MISO	GPIO_A1_5	SPI_M3_CS2N	CAN_STBY1	SPI_S1_DO

SPI_MS3_CS3N	BB_DEBUG_SCK	GPIO_A1_6	SPI_M3_CS3N	CAN_STBY2	SPI_S1_SCK
SPI_MS3_CS4N	BB_DEBUG_CSN	GPIO_A1_7	SPI_M3_CS4N	CAN_STBY3	SPI_S1_CSN

5.5.3 I2C Interface (10)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
AD3	I2C_SDA0	INOUT	PU	1.8v digital IO	I2C_SDA0/GPIO_B1_0
AE3	I2C_SCLK0	INOUT	PU	1.8v digital IO	I2C_SCLK0/GPIO_B1_1
AC4	I2C_SDA1	INOUT	PU	1.8v digital IO	I2C_SDA1/GPIO_B1_2
AD4	I2C_SCLK1	INOUT	PU	1.8v digital IO	I2C_SCLK1/GPIO_B1_3
AC3	I2C_SDA2	INOUT	PU	1.8v digital IO	I2C_SDA2/GPIO_B1_4
AC5	I2C_SCLK2	INOUT	PU	1.8v digital IO	I2C_SCLK2/GPIO_B1_5
H24	I2C_SDA3	INOUT	PU	1.8v digital IO	I2C_SDA3/GPIO_B1_6/BB_SPI_ENB_B
F24	I2C_SCLK3	INOUT	PU	1.8v digital IO	I2C_SCLK3/GPIO_B1_7/BB_SPI_CLK_B
F22	I2C_SDA4	INOUT	PD	1.8v digital IO	JTAG_TMS/GPIO_D0_4/ BB_SPI_~~DI~~ MISO_B /I2C_SDA4
G24	I2C_SCLK4	INOUT	PD	1.8v digital IO	JTAG_TCK/GPIO_D0_5/ BB_SPI_~~DO~~ MOSI_B /I2C_SCLK4

Share function

Name	Function_0	Function_1	Function_2	Function_3
I2C_SDA0	I2C_SDA0	GPIO_B1_0		
I2C_SCLK0	I2C_SCLK0	GPIO_B1_1		
I2C_SDA1	I2C_SDA1	GPIO_B1_2		
I2C_SCLK1	I2C_SCLK1	GPIO_B1_3		
I2C_SDA2	I2C_SDA2	GPIO_B1_4		
I2C_SCLK2	I2C_SCLK2	GPIO_B1_5		
I2C_SDA3	I2C_SDA3	GPIO_B1_6	BB_SPI_ENB_B	
I2C_SCLK3	I2C_SCLK3	GPIO_B1_7	BB_SPI_CLK_B	
I2C_SDA4	JTAG_TMS	GPIO_D0_4	BB_SPI_~~DI~~ MISO_B	I2C_SDA4
I2C_SCLK4	JTAG_TCK	GPIO_D0_5	BB_SPI_~~DO~~ MOSI_B	I2C_SCLK4

5.5.4 UART Interface (10)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
AC7	UART_RX0	INOUT	PU	1.8v digital IO	SEC_UART_SIN/GPIO_C1_0/UART_SIN0
Y6	UART_TX0	INOUT	N/A	1.8v digital IO	SEC_UART_SOUT/GPIO_C1_1/UART_SOUT0

AA7	UART_RX1	INOUT	PU	1.8v digital IO	TROOT_RXD/GPIO_C1_2/CAN_RXD0/UART_SIN1
AA6	UART_TX1	INOUT	N/A	1.8v digital IO	TROOT_TXD/GPIO_C1_3/CAN_TXD0/UART_SOUT1
AB5	UART_RX2	INOUT	PU	1.8v digital IO	UART_SIN2/GPIO_C1_4/CAN_RXD1
AB6	UART_TX2	INOUT	PU	1.8v digital IO	UART_SOUT2/GPIO_C1_5/CAN_TXD1
V6	UART_RX3	INOUT	PU	1.8v digital IO	UART_SIN3/GPIO_C1_6/CAN_RXD2
W7	UART_TX3	INOUT	PU	1.8v digital IO	UART_SOUT3/GPIO_C1_7/CAN_TXD2/CEVA_UART_TX
P22	UART_SIN4	INOUT	PD	1.8v digital IO	JTAG_TDI/GPIO_D0_6/CAN_RXD3/BB_PA_ON_2G/UART_SIN4/UART_CTS_N1
R22	UART_SOUT4	INOUT	N/A	1.8v digital IO	JTAG_TDO/GPIO_D0_7/CAN_TXD3/BB_PA_ON_5G/UART_SOUT4/UART_RTS_N1

Share function

Name	Function_0	Function_1	Function_2	Function_3	Function_4	Function_5
UART_RX0	SEC_UART_SIN	GPIO_C1_0	UART_SIN0			
UART_TX0	SEC_UART_SOUT	GPIO_C1_1	UART_SOUT0			
UART_RX1	TROOT_RXD	GPIO_C1_2	CAN_RXD0	UART_SIN1		
UART_TX1	TROOT_TXD	GPIO_C1_3	CAN_TXD0	UART_SOUT1		
UART_RX2	UART_SIN2	GPIO_C1_4	CAN_RXD1	ATE_TEST_IN_24		
UART_TX2	UART_SOUT2	GPIO_C1_5	CAN_TXD1	ATE_TEST_IN_25		
UART_RX3	UART_SIN3	GPIO_C1_6	CAN_RXD2	ATE_TEST_IN_26		
UART_TX3	UART_SOUT3	GPIO_C1_7	CAN_TXD2	CEVA_UART_TX		
UART_SIN4	JTAG_TDI	GPIO_D0_6	CAN_RXD3	BB_PA_ON_2G	UART_SIN4	UART_CTS_N1
UART_SOUT4	JTAG_TDO	GPIO_D0_7	CAN_TXD3	BB_PA_ON_5G	UART_SOUT4	UART_RTS_N1

5.5.5 PWM Interface (10)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
H22	PWM0	OUT	N/A	1.8v digital IO	PWM0/GPIO_D1_0
J22	PWM1	OUT	N/A	1.8v digital IO	PWM1/GPIO_D1_1/TRACE_DATA_7
L22	PWM2	INOUT	PU	1.8v digital IO	PWM2/GPIO_D1_2/UART_SIN5/SPI_M2_DI/TRACE_DATA_6
M22	PWM3	OUT	N/A	1.8v digital IO	PWM3/GPIO_D1_3/UART_SOUT5/SPI_M2_DO/TRACE_DATA_5
N22	PWM4	INOUT	PU	1.8v digital IO	PWM4/GPIO_D1_4/UART_SIN6/SPI_M2_SCLK/TRACE_DATA_4/BB_PA_ON_2G_1
T22	PWM5	INOUT	PU	1.8v digital IO	PWM5/GPIO_D1_5/UART_SOUT6/SPI_M2_CS0N/TRACE_DATA_3/BB_PA_ON_5G_1
U22	PWM6	INOUT	PU	1.8v digital IO	PWM6/GPIO_D1_6/UART_SIN7/SPI_M2_CS1N/TRACE_DATA_2/CAN_TCL

					K0
U23	PWM7	INOUT	PU	1.8v digital IO	PWM7/GPIO_D1_7/UART_SOUT7/SPI_M2_CS2N/TRACE_DATA_1/CAN_TCLK1
V22	PWM8	INOUT	PU	1.8v digital IO	PWM8/GPIO_A2_0/UART_SIN8/SPI_M2_CS3N/TRACE_DATA_0/CAN_TCLK2
W22	PWM9	INOUT	PU	1.8v digital IO	PWM9/GPIO_A2_1/UART_SOUT8/SPI_M2_CS4N/TRACE_CLK/CAN_TCLK3

Share function

Name	Function_0	Function_1	Function_2	Function_3	Function_4	Function_5
PWM0	PWM0	GPIO_D1_0				
PWM1	PWM1	GPIO_D1_1			TRACE_DATA_7	
PWM2	PWM2	GPIO_D1_2	UART_SIN5	SPI_M2_DI	TRACE_DATA_6	
PWM3	PWM3	GPIO_D1_3	UART_SOUT5	SPI_M2_DO	TRACE_DATA_5	
PWM4	PWM4	GPIO_D1_4	UART_SIN6	SPI_M2_SCLK	TRACE_DATA_4	BB_PA_ON_2G_1
PWM5	PWM5	GPIO_D1_5	UART_SOUT6	SPI_M2_CS0N	TRACE_DATA_3	BB_PA_ON_5G_1
PWM6	PWM6	GPIO_D1_6	UART_SIN7	SPI_M2_CS1N	TRACE_DATA_2	CAN_TCLK0
PWM7	PWM7	GPIO_D1_7	UART_SOUT7	SPI_M2_CS2N	TRACE_DATA_1	CAN_TCLK1
PWM8	PWM8	GPIO_A2_0	UART_SIN8	SPI_M2_CS3N	TRACE_DATA_0	CAN_TCLK2
PWM9	PWM9	GPIO_A2_1	UART_SOUT8	SPI_M2_CS4N	TRACE_CLK	CAN_TCLK3

5.5.6 I2S Interface (16)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
AA28	I2S_WS0	INOUT	PU	1.8v digital IO	I2S_WS_0/GPIO_B2_0
AA26	I2S_SDI0	INOUT	PD	1.8v digital IO	I2S_SDI_0/GPIO_B2_1
AB28	I2S_SDO0	INOUT	PU	1.8v digital IO	I2S_SDO_0/GPIO_B2_2
AA27	I2S_CLK0	INOUT	PU	1.8v digital IO	I2S_CLK_0/GPIO_B2_3
AC26	I2S_WS1	INOUT	PU	1.8v digital IO	I2S_WS_1/GPIO_B2_4
Y25	I2S_SDI1	INOUT	PD	1.8v digital IO	I2S_SDI_1/GPIO_B2_5

AB27	I2S_SDO1	INOUT	PU	1.8v digital IO	I2S_SDO_1/GPIO_B2_6
AA25	I2S_CLK1	INOUT	PU	1.8v digital IO	I2S_CLK_1/GPIO_B2_7
AA22	I2S_WS2	INOUT	PU	1.8v digital IO	I2S_WS_2/GPIO_C2_0/MON_OUT_24/BB_RXTX_A/ATE_TEST_IN_8
AA23	I2S_SDI2	INOUT	PD	1.8v digital IO	I2S_SDI_2/GPIO_C2_1/MON_OUT_25/BB_ENABLE_A/ATE_TEST_IN_9
AA24	I2S_SDO2	INOUT	PU	1.8v digital IO	I2S_SDO_2/GPIO_C2_2/MON_OUT_26/BB_RXHP_A/ATE_TEST_IN_10
Y24	I2S_CLK2	INOUT	PU	1.8v digital IO	I2S_CLK_2/GPIO_C2_3/MON_OUT_27/BB_RX_LNA_VBIAS_2G/ATE_TEST_IN_11
AC25	I2S_WS3	INOUT	PU	1.8v digital IO	I2S_WS_3/GPIO_C2_4/DVP_EXT_OUT_0/MON_OUT_28/BB_RXTX_B/ATE_TEST_IN_12
AB24	I2S_SDI3	INOUT	PD	1.8v digital IO	I2S_SDI_3/GPIO_C2_5/DVP_EXT_OUT_1/MON_OUT_29/BB_ENABLE_B/ATE_TEST_IN_13
AC24	I2S_SDO3	INOUT	PU	1.8v digital IO	I2S_SDO_3/GPIO_C2_6/DVP_EXT_OUT_2/MON_OUT_30/BB_RXHP_B/ATE_TEST_IN_14
AB23	I2S_CLK3	INOUT	PU	1.8v digital IO	I2S_CLK_3/GPIO_C2_7/DVP_EXT_OUT_3/MON_OUT_31/BB_RX_LNA_VBIAS_5G/ATE_TEST_IN_15

Share function

Name	Function_0	Function_1	Function_2	Function_3	Function_4	Function_5
I2S_WS0	I2S_WS_0	GPIO_B2_0				
I2S_SDI0	I2S_SDI_0	GPIO_B2_1				
I2S_SDO0	I2S_SDO_0	GPIO_B2_2				
I2S_CLK0	I2S_CLK_0	GPIO_B2_3				
I2S_WS1	I2S_WS_1	GPIO_B2_4				
I2S_SDI1	I2S_SDI_1	GPIO_B2_5				
I2S_SDO1	I2S_SDO_1	GPIO_B2_6				
I2S_CLK1	I2S_CLK_1	GPIO_B2_7				
I2S_WS2	I2S_WS_2	GPIO_C2_0		MON_OUT_24	BB_RXTX_A	ATE_TEST_IN_8
I2S_SDI2	I2S_SDI_2	GPIO_C2_1		MON_OUT_25	BB_ENABLE_A	ATE_TEST_IN_9
I2S_SDO2	I2S_SDO_2	GPIO_C2_2		MON_OUT_26	BB_RXHP_A	ATE_TEST_IN_10
I2S_CLK2	I2S_CLK_2	GPIO_C2_3		MON_OUT_27	BB_RX_LNA_VBIAS_2G	ATE_TEST_IN_11
I2S_WS3	I2S_WS_3	GPIO_C2_4	DVP_EXT_OUT_0	MON_OUT_28	BB_RXTX_B	ATE_TEST_IN_12
I2S_SDI3	I2S_SDI_3	GPIO_C2_5	DVP_EXT_OUT_1	MON_OUT_29	BB_ENABLE_B	ATE_TEST_IN_13
I2S_SDO3	I2S_SDO_3	GPIO_C2_6	DVP_EXT_OUT_2	MON_OUT_30	BB_RXHP_B	ATE_TEST_IN_14

I2S_CLK3	I2S_CLK_3	GPIO_C2_7	DVP_EXT_OUT_3	MON_OUT_31	BB_RX_LNA_VBIAS_5G	ATE_TEST_IN_15

5.5.7 SD Interface (8)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
U28	SD_CCLK_OUT	OUT	N/A	1.8/3.3v digital IO	QSPI_SCK/SD_CCLK_OUT/GPIO_D2_0
U27	SD_CCMD	OUT	N/A	1.8/3.3v digital IO	QSPI_CS_N/SD_CCMD/GPIO_D2_1
V28	SD_CARD_DETECT_N	INOUT	PU	1.8/3.3v digital IO	GPIO_D2_2/SD_CARD_DETECT_N
V27	SD_CARD_WPRT	INOUT	PU	1.8/3.3v digital IO	GPIO_D2_3/SD_CARD_WPRT
W28	SD_CDATA_0	INOUT	PU	1.8/3.3v digital IO	QSPI_DATA_0/SD_CDATA_0/GPIO_D2_4
W27	SD_CDATA_1	INOUT	PU	1.8/3.3v digital IO	QSPI_DATA_1/SD_CDATA_1/GPIO_D2_5
Y28	SD_CDATA_2	INOUT	PU	1.8/3.3v digital IO	QSPI_DATA_2/SD_CDATA_2/GPIO_D2_6
Y27	SD_CDATA_3	INOUT	PU	1.8/3.3v digital IO	QSPI_DATA_3/SD_CDATA_3/GPIO_D2_7

Share function

Name	Function_0	Function_1	Function_2
SD_CCLK_OUT	QSPI_SCK	SD_CCLK_OUT	GPIO_D2_0
SD_CCMD	QSPI_CS_N	SD_CCMD	GPIO_D2_1
SD_CARD_DETECT_N	GPIO_D2_2	SD_CARD_DETECT_N	
SD_CARD_WPRT	GPIO_D2_3	SD_CARD_WPRT	
SD_CDATA_0	QSPI_DATA_0	SD_CDATA_0	GPIO_D2_4
SD_CDATA_1	QSPI_DATA_1	SD_CDATA_1	GPIO_D2_5
SD_CDATA_2	QSPI_DATA_2	SD_CDATA_2	GPIO_D2_6
SD_CDATA_3	QSPI_DATA_3	SD_CDATA_3	GPIO_D2_7

5.5.8 DVP Interface (24)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
AC28	PCLK1	INOUT	PD	1.8v digital IO	PCLK1/GPIO_A2_2/I2C_SDA3/TYPEC_DIG_OUT_0/MON_OUT_0/ATE_TEST_OUT_0/DVP_EXT_OUT_4
AD28	DE1	INOUT	PD	1.8v digital IO	PDE1/GPIO_A2_3/I2C_SCLK3/TYPEC_DIG_OUT_1/MON_OUT_1/ATE_TEST_OUT_1/DVP_EXT_OUT_5
AC27	VSYNC1	INOUT	PD	1.8v digital IO	PVSYNC1/GPIO_A2_4/UART_SIN7/TYPEC_DIG_OUT_2/MON_OUT_2/ATE_TEST_OUT_2/DVP_EXT_OUT_6
AE28	HSYNC1	INOUT	PD	1.8v digital IO	PHSYNC1/GPIO_A2_5/UART_SOUT7/TYPEC_DIG_OUT_3/MON_OUT_3/ATE_TEST_OUT_3/DVP_EXT_OUT_7
AF28	QE1_0	INOUT	PU	1.8v digital IO	PDATA1_0/GPIO_A3_0/UART_SIN8/TYPEC_DIG_OUT_4/MON_OUT_4/ATE_TEST_OUT_4
AD27	QE1_1	INOUT	PU	1.8v digital IO	PDATA1_1/GPIO_A3_1/UART_SOUT8/TYPEC_DIG_OUT_5/MON_OUT_5/ATE_TEST_OUT_5
AG28	QE1_2	INOUT	PU	1.8v digital IO	PDATA1_2/GPIO_A3_2/I2C_SDA4/TYPEC_DIG_IN_6/MON_OUT_6/ATE_TEST_OUT_6
AE27	QE1_3	INOUT	PU	1.8v digital IO	PDATA1_3/GPIO_A3_3/I2C_SCLK4/TYPEC_DIG_IN_7/MON_OUT_7/ATE_TEST_OUT_7
AH26	QE1_4	INOUT	PD	1.8v digital IO	PDATA1_4/GPIO_A3_4/SPI_M3_CS1N/TYPEC_DIG_IN_8/MON_OUT_8/ATE_TEST_OUT_8
AF27	QE1_5	INOUT	PD	1.8v digital IO	PDATA1_5/GPIO_A3_5/SPI_M3_CS2N/TYPEC_DIG_IN_9/MON_OUT_9/ATE_TEST_OUT_9
AG27	QE1_6	INOUT	PD	1.8v digital IO	PDATA1_6/GPIO_A3_6/SPI_M3_CS3N/TYPEC_DIG_OUT_10/MON_OUT_10/ATE_TEST_OUT_10
AH27	QE1_7	INOUT	PD	1.8v digital IO	PDATA1_7/GPIO_A3_7/SPI_M3_CS4N/TYPEC_DIG_OUT_11/MON_OUT_11/ATE_TEST_OUT_11
AD26	PCLK0	INOUT	PD	1.8v digital IO	PCLK0 /GPIO_A2_6/MON_OUT_12/ATE_TEST_OUT_12
AD25	DE0	INOUT	PD	1.8v digital IO	PDE0/GPIO_A2_7/MON_OUT_13/ATE_TEST_OUT_13
AF26	VSYNC0	INOUT	PD	1.8v digital IO	PVSYNC0/GPIO_B0_0/MON_OUT_14/ATE_TEST_OUT_14
AE26	HSYNC0	INOUT	PD	1.8v digital IO	PHSYNC0 /GPIO_B0_1/MON_OUT_15/ATE_TEST_OUT_15
AG26	QE0_0	INOUT	PU	1.8v digital IO	MON_OUT_16/GPIO_B3_0/PDATA0_0/ATE_TEST_IN_0
AF25	QE0_1	INOUT	PU	1.8v digital IO	MON_OUT_17/GPIO_B3_1/PDATA0_1/ATE_TEST_IN_1
AD23	QE0_2	INOUT	PU	1.8v digital IO	MON_OUT_18/GPIO_B3_2/PDATA0_2/ATE_TEST_IN_2

AE24	QE0_3	INOUT	PU	1.8v digital IO	MON_OUT_19/**GPIO_B3_3/PDATA0_3/ATE_TEST_IN_3**
AC22	QE0_4	INOUT	PU	1.8v digital IO	MON_OUT_20/GPIO_B3_4/PDATA0_4/ATE_TEST_IN_4
AE23	QE0_5	INOUT	PU	1.8v digital IO	MON_OUT_21 /GPIO_B3_5/PDATA0_5/ATE_TEST_IN_5
AF23	QE0_6	INOUT	PU	1.8v digital IO	MON_OUT_22/GPIO_B3_6/PDATA0_6/ATE_TEST_IN_6
AD22	QE0_7	INOUT	PU	1.8v digital IO	MON_OUT_23/GPIO_B3_7/PDATA0_7/ATE_TEST_IN_7

Share function

Name	Function_0	Function_1	Function_2	Function_3	Function_4	Function_5
PCLK1	PCLK1	GPIO_A2_2	I2C_SDA3	TYPEC_DIG_OUT_0	MON_OUT_0	ATE_TEST_OUT_0
DE1	PDE1	GPIO_A2_3	I2C_SCLK3	TYPEC_DIG_OUT_1	MON_OUT_1	ATE_TEST_OUT_1
VSYNC1	PVSYNC1	GPIO_A2_4	UART_SIN7	TYPEC_DIG_OUT_2	MON_OUT_2	ATE_TEST_OUT_2
HSYNC1	PHSYNC1	GPIO_A2_5	UART_SOUT7	TYPEC_DIG_OUT_3	MON_OUT_3	ATE_TEST_OUT_3
QE1_0	PDATA1_0	GPIO_A3_0	UART_SIN8	TYPEC_DIG_OUT_4	MON_OUT_4	ATE_TEST_OUT_4
QE1_1	PDATA1_1	GPIO_A3_1	UART_SOUT8	TYPEC_DIG_OUT_5	MON_OUT_5	ATE_TEST_OUT_5
QE1_2	PDATA1_2	GPIO_A3_2	I2C_SDA4	TYPEC_DIG_IN_6	MON_OUT_6	ATE_TEST_OUT_6
QE1_3	PDATA1_3	GPIO_A3_3	I2C_SCLK4	TYPEC_DIG_IN_7	MON_OUT_7	ATE_TEST_OUT_7
QE1_4	PDATA1_4	GPIO_A3_4	SPI_M3_CS1N	TYPEC_DIG_IN_8	MON_OUT_8	ATE_TEST_OUT_8
QE1_5	PDATA1_5	GPIO_A3_5	SPI_M3_CS2N	TYPEC_DIG_IN_9	MON_OUT_9	ATE_TEST_OUT_9
QE1_6	PDATA1_6	GPIO_A3_6	SPI_M3_CS3N	TYPEC_DIG_OUT_10	MON_OUT_10	ATE_TEST_OUT_10
QE1_7	PDATA1_7	GPIO_A3_7	SPI_M3_CS4N	TYPEC_DIG_OUT_11	MON_OUT_11	ATE_TEST_OUT_11
PCLK0	PCLK0	GPIO_A2_6			MON_OUT_12	ATE_TEST_OUT_12
DE0	PDE0	GPIO_A2_7			MON_OUT_13	ATE_TEST_OUT_13
VSYNC0	PVSYNC0	GPIO_B0_0			MON_OUT_14	ATE_TEST_OUT_14
HSYNC0	PHSYNC0	GPIO_B0_1			MON_OUT_15	ATE_TEST_OUT_15
QE0_0	MON_OUT_16	GPIO_B3_0			PDATA0_0	ATE_TEST_IN_0
QE0_1	MON_OUT_17	GPIO_B3_1			PDATA0_1	ATE_TEST_IN_1
QE0_2	MON_OUT_18	GPIO_B3_2			PDATA0_2	ATE_TEST_IN_2
QE0_3	MON_OUT_19	GPIO_B3_3			PDATA0_3	ATE_TEST_IN_3
QE0_4	MON_OUT_20	GPIO_B3_4			PDATA0_4	ATE_TEST_IN_4

QE0_5	MON_OUT_21	GPIO_B3_5			PDATA0_5	ATE_TEST_IN_5
QE0_6	MON_OUT_22	GPIO_B3_6			PDATA0_6	ATE_TEST_IN_6
QE0_7	MON_OUT_23	GPIO_B3_7			PDATA0_7	ATE_TEST_IN_7

5.5.9 EMMC Interface (11)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
J28	EMMC_CLKOUT	OUT	N/A	1.8/3.3v digital IO	EMMC_CCLK_OUT/GPIO_B0_2
J27	EMMC_CCMD	INOUT	PU	1.8/3.3v digital IO	EMMC_CCMD/GPIO_B0_3
K22	EMMC_PWR	OUT	N/A	1.8/3.3v digital IO	EMMC_PWR/GPIO_B0_4
H25	EMMC_D0	INOUT	PU	1.8/3.3v digital IO	EMMC_D0/GPIO_C3_0
H26	EMMC_D1	INOUT	PU	1.8/3.3v digital IO	EMMC_D1/GPIO_C3_1
J25	EMMC_D2	INOUT	PU	1.8/3.3v digital IO	EMMC_D2/GPIO_C3_2
J26	EMMC_D3	INOUT	PU	1.8/3.3v digital IO	EMMC_D3/GPIO_C3_3
K27	EMMC_D4	INOUT	PU	1.8/3.3v digital IO	EMMC_D4/GPIO_C3_4
K28	EMMC_D5	INOUT	PU	1.8/3.3v digital IO	EMMC_D5/GPIO_C3_5
L28	EMMC_D6	INOUT	PU	1.8/3.3v digital IO	EMMC_D6/GPIO_C3_6
L27	EMMC_D7	INOUT	PU	1.8/3.3v digital IO	EMMC_D7/GPIO_C3_7

Share function

Name	Function_0	Function_1
EMMC_CLKOUT	EMMC_CCLK_OUT	GPIO_B0_2
EMMC_CCMD	EMMC_CCMD	GPIO_B0_3
EMMC_PWR	EMMC_PWR	GPIO_B0_4
EMMC_D0	EMMC_D0	GPIO_C3_0
EMMC_D1	EMMC_D1	GPIO_C3_1

EMMC_D2	EMMC_D2	GPIO_C3_2
EMMC_D3	EMMC_D3	GPIO_C3_3
EMMC_D4	EMMC_D4	GPIO_C3_4
EMMC_D5	EMMC_D5	GPIO_C3_5
EMMC_D6	EMMC_D6	GPIO_C3_6
EMMC_D7	EMMC_D7	GPIO_C3_7

5.5.10 Ethernet Interface (17)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
L26	GBE_TXC	INOUT	PD	3.3v digital IO	GBE_TXC/GPIO_D3_0/BB_SPI_ENB_A/SPI_M3_DI
M26	GBE_TXEN	INOUT	PU	3.3v digital IO	GBE_TXEN/GPIO_D3_1/BB_SPI_DI_A/SPI_M3_DO
M28	GBE_TXD0	INOUT	PU	3.3v digital IO	GBE_TXD0/GPIO_D3_2/BB_SPI_DO_A/SPI_M3_SCLK
M27	GBE_TXD1	INOUT	PU	3.3v digital IO	GBE_TXD1/GPIO_D3_3/BB_SPI_CLK_A/SPI_M3_CS0N
N27	GBE_TXD2	INOUT	PU	3.3v digital IO	GBE_TXD2/GPIO_D3_4/BB_RXTX_A/SPI_M3_CS1N
N28	GBE_TXD3	INOUT	PD	3.3v digital IO	GBE_TXD3/GPIO_D3_5/BB_ENABLE_A/SPI_M3_CS2N
P28	GBE_RXC	INOUT	PD	3.3v digital IO	GBE_RXC/GPIO_D3_6/BB_RXHP_A/SPI_M3_CS3N
P27	GBE_RXEN	INOUT	PD	3.3v digital IO	GBE_RXEN/GPIO_D3_7/BB_RX_LNA_VBIAS_2G/SPI_M3_CS4N
R28	GBE_RXD0	INOUT	PD	3.3v digital IO	GBE_RXD0/GPIO_B4_0/BB_RX_LNA_VBIAS_5G/I2S_SDO_3
R27	GBE_RXD1	INOUT	PD	3.3v digital IO	GBE_RXD1/GPIO_B4_1/BB_PA_ON_2G/I2S_SDO_2
T28	GBE_RXD2	INOUT	PD	3.3v digital IO	GBE_RXD2/GPIO_B4_2/BB_PA_ON_5G/I2S_SDO_1
T27	GBE_RXD3	INOUT	PD	3.3v digital IO	GBE_RXD3/GPIO_B4_3/BB_ANT_SW_SEL/I2S_SDO_0
L25	GBE_MDC	INOUT	PU	3.3v digital IO	GBE_MDC/GPIO_B4_4/BB_ANT_SW_SEL_N/I2S_CLK_3
M25	GBE_MDIO	INOUT	PU	3.3v digital IO	GBE_MDIO/GPIO_B4_5/BS_SEL/I2S_WS_3
H23	GBE_INT	INOUT	PD	3.3v digital IO	GBE_INT/GPIO_A4_0/UART_SIN5/I2C_SCLK3
J23	GBE_CLK	INOUT	PU	3.3v digital IO	GBE_CLK/GPIO_A4_1/UART_SOUT5/I2C_SDA3
G23	GBE_RST	INOUT	PU	3.3v digital IO	GBE_RST/GPIO_B0_7/BS_SEL_N

Share function

Name	Function_0	Function_1	Function_2	Function_3
GBE_TXC	GBE_TXC	GPIO_D3_0	BB_SPI_ENB_A	SPI_M3_DI
GBE_TXEN	GBE_TXEN	GPIO_D3_1	BB_SPI_DI_A	SPI_M3_DO
GBE_TXD0	GBE_TXD0	GPIO_D3_2	BB_SPI_DO_A	SPI_M3_SCLK
GBE_TXD1	GBE_TXD1	GPIO_D3_3	BB_SPI_CLK_A	SPI_M3_CS0N
GBE_TXD2	GBE_TXD2	GPIO_D3_4	BB_RXTX_A	SPI_M3_CS1N
GBE_TXD3	GBE_TXD3	GPIO_D3_5	BB_ENABLE_A	SPI_M3_CS2N
GBE_RXC	GBE_RXC	GPIO_D3_6	BB_RXHP_A	SPI_M3_CS3N
GBE_RXEN	GBE_RXEN	GPIO_D3_7	BB_RX_LNA_VBIAS_2G	SPI_M3_CS4N
GBE_RXD0	GBE_RXD0	GPIO_B4_0	BB_RX_LNA_VBIAS_5G	I2S_SDO_3
GBE_RXD1	GBE_RXD1	GPIO_B4_1	BB_PA_ON_2G	I2S_SDO_2
GBE_RXD2	GBE_RXD2	GPIO_B4_2	BB_PA_ON_5G	I2S_SDO_1
GBE_RXD3	GBE_RXD3	GPIO_B4_3	BB_ANT_SW_SEL	I2S_SDO_0
GBE_MDC	GBE_MDC	GPIO_B4_4	BB_ANT_SW_SEL_N	I2S_CLK_3
GBE_MDIO	GBE_MDIO	GPIO_B4_5	BS_SEL	I2S_WS_3
GBE_INT	GBE_INT	GPIO_A4_0	UART_SIN5	I2C_SCLK3
GBE_CLK	GBE_CLK	GPIO_A4_1	UART_SOUT5	I2C_SDA3
GBE_RST	GBE_RST	GPIO_B0_7	BS_SEL_N	

5.5.11 HDMI Interface (12)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
AB21	HDMI_RREF	INOUT	NA	Analog	Reference resistor connection
AG24	HDMI_RX0N	IN	NA	Analog	Negative TMDS differential line data input for data channel 0
AH24	HDMI_RX0P	IN	NA	Analog	Positive TMDS differential line data input for data channel 0
AG23	HDMI_RX1N	IN	NA	Analog	Negative TMDS differential line data input for data channel 1
AH23	HDMI_RX1P	IN	NA	Analog	Positive TMDS differential line data input for data channel 1

AG22	HDMI_RX2N	IN	NA	Analog	Negative TMDS differential line data input for data channel 2
AH22	HDMI_RX2P	IN	NA	Analog	Positive TMDS differential line data input for data channel 2
AG25	HDMI_RXCN	IN	NA	Analog	Negative TMDS differential line clock input
AH25	HDMI_RXCP	IN	NA	Analog	Positive TMDS differential line clock input
AD21	HDMI_SCL_PAD	INOUT	PU	1.8v digital IO	HDMI_SCL/GPIO_A4_2/I2C_SCLK4
AE21	HDMI_SDA_PAD	INOUT	PU	1.8v digital IO	HDMI_SDA/GPIO_A4_3/I2C_SDA4
AF20	HDMI_CEC_PAD	INOUT	PU	1.8v digital IO	HDMI_CEC/GPIO_A4_4

Share function

Name	Function_0	Function_1	Function_2
HDMI_SCL	HDMI_SCL	GPIO_A4_2	I2C_SCLK4
HDMI_SDA	HDMI_SDA	GPIO_A4_3	I2C_SDA4
HDMI_CEC	HDMI_CEC	GPIO_A4_4	

5.5.12 MIPI Interface (56)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
AE14	MIPI0_CLKN	INOUT	NA	Analog	MIPI Differential Clock Lane of Link_0
AD14	MIPI0_CLKP	INOUT	NA	Analog	
AH14	MIPI0_D0N	INOUT	NA	Analog	MIPI Differential Data Lane of Link_0
AG14	MIPI0_D0P	INOUT	NA	Analog	
AH13	MIPI0_D1N	INOUT	NA	Analog	
AG13	MIPI0_D1P	INOUT	NA	Analog	
AC15	MIPI0_REXT	INOUT	NA	Analog	Analog Probing Pin of Link_0
AE12	MIPI1_CLKN	INOUT	NA	Analog	MIPI Differential Clock Lane of Link_1
AD12	MIPI1_CLKP	INOUT	NA	Analog	
AH11	MIPI1_D0N	INOUT	NA	Analog	MIPI Differential Data Lane of Link_1
AG11	MIPI1_D0P	INOUT	NA	Analog	
AH12	MIPI1_D1N	INOUT	NA	Analog	
AG12	MIPI1_D1P	INOUT	NA	Analog	
AC12	MIPI1_REXT	INOUT	NA	Analog	Analog Probing Pin of Link_1
AE17	MIPI2_CLKN	INOUT	NA	Analog	MIPI Differential Clock Lane of Link_2
AF17	MIPI2_CLKP	INOUT	NA	Analog	
AH18	MIPI2_D0N	INOUT	NA	Analog	MIPI Differential Data Lane of Link_2

AG18	MIPI2_D0P	INOUT	NA	Analog	
AH17	MIPI2_D1N	INOUT	NA	Analog	
AG17	MIPI2_D1P	INOUT	NA	Analog	
AC17	MIPI2_REXT	INOUT	NA	Analog	Analog Probing Pin of Link_2
AE15	MIPI3_CLKN	INOUT	NA	Analog	MIPI Differential Clock Lane of Link_3
AF15	MIPI3_CLKP	INOUT	NA	Analog	
AH16	MIPI3_D0N	INOUT	NA	Analog	MIPI Differential Data Lane of Link_3
AG16	MIPI3_D0P	INOUT	NA	Analog	
AH15	MIPI3_D1N	INOUT	NA	Analog	
AG15	MIPI3_D1P	INOUT	NA	Analog	
AD15	MIPI3_REXT	INOUT	NA	Analog	Analog Probing Pin of Link_3
AE11	MIPI4_CLKN	INOUT	NA	Analog	MIPI Differential Clock Lane of Link_4
AF11	MIPI4_CLKP	INOUT	NA	Analog	
AH10	MIPI4_D0N	INOUT	NA	Analog	MIPI Differential Data Lane of Link_4
AG10	MIPI4_D0P	INOUT	NA	Analog	
AH9	MIPI4_D1N	INOUT	NA	Analog	
AG9	MIPI4_D1P	INOUT	NA	Analog	
AD11	MIPI4_REXT	INOUT	NA	Analog	Analog Probing Pin of Link_4
AE9	MIPI5_CLKN	INOUT	NA	Analog	MIPI Differential Clock Lane of Link_5
AF9	MIPI5_CLKP	INOUT	NA	Analog	
AH8	MIPI5_D0N	INOUT	NA	Analog	MIPI Differential Data Lane of Link_5
AG8	MIPI5_D0P	INOUT	NA	Analog	
AH7	MIPI5_D1N	INOUT	NA	Analog	
AG7	MIPI5_D1P	INOUT	NA	Analog	
AE8	MIPI5_REXT	INOUT	NA	Analog	Analog Probing Pin of Link_5
AE6	MIPI6_CLKN	INOUT	NA	Analog	MIPI Differential Clock Lane of Link_6
AF6	MIPI6_CLKP	INOUT	NA	Analog	
AH6	MIPI6_D0N	INOUT	NA	Analog	MIPI Differential Data Lane of Link_6
AG6	MIPI6_D0P	INOUT	NA	Analog	
AH5	MIPI6_D1N	INOUT	NA	Analog	
AG5	MIPI6_D1P	INOUT	NA	Analog	
AD9	MIPI6_REXT	INOUT	NA	Analog	Analog Probing Pin of Link_6
AE5	MIPI7_CLKN	INOUT	NA	Analog	MIPI Differential Clock Lane of Link_7
AF5	MIPI7_CLKP	INOUT	NA	Analog	
AH4	MIPI7_D0N	INOUT	NA	Analog	MIPI Differential Data Lane of Link_7
AG4	MIPI7_D0P	INOUT	NA	Analog	
AH3	MIPI7_D1N	INOUT	NA	Analog	
AG3	MIPI7_D1P	INOUT	NA	Analog	
AD8	MIPI7_REXT	INOUT	NA	Analog	Analog Probing Pin of Link_7

5.5.13 PCIE Interface (9)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
B18	PCIE_RX0N	INOUT	NA	Analog	High-Speed Differential Receive Pair
A18	PCIE_RX0P	INOUT	NA	Analog	High-Speed Differential Receive Pair
B17	PCIE_RX1N	INOUT	NA	Analog	High-Speed Differential Receive Pair
A17	PCIE_RX1P	INOUT	NA	Analog	High-Speed Differential Receive Pair
A19	PCIE_TX0P	INOUT	NA	Analog	High-Speed Differential Transmit Pair
B19	PCIE_TX0N	INOUT	NA	Analog	High-Speed Differential Transmit Pair
B16	PCIE_TX1N	INOUT	NA	Analog	High-Speed Differential Transmit Pair
A16	PCIE_TX1P	INOUT	NA	Analog	High-Speed Differential Transmit Pair
G16	PCIE_RESREF	INOUT	NA	Analog	Reference Resistor Connection

5.5.14 USB Interface (11)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
AG19	USB_DN	INOUT	NA	Analog	USB D– Signal
AH19	USB_DP	INOUT	NA	Analog	USB D+ Signal
AD17	USB_ID	IN	NA	Analog	USB Mini-Receptacle Identifier and Test Point for DC Points Probes
AD18	USB_RESREF	INOUT	NA	Analog	Reference Resistor Connection
AG21	USB_RX0N	IN	NA	Analog	High-Speed Differential Receive Pair
AH21	USB_RX0P	IN	NA	Analog	High-Speed Differential Receive Pair
AG20	USB_TX0N	OUT	NA	Analog	High-Speed Differential Transmit Pair
AH20	USB_TX0P	OUT	NA	Analog	High-Speed Differential Transmit Pair
AE18	USB_VBUS	INOUT	NA	Analog	USB 5-V Power Supply Pin
AD20	USB_OC_PAD	IN	PU	1.8v digital IO	USB_OC/GPIO_B0_5
AE20	USB_PWR_PAD	OUT	PU	1.8v digital IO	USB_PWR_CTRL/GPIO_B0_6

Share function

Name	Function_0	Function_1
USB_OC	USB_OC	GPIO_B0_5
USB_PWR	USB_PWR_CTRL	GPIO_B0_6

5.5.15 TYPEC Interface (17)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
D18	TYPEC_AUXN	I/O	NA	Analog	AUX differential TX/RX serial data
C17	TYPEC_AUXP	I/O	NA	Analog	AUX differential TX/RX serial data
E15	TYPEC_AUX_PDPUP	O	NA	Analog	AUX pull-up/pull-down polarity reversal pins. Normal connector orientation, weak pull-up. Used to reverse this for the flipped connector case
D15	TYPEC_AUX_PUPDN	O	NA	Analog	AUX pull-up/pull-down polarity reversal pins. Normal connector orientation, weak pull-down. Used to reverse this for the flipped connector case
A21	TYPEC_CC1	I/O	NA	Analog	Configuration channel 1 pin used for connection detect interface configuration and VCONN
B21	TYPEC_CC2	I/O	NA	Analog	Configuration channel 2 pin used for connection detect interface configuration and VCONN
A20	TYPEC_REXT	I	NA	Analog	PMA external calibration resistor. An external resistor must be connected between this pin and package ground. 3.01kΩ with 1% tolerance.
A22	TYPEC_REXT_CC	I	NA	Analog	Bump to connect external precision resistors for internal calibration circuits
E17	TYPEC_TX0N	O	NA	Analog	PMA lane0 transmitter serial data-USB TX or DP TX. TX1+/TX1- USB Type-C receptacle pins
D17	TYPEC_TX0P	O	NA	Analog	PMA lane0 transmitter serial data-USB TX or DP TX. TX1+/TX1- USB Type-C receptacle pins
E20	TYPEC_TX3N	O	NA	Analog	PMA lane0 transmitter serial data-USB TX or DP TX. TX2+/TX2- USB Type-C receptacle pins
F20	TYPEC_TX3P	O	NA	Analog	PMA lane0 transmitter serial data-USB TX or DP TX. TX2+/TX2- USB Type-C receptacle pins
E18	TYPEC_TXRX1N	I/O	NA	Analog	PMA lane0 transmitter serial data-USB RX or DP TX. RX1+/RX1- USB Type-C receptacle pins
F18	TYPEC_TXRX1P	I/O	NA	Analog	PMA lane0 transmitter serial data-USB RX or DP TX. RX1+/RX1- USB Type-C receptacle pins
D20	TYPEC_TXRX2N	I/O	NA	Analog	PMA lane0 transmitter serial data-USB RX or DP TX. RX2+/RX2- USB Type-C receptacle pins
C20	TYPEC_TXRX2P	I/O	NA	Analog	PMA lane0 transmitter serial data-USB RX or DP TX. RX2+/RX2- USB Type-C receptacle pins
B20	TYPEC_VBUS	I	NA	Analog	vbus Bump into the PHY for VBUS monitor. This is a divided input from the VBUS pin of the USB2 IP or an independent input from the connector

5.5.16 Analog block Interface (49)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
E23	AD_IN_0	SAR3 input pad	in		SAR3 input pad
E22	AD_IN_1	SAR3 input pad	in		SAR3 input pad
B28	AD_IN_2	SAR3 input pad	in		SAR3 input pad
C26	AD_IN_3	SAR3 input pad	in		SAR3 input pad
F21	AD_IN_4	SAR3 input pad	in		SAR3 input pad
D21	AD_IN_5	SAR3 input pad	in		SAR3 input pad
E21	AD_IN_6	SAR3 input pad	in		SAR3 input pad
G21	AD_IN_7	SAR3 input pad	in		SAR3 input pad
J20	AVDD1V8_A	Analog 1.8v power supply	in		Analog 1.8v power supply
J21	AVDD1V8_A	Analog 1.8v power supply	in		Analog 1.8v power supply
G19	AVDD1V8_OSC	Cystal 1.8v power supply	in		Cystal 1.8v power supply
K21	AVDD1V8_PLL	PLL 1.8v power supply	in		PLL 1.8v power supply
H21	AVSS_A	Analog ground	in		Analog ground
H20	AVSS_A	Analog ground	in		Analog ground
G20	AVSS_OSC	Cystal ground	in		Cystal ground
K20	AVSS_PLL	PLL ground	in		PLL ground
B22	CLKREF_SEL_PAD	Cystal mode selection(dedication pin to select) 0:40MHz cystal 1:20MHz cystal	in		Cystal mode selection(dedication pin to select) 0:40MHz cystal 1:20MHz cystal
A26	IADC_VINN_A	IADC_A N input pad	in		IADC_A N input pad
D28	IADC_VINN_B	IADC_B N input pad	in		IADC_B N input pad
E26	IADC_VINN_C	IADC_C N input pad	in		IADC_C N input pad
G28	IADC_VINN_D	IADC_D N input pad	in		IADC_D N input pad
B26	IADC_VINP_A	IADC_A P input pad	in		IADC_A P input pad
D27	IADC_VINP_B	IADC_B P input pad	in		IADC_B P input pad
E25	IADC_VINP_C	IADC_C P input pad	in		IADC_C P input pad
G27	IADC_VINP_D	IADC_D P input pad	in		IADC_D P input pad
A25	IDAC_OUTN_A	IDAC_A N output pad	out		IDAC_A N output pad
E28	IDAC_OUTN_B	IDAC_B N output pad	out		IDAC_B N output pad
B25	IDAC_OUTP_A	IDAC_A P output pad	out		IDAC_A P output pad
E27	IDAC_OUTP_B	IDAC_B P output pad	out		IDAC_B P output pad
C25	PDET_A_2G	SAR1 input pad	in		SAR1 input pad
C24	PDET_A_5G	SAR2 input pad	in		SAR2 input pad
D24	PDET_B_2G	SAR1 input pad	in		SAR1 input pad
D23	PDET_B_5G	SAR2 input pad	in		SAR2 input pad

A27	QADC_VINN_A	QADC_A N input pad	in		QADC_A N input pad
C28	QADC_VINN_B	QADC_B N input pad	in		QADC_B N input pad
F26	QADC_VINN_C	QADC_C N input pad	in		QADC_C N input pad
H28	QADC_VINN_D	QADC_D N input pad	in		QADC_D N input pad
B27	QADC_VINP_A	QADC_A P input pad	in		QADC_A P input pad
C27	QADC_VINP_B	QADC_B P input pad	in		QADC_B P input pad
F25	QADC_VINP_C	QADC_C P input pad	in		QADC_C P input pad
H27	QADC_VINP_D	QADC_D P input pad	in		QADC_D P input pad
A24	QDAC_OUTN_A	QADC_A N output pad	out		QADC_A N output pad
F28	QDAC_OUTN_B	QADC_B N output pad	out		QADC_B N output pad
B24	QDAC_OUTP_A	QADC_A P output pad	out		QADC_A P output pad
F27	QDAC_OUTP_B	QADC_B P output pad	out		QADC_B P output pad
D26	RSSI_1	SAR1 input pad	in		SAR1 input pad
C23	RSSI_2	SAR2 input pad	in		SAR2 input pad
A23	XTAL1	20MHz cystal oscillator input	in		20MHz cystal oscillator input
B23	XTAL2	20MHz cystal oscillator output	out		20MHz cystal oscillator output

5.5.17 DDR Interface (152)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
M1	DDR_A0	out			SDRAM address
L2	DDR_A1	out			SDRAM address
F1	DDR_A10	out			SDRAM address
G1	DDR_A11	out			SDRAM address
E1	DDR_A12	out			SDRAM address
E2	DDR_A13	out			SDRAM address
D1	DDR_A14	out			SDRAM address
D2	DDR_A15	out			SDRAM address
C2	DDR_A16	out			SDRAM address
C1	DDR_A17	out			SDRAM address
J1	DDR_A2	out			SDRAM address
K1	DDR_A3	out			SDRAM address
L1	DDR_A4	out			SDRAM address
K2	DDR_A5	out			SDRAM address
H2	DDR_A6	out			SDRAM address
H1	DDR_A7	out			SDRAM address
J3	DDR_A8	out			SDRAM address
G2	DDR_A9	out			SDRAM address
J6	DDR_ACTN	out			SDRAM act

G6	DDR_ALERTN	in			SDRAM alert output
C5	DDR_ATO	out			Analog test output
H13	DDR_AVDD18	in			DDR PLL analog 1.8v power supply
H12	DDR_AVSS1V8	in			DDR PLL analog ground
H3	DDR_BA0	out			SDRAM bank address
J4	DDR_BA1	out			SDRAM bank address
F4	DDR_BG0	out			SDRAM bank group address
F3	DDR_BG1	out			SDRAM bank group address
B1	DDR_CK	out			SDRAM clock
D3	DDR_CKE0	out			SDRAM clock enable
C3	DDR_CKE1	out			SDRAM clock enable
B2	DDR_CKN	out			SDRAM clock#
E3	DDR_CSN0	out			SDRAM chip select
E4	DDR_CSN1	out			SDRAM chip select
R4	DDR_DM0	inout			SDRAM data mask
Y1	DDR_DM1	inout			SDRAM data mask
N2	DDR_DM2	inout			SDRAM data mask
L5	DDR_DM3	inout			SDRAM data mask
F11	DDR_DM4	inout			SDRAM data mask
A7	DDR_DM5	inout			SDRAM data mask
B14	DDR_DM6	inout			SDRAM data mask
F15	DDR_DM7	inout			SDRAM data mask
U5	DDR_DQ0	inout			SDRAM data
V4	DDR_DQ1	inout			SDRAM data
AD1	DDR_DQ10	inout			SDRAM data
AB2	DDR_DQ11	inout			SDRAM data
AB1	DDR_DQ12	inout			SDRAM data
AA1	DDR_DQ13	inout			SDRAM data
Y2	DDR_DQ14	inout			SDRAM data
W2	DDR_DQ15	inout			SDRAM data
V1	DDR_DQ16	inout			SDRAM data
U2	DDR_DQ17	inout			SDRAM data
W1	DDR_DQ18	inout			SDRAM data
U1	DDR_DQ19	inout			SDRAM data
Y5	DDR_DQ2	inout			SDRAM data
R1	DDR_DQ20	inout			SDRAM data
P1	DDR_DQ21	inout			SDRAM data
P2	DDR_DQ22	inout			SDRAM data
N1	DDR_DQ23	inout			SDRAM data
R6	DDR_DQ24	inout			SDRAM data

R3	DDR_DQ25	inout			SDRAM data
P6	DDR_DQ26	inout			SDRAM data
P5	DDR_DQ27	inout			SDRAM data
M3	DDR_DQ28	inout			SDRAM data
M4	DDR_DQ29	inout			SDRAM data
AA4	DDR_DQ3	inout			SDRAM data
L3	DDR_DQ30	inout			SDRAM data
L4	DDR_DQ31	inout			SDRAM data
E6	DDR_DQ32	inout			SDRAM data
D6	DDR_DQ33	inout			SDRAM data
C6	DDR_DQ34	inout			SDRAM data
E7	DDR_DQ35	inout			SDRAM data
D9	DDR_DQ36	inout			SDRAM data
F9	DDR_DQ37	inout			SDRAM data
E9	DDR_DQ38	inout			SDRAM data
C9	DDR_DQ39	inout			SDRAM data
AA3	DDR_DQ4	inout			SDRAM data
A2	DDR_DQ40	inout			SDRAM data
A3	DDR_DQ41	inout			SDRAM data
B4	DDR_DQ42	inout			SDRAM data
A4	DDR_DQ43	inout			SDRAM data
A6	DDR_DQ44	inout			SDRAM data
B7	DDR_DQ45	inout			SDRAM data
B8	DDR_DQ46	inout			SDRAM data
A8	DDR_DQ47	inout			SDRAM data
A9	DDR_DQ48	inout			SDRAM data
B10	DDR_DQ49	inout			SDRAM data
U4	DDR_DQ5	inout			SDRAM data
A10	DDR_DQ50	inout			SDRAM data
A13	DDR_DQ51	inout			SDRAM data
A12	DDR_DQ52	inout			SDRAM data
B13	DDR_DQ53	inout			SDRAM data
A14	DDR_DQ54	inout			SDRAM data
A15	DDR_DQ55	inout			SDRAM data
D11	DDR_DQ56	inout			SDRAM data
C11	DDR_DQ57	inout			SDRAM data
E12	DDR_DQ58	inout			SDRAM data
F12	DDR_DQ59	inout			SDRAM data
V3	DDR_DQ6	inout			SDRAM data
D14	DDR_DQ60	inout			SDRAM data

C14	DDR_DQ61	inout			SDRAM data
F14	DDR_DQ62	inout			SDRAM data
C15	DDR_DQ63	inout			SDRAM data
U3	DDR_DQ7	inout			SDRAM data
AE2	DDR_DQ8	inout			SDRAM data
AE1	DDR_DQ9	inout			SDRAM data
Y4	DDR_DQS0	inout			SDRAM data strobe
Y3	DDR_DQS0N	inout			SDRAM data strobe
AC2	DDR_DQS1	inout			SDRAM data strobe
AC1	DDR_DQS1N	inout			SDRAM data strobe
T2	DDR_DQS2	inout			SDRAM data strobe
T1	DDR_DQS2N	inout			SDRAM data strobe
P4	DDR_DQS3	inout			SDRAM data strobe
P3	DDR_DQS3N	inout			SDRAM data strobe
C8	DDR_DQS4	inout			SDRAM data strobe
D8	DDR_DQS4N	inout			SDRAM data strobe
B5	DDR_DQS5	inout			SDRAM data strobe
A5	DDR_DQS5N	inout			SDRAM data strobe
B11	DDR_DQS6	inout			SDRAM data strobe
A11	DDR_DQS6N	inout			SDRAM data strobe
D12	DDR_DQS7	inout			SDRAM data strobe
C12	DDR_DQS7N	inout			SDRAM data strobe
D5	DDR_DTO0	out			Digital test out
F7	DDR_DTO1	out			Digital test out
G5	DDR_ODT0	out			SDRAM on-die termination
H5	DDR_ODT1	out			SDRAM on-die termination
H4	DDR_PARITY	out			SDRAM parity input
F8	DDR_PLL_VDD	in			DDR PHY PLL power supply
G8	DDR_PLL_VDD	in			DDR PHY PLL power supply
C4	DDR_RAM_RSTN	out			SDRAM reset
G11	DDR_VDDQ	in			DDR IO power supply
T7	DDR_VDDQ	in			DDR IO power supply
J8	DDR_VDDQ	in			DDR IO power supply
K8	DDR_VDDQ	in			DDR IO power supply
N7	DDR_VDDQ	in			DDR IO power supply
P7	DDR_VDDQ	in			DDR IO power supply
L7	DDR_VDDQ	in			DDR IO power supply
L8	DDR_VDDQ	in			DDR IO power supply
U6	DDR_VDDQ	in			DDR IO power supply
M8	DDR_VDDQ	in			DDR IO power supply

G9	DDR_VDDQ	in			DDR IO power supply
H7	DDR_VDDQ	in			DDR IO power supply
G10	DDR_VDDQ	in			DDR IO power supply
R7	DDR_VDDQ	in			DDR IO power supply
J7	DDR_VDDQ	in			DDR IO power supply
R8	DDR_VDDQ	in			DDR IO power supply
U7	DDR_VDDQ	in			DDR IO power supply
H8	DDR_VDDQ	in			DDR IO power supply
H6	DDR_VREFI	in			DDR power supply
M6	DDR_VREFI_ZQ	in			DDR power supply
K7	DDR_VREFO_0	out			DDR power supply
M7	DDR_VREFO_1	out			DDR power supply
L6	DDR_ZQ	in			DDR power supply

5.5.18 P/G Interface (242)

Pin No.	Name	Pin Direction	Reset	IO Type	Description
R10	VDD				core power supply
K19	VDD				core power supply
N17	VDD				core power supply
U18	VDD				core power supply
R17	VDD				core power supply
P12	VDD				core power supply
AA13	VDD				core power supply
AA16	VDD				core power supply
P15	VDD				core power supply
N16	VDD				core power supply
Y18	VDD				core power supply
U16	VDD				core power supply
P14	VDD				core power supply
K17	VDD				core power supply
AA15	VDD				core power supply
N14	VDD				core power supply
K18	VDD				core power supply
P11	VDD				core power supply
N13	VDD				core power supply
T17	VDD				core power supply

P17	VDD				core power supply
V15	VDD				core power supply
V19	VDD				core power supply
P16	VDD				core power supply
V18	VDD				core power supply
AA14	VDD				core power supply
L18	VDD				core power supply
U19	VDD				core power supply
Y17	VDD				core power supply
U17	VDD				core power supply
P10	VDD				core power supply
V17	VDD				core power supply
K14	VDD				core power supply
R18	VDD				core power supply
K10	VDD				core power supply
W18	VDD				core power supply
N12	VDD				core power supply
W17	VDD				core power supply
K15	VDD				core power supply
U15	VDD				core power supply
M10	VDD				core power supply
M18	VDD				core power supply
N15	VDD				core power supply
T18	VDD				core power supply
L17	VDD				core power supply
Y19	VDD				core power supply
P19	VDD				core power supply
P13	VDD				core power supply
P18	VDD				core power supply
M17	VDD				core power supply
N19	VDD				core power supply
N10	VDD				core power supply
K16	VDD				core power supply
N11	VDD				core power supply
AA17	VDD				core power supply
N18	VDD				core power supply
V16	VDD				core power supply
L10	VDD				core power supply
AA5	VSS				core ground
M2	VSS				core ground

P8	VSS				core ground
AA8	VSS				core ground
B12	VSS				core ground
AA9	VSS				core ground
J16	VSS				core ground
Y8	VSS				core ground
V9	VSS				core ground
R16	VSS				core ground
Y7	VSS				core ground
V8	VSS				core ground
U20	VSS				core ground
R13	VSS				core ground
P20	VSS				core ground
AF24	VSS				core ground
P21	VSS				core ground
H9	VSS				core ground
R15	VSS				core ground
M19	VSS				core ground
Y15	VSS				core ground
T16	VSS				core ground
AA11	VSS				core ground
T19	VSS				core ground
G13	VSS				core ground
AD2	VSS				core ground
AA21	VSS				core ground
AB9	VSS				core ground
J9	VSS				core ground
T9	VSS				core ground
R12	VSS				core ground
T8	VSS				core ground
H19	VSS				core ground
N8	VSS				core ground
V20	VSS				core ground
R19	VSS				core ground
AB16	VSS				core ground
C18	VSS				core ground
J19	VSS				core ground
M9	VSS				core ground
W13	VSS				core ground
N9	VSS				core ground

J2	VSS				core ground
B15	VSS				core ground
J5	VSS				core ground
Y12	VSS				core ground
L19	VSS				core ground
AA12	VSS				core ground
P9	VSS				core ground
B6	VSS				core ground
H15	VSS				core ground
W15	VSS				core ground
J12	VSS				core ground
T20	VSS				core ground
M5	VSS				core ground
M15	VSS				core ground
K9	VSS				core ground
AB10	VSS				core ground
M14	VSS				core ground
F17	VSS				core ground
E14	VSS				core ground
Y26	VSS				core ground
U8	VSS				core ground
L16	VSS				core ground
L9	VSS				core ground
W19	VSS				core ground
M12	VSS				core ground
W20	VSS				core ground
R9	VSS				core ground
N20	VSS				core ground
M16	VSS				core ground
F2	VSS				core ground
R14	VSS				core ground
AA2	VSS				core ground
R5	VSS				core ground
F5	VSS				core ground
AB15	VSS				core ground
J15	VSS				core ground
AA20	VSS				core ground
R2	VSS				core ground
T12	VSS				core ground
J24	VSS				core ground

M13	VSS				core ground
Y13	VSS				core ground
E8	VSS				core ground
V5	VSS				core ground
W12	VSS				core ground
U21	VSS				core ground
H10	VSS				core ground
P26	VSS				core ground
AB17	VSS				core ground
T15	VSS				core ground
H11	VSS				core ground
AA10	VSS				core ground
T14	VSS				core ground
T13	VSS				core ground
W8	VSS				core ground
J17	VSS				core ground
Y14	VSS				core ground
Y16	VSS				core ground
W16	VSS				core ground
L14	VSS				core ground
W14	VSS				core ground
L12	VSS				core ground
B9	VSS				core ground
B3	VSS				core ground
C21	VSS				core ground
E11	VSS				core ground
U9	VSS				core ground
G12	VSS				core ground
V2	VSS				core ground
J11	VSS				core ground
J10	VSS				core ground
AC21	VSS				core ground
L15	VSS				core ground
AF21	VSS				core ground
Y20	VSS				core ground
L13	VSS				core ground
J14	OTP_VDDIO1V8				OTP IO 1.8v power supply
H14	CA7_AVDD1V8				CA7 PLL 1.8v analog power supply
J13	CA7_AVSS1V8				CA7 PLL analog ground
K11	CA7_VDD				CA7 core power supply

K13	CA7_VDD				CA7 core power supply
M11	CA7_VDD				CA7 core power supply
L11	CA7_VDD				CA7 core power supply
K12	CA7_VDD				CA7 core power supply
AB13	CEVA_AVDD1V8				CEVA PLL 1.8v analog power supply
AB14	CEVA_AVSS1V8				CEVA PLL analog ground
U11	CEVA_VDD				CEVA core power supply
U10	CEVA_VDD				CEVA core power supply
V10	CEVA_VDD				CEVA core power supply
V11	CEVA_VDD				CEVA core power supply
Y11	CEVA_VDD				CEVA core power supply
U14	CEVA_VDD				CEVA core power supply
W10	CEVA_VDD				CEVA core power supply
Y9	CEVA_VDD				CEVA core power supply
R11	CEVA_VDD				CEVA core power supply
Y10	CEVA_VDD				CEVA core power supply
V14	CEVA_VDD				CEVA core power supply
W11	CEVA_VDD				CEVA core power supply
U13	CEVA_VDD				CEVA core power supply
W9	CEVA_VDD				CEVA core power supply
U12	CEVA_VDD				CEVA core power supply
V12	CEVA_VDD				CEVA core power supply
T10	CEVA_VDD				CEVA core power supply
T11	CEVA_VDD				CEVA core power supply
V13	CEVA_VDD				CEVA core power supply
L20	VDD18_EMMC_0				EMMC IO 1.8v power supply for domain-0
M20	VDD18_EMMC_1				EMMC IO 1.8v power supply for domain-1
L21	VDD3_EMMC				EMMC IO 3v power supply
R21	VDD18_SD_0				SD IO 1.8v power supply for domain-0
R20	VDD18_SD_1				SD IO 1.8v power supply for domain-1
T21	VDD3_SD				SD IO 3v power supply
M21	VDD33_RGM				RGM II IO 3.3v power supply
N21	VDD33_RGM				RGM II IO 3.3v power supply
AB19	VP_HDMI	INOUT			HDMI 0.9 V core devices power supply
AC20	VPH_HDMI	INOUT			HDMI 1.8V I/O devices power supply
AB20	VP3V3_TERM_HDMI	INOUT			HDMI 3.3Vtermination resistors analog power supply
AF14	MIPI_AGND				MIPI analog ground
AF4	MIPI_AGND				MIPI analog ground
AF18	MIPI_AGND				MIPI analog ground
AF12	MIPI_AGND				MIPI analog ground

AC11	MIPI_AGND				MIPI analog ground
AC9	MIPI_AGND				MIPI analog ground
AC14	MIPI_AGND				MIPI analog ground
AF8	MIPI_AGND				MIPI analog ground
AB12	MIPI_AVDD1V8				MIPI analog power supply
AB11	MIPI_AVDD1V8				MIPI analog power supply
G14	PCIE_VP				PCIE Low voltage supply
G15	PCIE_VPH				PCIE High voltage supply
H16	PCIE_VPTX				PCIE Transmitter supply voltage
AC18	USB_VDD3V3				USB high-speed SuperSpeed, High-voltage supply
AB18	USB_VDDH3V3				USB high-speed, High-voltage supply
AA19	USB_VP0V9				USB SuperSpeed, low-voltage supply
AA18	USB_DVDD0V9				USB high-speed, low-voltage supply
J18	TYPEC_AVDD				PMA digital core supply
H17	TYPEC_AVDD				PMA transceiver core supply
H18	TYPEC_AVDD_CLK				Clean analog power for HS clock applications
G18	TYPEC_AVDD_H_1V8				High voltage power for the bias and parts of the PLL
G17	TYPEC_AVDD_VH_3V3				AUX 3.3v IO Supply
Y21	VDD18				1.8v digital IO power supply
V21	VDD18				1.8v digital IO power supply
W21	VDD18				1.8v digital IO power supply
V7	VDD18_R				1.8v digital IO power supply for right bar

6. Electrical Specification

6.1 Internal Logic Power Recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Units
Internal digital logic power	VDD	0.8	0.9	1	V
Supply voltage for CUP	CA7_VDD	0.8	0.9	1.1	V
Supply voltage for DSP	CEVA_VDD	0.8	0.9	1.1	V
Supply voltage for OTP	OTP_VDDIO1V8	1.62	1.8	1.98	V

6.2 Digital IO Electrical Characteristics

6.2.1 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital general IO @1.8V	Input Low Voltage	V_{IL}	-0.3		0.63	V
	Input High Voltage	V_{IH}	1.17		1.98	V
	Threshold Point	V_T	0.83	0.91	1	V
	Schmitt Trigger Low to High Threshold Point	V_{T+}	0.95	1.03	1.11	V
		V_{T-}	0.67	0.79	0.9	V
	Input Leakage Current @V_I=1.8V or 0V	I_I			±10μ	A
	Tri-state Output Leakage Current @V_O=1.8V or 0V	I_{OZ}			±10μ	A
	Pull-up Resistor	R_{PU}	54k	80k	120k	Ω
	Pull-down Resistor	R_{PD}	55k	95k	176k	Ω
	Output Low Voltage	V_{OL}			0.45	V
	Output High Volgate	V_{OH}	1.35			V
	Low Level Output Current	I_{OL}				
		00	7.4	12.2	17.4	mA

	@V_{OL}(max)	01	14.8	24.3	34.5	mA
		10	22.1	36.2	51.0	mA
		11	29.3	47.8	66.6	mA
	Low Level Output Current @V_{OH}(min)	I_{OH}				
		00	4.9	11.0	19.8	mA
		01	9.8	21.9	39.5	mA
		10	14.6	32.9	59.1	mA
		11	19.5	43.7	78.6	mA
Digital SD IO	Input Low Voltage	V_{IL}	-0.3		0.7125	V
	Input High Voltage	V_{IH}	1.875		3.15	V
	Threshold Point	V_T	0.81	0.95	1.12	V
	Schmitt Trigger Low to High Threshold Point	V_{T+}	1	1.1	1.23	V
		V_{T-}	0.74	0.9	1.08	V
	Input Leakage Current @V_I=1.8V or 0V	I_I			±10μ	A
	Tri-state Output Leakage Current @V_O=1.8V or 0V	I_{OZ}			±10μ	A
	Pull-up Resistor	R_{PU}	33k	59k	89k	Ω
	Pull-down Resistor	R_{PD}	34k	61k	95k	Ω
	Output Low Voltage	V_{OL}			0.35625	V
	Output High Volgate	V_{OH}	2.1375			V
	Low Level Output Current @V_{OL}(max)	I_{OL}				
		000	3.2	5.4	8.3	mA
		001	4.7	8.0	12.3	mA
		010	6.3	10.7	16.4	mA
		011	7.8	13.2	20.2	mA
		100	9.4	15.9	24.2	mA
		101	10.9	18.4	28.1	mA
		110	12.4	20.9	31.8	mA
		111	13.9	23.4	35.5	mA
	Low Level Output Current @V_{OH}(min)	I_{OH}				
		000	5.0	7.6	11.2	mA
		001	7.5	11.4	16.8	mA

		010	10.0	15.2	22.3	mA
		011	12.4	18.9	27.8	mA
		100	14.9	22.6	33.3	mA
		101	17.4	26.3	38.7	mA
		110	19.8	30.0	44.1	mA
		111	22.3	33.7	49.5	mA
Digital RGMII IO	Input Low Voltage	V_{IL}	-0.3		0.8	V
	Input High Voltage	V_{IH}	2.0		3.465	V
	Threshold Point	V_T	1.02	1.18	1.37	V
	Schmitt Trigger Low to High Threshold Point	V_{T+}	1.23	1.34	1.5	V
		V_{T-}	0.97	1.13	1.33	V
	Input Leakage Current @V_I=1.8V or 0V	I_I			±10μ	A
	Tri-state Output Leakage Current @V_O=1.8V or 0V	I_{OZ}			±10μ	A
	Pull-up Resistor	R_{PU}	26k	46k	71k	Ω
	Pull-down Resistor	R_{PD}	27k	48k	102k	Ω
	Output Low Voltage	V_{OL}			0.4	V
	Output High Volgate	V_{OH}	2.4			V
	Low Level Output Current @V_{OL}(max)	I_{OL}				
		000	4.0	6.3	8.9	mA
		001	6.0	9.4	13.3	mA
		010	8.0	12.6	17.7	mA
		011	10.0	15.6	21.9	mA
		100	12.0	18.7	26.2	mA
		101	14.0	21.8	30.4	mA
		110	15.9	24.7	34.5	mA
		111	17.8	2707	38.5	mA
	Low Level Output Current @V_{OH}(min)	I_{OH}				
		000	6.0	9.3	14.2	mA
		001	9.0	14.0	21.3	mA
		010	12.1	18.6	28.4	mA
		011	15.1	23.3	35.5	mA

Symbol		Parameter	2.5 GT/s	5.0 GT/s	Unit	Comments	
		100	18.1	27.9	42.6	mA	
		101	21.1	32.5	49.7	mA	
		110	24.1	37.2	56.8	mA	
		111	27.1	41.8	63.8	mA	

6.3 PCIE electrical Characteristics

Transmitter Specifications					
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations. See Note 1.
VTX-DIFF-PP	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	As measured with compliance test load. Defined as 2*|VTXD+ - VTXD- |.
VTX-DIFF-PP-LOW	Low power differential p-p Tx voltage swing	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	As measured with compliance test load. Defined as 2*|VTXD+ - VTXD- |. See Note 9.
VTX-DE-RATIO-3.5dB	Tx de-emphasis level ratio	3.0 (min) 4.0 (max)	3.0 (min) 4.0 (max)	dB	See Note 11 for details.
VTX-DE-RATIO-6dB	Tx de-emphasis level	N/A	5.5 (min) 6.5 (max)	dB	See Note 11 for details
TMIN-PULSE	Instantaneous lone pulse width	Not specified	0.9 (min)	UI	Measured relative to rising/falling pulse. See Notes 2, 10.
TTX-EYE	Transmitter Eye including all jitter sources	0.75 (min)	0.75 (min)	UI	Does not include SSC or Refclk jitter. Includes Rj at 10-12. See Notes 2, 3, 4, and 10. Note that 2.5 GT/s and 5.0 GT/s use different jitter determination methods.
TTX-EYE-MEDIAN-to-MAX-JITTER	Maximum time between the jitter median and max deviation from the median	0.125 (max)	Not specified	UI	Measured differentially at zero crossing points after applying the 2.5 GT/s clock recovery function. See Note 2.
TTX-HF-DJ-DD	Tx deterministic jitter > 1.5 MHz	Not specified	0.15 (max)	UI	Deterministic jitter only. See Notes 2 and 10.
TTX-LF-RMS	Tx RMS jitter < 1.5 MHz	Not specified	3.0	ps RMS	Total energy measured over a 10 kHz –1.5 MHz range.

TTX-RISE-FALL	Transmitter rise and fall time	0.125 (min)	0.15 (min)	UI	Measured differentially from 20% to 80% of swing. See Note 2.
TRF-MISMATCH	Tx rise/fall mismatch	Not specified	0.1 (max)	UI	Measured from 20% to 80% differentially. See Note 2.
BWTX-PLL	Maximum Tx PLL bandwidth	22 (max)	16 (max)	MHz	Second order PLL jitter transfer bounding function. See Note 6
BWTX-PLL-LO-3DB	Minimum Tx PLL BW for 3 dB peaking	1.5 (min)	8 (min)	MHz	Second order PLL jitter transfer bounding function. See Notes 6 and 8.
BWTX-PLL-LO-1DB	Minimum Tx PLL BW for 1 dB peaking	Not specified	5 (min)	MHz	Second order PLL jitter transfer bounding function. See Notes 6 and 8.
PKGTX-PLL1	Tx PLL peaking with 8 MHz min BW	Not specified	3.0 (max)	dB	Second order PLL jitter transfer bounding function. See Notes 6 and 8.
PKGTX-PLL2	Tx PLL peaking with 5 MHz min BW	Not specified	1.0 (max)	dB	See Note 8.
RLTX-DIFF	Tx package plus Si differential return loss	10 (min)	10 (min) for 0.05 -1.25 GHz 8 (min) for1.25 -2.5 GHz	dB	
RLTX-CM	Tx package plus Si common mode return loss	6 (min)	6 (min)	dB	Measured over 0.05 – 1.25 GHz range for 2.5 GT/s and 0.05 – 2.5 GHz range for 5.0 GT/s. (S11 parameter)
ZTX-DIFF-DC	DC differential Tx impedance	80 (min) 120 (max)	120 (max)	Ω	Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF.
VTX-CM-AC-PP	Tx AC common mode voltage (5.0	Not specified	100 (max)	mVPP	See Note 5.

	GT/s)				
VTX-CM-AC-P	Tx AC common mode voltage (2.5 GT/s)	20	Not specified	mV	See Note 5.
ITX-SHORT	Transmitter short-circuit current limit	90 (max)	90 (max)	mA	The total current Transmitter can supply when shorted to ground.
VTX-DC-CM	Transmitter DC common-mode voltage	0 (min) 3.6 (max)	0 (min) 3.6 (max)	V	The allowed DC common-mode voltage at the Transmitter pins under any conditions
VTX-CM-DC-ACTIVEIDLE-DELTA	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle.	0 (min) 100 (max)	0 (min) 100 (max)	mV	|VTX-CM-DC [during L0] – VTX-CM-Idle-DC [during Electrical Idle]|<= 100 mV VTX-CM-DC = DC(avg) of |VTX-D+ + VTX-D-|/2 VTX-CM-Idle-DC= DC(avg) of |VTX-D+ + VTX-D-|/2 [Electrical Idle]
VTX-CM-DC-LINEDELTA	Absolute Delta of DC Common Mode Voltage between D+ and D-	0 (min) 25 (max)	0 (min) 25 (max)	mV	|VTX-CM-DC-D+ [during L0] – VTX-CM-DC-D- [during L0.]| ≤ 25mV VTX-CM-DC-D+ = DC(avg) of |VTX-D+| [during L0] VTX-CM-DC-D- = DC(avg) of |VTX-D-| [during L0]
VTX-IDLE-DIFF-AC-p	Electrical Idle Differential Peak Output Voltage	0 (min) 20 (max)	0 (min) 20 (max)	mV	VTX-IDLE-DIFFp = |VTX-Idle-D+ - VTx-Idle-D-| ≤ 20 mV. Voltage must be high pass filtered to remove any DC component.
VTX-IDLE-DIFF-DC	DC Electrical Idle Differential Output Voltage	Not specified	0 (min) 5 (max)	mV	VTX-IDLE-DIFF-DC = |VTX-Idle-D+ - VTx-Idle-D-| ≤ 5 mV. Voltage must be low pass filtered to remove any AC component. Filter characteristics complementary to above.
VTX-RCV-DETECT	The amount of voltage change	600 (max)	600 (max)	mV	The total amount of voltage change in a positive direction that a Transmitter can apply to sense

	allowed during Receiver Detection				whether a low impedance Receiver is present. Note: Receivers display substantially different impedance for VIN <0 vs VIN > 0.
TTX-IDLE-MIN	Minimum time spent in Electrical Idle	20 (min)	20 (min)	ns	Minimum time a Transmitter must be in Electrical Idle.
TTX-IDLE-SET-TOIDLE	Maximum time to transition to a valid Electrical Idle after sending an EIOS	8 (max)	8 (max)	ns	After sending the required number of EIOSs, the Transmitter must meet all Electrical Idle specifications within this time. This is measured from the end of the last UI of the last EIOS to the Transmitter in Electrical Idle.
TTX-IDLE-TO-DIFFDATA	Maximum time to transition to valid diff signaling after leaving Electrical Idle	8 (max)	8 (max)	ns	Maximum time to transition to valid diff signaling after leaving Electrical Idle. This is considered a debounce time to the Tx.
TCROSSLINK	Crosslink random timeout	1.0 (max)	1.0 (max)	ms	This random timeout helps resolve potential conflicts in the crosslink configuration.
LTX-SKEW	Lane-to-Lane Output Skew	500 ps + 2 UI (max)	500 ps + 4 UI (max)	ps	Between any two Lanes within a single Transmitter.
CTX	AC Coupling Capacitor	75 (min) 200 (max)	75 (min) 200 (max)	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
Notes	1. SSC permits a +0, - 5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz. 2. Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although deconvolution is recommended. At least 106 UI of data must be acquired. 3. Transmitter jitter is measured by driving the Transmitter under test with a low jitter				

	"ideal" clock and connecting the DUT to a reference load. 4. Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5 GT/s and 5.0 GT/s use different filter functions. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins. 5. Measurement is made over at least 106 UI. 6. The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table. 7. Measurements are made for both common mode and differential return loss. The DUT must be powered up and DC isolated, and its data+/data- outputs must be in the low-Z state at a static value 8. A single combination of PLL BW and peaking is specified for 2.5 GT/s implementations. For 5.0 GT/s, two combinations of PLL BW and peaking are specified to permit designers to make a tradeoff between the two parameters. If the PLL's min BW is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. In both cases, the max PLL BW is 16 MHz. 9. Low swing output, defined by VTX-DIFF-PP-LOW must be implemented with no de-emphasis. 10. For 5.0 GT/s, de-emphasis timing jitter must be removed. An additional HPF function must be applied. This parameter is measured by accumulating a record length of 106 UI while the DUT outputs a compliance pattern. TMIN-PULSE is defined to be nominally 1 UI wide and is bordered on both sides by pulses of the opposite polarity. 11. Root complex Tx de-emphasis is configured from Upstream controller. Downstream Tx de-emphasis is set via a command, issued at 2.5 GT/s.				
Receiver Specifications					
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	UI does not account for SSC caused variations.
VRX-DIFF-PP-CC	Differential Rx peak-peak voltage for common Refclk Rx architecture	0.175 (min) 1.2 (max)	0.120 (min) 1.2 (max)	V	
VRX-DIFF-PP-DC	Differential Rx peak-peak voltage for data clocked	0.175 (min) 1.2 (max)	0.100 (min) 1.2 (max)	V	

	Rx architecture				
TRX-EYE	Receiver eye time opening	0.40 (min)	N/A	UI	Minimum eye time at Rx pins to yield a 10-12 BER. See Note 1.
TRX-TJ-CC	Max Rx inherent timing error	N/A	0.40 (max)	UI	Max Rx inherent total timing error for common Refclk Rx architecture. See Note 2.
TRX-TJ-DC	Max Rx inherent timing error	N/A	0.34 (max)	UI	Max Rx inherent total timing error for data clocked Rx architecture. See Note 2.
TRX-DJ-DD-CC	Max Rx inherent deterministic timing error	N/A	0.30 (max)	UI	Max Rx inherent deterministic timing error for common Refclk Rx architecture. See Note 2.
TRX-DJ-DD-DC	Max Rx inherent deterministic timing error	N/A	0.24 (max)	UI	Max Rx inherent deterministic timing error for data clocked Rx architecture. See Note 2.
TRX-EYE-MEDIAN-to-MAX-JITTER	Max time delta between median and deviation from median	0.3 (max)	Not specified	UI	Only specified for 2.5 GT/s.
TRX-MIN-PULSE	Minimum width pulse at Rx	Not specified	0.6 (min)	UI	Measured to account for worst Tj at 10-12 BER.
VRX-MAX-MIN-RATIO	min/max pulse voltage on consecutive UI	Not specified	5 (max)	--	Rx eye must simultaneously meet VRX_EYE limits.
BWRX-PLL-HI	Maximum Rx PLL bandwidth	22 (max)	16 (max)	MHz	Second order PLL jitter transfer bounding function . See Note 3.
BWRX-PLL-LO-3DB	Minimum Rx PLL BW for 3 dB peaking	1.5 (min)	8 (min)	MHz	Second order PLL jitter transfer bounding function. See Note 3.
BWRX-PLL-LO-1DB	Minimum Rx PLL BW for 1 dB peaking	Not specified	5 (min)	MHz	Second order PLL jitter transfer bounding function. See Note 3.
PKGRX-PLL1	Rx PLL peaking with 8 MHz min BW	Not specified	3.0	dB	Second order PLL jitter transfer bounding function . See Note 3.
PKGRX-PLL2	Rx PLL	Not	1.0	dB	Second order PLL jitter transfer

	peaking with 5 MHz min BW	specified			bounding function. See Note 3.
RLRX-DIFF	Rx package plus Si differential return loss	10 (min)	10 (min) for 0.05 - 1.25 GHz 8 (min) for 1.25 - 2.5 GHz	dB	See Note 4.
RLRX-CM	Common mode Rx return loss	6 (min)	6 (min)	dB	See Note 4.
ZRX-DC	Receiver DC common mode impedance	40 (min) 60 (max)	40 (min) 60 (max)	Ω	DC impedance limits are needed to guarantee Receiver detect. See Note 5.
ZRX-DIFF-DC	DC differential impedance	80 (min) 120 (max)	Not specified	Ω	For 5.0 GT/s covered under RLRX-DIFF parameter. See Note 5.
VRX-CM-AC-P	Rx AC common mode voltage	150 (max)	150 (max)	mVP	Measured at Rx pins into a pair of 50 Ω terminations into ground. See Note 6.
ZRX-HIGH-IMP-DCPOS	DC Input CM Input Impedance for V>0 during Reset or power down	50 k (min)	50 k (min)	Ω	Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 200 mV with respect to ground. See Note 7.
ZRX-HIGH-IMP-DCNEG	DC Input CM Input Impedance for V<0 during Reset or power down	1.0 k (min)	1.0 k (min)	Ω	Rx DC CM impedance with the Rx terminations not powered, measured over the range -150 – 0 mV with respect to ground. See Note 7.
VRX-IDLE-DETDIFFp-p	Electrical Idle Detect Threshold	65 (min) 175 (max)	65 (min) 175 (max)	mV	VRX-IDLE-DET-DIFFp-p = 2*|VRX-D+ - VRXD-|. Measured at the package pins of the Receiver.
TRX-IDLE-DET-DIFFENTERTIME	Unexpected Electrical Idle Enter Detect	10 (max)	10 (max)	ms	An unexpected Electrical Idle (VRXDIFFp-p < VRX-IDLE-DET-DIFFp-p) must be

	Threshold Integration Time				recognized no longer than TRX-IDLEDET-DIFF-ENTERTIME to signal an unexpected idle condition.
LRX-SKEW	Lane to Lane skew	20 (max)	8 (max)	ns	Across all Lanes on a Port. This includes variation in the length of a SKP Ordered Set at the Rx as well as any delay differences arising from the interconnect itself. See Note 8.
Notes	1. Receiver eye margins are defined into a 2 x 50 Ω reference load. 2. The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing. 3. Two combinations of PLL BW and peaking are specified at 5.0 GT/s to permit designers to make tradeoffs between the two parameters. If the PLL's min BW is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. Note: a PLL BW extends from zero up to the value(s) defined as the min or max in the above table. For 2.5 GT/s a single PLL bandwidth and peaking value of 1.5-22 MHz and 3.0 dB are defined. 4. Measurements must be made for both common mode and differential return loss. In both cases the DUT must be powered up and DC isolated, and its D+/D- inputs must be in the low-Z state. 5. The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered. 6. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V-CMDC|}. 7. ZRX-HIGH-IMP-DC-NEG and ZRX-HIGH-IMP-DC-POS are defined respectively for negative and positive voltages at the input of the Receiver. Transmitter designers need to comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits. 8. The LRX-SKEW parameter exists to handle repeaters that regenerate Refclk and introduce differing numbers of skips on different Lanes.				

6.4 TYPEC electrical Characteristics

6.4.1 Operating Conditions

Name	Min	Typ	Max	Units	Description
$V_{avdd\_cmn\_clk}$	0.813	0.9	1.0	V	Core supply voltage at the junction. Refer to Table 'Power supply budget'.
V_{avdd_h}	1.58	1.8	1.994	V	IO supply voltage at the junction. Refer to Table 'Power supply budget'
$V_{avdd\_tx\_<>}$	0.813	0.9	1.0	V	Core supply voltage at the junction. Refer to Table 'Power supply budget'.
V_{avdd_xcvr}	0.813	0.9	1.0	V	Core supply voltage at the junction. Refer to Table 'Power supply budget'.
$V_{avdd\_xcvr\_clk\_<>}$	0.813	0.9	1.0	V	Core supply voltage at the junction. Refer to Table 'Power supply budget'.
T_j	-40	25	125	℃	Junction temperature

6.4.2 Power supply budgeting

Name	Voltage			Description
	Min	Typ	Max	
Supply Budgeting for avdd and avdd_clk: 0.9V				
Off die VRM DC variation	-3.50%		8.50%	On board voltage regulator DC accuracy.
Off die VRM AC VRM noise	2.00%			Peak-to-peak 18mV frequency content: 50KHz to 500KHz
	1.00%			Peak-to-peak 9mV with frequency content: 500KHz to 10MHz; no single frequency noise amplitude can be more than 5mV.
Off die total supply variation	-5.0%	-	10.0%	Total off-die voltage variation at package pin of supply die to external voltage regulator.
AC Self Induced + Coupling Noise	1.70%			This 15.3mV peak-to-peak noise due to switching current through package parasitics. This is wideband.
Package IR (DC) drop	-1.0%	-	0.00%	The 9mV IR drop is due to worst case DC current of the PHY.
On die IR (DC) drop	-2.50%	-	0.00%	The 22.5mV drop is due to worst case DC current and worst case metal routing

				parasitic.
Final Voltage range (V)	0.813	0.90	1.00	This is the expected voltage at the junction. It includes 2.7mV margin for the design.

Name	Voltage			Description
	Min	Typ	Max	
Supply Budgeting for 1.8V IO supply (avdd_h)				
Off die VRM DC variation	-8.50%		8.50%	On board voltage regulator DC accuracy.
Off die VRM AC VRM noise	2.00%			Peak-to-peak 36mV frequency content: 50KHz to 500KHz
	1.00%			Peak-to-peak 18mV with frequency content: 500KHz to 10MHz.
Off die total supply variation	-10.0%	-	10.0%	Total off-die voltage variation at package pin of supply due to external voltage regulator.
AC Self Induced + Coupling Noise	0.50%			This 9mV peak-to-peak noise is due to switching current through package parasitics. This is wideband.
Package IR (DC) drop	-0.5%	-	0.00%	This 9mV IR drop is due to worst case DC current of the PHY
On die IR (DC) drop	-1.00%	-	0.00%	This 18mV drop is due to worst case DC current and worst case metal routing parasitic.
Final Voltage range (V)	-1.58	1.8	1.994	This is the expected voltage at the junction. It includes 0.5mV margin for the design.

6.4.3 Common Electrical Specifications

6.4.3.1 Reference Clock Input Specifications

Minimize exposure to nearby aggressor signals that could contaminate the clock with crosstalk, especially if these signals are lower than 1MHz in frequency.
If these bumps are not used, it is not necessary to AC couple or terminate these pins. They can be left floating.

Reference clock specification for USB3 and DP

Normative Electrical Parameters	Min	Typ	Max	Units	Description
External Clock Frequency	-	24	-	MHz	-
Input Duty Cycle	48	-	52	%	-
Single-ended clock input voltage (CMOS level)	0.85	-	1	V	-
Input Random Jitter	-	-	140	dBC/ Hz	Noise floor density from 10 KHz to 10 MHz
	-	-	2.9	ps	For a 24MHz reference,integrated jitter from 10KHz to 10MHz
Input determinestic Jitter	-	-	4	ps	Over a band of 10KHz to 10MHz

6.4.3.2 DP Transmitter electrical specification

DP Transmitter module electrical Specifications

Symbol	Description	Min	Typ	Max	Units	Comments
UI	UI_HBR2	185.129	185	186.172	ps	-Unit Interval for high bit rate (DP: 5.4Gbps/ lane). Frequency ppm -5300 to +300
	USB3	199.94	200	200.06		UI with ± 300ppm with-out SSC
	UI_HBR	370.259	370	372.343		Unit Interval for high bit rate (DP: 2.7Gbps/ lane). Frequency ppm -5300 to +300
	UI_RBR	617.098	617	620.573		Unit Interval for high bit rate (DP: 1.62Gbps/ lane). Frequency ppm -5300 to +300
$V_{TX-DIFFp-p}$	Differential p-p TX voltage swing including low power	100	-	1200	mV	For USB 3.0, no EQ is required.
$I_{TX-SHORT}$	Transmit lane short-circuit current	-	-	100	mA	-

$RL_{TX-DIFF}$	Transmitter differential return loss	-	-	0 < -20dB < 100Mhz 100Mhz < -18dB < 300Mhz 300Mhz < -16dB < 600Mhz 600Mhz < -10dB < 2500Mhz 2500Mhz < -9dB < 4875Mhz 4875Mhz < -8dB < 11200Mhz 11200Mhz < -5dB < 16800Mhz and -3dB beyond that	db	
RL_{TX-CM}	Transmitter common mode return loss	-	-	50Hz < -8dB < 15000Mhz	dB	
Z_{TX_cal}	DC differential TX impedance. Cali-brated differential driver imped-ance when in normal mode.	80	100	120	Ω	
$T_{20-80TX}$	TX Rise/Fall Time	-	-	0.41	UI	
T_{skewTX}	TX Differential Skew	20	-	30	ps	
J_{TT}	Transmitter total jitter (peak-to-peak) (Tj)	-	-	65		USB3.0
		-	-			Edp/dp
$T_{TX-RJ-PLL}$	Random jitter (Max)	-	-	1.4	Ps rms	USB3.0 and DP is after TXLF
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to	-	-	8	ns	

	valid diff signaling after leaving Electrical Idle					
T_{EIExit}	Time to exit Electrical Idle (L0s) state and to enter L0	-	-	5	Txsys-clk	

6.5 USB electrical Characteristics

Power Supply	Ball Name	Value
High-voltage power supply	USB_VDD3V3	3.3 V (+ 10%, - 7%) at the macro pins with respect to gd (ground)
High-voltage power supply	USB_VDDH3V3	3.3 V (+ 10%, - 7%) at the macro pins with respect to gd (ground)
Low-voltage supply	USB_DVDD0V9	0.90 V (+ 10%, - 7%) at the macro pins with respect to gd (ground)
Low-voltage supply	USB_VP0V9	0.90 V (+ 10%, - 7%) at the macro pins with respect to gd (ground)

6.5.1 USB 3.0 Transmitter Normative Electrical Parameters

Symbol	Parameter	5.0 GT/s	Units	Comments
UI	Unit Interval	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each device. Period does not account for SSC induced variations
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX-DE-RATIO}$	Tx de-emphasis	3.0 (min) 4.0 (max)	dB	Nominal is 3.5 dB
$R_{TX-DIFF-DC}$	DC differential impedance	72 (min) 120 (max)	Ω	
$V_{TX-RCV-DETECT}$	The amount of voltage change	0.6 (max)	V	Detect voltage transition should be an

	allowed during Receiver Detection			increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an “off” receiver’s input goes below ground. See Section 1.2.5.6 and Note 9 for details
$C_{AC-COUPLING}$	AC Coupling Capacitor	75 (min) 200 (max)	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$T_{CDR\_SLEW\_MAX}$	Max slew rate	10	ms/sec	See the jitter white paper for details on this measurement.
$T_{MIN-PULSE-Dj}$	Deterministic min pulse	0.96	UI	Tx pulse width variation that is deterministic.
$T_{MIN-PULSE-Tj}$	Tx min pulse	0.90	UI	Min Tx pulse at 10^{-12} including Dj and Rj.
T_{TX-EYE}	Transmitter Eye	0.625 (min)	UI	Includes all jitter sources
$T_{TX—DJ-DD}$	Tx deterministic jitter	0.19 (max)	UI	Deterministic jitter only assuming the Dual Dirac distribution
$C_{TX-PARASITIC}$	Tx input capacitance for return loss	1.25 (max)	pf	Parasitic capacitance to ground
R_{TX-DC}	Transmitter DC common mode impedance	18 (min) 30 (max)	Ω	DC impedance limits to guarantee Receiver detect behavior. Measured with respect to AC ground over a voltage of 0-500mV.
$I_{TX-SHORT}$	Transmitter shortcircuit current limit	60 (max)	mA	The total current Transmitter can supply when shorted to ground.
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0 (min) 2.2 (max)	V	The instantaneous allowed DC common-mode voltages at the connector side of the AC coupling capacitors.
$V_{TX-CM-ACPP\_ACTIVE}$	Tx AC common mode voltage active	100 mv	mVPP	Max mismatch from D+ D- for both time and amplitude. While signaling.
$V_{TX-CM-DC-ACTIVEIDLE-DELTA}$	Absolute Common Mode Voltage between *U1* and *U0*	200 (max)	mV	peak
$V_{TX-IDLE-DIFF-AC-pp}$	Electrical Idle Differential Peak – Peak Output Voltage	0 (min) 10 (max)	mV	
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	0 (min) 10 (max)	mV	Voltage must be low pass filtered to remove any AC component. This limits the common mode error when resuming U1 to U0

6.5.2 USB 3.0 Receiver Electrical Parameters

Symbol	Parameter	5.0 GT/s	Units	Comments
UI	Unit Interval	199.94 (min) 200.06 (max)	ps	UI does not account for SSC caused variations.
$V_{RX-DIFF-PP-POST-EQ}$	Differential Rx peakpeak voltage	*30* (min)	mV	Measured after the Rx EQ function
T_{RX-TJ}	Max Rx inherent timing error	*0.45* (max)	UI	Measured after the Rx EQ function
$T_{RX-DJ-DD}$	Max Rx inherent deterministic timing error	*0.3* (max)	UI	Max Rx inherent deterministic timing error
$C_{RX-PARASITIC}$	Rx input capacitance for return loss	1.1 (max)	pf	
R_{RX-DC}	Receiver DC common mode impedance	18 (min) 30 (max)	Ω	DC impedance limits are needed to guarantee Receiver detect. Measured with respect to ground over a voltage of 500 mV max.
$R_{RX-DIFF-DC}$	DC differential impedance	72 (min) 120 (max)	Ω	
$V_{RX-CM-AC-P}$	Rx AC common mode voltage	150 (max)	mV Peak	Measured at Rx pins into a pair of 50 Ω terminations into ground. Includes Tx and channel conversion, AC range up to 5 GHz
$V_{RX-CM-DC-ACTIVEIDLE-DELTA\_P}$	Rx AC common mode voltage during the U1 to U0 transition	200 (max)	mV Peak	Measured at Rx pins into a pair of 50 Ω terminations into ground. Includes Tx and channel conversion, AC range up to 5 GHz
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input CM Input Impedance for V>0 during Reset or power down	25 k (min)	Ω	Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 500 mV with respect to ground.
$V_{RX-LFPS-DET-DIFFp-p}$	LFPS Detect Threshold	100 (min) 300 (max)	mV	Below the min is noise Must wake up above the max.

6.6 HDMI Electrical Characteristics

DC Characteristics	
Item	value
Input Differential Voltage Level. V_{idiff}	150≤ V_{idiff} ≤ 1200mV
Input Common Mode Voltage, V_{icm} V_{icm1}	If Sink supports only <=165M: $(AV_{cc} - 300mV) \leq V_{icm1} \leq (AV_{cc} - 37.5mV)$

	If sink supports >165Mhz $(AV_{cc} - 400mV) \leq V_{icm1} \leq (AV_{cc} - 37.5mV)$
V_{icm2}	$AV_{cc} \pm 400mV$
When source Disabled or disconnected	
Differential Voltage level	$AV_{cc} \pm 10mV$
AC input characteristics	
Minimum differential sensitivity (peak-to-peak)	150 mV
Maximum differential input (peak-to-peak)	1560mV
Max Allowable Intra-Pair Skew at Sink Connector	For TMDS Clock rates 222.75MHz and below: 0.4 T_{bit} For TMDS Clock rates above 222.75MHz: 0.15 T_{bit} + 112psecs
Max Allowable Inter-Pair Skew at Sink Connector	0.2 $T_{character}$ + 1.78nsecs
TMDS Clock Jitter	0.30 T_{bit}
Impedance Characteristics	
TDR Rise Time at TP2 (10%-90%)	≤200 psec
Through connection impedance	100 ohms ±15%
At Termination impedance (when V_{icm} is within V_{icm1} range)	100 ohms ±10%
At Termination impedance (when V_{icm} is within V_{icm2} range)	100 ms ±10%

6.7 MIPI Electrical Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Input DC Specifications						
VI	Input signal voltage range		-50		1350	mv
I_{LEAK}	Input leakage current	Note1	-10		10	μA
V_{GNDSH}	Ground shift		-50		50	mv
$V_{OH(absmax)}$	Maximum transient output voltage level		-0.15		1.45	v
$t_{VOH(absmax)}$	Maximum transient time above VOH(absmax)				20	ns
HS Line Drivers DC Specifications						
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	Note2	140	200	270	mv
$\Delta\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	Note2			14	mv
V_{CMTX}	Steady-state common-mode output voltage	Note2	150	200	250	mv
$\Delta V_{CMTX(1,0)}$	Changes in steady-state common-mode output voltage between logic states	Note2			5	mv
V_{OHHS}	HS output high voltage	Note2			360	mv
Z_{OS}	Single-ended output impedance		40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch				10	%
NOTE	1.					
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage		-50		50	mv
V_{OH}	Output high-level SE voltage		1.1	1.2	1.3	v
Z_{OLP}	Single-ended output impedance		110			Ω
$\Delta Z_{OLP(01,10)}$	Single-ended output impedance mismatch driving opposite level				20	%
$\Delta Z_{OLP(00,11)}$	Single-ended output impedance mismatch driving same level				5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold				70	mv
V_{IDTL}	Differential input low voltage threshold		-70			mv
V_{IHHS}	Single ended input high voltage				460	mv

V_{ILHS}	Single ended input low voltage		-40			mv
V_{CMRXDC}	Input common mode voltage		70		330	mv
Z_{ID}	Differential input impedance		80		125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage				550	mv
V_{Ih}	Input high voltage		880			mv
V_{HYST}	Input hysteresis		25			mv
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold				200	mv
V_{IHF}	Input high fault threshold		450			mv
HS Line Drivers AC Specifications						
F_{DDRCLK}	DDR CLK frequency	On CLKP/N outputs	40		750	MHz
UI_{INST}	UI instantaneous	Note3			12.5	ns
ΔUI	UI variation	Note4	-10%		10%	UI
		Note5	-5%		5%	UI
t_{CDC}	DDR CLK duty cycle	$t_{CDC}=t_{CPH}/P_{DDRCLK}$		50		%
t_{CPH}	DDR CLK high time			1		UI
t_{CPL}	DDR CLK low time			1		UI
-	DDR CLK / DATA Jitter	Note6		75		ps pk-pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew			0.075		UI
$t_{SKEW[TX]}$	Data to Clock Skew	Note7	-0.15		0.15	UI
		Note8	-0.20		0.20	UI
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time	Note9	0.15			UI
		Note10	0.20			UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time	Note9	0.15			UI
		Note10	0.20			UI
t_r	Differential output signal rise time	20% to 80%, R_L = 50 Ω, Note11			0.30	UI
		20% to 80%, R_L = 50 Ω, Note12			0.35	UI
		20% to 80%, R_L = 50 Ω, Note13	100			ps
t_f	Differential output signal fall time	20% to 80%, R_L = 50 Ω, Note11			0.30	UI
		20% to 80%, R_L = 50 Ω, Note12			0.35	UI
		20% to 80%, R_L = 50 Ω, Note13	100			ps

$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω ≤ R_L ≤ 125 Ω			15	mVrms
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz	80 Ω ≤ R_L ≤ 125 Ω			25	mVp
LP Line Drivers AC Specifications						
t_{rlp} , t_{flp}	Single ended output rise/fall time	15% to 85%, C_L < 70 pF			25	ns
t_{reot}		30% to 85%, C_L < 70 pF			35	ns
$\partial V/\partial t_{SR}$	Signal slew rate	15% to 85%, C_L < 70 pF,Note14			150	mV/ns
C_L	Load capacitance	Note15	0		70	pF
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz				200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz		-50		50	mVpp
C_{CM}	Common mode termination	Note16			60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection				300	V.ps
T_{MIN}	Minimum pulse response		20			ns
V_{INT}	Pk-to-Pk interference voltage				400	mVpp
f_{INT}	Interference frequency		450			MHZ

Note

1. $V_{GNDSH(min)} \le V_I \le V_{GNDSH(max)} + V_{OH(absmax)}$. Lane module in LP receive mode.
2. 80 Ω ≤RL≤125 Ω
3. This value corresponds to a minimum Mbps data rate.
4. When UI ≥ 1ns, within a single burst.
5. When UI < 1ns, within a single burst.
6. Jitter specification with clean clock at REFCLK input.
7. Total silicon and package skew delay budget of 0.3*UI_{INST} when D-PHY is supporting maximum data rate = 1 Gbps.
8. Total silicon and package skew delay budget of 0.4* UI_{INST} when D-PHY is supporting maximum data rate > 1 Gbps.
9. Total setup and hold window for receiver of 0.3* UI_{INST} when D-PHY is supporting maximum data rate = 1 Gbps.
10. Total setup and hold window for receiver of 0.4* UI_{INST} when D-PHY is supporting maximum data rate > 1 Gbps.
11. Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).
12. Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).
13. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.

	14. Measured as average across any 50 mV of the output signal transition. 15. C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. 16. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

6.8 DDR Electrical Characteristics

6.8.1 Absolute Maximum DC Ratings

Symbol	Description	Rating	Units
DDR_VDD_AMAX	Voltage on VDD pin relative to VSS	-0.5 to 1.05	V
DDR_VDDQ_AMAX	Voltage on VDDQ pin relative to VSS	-0.5 to 1.98	V
DDR_PLL_AMAX	Voltage on VAA_PLL pin relative to VSS	-0.5 to 1.98	V

6.8.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Units
DDR_VDD_PLL	PLL and SSTL receiver supply voltage	1.62	1.8	1.98	V
DDR_VDDQ_4	SSTL output supply voltage (DDR4)	1.14	1.2	1.26	V
DDR_VDDQ_3	SSTL output supply voltage (DDR3)	1.425	1.5	1.575	V
DDR_VDDQ_3L	SSTL output supply voltage (DDR3L)	1.283	1.35	1.45	V
DDR_VDDQ_3U	SSTL output supply voltage (DDR3U)	1.19	1.25	1.31	V
DDR_VDDQ_L3	SSTL output supply voltage (LPDDR3)	1.14	1.2	1.3	V
DDR_VDDQ_LP	SSTL output supply voltage (LVCMOS)	1.65	1.8	1.95	V
DDR_VREF	SSTL reference supply voltage	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V
DDR_VTT	External termination voltage	VREF-40mV	VREF	VREF+40mV	V
DDR_T	Junction temperature	-40	25	125	℃

6.8.3 DC Characteristics

	Symbol	Parameter	Min	Typ	Max	Units
DDR4_Mode	DDR_VIH(DC)	DC input voltage High	VREF+0.1		VDDQ	V
	DDR_VIL(DC)	DC input voltage Low	VSSQ		VREF-0.1	V
	DDR_VOH	DC output logic High	0.9*VDDQ			V
	DDR_VOL	DC output logic Low			0.1*VDDQ	V
	DDR_RTT	Input termination resistance (ODT) to V_{DDQ}	200	240	280	ohm
			100	120	140	
			67	80	93	
			50	60	70	
			42	48	56	
			34	40	46	
			28	34	40	
DDR3_Mode	DDR_VIH(DC)	DC input voltage High	VREF+0.1		VDDQ	V
	DDR_VIL(DC)	DC input voltage Low	VSSQ-0.3		VREF-0.1	V
	DDR_VOH	DC output logic High	0.8*VDDQ			V
	DDR_VOL	DC output logic Low			0.2*VDDQ	V
	DDR_RTT	Input termination resistance (ODT) to VDDQ/2	100	120	140	ohm
			54	60	66	
			36	40	44	
DDR3L_Mode	DDR_VIH(DC)	DC input voltage High	VREF+0.09		VDDQ	V
	DDR_VIL(DC)	DC input voltage Low	VSSQ-0.3		VREF-0.09	V
	DDR_VOH	DC output logic High	0.8*VDDQ			V
	DDR_VOL	DC output logic Low			0.2*VDDQ	V
	DDR_RTT	Input termination resistance (ODT) to VDDQ/2	100	120	140	ohm
			54	60	66	
			36	40	44	
LPDDR3_Mode	DDR_VIH(DC)	DC input voltage High	VREF+0.1		VDDQ	V
	DDR_VIL(DC)	DC input voltage Low	VSSQ		VREF-0.1	V
	DDR_VOH	DC output logic High	0.9*VDDQ			V
	DDR_VOL	DC output logic Low			0.1*VDDQ	V
	DDR_RTT	Input termination resistance (ODT) to VDDQ	100	120	140	ohm
			200	240	280	

6.8.4 Recommended Operating Frequency

	Symbol	Parameter	Condition	Min	Typ	Max	Unit
DDR4_Mode	ddr_data_rate	DDR data rate	1.0V, 25℃				Mbps
			1.1V, -40℃				
			0.9V, 125℃			2400	
DDR3_Mode	ddr_data_rate	DDR data rate	1.0V, 25℃				Mbps
			1.1V, -40℃				
			0.9V, 125℃			2133	
DDR3L_Mode	ddr_data_rate	DDR data rate	1.0V, 25℃				Mbps
			1.1V, -40℃				
			0.9V, 125℃			1866	
LPDDR3_Mode	ddr_data_rate	DDR data rate	1.0V, 25℃				Mbps
			1.1V, -40℃				
			0.9V, 125℃			2133	

6.8.5 Electrical Characteristics for DDR IO

	Symbol	Parameter	Min	Typ	Max	Units
DDR4_Mode	DDR_C_IO	I/O capacitance (equivalent at VDDQ/2)	1.94	1.97	2.11	pF
	DDR_PRCVQ_AC	Input mode AC power (VDDQ rail)	0.17	0.20	0.23	uW/MHz
	DDR_PRCV_AC	Input mode AC power (VDD rail)	0.13	0.15	0.22	uW/MHz
	DDR_PDRVQ_AC	Output mode AC power (VDDQ rail)	8.08	8.08	9.77	uW/MHz
	DDR_PDRV_AC	Output mode AC power (VDD rail)	1.34	1.67	2.27	uW/MHz
DDR3_Mode	DDR_C_IO	I/O capacitance (equivalent at VDDQ/2)	1.91	1.94	2.07	pF
	DDR_PRCVQ_AC	Input mode AC power (VDDQ rail)	0.20	0.21	0.24	uW/MHz
	DDR_PRCV_AC	Input mode AC power (VDD rail)	0.13	0.15	0.19	uW/MHz
	DDR_PDRVQ_AC	Output mode AC power (VDDQ rail)	10.83	10.83	12.35	uW/MHz
	DDR_PDRV_AC	Output mode AC power (VDD rail)	1.35	1.68	2.27	uW/MHz

DDR3L_Mode	DDR_C_IO	I/O capacitance (equivalent at VDDQ/2)	1.92	1.96	2.09	pF
	DDR_PRCVQ_AC	Input mode AC power (VDDQ rail)	0.20	0.22	0.26	uW/MHz
	DDR_PRCV_AC	Input mode AC power (VDD rail)	0.13	0.15	0.22	uW/MHz
	DDR_PDRVQ_AC	Output mode AC power (VDDQ rail)	8.43	8.43	10.76	uW/MHz
	DDR_PDRV_AC	Output mode AC power (VDD rail)	1.34	1.67	2.27	uW/MHz
LPDDR3_Mode	DDR_C_IO	I/O capacitance (equivalent at VDDQ/2)	1.94	1.97	2.11	pF
	DDR_PRCVQ_AC	Input mode AC power (VDDQ rail)	0.20	0.23	0.26	uW/MHz
	DDR_PRCV_AC	Input mode AC power (VDD rail)	0.12	0.15	0.22	uW/MHz
	DDR_PDRVQ_AC	Output mode AC power (VDDQ rail)	7.38	7.38	9.17	uW/MHz
	DDR_PDRV_AC	Output mode AC power (VDD rail)	1.34	1.67	2.27	uW/MHz

6.9 ABB/PLL Electrical Characteristics

Reference Clock Electrical Parameters	Min.	Typ.	Max.	Units	Description
External Clock Frequency		20/40		MHz	CLKREF_SEL_PAD='0': 40MHz input CLKREF_SEL_PAD='1': 20MHz input A 20MHz crystal may also be used
Input Duty Cycle	49	50	51	%	
Single-ended clock input voltage (CMOS or sinewave)	0.8	1	1.2	V	
frequency accuracy	-20	0	20	ppm	
Input Jitter			2.5	ps	

Analog Signal Electrical Parameters	Min.	Typ.	Max.	Units	Description
DAC OUTPUTS	0	0.9	1.8	V	DAC outputs typical 0.65~1.15V
ADC INPUTS	0	0.9	1.8	V	ADC inputs typical 0.65~1.15V

AD INPUTS	0	0.9	1.8	V	AD inputs typical 0~1.8V
Other analog PAD	0		1.8	V	

Analog and PLL power suppy Electrical Parameters	Min.	Typ.	Max.	Units	Description
AVDD		1.8	1.98	V	1.8V analog power supply for ABB and PLL
AVSS	-0.2	0	0.2	V	analog ground for ABB and PLL