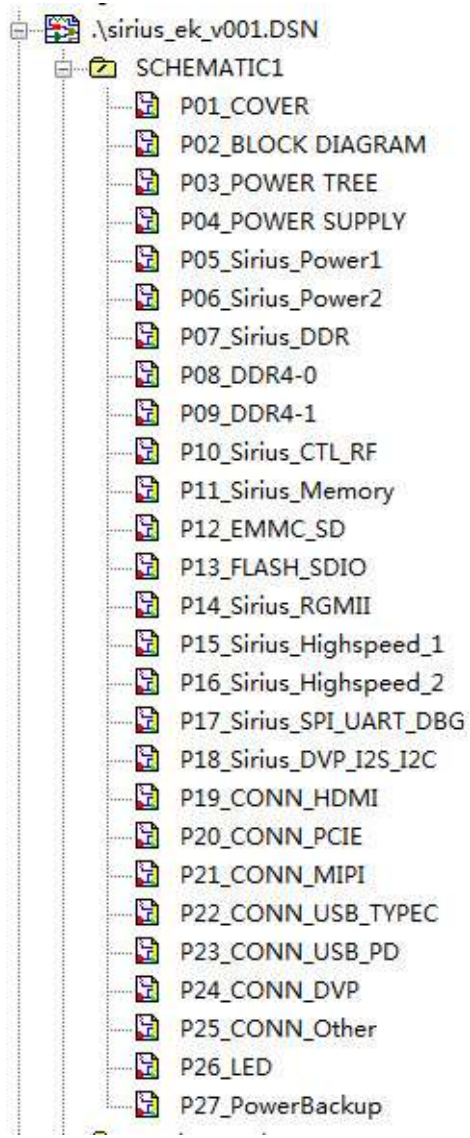
D

C

B

A



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Designed by Wuping Wang	Project Name **Sirius EK V001**	Rev 1.0.0
Date 2017.11.22	Size A4	Page Title P01_COVER
Dept: R&D, ARTOSYN		Sheet [1] of [27]

1

D

C

B

A

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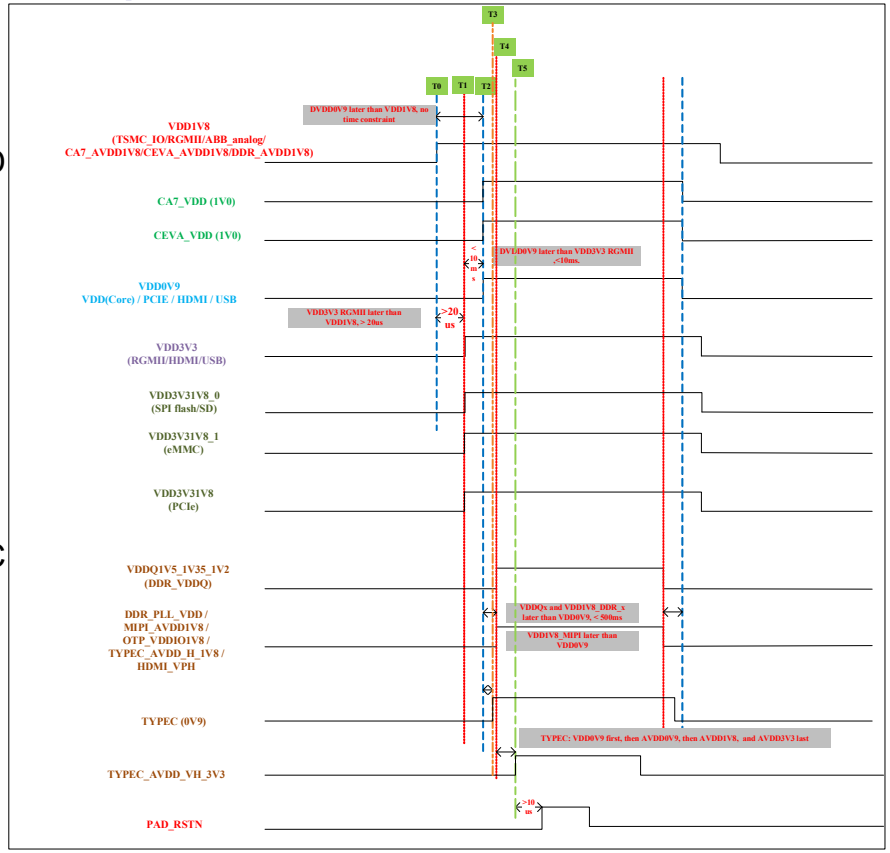
Date 2017.11.22	Size A4	Page Title P02_BLOCK DIAGRAM
Dept: R&D, ARTOSYN		Sheet [2] of [27]

Power Sequence



Power Tree

artosyn	ARTOSYN CONFIDENTIAL	
Designed by Wuping Wang	Project Name Sirius EK V001	Rev 1.0.0
Date 2017.11.22	Size C	Page Title P03_POWER TREE
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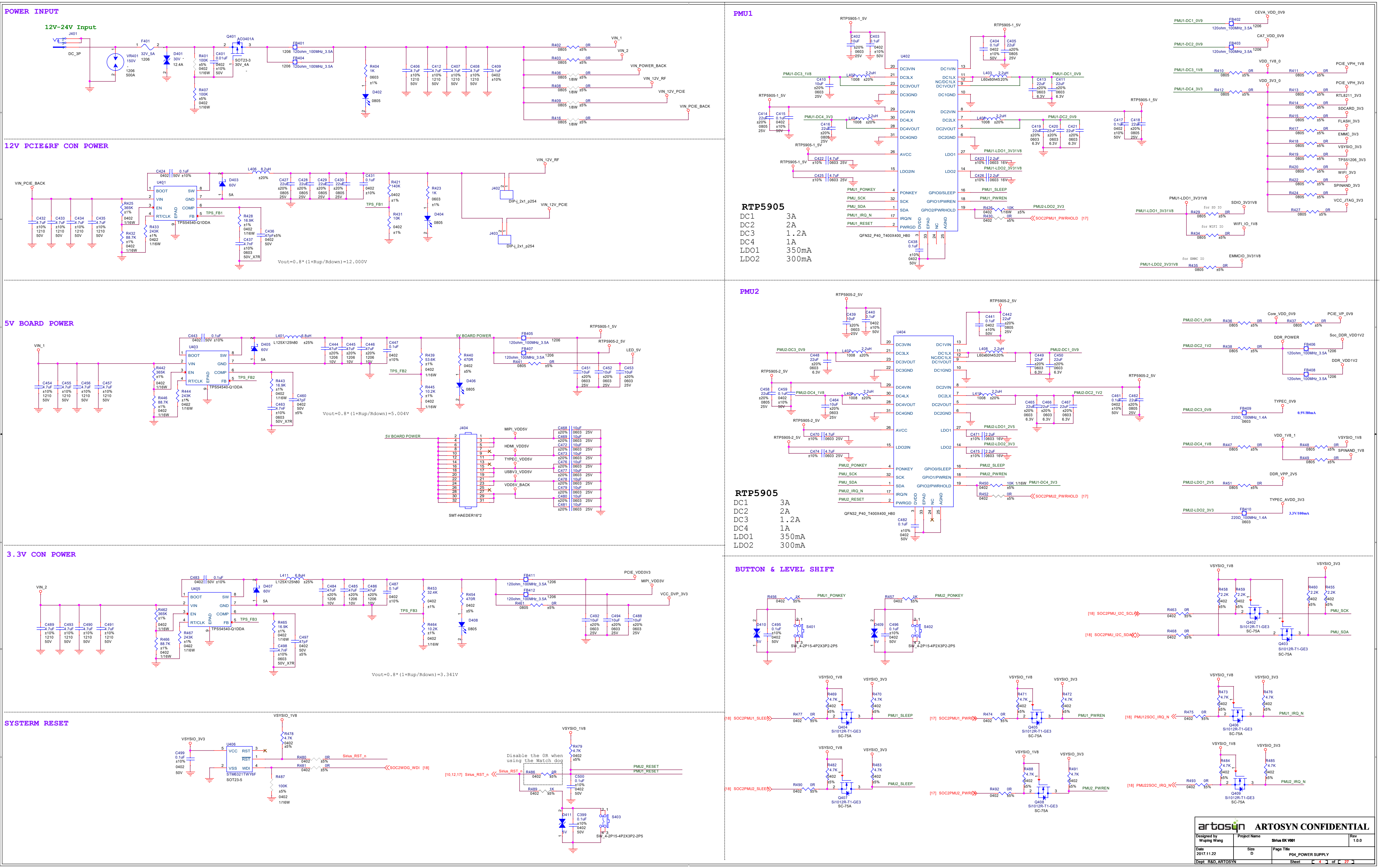

POWER INPUT
12V-24V Input
12V PCIE&RF CON POWER
Vout=0.8*(1+Rup/Rdown)=12.000V
5V BOARD POWER
Vout=0.8*(1+Rup/Rdown)=5.004V
3.3V CON POWER
Vout=0.8*(1+Rup/Rdown)=3.341V
SYSTERM RESET
Disable the 0R when using the Watch dog
PMU1
RTP5905
DC1 3A
DC2 2A
DC3 1.2A
DC4 1A
LDO1 350mA
LDO2 300mA
PMU2
RTP5905
DC1 3A
DC2 2A
DC3 1.2A
DC4 1A
LDO1 350mA
LDO2 300mA
BUTTON & LEVEL SHIFT
artosyn ARTOSYN CONFIDENTIAL
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Project Name Sirius EK V001
Rev 1.0.0
Date 2017.11.22
Size D
Page Title P04_POWER SUPPLY
Dept R&D_ARTOSYN
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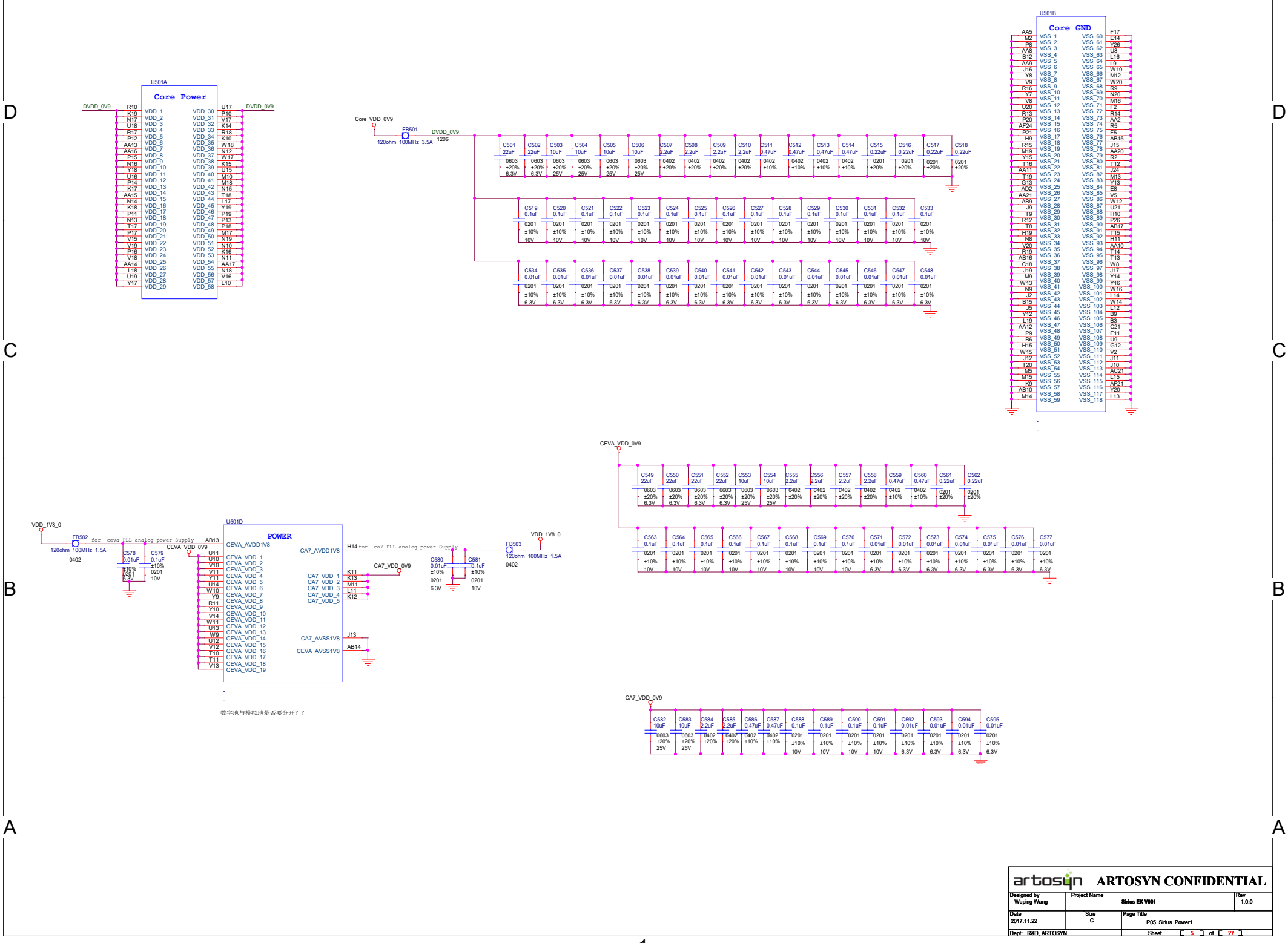

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Designed by Wuping Wang	Project Name Sirius EK V001	Rev 1.0.0
Date 2017.11.22	Size C	Page Title P05_Sirius_Power1
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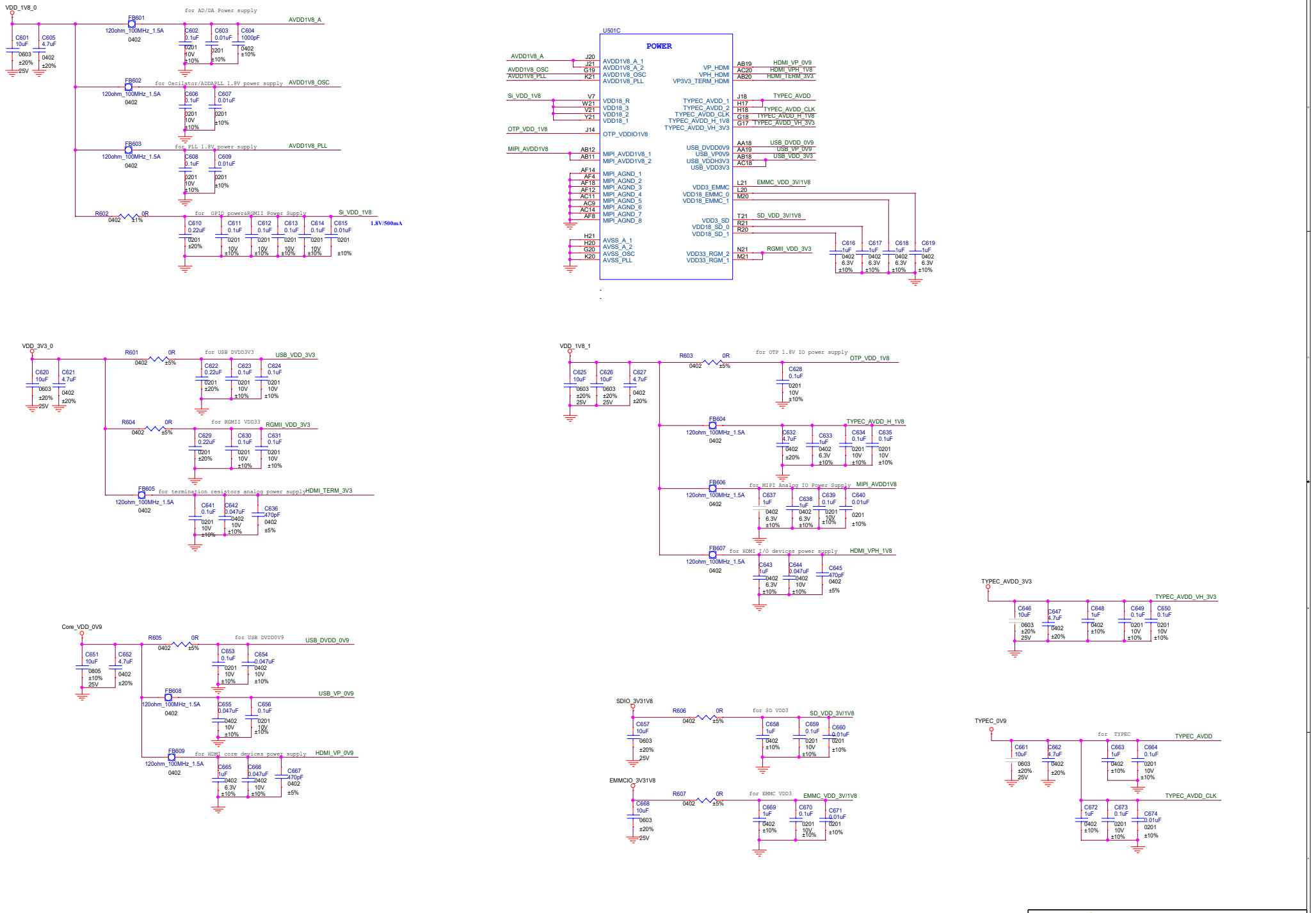

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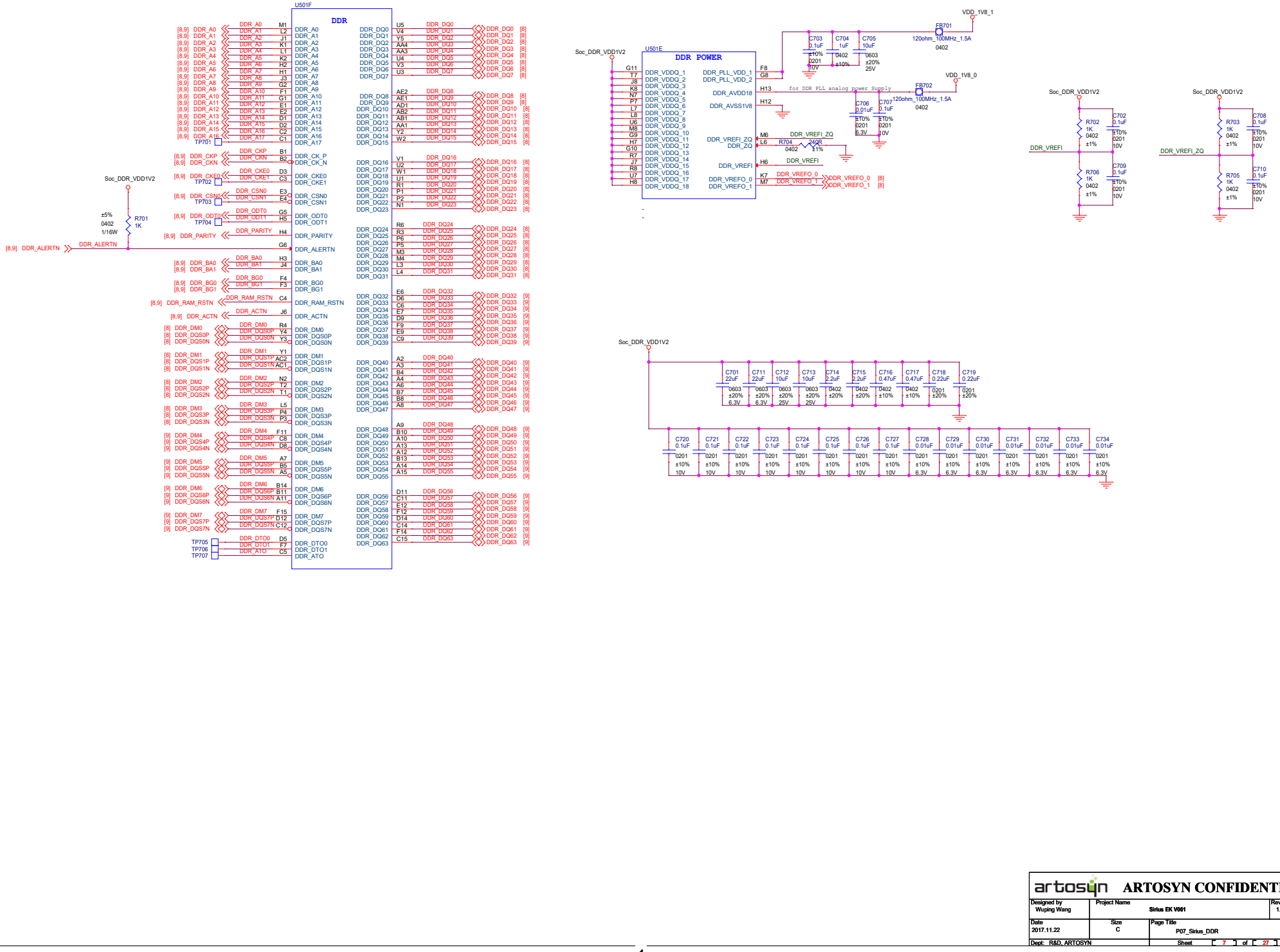
Date: 2017.11.22	Size: C	Page Title: P06_Sirius_Power2
Dept: R&D, ARTOSYN		Sheet 6 of 27



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Designed by Wuping Wang	Project Name Sirius EK V001	Rev 1.0.0
Date 2017.11.22	Size C	Page Title P07_Sirius_DDR
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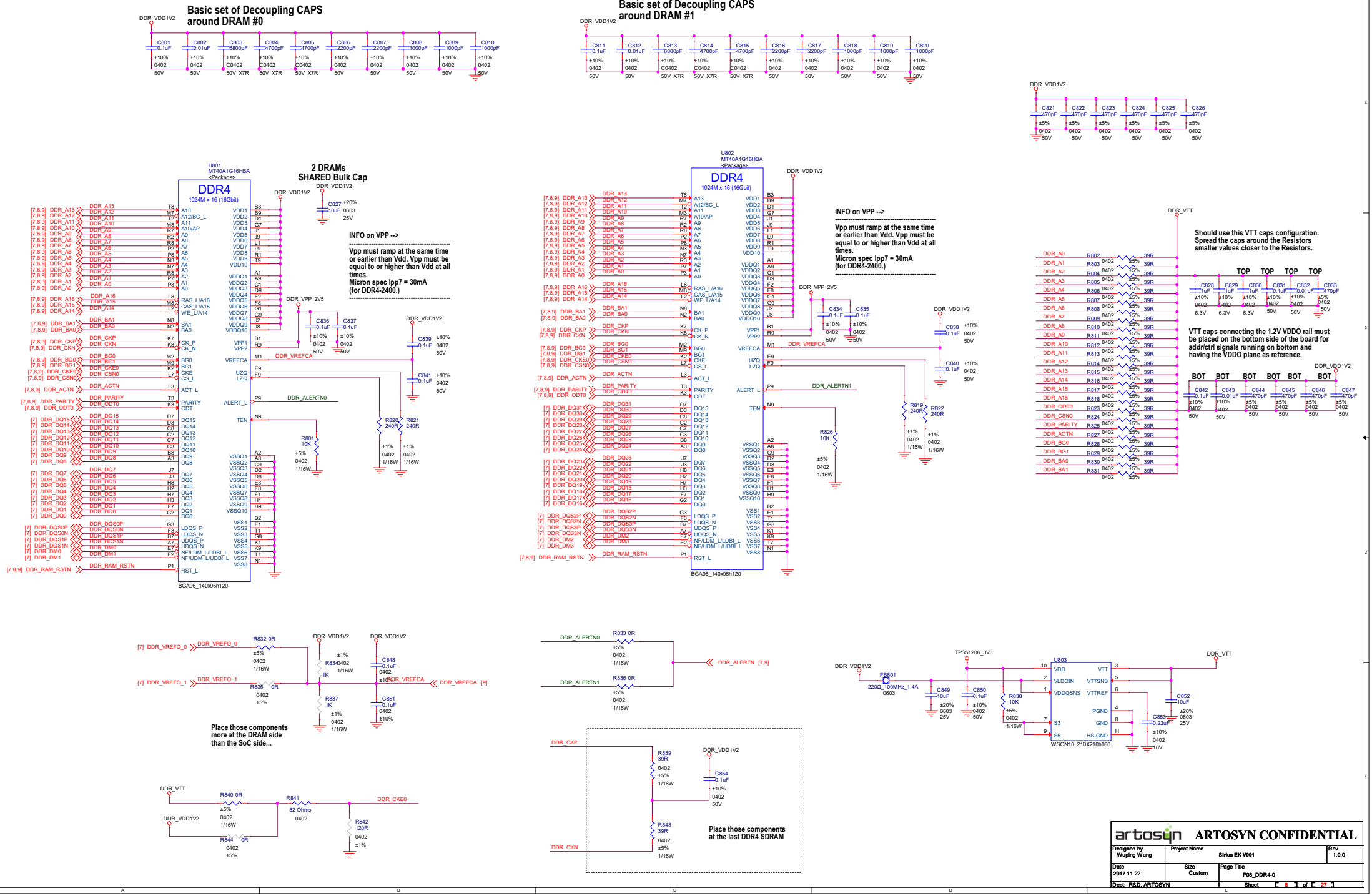
Basic set of Decoupling CAPS around DRAM #0
DDR_VDD1V2
C801 0.1uF ±10% 0402 50V
C802 0.01uF ±10% 0402 50V
C803 6800pF ±10% C0402 50V_X7R
C804 4700pF ±10% C0402 50V_X7R
C805 4700pF ±10% C0402 50V_X7R
C806 2200pF ±10% 0402 50V
C807 2200pF ±10% 0402 50V
C808 1000pF ±10% 0402 50V
C809 1000pF ±10% 0402 50V
C810 1000pF ±10% 0402 50V
Basic set of Decoupling CAPS around DRAM #1
DDR_VDD1V2
C811 0.1uF ±10% 0402 50V
C812 0.01uF ±10% 0402 50V
C813 6800pF ±10% C0402 50V_X7R
C814 4700pF ±10% C0402 50V_X7R
C815 4700pF ±10% C0402 50V_X7R
C816 2200pF ±10% 0402 50V
C817 2200pF ±10% 0402 50V
C818 1000pF ±10% 0402 50V
C819 1000pF ±10% 0402 50V
C820 1000pF ±10% 0402 50V
DDR_VDD1V2
C821 470pF ±5% 0402 50V
C822 470pF ±5% 0402 50V
C823 470pF ±5% 0402 50V
C824 470pF ±5% 0402 50V
C825 470pF ±5% 0402 50V
C826 470pF ±5% 0402 50V
U801
MT40A1G16HBA
<Package>
DDR4
1024M x 16 (16Gbit)
BGA96_140x95h120
2 DRAMs SHARED Bulk Cap
DDR_VDD1V2
C827 10uF ±20% 0603 25V
INFO on VPP -->
Vpp must ramp at the same time or earlier than Vdd. Vpp must be equal to or higher than Vdd at all times.
Micron spec Ipp7 = 30mA (for DDR4-2400.)
DDR_VPP_2V5
C836 0.1uF ±10% 0402 50V
C837 0.1uF ±10% 0402 50V
C839 0.1uF ±10% 0402 50V
C841 0.1uF ±10% 0402 50V
DDR_VREFCA
DDR_ALERTN0
R820 240R ±1% 0402 1/16W
R821 240R ±1% 0402 1/16W
R801 10K ±5% 0402 1/16W
U802
MT40A1G16HBA
<Package>
DDR4
1024M x 16 (16Gbit)
BGA96_140x95h120
DDR_VDD1V2
INFO on VPP -->
Vpp must ramp at the same time or earlier than Vdd. Vpp must be equal to or higher than Vdd at all times.
Micron spec Ipp7 = 30mA (for DDR4-2400.)
DDR_VPP_2V5
C834 0.1uF ±10% 0402 50V
C835 0.1uF ±10% 0402 50V
C838 0.1uF ±10% 0402 50V
C840 0.1uF ±10% 0402 50V
DDR_VREFCA
DDR_ALERTN1
R819 240R ±1% 0402 1/16W
R822 240R ±1% 0402 1/16W
R826 10K ±5% 0402 1/16W
DDR_VTT
Should use this VTT caps configuration. Spread the caps around the Resistors smaller values closer to the Resistors.
R802 39R ±5% 0402 1/16W
R803 39R ±5% 0402 1/16W
R804 39R ±5% 0402 1/16W
R805 39R ±5% 0402 1/16W
R806 39R ±5% 0402 1/16W
R807 39R ±5% 0402 1/16W
R808 39R ±5% 0402 1/16W
R809 39R ±5% 0402 1/16W
R810 39R ±5% 0402 1/16W
R811 39R ±5% 0402 1/16W
R812 39R ±5% 0402 1/16W
R813 39R ±5% 0402 1/16W
R814 39R ±5% 0402 1/16W
R815 39R ±5% 0402 1/16W
R816 39R ±5% 0402 1/16W
R817 39R ±5% 0402 1/16W
R818 39R ±5% 0402 1/16W
R823 39R ±5% 0402 1/16W
R824 39R ±5% 0402 1/16W
R825 39R ±5% 0402 1/16W
R827 39R ±5% 0402 1/16W
R828 39R ±5% 0402 1/16W
R829 39R ±5% 0402 1/16W
R830 39R ±5% 0402 1/16W
R831 39R ±5% 0402 1/16W
TOP
C828 1uF ±10% 0402 6.3V
C829 1uF ±10% 0402 6.3V
C830 1uF ±10% 0402 6.3V
C831 0.1uF ±10% 0402 50V
C832 0.01uF ±10% 0402 50V
C833 470pF ±5% 0402 50V
VTT caps connecting the 1.2V VDDO rail must be placed on the bottom side of the board for addr/ctrl signals running on bottom and having the VDDO plane as reference.
DDR_VDD1V2
BOT
C842 0.1uF ±10% 0402 50V
C843 0.01uF ±10% 0402 50V
C844 470pF ±5% 0402 50V
C845 470pF ±5% 0402 50V
C846 470pF ±5% 0402 50V
C847 470pF ±5% 0402 50V
DDR_VREFO_0
DDR_VREFO_1
R832 0R ±5% 0402 1/16W
R834 1K ±1% 0402 1/16W
R835 0R ±5% 0402
R837 1K ±1% 0402 1/16W
C848 0.1uF ±10% 0402
C851 0.1uF ±10% 0402
DDR_VREFCA [9]
Place those components more at the DRAM side than the SoC side...
DDR_ALERTN0
DDR_ALERTN1
R833 0R ±5% 0402 1/16W
R836 0R ±5% 0402 1/16W
DDR_ALERTN [7,9]
TPS51206_3V3
DDR_VDD1V2
FB801 220Ω_100MHz_1.4A 0603
C849 10uF ±20% 0603 25V
C850 0.1uF ±10% 0402 50V
R838 10K ±5% 0402 1/16W
U803
VDD
VLDOIN
VDDQSNS
VTT
VTTSNS
VTTREF
PGND
GND
S3
S5
HS-GND
H
WSON10_210X210h080
C852 10uF ±20% 0603 25V
C853 0.22uF ±10% 0402 16V
DDR_VTT
DDR_VDD1V2
R840 0R ±5% 0402 1/16W
R841 82 Ohms 0402
R842 120R 0402 ±1%
R844 0R ±5% 0402
DDR_CKE0
DDR_CKP
DDR_CKN
R839 39R ±5% 0402 1/16W
R843 39R ±5% 0402 1/16W
C854 0.1uF ±10% 0402 50V
Place those components at the last DDR4 SDRAM
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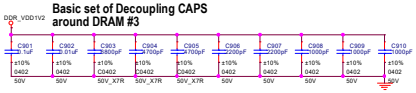
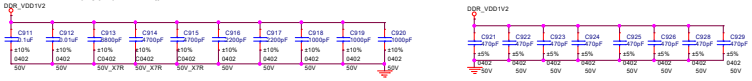
Basic set of Decoupling CAPS around DRAM #3



Basic set of Decoupling CAPS around DRAM #4

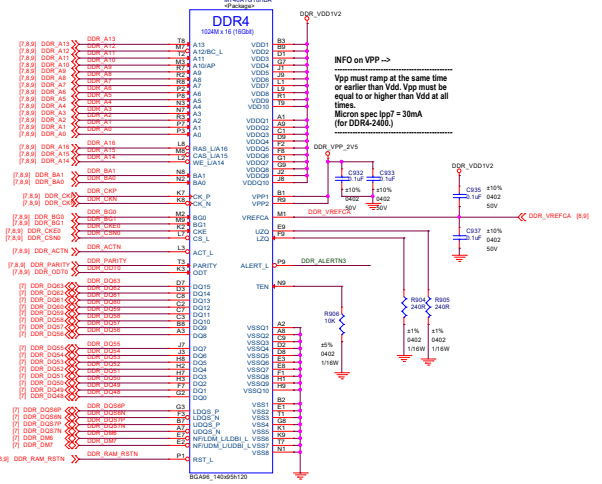


2 DRAMs SHARED Bulk Cap

INFO on VPP -->

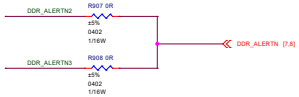
Vpp must ramp at the same time or earlier than Vdd. Vpp must be equal to or higher than Vdd at all times.
Micron spec Ipp7 = 30mA (for DDR4-2400.)

Place test pads on these page as close as possible to the Bcm72520 balls they connected to.



INFO on VPP -->

Vpp must ramp at the same time or earlier than Vdd. Vpp must be equal to or higher than Vdd at all times.
Micron spec Ipp7 = 30mA (for DDR4-2400.)



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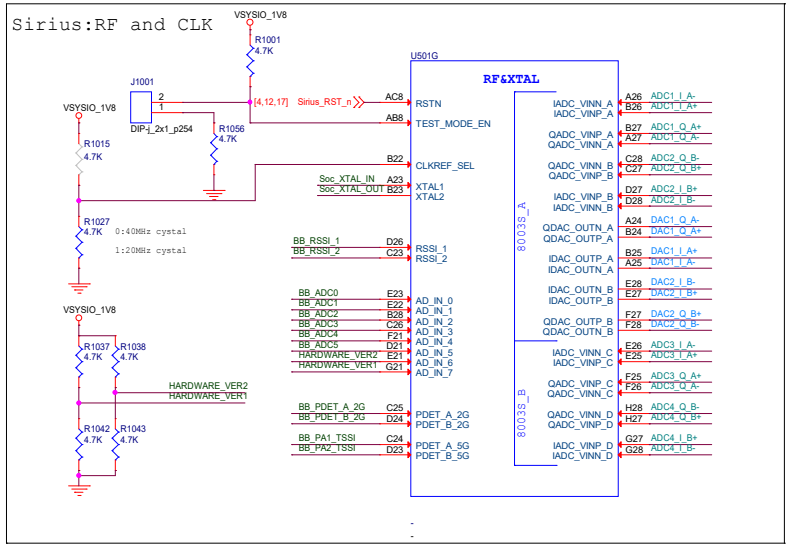
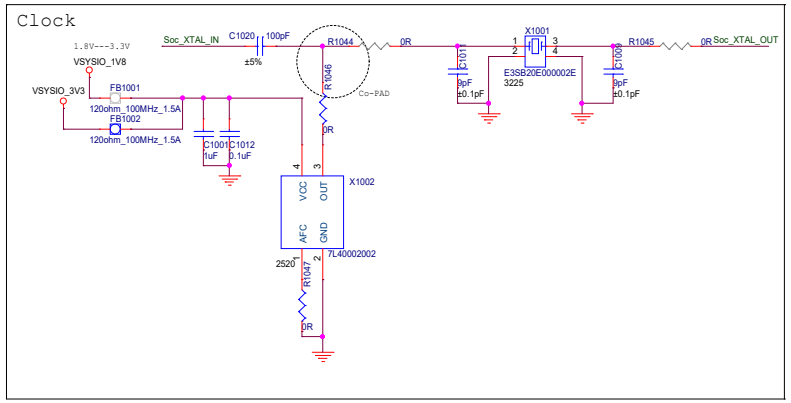
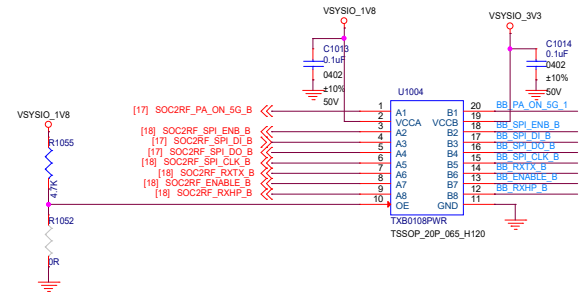
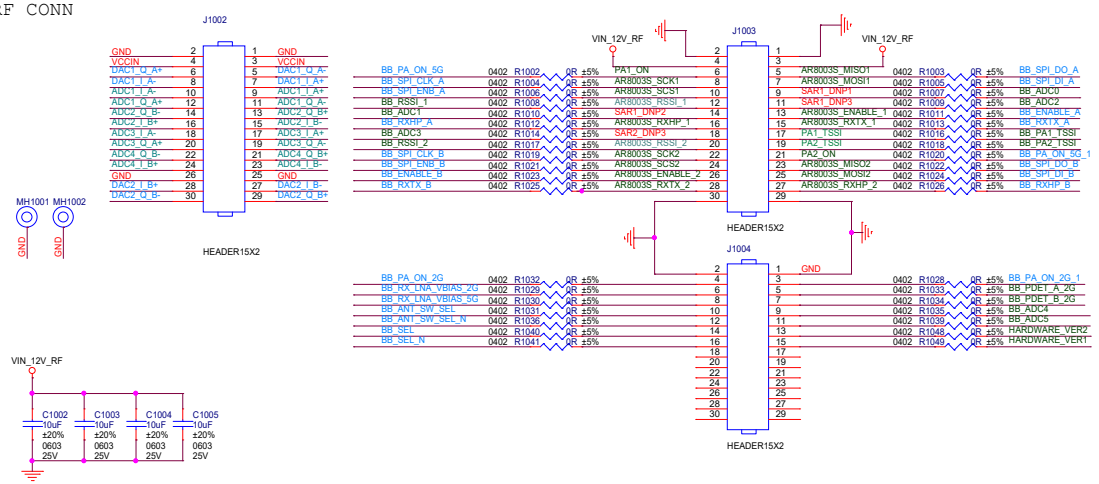
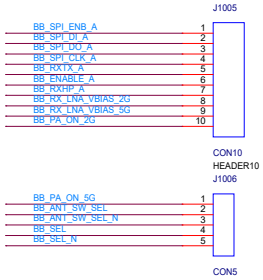


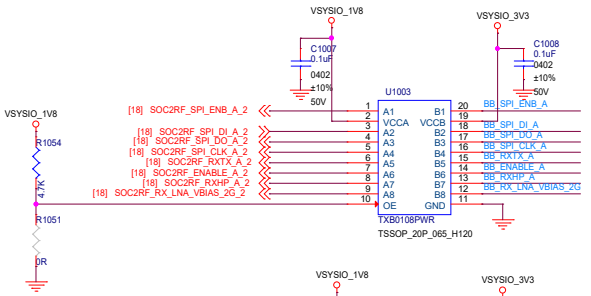


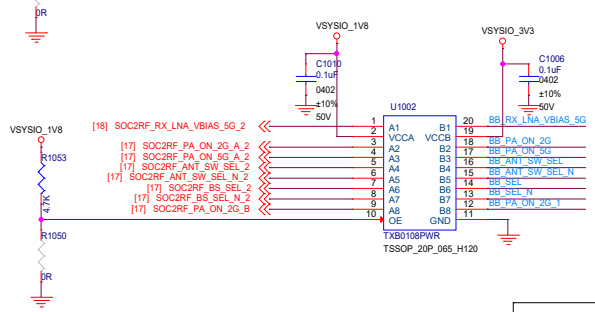




defult function	share fuction
GBE_TXC	BB_SPI_ENB_A
GBE_TXEN	BB_SPI_DI_A
GBE_TXD0	BB_SPI_DO_A
GBE_TXD1	BB_SPI_CLK_A
GBE_TXD2	BB_RXTX_A
GBE_TXD3	BB_ENABLE_A
GBE_RXC	BB_RXHP_A
GBE_RXEN	BB_RX_LNA_VBIAS_2G
GBE_RXD0	BB_RX_LNA_VBIAS_5G
GBE_RXD1	BB_PA_ON_2G
GBE_RXD2	BB_PA_ON_5G
GBE_RXD3	BB_ANT_SW_SEL
GBE_MDC	BB_ANT_SW_SEL_N
GBE_MDIO	BS_SEL
GBE_RST	BS_SEL_N







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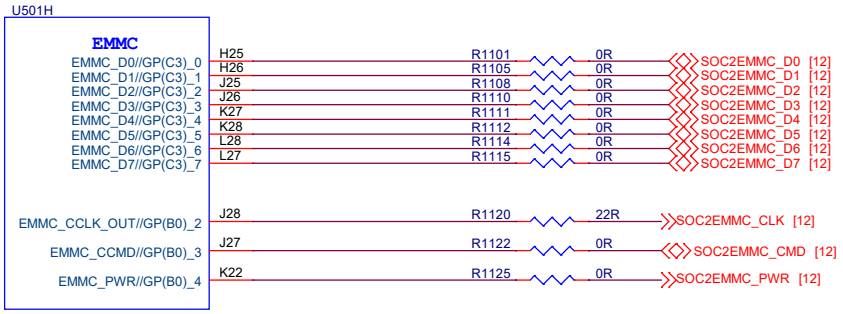
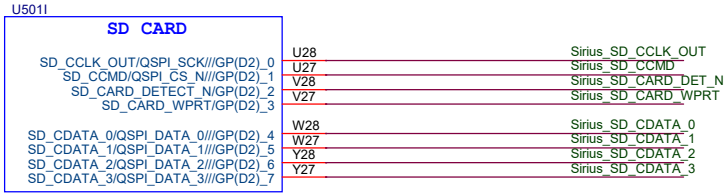
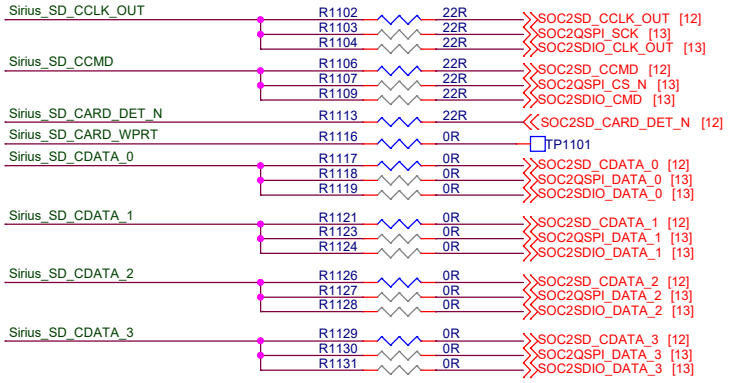
SOC EMMC & SD







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Date 2017.11.22	Size B	Page Title P11_Sirius_Memory
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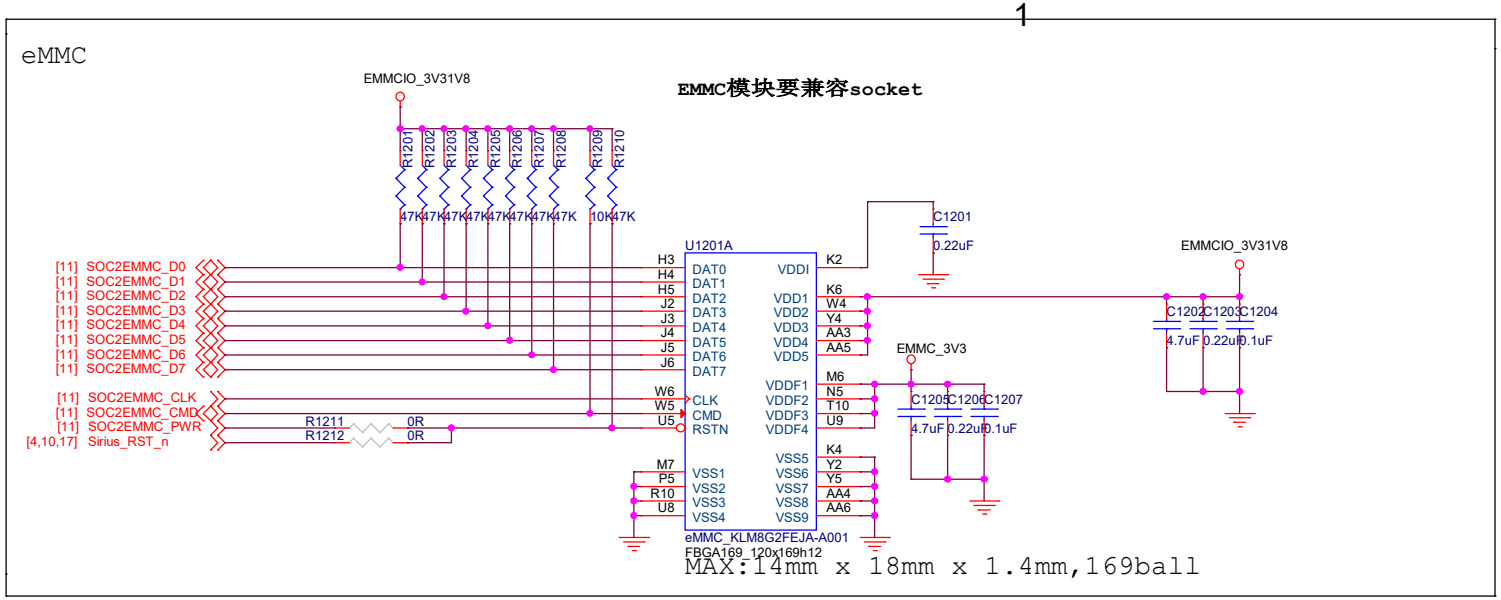

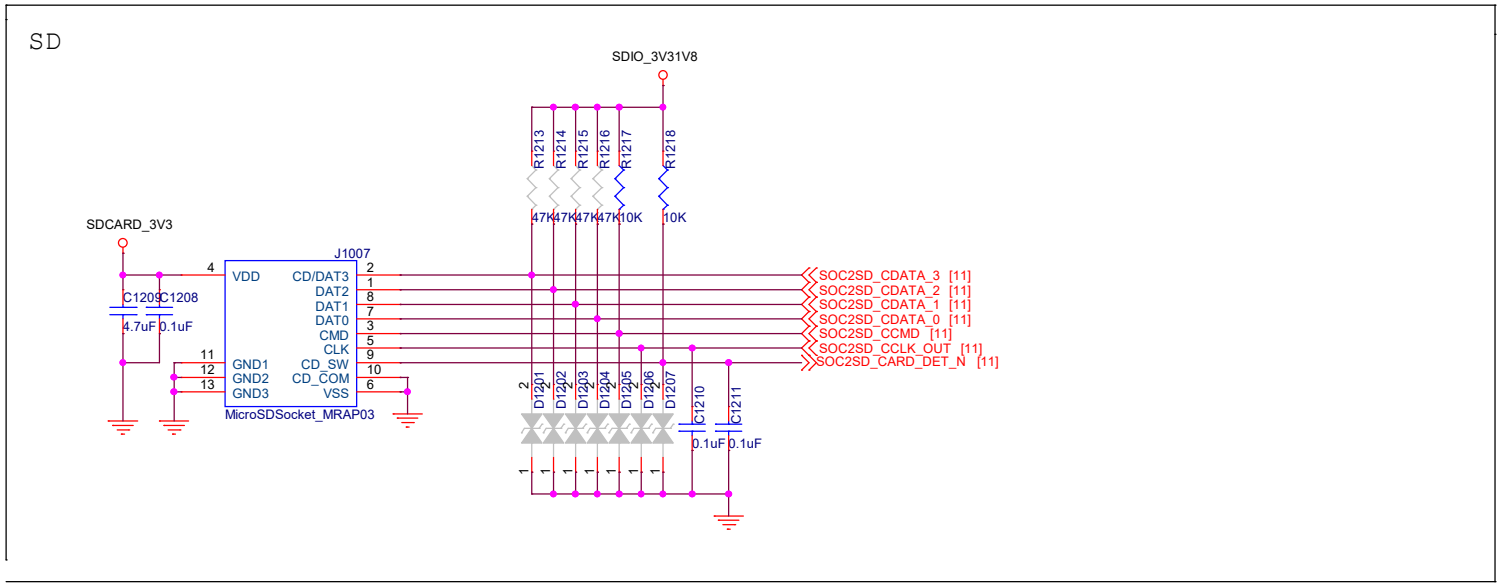

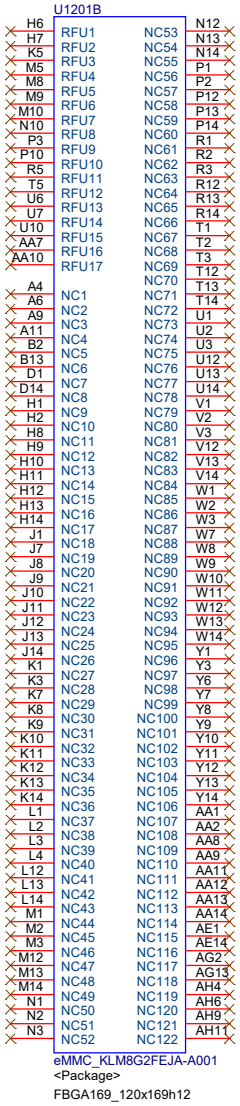

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Designed by Wuping Wang	Project Name Sirius EK V001	Rev 1.0.0
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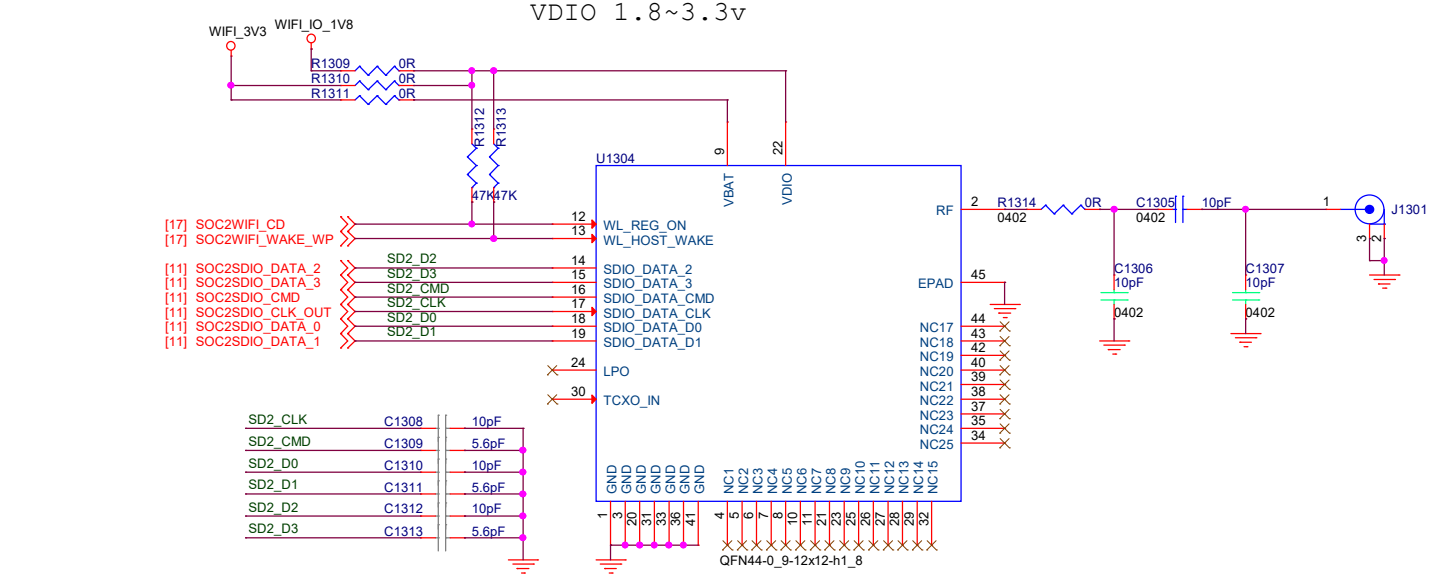
QSPI & SPI Nand flash

SDIO WIFI Module



artosyn ARTOSYN CONFIDENTIAL		
Designed by Wuping Wang	Project Name Sirius EK V001	Rev 1.0.0
Date 2017.11.22	Size B	Page Title P13_FLASH_SDIO
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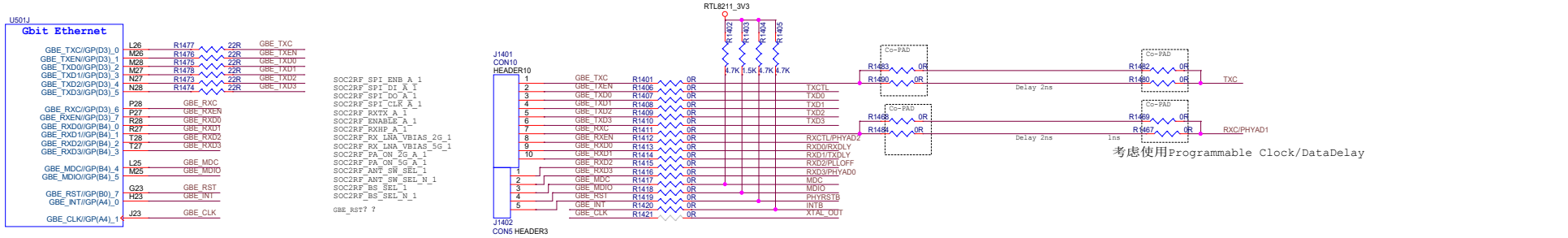
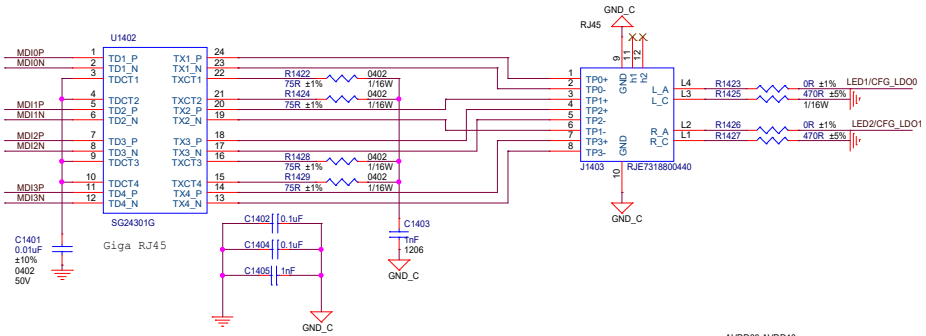
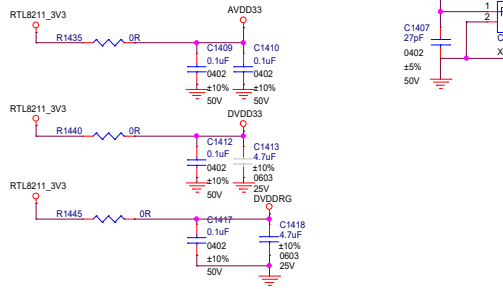


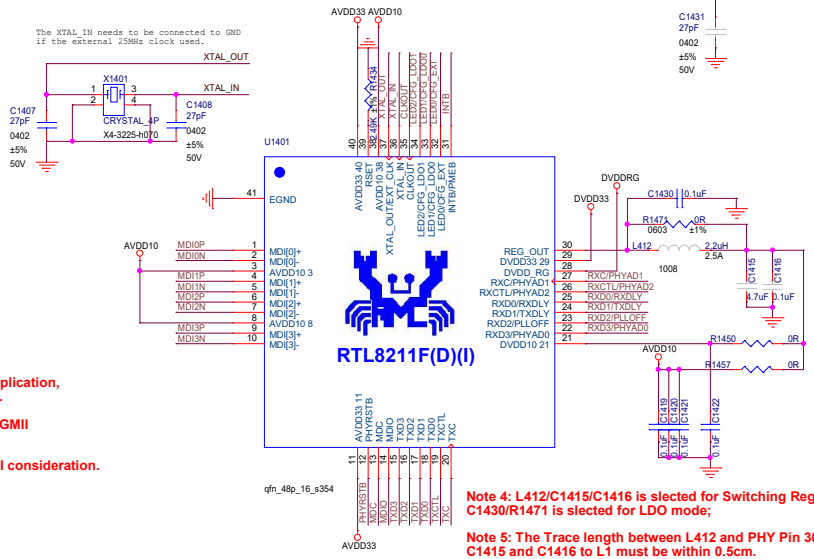
PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

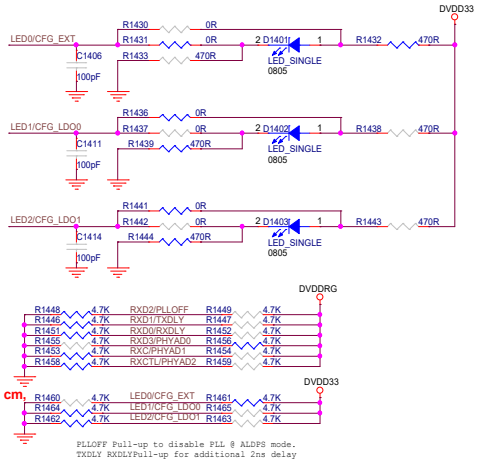
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V (default)	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11

	LED Resistances Setting
CFG_EXT=1'b1	R1430(NC), R1431, R1432, R1433(NC)
CFG_EXT=1'b0	R1430, R1431(NC), R1432(NC), R1433
CFG_LDO0=1'b1	R1434(NC), R1437, R1438, R1439(NC)
CFG_LDO0=1'b0	R1434, R1437(NC), R1438(NC), R1439
CFG_LDO1=1'b1	R1441(NC), R1442, R1443, R1444(NC)
CFG_LDO1=1'b0	R1441, R1442(NC), R1443(NC), R1444









Note 1: R1440/R1445 is not needed for ONLY 3.3V RGMII application, and DVDDRG can be connected directly to DVDD33.

Note 2: DVDDRG must be short to DVDD33 if the external RGMII 3.3V is selected.

Note 3: CAPs(C1417/C1448) must be closed to pin28 for EMI consideration.

Note 4: L412/C1415/C1416 is slected for Switching Regulator mode; C1430/R1471 is slected for LDO mode;

Note 5: The Trace length between L412 and PHY Pin 30 must be within 0.5 cm. C1415 and C1416 to L1 must be within 0.5cm.

Note 6: Any inductance or bead except L1 is not allowed on the path from REGOUT to DVDD10/AVDD10.

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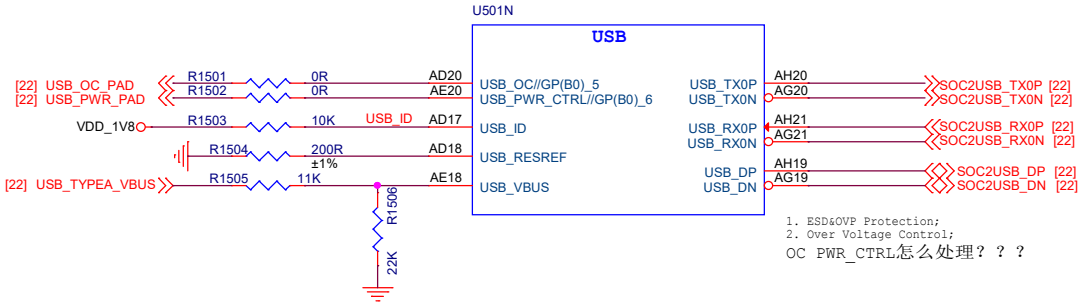
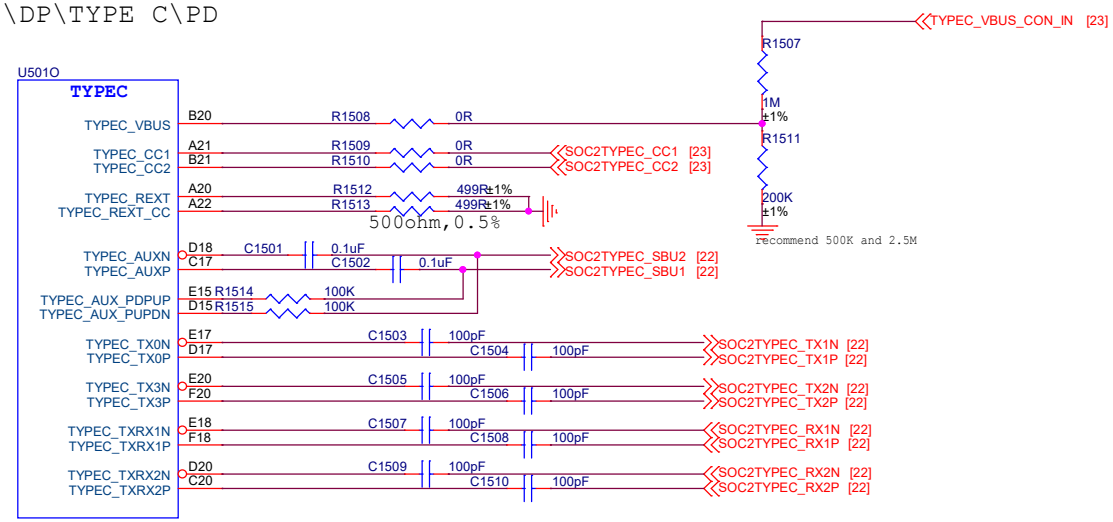
SOC:USB3.0 AND USB2.0



SOC:USB3.0\DP\TYPE C\PD



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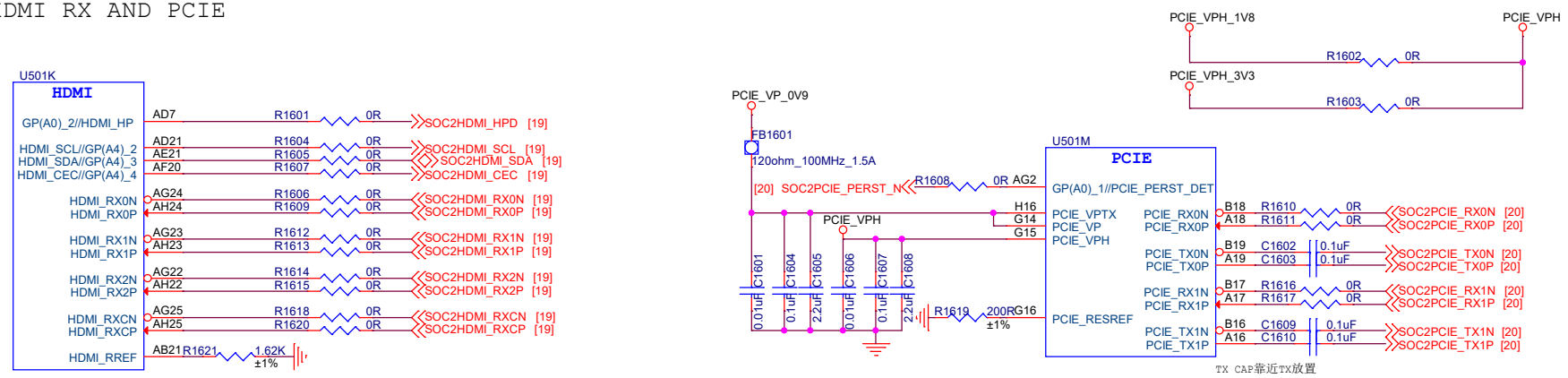
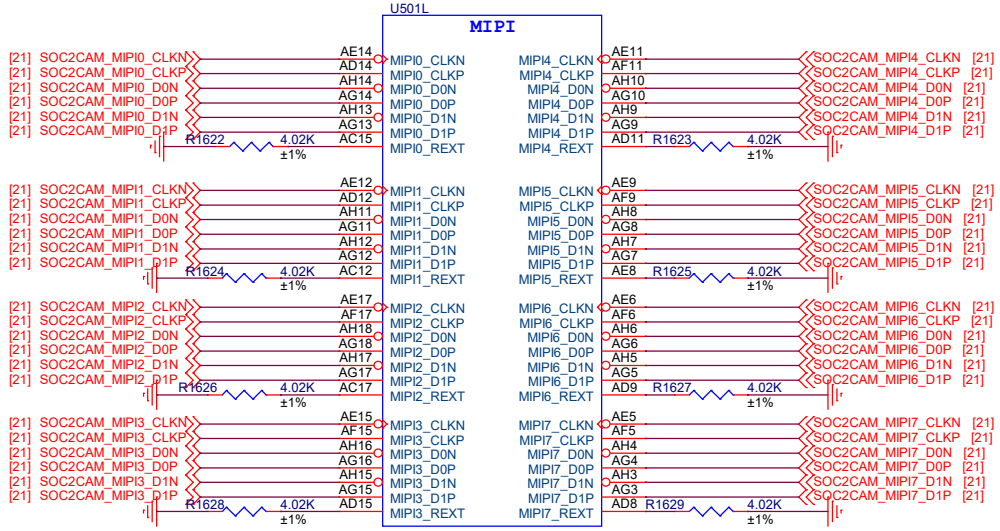
SOC:HDMI RX AND PCIE



SOC:MIPI CSI RX*8 AND TX*2



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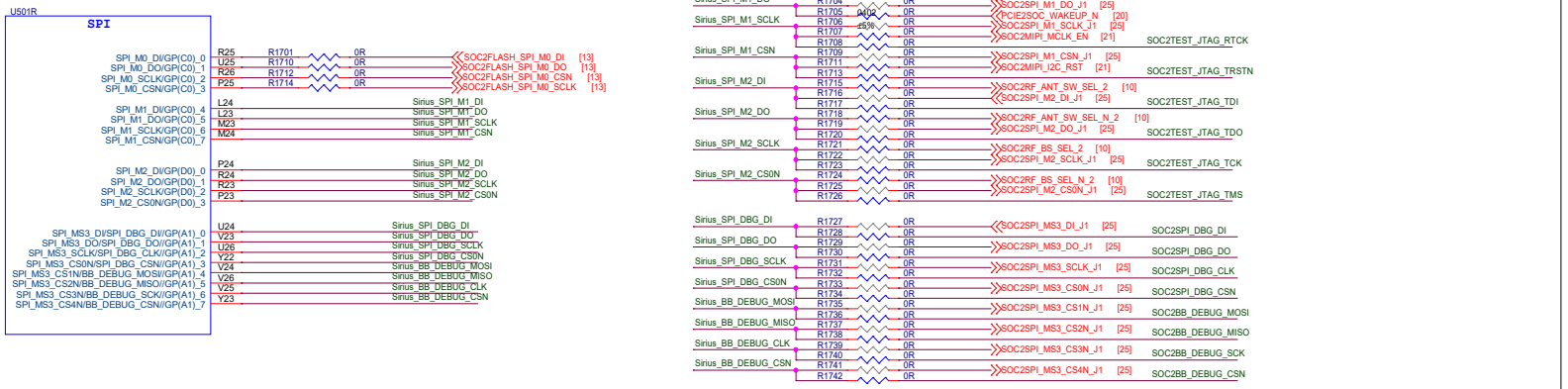
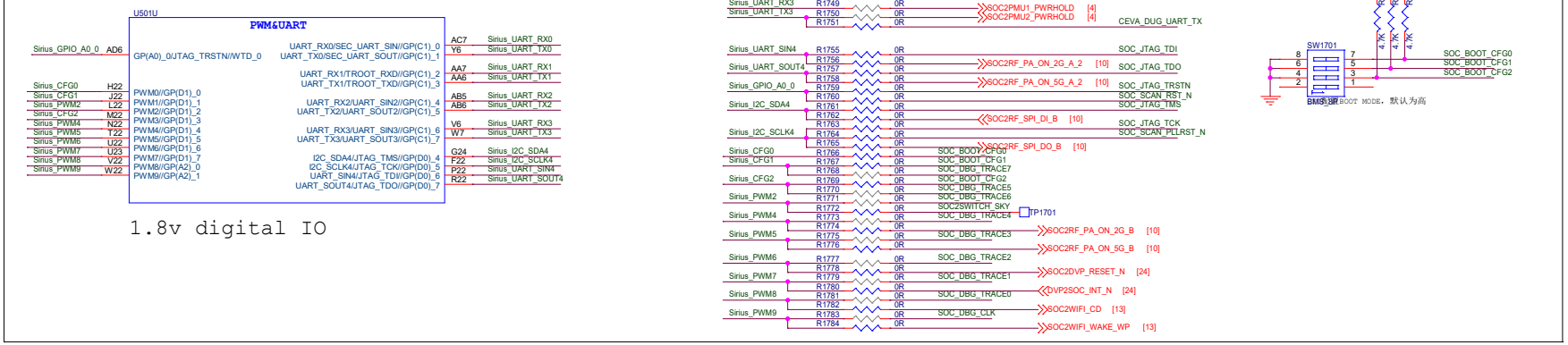
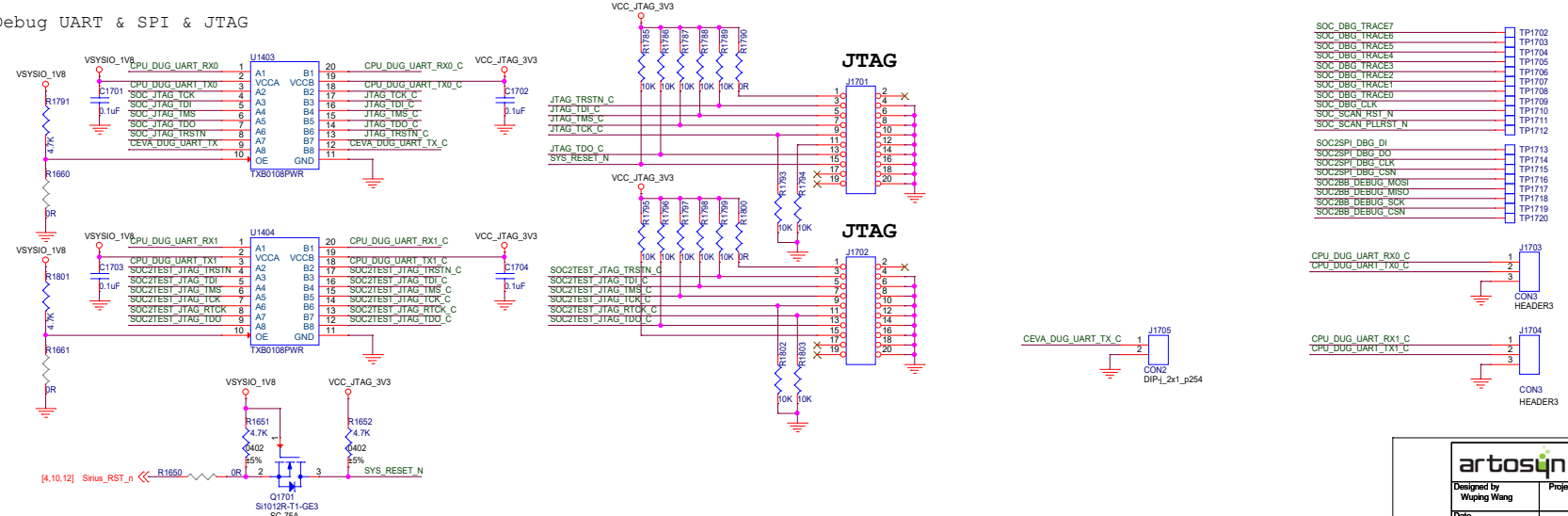
SOC SPI



UART&CFG



Debug UART & SPI & JTAG



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Sirius DVP

U501P

DVP

PCLK0/(GP(A2)_6	AD26	Sirius_PCLK0
DE0/(GP(A2)_7	AD25	Sirius_DE0
VSYNC0/(GP(B0)_0	AF26	Sirius_VSYNC0
HSYNC0/(GP(B0)_1	AE26	Sirius_HSYNC0
QE0_0/(GP(B3)_0	AG26	Sirius_QE0_0
QE0_1/(GP(B3)_1	AF25	Sirius_QE0_1
QE0_2/(GP(B3)_2	AD23	Sirius_QE0_2
QE0_3/(GP(B3)_3	AE24	Sirius_QE0_3
QE0_4/(GP(B3)_4	AC22	Sirius_QE0_4
QE0_5/(GP(B3)_5	AE23	Sirius_QE0_5
QE0_6/(GP(B3)_6	AF23	Sirius_QE0_6
QE0_7/(GP(B3)_7	AD22	Sirius_QE0_7
PCLK1/(GP(A2)_2	AC28	Sirius_PCLK1
DE1/(GP(A2)_3	AD28	Sirius_DE1
VSYNC1/(GP(A2)_4	AC27	Sirius_VSYNC1
HSYNC1/(GP(A2)_5	AE28	Sirius_HSYNC1
QE1_0/(GP(A3)_0	AF28	Sirius_QE1_0
QE1_1/(GP(A3)_1	AD27	Sirius_QE1_1
QE1_2/(GP(A3)_2	AG28	Sirius_QE1_2
QE1_3/(GP(A3)_3	AE27	Sirius_QE1_3
QE1_4/(GP(A3)_4	AH26	Sirius_QE1_4
QE1_5/(GP(A3)_5	AF27	Sirius_QE1_5
QE1_6/(GP(A3)_6	AG27	Sirius_QE1_6
QE1_7/(GP(A3)_7	AH27	Sirius_QE1_7

Sirius_PCLK1	R1805	0R	SOC2DVP_PCLK1	[24]
	R1806	0R	SOC2TYPEC_VBUS_SOURCE_EN	[23]
Sirius_DE1	R1811	0R	SOC2DVP_DE1	[24]
	R1812	0R	SOC2TYPEC_VBUS_SINK_EN	[23]
Sirius_VSYNC1	R1814	0R	SOC2DVP_VSYNC1	[24]
	R1815	0R	SOC2TYPEC_VBUS_BDIS_EN	[23]
Sirius_HSYNC1	R1819	0R	SOC2DVP_HSYNC1	[24]
	R1820	0R	SOC2TYPEC_VBUS_FDIS_EN	[23]
Sirius_QE1_0	R1823	0R	SOC2DVP_QE1_0	[24]
	R1825	0R	SOC2TYPEC_VCONN2CC1	[23]
Sirius_QE1_1	R1827	0R	SOC2DVP_QE1_1	[24]
	R1828	0R	SOC2TYPEC_VCONN2CC2	[23]
Sirius_QE1_2	R1829	0R	SOC2DVP_QE1_2	[24]
	R1830	0R	SOC2TYPEC_VBUS_OC_IN	[23]
	R1898	0R	SOC2TYPEC_GPIO_PG	[23]
Sirius_QE1_3	R1831	0R	SOC2DVP_QE1_3	[24]
	R1832	0R	SOC2TYPEC_CC1_OC_IN	[23]
	R1899	0R	SOC2TYPEC_GPIO_DEADBAT	[23]
Sirius_QE1_4	R1833	0R	SOC2DVP_QE1_4	[24]
	R1834	0R	SOC2TYPEC_CC2_OC_IN	[23]
Sirius_QE1_5	R1835	0R	SOC2DVP_QE1_5	[24]
	R1836	0R	SOC2TYPEC_DEAD_BAT_IN	[23]
Sirius_QE1_6	R1837	0R	SOC2DVP_QE1_6	[24]
	R1838	0R	SOC2TYPEC_VBUS_OC_EN	[23]
Sirius_QE1_7	R1839	0R	SOC2DVP_QE1_7	[24]
	R1840	0R	SOC2TYPEC_VCONN_OC_EN	[23]

Sirius_PCLK0	R1807	0R	SOC2DVP_PCLK0	[24]
Sirius_DE0	R1808	0R	SOC2DVP_DE0	[24]
Sirius_VSYNC0	R1809	0R	SOC2DVP_VSYNC0	[24]
Sirius_HSYNC0	R1810	0R	SOC2DVP_HSYNC0	[24]
Sirius_QE0_0	R1813	0R	SOC2DVP_QE0_0	[24]
Sirius_QE0_1	R1816	0R	SOC2DVP_QE0_1	[24]
Sirius_QE0_2	R1817	0R	SOC2DVP_QE0_2	[24]
Sirius_QE0_3	R1818	0R	SOC2DVP_QE0_3	[24]
Sirius_QE0_4	R1821	0R	SOC2DVP_QE0_4	[24]
Sirius_QE0_5	R1822	0R	SOC2DVP_QE0_5	[24]
Sirius_QE0_6	R1824	0R	SOC2DVP_QE0_6	[24]
Sirius_QE0_7	R1826	0R	SOC2DVP_QE0_7	[24]

DVP 0和MON OUT复用接口
DVP 1和MON OUT复用接口
DVP 0和TYPE C 兼容设计

Sirius I2S&GPIO

U501Q

I2S

I2S_WS_0/GP(B2)_0	AA27	Sirius_I2S_WS0
I2S_SDI_0/GP(B2)_1	AA26	Sirius_I2S_SDI0
I2S_SDO_0/GP(B2)_2	AB28	Sirius_I2S_SDO0
I2S_CLK_0/GP(B2)_3	AA28	Sirius_I2S_CLK0
I2S_WS_1/GP(B2)_4	AA25	Sirius_I2S_WS1
I2S_SDI_1/GP(B2)_5	Y25	Sirius_I2S_SDI1
I2S_SDO_1/GP(B2)_6	AB27	Sirius_I2S_SDO1
I2S_CLK_1/GP(B2)_7	AC26	Sirius_I2S_CLK1
I2S_WS_2/GP(C2)_0	Y24	Sirius_I2S_WS2
I2S_SDI_2/GP(C2)_1	AA23	Sirius_I2S_SDI2
I2S_SDO_2/GP(C2)_2	AA24	Sirius_I2S_SDO2
I2S_CLK_2/GP(C2)_3	AA22	Sirius_I2S_CLK2
I2S_WS_3/GP(C2)_4	AB23	Sirius_I2S_WS3
I2S_SDI_3/GP(C2)_5	AB24	Sirius_I2S_SDI3
I2S_SDO_3/GP(C2)_6	AC24	Sirius_I2S_SDO3
I2S_CLK_3/GP(C2)_7	AC25	Sirius_I2S_CLK3

1.8v digital IO

Sirius_I2S_WS0	R1841	0R	SOC2PMU1_SLEEP	[4]
Sirius_I2S_SDI0	R1842	0R	SOC2PMU2_SLEEP	[4]
Sirius_I2S_SDO0	R1843	0R	PMU12SOC_IRQ_N	[4]
Sirius_I2S_CLK0	R1844	0R	PMU22SOC_IRQ_N	[4]
Sirius_I2S_WS1	R1845	0R	SOC2DVP_I2S_WS1	[24]
Sirius_I2S_SDI1	R1846	0R	SOC2DVP_I2S_SDI1	[24]
Sirius_I2S_SDO1	R1847	0R	SOC2DVP_I2S_SDO1	[24]
Sirius_I2S_CLK1	R1849	0R	SOC2DVP_I2S_CLK1	[24]
Sirius_I2S_WS2	R1853	0R	SOC2RF_RXTX_A_2	[10]
	R1855	0R	SOC2I2S_WS_2_MON	[24]
Sirius_I2S_SDI2	R1856	0R	SOC2RF_ENABLE_A_2	[10]
	R1857	0R	SOC2I2S_SDI_2_MON	[24]
Sirius_I2S_SDO2	R1858	0R	SOC2RF_RXHP_A_2	[10]
	R1859	0R	SOC2I2S_SDO_2_MON	[24]
Sirius_I2S_CLK2	R1860	0R	SOC2RF_RX_LNA_VBIAS_2G_2	[10]
	R1861	0R	SOC2I2S_CLK_2_MON	[24]
Sirius_I2S_WS3	R1862	0R	SOC2RF_RXTX_B	[10]
	R1863	0R	SOC2DVP_EXT_OUT_0	[24]
Sirius_I2S_SDI3	R1864	0R	SOC2RF_ENABLE_B	[10]
	R1865	0R	SOC2DVP_EXT_OUT_1	[24]
Sirius_I2S_SDO3	R1866	0R	SOC2RF_RXHP_B	[10]
	R1867	0R	SOC2DVP_EXT_OUT_2	[24]
Sirius_I2S_CLK3	R1868	0R	SOC2RF_RX_LNA_VBIAS_5G_2	[10]
	R1869	0R	SOC2DVP_EXT_OUT_3	[24]

GPIO

U501T

GP(A0)_3//UART_SIN5	AH2	R1848	0R	SOC2WDG_WDI [4]
GP(A0)_4//UART_SOUT5	AF2	R1850	0R	SOC2RF_SPI_DO_A_2 [10]
GP(A0)_5//WTD_1	AF1	R1851	0R	SOC2RF_SPI_ENB_A_2 [10]
GP(A0)_6/UART_SIN1	AG1	R1852	0R	SOC2RF_SPI_DI_A_2 [10]
GP(A0)_7//UART_SOUT1	AF3	R1854	0R	SOC2RF_SPI_CLK_A_2 [10]

1.8v digital IO

Sirius I2C

VSYSIO_1V8

U501S

I2C

I2C_SDA0/GP(B1)_0	AE3	SOC2PMU_I2C_SDA0 [4]
I2C_SCLK0/GP(B1)_1	AD3	SOC2PMU_I2C_SCLK0 [4]
I2C_SDA1/GP(B1)_2	AD4	SOC2SMB_I2C_SDA [20]
I2C_SCLK1/GP(B1)_3	AC4	SOC2SMB_I2C_SCLK [20]
I2C_SDA2/GP(B1)_4	AC5	SOC2MIPI_I2C_SDA1 [21]
I2C_SCLK2/GP(B1)_5	AC3	SOC2MIPI_I2C_SCLK1 [21]
I2C_SDA3/GP(B1)_6	F24	SOC2DVP_I2C_SDA [24]
I2C_SCLK3/GP(B1)_7	H24	SOC2DVP_I2C_SCLK [24]

1.8v digital IO

R1870	2.2K		
R1871	2.2K		
R1872	2.2K		
R1873	2.2K		
R1874	2.2K		
R1875	2.2K		
R1876	0R	SOC2PMU_I2C_SDA0	[4]
R1877	0R	SOC2PMU_I2C_SCLK0	[4]
R1878	0R	SOC2SMB_I2C_SDA	[20]
R1880	0R	SOC2SMB_I2C_SCLK	[20]
R1879	0R	SOC2SMB_I2C_SDA	[20]
R1881	0R	SOC2SMB_I2C_SCLK	[20]
R1882	0R	SOC2MIPI_I2C_SDA1	[21]
R1883	0R	SOC2MIPI_I2C_SCLK1	[21]
R1884	0R	SOC2DVP_I2C_SDA	[24]
R1886	0R	SOC2DVP_I2C_SCLK	[24]
R1885	0R	SOC2DVP_I2C_SDA	[24]
R1887	0R	SOC2DVP_I2C_SCLK	[24]
R1888	0R	SOC2MIPI_I2C_SDA2	[21]
R1889	0R	SOC2MIPI_I2C_SCLK2	[21]
R1890	0R	SOC2RF_SPI_ENB_B	[10]
R1891	0R	SOC2RF_SPI_CLK_B	[10]

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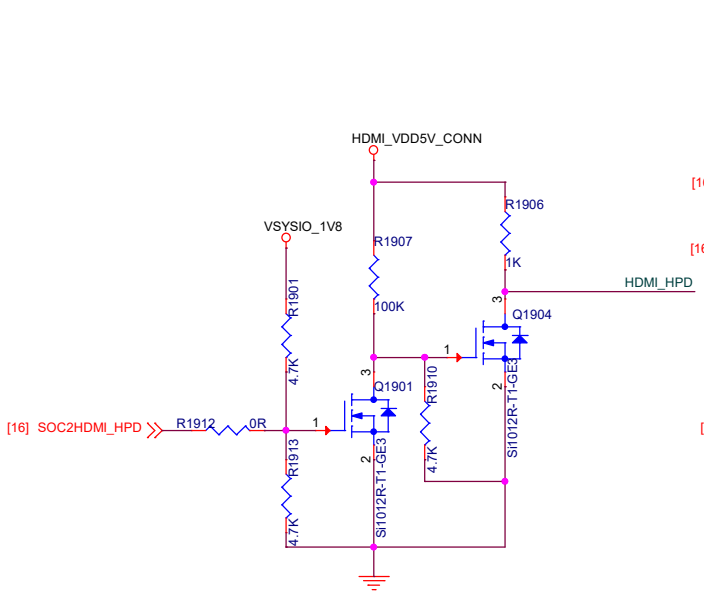
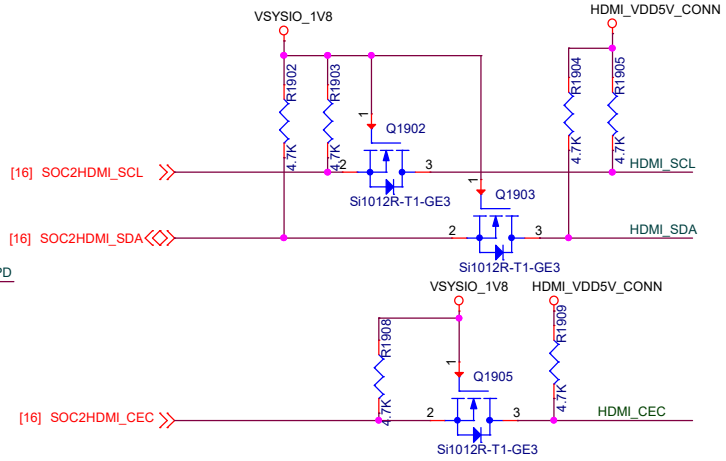
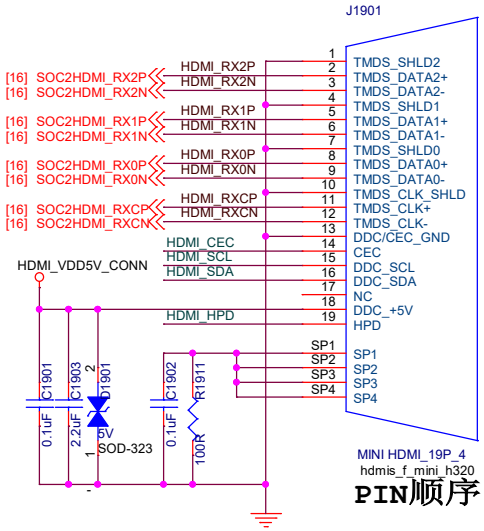
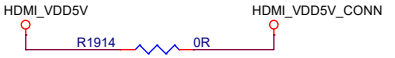


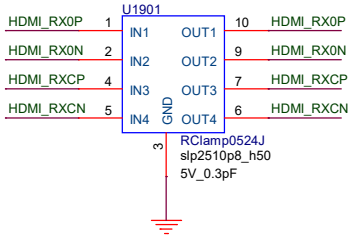


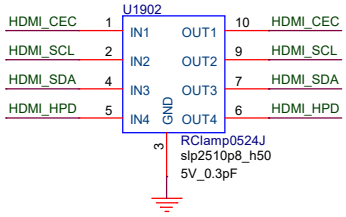


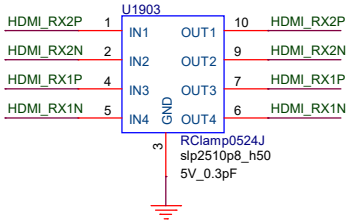
PIN顺序！ 需要确认！



Sourse supply 5V power







artosyn **ARTOSYN CONFIDENTIAL**

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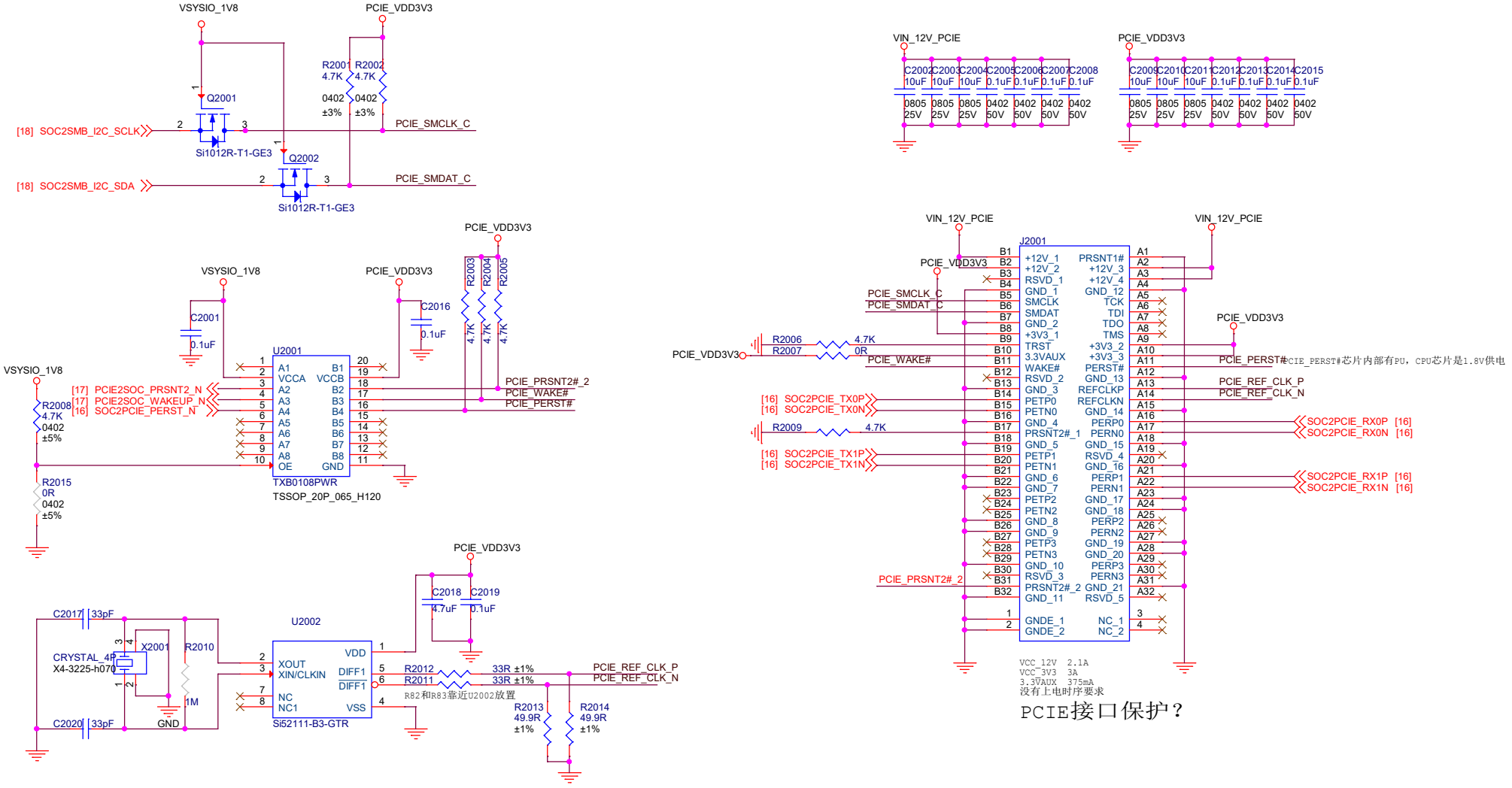

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Page Title: P20_CONN_PCIE	
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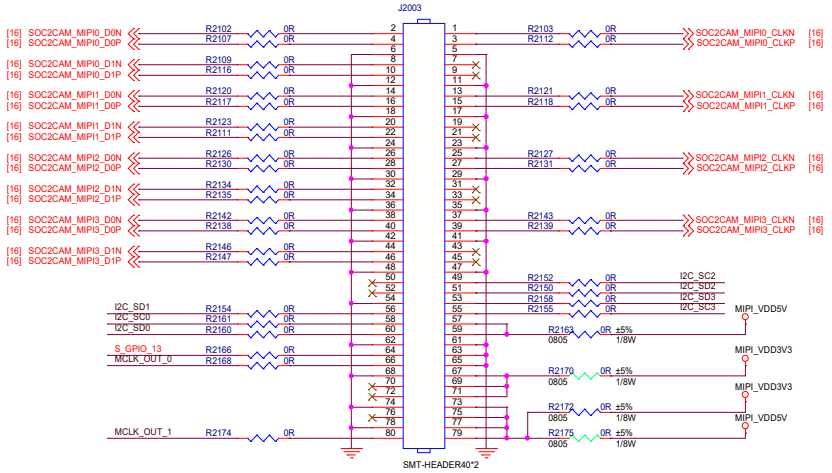
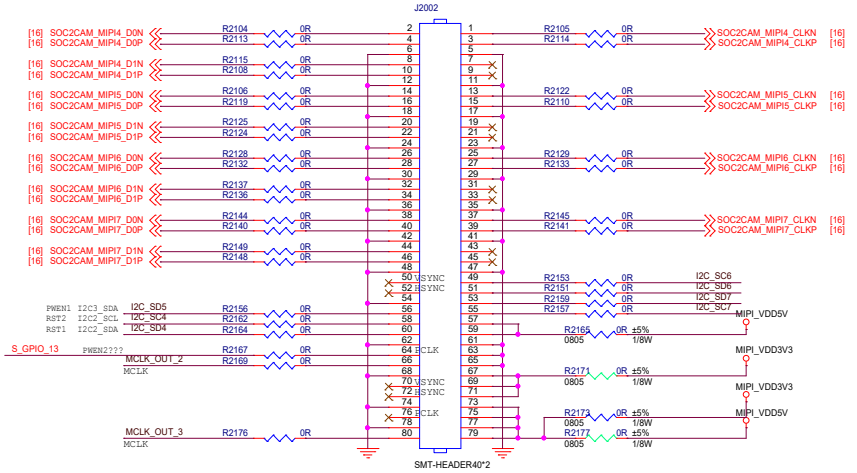
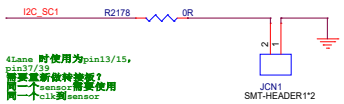
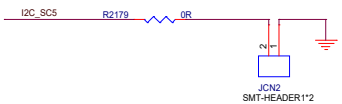
Sensor Connecter



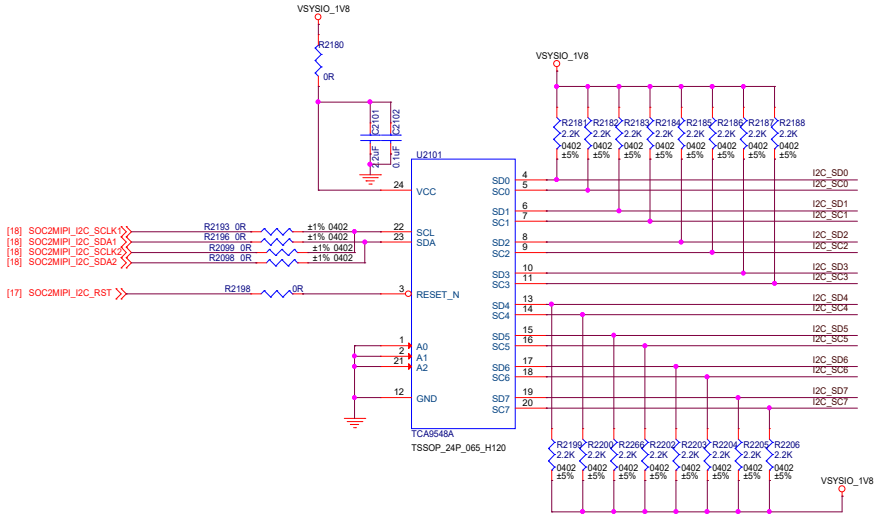


接口定义

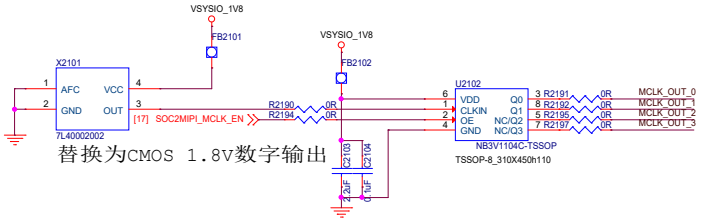




Sensor I2C Switch



Sensor MLCK router



替换为CMOS 1.8V数字输出

artosyn ARTOSYN CONFIDENTIAL		
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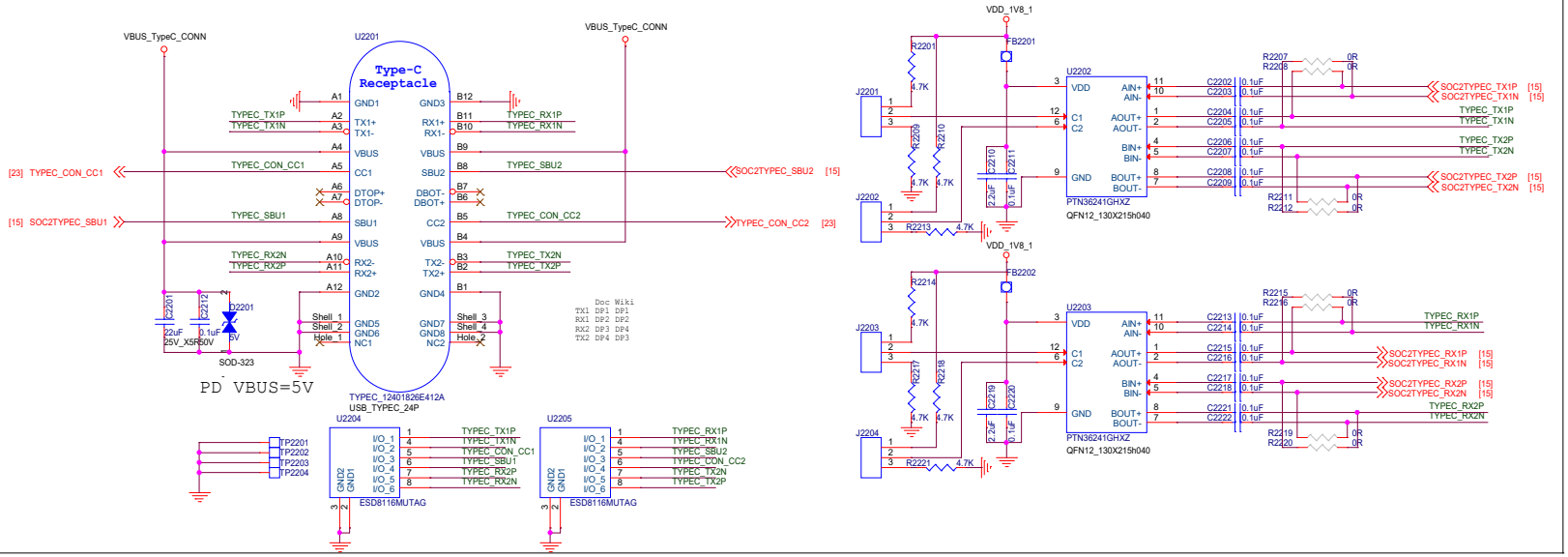
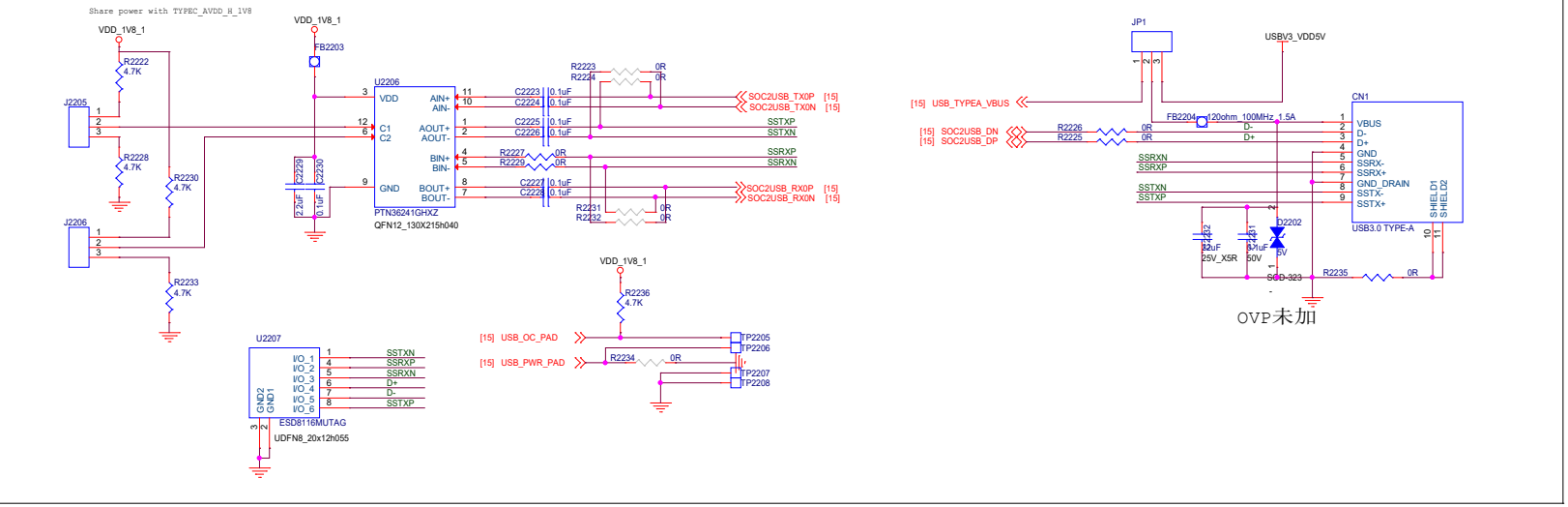
TYPE C Conn: USB3.0、DP and PD



TYPE A Conn: USB3.0 and USB2.0



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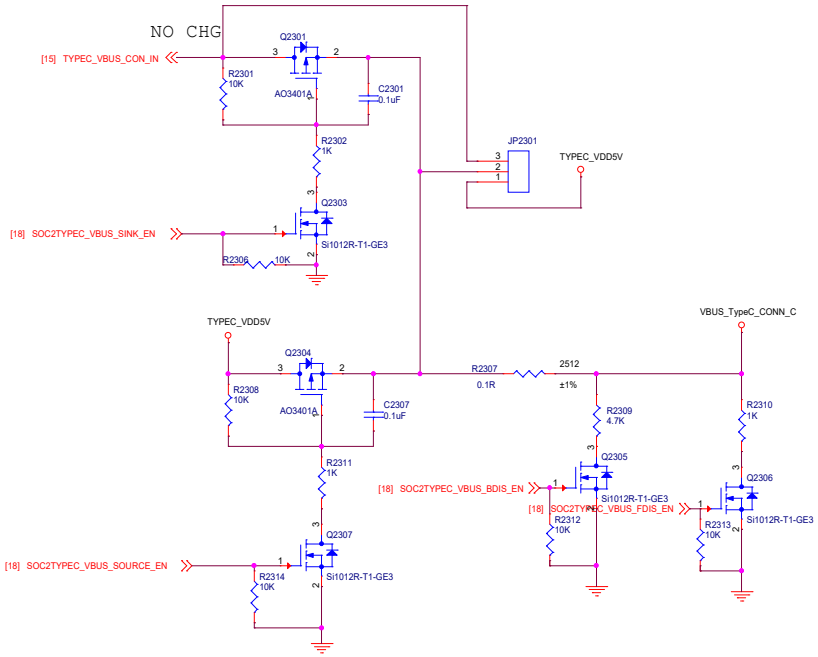
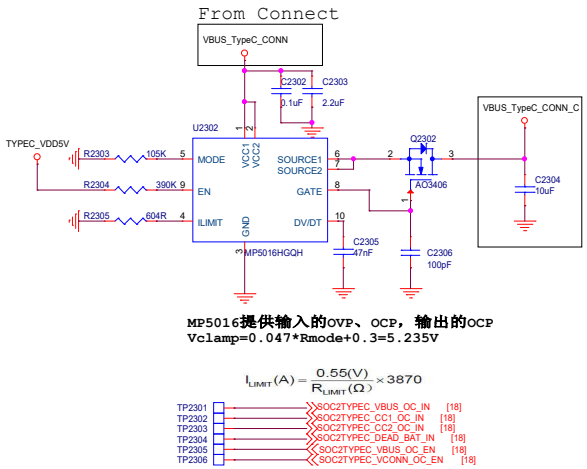
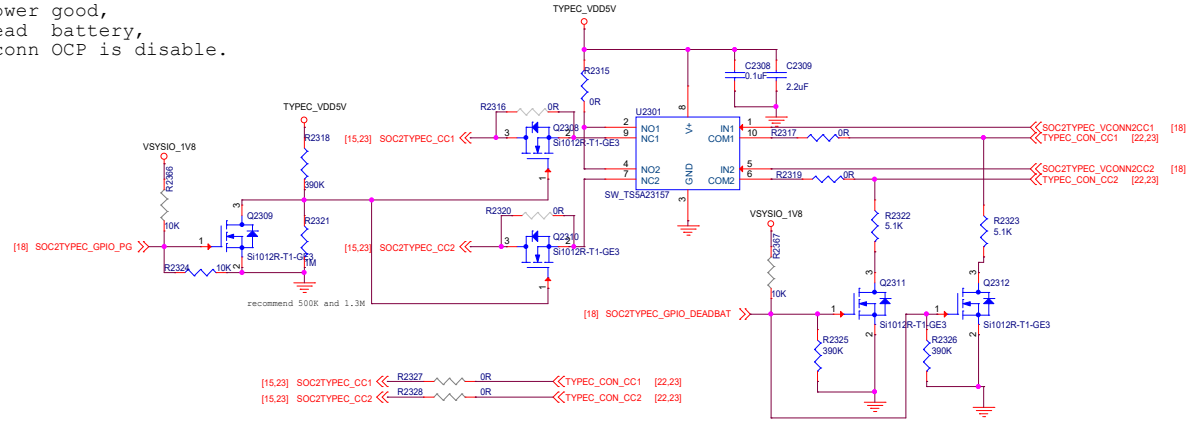
PD Feature option:
1)Discharge,2)Sink/chg and source router



PD Feature option:
1)Input OVP,2)VBUS Input/Output OCP



Type C cc Feature and PD Feature option:
1)Active cable,
2)Power good,
3)Dead battery,
4)Vconn OCP is disable.



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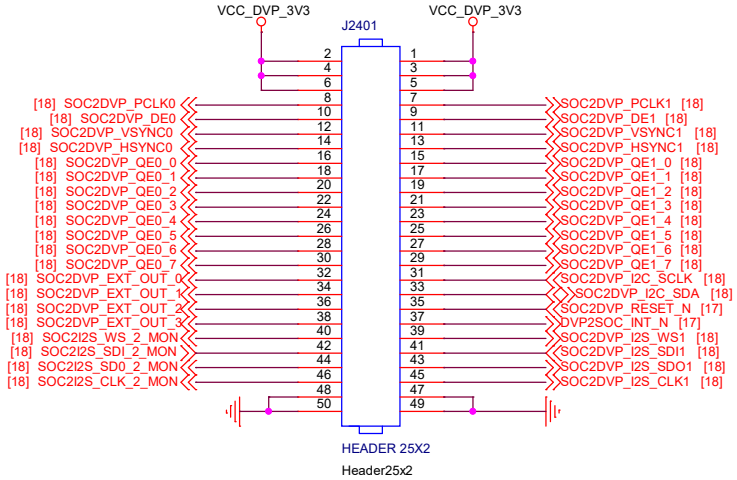

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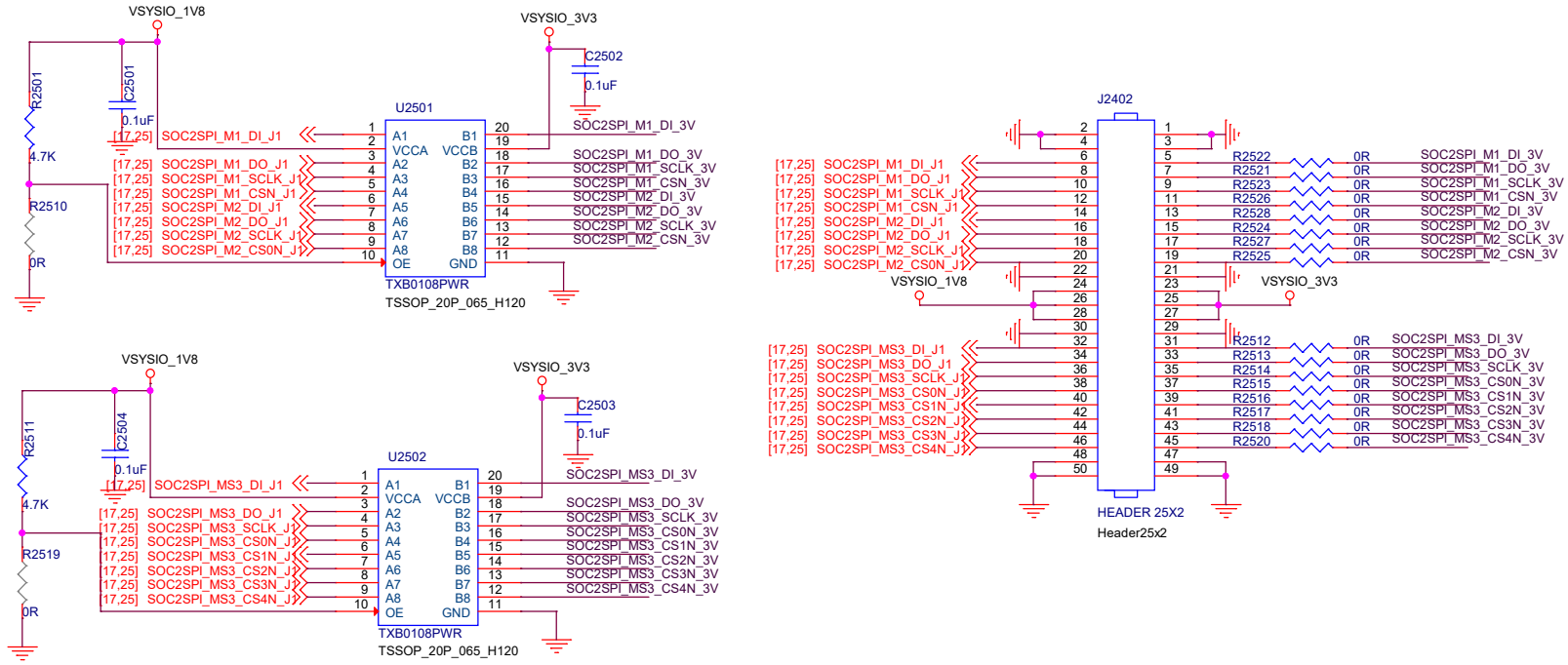

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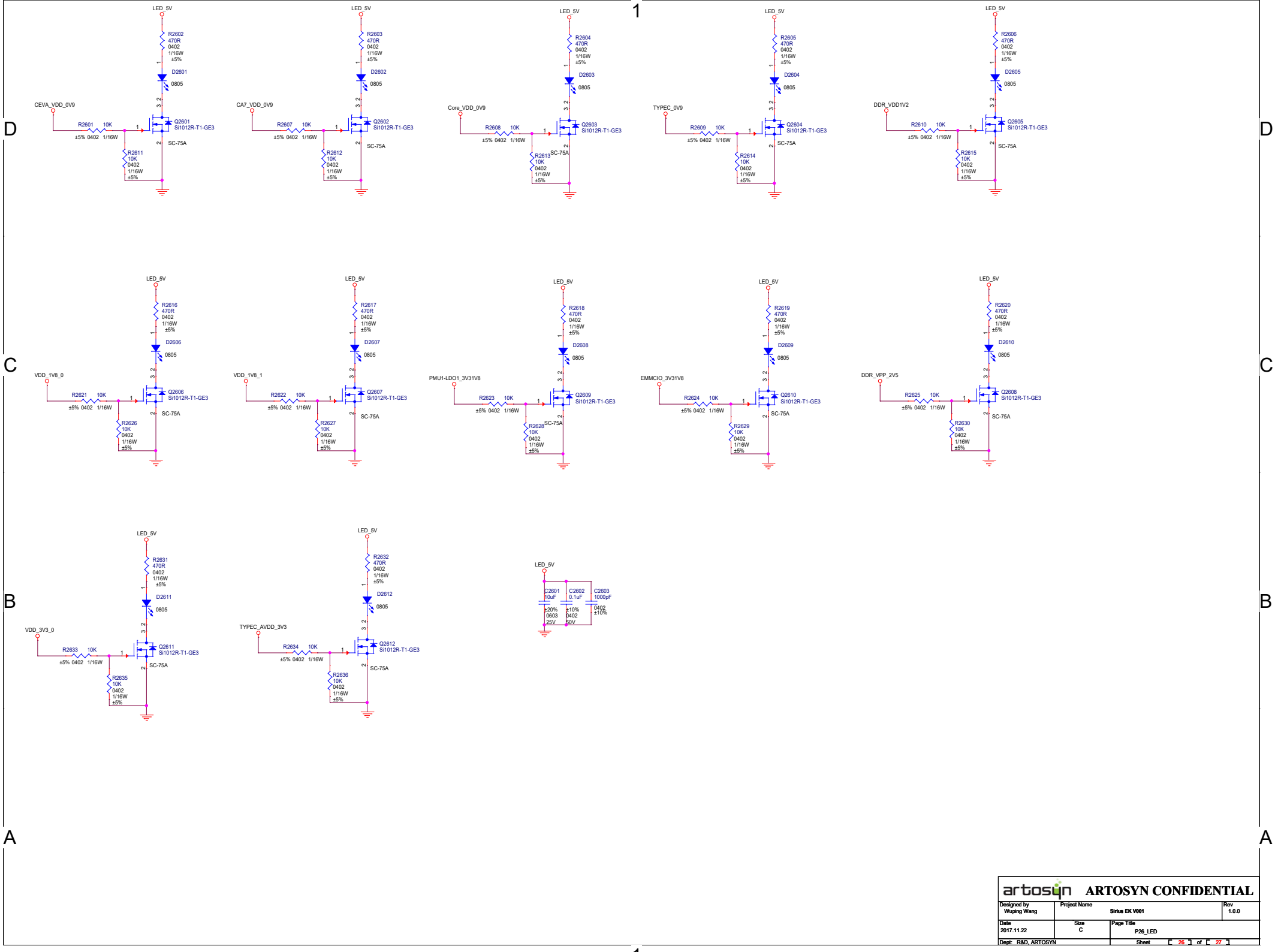

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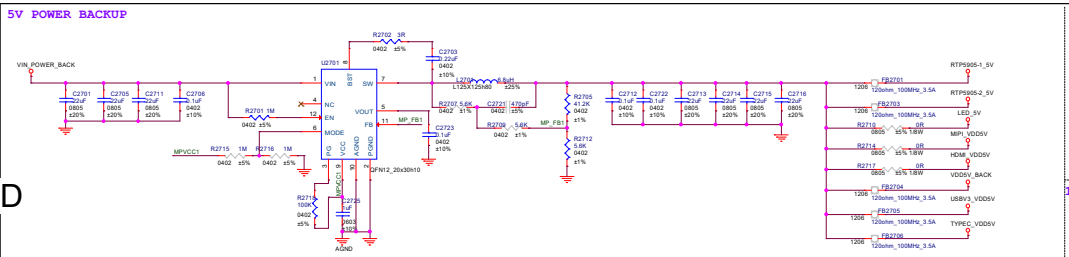
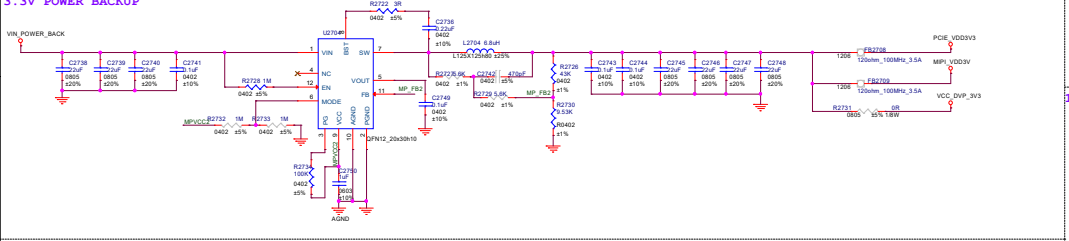
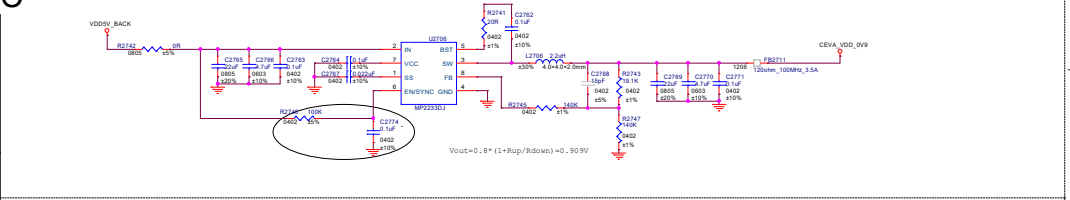
5V POWER BACKUP



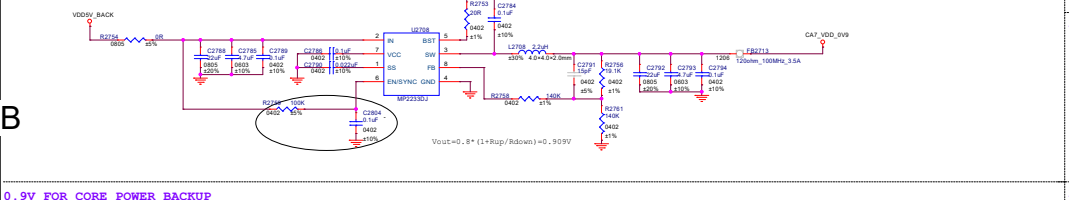
3.3V POWER BACKUP



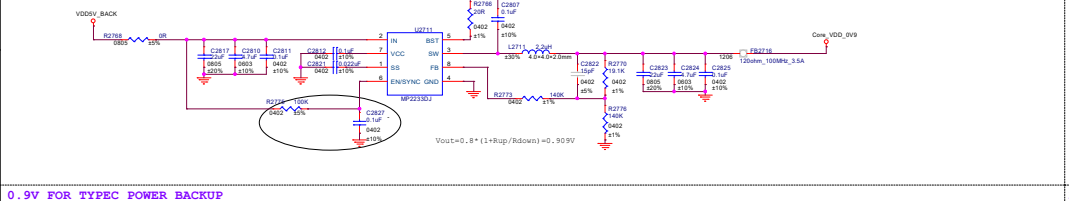
0.9V FOR CEVA POWER BACKUP



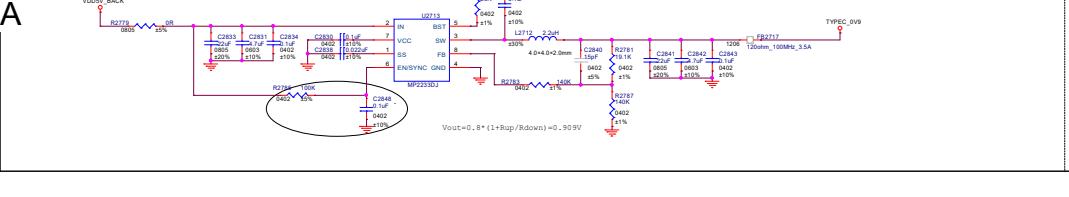
0.9V FOR CA7 POWER BACKUP



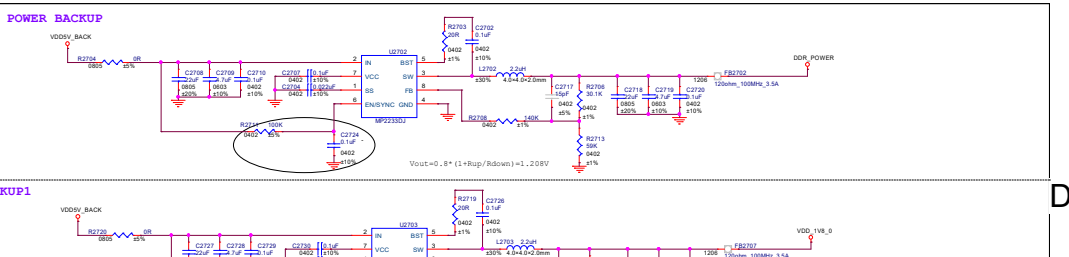
0.9V FOR CORE POWER BACKUP



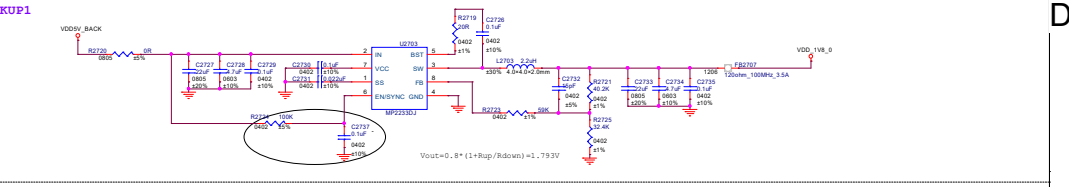
0.9V FOR TYPEC POWER BACKUP



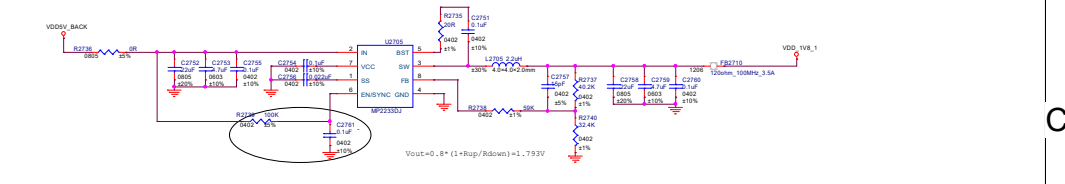
1.2V FOR DDR4 POWER BACKUP



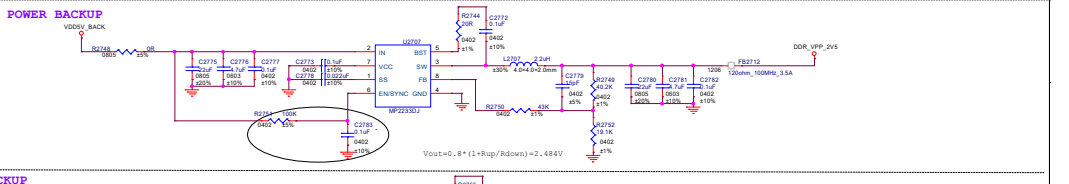
1.8V POWER BACKUP1



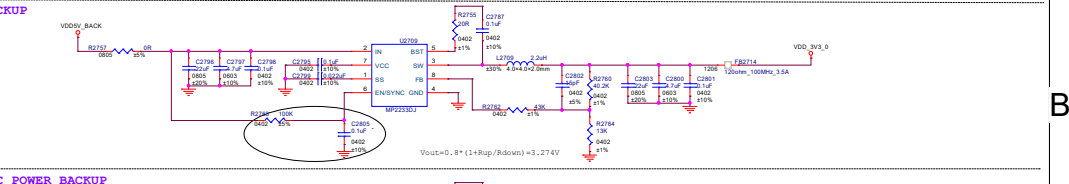
1.8V POWER BACKUP2



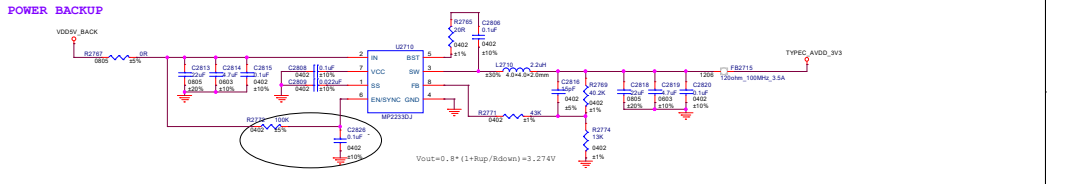
2.5V FOR DDR4 POWER BACKUP



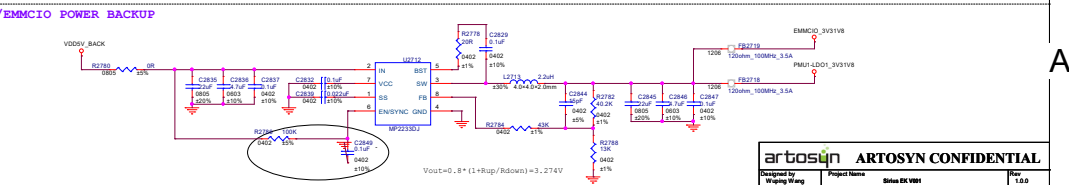
3.3V POWER BACKUP



3.3V FOR TYPEC POWER BACKUP



3.3V FOR SDIO/EMMCIO POWER BACKUP



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