SYNOPSYS®
Predictable Success

Formality Version F-2011.09 Update Training

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Overview

- Changes to Default Behavior
- Enhancements to the GUI
- Low Power
  - Low Power Support Updates
  - Low Power Library Checker
  - Power-Aware Library Verification Mode (LVM)
- ECO Verification
- Enhancements to `synopsys_auto_setup` mode
- Updated Commands and Variables
- New Commands and Variables

CHANGES TO DEFAULT BEHAVIOR

Changes to Default Behavior

- **`verification_force_upf_supplies_on`**
  - In earlier versions, the default was **`false`**
  - Starting with version F-2011.09, the default is **`true`**

- All UPF supplies are constrained to the “on” state.

- After successful “all power on” verification, set this variable to *false* to get a complete verification of all power states.

Changes to Default Behavior

- The following warning message is still generated if the **`verification_force_upf_supplies_on`** variable is set to **`true`**.

```
ATTENTION: Verification was run with all UPF supplies
constrained to their ON state. This is only a partial
verification result as it does not cover all
operational states.
```

- Reasons for change
  - Runs UPF verification faster
  - Allows debugging of UPF issues before a full PST verification

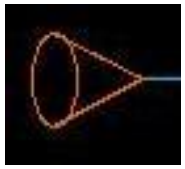
ENHANCEMENTS TO THE GUI

Enhancements to the GUI

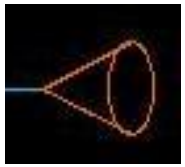
- Viewing objects
  - Design View
  - Logic Cone View
- Probe points
  - Inverted probe
  - 1-to-N probe
- Zoom in and out of a view
  - Zoom 2x
  - Zoom Selected
- Auto-run option in hierarchical script dialog

Enhancements to the GUI

- The GUI displays only the selected object and one level of fanin or fanout.
- Faster load time for GUI.
- You can expand the design to view additional logic of the parent design.

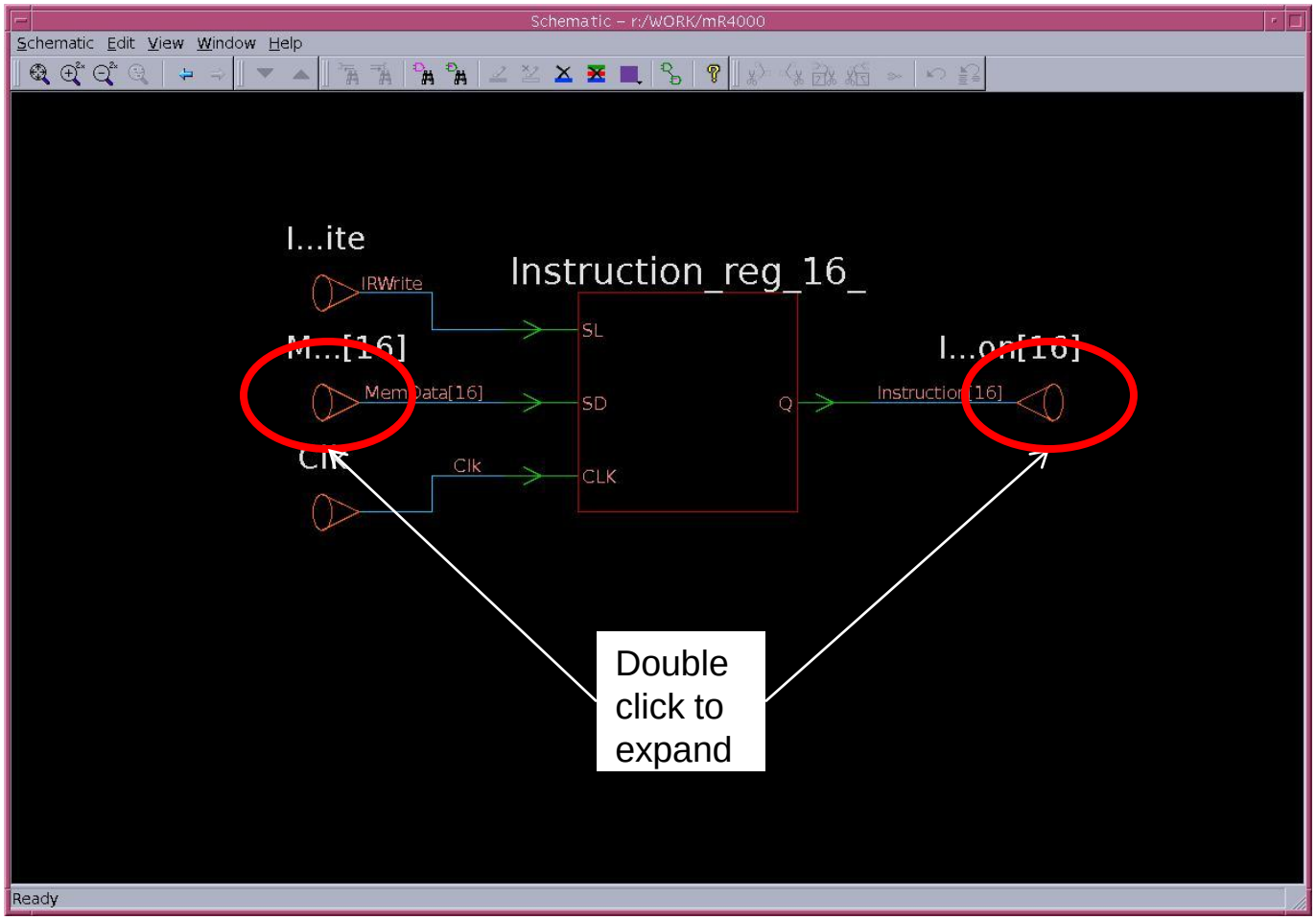


Symbol to expand the fanin

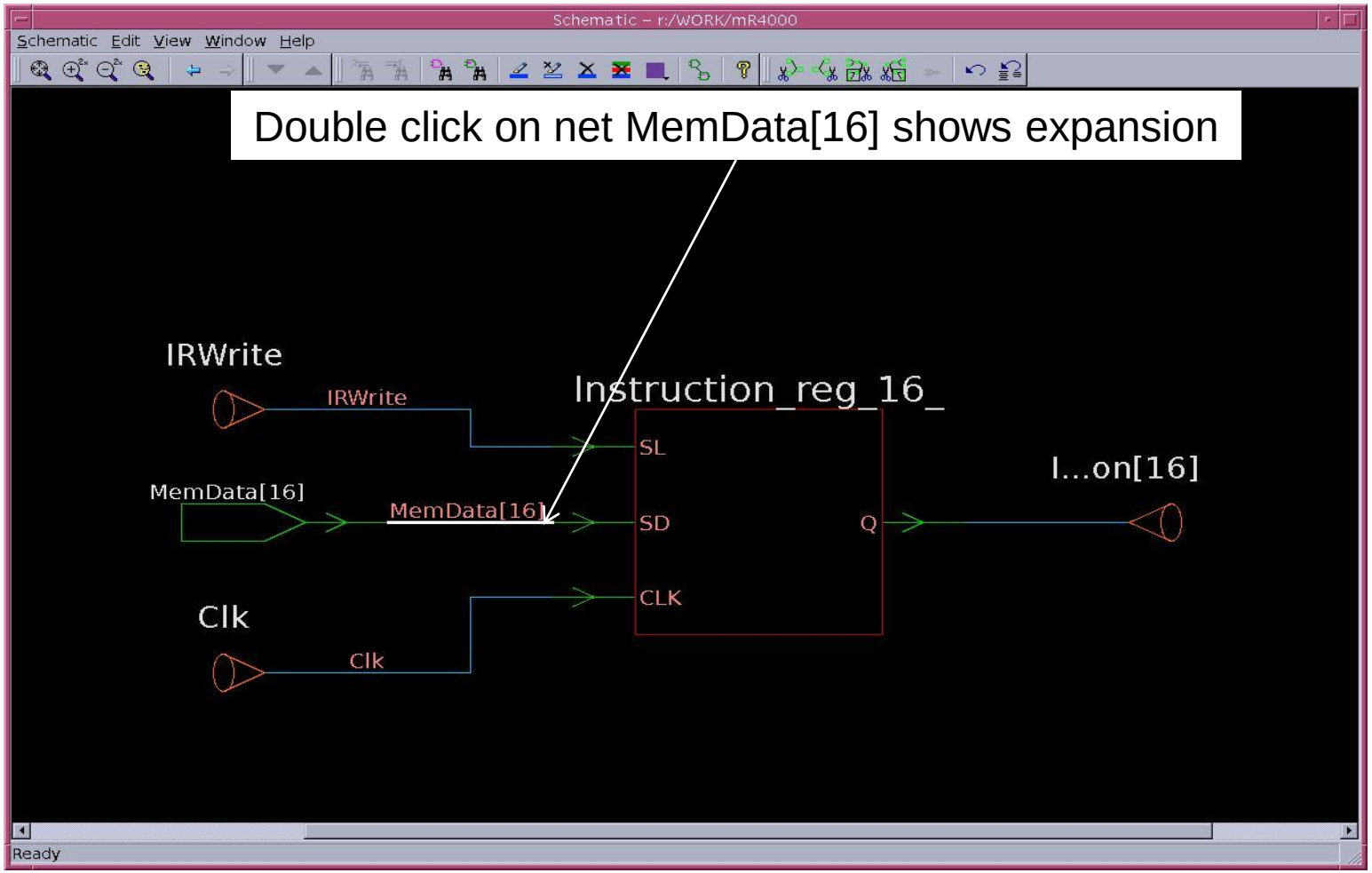


Symbol to expand the fanout

Enhancements to the GUI



Enhancements to the GUI



Enhancements to the GUI

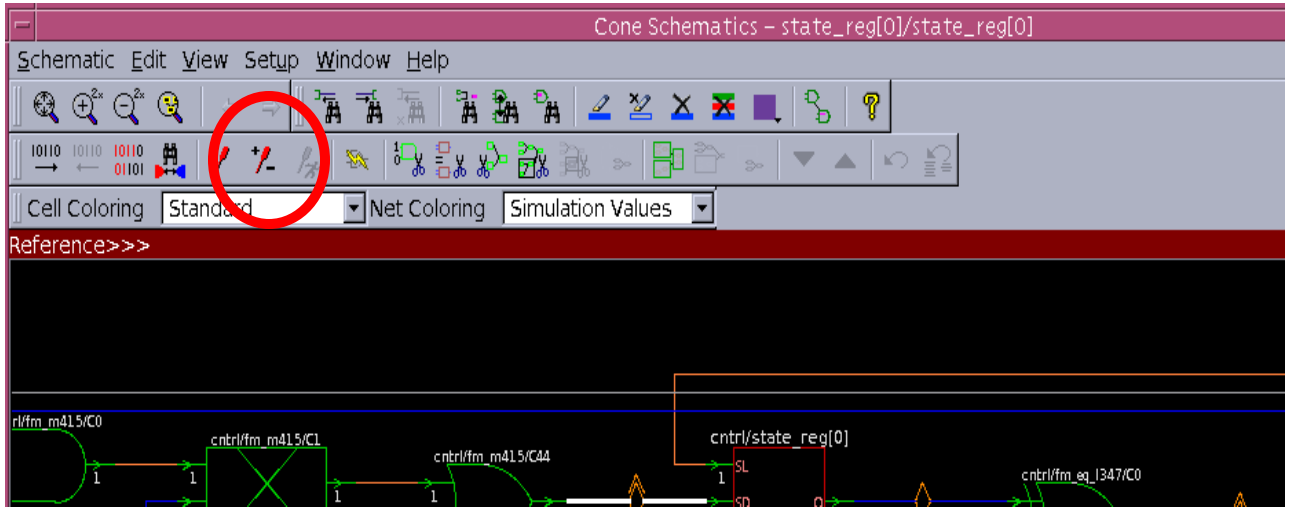
- Control of schematic expansion
  - Mouse double click
    - Expands one level
  - Shift + Mouse double click
    - Completely expands branch
  - Menu Bar Edit -> Prune -> Expand schematic
  - Shows full schematic

Enhancements to the GUI

- Probe point enhancements
  - Inverted probe
  - 1-to-N probe
- In earlier versions, these features were available only in the batch mode.
- Starting with version F-2011.09, they are also available in the GUI.

Enhancements to the GUI

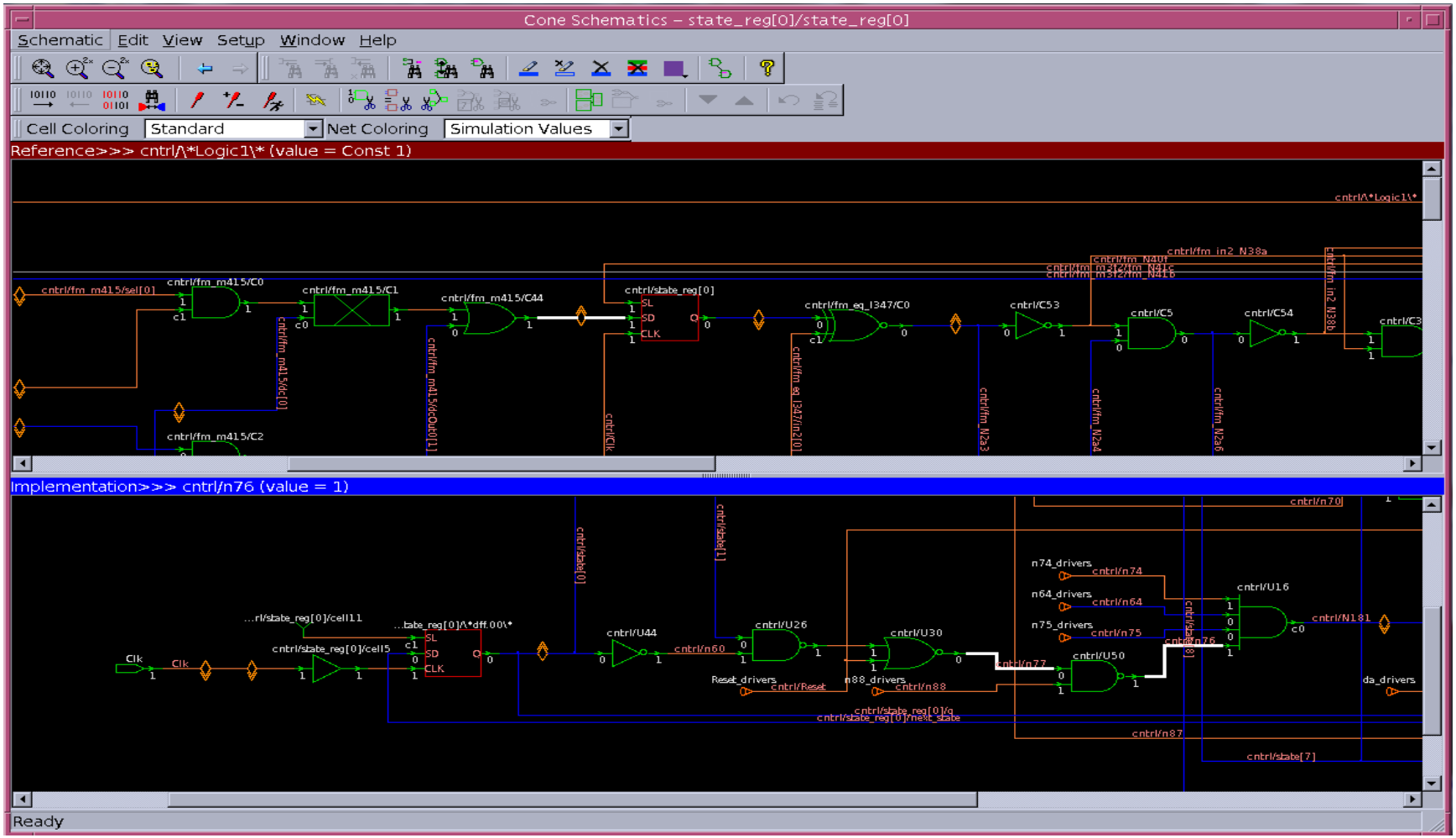
- Select a probe point in the Schematic window.
- Click “Set Inverted Probe Point”.



Enhancements to the GUI

- Setting a 1-N probe point
  1. Select a reference net.
  2. Select N implementation nets.
     1. Click to select the first implementation net.
     2. Ctrl + click to select the remaining implementation nets.

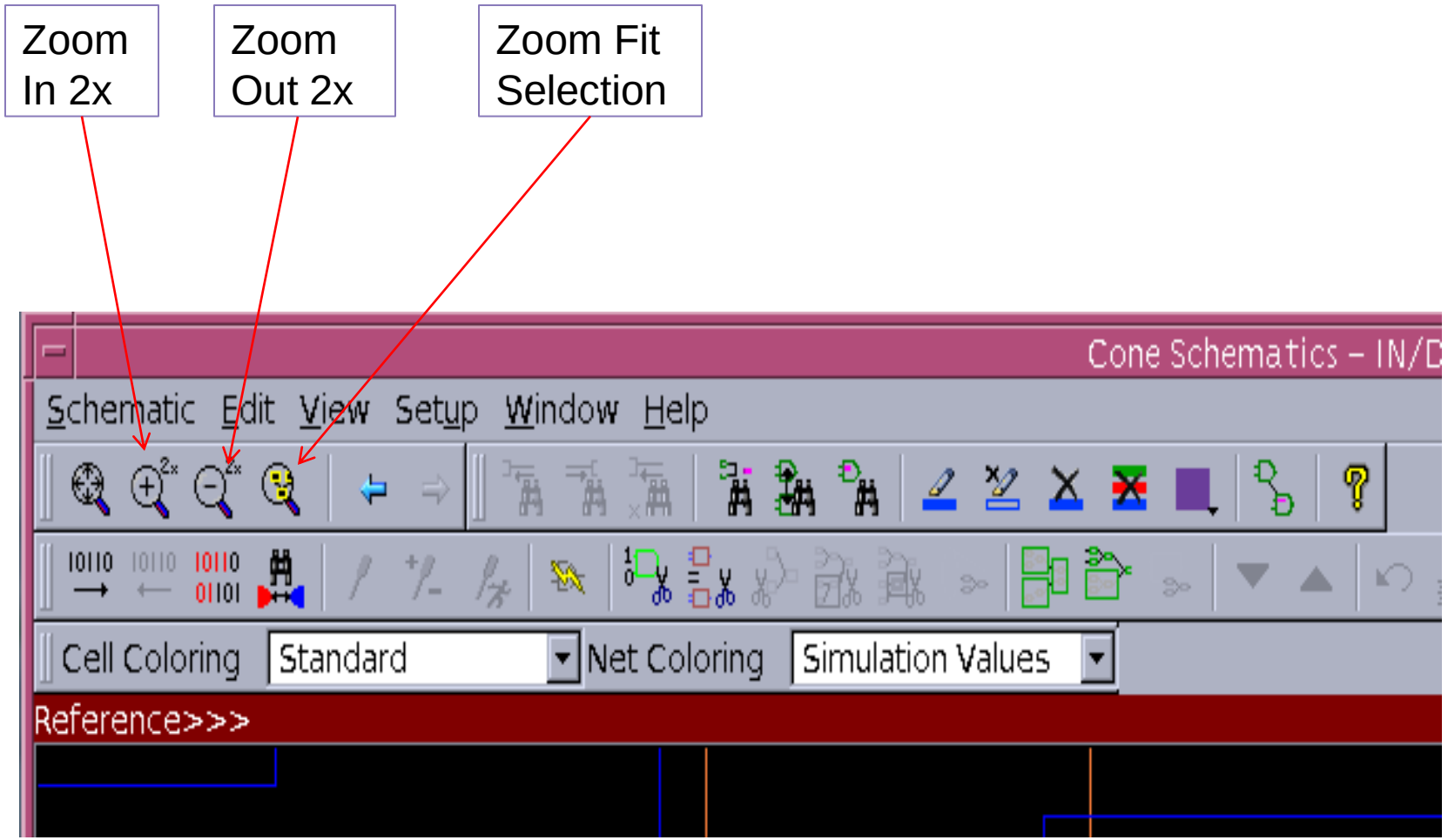
Enhancements to the GUI



Enhancements to the GUI

- Zoom the view of a schematic (E-2010.12-SP2)
  - Three new buttons on the Zoom Bar
  - Zoom In 2x (keyboard “i”) – Increase the magnification in the active view by 2x
  - Zoom Out 2x (keyboard “o”) - Shrink the magnification in the active view by 2x
  - Zoom Fit Selection (keyboard “t”) – Zoom to a selected design
- Available in all schematic windows

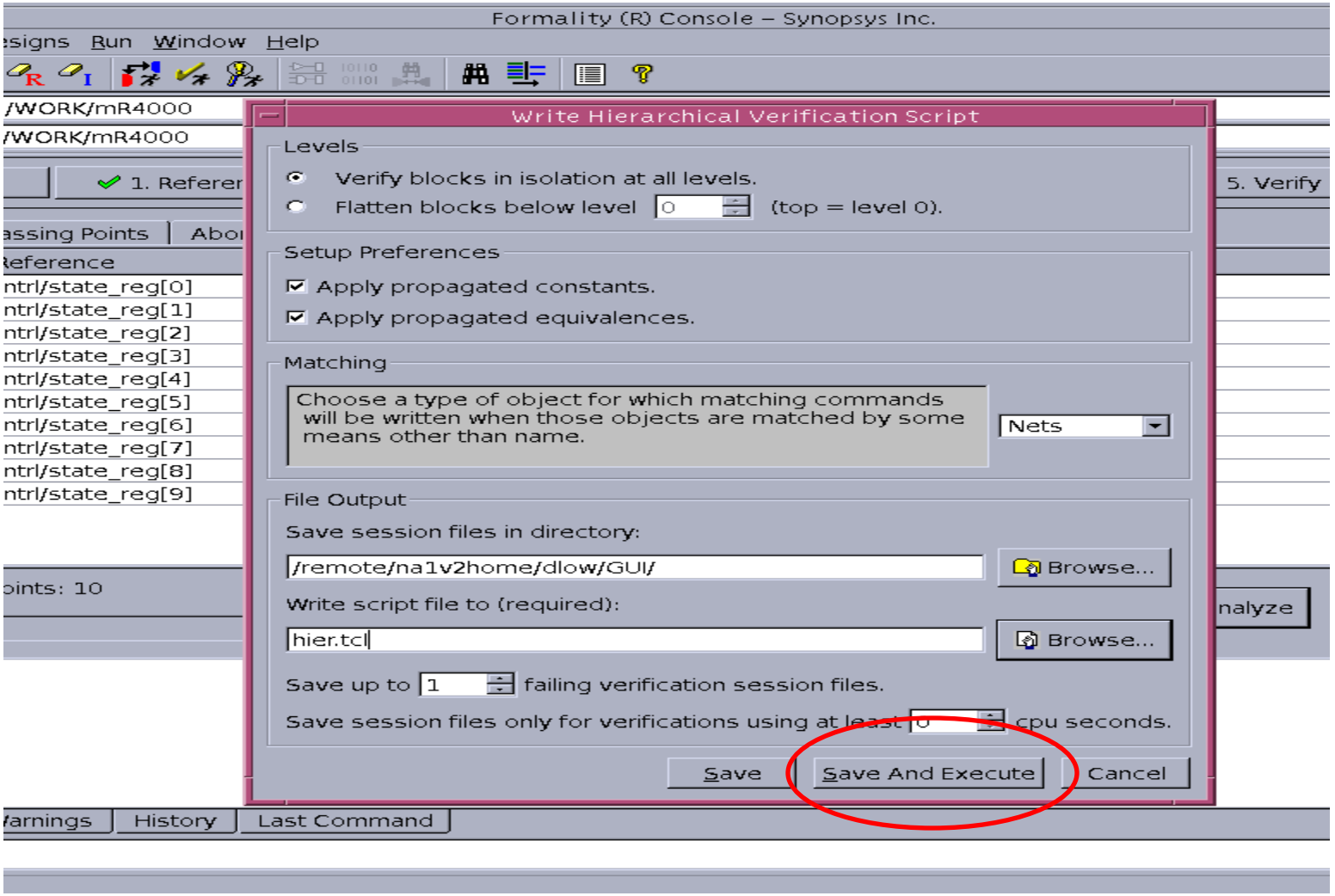
Enhancements to the GUI



Enhancements to the GUI

- Auto-run option in the Write Hierarchical Script window
  - Available since E-2010.12-SP1
  - Execute the hierarchical verification script upon creation
  - Available only in the GUI
  - Saves from having to “source” hierarchical verification script

Enhancements to the GUI



LOW-POWER DESIGN SUPPORT

Low-Power Design Support

- Formality supports the Synopsys Low-Power Flow
- Any UPF design in the Synopsys flow can be formally verified
- Updated UPF Commands
- New UPF Commands
- New Formality Variables for UPF Support

Low-Power Design Support

- Updated Commands
  - set_isolation
    -source
    -sink
    -elements
    -applies_to

You can now use these options simultaneously. The ports must satisfy all the filters that are applied.

  - set_isolation_control -location fanout

  - set_port_attribute
    -receiver_supply supply_set_ref
    -driver_supply supply_set_ref

Low-Power Design Support

- `set_retention`
  - `-save_condition {{boolean_function}}`
  - `-restore_condition {{boolean_function}}`
  - `-retention_condition {{boolean_function}}`

These retention options allow for more complex descriptions to control the save, restore, or retention behavior of the retention devices.

Low-Power Design Support

- `set_retention_control`
  `-assert_r_mutex {{net_name <high | low}}`
  `-assert_s_mutex {{net_name <high | low}}`
  `-assert_rs_mutex {{net_name <high | low}}`

- These assertions should have been verified (to not be triggered) with simulation.

- Formality inserts logic that generates don't care attributes on the retention devices if the assertion has been violated.

Low-Power Design Support

- Formality now supports the following new commands:
  - `query_cell_instances`
  - `query_cell_mapped`
  - `query_net_ports`
  - `query_port_net`
  - `find_objects`
  - `create_logic_net`
  - `create_logic_port`
  - `connect_logic_net`

Low-Power Design Support

New Formality variables to support UPF

- `verification_insert_upf_isolation_cutpoints`
  - Default is true.
  - Formality automatically inserts cut points on the data inputs of isolation cells.
    - Creating manual cut points and using the `set_constraint` command between ISO and power controls is no longer required.
    - Reduces false failing points due to x propagation differences and prevents unknown values from escaping from the powered off domain when the isolation cell is not active.
    - Better verification performance.

Low-Power Design Support

New Formality variables to support UPF

- `upf_warn_on_failed_parallel_resolved_check`
  - The default is false.
  - Formality reports an error if a parallel driven supply net does not have all of the same root voltage driver.
    - Compliant with the IEEE-1801 standard.
    - Changing this variable to true will resolve this check to a warning and allows the `load_upf` command to proceed.

Low-Power Design Support

New Formality variables to support UPF

- `upf_create_implicit_supply_sets`
- The default is false.
- Controls which UPF supply nets are used by Formality for UPF `set_isolation -location fanout` command.
- When this variable is set to false, the default isolation cell supplies are defined by the `set_isolation -location fanout` command
- When the variable is set to true, the supplies for these isolation cells are the sink domain default isolation supply set
- Any explict `connect_supply_net` commands override these default connections.

Low-Power Design Support

New Formality variables to support UPF

- `hdlin_merge_parallel_switches`
- The default is true. (Available since E-2010.12-SP3)
- For PG netlist with multiple coarse grain switch cells you can have nets driven by multiple parallel switch cells
- Affects verification performance and makes debugging difficult
- Merges switch cells that are equivalent.
  - Schematics are easier to read
  - Works on .db file format libraries only (not Verilog cells)
- Messages are added to the log file
  - The supply nets that were affected
  - The number of driving switch cells that were eliminated

LOW-POWER LIBRARY CHECKER

Low-Power Library Checker

- Low-power libraries might contain cells that are incorrectly or incompletely modeled with respect to their power behavior

- The new checker for low-power library cells checks for:
  - Modeling consistency
  - Completeness

- Indicates verification problems before they occur

Low-Power Library Checker

- The library checker performs checks for the following:
  - All power cells
    - Unread power and ground pins
    - Missing power-down function on outputs
    - Inconsistent pin directions
    - Supply net driven by both a port and a constant
  - Switch cells
    - Switched supply used internally
    - Missing or invalid switch function
  - Retention cells
    - Missing second (retention) SEQ
    - Missing save or restore signals
    - Missing backup supplies
    - Missing paths between the SEQs

Low-Power Library Checker

- Example transcript from the log file after running the `set_top` command

```
************ Library Checking Summary ************
Warning:  300 unlinked power cell(s) with unread pg pins.
Warning:  610 unlinked power cell(s) with no power down functions on outputs.
Warning:  24 unlinked power cell(s) with no retention ff or latch.
Warning:  4 unlinked power cell(s) marked as retention with unread backup pg pins.
Use 'report_libraries -defects all' for more details.
**************************************************
```

- Reports all linked and unlinked cells

Low-Power Library Checker

- Update to the `report_libraries` command:
  - `report_libraries -defects errors`
    Reports model defects that will cause load_upf errors
  - `report_libraries -defects all`
    Reports all model defects

```
#########################################
####    TECH LIB - r:/PGLIB
#########################################
Library Cell /Defect List                Attributes
-------------------------                ----------
buf_hdr_swnpd#PWR                          u
   port Y : no power_down_function
buf_hdr_sw2pg#PWR                          u
   port VDDB : unread pg_pin
   port VSSB : unread pg_pin
```

Example transcript output

Low-Power Library Checker

- Variable to ignore errors

```
set hdlin_library_ignore_errors true
```

- The default is *true*.
- If set to *false*, errors detected cause the set_top or load_upf commands to fail.

- Containers are not backward compatible.

Low-Power Library Checker

- Errors in the following can be automatically corrected
  - All power cells
  - Unread power/ground pins
  - Missing PDF (power down function) on outputs
  - Inconsistent pin directions
  - Supply net driven by both a port and a constant

LIBRARY VERIFICATION MODE FOR POWER-AWARE CELLS

Library Verification Mode for Power-Aware Libraries

- DB cell libraries can contain both non-power aware and power aware versions
- Because the current LVM would only use the non-power aware DB cell model, LVM could not verify:
  - power aware Verilog to power aware DB
  - power aware DB to power aware DB

Library Verification Mode for Power-Aware Libraries

- Two modes added to verify power aware versions
  - `library_verification VERILOG_PWRDB`

    Verify power aware Verilog cells with power-aware DB cells.
  - `library_verification PWRDB_VERILOG`

    Verify power-aware DB cells with power aware Verilog cells.

- Changes to the `library_verification DB_DB` verification modes:
  - Verifies both non power and power designs
  - Reports unmatched designs including power designs

Library Verification Mode for Power-Aware Libraries

- Reports updated to show match and unmatched designs including power designs

Designs in DB_ref
- A
- B
- C
- A#PWR
- B#PWR
- C#PWR

Designs in DB_imp
- A
- B
- D
- A#PWR
- B#PWR
- D#PWR

Matched Design list
- A
- B
- A#PWR
- B#PWR