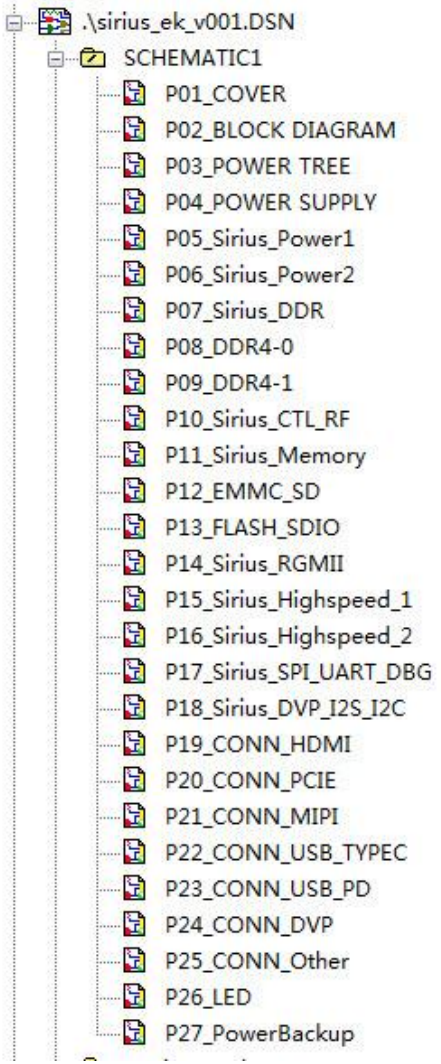





| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name **Sirius EK V001** | Rev 1.0.0 |
| Date 2017.11.22 | Size A4 | Page Title P01_COVER |
| Dept: R&D, ARTOSYN | | Sheet [ 1 ] of [ 27 ] |

1

D

C

B

A

D

C

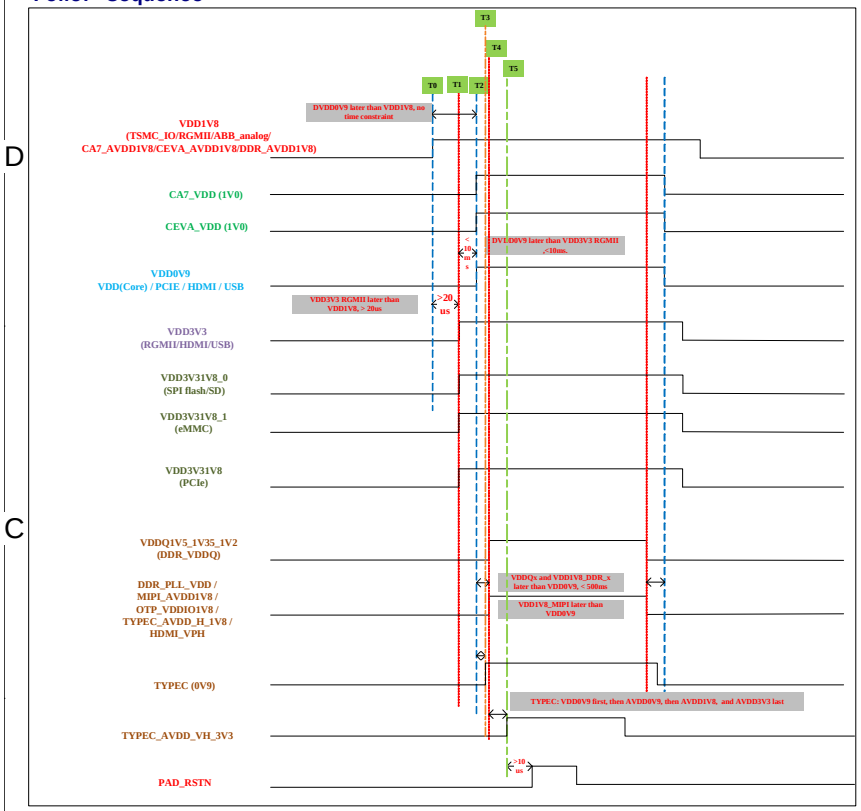
B

A

artosyn **ARTOSYN CONFIDENTIAL**

| | | |
|---|---|---|
| Designed by<br>Wuping Wang | Project Name<br>**Sirius EK V001** | Rev<br>1.0.0 |
| Date<br>2017.11.22 | Size<br>A4 | Page Title<br>P02_BLOCK DIAGRAM |
| Dept: R&D, ARTOSYN | | Sheet [ 2 ] of [ 27 ] |

## Power Sequence

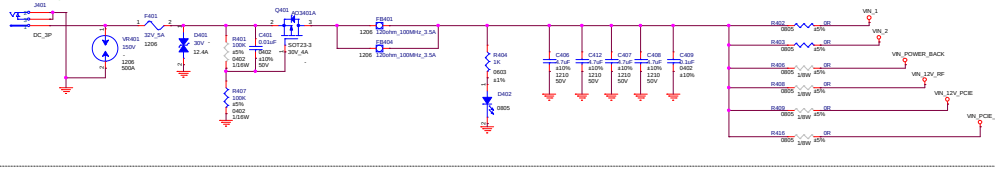



## Power Tree

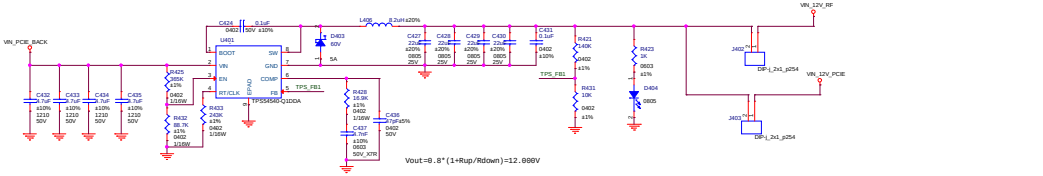
| | ARTOSYN CONFIDENTIAL | | |
|---|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | | Rev 1.0.0 |
| Date 2017.11.22 | Size C | Page Title P03_POWER TREE | |
| Dept: R&D_ARTOSYN | | Sheet 3 of 27 | |

## POWER INPUT

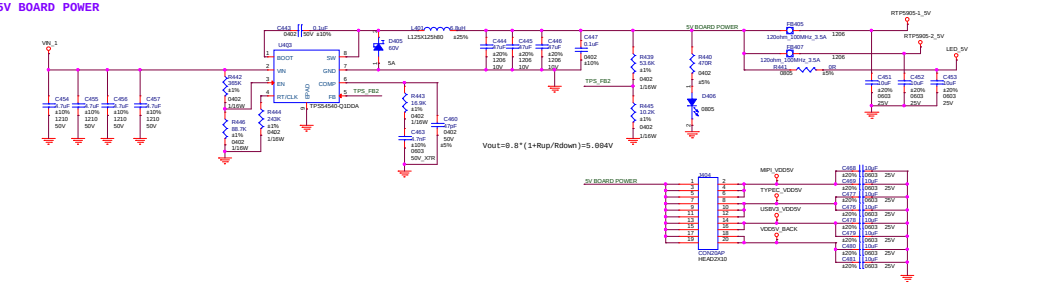
12V-24V Input



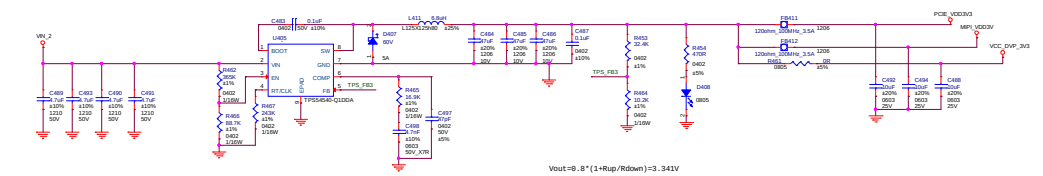
## 12V PCIE&RF CON POWER



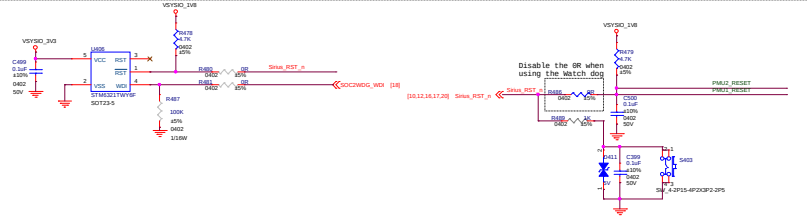

## 5V BOARD POWER



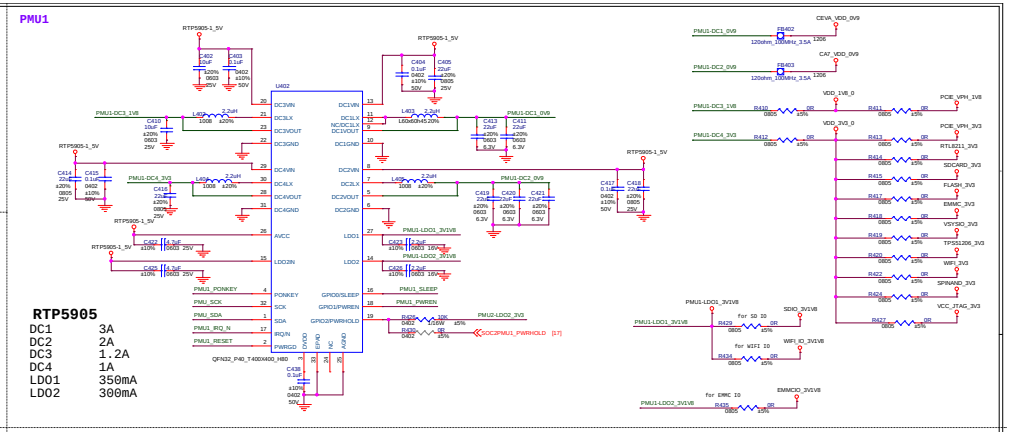

## 3.3V CON POWER




## SYSTERM RESET



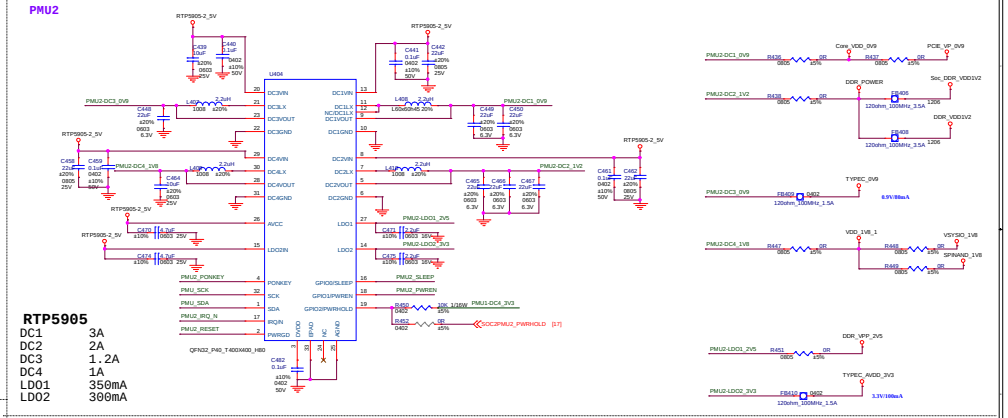

## PMU1



**RTP5905**

| | |
|---|---|
| DC1 | 3A |
| DC2 | 2A |
| DC3 | 1.2A |
| DC4 | 1A |
| LDO1 | 350mA |
| LDO2 | 300mA |

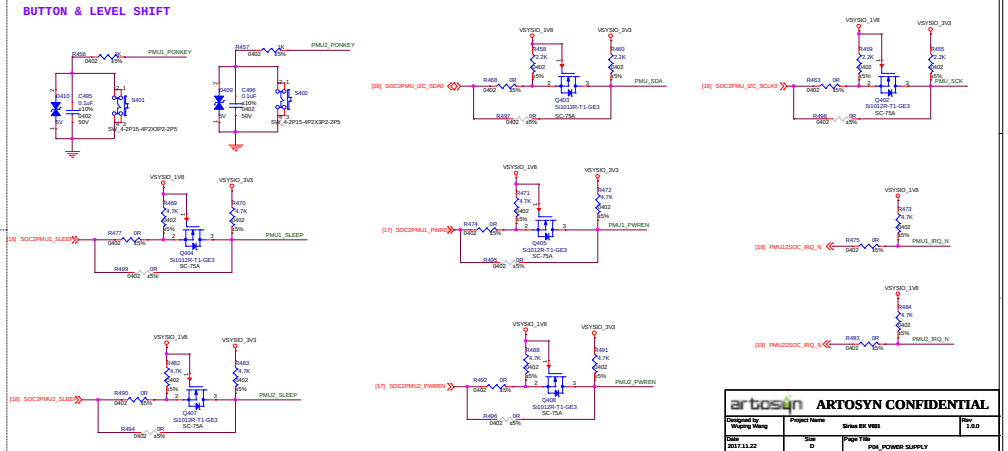
## PMU2



**RTP5905**

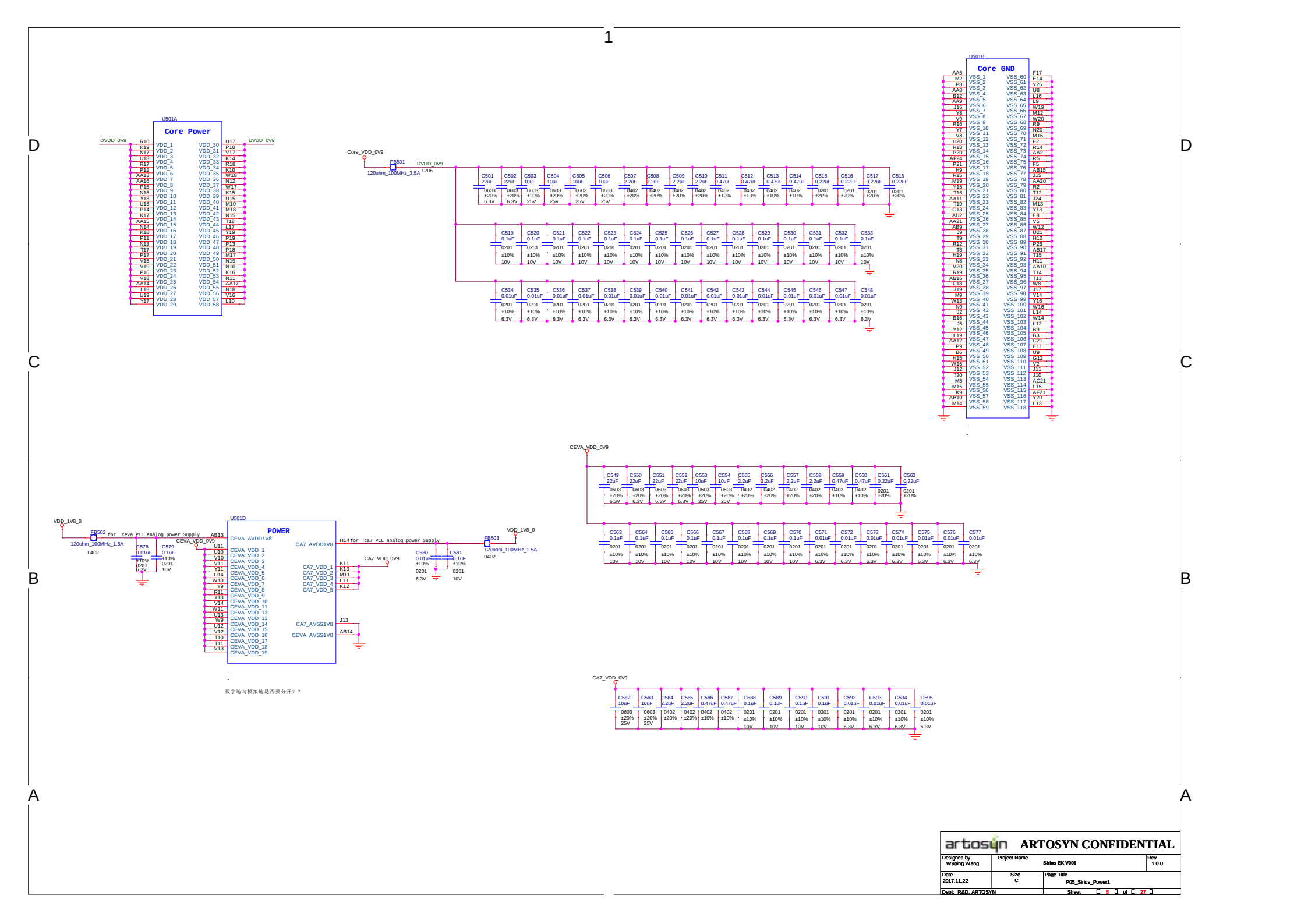
| | |
|---|---|
| DC1 | 3A |
| DC2 | 2A |
| DC3 | 1.2A |
| DC4 | 1A |
| LDO1 | 350mA |
| LDO2 | 300mA |

## BUTTON & LEVEL SHIFT

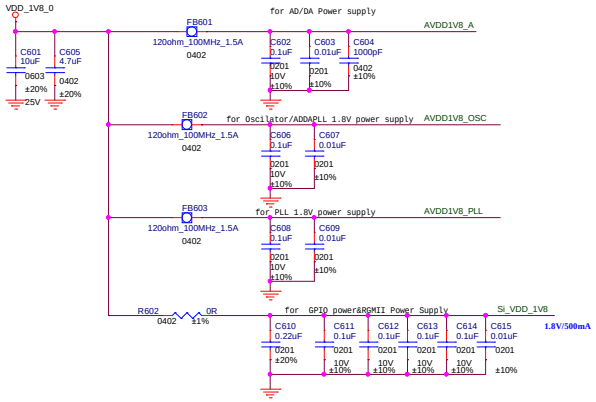


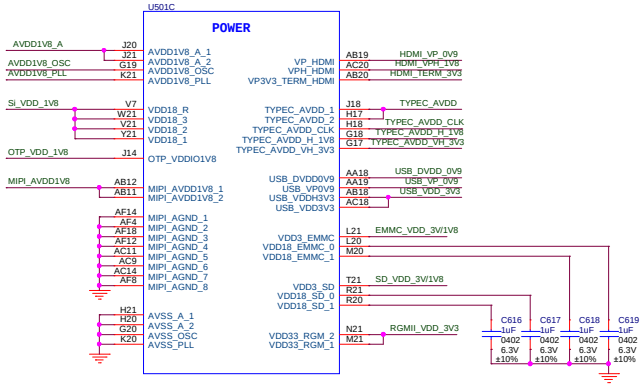


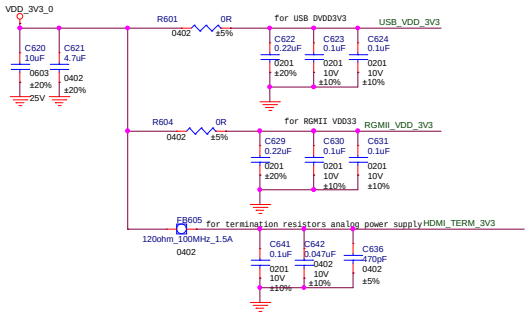
| | | |
|---|---|---|
| Designed by: Wuping Wang | Project Name: Sirius EK V001 | Rev: 1.0.0 |
| Date: 2017.11.22 | Size: D | Page Title: P04_POWER SUPPLY |
| Dept: R&D_ARTOSYN | Sheet: 4 of 27 | |

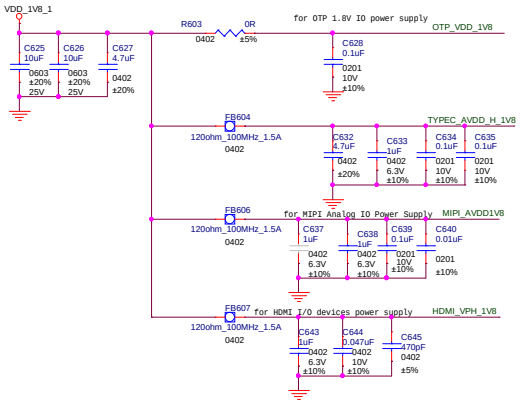


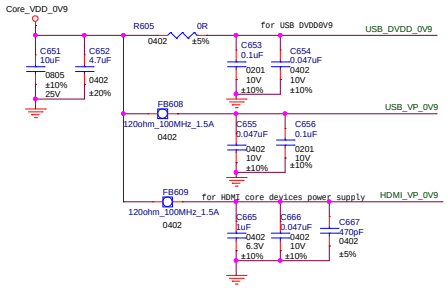

| | | | |
|---|---|---|---|
| artosyn ARTOSYN CONFIDENTIAL | | | |
| Designed by Wuping Wang | Project Name Sirius EK V001 | | Rev 1.0.0 |
| Date 2017.11.22 | Size C | Page Title P05_Sirius_Power1 | |
| Dept: R&D ARTOSYN | | Sheet 5 of 27 | |

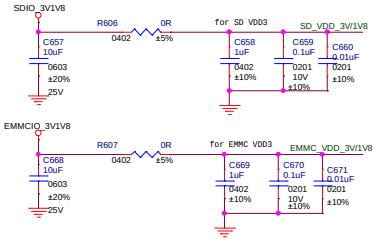


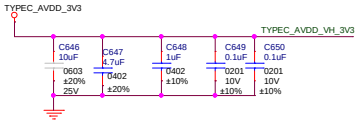



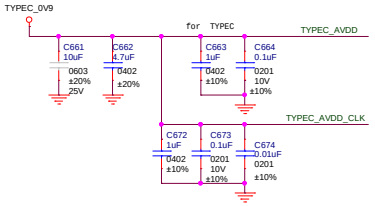



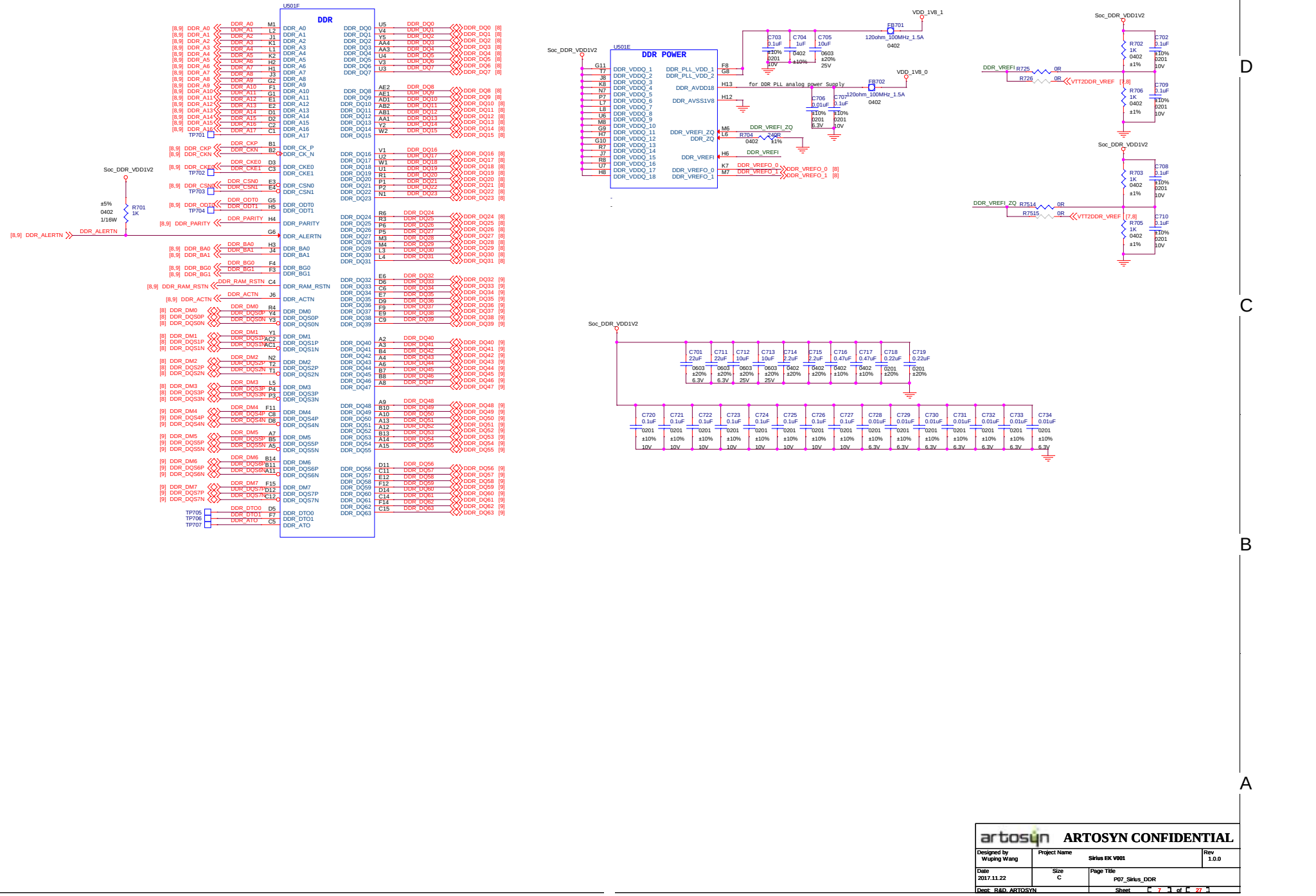



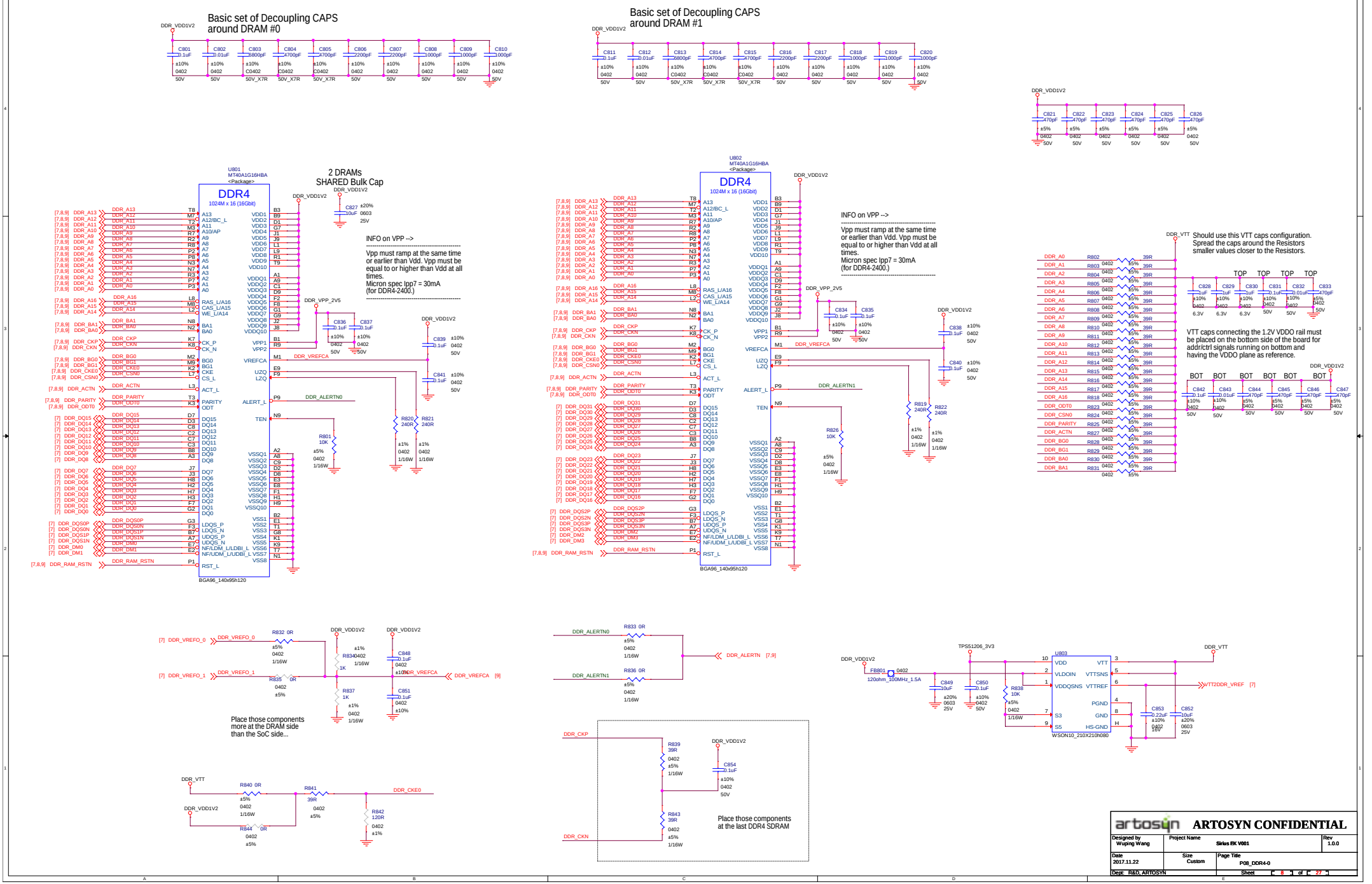



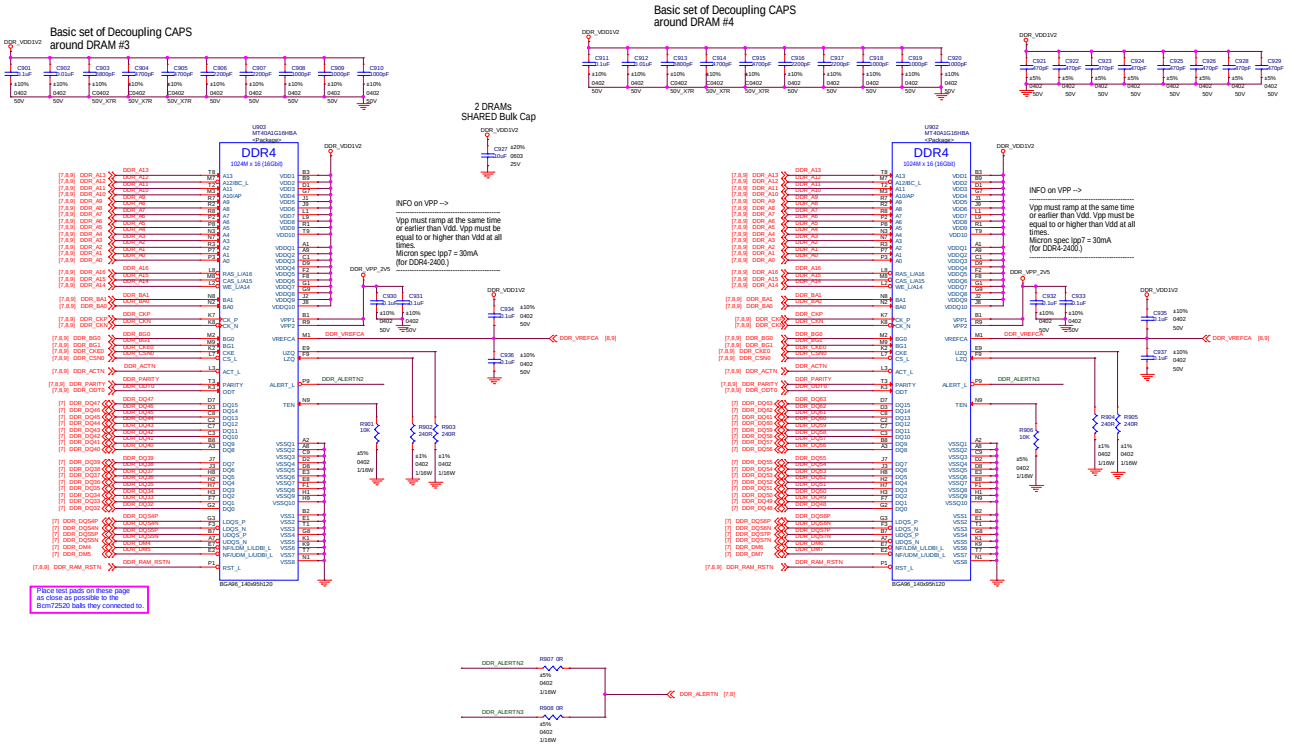

| | | |
|---|---|---|
| artosyn **ARTOSYN CONFIDENTIAL** | | |
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size C | Page Title P06_Sirius_Power2 |
| Dept: R&D, ARTOSYN | Sheet 6 of 27 | |





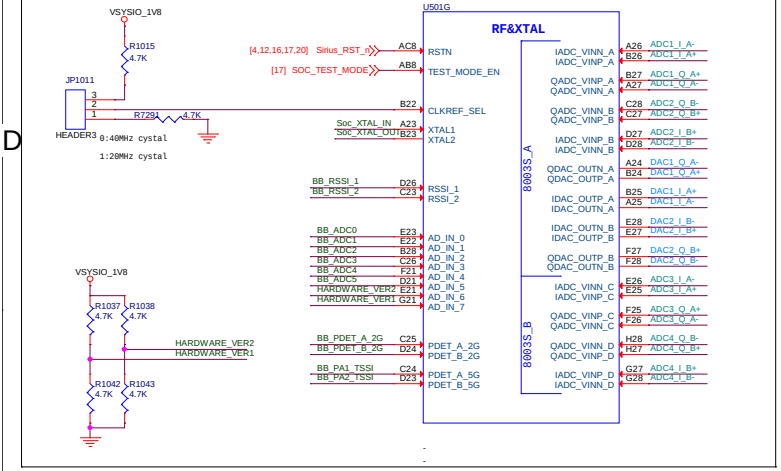

| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size C | Page Title P07_Sirius_DDR |
| Dept: R&D ARTOSYN | | Sheet 7 of 27 |


Basic set of Decoupling CAPS around DRAM #0
Basic set of Decoupling CAPS around DRAM #1
2 DRAMs SHARED Bulk Cap
U801 MT40A1G16HBA <Package>
U802 MT40A1G16HBA <Package>
DDR4
1024M x 16 (16Gbit)
BGA96_140x95h120
INFO on VPP -->
Vpp must ramp at the same time or earlier than Vdd. Vpp must be equal to or higher than Vdd at all times.
Micron spec Ipp7 = 30mA (for DDR4-2400.)
Should use this VTT caps configuration. Spread the caps around the Resistors smaller values closer to the Resistors.
VTT caps connecting the 1.2V VDDO rail must be placed on the bottom side of the board for addr/ctrl signals running on bottom and having the VDDO plane as reference.
Place those components more at the DRAM side than the SoC side...
Place those components at the last DDR4 SDRAM
WSON10_210X210h080
ARTOSYN CONFIDENTIAL
Designed by Wuping Wang
Project Name Sirius EK V001
Rev 1.0.0
Date 2017.11.22
Size Custom
Page Title P08_DDR4-0
Dept: R&D, ARTOSYN
Sheet 8 of 27

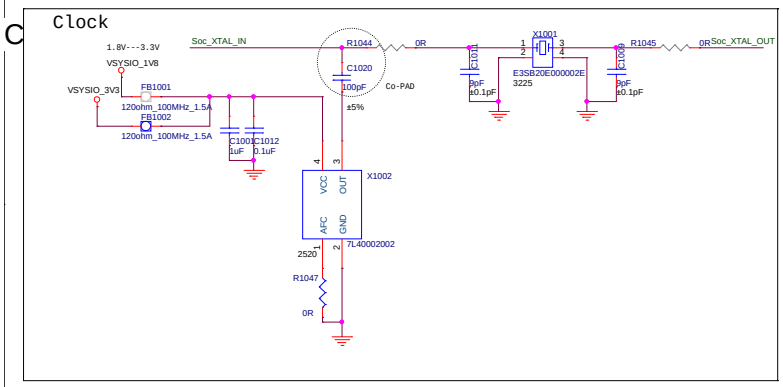



| | | |
|---|---|---|
| artosyn ARTOSYN CONFIDENTIAL | | |
| Designed by: Weiqing Wang | Project Name: Sirius BK V001 | Rev: 1.0.0 |
| Date: 2017.11.22 | Size: D | Page Title: P09_DDR4-1 |
| Check: R&D_ARTOSYN | | Sheet: C_9_1_of_C_39_1 |

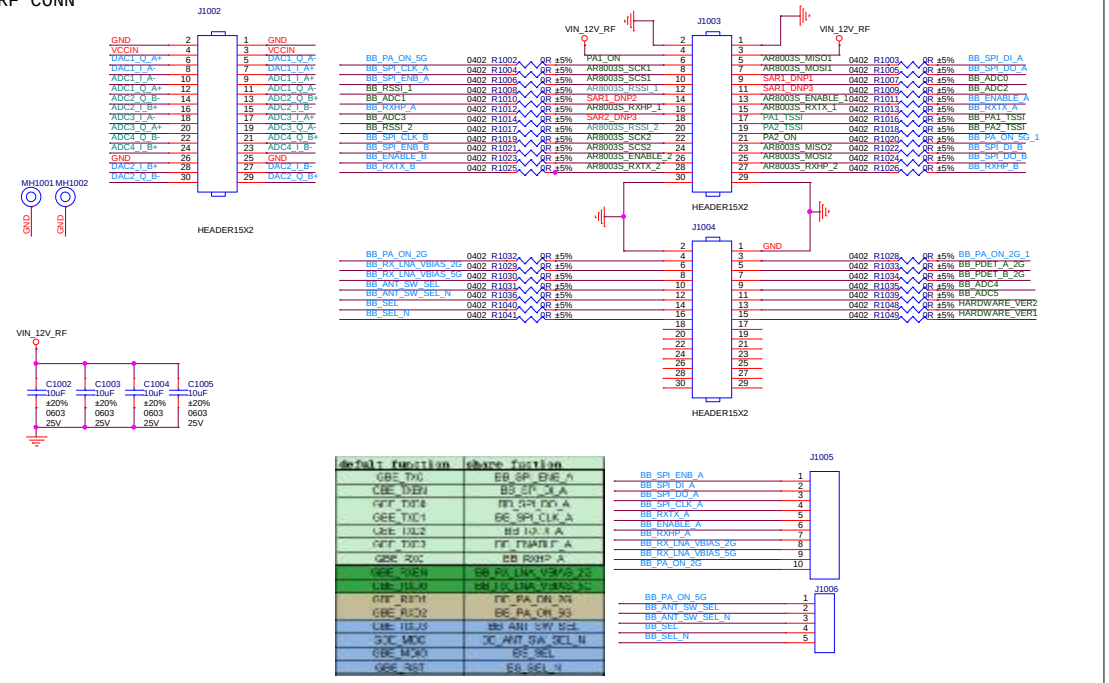
## Sirius:RF and CLK




## Clock

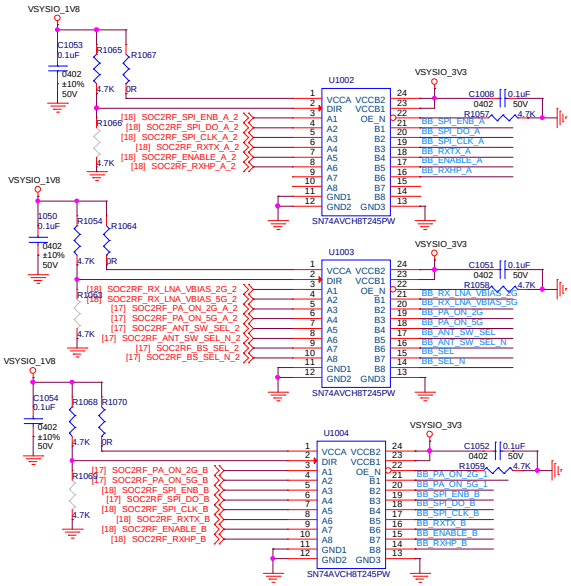



## RF CONN




| default function | share function |
|---|---|
| GBE_TXC | BB_SP_ENB_A |
| GBE_DEN | BB_SPI_DI_A |
| ANT_TXD0 | BB_SPI_DO_A |
| GBE_TXD1 | BB_SPI_CLK_A |
| GBE_TXD2 | BB_RXTX_A |
| ANT_TXD3 | BB_ENABLE_A |
| GBE_RXC | BB_RXHP_A |
| GBE_RXEN | BB_RX_LNA_VBIAS_2G |
| GBE_RXD0 | BB_RX_LNA_VBIAS_5G |
| ANT_RXD1 | BB_PA_ON_2G |
| GBE_RXD2 | BB_PA_ON_5G |
| GBE_RXD3 | BB_ANT_SW_SEL |
| GBE_MDC | BB_ANT_SW_SEL_N |
| GBE_MDIO | BB_SEL |
| GBE_RST | BB_SEL_N |



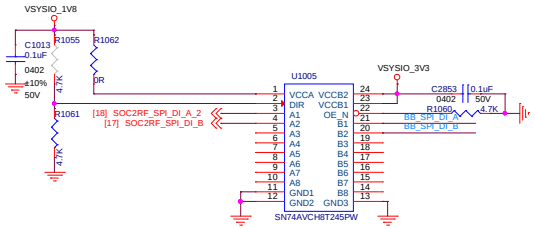



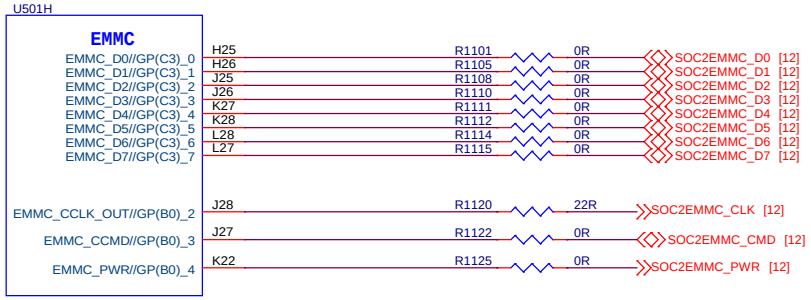

Table 1. Function Table (Each 8-Bit Section)

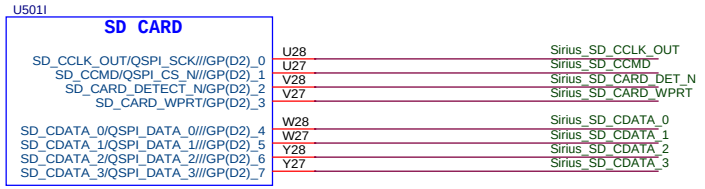
| Control Inputs | | Output Circuits | | |
|---|---|---|---|---|
| DIR | OE | A PORT | B PORT | Operation |
| L | L | Enabled | Hi-Z | Data A to B |
| L | H | Hi-Z | Enabled | Data B to A |
| X | X | Hi-Z | Hi-Z | Isolation |

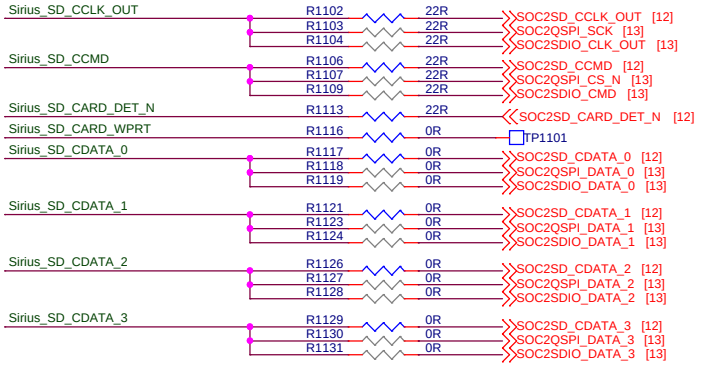


| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size C | Page Title P10_Sirius_CTL_RF |
| Dept: R&D ARTOSYN | | Sheet 10 of 27 |

# SOC EMMC & SD



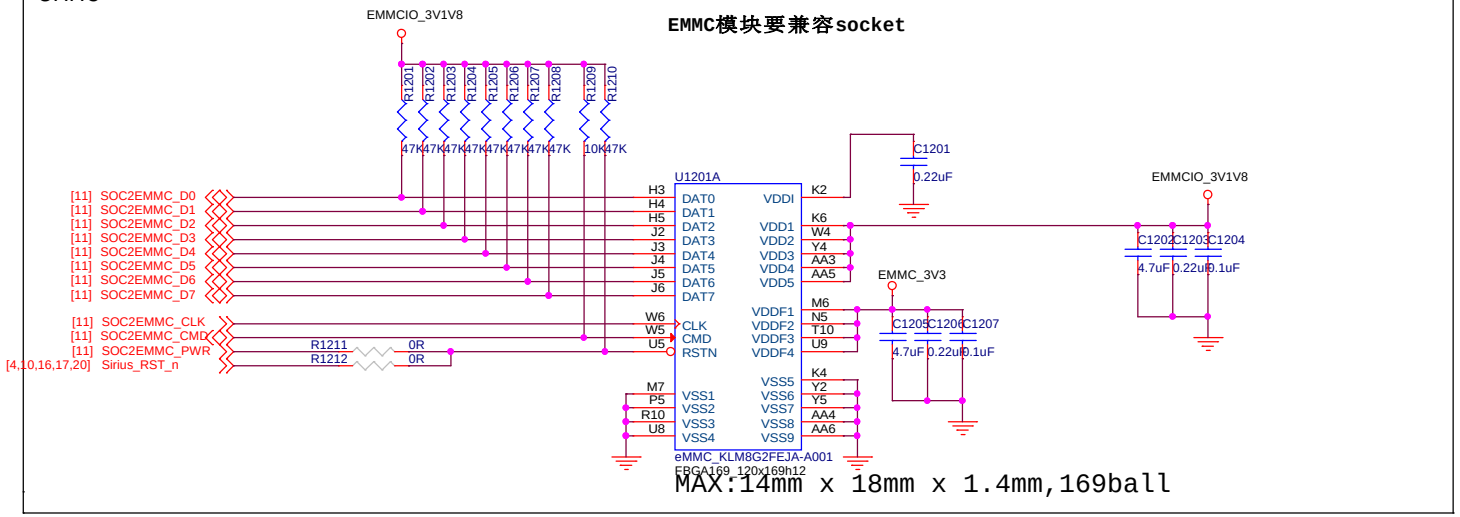




artosyn **ARTOSYN CONFIDENTIAL**

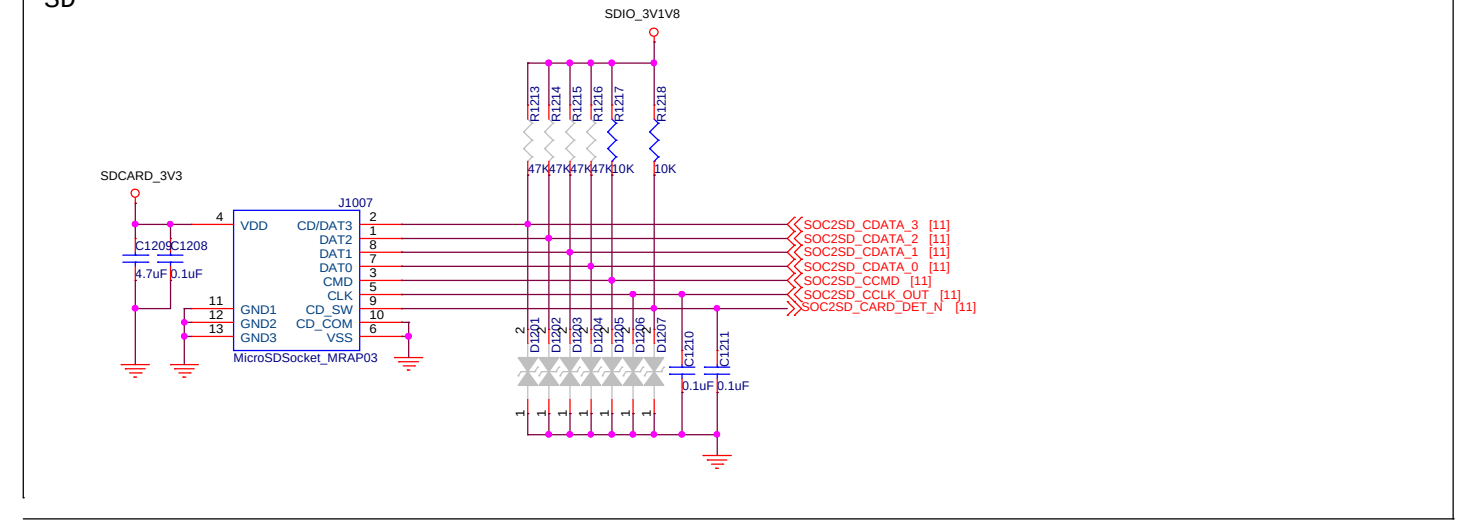
| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size B | Page Title P11_Sirius_Memory |
| Dept: R&D, ARTOSYN | | Sheet [ 11 ] of [ 27 ] |

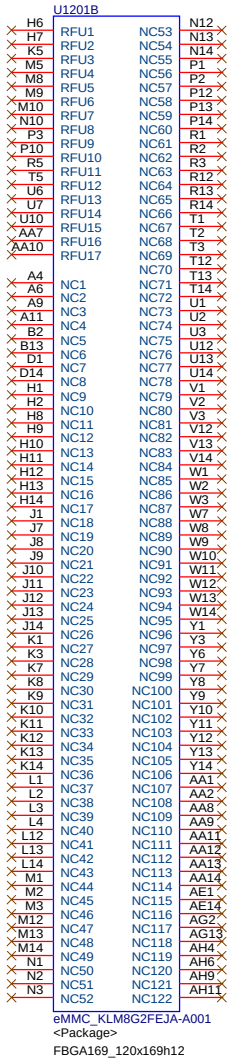
## eMMC




MAX:14mm x 18mm x 1.4mm,169ball

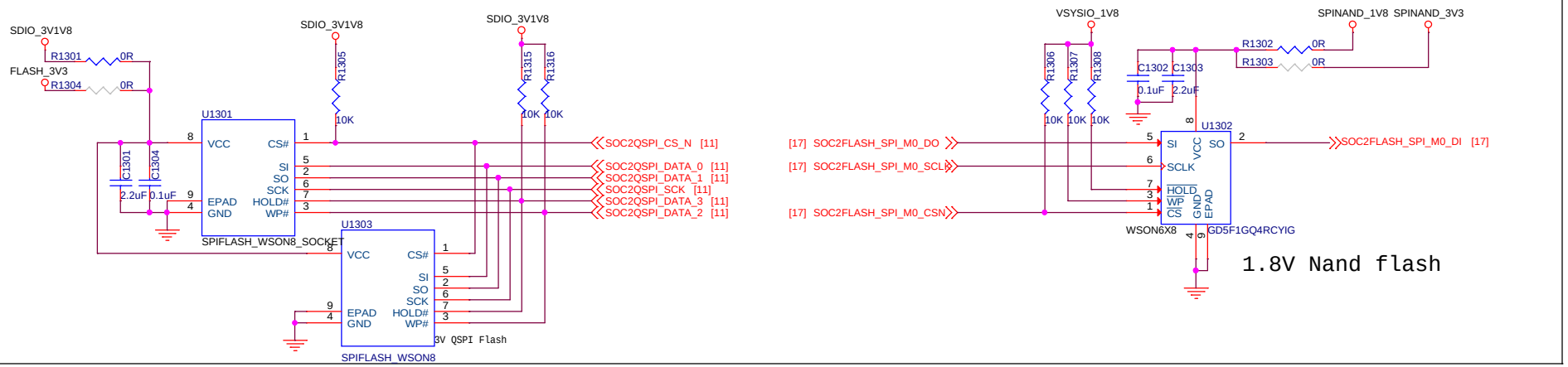
## SD



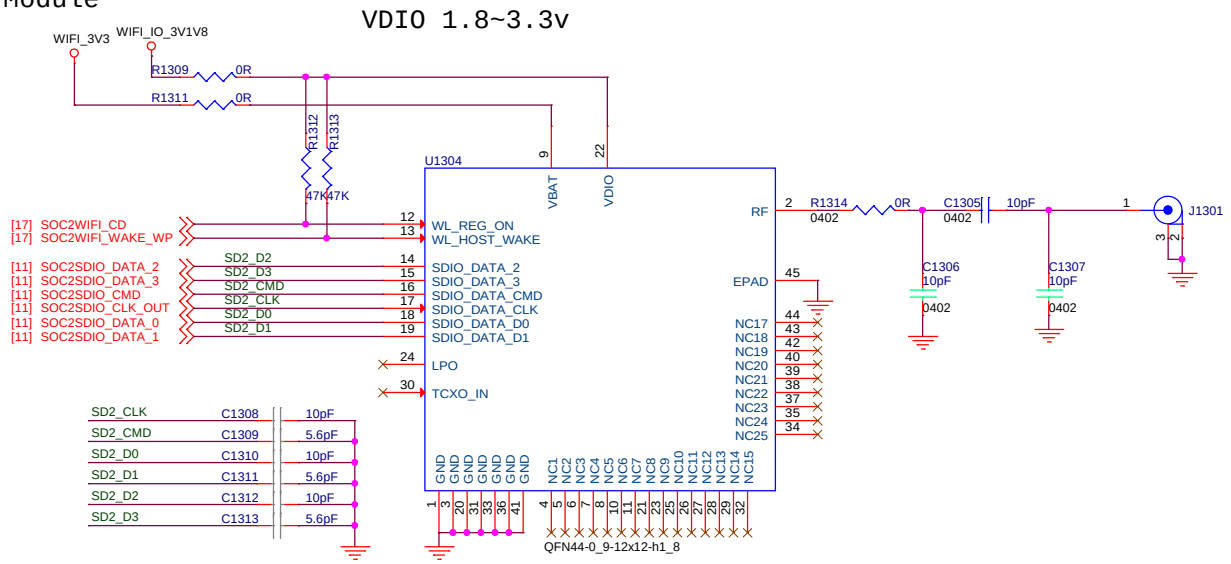




| | | |
|---|---|---|
| artosyn **ARTOSYN CONFIDENTIAL** | | |
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size B | Page Title P12_EMMC_SD |
| Dept: R&D, ARTOSYN | | Sheet 12 of 27 |

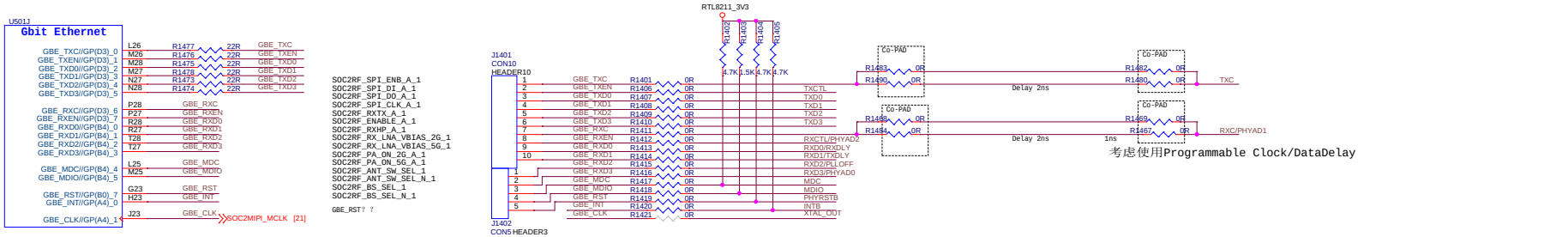
## QSPI & SPI Nand flash

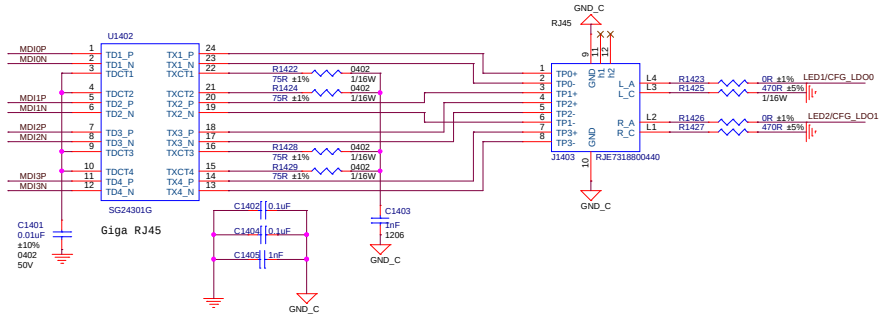



## SDIO WIFI Module




| | | |
|---|---|---|
| ARTOSYN CONFIDENTIAL | | |
| Designed by: Wuping Wang | Project Name: Sirius EK V001 | Rev: 1.0.0 |
| Date: 2017.11.22 | Size: B | Page Title: P13_FLASH_SDIO |
| Dept: R&D, ARTOSYN | | Sheet 13 of 27 |

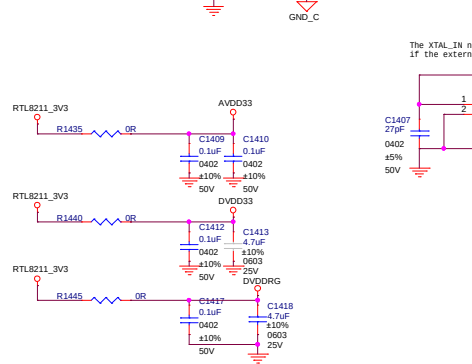


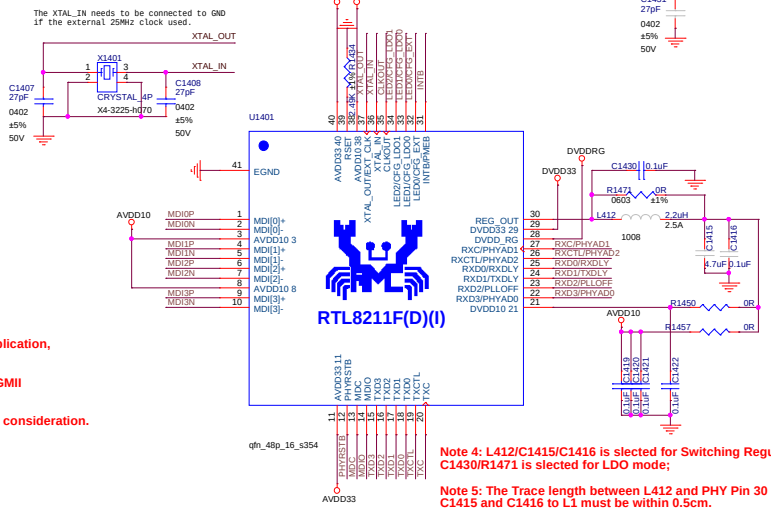



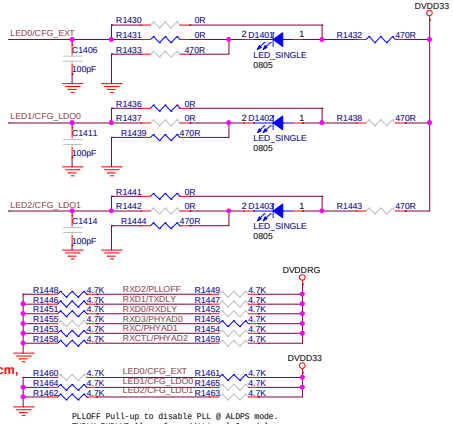

| PHY Address | PHYAD[2:0] |
|---|---|
| 0 | 3'b000 |
| 1 (default) | 3'b001 |
| 2 | 3'b010 |
| 3 | 3'b011 |
| 4 | 3'b100 |
| 5 | 3'b101 |
| 6 | 3'b110 |
| 7 | 3'b111 |

| RGMII Power Source | CFG_EXT | CFG_LDO[1:0] |
|---|---|---|
| External 3.3V (default) | 1'b1 | 2'b00 |
| External 2.5V | 1'b1 | 2'b01 |
| External 1.8V | 1'b1 | 2'b10 |
| External 1.5V | 1'b1 | 2'b11 |
| Internal 2.5V | 1'b0 | 2'b01 |
| Internal 1.8V | 1'b0 | 2'b10 |
| Internal 1.5V | 1'b0 | 2'b11 |

| | LED Resistances Setting |
|---|---|
| CFG_EXT=1'b1 | R1430(NC), R1431, R1432, R1433(NC) |
| CFG_EXT=1'b0 | R1430, R1431(NC), R1432(NC), R1433 |
| CFG_LDO0=1'b1 | R1434(NC), R1437, R1438, R1439(NC) |
| CFG_LDO0=1'b0 | R1434, R1437(NC), R1438(NC), R1439 |
| CFG_LDO1=1'b1 | R1441(NC), R1442, R1443, R1444(NC) |
| CFG_LDO1=1'b0 | R1441, R1442(NC), R1443(NC), R1444 |




**Note 1: R1440/R1445 is not needed for ONLY 3.3V RGMII application, and DVDDRG can be connected directly to DVDD33.**

**Note 2: DVDDRG must be short to DVDD33 if the external RGMII 3.3V is selected.**

**Note 3: CAPs(C1417/C1448) must be closed to pin28 for EMI consideration.**

**Note 4: L412/C1415/C1416 is slected for Switching Regulator mode; C1430/R1471 is slected for LDO mode;**

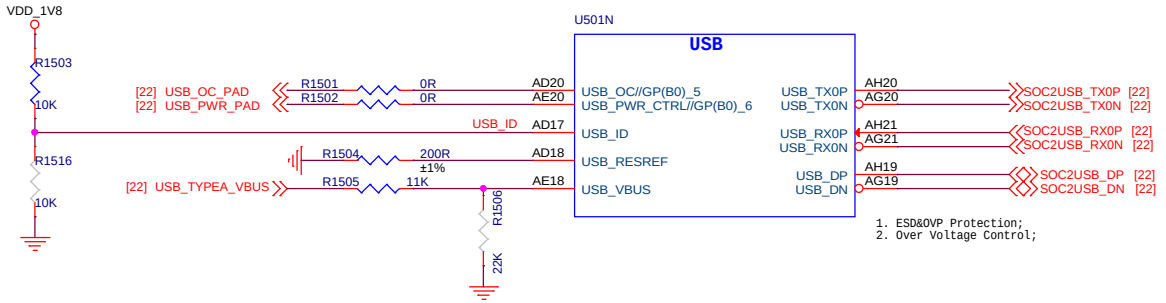
**Note 5: The Trace length between L412 and PHY Pin 30 must be within 0.5 cm, C1415 and C1416 to L1 must be within 0.5cm.**

**Note 6: Any inductance or bead except L1 is not allowed on the path from REGOUT to DVDD10/AVDD10.**

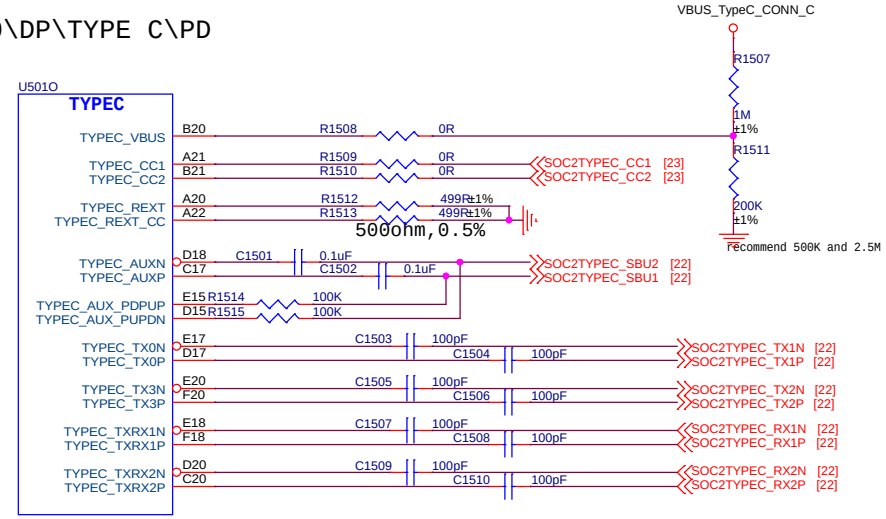


| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name: Sirius EK V001 | Rev: 1.0.0 |
| Date: 2017.11.22 | Size: C | Page Title: P14_Sirius_RGMII |
| Dept: R&D, ARTOSYN | Sheet 14 of 27 | |

## SOC:USB3.0 AND USB2.0



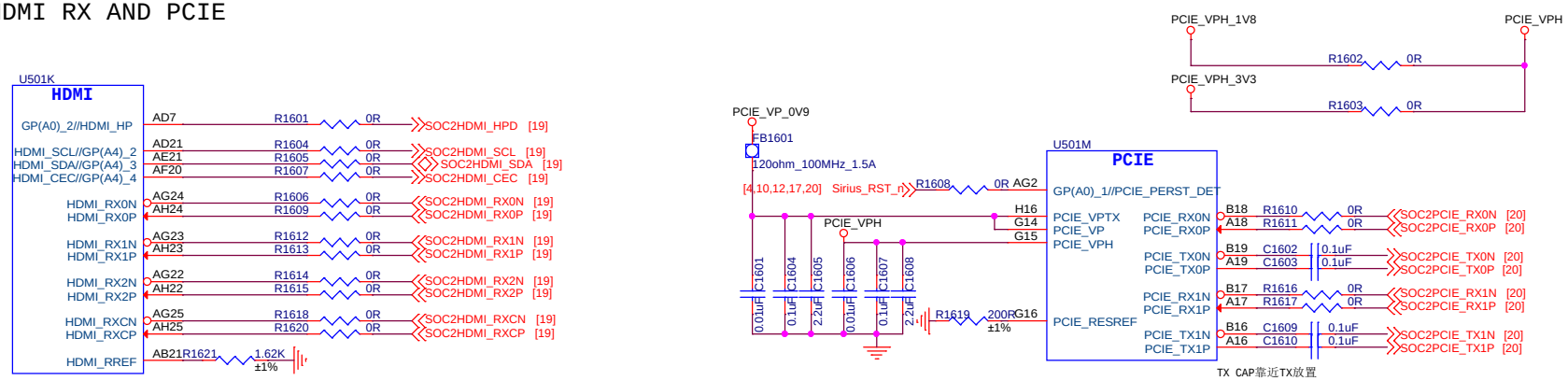

## SOC:USB3.0\DP\TYPE C\PD



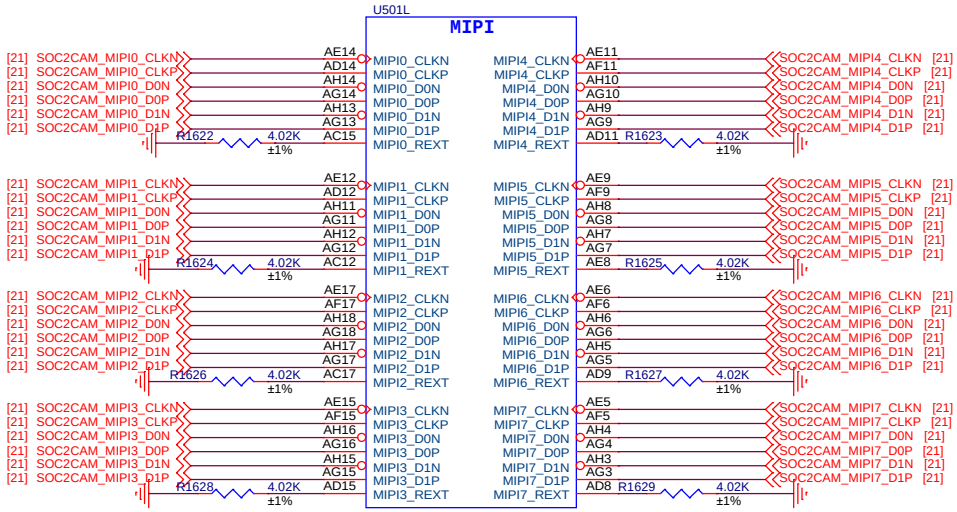

artosyn **ARTOSYN CONFIDENTIAL**

| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size B | Page Title P15_Sirius_Highspeed_1 |
| Dept: R&D, ARTOSYN | | Sheet [ 15 ] of [ 27 ] |

## SOC:HDMI RX AND PCIE



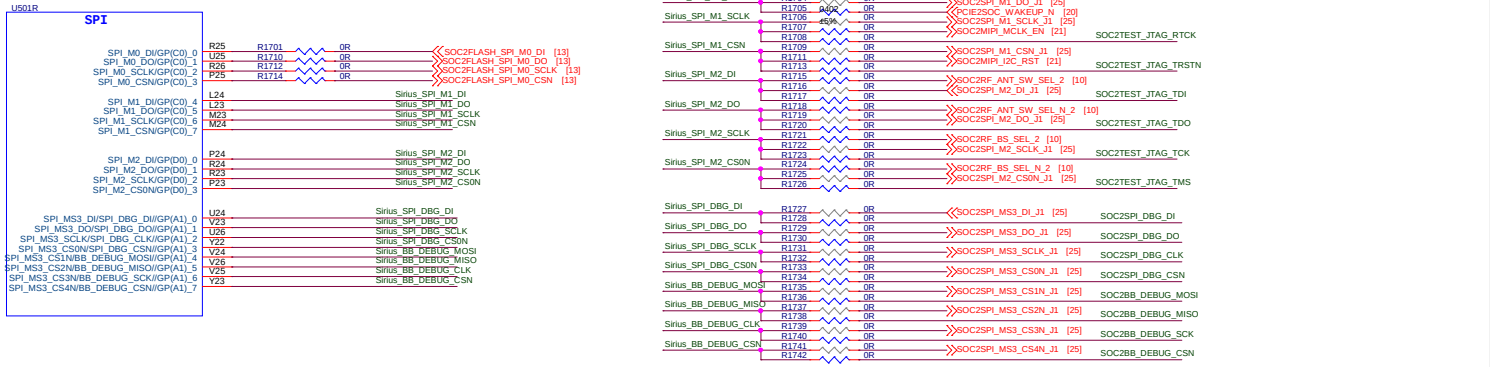

## SOC:MIPI CSI RX*8 AND TX*2



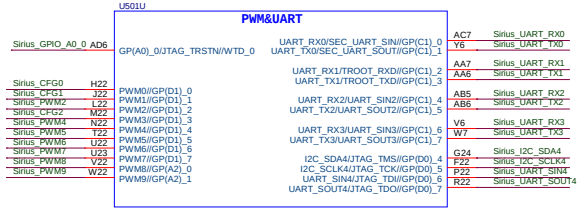

ARTOSYN CONFIDENTIAL

| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size B | Page Title P16_Sirius_Highspeed_2 |
| Dept: R&D, ARTOSYN | | Sheet 16 of 27 |

## SOC SPI

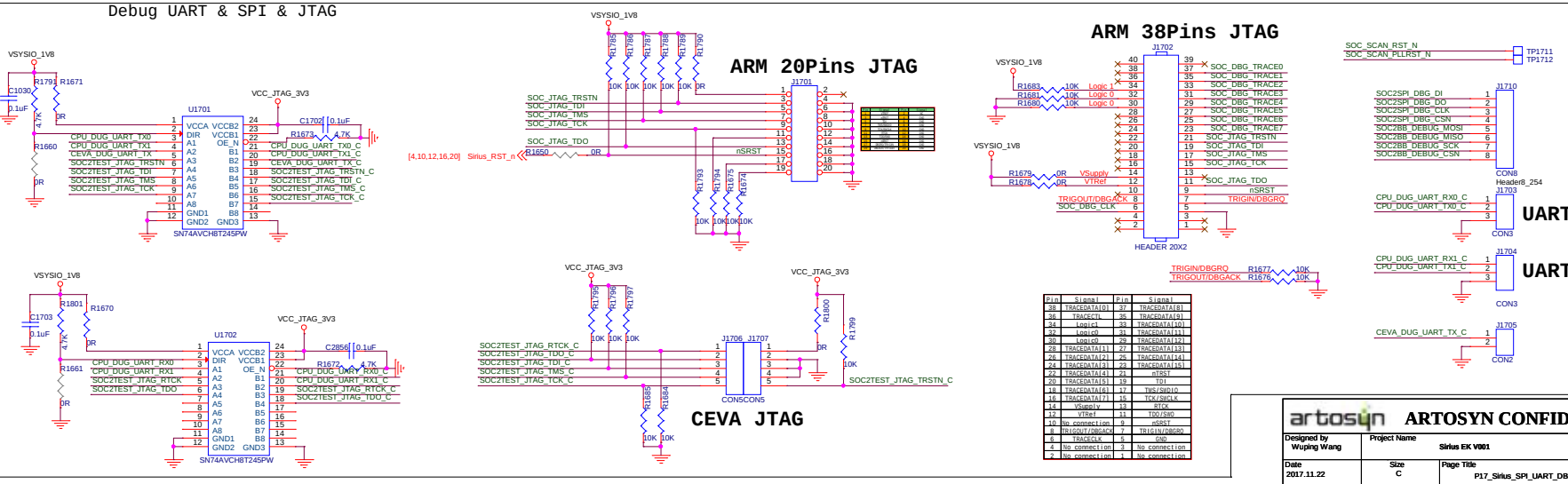



## UART&CFG




1.8v digital IO


## Debug UART & SPI & JTAG




| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 38 | TRACEDATA[0] | 37 | TRACEDATA[8] |
| 36 | TRACECTL | 35 | TRACEDATA[9] |
| 34 | Logic1 | 33 | TRACEDATA[10] |
| 32 | Logic0 | 31 | TRACEDATA[11] |
| 30 | Logic0 | 29 | TRACEDATA[12] |
| 28 | TRACEDATA[1] | 27 | TRACEDATA[13] |
| 26 | TRACEDATA[2] | 25 | TRACEDATA[14] |
| 24 | TRACEDATA[3] | 23 | TRACEDATA[15] |
| 22 | TRACEDATA[4] | 21 | nTRST |
| 20 | TRACEDATA[5] | 19 | TDI |
| 18 | TRACEDATA[6] | 17 | TMS/SWDIO |
| 16 | TRACEDATA[7] | 15 | TCK/SWCLK |
| 14 | VSupply | 13 | RTCK |
| 12 | VTRef | 11 | TDO/SWO |
| 10 | No connection | 9 | nSRST |
| 8 | TRIGOUT/DBGACK | 7 | TRIGIN/DBGRQ |
| 6 | TRACECLK | 5 | GND |
| 4 | No connection | 3 | No connection |
| 2 | No connection | 1 | No connection |

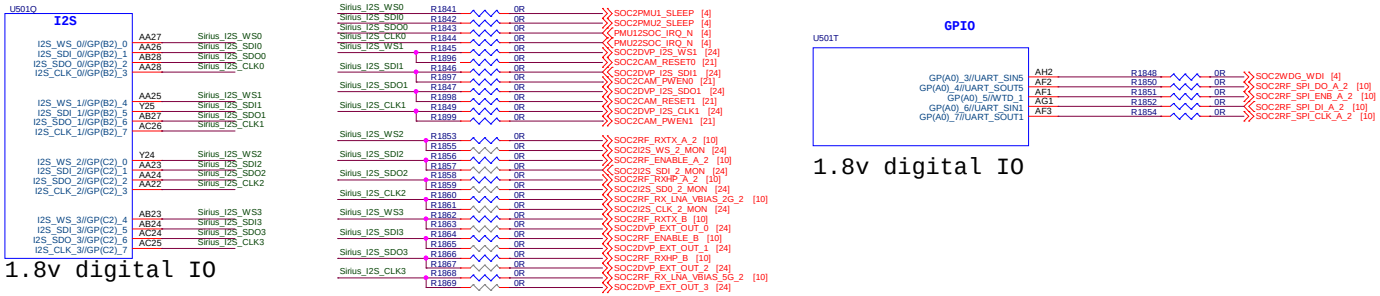
artosyn **ARTOSYN CONFIDENTIAL**

| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name: Sirius EK V001 | Rev: 1.0.0 |
| Date: 2017.11.22 | Size: C | Page Title: P17_Sirius_SPI_UART_DBG |
| Dept: R&D, ARTOSYN | | Sheet 17 of 27 |

## Sirius DVP


DVP 0和MON OUT复用接口
DVP 1和MON OUT复用接口
DVP 0和TYPE C 兼容设计

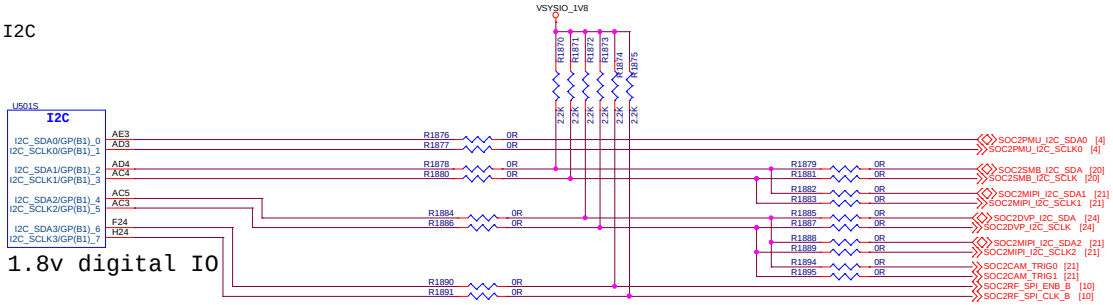
## Sirius I2S&GPIO




1.8v digital IO

1.8v digital IO

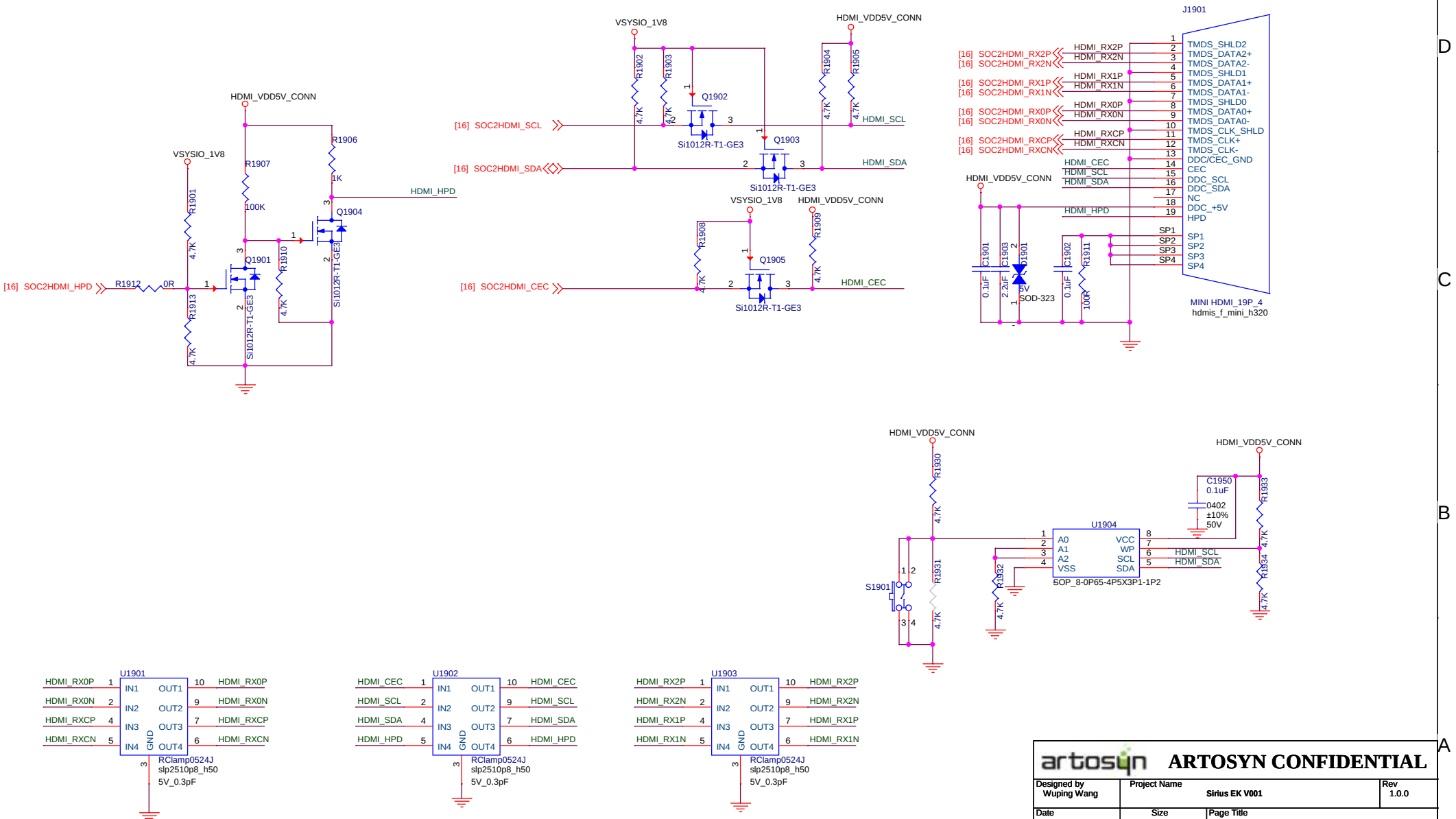
## Sirius I2C




1.8v digital IO

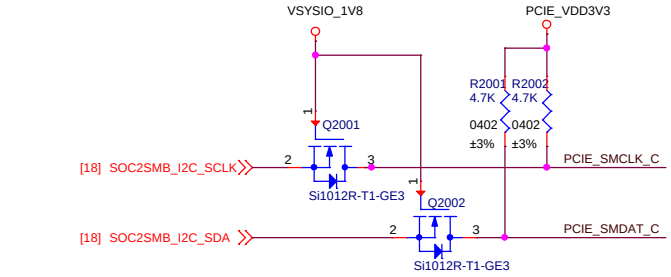
ARTOSYN CONFIDENTIAL

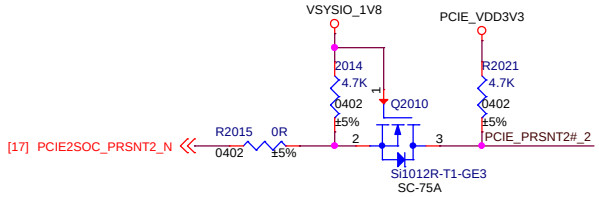
| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size C | Page Title P18_Sirius_DVP_I2S_I2C |
| Dept: R&D ARTOSYN | | Sheet 18 of 27 |

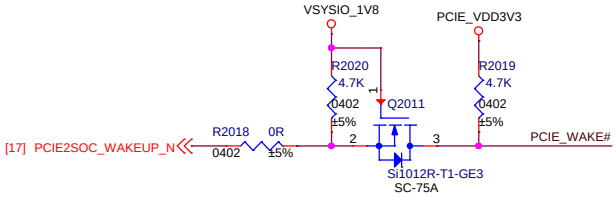


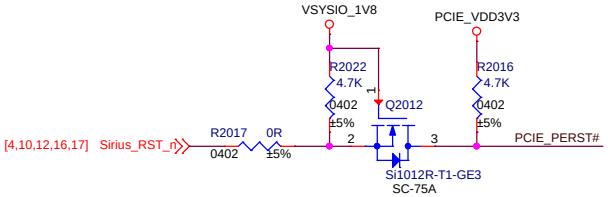

ARTOSYN CONFIDENTIAL

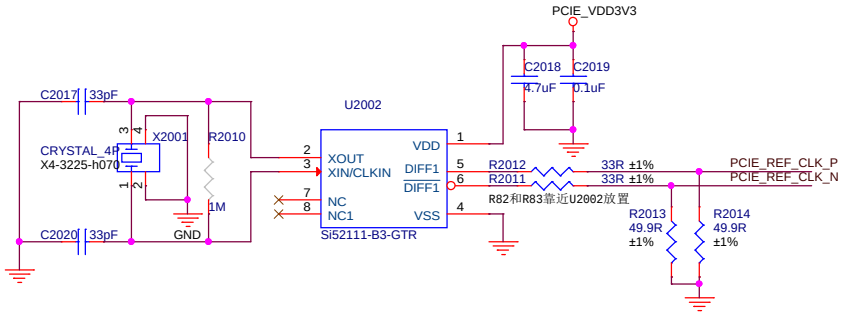
| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size B | Page Title P19_CONN_HDMI |
| Dept: R&D, ARTOSYN | | Sheet 19 of 27 |

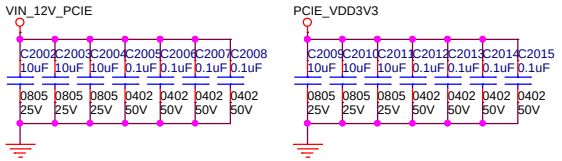


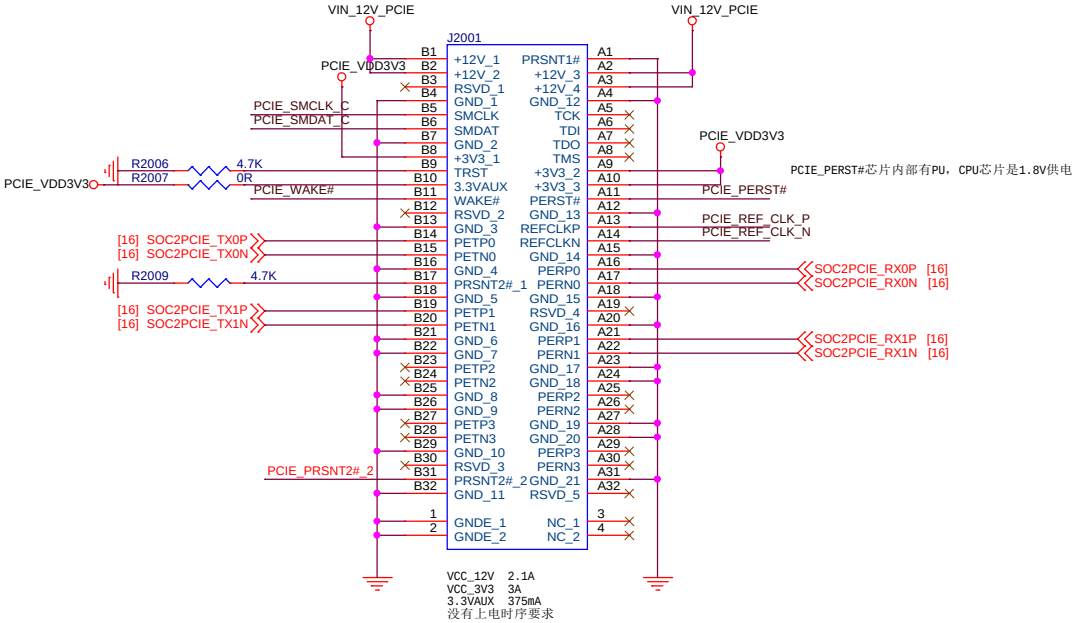







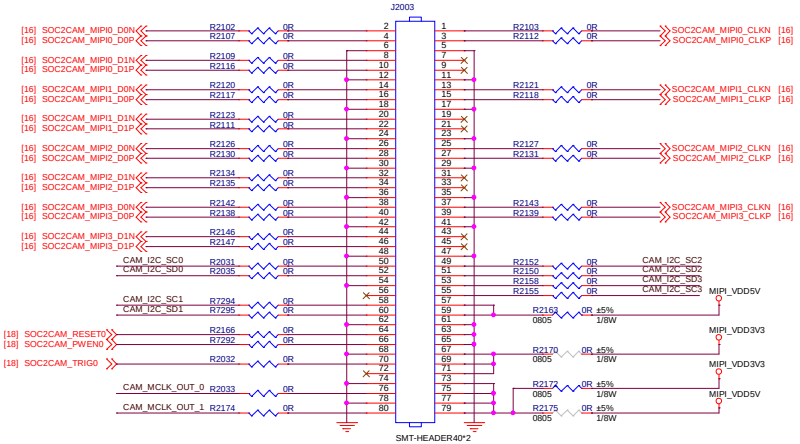


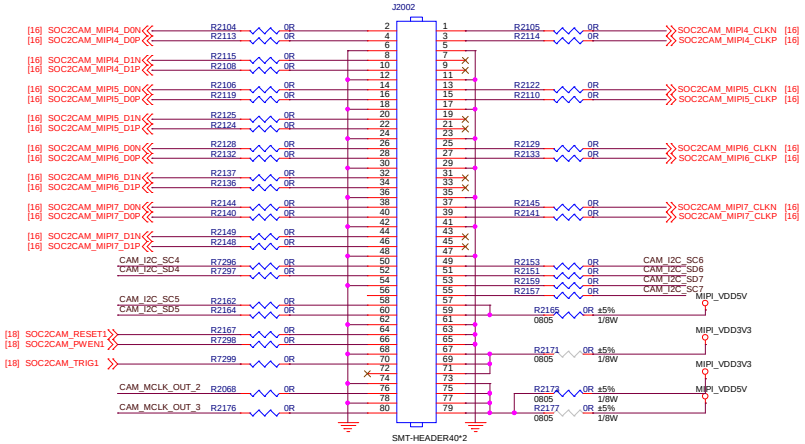

PCIE接口保护？

artosyn **ARTOSYN CONFIDENTIAL**

| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size B | Page Title P20_CONN_PCIE |
| Dept: R&D, ARTOSYN | | Sheet 20 of 27 |

## Sensor Connecter

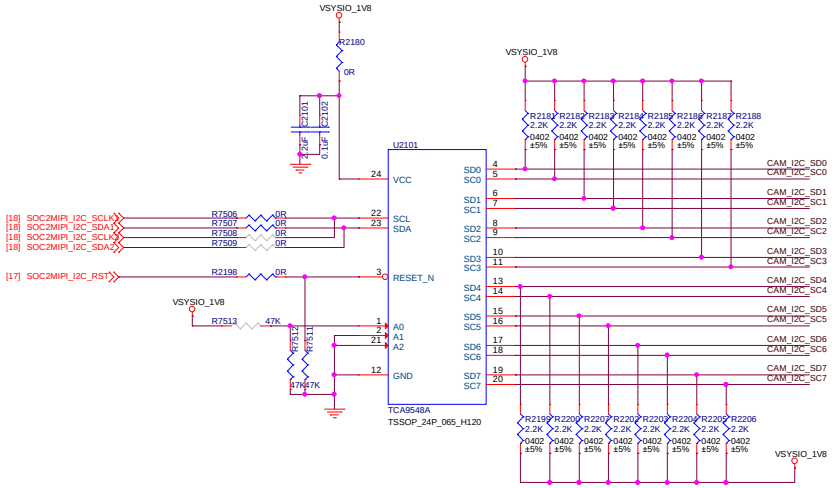


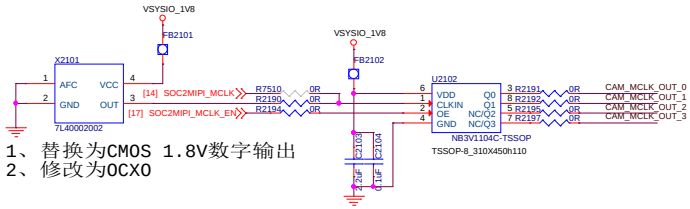

接口定义

4Lane 时使用为pin13/15，pin37/39
需要重新做种验证？
同一个sensor要其使用
同一个clk到sensor

## Sensor I2C Switch




## Sensor MLCK router

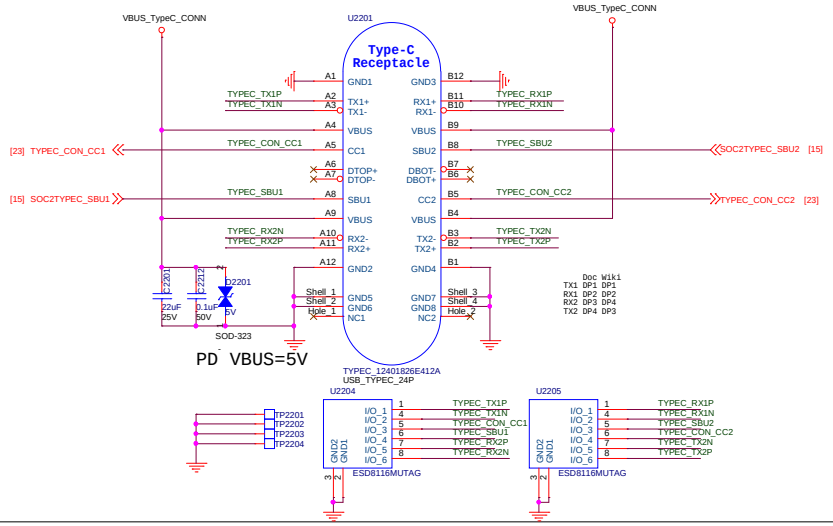


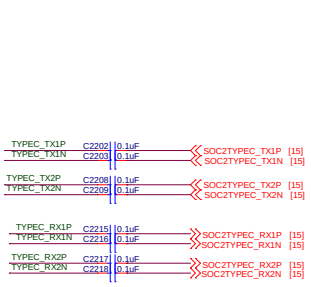

1、替换为CMOS 1.8V数字输出
2、修改为OCXO



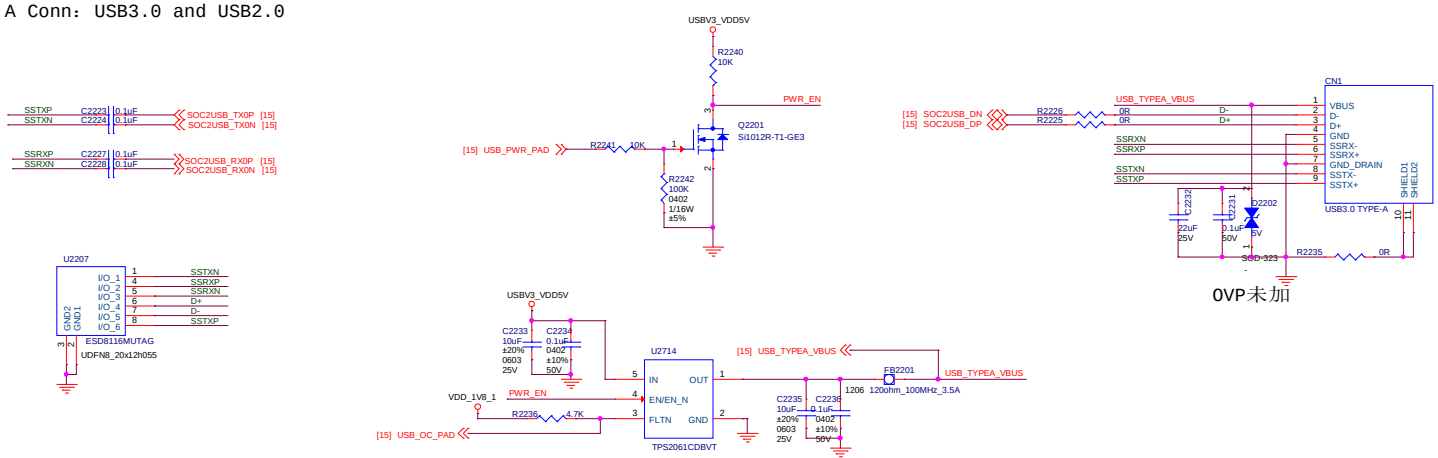
| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size C | Page Title P21_CONN_MIPI |
| Dept: R&D ARTOSYN | | Sheet 21 of 27 |

## TYPE C Conn：USB3.0、DP and PD



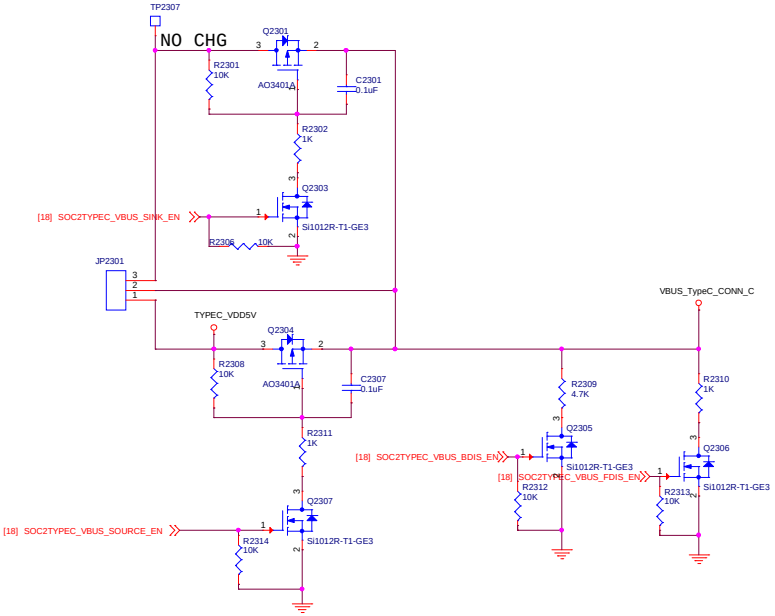

## TYPE A Conn：USB3.0 and USB2.0



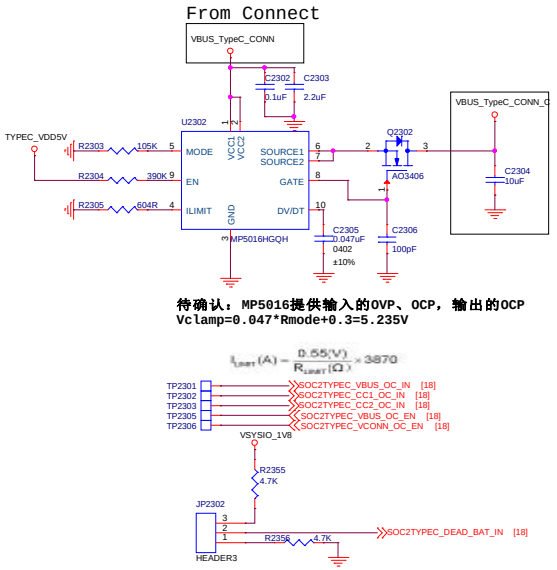



| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size C | Page Title P22_CONN_USB_TYPEC |
| Dept: R&D ARTOSYN | | Sheet 22 of 27 |

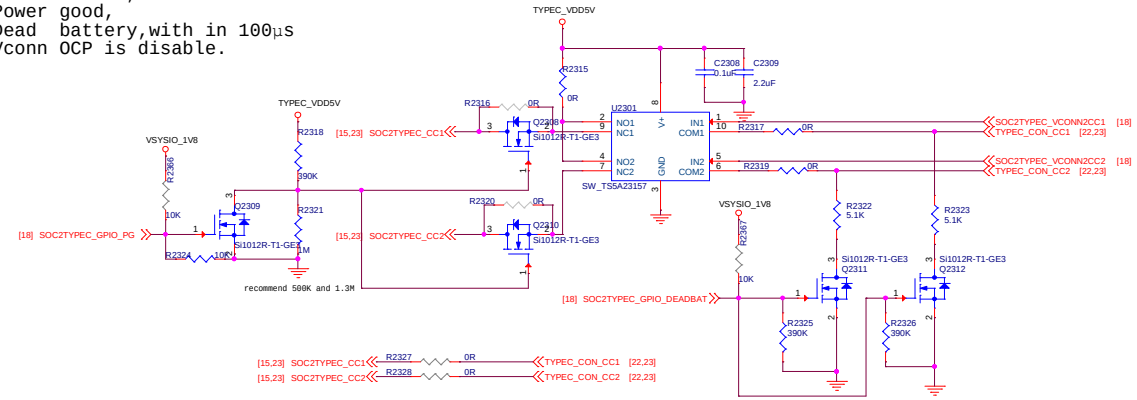
PD Feature option:
1)Discharge,2)Sink/chg and source router




PD Feature option:
1)Input OVP,2)VBUS Input/Output OCP

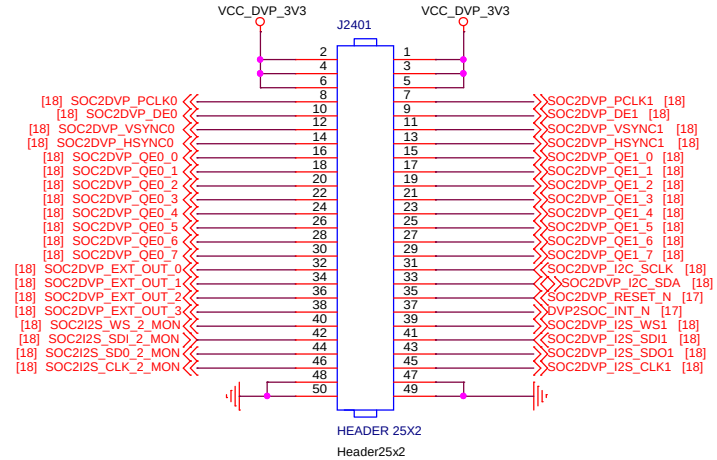



Type C cc Feature and PD Feature option:
1)Active cable,
2)Power good,
3)Dead battery,with in 100μs
4)Vconn OCP is disable.

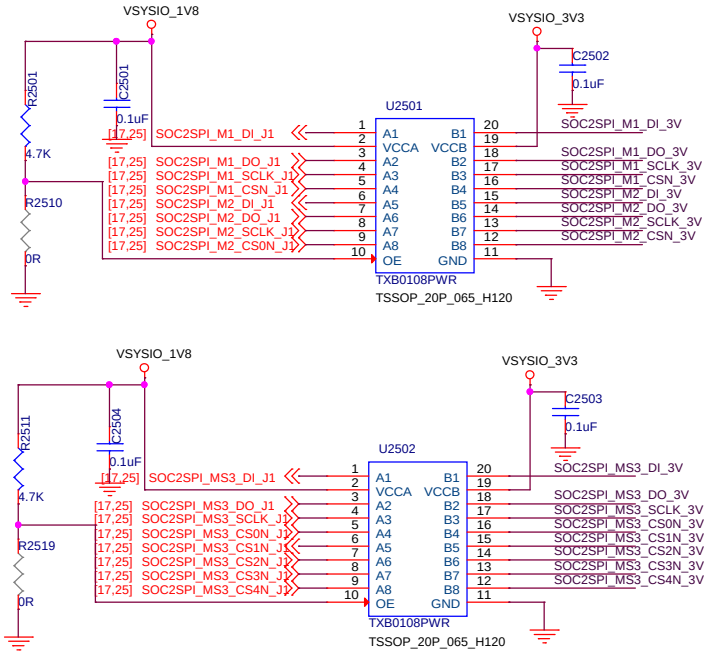





| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size C | Page Title P23_CONN_USB_PD |
| Dept: R&D ARTOSYN | | Sheet 23 of 27 |

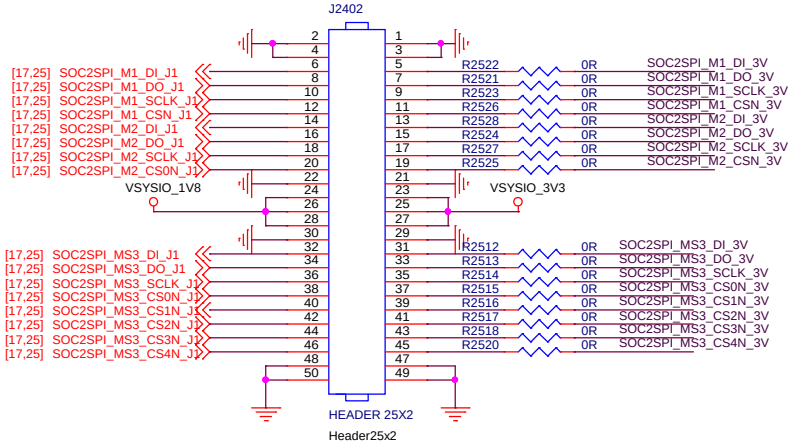



| | | |
|---|---|---|
| artosyn **ARTOSYN CONFIDENTIAL** | | |
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size B | Page Title P24_CONN_DVP |
| Dept: R&D, ARTOSYN | | Sheet [ 24 ] of [ 27 ] |



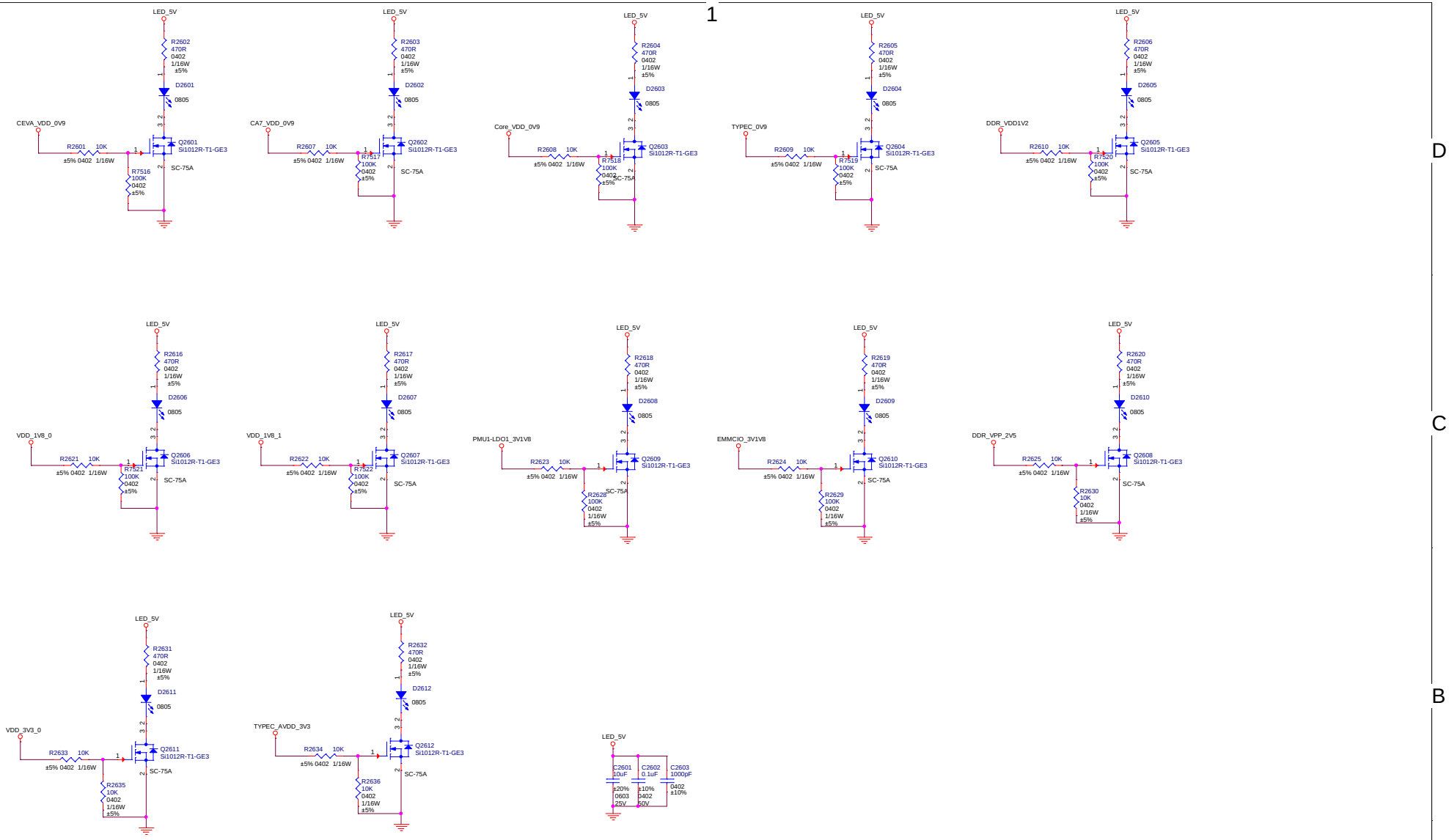







ARTOSYN CONFIDENTIAL

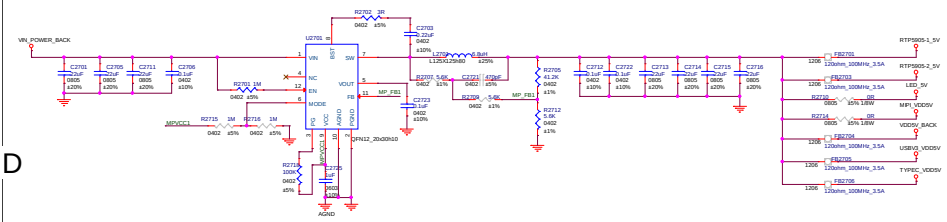
| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size B | Page Title P25_CONN_Other |
| Dept: R&D, ARTOSYN | | Sheet 25 of 27 |



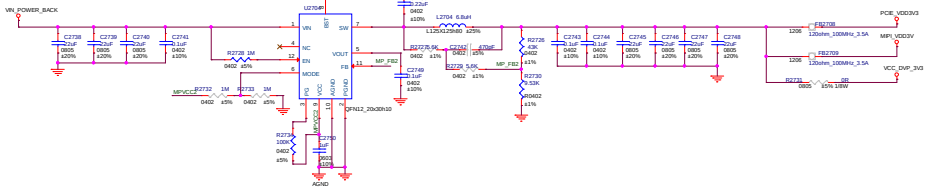

ARTOSYN CONFIDENTIAL

| | | |
|---|---|---|
| Designed by Wuping Wang | Project Name Sirius EK V001 | Rev 1.0.0 |
| Date 2017.11.22 | Size C | Page Title P26_LED |
| Dept: R&D_ARTOSYN | Sheet 26 of 27 | |

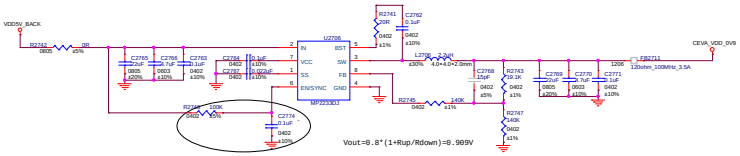
## 5V POWER BACKUP



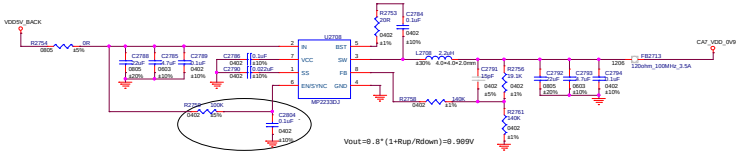

## 3.3V POWER BACKUP



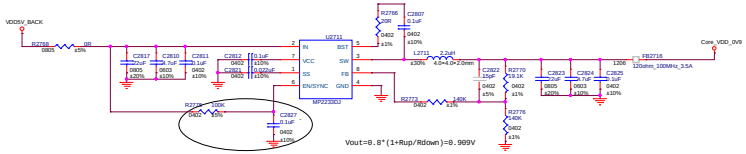

## 0.9V FOR CEVA POWER BACKUP



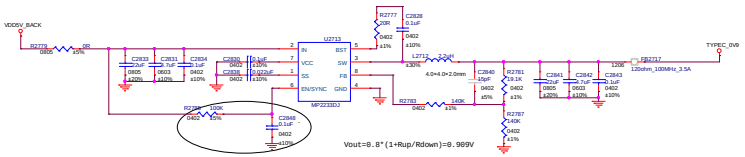

## 0.9V FOR CA7 POWER BACKUP



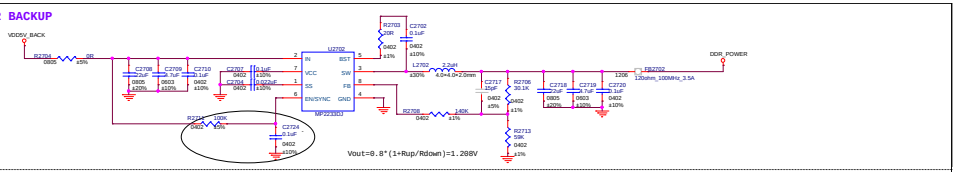

## 0.9V FOR CORE POWER BACKUP



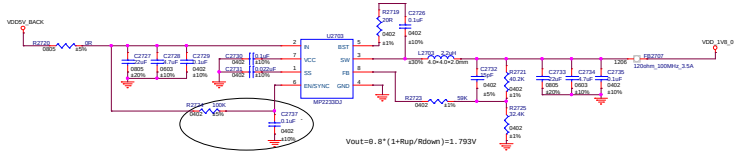

## 0.9V FOR TYPEC POWER BACKUP



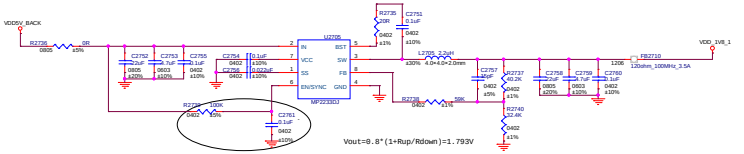

## 1.2V FOR DDR4 POWER BACKUP



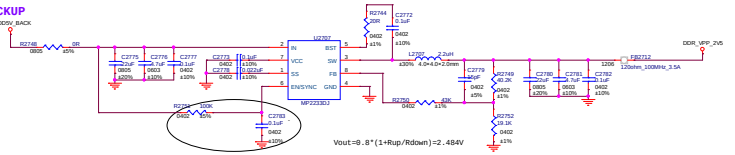

## 1.8V POWER BACKUP1



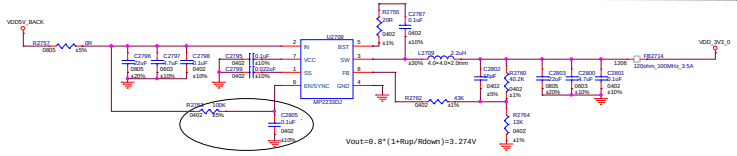

## 1.8V POWER BACKUP2



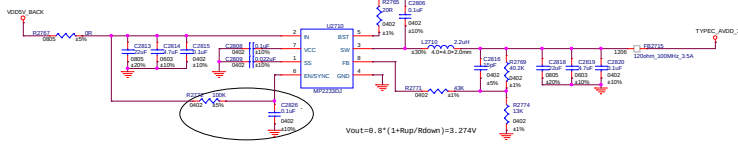

## 2.5V FOR DDR4 POWER BACKUP



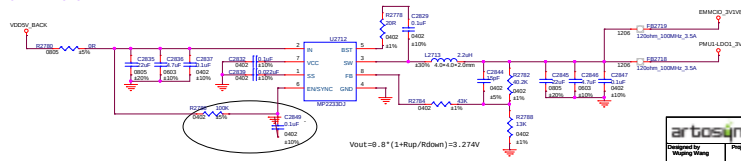

## 3.3V POWER BACKUP




## 3.3V FOR TYPEC POWER BACKUP




## 3.3V FOR SDIO/EMMCIO POWER BACKUP






| | | |
|---|---|---|
| Designed by: Yuqing Wang | Project Name: Sirius EK V00 | Rev: 1.0.0 |
| Date: 2017.11.22 | Size: D | Page Title: P27_PowerBackup |
| Check: R&D_ARTOSYN | | Sheet: 27 of 27 |