SYNOPSYS®

# DesignWare Cores DDRn Power Integrity and Supply Impedance Determination for DDR Interfaces

**Application Note**

**DWC DDRn Signal Integrity Application Note**

Version 1.0
January 2017

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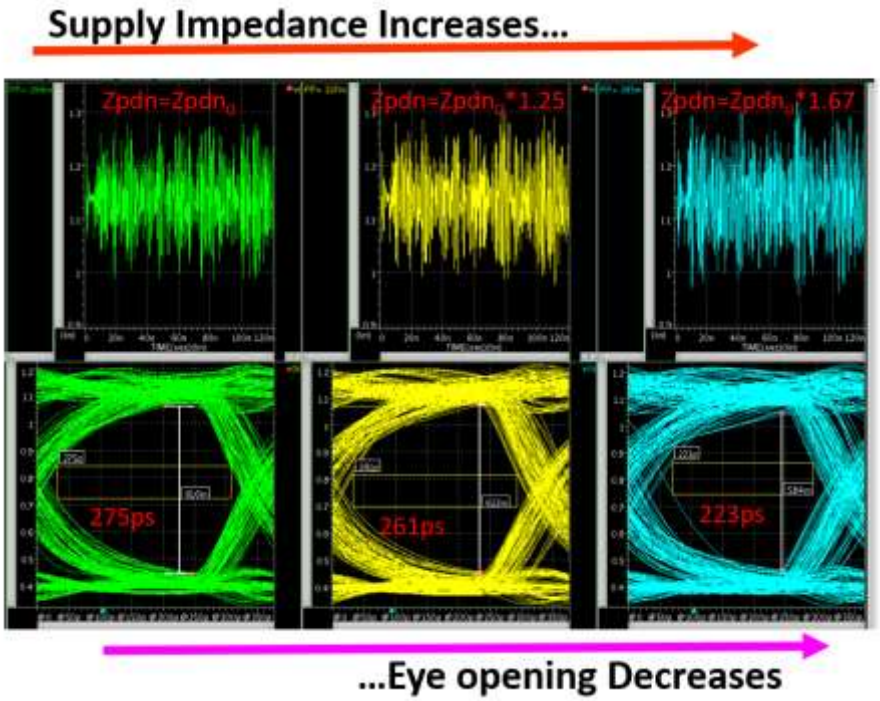
# Revision History

| Doc. Revision | Date | Description |
|---|---|---|
| 1.0 | January 2017 | Initial release |

# 1 The Scope of Power Integrity

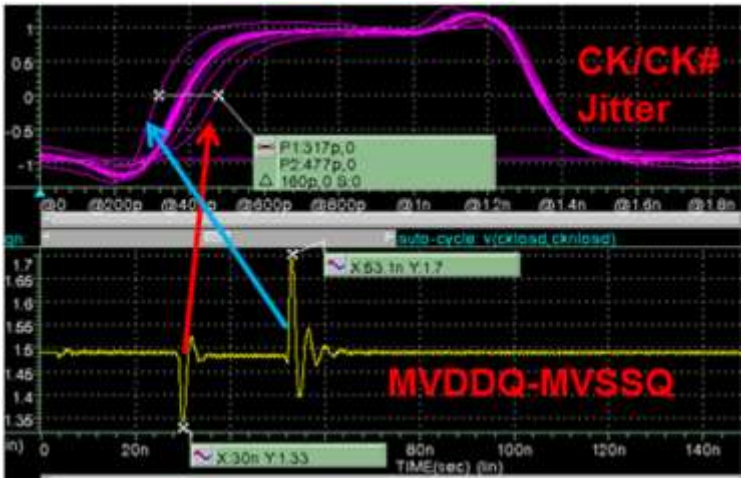
Power integrity as a topic covers the ability of a particular system to maintain its voltage rail as close to ideal DC as possible. Failing that, power integrity is about evaluating the timing impact of any divergence from the ideal voltage level. Figure 1 illustrates how the eye opening at a given bit rate will close as the supply impedance increases. Higher supply impedance means the drawn current will result in more power rail voltage noise. The increased voltage noise will yield increased Power Supply Induced Jitter, PSIJ, that will lead to greater deterioration of the eye opening.

Figure 1:For a given bit rate, as supply impedance increases, the size of the eye opening decreases.




Transient variations from the nominal supply voltage will cause signal edges to be delayed with decreases in voltage and arrive early with increases in voltage (Figure 2). This leads to jitter as shown in the figure. Jitter will erode the timing of the memory interface. Jitter related to variations in the supply voltage is described as Power Supply Induced Jitter (PSIJ).

**Figure 2: Transient changes in supply voltage lead to clock jitter.**

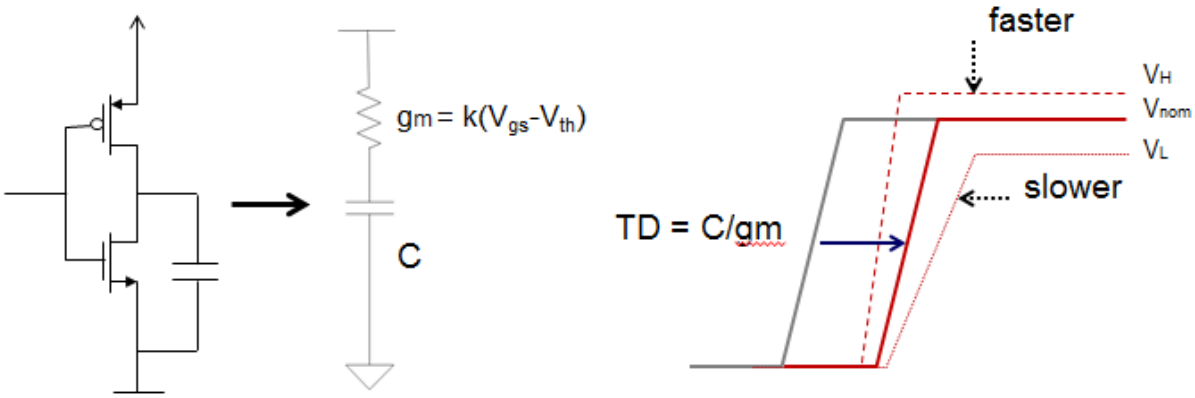



From basic circuit analysis, the total delay of a transistor is given by:

$$delay = RC = \frac{C}{gm} \propto 1/(Vgs - Vth)$$

Therefore, higher the supply voltage shorter the delay and vice versa. The figure below illustrates this with the help of an equivalent circuit of an inverter.

Figure 3: Generating power supply induced jitter in transistors.




To minimize PSIJ, the supply impedance must be kept low to reduce the change in voltage associated with the transient current. Table 1 is a list of memory interface variables that must be considered when determining supply impedance requirements. Starting from a baseline system with power supply induced jitter, of +/- *N* ps, the table lists the relative change in a particular interface parameter and the change in supply impedance needed to maintain the PSIJ performance at the same level as the baseline system. Note that Anything that increases currents will require a lower supply impedance. Anything that increases jitter sensitivity will also require a lower supply impedance.

**Table 1:Parameters that influence supply impedance requirements.**

| Interface Parameter Impact on Supply Impedance (Zpdn) Requirements | | | |
|---|---|---|---|
| **Parameter Name** | **Relative Change in Parameter** | **Change in Zpdn to Maintain Jitter Performance** | **Comments** |
| Bit Rate | Increase | Decreases | Tighter jitter specs |
| DC Voltage | Increase | Increases | Lower PSIJ sensitivity outweighs greater current |
| Interface Width | Increase | Decreases | Greater current. A 72 bit interface will require a proportionally lower Zpdn than a 32 bit interface. |
| ODT at Target Device | Increase | Decreases | Higher ODT will result in larger signal swing and higher switching currents. |
| Zsource | Increase | Increases | Higher Source Impedance will generate a lower signal swing with lower switching currents. |
| Host Silicon Process | Slower | Decreases | Greater PSIJ sensitivity in slower process. |
| Capacitive Load | increase | Decreases | Greater current draw |
| Slew Rate | Increase | Decreases | Faster current draw. |

## 1.1 Voltage Domains for DDR PHY

There are typically five voltage domains in a DDR interface.

1. **VDDQ** – This is the IO domain that connect to the system side PAD of the PHY. The nominal voltage will match the nominal voltage of the memory protocol being implemented; 1.2V for DDR4, 1.5V for DDR3, etc. This power may be shared on the board with the memory device. The AC ripple specification for this rail is +/-5% (2.5% for LPDDR4 applications) with the minimum level being maintained above the minimum DC specification.
2. **VDD** – This is the core power domain. For the DDR PHY, this will power the core side of the IO structure, the macro blocks, the PHY Utility Block (PUB), controller and the core domain portion of the PLL. This voltage will be determined by the process in which the IP is ported. VDD is often shared with the rest of the SOC. If that is the case, the power integrity analysis must account for the current needs of the rest of the SOC. The AC ripple specification for this rail is +/-2.5% (2.0% for LPDDR4 applications) with the minimum level being maintained above the minimum DC specification.
3. **VDD_PLL** – This is the 1.8V supply that is used to power the PLL. For the DDR4 MultiPHY and the Gen2 MultiPHY, this rail will also power receiver circuitry. If this supply is shared elsewhere on the board the DDR portion should be isolated with a ferrite bead. The AC ripple specification for this rail is +/-2.5% with the minimum level being maintained above the minimum DC specification.
4. **VREF** – This is a level that is delivered to the IOs to capture the appropriate signal levels. This should be placed at the mid-point of the signal swing. For DDR3/3L, this will be at 50% of the VDDQ level. For interfaces that are pull-up or pull-down terminated, this will be trained to the optimum level by the PHY. It is recommended that VREF be internally generated.
5. **VTT** – This is the termination voltage used for Command/Address signals that do not have on die termination. This voltage is 50% of the VDDQ voltage and applies to Command/Address interfaces of DDR2, DDR3(L), DDR4 and LPDDR3-board mounted.

# 2 Power Integrity & Determining Supply Impedance

Proper control of the supply impedance on all power rails is critical to maintaining the power supply induced jitter (PSIJ) within a specified level to ensure that a particular interface will meet required period jitter specifications as well as eye opening targets.

The supply impedance of a power delivery network, $Z_{PDN}$, is determined by the maximum tolerable peak voltage ripple, $V_{Rip}$, divided by the current being drawn during a switching event, $I_{Sw}$.

$$Z_{PDN} = \frac{V_{Rip}}{I_{Sw}}$$

Power integrity analysis involves defining and controlling each of the three parameters in the above equation. This note will begin with an example supply impedance calculation for the VDDQ IO rail. This is a jumping off point to discuss the various facets of determining a controlling rail noise, switching current and supply impedance. This example covers the VDDQ supply. $V_{Rip}$, $I_{Sw}$ and $Z_{PDN}$ issues pertaining to core, VDD, VAA_PLL, Vref and Vtt will also be discussed. Following this example, the note will elaborate on:

1. Components of the power delivery network that determine the supply impedance.
2. Current profiles of the interface.
3. Requirements of each of the voltage domains.

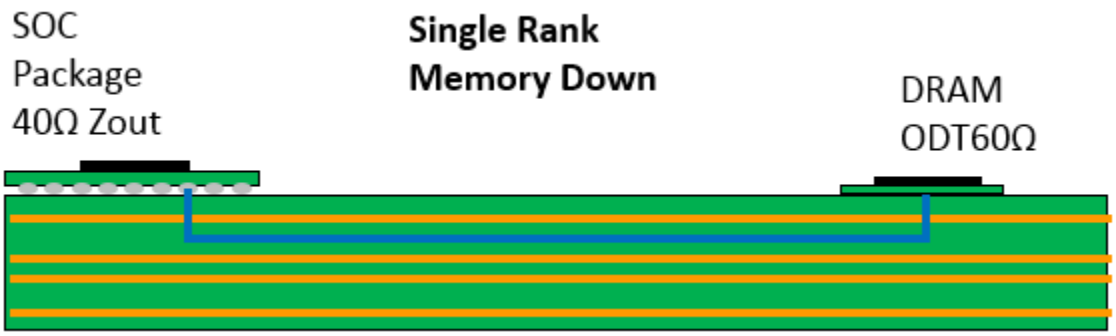
## 2.1 Determining Target Supply Impedance: An Example

DDR links are single-ended parallel interfaces. They can generate large simultaneous switching currents. The IO rails are particularly susceptible to this. This example will describe how to determine the supply impedance for the IO rail of a for a DDR4 interface operating at 2400 Mbps.

- DDR4 operating at 2400Mbps.
- IP is LPDDR4 multiPHY (V1) in a TSMC 16FFPLL process.
- The interface is 32bits wide.
- Source impedance is 40Ω, ODT at the SDRAM load is 60Ω to VDDQ on the data lanes.
- Command/Address/Control/CK/CKn are terminated with 50Ω to VTT=VDDQ/2 at the end of a daisy chain route.
- Loading is a single rank.

In the process this analysis will illustrate the concepts associated with $I_{Sw}$, $V_{Rip}$ and $Z_{PDN}$, how they vary and how they can be controlled.

**Figure 4:Single Rank memory down DDR4 interface used for analysis.**



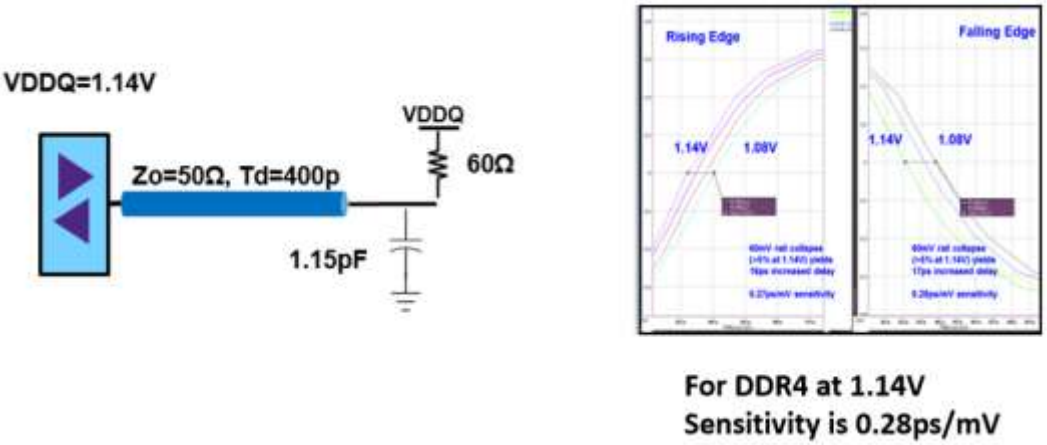

## 2.1.1 Power Supply Induced Jitter and Determining Voltage Ripple Targets.

Since supply impedance is key to controlling supply induced jitter, the first thing to determine is what the target jitter should be. The most stringent specification constraining jitter in a given DDR interface is the CK/CK# period jitter specification. Write transactions generate significant power rail noise from simultaneously switching outputs, there is significant tracking of the PSIJ between the DQ and DQS/DQS# signals. The CK/CK# period jitter specification does not benefit from tracking making it tougher to meet.

For DDR4, the total period jitter spec is +/-42ps. JEDEC defines period jitter as the variation of a given clock period from the average clock period. At 2400Mbps, the average period is 833ps. Therefore, the CK/CK# signal could vary from 791ps to 875ps without violating the specification. JEDEC goes further to specify deterministic jitter to +/-21ps at 2400Mbps. PSIJ is considered deterministic jitter. For budgeting purposes, we can assume that 2/3 of the specification is available for PSIJ from the IO rail (VDDQ) with the rest of the budget for core contributions. This gives us a target of +/-14ps from which to determine the needed supply impedance on the IO rail. For faster bit rates, the jitter target will decrease causing the required supply impedance to be lower.

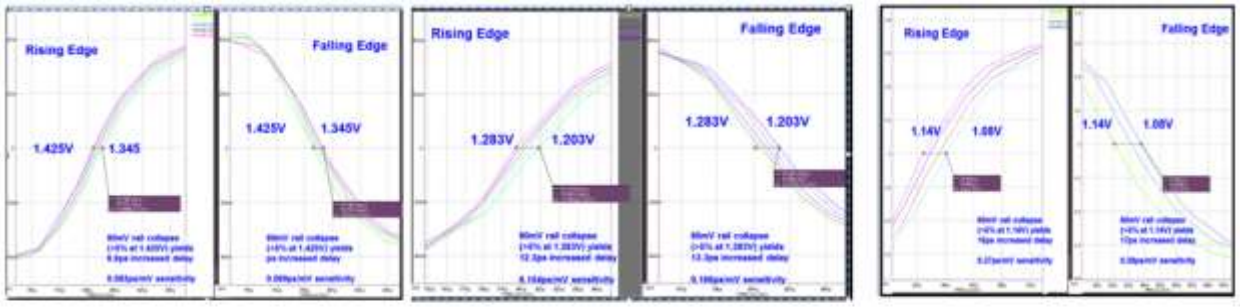
The amount of jitter that is created by noise on the power rail will increase as the silicon process gets slower. All analysis of supply sensitivity should be performed in the worst-case process corner. The jitter sensitivity to rail noise increase as the initial rail voltage decreases. When analyzing PSIJ, the lowest DC voltage for a given protocol should be used for the analysis. Figure 5 shows a simple test bench for determining the delay sensitivity to rail noise. The output pad should be loaded with a small capacitance and terminated to VDDQ for DDR4 to approximate the target configuration. An initial delay is measured at 1.14V. Then the DC voltage is dropped and the increase in delay is characterized. The sensitivity is determined by dividing the total increase in delay by the change in voltage.

**Figure 5: Determine supply sensitivity by lowering DC voltage and measuring increase in delay.**




Because of the DC voltage effect, different protocols will have different supply sensitivities. For a PHY that will be supporting multiple protocols within the same supply impedance environment (package and board), the supply impedance should be determined by the lowest voltage DDR protocol operating at its highest bit rate. Figure 6 shows different sensitivities for different protocols.

**Figure 6: Jitter sensitivity to supply increases as initial voltage level decreases.**




To determine the $V_{Rip}$ target, the desired maximum jitter is divided by the supply sensitivity determined in Figure 5.

$$V_{Rip-Target} = \frac{Peak\ Jitter}{Sensitivity} = \frac{14ps}{0.28ps/mV} = 50mV$$

The supply impedance design must limit the maximum peak ripple on the VDDQ rail to 50mV across the applicable frequency spectrum. The next step is to determine the switching current, $I_{Sw}$.

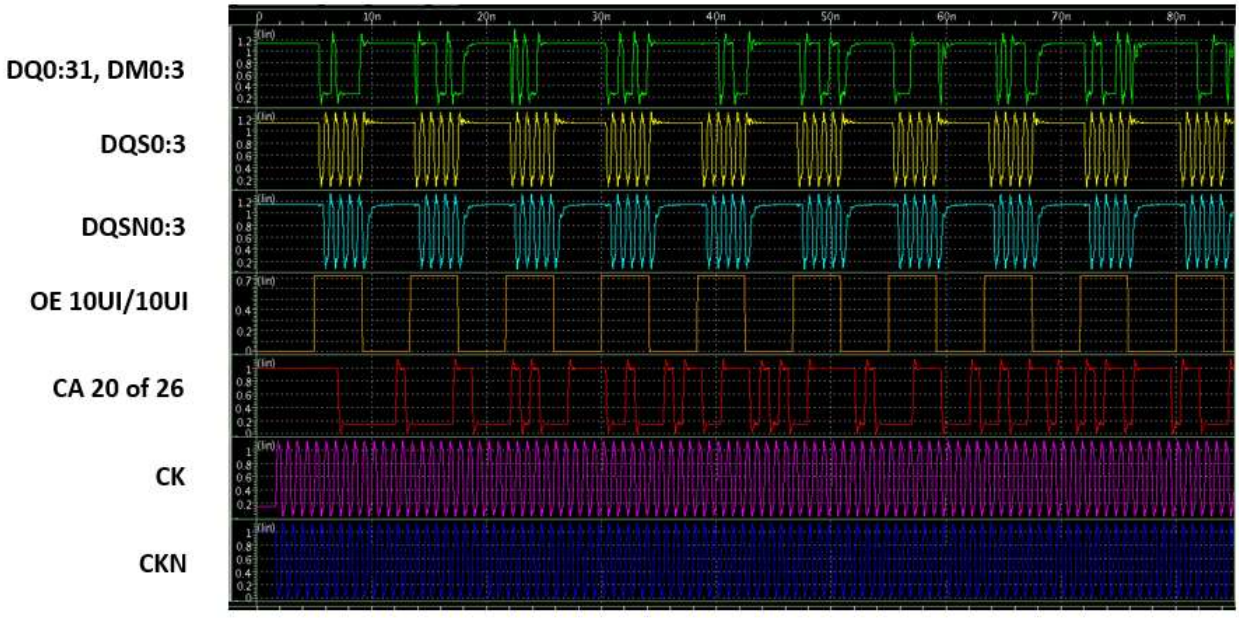
## 2.1.2 Determining the Switching Current

Switching current for the interface in question must be determined. While the amplitude of current will be greater in the Typical or Best Case PVT corners, the PSIJ sensitivity to the generated noise in these corners is significantly smaller than in the Worst-Case corner described above. Consequently, the current generation will be taken in the worst-case corner. Combining the maximum current from the Best Case PVT corner with the maximum sensitivity from the Worst Case PVT corner will create unnecessarily pessimistic values of supply impedance.

A Write simulation for the configuration in Figure 4 will be performed and the current for the VDDQ value will be monitored. For this analysis the following signaling conditions apply:

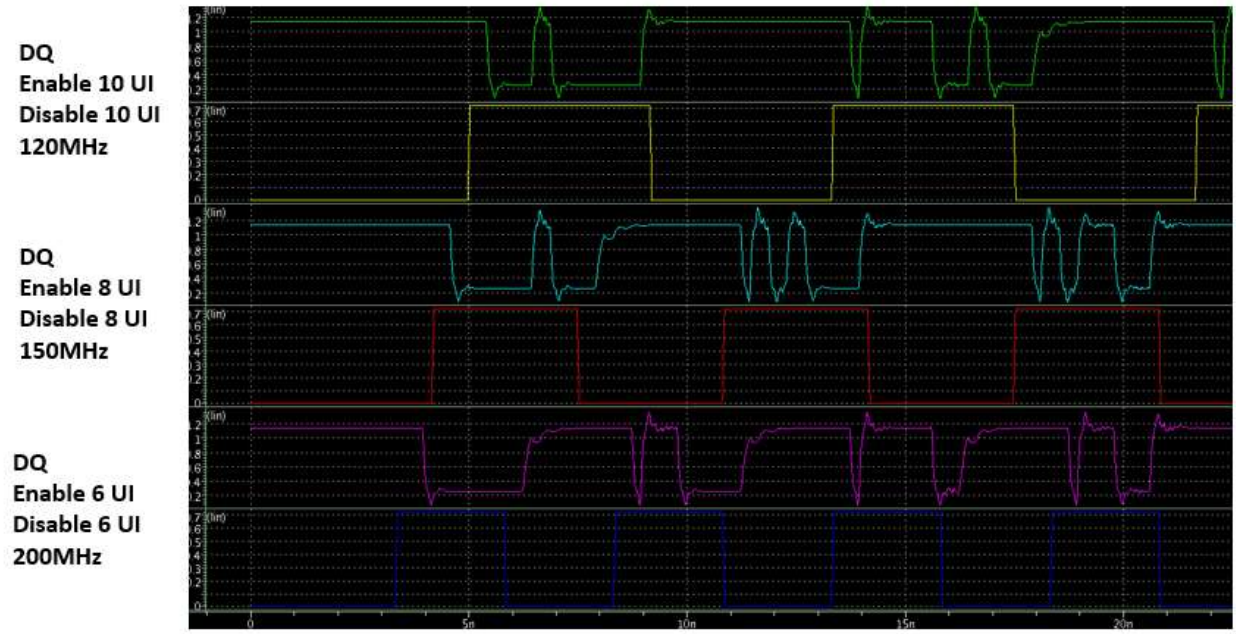
- A double data rate PRBS7 pattern will be applied to each of the 32 DQ signals and 4 DM signals. Identical patterns are applied to each bit exciting maximum current conditions.
- Differential strobe pattern that is 90° out of phase with the DQ/DM is applied to the 4 DQS/DQSN pairs.
- The OE, output enable, signal for the data lanes is toggled on for 10UI and then off for 10UI. This will excite frequency content of 120MHz in the current profile
- There are a total of ~26 Command/Address/Control signals on this interface. For this analysis it was assumed that 20 of these signals will be toggling.
- One CK/CKN signal is driven with a differential clock pattern edge-aligned with the DQS/DQSN signals.

- **Figure 7: Signal patterns on the interface used to generate the current vs time profile.**




In generating the patterns, it is important to account for the package environment of the SOC. Typically, the package inductance and on die decoupling generate a resonant point in the 100MHz to 200MHz range in order to be sure supply impedance is well accounted for in this region, the OE signal will also be toggled at 8 UI on 8 UI off, 150MHz, and 6 UI on 6 UI off, 200MHz. These results will be overlaid to determine the final supply impedance requirement.

**Figure 8:Varying OE toggle rates.**




Summing all of the currents provides the I vs. T plot in Figure 9 with an average current of 277mA. Then convert the I vs. T to I vs. F by performing an FFT,

**Figure 9: Total current vs time for the described interface.**

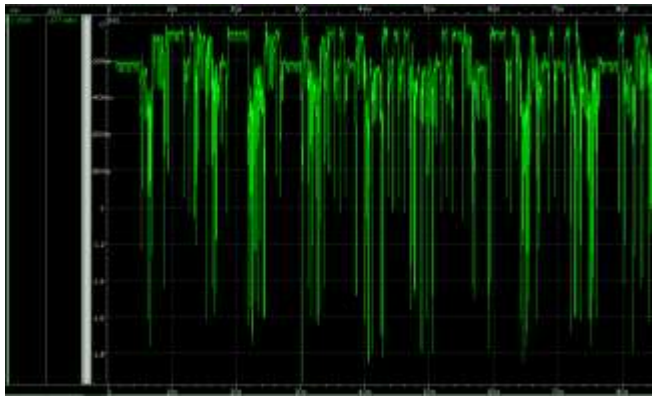
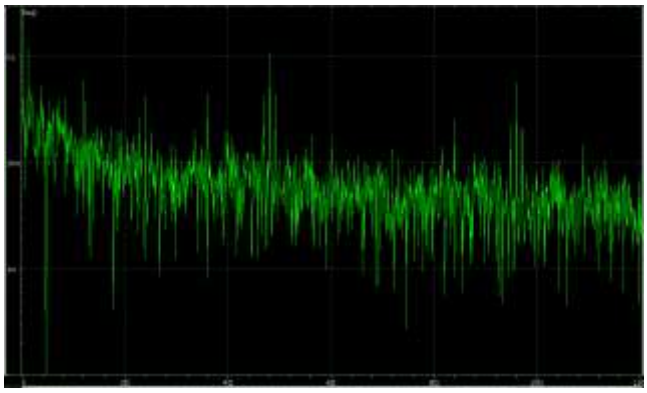
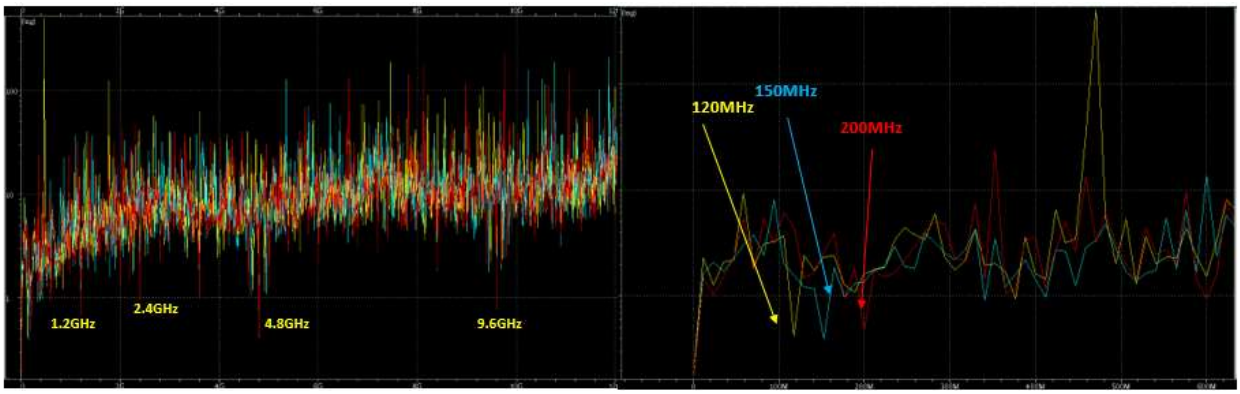


**Figure 10:Current vs. Frequency.**



The supply impedance is then determined by dividing the $V_{Rip}$ requirement of 50mV by the I vs. F waveform to get the supply impedance vs. frequency. In Figure 11 on the left shows the 3 supply impedance curves for the different OE toggle rates. Current concentrates at multiples of the 1.2GHz operating frequency. On the right is a zoom to the supply impedance requirement driven by the different OE toggle rates. This region will be the most critical because it usually aligns with the package resonant point.

**Figure 11:Vrip/ (I vs. Frequency) for analyzed cases with varying OE toggle rates.**




**Finally, a meaningful supply impedance specification is developed to guide designers, Figure 12. This is an approximation. It should be used for conservative guidance, but should be confirmed with time domain simulations of the interface after the initial power delivery network is designed. Simulations with real SSO conditions will assure that the jitter kept within specifications. The results in Figure 12 are worst case results reflecting SSO patterns on the data lanes and the CA bus.**

Figure 13 shows the specification relative to a simulation with more typical random patterns applied to the data lanes and the CA.  Output Enable on the data is toggled at 10UI enable/10UI disable.

**Figure 12:Approximate Supply impedance specification for single rank interface with worst case patterns.**

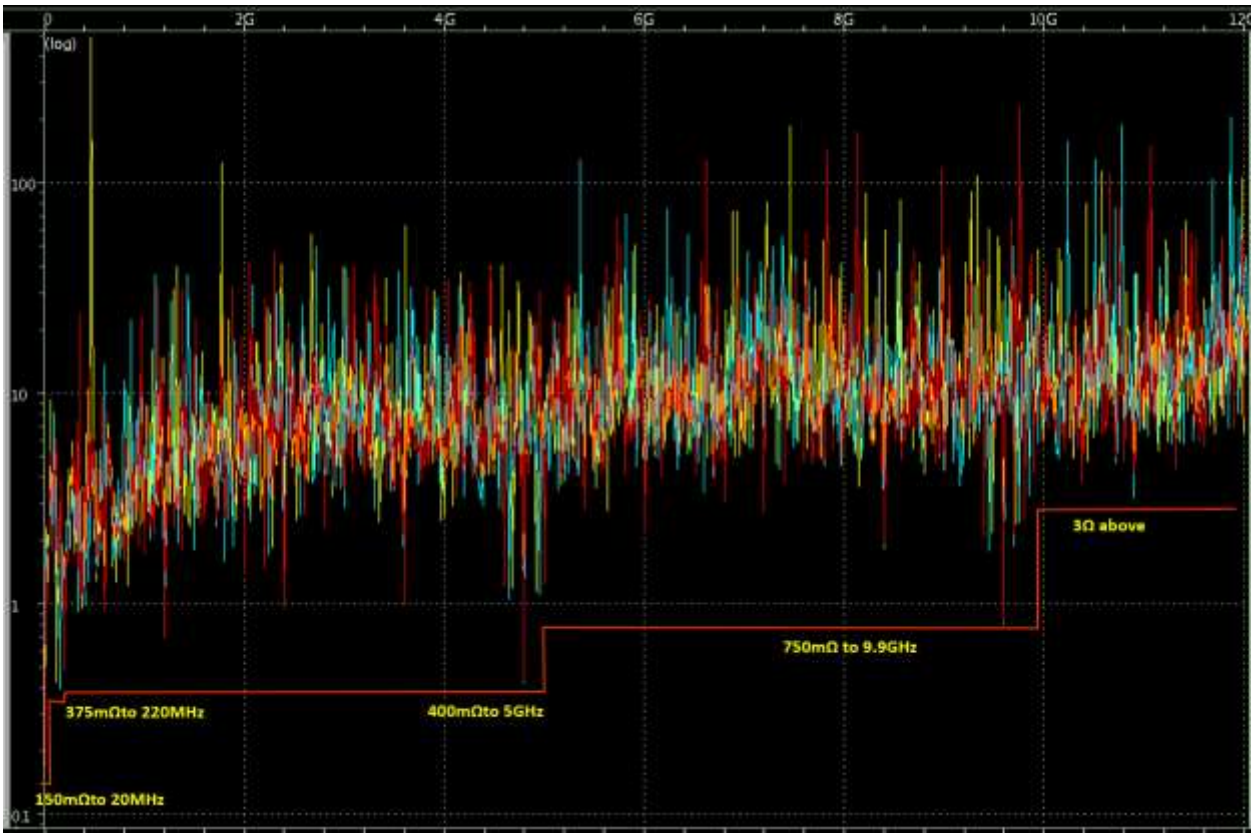
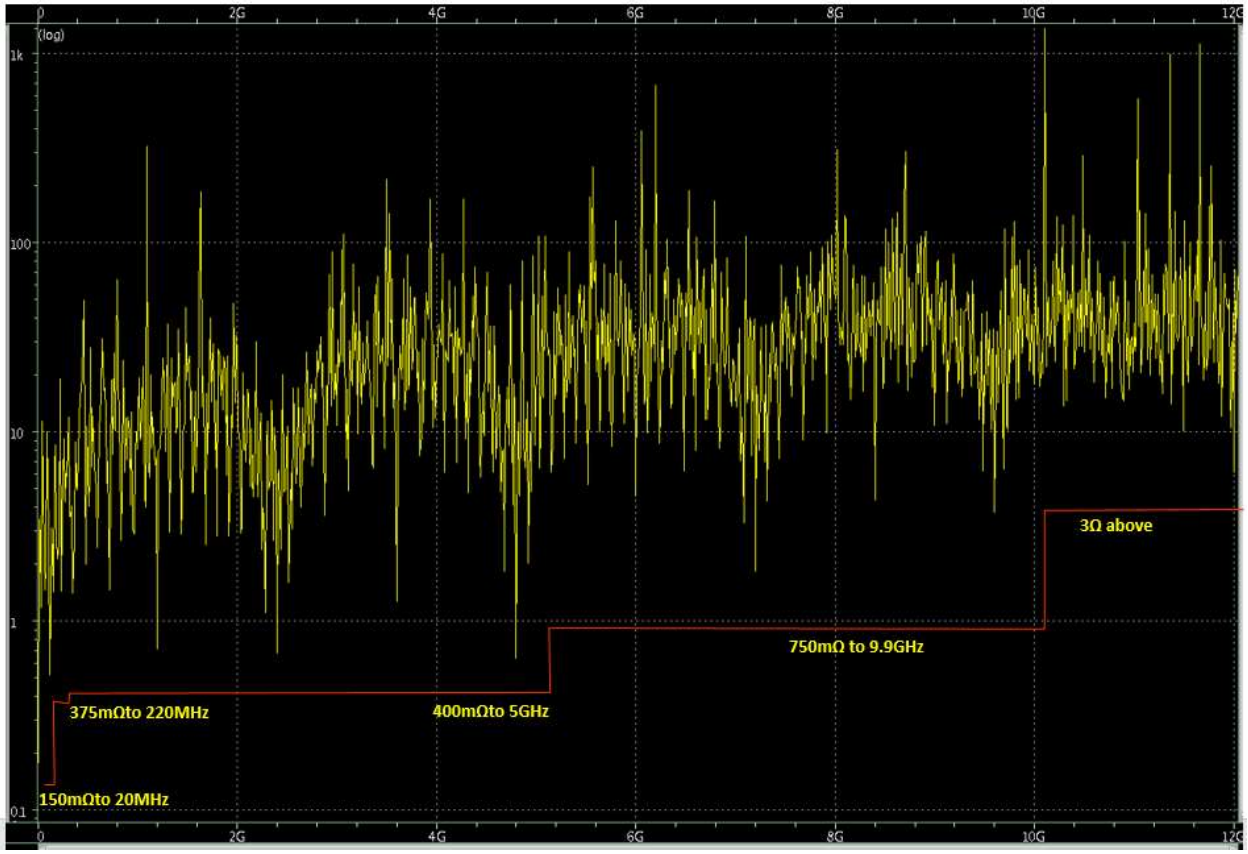


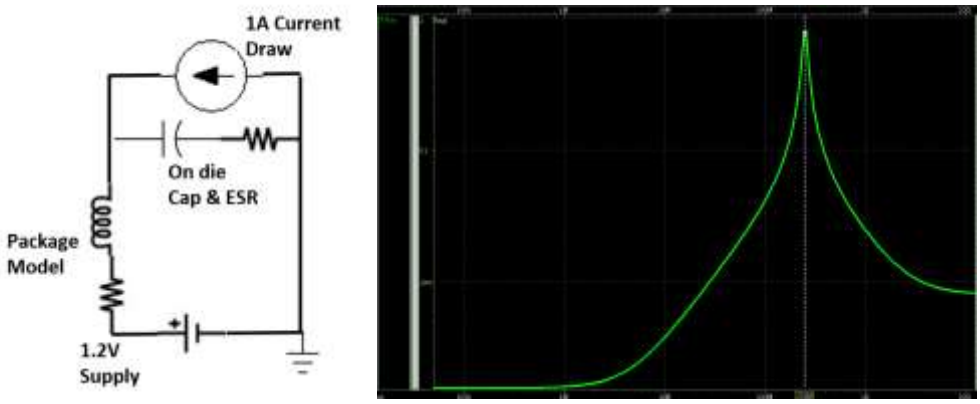
**Figure 13: Random patterns applied to interface yield a significant increase in margin to the derived supply impedance specification.**



## 2.1.3 Actual Design vs. Target Impedance Specification

With the target impedance determined, the next step is to determine whether the measured supply impedance of the actual power delivery network will meet the specification. To do that, simulate the circuit the PDN as shown in Figure 14. This example includes the package parasitic inductance and capacitance as well as on die decoupling and its equivalent series resistance. The resultant resonant peak is 775mΩ at 253MHz. Referring to the target specification in Figure 12, the PDN impedance violates the 400mΩ specification at this frequency.

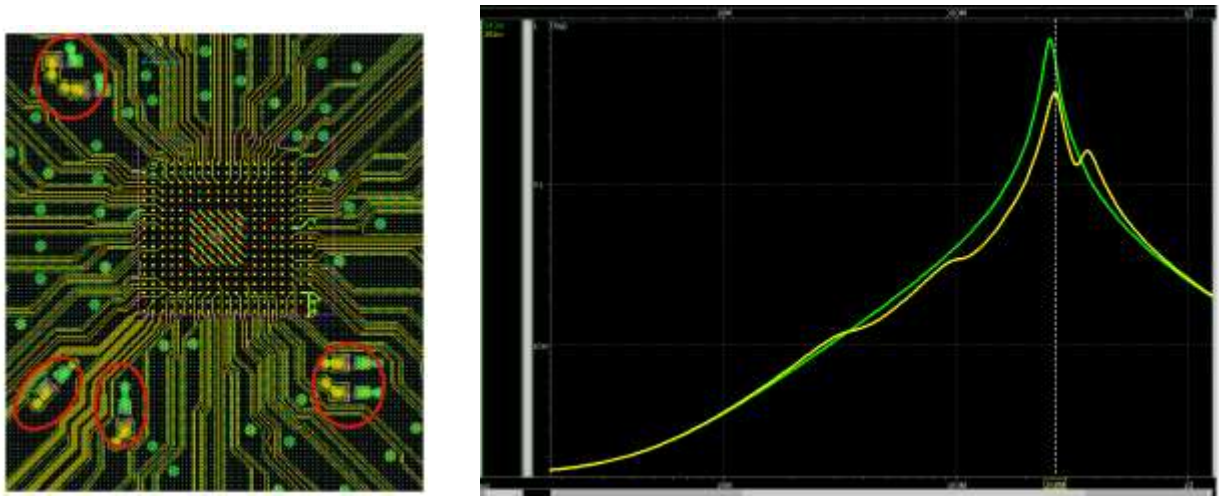
**Figure 14: Determining the supply impedance over frequency.**




**The first step to address the spec violation is to sweep package inductance and on-die decoupling to determine whether a solution that is practical to implement is available. Then look to include SMT capacitors on the package substrate. These SMT capacitors can be very effective in managing resonant peaks in the 100MHz to 200MHz range. For high frequency applications, it is prudent to always include footprints for on-package capacitors in case they are needed. These are not as effective at high frequencies associated with the edge rate because of the intervening package inductance. They are, however, beneficial at midrange frequencies associated with package resonances such as with this example. In this case, three 0402 capacitors of 100nF, 10nF and 1nF were placed on the substrate. As shown in**

Figure 15, these knocked the peak resonance impedance down to 361mΩ at 268MHz, meeting the target specification.

**Figure 15: Provide for substrate mounted capacitors; supply impedance with capacitors in place.**



## 2.2 A Word about Signal:Power:Ground Ratios.

When Signal:Power:Ground ratios are quoted for a particular interface, this is a simplistic way of describing the necessary supply impedance for a particular interface. They are quoted with numerous caveats:

- The power bumps are well distributed around the interface.
- The number of vias through a layer and balls are at least half of the number of bump connections.
- The number of ball are at least half of the number of bumps.
- There is not excessive slotting of the power planes
- Bond wires are kept as short as possible

Supply impedance is a complex combination of inductance, capacitance and resistance. The required supply impedance is driven by all of the parameters outlined in Table 1. In addition, the application must be considered when making a judgement about supply impedance. For example, an LPDDR3 interface that operates unterminated at 2133Mbps will probably need a lower supply impedance than a terminated interface. In addition to the greater signal swing of the unterminated interface, reflections will erode the unterminated timing budget more than the budget for the terminated interface. To compensate for this, a lower supply impedance will be required.
In lieu of quoting blanket ratios, Synopsys will review the customer's entire supply impedance design and make recommendations as appropriate. This review can be requested through the CAE group.

# 3 Components of the Power Delivery Network

The components of the power delivery network are broken up into five categories that correspond to the frequency range each category impacts. Reference Figure 16

**Voltage Regulator Module (VRM) –** DC to KHz range.

**Bulk Decoupling Capacitors-** KHz-MHz range.

- Includes Bulk capacitors in 10uF to 100's uF range and high frequency ceramic capacitors in the 1nF to 10uF range.

**Surface Mount Capacitors (package substrate) -** 10KHz to low 100MHz range

**Package Impedance –** 100MHz to 200MHz range. The inductance sets the cut off frequency.

**On Die Decoupling** – Supplies all of the current in the frequency range above the cutoff frequency determined by the package.

**Figure 16: The supply impedance network.**

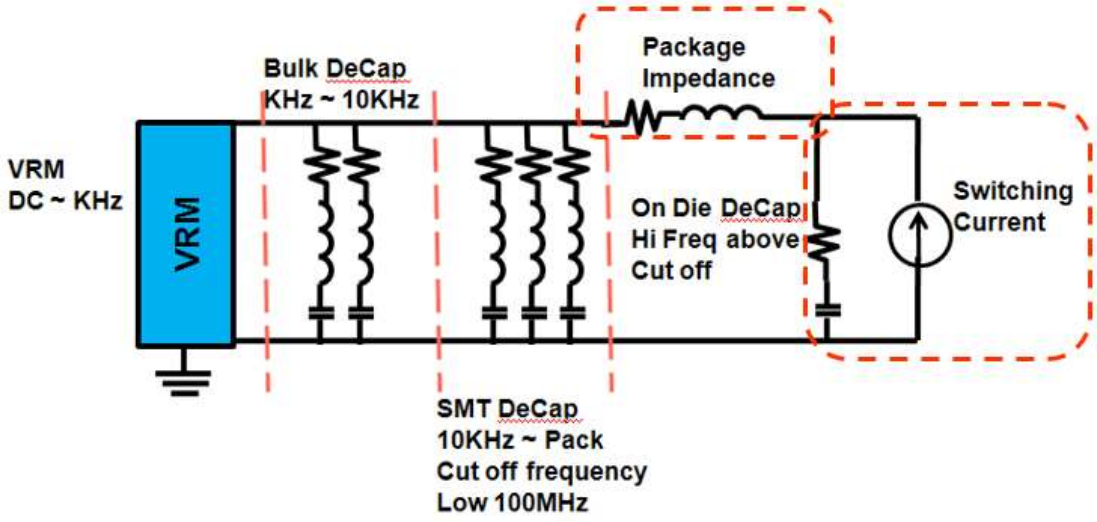



Figure 16 illustrates a typical power distribution network. Each of the components has a different frequency range of effectiveness. It is important that the power distribution network provides low impedance power delivery across the frequency spectrum to control power noise. When impedance is low, large changes in current will only result in small changes in noise. Figure 17 illustrate how the various components of the PDN influence supply impedance at different frequencies.

The light blue curve labeled "ALL" is the composite impedance magnitude (Ohms) of all the elements combined vs. frequency. The other curves represent impedance plots of contributions of different power supply network elements vs. frequency. Note that inductive elements like the package only impedance (dark blue curve) increase with increasing frequency. Capacitive elements like on die decoupling caps (or Diecap, green curve) decrease with increasing frequency. The components of the power supply network have different frequency ranges of effectiveness and can be modeled electrically as shown in Figure 18. The next three sections describe the main elements of the power supply network, the voltage regulator, the supply interconnect path, and the decoupling capacitors, and their influences on the overall power impedance.

**Figure 17: Power network impedance plot.**

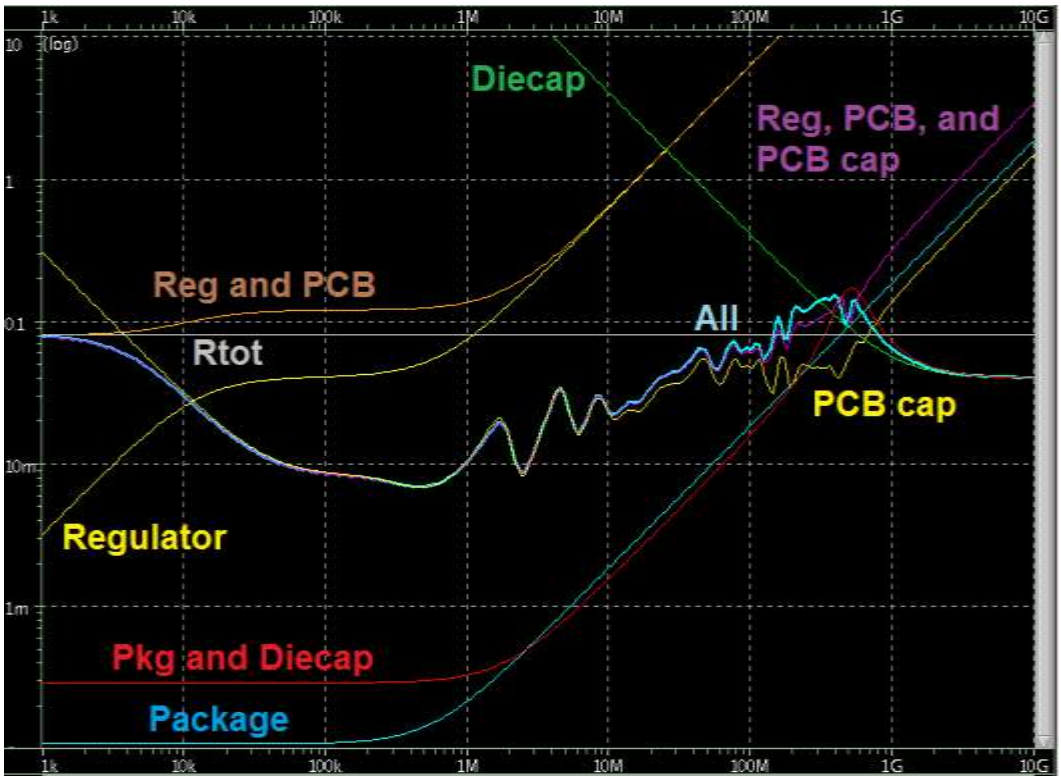
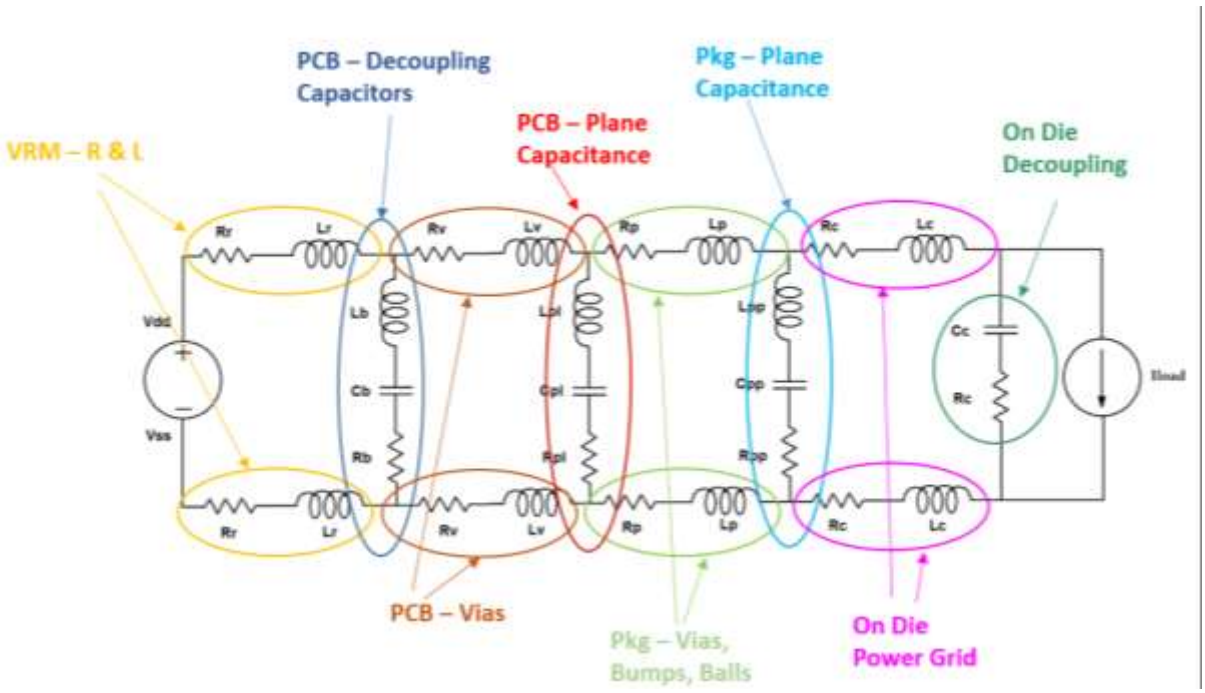



**Figure 18: Electrical model of power supply network.**



## 3.1 Voltage Regulator

The VRM (Voltage Regulator Module) is typically a brick type module component or integrated circuit on the PCB providing current and regulated voltage for the DDR IO, termination voltage VTT, and Vref voltage of the DDR interface. The VRM circuit is the Lr inductance and Rr resistor (and VDD DC supply) shown on the left side of **Error! Reference s ource not found.**. The VRM will provide low impedance from DC to the low kHz range (Yellow curve labeled "Regulator" in Figure 17). Beyond this frequency, the VRM cannot respond quickly enough to meet the current demands. The regulator and PCB vias cause the low frequency impedance to increase as seen by the brown curve on the impedance plot labeled "Reg and PCB". The power supply is typically distributed from the VRM with the use of power and ground plane layers in the PCB. PCB vias are required to connect the VRM to the power and ground balls of the DDR host and SDRAM devices.

## 3.2 Power Network Interconnect

The physical metal structures of the PCB, package, and on die power network are used to deliver the power to the switching circuits on die. These consist of PCB vias and power planes from VRM to device package, package balls, package vias, package planes, package bumps or bond wires, and, on die power networks (metal busses). These physical structures can be modeled electrically as resistances and inductances as shown in Figure 18.

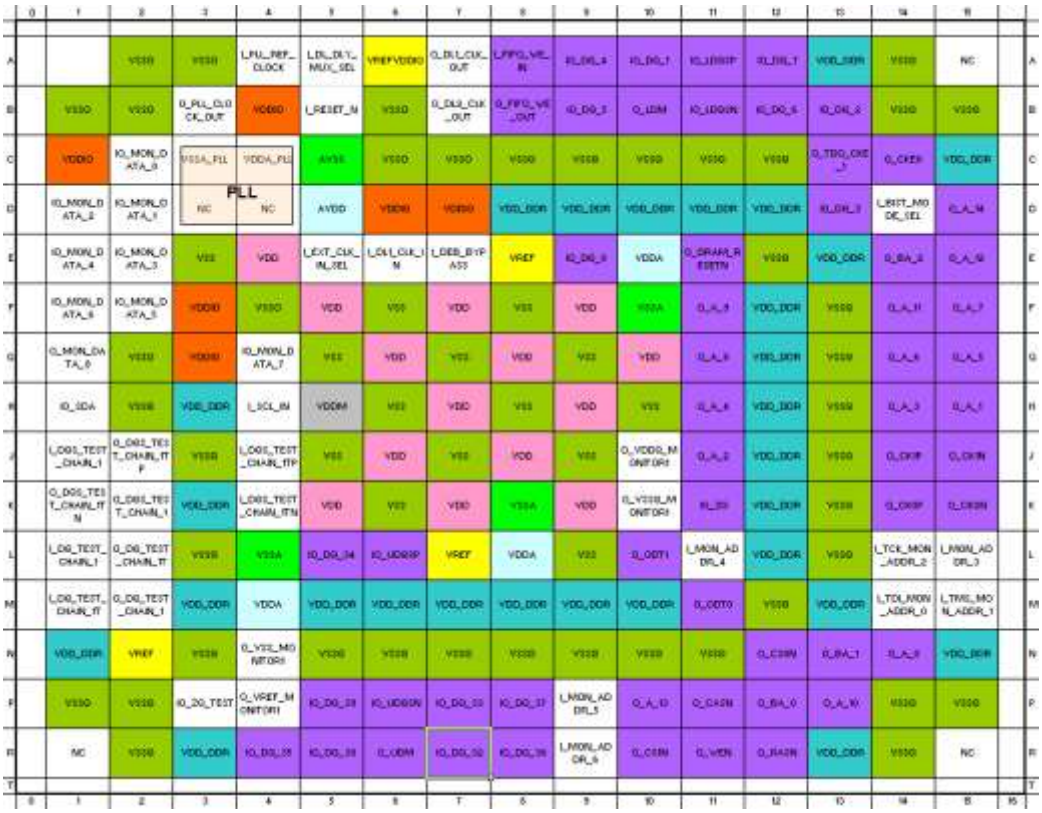
The outer loop of the power net circuit model in Figure 18 (excluding capacitances) is largely inductive and resistive in nature. The inductance is usually of more importance here as it will determine the cutoff frequency of the network, that frequency at which on board decoupling capacitors cease to be effective. In Figure 17, the impedance vs. frequency is shown for the outer loop inductance and resistance with no decoupling capacitors as seen from the die load back towards the regulator. It is interesting to note that if the inductances were set to zero the network would have a constant low impedance (Rtot grey horizontal line) across all frequencies. The inductance is increasing impedance with increasing frequency:

$$X_L = j\omega L$$

It is imperative that all inductance be minimized as much as possible. The highest contributors are PCB via inductance, and package via inductance, or bond wire inductance.

The first area of inductance to be tackled is PCB power plane via to Package ball inductance. These vias can have large inductance in the order of hundreds of pH for a power/ground pair loop. The key here is to lower loop area by placing power/ground planes higher in the PCB layer stack-up to shorten via connections to the chip package pins. Also, maximize the number of power and ground pins. This adds more parallel connections and scales the inductance down by the number of connections. Another factor is package power/ground pin arrangement. Further lower power/ground pin loop area by placing power pins and grounds in close proximity to each other. Figure 19 shows an example test chip pin out. The DDR interface is on the right-hand side of the chip (purple signal pins). The DDR IO power pins (VDD_DDR, light blue) are always directly adjacent to ground pins (VSSQ, green) which helps lower loop inductance in the power pins of the package.

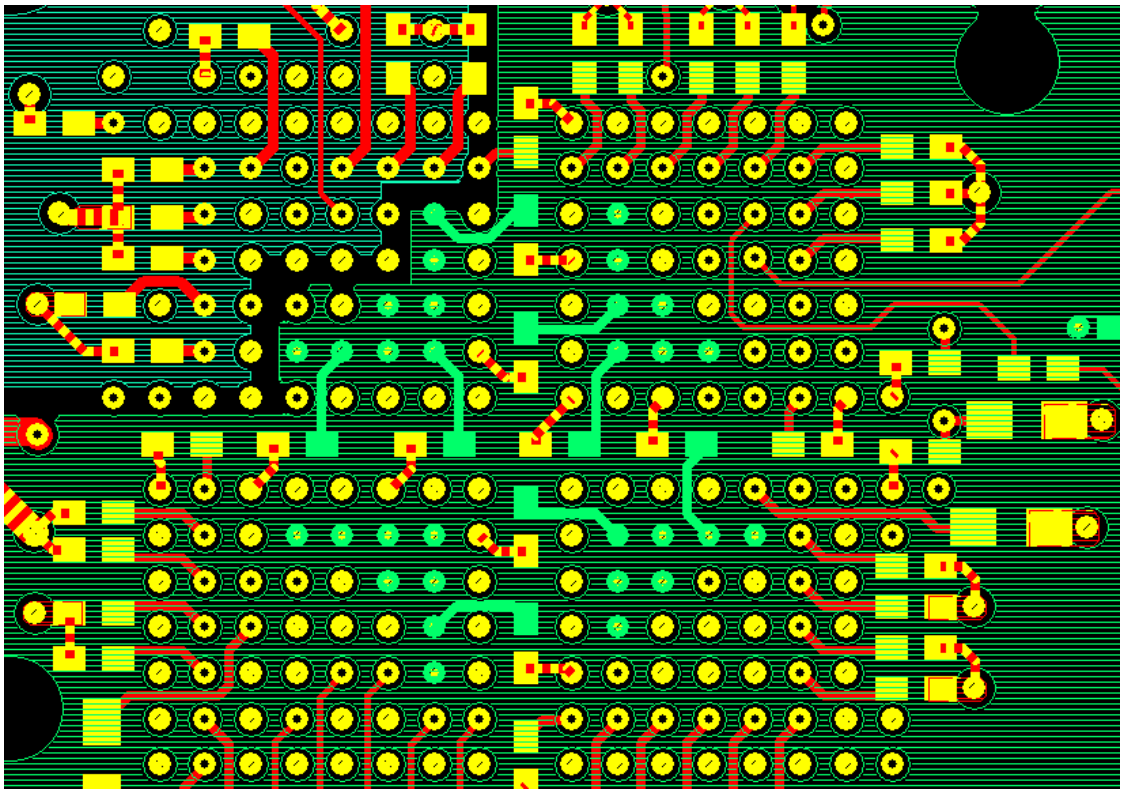
**Figure 19: Example Test Chip DDR IO Power/Ground Pin placement**




## 3.2.1 PCB Parasitics

Power and ground PCB planes internal to the PCB are used to supply power from the regulator to the device package pins. This is labeled as Lpl, Cpl, and Rpl in Figure 18. In multi-layer PCBs power, ground, and signal vias are used to bring nets from layers other than the top layer to the device balls These vias need clear-out spaces from the power and ground planes to avoid shorting. These clear-outs (if too big) combined with small power net plane area fills in the pin field region of a high-density chip can increase power plane impedance by reducing the metal available to carry the power supply current. Figure 20 shows an example of a good PCB power plane layout. The power net connections from PCB vias to power plane are shown as green circles and traces to the green power plane. The power vias are well supplied from the power plane metal fill and the clear-outs from other signal vias does not cut off the flow of current from the power plane to the power vias.

**Figure 20: Device Power Plane Connections**



The power and ground planes also form a parallel plate capacitor (assuming power and ground planes are adjacent to each other) which can be useful at much higher frequencies than the PCB mounted decoupling caps. The only drawbacks are; the capacitance is small since the size of the plane area is quite small (typical plane cap = 322pF per square inch power plane cap area for a typical board) and the loop inductance of the power and ground vias connecting the planes to the package balls will limit their high frequency effectiveness. The equation for PCB power plane cap is roughly:

$$Power\ Plane\ Capacitance = \frac{8.854\times10^{-12}\cdot\varepsilon_r\cdot A}{d}$$

where $\varepsilon_r$ is the relative dielectric constant of the dielectric between the planes, A is the area of the planes in square meters, d is the distance in meters between the planes. A few ways to maximize this capacitance is to keep the distance d between power and ground planes small (use thinner dielectric), use higher $\varepsilon_r$ dielectric material between the power and ground planes, and increase the A, or area of the planes. One way to maximize plane area is to fill unused plane areas on adjacent routing layers with power and ground plane fill and connect with stitching vias.

## 3.2.2 Package Parasitics

**Packages have vias to connect from balls to inner die layers. This inductance is Lp and Rp in Figure 18. The inductance of these connections can be reduced by having larger numbers of via connections.**

Figure 21 shows the power and ground net connections in a typical flip chip package and Table 2 shows typical values of inductance for those connections. Inductance values should be obtained through electrical model extractions in 3D field solvers. Note that package balls and core vias have largest individual inductance, but this can be counteracted by using higher numbers in parallel as space permits.

**Figure 21: Flip Chip Power and Ground Nets**

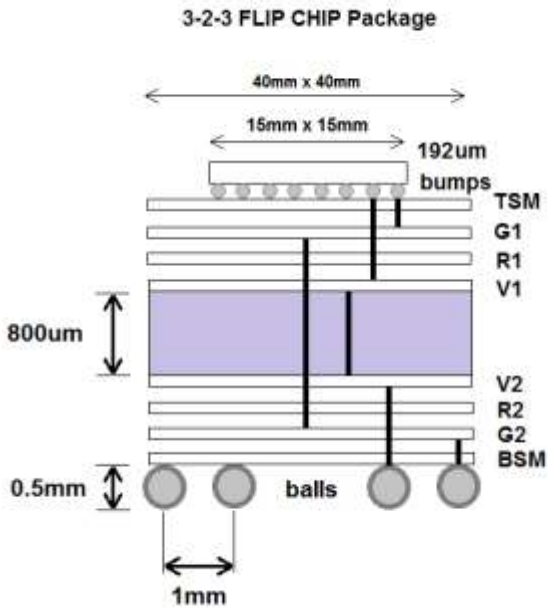


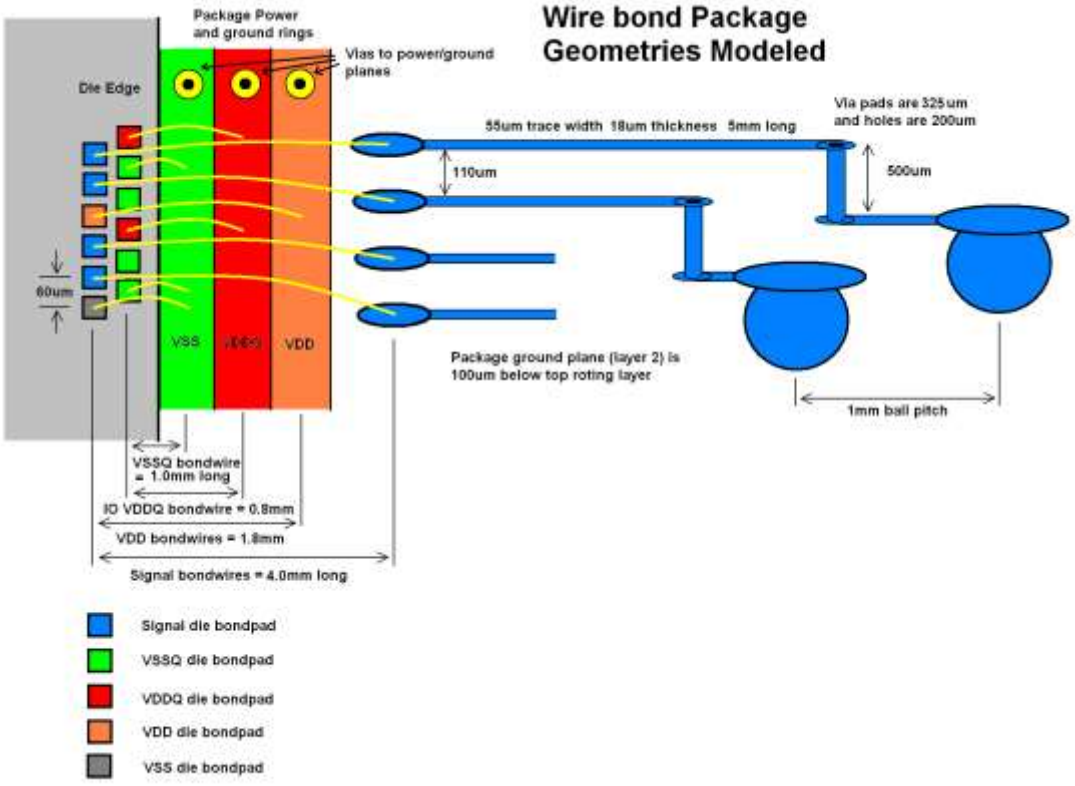

**Table 2: Flip Chip Inductance**

| Physical Dimensions | Lself1 | Lself2 | M | Lloop | Number of Pairs | Equivalent Inductance |
|---|---|---|---|---|---|---|
| C4 Solder Bump diam=90um pitch=192um | 15.67pH | 15.67pH | 4.24pH | 22.87pH | 2000 | 0.01pH |
| A Vias through build up layers diam=50um length=35um pitch=192um | 4.82pH | 4.82pH | 0.64pH | 8.35pH | 2000 | 0.03pH |
| Vias through Core diam=300um length=800um pitch=707um | 246.5pH | 246.5pH | 84.57pH | 323.8pH | 145 | 2.23pH |
| Solder balls diam=500um length=500um pitch=1mm | 86.67pH | 86.67pH | 25.17pH | 122.98pH | 112 | 1.09pH |

Wirebond packages have extra inductance in the form of bond wires (approximately 1nH partial inductance per mm length) from package to die. This is shown for a typical four-layer package in Figure 22. Ground and power net bond

wires are located on outer rows of the die bond pads to make shortest possible connections to the ground and power busses of the package. Power bond wires are located very close to ground bond wires to minimize loop area. The power and ground vias have similar inductance to the core vias of the flip chip package since their geometries are roughly similar. Their inductance tends to be high so it is important to maximize the number of power ground vias in the package.

**Figure 22: Wire Bond Package Power and Signal Interconnect**




The impedance of the package alone (flip chip case) is shown by the darker blue curve labeled ‘Package” in Figure 17. This package inductance will create a cutoff frequency beyond which PCB mounted capacitors will have negligible impact. The cut off frequency $F_{CO}$ is determined based on the target impedance of the power supply. If the target impedance is 80mΩ and the total inductance for the supply is 65pH, the cut off frequency is calculated by:

$$Z_{pdn-target} = 2\pi F_{co} L_{package}$$

$$F_{co-package} = \frac{80m\Omega}{2\pi \times 65pH} = 196MHz$$

All switching current above this cut off frequency will be delivered by the on die capacitance indicated by the green curve labeled “Diecap” in the plot. Note that the package inductance will form an anti-resonance with the diecap due to the lack of damping in those circuits and this is shown by the peak in the red curve labeled “Pkg and Diecap” at around 500-600 MHz in the plot.

When inductances of the power network cannot be minimized further, decoupling capacitance is used to lower the impedance of the power network, which is discussed in the next section.

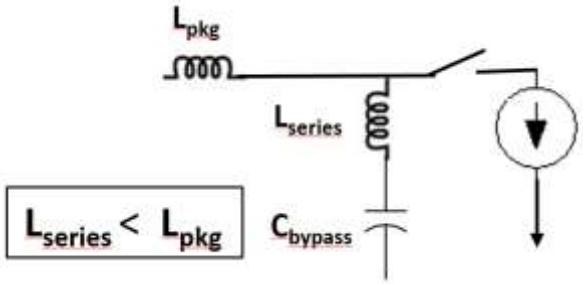
## 3.3 "Decoupling" Capacitors

Capacitors have two traits that are important to PDN design, they store charge and they form high frequency short circuits.

### 3.3.1 Bypassing (Charge Storage)

The charge storage feature delivers current through a low inductance path "bypassing" the higher inductance paths, i.e. the package. For bypass capacitance to have a benefit, it must be located between the current source and the inductance being bypassed, and the inductance associated with the capacitor must be less than the inductance being bypassed. For example, a capacitor mounted on the substrate of a wire bond package will not have much impact since the package inductance and the wire inductance in series with the capacitor are about the same. If the package were mounted in a socket, however, Lseries would be less than Pkg and would have a benefit. Bypassing prevents noise and voltage droop from being injected on the power rail. Bypassing plays an important role in the frequency range dominated by the rise time and its harmonics. It is primarily done with the on die decoupling.

**Figure 23: Effective bypass capacitance.**




### 3.3.2 Coupling (Make noise common between power and ground)

"Decoupling" is a misnomer when used to describe capacitance. A capacitor acts as a high frequency short. It will "couple" noise from an active line to a quiet line. Coupling capacitance will take noise that appears on the power rail and use the high frequency short to couple it to the ground, making the noise common to both rails and reducing its impact. Coupling capacitance has its most dominant effect in the frequency range dominated by the bit rate of the DDR interface and below.

### 3.3.3 Implementing Capacitors in the Power Delivery Network

Printed circuit board decoupling capacitor values should be chosen to reduce the impedance of the power distribution network below the target impedance over the widest range of frequencies with the fewest components. Individual capacitors will only be effective in a certain range of frequencies since they are limited by the self and mounting inductance of the capacitor. Decoupling caps are added in stages. Each stage lowers impedance over a certain frequency range. The first group of capacitors are the PCB decoupling caps labeled CB in Figure 18 (along with parasitic Rb and Lb). PCB decoupling capacitance is limited to approximately 100MHz by internal body inductance, and PCB mounting inductance (PCB vias to power and ground planes).

Choose bulk decoupling caps that will lower the Regulator and PCB (brown curve) impedance in Figure 17 of the outer loop inductance of the power network below the target impedance. PCB decoupling caps and their important electrical parameters are shown in Table 3. Choose the capacitors with the lowest resonant frequency (47uF) and enough of them

in parallel to reduce the impedance below the target impedance. This is shown in Figure 17 as the Reg, PCB, and PCB cap purple curve.

**Table 3: Capacitor values, parasitics and self-resonant frequencies.**

| Capacitor Value | Unit | Capacitor Size | Capacitor ESR (mOhm) | Capacitor ESL (nH) | Mounting Inductance (nH) | Package Inductance (nH) | Self-Resonant Freq. (MHz) | Capacitor Impedance at cut off (Ohms) |
|---|---|---|---|---|---|---|---|---|
| 47 | uF | 1206 | 20 | 1.25 | 0.3 | 0.5 | 0.512 | 3.330 |
| 22 | uF | 1206 | 20 | 1.25 | 0.3 | 0.5 | 0.748 | 3.330 |
| 10 | uF | 0805 | 30 | 0.8 | 0.3 | 0.5 | 1.257 | 2.614 |
| 4.7 | uF | 0805 | 30 | 0.8 | 0.3 | 0.5 | 1.833 | 2.614 |
| 2.2 | uF | 0805 | 30 | 0.8 | 0.3 | 0.5 | 2.679 | 2.614 |
| 1 | uF | 0603 | 40 | 0.7 | 0.3 | 0.5 | 4.104 | 2.463 |
| 470 | nF | 0603 | 40 | 0.7 | 0.3 | 0.5 | 5.986 | 2.463 |
| 220 | nF | 0603 | 40 | 0.7 | 0.3 | 0.5 | 8.749 | 2.465 |
| 100 | nF | 0603 | 40 | 0.7 | 0.3 | 0.5 | 12.977 | 2.468 |
| 47 | nF | 0603 | 40 | 0.7 | 0.3 | 0.5 | 18.929 | 2.475 |
| 22 | nF | 0603 | 40 | 0.7 | 0.3 | 0.5 | 27.667 | 2.490 |
| 10 | nF | 0402 | 60 | 0.55 | 0.3 | 0.5 | 43.257 | 2.302 |
| 4.7 | nF | 0402 | 60 | 0.55 | 0.3 | 0.5 | 63.097 | 2.372 |
| 2.2 | nF | 0402 | 60 | 0.55 | 0.3 | 0.5 | 92.225 | 2.521 |
| 1 | nF | 0402 | 60 | 0.55 | 0.3 | 0.5 | 136.791 | 2.859 |
| 470 | pF | 0402 | 60 | 0.55 | 0.3 | 0.5 | 199.530 | 3.558 |
| 220 | pF | 0402 | 60 | 0.55 | 0.3 | 0.5 | 291.640 | 5.055 |

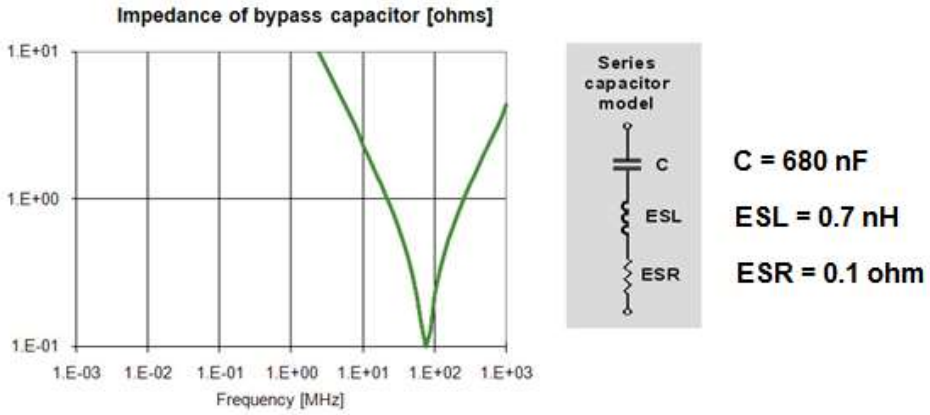
Bulk capacitance, electrolytic or tantalum, is used in the low frequency range, up to the 10's of KHz range to reduce the effect of regulator and PCB inductance. These PCB mounted capacitors are either electrolyte dielectric based in a cylinder can shape or a solid tantalum dielectric in a brick shape which offers high capacitance in a larger package. The tradeoff for high capacitance is poor high frequency performance due to the large parasitic inductance.

**After this range, higher frequency SMT capacitors are applied. These capacitors are useful into the range of 100's of MHz. Continue to add capacitors of different values since they are effective over a range of different frequencies. When their self-resonant frequency is higher than the PCB power and ground via and package inductance they tend to lose their effectiveness. Small valued capacitance for higher frequencies can get swamped by the via inductance and capacitor package inductance. In Figure 17 we can see the effect of mid-range PCB decoupling caps from 1MHz to 200MHz with the Reg, PCB, and PCB cap purple curve. The impedance of all the PCB caps is shown by the yellow "PCB cap" curve in the impedance plot in Figure 17. This is the composite impedance of several different PCB capacitors of different values in parallel. It is a somewhat trial and error process to choose caps values. Usually common values like decades or logs values are used to give maximum frequency coverage.**

Figure 24 shows an impedance vs. frequency plot for a single 680nF 0603 PCB SMT ceramic cap. It forms a" V" shape in the impedance profile since the pure capacitance is limited by parasitic self-inductance and PCB mounting inductances. At the lowest impedance point is the resonant frequency where capacitance and inductance are equal and opposite and only the self-resistance remains. The self-resonant frequency is given by the equation:

$$Self Resonant\ Frequency = \frac{1}{2\pi\sqrt{(ESL + Mounting\ Inductance)\times C}}$$

**Figure 24: Single PCB Decoupling Cap**




To increase the effectiveness of these capacitors the inductance must be minimized. The inductance depends heavily on loop area of the current paths of the decoupling capacitor pins and PCB mounting to the PCB power and ground planes as Figure 25 shows. Figure 26 shows different capacitor PCB footprints to minimize loop area and the resulting mounting inductance. The tradeoff here is PCB space vs. lower inductance. Another improvement can be to place decoupling caps on the top layer of the PCB and use higher layers in the pcb stackup for power planes to connect the decoupling cap power vias to. This lowers inductance by again minimizing loop area of the power network.

**Figure 25: PCB Decoupling Cap Current Loop Area**

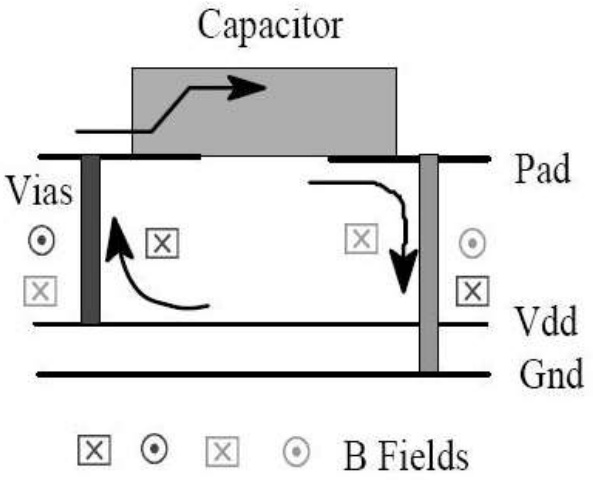
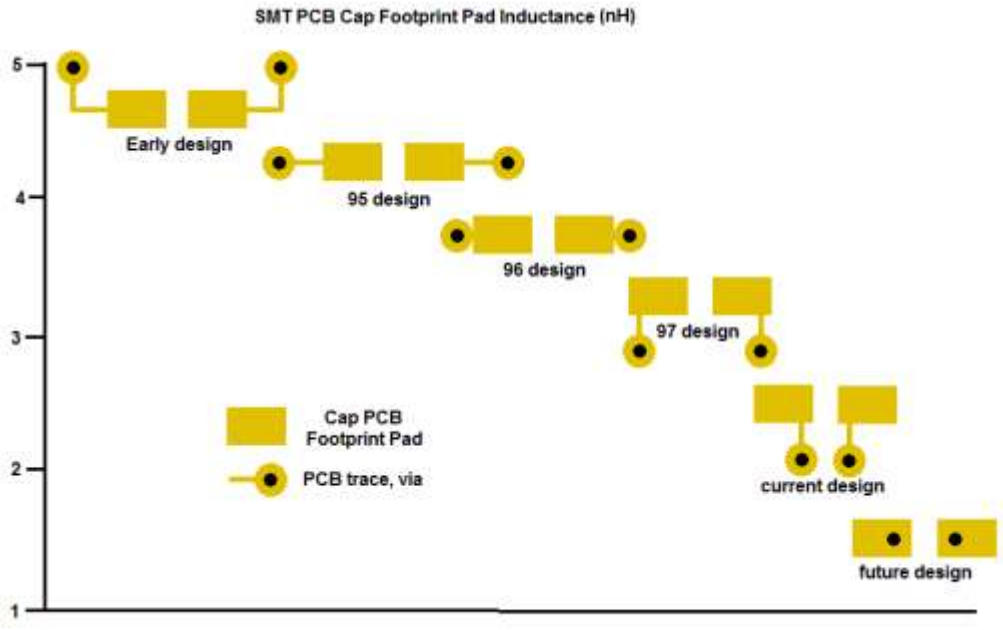


**Figure 26: PCB Decoupling Cap Footprint vs. Mounting Inductance**




The PCB power ground plane capacitance is added and is usually defined more by chip placement and board space than any other parameter. This is Cpl in Figure 18. This capacitance is fairly small but it's effect can be seen at around 500MHz on the Reg, PCB, PCB cap purple curve in Figure 17.

#### 3.3.3.1 Spreading Inductance

It is important that VDDQ and VDD power planes on the board be placed directly adjacent to the VSS plane in order to lessen the spreading inductance. This is the inductance associated with the current flow from the sources, VRM or supply capacitors, to the package balls. Capacitors should be placed as close as possible to the host to minimize this inductance. The spreading inductance in picoHenries/Square is approximated by the formula:

$$L_{\left(pH/_{square}\right)}=\frac{32pH}{mil}\times Height\ (mils)$$

Height is the distance between planes. Multiply this value by the number of squares (length/width) of the routed copper to the host to get the inductive contribution. 4 mils of separation between planes would yield 128pH/square, whereas 50 mils of separation would yield 1.6nH/square. The practical consideration this raises is that care should be used when implementing 4 layer boards which can have very thick cavities.

### 3.3.4 On Die Decoupling Capacitors

The on die decoupling capacitors are chosen next. These are indicated by Cc in Figure 18. This decoupling capacitor functions primarily as a bypass capacitor since it occurs after the PCB and package inductance. It will provide the high frequency currents associated with the edge rate. On die decoupling comes at the expense of die area. The goal is to

determine what is the absolute minimum capacitance that can be provided on die and still meet the system target impedance.
One methodology to determine this is:

1. Determine maximum power supply noise AC amplitude that the IOs (best case, typical, and worst case PVT corners) can tolerate based on SSO jitter budget, (7.5% of DDR data bit period typically)
2. Simulate the I/Os in Hspice and determine I/O current draw at the slowest slew rate of all the IOs in parallel driving loads similar to worst case PCB and memory load encountered in the DDR system.
3. Determine the maximum power supply impedance value to achieve desired AC noise amplitude with the total AC current drawn (Zpdn= Power Supply Voltage Collapse(mV)/Maximum IO Switching Current(mA)).
4. Determine the lowest power supply $F_{knee}$ frequency of the switching signal waveforms based on output rise time $F_{knee} = 0.5/T_{r\ (10\%-90\%)}$ where the rise time is measured at the I/O output pad.
5. Calculate amount of total on-die capacitance required to achieve the impedance at that frequency

Note: This will yield a first order approximation. It is recommended that transistor level simulations be performed to determine:

1. The amount of jitter created by power rail collapse.
2. The power rail noise created by specific data transaction patterns
3. The amount of on die decoupling required to keep the power rail noise within the necessary limits to control power supply induced jitter.

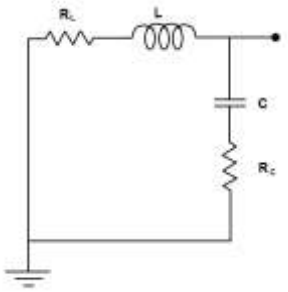
In Figure 17 the green Diecap curve shows the impedance of the on die decoupling cap impedance. Also, note the dark blue Package inductance curve. The Red Pkg and Diecap curve shows the effect of package and die capacitance together yielding a resonant peak at about 500MHz. The complete power supply impedance curve with all decoupling caps added is the light blue curve labeled “All”. In an ideal world, the target impedance is met across the entire spectrum. In reality there might be some larger peaks at specific frequencies that might poke through and cannot be minimized. They might not be a problem if they do not occur at a particular frequency of interest like a clock frequency.

#### 3.3.4.1 Package-Die Capacitance Resonance

An interesting thing to note is that resistance of the power supply network can be used to optimize the impedance. This is particularly the case with the resistive interconnect of the on die capacitors. Since it is lossy in nature it can be used to dampen the frequency response of the reactive Cs and Ls of the power network.
Looking at the circuit in Figure 18, examine the far-right hand part of the network including the package inductance and on die decoupling cap network of the power supply. This is shown in Figure 27.

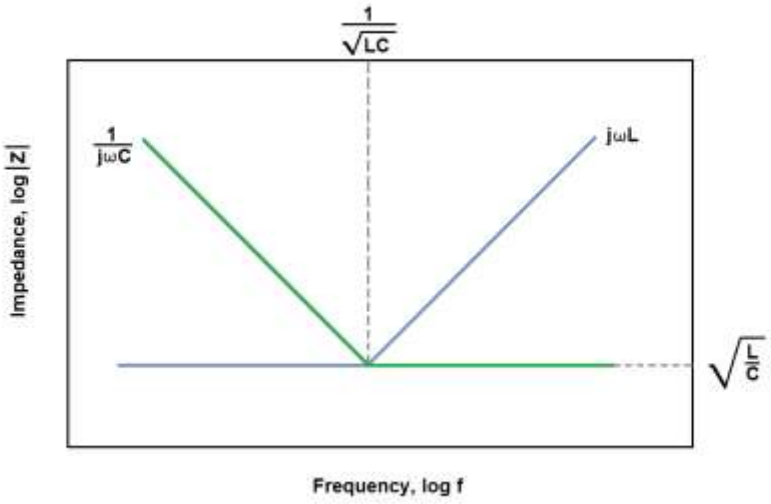

*Each PHY databook includes a table listing decoupling capacitance associated with each cell on the pad ring and wire bond pad if applicable. Additional decoupling is available for in the form of “Snap Caps”. These Snap Caps can be added to the outside of the pad ring.*

**Figure 27: Package Inductance and On-die Capacitance Network**




The impedance profile of the package inductance is the same as the blue Package impedance curve in Figure 17. The impedance profile of the on die decoupling capacitance including parasitic $R_c$ is a mirror image of the inductance network with an initial decreasing slope and flattening out at the knee frequency to the constant resistance at higher frequency. Choosing C and $R_c$ judiciously can align its knee frequencies and magnitude perfectly to cancel the RL network as can be seen in Figure 28. The result is a purely resistive network that achieves perfect compensation which is not unlike compensation used in scope probes for optimal signal transfer.

**Figure 28: Power Network Compensation**




The ability to perform this compensation depends a lot on the ability to tune the resistive interconnect for the amount of on die decoupling caps provided. This is somewhat limited by the geometry of interconnect laid out in the decoupling IO cells in the library. It also depends on the resistance and inductance of the package interconnect which is usually fixed in the system. However, even if perfect compensation is not achieved it will help a great deal to keep resonances in the system to a minimum.

# 4 Considerations for the Core VDD Supply

The VDD supply is a bit more complex than the VDDQ supply because there are multiple current sources with differing switching characteristics that must be accounted for. Those currents include:

- Macro block generated currents where the dominant tone is related to the DDR Clock. This would be 2400MHz for a 2400Mbps interface, for example.
- Currents generated by the core side of the IO structure
- PUB currents
- Currents from the VDD shared with the rest of the SOC.

## 4.1 Determining VDD Power Rail Noise from the DDRPHY

For the PHY itself, a model should be generated of the die resistance and capacitance, the RDL, the package parasitics, on package decoupling, etc. A model of the typical current profile should be applied around the die for each of the sources, Figure 29. When these are applied the end, result is the noise on the rail found in Figure 30

**Figure 29: Model of the on-die resistance and capacitance, RDL, package and all currents from sources in the PHY.**

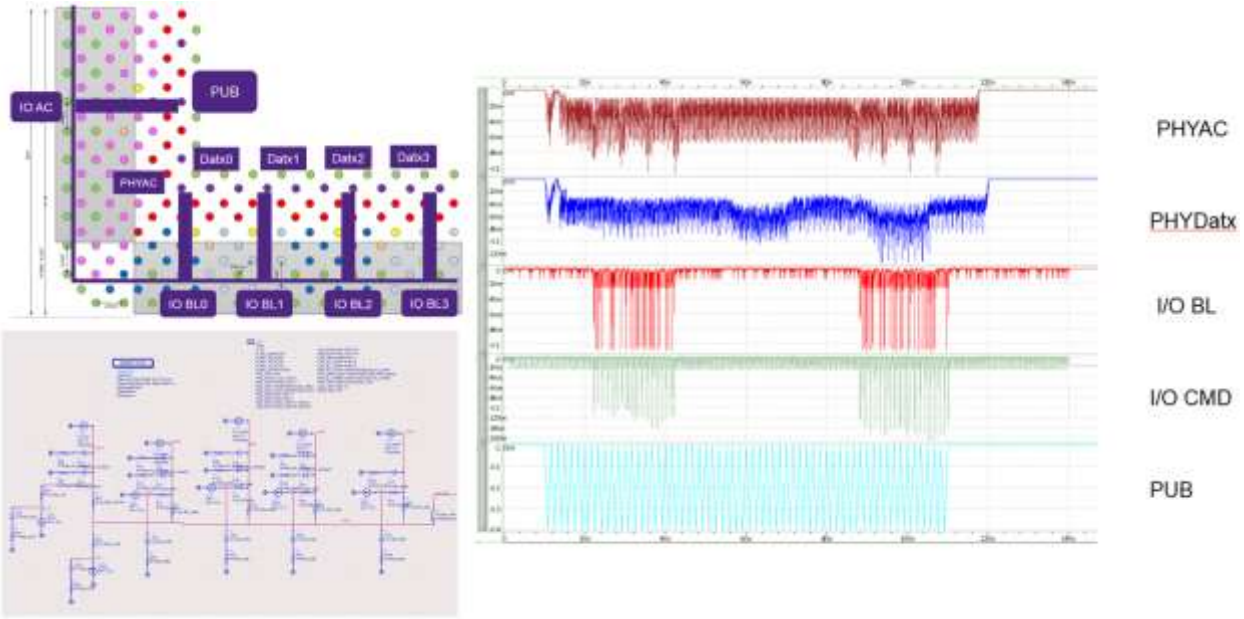
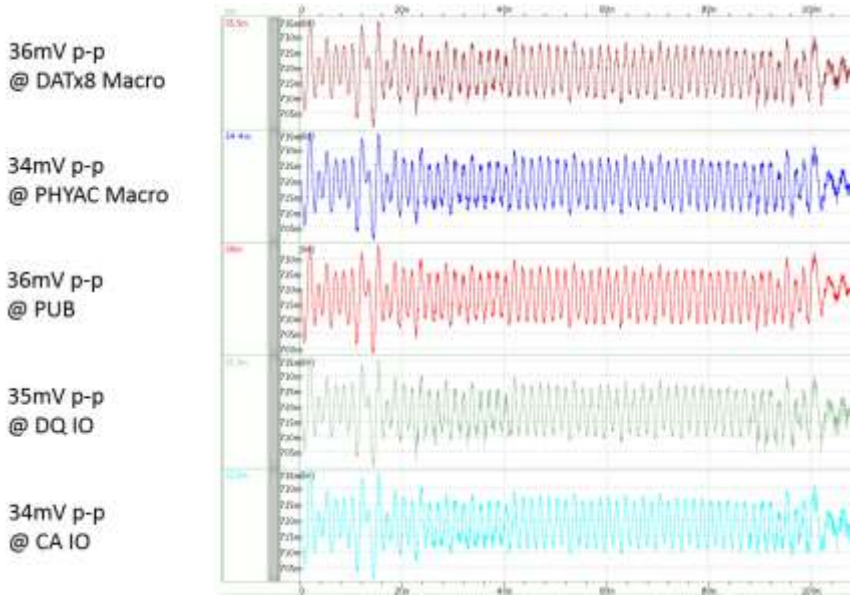


**Figure 30: Resulting noise waveforms around the die.**




Note that much of the high frequency content in the current waveforms found in Figure 29 is absent from the voltage noise waveform in Figure 30. Most of the higher frequency and some of the lower frequency noise is filtered out by the supply impedance curve resulting in a noise waveform that reflects the primary resonant point of the supply impedance, Figure 31.

**Figure 31: PDN filters high frequency current noise.**

## 4.2 Considering Noise from the Rest of the SOC

The VDD core voltage of a particular process is typically the same for the DDR PHY as for the rest of the SOC. In those cases where it differs, the core supply delivery network for the SOC would be isolated from the DDR core by definition. This raises the question of whether to isolate the DDR PHY core voltage on die from the rest of the SOC when the voltage is the same. In many low power applications, there is a benefit to powering down regions of the chip not being exercised, so isolation is done to support this. In cases where the application does not require isolation to allow separate power down regions, a decision regarding isolation must be made. It is difficult to make a blanket recommendation for all applications, so the advantages and disadvantages must be weighed. Simulations will likely be required to make this decision.

## 4.3 Isolating the DDR PHY Core Voltage (Die and Package)

### 4.3.1 Advantages

- Noise will only come from the DDR PHY. This will all be based on the same clock, consequently the noise will be synchronous with the edges of the signals. The jitter impact of synchronous jitter will be very low. The noise frequency will be at the bit rate or a multiple thereof. Consequently, the phase of the noise to the switching edges will be less variable than with asynchronous noise.

### 4.3.2 Disadvantages

- There will be a larger supply impedance through the package since it is not shared with the rest of the SOC.
- The DDR PHY will not have access to decoupling, explicitly placed and from non-switching gates, from the rest of the SOC. This may require that additional decoupling be placed in the PHY.

## 4.4 Joining the DDR PHY and SOC Core Voltage

### 4.4.1 Advantages

- Significant decoupling is available from explicit decoupling on the rest of the SOC as well as the substantial decoupling available from the non-switching gates.
- The supply impedance will be lower since all ball/via/bump paths for the core will be shared.

### 4.4.2 Disadvantages

- More current must share the lower supply impedance.
- This current will probably not be synchronous with the DDR edges or be a multiple of this frequency. Consequently, the asynchronous noise could be a source of significant jitter.
- Peak noise will occur at or near the package/die resonant frequency. This will probably require the inclusion of on substrate decoupling capacitors to control this.

## 4.5 Isolating the DDR PHY Core Voltage on the Die Only (Common in Package)

The impact of this will be very similar to the case where the DDR PHY and SOC are merged. There will be additional filtering of the SOC noise by the inductance of the path from the die on the SOC side, down to the package plane, and back to the DDR side. The impact of this will be to reduce the noise somewhat (simulations required) and will reduce the impact of on die decoupling from the rest of the SOC.

# 5 VAA_PLL Supply

VAA_PLL supply is used for providing power to the PLLs and IO Receiver circuits in the Gen2 multiPHY and the DDR4 MultiPHY. For all other IP, this supply is confined to only the PLLs. The guidelines provided cover 5 different system cases depending on the IP mentioned above and how it is used. Five different implementation scenarios are described below.

1. **PLL only VAA_PLL Supplies – Not Shared on PCB**
2. **PLL only VAA_PLL Supplies – Shared on PCB**
3. **PLL and IO RX VAA_PLL Supplies – Not shared on PCB**
4. **PLL and IO RX VAA_PLL Supplies – Shared on PCB**
5. **PLL and IO RX VAA_PLL Supplies – PDR=OFF constantly**

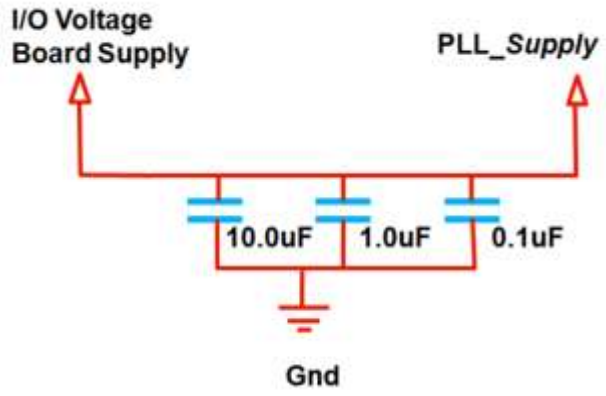
## 5.1 PLL only VAA_PLL Supplies – Not Shared on PCB

In this first case VAA_PLL supply is only needed to provide power to the PLL circuits. The VAA_PLL supply is used to provide clean power to the analog portion of the PLL and should be an isolated supply net through the package from the PCB. Decoupling circuits should be included on the PCB to help reduce noise on the VAA_PLL supply. If the VAA_PLL supply on the PCB is not shared with any other circuits on the PCB there is no requirement for more filtering components (like series ferrite bead) other than the decoupling caps as shown here (Figure 32) or on die. In this example there is a large 10uF capacitor and two smaller capacitors (1.0uF and 0.1uF). The small 0.1uF capacitor should be placed as close to the VAA_PLL pin of the package. The 1.0uF can be placed farther out than the 0.1uF capacitor and the 10uF capacitor placement will be less critical. The smaller two capacitors should be placed for every VAA_PLL pin of the package whereas the 10uF could be shared for a few VAA_PLL pins in a more central location.

The VAA_PLL supply net may be routed as a wide signal net trace with adjacent ground net trace which can be used as shielding, and should be spaced away from other noisy nets at least 3 times the height above the reference plane. Some of the byte lanes may have a VAA_PLL IO cell in the IO ring. Some of these VAA_PLL nets in the package may be combined and routed to a single package ball. It is recommended that no more than 5 PLLs' VAA_PLL nets be combined to one package ball. Target impedance and IR drop should be considered for the VAA_PLL power nets. For example, if the PLLs are operating in DDR3-1600 mode (clock = 800MHz) for Gen2 multiPHY, each PLL draws a maximum of 12mA each on VAA_PLL. The max AC supply noise at the PLL should be limited to +/-2.5% nominal VAA_PLL (from databook) or +/-2.5% of 1.8V = +/-45mV or 90mVpp. To a first order the target impedance should be 90mV/(5 * 12mA) = 1.5 ohms. For IR drop the minimum DC supply voltage at the PLL on die should be no less than nominal VAA_PLL – 10% or 1.8V * 0.9 = 1.62V.

On die, PLLs require PVAA_PLL cells in the IO ring to bring VAA_PLL supply to the core and provide ESD clamping to protect this supply. In general, one PVAA_PLL cell is used for each PLL. In flip chip applications, each PVAA_PLL should have its own bump. In wirebond packages each PVAA_PLL cell will have its own bondwire. If one PVAA_PLL cell is used to connect to a couple of PLLs, IR drop should be studied to ensure this is acceptable.
PLLs for the DDR PHY macros blocks contain regulators within the PLL block; therefore, no additional 1.8V VAA_PLL rail on-die decoupling capacitance is required for the PLLs.

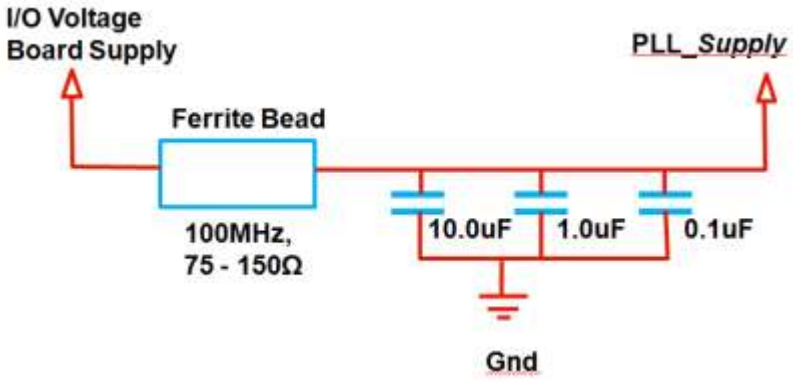
**Figure 32: PLL PCB Supply filter - Not shared on PCB**




## 5.2 PLL only VAA_PLL Supplies – Shared on PCB

If the VAA_PLL PCB supply is shared with other circuits on the PCB it is recommended to include a ferrite filter circuit on the PCB as shown in the figure below.

**Figure 33: Ferrite bead PCB filter circuit for VAA_PLL**

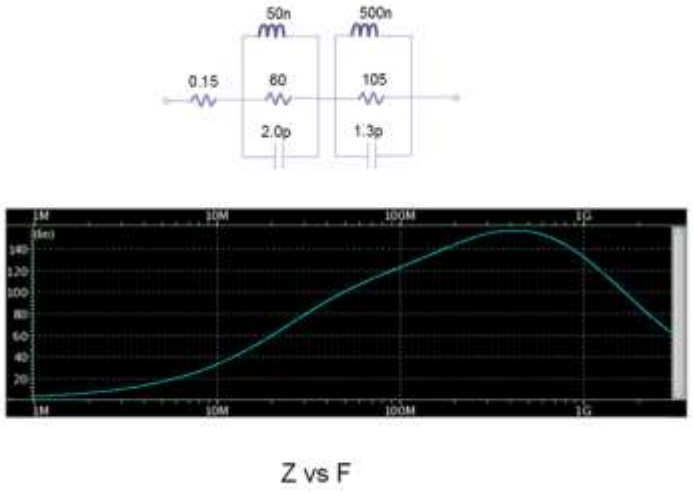



The ferrite is used to prevent noise from the other circuits on the PCB from entering the DDR PLL circuits on chip. Use of the ferrite circuit requires some specific attention on a few points. The bead material type, DC IR drop limit, maximum DC current limit, and the frequency response of the filter circuit need to be considered.
Ferrite beads come in a couple of types: non-resonant or absorptive beads and high Q or resonant beads. For filtering power supplies the non-resonant or absorptive bead types should be used. Using high Q beads can lead to unwanted power supply resonances.

For the DC IR drop, the ferrite is a series element with a finite DC resistance. A budget for the IR drop of the VAA_PLL supply should be created to determine the amount of DC IR drop that can be tolerated in the ferrite as well as package and on die interconnect. For example, if an IR drop budget allows 0.5% IR drop of the VAA_PLL rail for the ferrite bead, the voltage drop must be less than 1.8V x 0.5% = 9mV. If we have 5 PLLs sharing one ferrite bead the DC current will be 5

x 12mA =60mA, if we use the same example with Gen 2 PLL at 800MHz clock. Ferrite bead max DC resistance must be less than or equal to 9mV/60mA = 0.15 ohms.
Ferrite beads are a magnetic circuit and large currents flowing can cause the magnetic circuit to saturate and limit filter effectiveness. It is recommended to keep maximum current through ferrite bead to less than ½ the maximum current rating.
Target impedance and IR drop should be considered for the VAA_PLL power nets. Target impedance of the VAA_PLL supply will be the same as the "Not shared on PCB" case (1.5 ohms) but we now have the series ferrite in the circuit. The challenge is to attenuate the VAA_PLL supply noise entering from the PCB across as wide as possible range of frequencies while providing a low impedance supply at the range of frequencies the PLL requires. The PLL output frequency is 1600MHz (the 800MHz DDR clock is generated by a divide by 2 circuit in the last flip flop stage of the PHYAC macro for low duty cycle error). The output of the PLL is a 1600MHz clock with harmonics since the output is trapezoidal in nature. The input REFCLK to the PLL is a 400MHz clock (4x step up in PLL) and the PLL has a lower frequency loop bandwidth (<10MHz – need to check with PLL designers). In order to prevent noise from entering the PLL supply the ferrite needs to block noise from less than 10MHz to multiple GHz range.
Many different families of ferrites exist but certain families are optimized for blocking noise in power supplies in this frequency range in a small form factor. One such bead is the BLM15PX121SN1 bead from Murata Erie in a 0402 package. Here is the frequency response of the ferrite bead.

**Figure 34: Ferrite bead Impedance vs. Frequency Response**




Z vs F

Bead manufacturers usually provide an Hspice model for the bead – in this case we show a simplified equivalent model. On the datasheets for a bead the manufacturers usually specify a bead impedance at a specific frequency such as 120ohm impedance at 100MHz which is the case for our ferrite here. For the purpose of choosing a reasonable bead component for our filter, the response of the ferrite with impedance of approximately 100 to 120ohms @ 100MHz should give us decent broadband filtering coverage for the PLL circuit power.

Assuming we are seeing VAA_PLL PCB AC noise at about 100MHz and it is a maximum of around +/-10% nominal VAA_PLL= 1.8V x +/-10% = +/-90mV or 180 mVpp and our power network impedance equivalent to 90mVpp/60mA = 1.5 ohms from before, the noise seen at the PLL from the PCB would be 180mVpp x (1.5 ohms/(120ohms + 1.5ohms) = 2.22mVpp. At 10MHz the ferrite has an impedance of 32 ohms so PCB noise of 180mVpp would give 180mVpp x (1.5ohms/(1.5ohms + 32ohms) = 8mVpp. At 1.6GHz the ferrite is about 75 ohms so the noise from the PCB would be about 180mVpp x (1.5ohms/(1.5ohms + 75ohms) = 3.5mVpp. The ferrite will provide good broadband coverage.

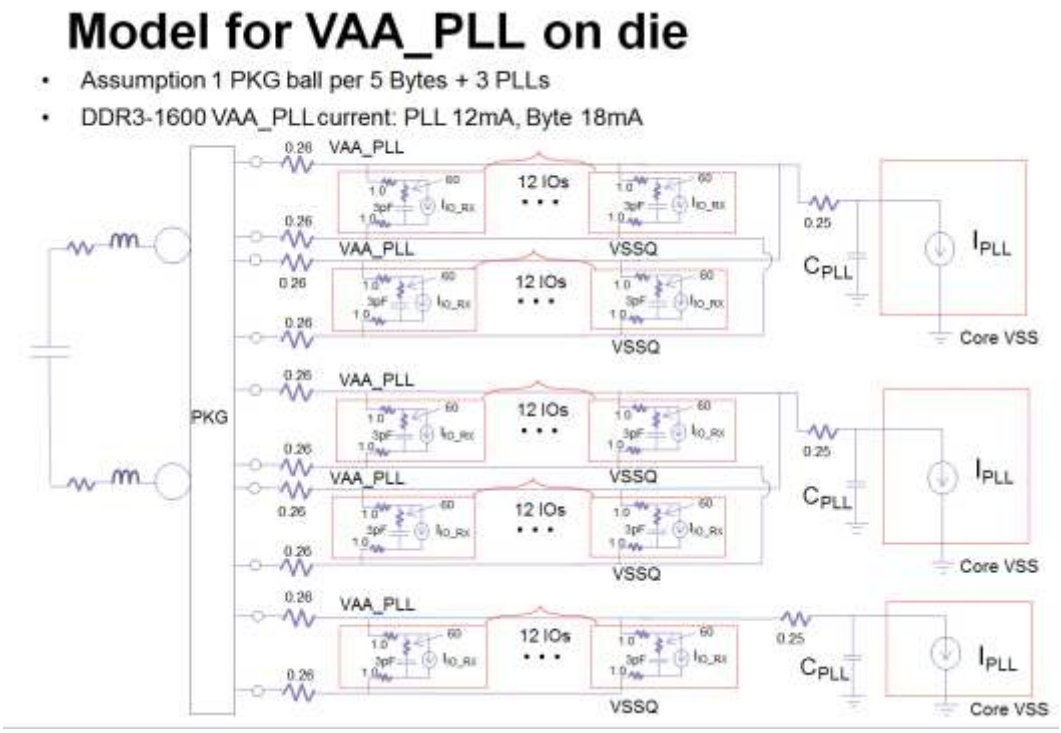
Next the PCB capacitors need to be added to maintain the VAA_PLL power supply at a low impedance to the PLLs. The values used are 10uF, 1uF and 0.1uF which cover the supply over a range of frequencies. The small 0.1uF capacitor should be placed as close to the VAA_PLL pin of the package. The 1.0uF can be placed farther out than the 0.1uF capacitor and the 10uF capacitor placement will be less critical. The complete PCB filter is shown in figure 87.
As in the “Not shared on PCB” case, the VAA_PLL supply net may be routed as a wide signal net trace with adjacent ground net trace which can be used as shielding, and should be spaced away from other noisy nets 3 times the height above the reference plane. Some of the byte lanes may have a VAA_PLL IO cell in the IO ring. Some of these VAA_PLL nets in the package may be combined and routed to a single package ball. It is recommended that no more than 5 PLLs VAA_PLL nets be combined to one package ball.

On die, PLLs require PVAA_PLL cells in the IO ring to bring VAA_PLL supply to the core and provide ESD clamping to protect this supply. In general, one PVAA_PLL cell is used for each PLL. In flip chip applications, each PVAA_PLL should have its own bump. In wirebond packages each PVAA_PLL cell will have its own bondwire. If one PVAA_PLL cell is used to connect to a couple of PLLs, IR drop should be studied to ensure this is acceptable.
PLLs for the DDR PHY macros blocks contain regulators within the PLL block, therefore no additional 1.8V VAA_PLL rail on-die decoupling capacitance is required for the PLLs.

## 5.3 PLL and IO RX VAA_PLL Supplies – Not shared on PCB

Some DDR IP, like Designware Gen 2 multiPHY use VAA_PLL for IO RX supply as well as PLL supply. In this case PCB and extra on die decoupling will be required to attenuate the VAA_PLL supply noise from RX IO circuits from exceeding PLL AC ripple limits (+/-2.5% nominal VAA_PLL). The extra current draw of the IO RX must also be considered in the IR drop analysis of the combined VAA_PLL supply for both IO RX and PLL. The IO RX circuit current draw may be dynamically switched by the PHY controlling the PDR pins of the IO (Power Down Receiver = 1 for IO RX power down) depending on write cycle (PDR=1) and read cycles (PDR=0) in order to conserve power on the IO supplies. The worst-case scenario for VAA_PLL supply noise is when PDR is dynamically switched which is the case considered here.

**Figure 34: On Die VAA_PLL supply - 5 Byte lanes and 3 PLLs**




An example system using Gen 2 multiPHY IP is given in Figure 34 which has one VAA_PLL package ball through a flip chip package feeding 5 byte lanes, each with a PVAA_PLL cell and its own bump, two byte lanes share one PLL except for the last byte lane which has its own PLL. The 5 VAA_PLL bumps in the package are routed together and connect to one ball on the package. The VAA_PLL and VSSQ bumps have RDL of about 0.26 Ohms each connected to the PVAA_PLL and PVSSQ cells in close proximity to each other. The PLL have another 0.26 Ohm max routing resistance to the PLL.

The PLLs for Gen 2 MultiPHY use 12mA at 800MHz (DDR3 -1600Mbps system). The IO RX will use about 1.5mA each (DC + AC current calculated from power numbers in the databook) in DDR3-1600 mode. Total current for the IO RX will be 12 x 1.5mA = 18mA. Total current for 5 byte lanes + 3 PLLs will be (5 x 18mA ) + (3 x 12mA) = 126mA.

Since the VAA_PLL supply is not shared on the PCB, a series filter element such as the ferrite bead will not be required. Assuming the Voltage regulator on the PCB takes 5% of the IR budget, 5% is left for package and on die routing. Assuming the package IR drop is 1.0%, on die IR drop is allowed to be 4% or 1.8V x 4% = 72mV. IR drop through the bumps and RDL will be (18mA *2 + 12mA) x (0.26ohms x 2) = 25mV. IR drop to the PLL will be an additional (0.26ohms 12mA) = 3.1mV for a total of 25mV + 3.1mV = 28.1mV which is less than the limit (72mV) as an example.
The byte lanes require one PVAA_PLL cell which is located in the center of the byte lane to balance IR drop along the MVAA_PLL bus to the signal IO cells. Each MVAA_PLL bus has a branch of 6 IO cells. The resistance from PVAA_PLL pad to MVAA_PLL bus is 0.292 ohms (Gen 2 multiPHY databook). The horizontal bus resistance per IO cell is 0.292ohms (Gen 2 multiPHY databook). Assuming 2:1:1 signal to power to Ground IO cells so each signal IO is 3 cells away from each other.

## 5.3.1 Example IR drop Calculation in IO ring

IR drop from PVAA_PLL pad to MVAA_PLL bus = 18mA X 0.292ohms = 5mV
IR drop MVAA_PLL bus from PVAA_PLL cell to sixth signal IO cell =
(6 x 1.5mA) x (0.292ohms X 3 IO cells) +

(5 x 1.5mA) x (0.292ohms X 3 IO cells) +
(4 x 1.5mA) x (0.292ohms X 3 IO cells) +
(3 x 1.5mA) x (0.292ohms X 3 IO cells) +
(2 x 1.5mA) x (0.292ohms X 3 IO cells) +
(1 x 1.5mA) x (0.292ohms X 3 IO cells)
= 27.6mV

Total IR drop from PVAA_PLL bump to last IO cell = 25mV + 5mV + 27.6mV = 57.6mV
This is less than 72mV limit.

More of the budget could be assigned to allow the package or on die IR drop to increase for example.
The VAA_PLL supply net may be routed as a wide signal net trace with adjacent ground net trace which can be used as shielding, and should be spaced away from other noisy nets 3 times the height above the reference plane. Some of the byte lanes may have a VAA_PLL IO cell in the IO ring. Some of these VAA_PLL nets in the package may be combined and routed to a single package ball. It is recommended that no more than 5 PLLs VAA_PLL nets be combined to one package ball.

For example, if the PLLs are operating in DDR3-1600 mode (clock = 800MHz) for Gen2 multiPHY, each PLL draws a maximum of 12mA each on VAA_PLL. The IO RX draw 18mA for one byte on VAA_PLL. For one branch of the VAA_PLL supply network to a PLL it has a current draw of 12mA + (2 x 18mA) = 48mA. The max AC supply noise at the PLL should be limited to +/-2.5% nominal VAA_PLL (from databook) or +/-2.5% of 1.8V = +/-45mV or 90mVpp. To a first order the target impedance should be 90mV/(48mA) = 1.875 ohms.

Figure 35 shows the current draw of one byte lane of IO RX (green) and the current draw of a single PLL (gold). Note that the IO RX are switching a PRBS7 pattern and the IOs are powered up (10 bits wide) and down (10 bits wide) as with alternating write and read bursts where the IO RX are powered down during write bursts (PDR=1).

**Figure 35: Current profiles of one byte lane IO RX (green) and one PLL (gold) each**

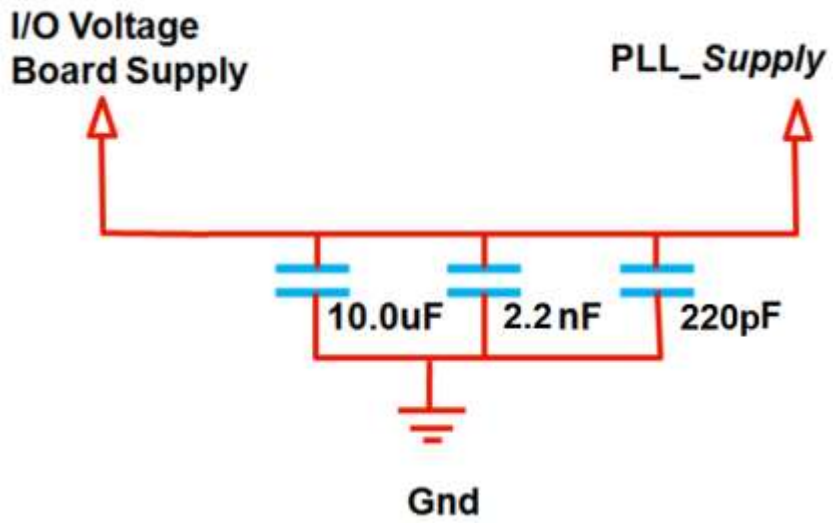

Examining the VAA_PLL power supply network in the frequency domain (Figure 36) reveals that target impedance can be met with the following decoupling caps.

PCB decoupling caps: one 10uF, one 2.2nF, one 220pF

On die decoupling caps at IO on VAA_PLL to VSSQ supply net: 10pF capacitance from VAA_PLL to VSSQ per signal IO. For example, a byte lane with 11 IOs would require 11 X 10pF/IO = 110pF.

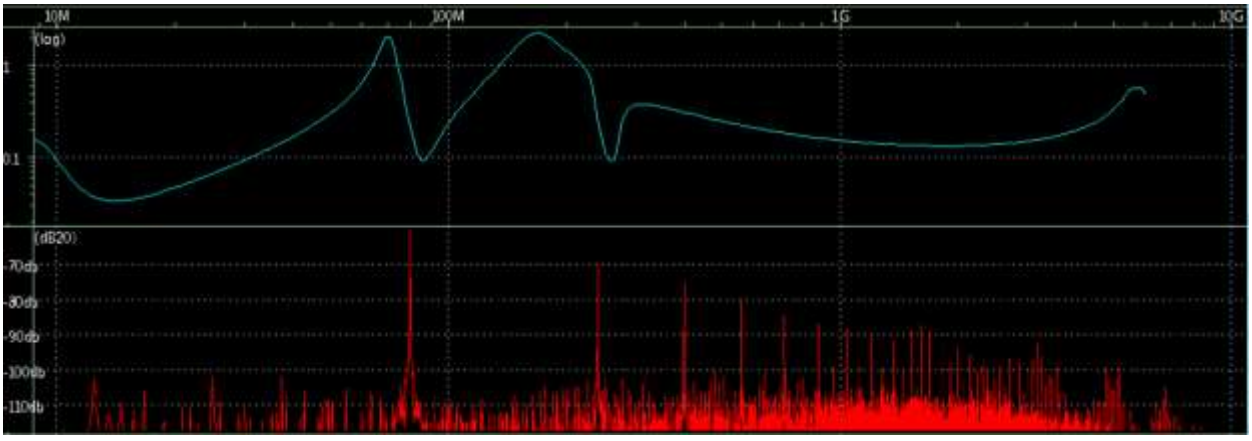
The 10pF/IO on die decap is required to reduce the switching noise on the VAA_PLL net due to the IO RX circuits. The VAA_PLL decap cells need to be added in the space between/around the PHY blocks and the IO cells or in between IO cells. The decap cells should be strapped to the PVAA_PLL bus of the IO cells in a direct manner as possible in higher die layers.

**Figure 36: PCB filter for VAA_PLL for RX IO and PLL Not shared on PCB**




Only one set of PCB decoupling caps is required per VAA_PLL package ball with the smallest 220pF cap closest to the package ball. The on-die decoupling (1.8V compatible) is required right at the PLLs for each PLL as shown in Figure 34.

**Figure 37: VAA_PLL Impedance and VAA_PLL current FFT vs. frequency plots**




The Impedance plot for VAA_PLL (blue) and the FFT of the VAA_PLL current for the IO RX and PLL (red) are shown in Figure 37. Note the largest current spike is from the IO Rx circuits switching on and off every 10 bit periods which is 625psec x 10 bits x 2 = 12.5 nsec or a frequency of 80MHz.

## PLL and IO RX VAA_PLL Supplies – Shared on PCB

Reusing the example system using Gen 2 multiPHY IP is given in Figure 34 which has one VAA_PLL package ball through a flip chip package feeding 5 byte lanes, each with a PVAA_PLL cell and its own bump, two byte lanes share one PLL except for the last byte lane which has its own PLL. The 5 VAA_PLL bumps in the package are routed together and connect to one ball on the package. The VAA_PLL and VSSQ bumps have RDL of about 0.26 Ohms each connected to the PVAA_PLL and PVSSQ cells in close proximity to each other. The PLL have another 0.26 Ohm max routing resistance to the PLL.

The PLLs for Gen 2 MultiPHY use 12mA at 800MHz (DDR3 -1600Mbps system). The IO RX will use about 1.5mA each (DC + AC current calculated from power numbers in the databook) in DDR3-1600 mode. Total current for the IO RX will be 12 x 1.5mA = 18mA. Total current for 5 byte lanes + 3 PLLs will be (5 x 18mA ) + (3 x 12mA) = 126mA.

The VAA_PLL supply is shared on the PCB, so a series ferrite bead will be required. In this case a ferrite was chosen with a lower DC resistance with almost the same frequency response as the bead used in the PLL only – Shared VAA_PLL supply on PCB. A BLM18SG121TN1 ferrite has DC resistance of 0.025 ohm in a slighter bigger 0603 package. IR drop through the bead will be 126mA x 0.025 ohms = 3.2mV. This is 3.2mV/1.8V = 0.18% of the IR drop budget. Assuming the Voltage regulator on the PCB takes 5% of the IR budget, 5% is left for ferrite bead, package, and on die routing. Assuming the package IR drop is 1.0%, on die IR drop is allowed to be 5% - 0.18% - 1.0% = 3.82% or 1.8V x 3.82% = 68.8mV. IR drop through the bumps and RDL will be (18mA *2 + 12mA) x (0.26ohms x 2) = 25mV. IR drop to the PLL will be an additional (0.26ohms x 12mA) = 3.1mV for a total of 25mV + 3.1mV = 28.1mV which is less than the limit (68.8mV).

The byte lanes require one PVAA_PLL cell which is located in the center of the byte lane to balance IR drop along the MVAA_PLL bus to the signal IO cells. Each MVAA_PLL bus has a branch of 6 IO cells. The resistance from PVAA_PLL pad to MVAA_PLL bus is 0.292 ohms (Gen 2 multiPHY databook). The horizontal bus resistance per IO cell is 0.292ohms (Gen 2 multiPHY databook). Assuming 2:1:1 signal to power to Ground IO cells so each signal IO is 3 cells away from each other.
IR drop from PVAA_PLL pad to MVAA_PLL bus = 18mA X 0.292ohms = 5mV
IR drop MVAA_PLL bus from PVAA_PLL cell to sixth signal IO cell =
(6 x 1.5mA) x (0.292ohms X 3 IO cells) +
(5 x 1.5mA) x (0.292ohms X 3 IO cells) +
(4 x 1.5mA) x (0.292ohms X 3 IO cells) +
(3 x 1.5mA) x (0.292ohms X 3 IO cells) +
(2 x 1.5mA) x (0.292ohms X 3 IO cells) +
(1 x 1.5mA) x (0.292ohms X 3 IO cells)
= 27.6mV

Total IR drop from PVAA_PLL bump to last IO cell = 25mV + 5mV + 27.6mV = 57.6mV
This is less than 68.6mV limit.

The same PCB decoupling caps and on die decoupling caps should be used as was recommended for the “PLL and IO RX VAA_PLL Supplies – Not shared on PCB” case.
PCB decoupling caps: one 10uF, one 2.2nF, one 220pF

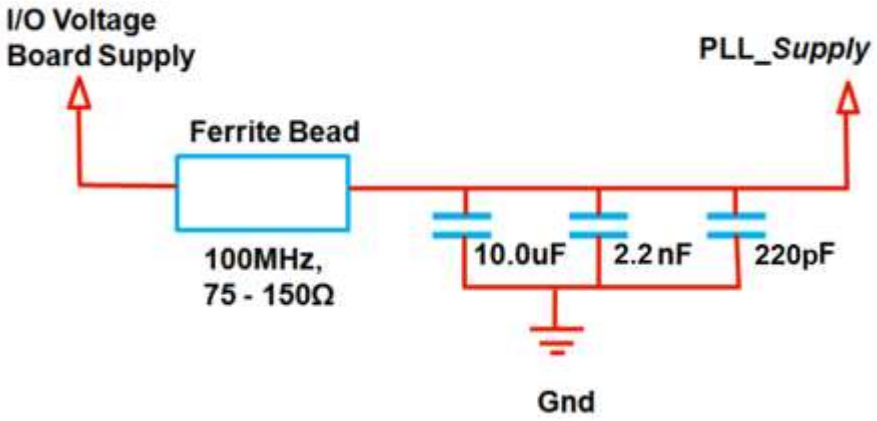
On die decoupling caps at IO on VAA_PLL to VSSQ supply net: 10pF capacitance from VAA_PLL to VSSQ per signal IO. For example, a byte lane with 11 IOs would require 11 X 10pF/IO = 110pF.

The 10pF/IO on die decap is required to reduce the switching noise on the VAA_PLL net due to the IO RX circuits. The VAA_PLL decap cells need to be added in the space between/around the PHY blocks and the IO cells or in between IO

cells. The decap cells should be strapped to the PVAA_PLL bus of the IO cells in a direct manner as possible in higher die layers.

The PCB filter circuit is shown in Figure 38.

**Figure 38: PCB filter for PLL and IO RX VAA_PLL Supplies - Shared on PCB**




## 5.4 PLL and IO RX VAA_PLL Supplies – PDR=OFF constantly

In DDR systems where VAA_PLL supplies are used for both PLLs and IO RX, and, power savings are not required for IO RX power, the PDR pin of the IO RX can be left = 0 which leaves the IO RX powered up all the time. In this case the ac noise on the VAA_PLL supply due to IO RX switching currents is considerably reduced. This is because only IO RX AC currents are switched, not AC and DC currents. For this system, no extra on –die VAA_PLL decoupling capacitance is required other than what is currently provided in the signal and power cells of the IO ring to sufficiently reduce the VAA_PLL supply noise to acceptable levels.

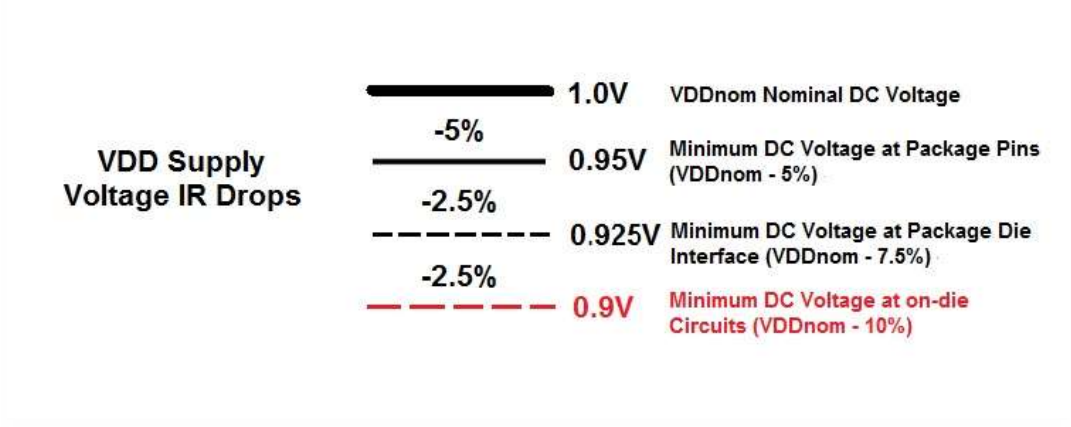
The guidelines established in the previous two sections for on PCB filter and bead in the case of “PLL and IO RX VAA_PLL Supplies – Shared on PCB” and for PCB filter in the case of “PLL and IO RX VAA_PLL Supplies – Not Shared on PCB” should still be adhered to even if PDR=0 constantly.

Note in all cases data from the proper databook should be used for the exact IP in the exact operating modes as required for a particular system. Both frequency domain and transient power supply network analysis should be performed to ensure the power network provides adequate performance.

# 6 Static DC or IR Drop

Static DC current voltage drop or IR drop needs to be considered to make sure adequate DC voltage is maintained at the circuits of the die. Usually the core VDD supply has the highest current demand and the lowest supply voltage (1.0V for example) so it should be considered first, but all supply networks should be reviewed. The goal is to determine what maximum resistance can be tolerated through the package and on die interconnect to feed power to the circuits on die. The maximum RMS current is estimated from core circuit simulations or power consumption estimates. The minimum core power supply voltage at the chip package pins must be specified, which is typically -5% of the nominal supply voltage. So, for nominal core supply of 1.0V, -5% would give us 0.95V, for example. Typically, another -5% voltage drop is allowed for the supply to the on-die circuits for a total of -10% for on die supply. This would be 0.9V to the on die circuits of the core with the maximum RMS current of the die for that supply (we will assume 1A).

**Figure 39: IR Drop Budget**



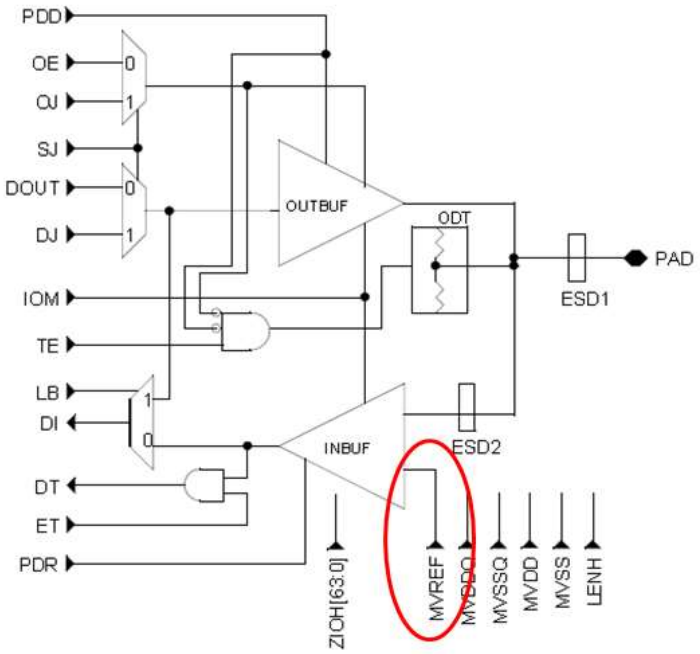

For IR drop, break the contributions into package and on-die interconnect. On die interconnect will include the losses from the bumps to the core power mesh and on die circuits in the case of flip chip. Ideally, give half the IR drop budget to the package (2.5% of 1.0V or 25mV) and half to the on die interconnect (another 25mV). Depending on the actual values that get divided between the package and on-die IR drop, one or the other can be allowed to take more of the budget if necessary as long as the total budget is met. Package loss is the resistance of all the metal interconnects for power and VSS nets (PCB to package vias from power planes, package balls, build up layer vias, Core vias, and bumps). A trial layout of power and ground nets with package planes and vias must be done to estimate the numbers of vias through each layer. The DC resistance for all these components is added up to see what the total value is (typically in a spreadsheet).

For a typical 40nm flip chip test chip, the package resistance for core power and ground nets is 9.62mΩ giving IR drop of about 10mV with 1.0Amp of current. This was deemed acceptable as it would give 40.38 mΩ to the on-die interconnect. On die interconnect was laid out to meet or beat this target.

## 6.1 Generating Vref and VTT

The DDR functional cells receive their inputs in a pseudo differential manner. Data signals determine their level with respect to a Vref signal which is equal to 0.5*VDDIO+/- 1%.

**Figure 40: Received Signals at Pad Referenced to the Input Vref Level**

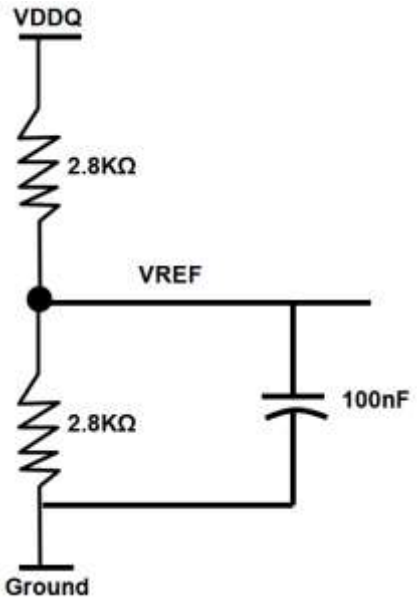



For DDR protocols DDR4, LPDDR3, and LPDDR4, VREF for the data must be variable to accommodate the different ODT impedances for the pull up termination. In these cases, the host will generate VREF internally. I some applications, like LPDDR3, the host can also create a Vref level to be delivered to the SDRAM.

For PHY products that do not support VREF generation, the reference voltage must be generated on the board. The Vref must track with the generated IO voltage. This is most commonly done with the regulator on the printed circuit board, though it can be done with the simple resistor divider shown Figure 41. This is simple, inexpensive and tracks voltage very well for lightly loaded nets.

Because dynamic noise is limited to +/- 2% of VREF, care must be taken when routing through the board and package. VREF is a very low current function. It should be treated as a signal rather than a power supply. To minimize DC drop, VREF etch should be a minimum of 20 mils wide. VREF should be routed close to a reference plane and should avoid any induced noise from active signals. A space to height above the reference plane ratio of <3:1 between Vref and the active signals is recommended.

**Figure 41: Vref Generated with Resistor Divider Network.**




VTT must track closely with Vref, however the resistor divider network will probably not be able not be able to support the current requirements for VTT termination. While Vref typically draws less than 3 mA of current, switching currents on VTT can be substantial, 500 mA or more. VTT power should be supplied to PCB circuits with low impedance power planes from the regulator. Local ceramic decoupling caps should be used to filter noise at the VTT terminations on PCB.

It is advised that a voltage regulator be used to generate VDDIO and VTT to manage the current requirements. Since VTT must track VREF(CA), it adheres to the same +/- 2% noise specification, substantial decoupling must be employed.