Design Pricing Matrix

Design Level Definitions

- Level 0 Miscellaneous and Minimal Design Involvement
  - ECO's and DRQ's requiring Text or material changes, strip outline changes, minor updates, STATS ChipPAC incurred errors, etc
  - DRQ's for Customer provided design with Drawing generation and/or Review, etc
  - Less than 1 day design time
- Level 1 Low complexity, standard HVM design and assembly rules
  - Less than 1 week design time
- Level 2 Moderate complexity, standard to minimum HVM design and assembly rules
  - Average 1 week design time
- Level 3 High complexity, minimum HVM to possible standard LVM design and assembly rules
  - Fairly straight forward design
  - Usually less than 2 weeks design time
- Level 4 Very high complexity and not straight forward. LVM to AVM design and assembly rules
  - This level is used for designs that exceed Level 3 conditions and are expected to have a high level of involvement between STATS ChipPAC and the Customer
  - Over 2 weeks design time
- Level 5 Hourly rate intended for special projects
  - This level is used for design efforts that are not covered by Levels 1 through 4

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Array Product Design Service Pricing

Pricing ($US)	PBGA, EBGA, TBGA-I, TBGA-II, FBGA	PBGA-SIP, FBGA-SiP, Multi-Die, Flip Chip	PiP/ PoP
Level 0	Refer to Page 9	Refer to Page 9	Refer to Page 9
Level 1	2,500	3,000	3,000
Level 2	5,000	6,000	6,500
Level 3	7,500	9,000	10,000
Level 4	10,000+	14,000+	15,000+
Level 5	15,000+	20,000+	20,000+

Pricings shown are design center recommendations and may be adjusted per project by mutual agreement between sales and design center management.

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Lead Frame Product Design Service Pricing

Pricing ($US)	All Lead Frames
Level 0	Refer to Page 9
Level 1	1,000
Level 2	2,500

- **Level 1** -- Low Lead Counts Design (<100)
- **Level 2** -- High Lead Counts Design (>100)

Pricings shown are design center recommendations and may be adjusted per project by mutual agreement between sales and design center management.

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Wafer Bump Design Service Pricing

Pricing ($US)	Wafer Bump (exclusive IPD / eWLB)
Level 1	500

- Level 1 -- Mask requiring Panelization and Verification

IPD / eWLB Product Design Service Pricing

IPD/ eWLB product design pricing is to be referred to Page 8, Page 23 and 24 for quotation

Pricings shown are design center recommendations and may be adjusted per project by mutual agreement between sales and design center management.

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Wafer Bump (eWLB / WLB) Design Service Pricing

Pricing ($US)	eWLB / WLB
Level 0	Refer to Page 9
Level 1	1,000
Level 2	2,000

- Level 1 -- Low Complexity Design
- Level 2 -- Medium Complexity Design

eWLB cum IPD Product Design Service Pricing
The design pricing is to be the price shown above plus the pricing of referred to Page 22 and 23 for quotation

Pricings shown are design center recommendations and may be adjusted per project by mutual agreement between sales and design center management.

Other Product Design Service Pricing

Customer Provided Designs

No charge for customer provided designs in general as long as SC rules are followed and no change is required or requested.

In the event that the customer provided design is only partially routed or requires effort involved, the designer will assess the project and determine the "Level" that best matches the amount of work needed to complete the project.

Re-Design and Re-Analyses

Pricing includes one re-design due to customer changes. Subsequent changes will be subject to re-quote.

Design "Modifications" under new Design Requests will be individually reviewed and assigned a "Level" that best matches the complexity of changes.

Additional Notes On Design Service Pricing

Service charges may be used as leverage to encourage HVM – ie: if the customer does HVM with SC, we would waive the charges. But, if the customer does not do HVM, then we can back-charge for the services.

All SC assisted designs will start at "Level 1" pricing, and can be adjusted accordingly.

Other Product Design Service Pricing

Miscellaneous Service Pricing

Level 0 (zero) Pricing:

- No design charges ($0) will be applied for minor updates like text changes or spelling errors.
- No design charges ($0) will be incurred for fixing errors caused by SC.
- Depending on the amount of time needed to create, update, or modify minor requests, whether DRQ or ECO, a dollar amount of $0 or $500 for items with less than 8 hours of work, or $1K per day may be applied for the service. This will be determined at the time of initial assessment and with the site manager or designated persons approval.

PBGA (Single Die)

- Level 1 -- Open tooled, unrestricted route.
  - -- Less than 300 lead count.
  - -- Die size is less than 25% of board area.
  - -- Wire bond fingers fall inside the inner row of solder balls.
  - -- Two layer substrate.
  - -- 1.27mm solder ball pitch minimum.

- Level 2 -- Clean net list with some customer specific requests.
  - -- Layout is symmetric with direct routes from die to ball pad.
  - -- Up to two split power and ground rings.
  - -- Die may extend over the first inner row of solder balls.
  - -- Two or four layer design with some shielded and matched traces.
  - -- Up to full array, 1.0mm to 1.27mm solder ball pitch.

- Level 3 -- Difficult interconnect with conflicting routing requirements.
  - -- Fingers may fall over second inner rows of solder balls.
  - -- High solder ball count.
  - -- Two to six layer design with some shielded and matched traces.
  - -- Inner layer trace and plane routing.
  - -- Multiple split power and ground rings.
  - -- Explicit electrical requirements that may limit trace routing options.
  - -- Full solder ball array or large package.

- Level 4 -- Unknown interconnect, restricted route.
  - -- Advanced electrical, mechanical, and thermal requirements.
  - -- Die layout and passive components developed at same time as package.
  - -- Multi-layer substrate using advanced rules.
  - -- Undefined requirements from customer until package feasibility is more defined.

- Level 5 -- Special projects
  - -- Research and development needed to define package.
  - -- Component materials not matching standard technologies.
  - -- Substrate materials not matching standard or known practices.
  - -- Embedded passives, unique routing strategies, unique array patterns.

EBGA (Single Die)

- Level 1 -- Open tooled, unrestricted route.
  - -- Less than 400 lead count.
  - -- Two layer substrate.
  - -- 1.27mm solder ball pitch minimum.
- Level 2 -- Clean net list with some customer specific requests.
  - -- Layout is symmetric with direct routes from die to ball pad.
  - -- Up to two split power and ground rings.
  - -- Moderate to high I/O count.
  - -- Standard HVM rules for die pad and bond finger pitch.
  - -- Large or small die size with respect to package substrate dimensions.
- Level 3 -- Difficult interconnect with conflicting routing requirements.
  - -- Large or small die size with respect to package substrate dimensions.
  - -- Tight HMV rules - staggered die pad and bond finger pitch.
  - -- High lead or I/O count, 1.0mm solder ball pitch.
  - -- Multiple layers (2-8) with some shielded and matched traces.
  - -- Inner layer trace and plane routing.
  - -- Explicit electrical requirements that may limit trace routing options
- Level 4 -- Unknown interconnect, restricted route.
  - -- Advanced electrical, mechanical, and thermal requirements.
  - -- Die layout and passive components developed at same time as package.
  - -- Multi-layer substrate using advanced rules.
  - -- Undefined requirements from customer until package feasibility is more defined.
- Level 5 -- Special projects
  - -- Research and development needed to define package.
  - -- Component materials not matching standard technologies.
  - -- Substrate materials not matching standard or known practices.
  - -- Embedded passives, unique routing strategies, unique array patterns.

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TBGA-I and TBGA-II

- Level 1 -- Open tooled, unrestricted route.
  - -- Moderate lead count
  - -- Single metal layer
- Level 2 -- Clean net list with some customer specific requests.
  - -- Layout is symmetric with direct routes from die-to-solder ball.
  - -- Large die size with respect to package substrate dimensions.
  - -- Single metal layer on tape, silver plating on stiffener for wire bonding and solder ball attach.
- Level 3 -- Difficult interconnect with conflicting routing requirements.
  - -- High solder ball count.
  - -- Explicit electrical requirements that may limit trace routing options.
  - -- Large die size with respect to package substrate dimensions.
  - -- Staggered die pads in tight die pad pitch – minimum HVM rules.
- Level 4 -- Unknown interconnect, restricted route.
  - -- Advanced electrical, mechanical, and thermal requirements.
  - -- Die layout and passive components developed at same time as package.
  - -- Multi-layer substrate using advanced rules.
  - -- Undefined requirements from customer until package feasibility is more defined.
- Level 5 -- Special projects
  - -- Research and development needed to define package.
  - -- Component materials not matching standard technologies.
  - -- Substrate materials not matching standard or known practices.
  - -- Embedded passives, unique routing strategies, unique array patterns.

FBGA

- Level 1
  -- Open tooled, unrestricted route.
  -- Low solder ball count (less than 200).
- Level 2
  -- Clean net list with some customer specific requests.
  -- Layout is symmetric with direct routes from die-to-solder ball.
  -- Two or four layer design with some shielded and matched traces.
- Level 3
  -- Difficult interconnect with conflicting routing requirements.
  -- High lead count.
  -- Two or four layer design with some shielded and matched traces.
  -- Explicit electrical requirements that may limit trace routing options
- Level 4
  -- Unknown interconnect, restricted route.
  -- Advanced electrical, mechanical, and thermal requirements.
  -- Die layout and passive components developed at same time as package.
  -- Multi-layer substrate using advanced rules.
  -- Undefined requirements from customer until package feasibility is more defined.
- Level 5
  -- Special projects
  -- Research and development needed to define package.
  -- Component materials not matching standard technologies.
  -- Substrate materials not matching standard or known practices.
  -- Embedded passives, unique routing strategies, unique array patterns.

PBGA-SIP / Multi-Die / Flip Chip

- Level 1 -- Clean net list with some customer specific requests.
  - -- Layout is symmetric with direct routes from die-to-die and die-to-solder ball.
  - -- Two die max. No passives. 2 Layer.
- Level 2 -- Moderately complex net list with customer specific requirements.
  - -- Up to 4 layers.
  - -- Die & passives not to exceed 35% of total package area.
- Level 3 -- Difficult interconnect with conflicting routing requirements.
  - -- High lead count.
  - -- More then 4 layers.
  - -- Explicit electrical requirements that may limit trace routing options.
  - -- Die & passives exceed 35% of total package area.
- Level 4 -- Unknown interconnect, restricted route.
  - -- Advanced electrical, mechanical, and thermal requirements.
  - -- Die layout and passive components developed at same time as package.
  - -- Multi-layer substrate using advanced rules.
  - -- Undefined requirements from customer until package feasibility is more defined.
- Level 5 -- Special projects
  - -- Research and development needed to define package.
  - -- Component materials not matching standard technologies.
  - -- Substrate materials not matching standard or known practices.
  - -- Embedded passives, unique routing strategies, unique array patterns.

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FBGA-SIP / Multi-Die

- Level 1 -- Clean net list with some customer specific requests.
  - -- Layout is symmetric with direct routes from die-to-die and die-to-solder ball.
  - -- Two die max. No passives. 2 Layer.
- Level 2 -- Moderately complex net list with customer specific requirements.
  - -- Up to 4 layers.
  - -- Die & passives not to exceed 35% of total package area.
- Level 3 -- Difficult interconnect with conflicting routing requirements.
  - -- High lead count.
  - -- More then 4 layers.
  - -- Explicit electrical requirements that may limit trace routing options.
  - -- Die & passives exceed 35% of total package area.
- Level 4 -- Unknown interconnect, restricted route.
  - -- Advanced electrical, mechanical, and thermal requirements.
  - -- Die layout and passive components developed at same time as package.
  - -- Multi-layer substrate using advanced rules.
  - -- Undefined requirements from customer until package feasibility is more defined.
- Level 5 -- Special projects
  - -- Research and development needed to define package.
  - -- Component materials not matching standard technologies.
  - -- Substrate materials not matching standard or known practices.
  - -- Embedded passives, unique routing strategies, unique array patterns.

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PiP / PoP

- Level 1 -- Clean net list with some customer specific requests.
  - -- Layout is symmetric with direct routes from did-to-die and die-to-solder ball.
  - -- Low solder ball count (less than 600).
  - -- No redistribution necessary.
  - -- Two or four layers which may include power and ground planes.
- Level 2 -- Two or four layer design with some shielded and matched traces.
  - -- Full array, 1.27mm or 1.0mm solder ball pitch.
  - -- Mid range solder ball count (600 to 1000).
  - -- Four layer routing with buried and blind vias.
  - -- Inner layer trace routing.
  - -- Multiple chip package.
- Level 3 -- Difficult interconnect with conflicting routing requirements.
  - -- High solder ball count (greater than 1000).
  - -- Greater than four layer routing with buried and blind vias.
  - -- Inner layer trace routing.
  - -- Explicit electrical requirements that may limit trace routing options.
  - -- Full solder ball array or large package.
- Level 4 -- Unknown interconnect, restricted route.
  - -- Advanced electrical, mechanical, and thermal requirements.
  - -- Die layout and passive components developed at same time as package.
  - -- Multi-layer substrate using advanced rules.
  - -- Undefined requirements from customer until package feasibility is more defined.
- Level 5 -- Special projects
  - -- Research and development needed to define package.
  - -- Component materials not matching standard technologies.
  - -- Substrate materials not matching standard or known practices.
  - -- Embedded passives, unique routing strategies, unique array patterns.

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