SYNOPSYS®

DesignWare Cores DDR4 multiPHY Interconnect Signal and Power Integrity Guidelines

Application Note

DWC DDR4 multiPHY Signal Integrity Application Note

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Revision History

Version	Date	Note
1.0	Dec. 16, 2015	Initial release
1.1	April 16, 2016	Added Note on terminating multiple DDR4 DIMMs.
1.2	August 26, 2016	Added section on Read Post-Amble glitch
1.3	September 2016	Editorial changes.
1.4	March 2017	Editorial updates.
1.5	April 2017	Removed references to retired generic signaling document

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Introduction

This document provides general guidance for all the signaling protocols supported by the DDR4 MultiPHY IP. This application note applies to all the process nodes for which the DDR4 MultiPHY IP is available.

In this document the user will find:

An outline of the signal and power integrity support Synopsys can provide for this IP.
A discussion of the JEDEC protocols covered by this IP.
Routing and implementation guidelines specific to the supported protocols.
Example Timing budgets for all the protocols supported by this IP.

- *These are example budgets for a specific process. The values in the budget are very close to what can be expected for any particular process node.*

Review Services and Signal Integrity Support

Synopsys encourages all customers to take advantage of the visual review services we offer as part of any DDR PHY license. These services include, but are not limited to, the following:

- IO ring review,
- Floorplan review,
- SoC layout (GDSII) review,
- Package design review,
- PCB design review,
- Signaling Environment Review.

These reviews, conducted early in the design process, are extremely effective in catching potential problems while they can be easily remedied. To begin any such review, please file a SolvNet case requesting the review.

In addition to the review services included with the PHY license, Synopsys offers interface specific signal integrity simulation support. This is a fee based service offered to support the signal and power integrity needs of our customers. This is a flexible service offered to support our customer's unique needs. Please contact your Synopsys representative for more information regarding our SI/PI services.

Features and Benefits of Protocols Supported by the DDR4 MultiPHY

This section will discuss the JEDEC protocols that are supported by the DDR4 MultiPHY. A summary of supported protocols can be found in the table below. Additionally, sections with more in depth discussion of the features that each protocol supports are found in subsequent sections.

Protocol	DDR3	DDR3L (1.35V)	DDR3U (1.25V)	DDR4	LPDDR2	LPDDR3
Applications	PCs, Servers, Embedded	PCs, Servers, Embedded	PCs, Servers, Embedded	Servers, Networking	Mobile Electronics (PCB, PoP)	Mobile Electronics (PCB, PoP)
Maximum Data Rate [Mbps]	2133	1866	1600	3200	1066	2133
Minimum Data Rate [Mbps]	667	800	800	1333	200	333
Maximum Clock [MHz]	1067	933	800	1600	533	1067
Minimum Clock [Mhz]	333	400	400	667	100	167
Memory Density/Size	1Gb - 8Gb	1Gb - 8Gb	1Gb - 8Gb	2Gb - 16Gb	2Gb - 8Gb	4Gb - 32Gb
DIMMs available?	yes	yes	yes	yes	no	no
Prefetch	8N	8N	8N	8N	2N, 4N	8N
Width Options	x4, x8, x16	x4, x8, x16	x4, x8, x16	x4, x8, x16	x16, x32	x16, x32
Logic Levels (IO-VDDQ & Core-VDD) [V]	1.5	1.35	1.25	1.2	1.2	1.2
Thick Oxide Compatibility (VDDQ)	2.5V, 1.8V	1.5V	-	1.8V, 1.5V	1.8V, some 2.5V	1.8V, 1.5V
Logic Levels (VPP) [V]	-	-	-	2.5	-	-
IO Logic Type	Terminated SSTL, pseudo-differential w/ VREF	Terminated SSTL, pseudo-differential w/ VREF	Terminated SSTL, pseudo-differential w/ VREF	Terminated SSTL, pseudo-differential w/ VREF	Unterminated LVCMOS, pseudo-differential w/ VREF	Unterminated LVCMOS, pseudo-differential w/ VREF
Strobing	Differential	Differential	Differential	Differential	Differential	Differential
Delay Locked Loop in SDRAM	Yes	Yes	Yes	Yes	No	No
Clocking	Differential Clock	Differential Clock	Differential Clock	Differential Clock	Differential Clock	Differential Clock
Drive Strength Options	PVT Compensated Output Driver (34 Ω typical)	PVT Compensated Output Driver (34 Ω typical)	PVT Compensated Output Driver (34 Ω typical)	PVT Compensated Output Driver (34 Ω typical)	PVT Compensated Output Driver (34 Ω typical)	PVT Compensated Output Driver (34 Ω typical)
Termination Type/Options	PVT Compensated On Die Termination	PVT Compensated On Die Termination	PVT Compensated On Die Termination	PVT Compensated pull up termination on DQ/DQS	No Parallel Termination	No Parallel Termination / 120 or 240 ohms pullup to VDDQ On Die
DQ Termination Voltage	VTT = VDDQ/2	VTT = VDDQ/2	VTT = VDDQ/2	VDDQ	VTT = VDDQ/2	VDDQ
CA Termination Voltage	VTT = VDDQ/2	VTT = VDDQ/2	VTT = VDDQ/2	VTT = VDDQ/2	-	-
Read/Write Data Leveling	yes	yes	yes	yes	no	yes
Data Bus Rate	DDR	DDR	DDR	DDR	DDR	DDR
CA Bus Rate	SDR	SDR	SDR	SDR	DDR	DDR
DQ VREF	VREF pin	VREF pin	VREF pin	Internally Generated	VREF pin	VREF pin
CA VREF	VREF pin	VREF pin	VREF pin	VREF pin	VREF pin	VREF pin
Calibration Aids	Minimal	Minimal	Minimal	Many	Minimal	Minimal
OCD (Off-Chip Calibration) - ZQ	yes	yes	yes	yes	yes	yes
ODT (On-Die Termination)	yes	yes	yes	yes	no	yes
DQ Data Bus Invertion?	no	no	no	yes	no	no
DQ CRC Check	no	no	no	yes	no	no
CA Parity Check	no	no	no	yes	no	no
Boundary Scan	no	no	no	yes	no	no
Bank Groups	no	no	no	yes	no	no

Table 1: Summary of supported protocols

DDR4 Features and Benefits

The introduction of DDR4 was the first new memory standard to be introduced by JEDEC for non-mobile memory in 6 years. This section includes an overview of the major features introduced and their resulting benefits. At this writing an initial version of this standard DDR4 SDRAM has been released with many of the specifics still TBD. What is presented here is an introduction to the major concepts that define DDR4.

1.2V Pseudo-Open Drain Signaling

The signaling level for DDR4 is 1.2V+/- 5% for the I/O voltage. Termination for the data lanes is pull-up to VDDQ. This serves to shift the VREF above the 50% level as is typical with center-tapped termination techniques found in earlier DDR standards. The advantage of this is that only a "0" toggle will burn termination power, "1's" can be signaled without burning any termination power. Figure 1 illustrates how to calculate the initial VREF level based on the output impedance of the driver and the ODT value of the receiver termination. Note that intersymbol interference effects will shift the effective VREF higher. This is address with VREF DQ training. Command/Address/Control signals are still center-tapped and require termination to VTT which is 50% of VDDQ.

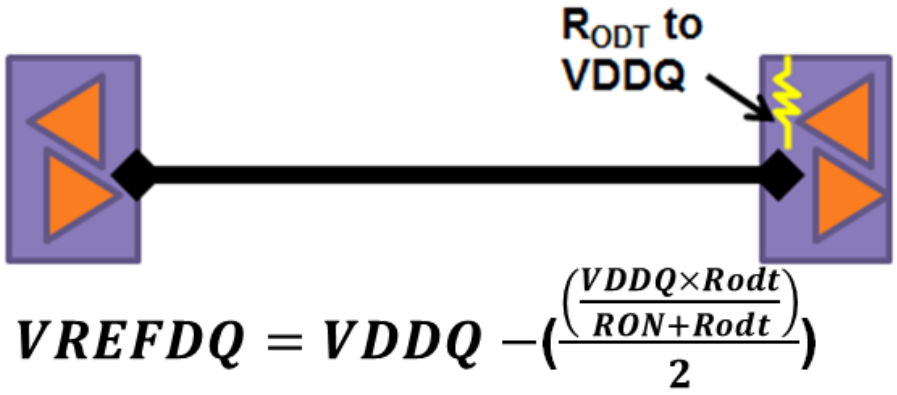

Figure 1: Data lanes implement pull-up termination to VDDQ (1.2V nominal).

BER Eye Characterization Techniques for DDR4

As DDR bit rates have been increasing, the impact of random jitter has become a more significant component in timing closure. The DDR4 standard is being written to accommodate Bit Error Rate techniques by defining the DQ receive parameters in terms of a data window instead of set up and hold specifications. Figure 2 illustrates this new window. As the specification is currently written, the window, 0.2UI in width and 136mV in height in this example, represents the needed window to support a BER of 1E-16. This specification is in its first release. Many changes and enhancements in this BER methodology will be included in the future.

The waveform in the figure is from the original release of the DDR4 standard. It is expected in the next specification release that the DJ and RJ components will not be separately defined. TdIVW will define a total opening required for a memory device to support a specified bit rate.

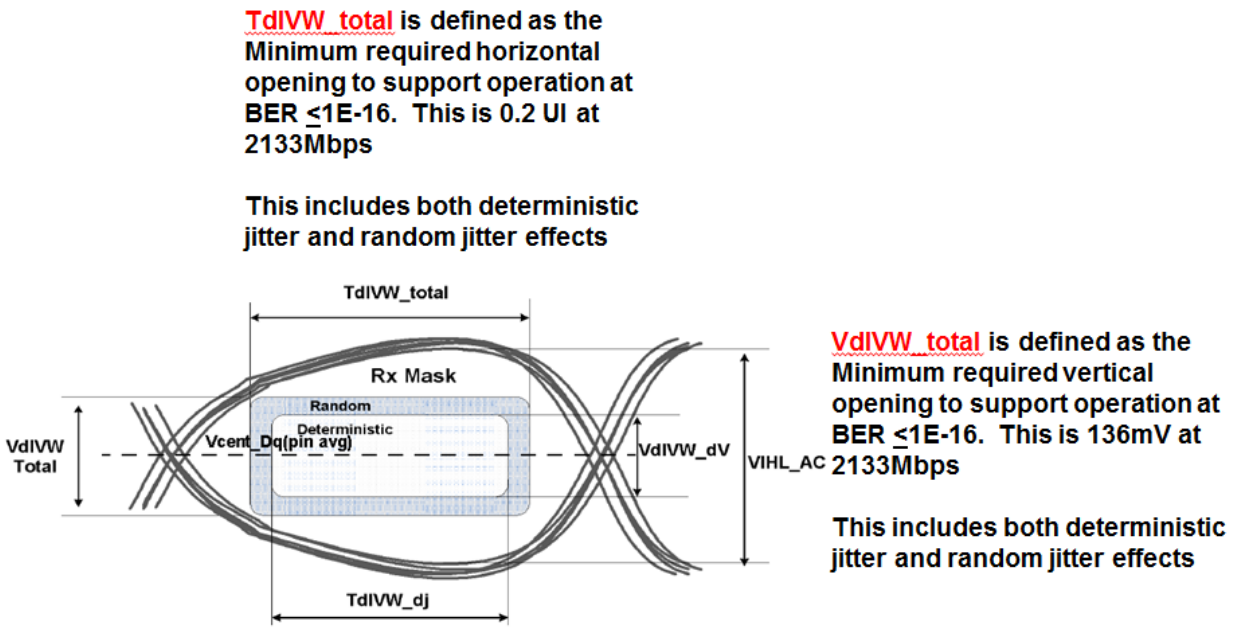

Figure 2: DQ Receiver data input valid window.

VREFDQ Training

Because the VREF level for DQ can vary by ODT level as described in Figure 1, VREF must be able to be trained to the correct level. Additionally, loading conditions will impact the available signal swing through inter-symbol interference effects. Figure 3 shows how heavier loading will reduce the signal swing and consequently require the VREF level to be shifted higher. The VREF training algorithm will allow the placement to be done within 0.8% of VDDQ accuracy. Training will settle to the average calculated Vref level across the byte lane. Since signal channel configurations can vary from byte lane to byte lane, training for different VREF levels between byte lanes is supported.

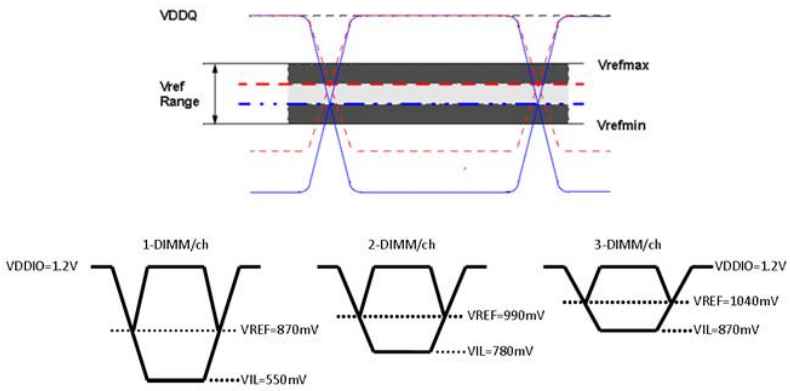

Figure 3: Vref Training optimizes the centering of VREF in the vertical scale.

Data Bus Inversion

Because there is no termination current when the pseudo-open drain link signals a "1", it is desirable to always signal more 1's than 0's across a byte lane. As shown in Table 2, whenever a pattern with more than 4 0's is launched in the right column, the data is inverted and then the DBI bit is set to 0. This DBI=0 bit tells the receiving element that the received byte must be inverted. DBI serves to reduce termination current by always signaling more 1's than 0's. Additionally, DBI helps to reduce the number of simultaneously switching outputs. Since no more than 4 bits can signal 0 at one time when DBI is implemented, less than ½ the byte lane will be switching in the same direction at any one time. While it is possible to have 4 bits switching high to low and 4 bits switching low to high, simultaneously, the result in this case will be very low switching current. DBI removes a significant amount of SSO noise from data transactions.

DQ[0:7] per UI	DBI	After Converting Data	# of "0" including DBI
0000_0000	0	1111_1111	1
0000_0001	0	1111_1110	2
0000_0011	0	1111_1100	3
0000_0111	0	1111_1000	4
0000_1111	1	0000_1111	4
0001_1111	1	0001_1111	3
0011_1111	1	0011_1111	2
0111_1111	1	0111_1111	1
1111_1111	1	1111_1111	0

Table 2: Data Bus Inversion patterns.

Gear Down Mode vs. 2T timing.

2T timing allows the user to double the available bit time for the Address and Command signals. This is especially helpful when heavy loading from multiple ranks causes erosion of the set

up time. It can also be useful in relaxing skew requirements in tightly packed PCB form factors found in enterprise applications.

Even with 2T timing, however, the control signals, CS#, ODT and CKE must still meet 1T timing, but their loading is constrained to 1 rank each.

Gear Down differs in that it also allows the Control signals to be operated with 2T bit times. Gear Down requires that the Controller and the SDRAM perform a handshake operation in order to agree on which clock edges to use to latch in commands.

DDR4 Alert_n Implementation

The Alert_n pin is an I/O signal driven by DDR4 SDRAM to signal to the host controller when the SDRAM detects an error on the DDR interface, or, is a signal driven by the host controller to the SDRAM during Connectivity test mode. This guideline covers 4 different system cases using Alert_n driven from SDRAM to host controller depending on the memory configurations used on the PCB:

Discrete SDRAM directly soldered on main PCB
UDIMM
RDIMM
LRDIMM

Discrete SDRAM directly soldered on main PCB

In this first case, discrete DDR4 SDRAM components are soldered directly to the main PCB that the host controller device resides on. The Alert_n signal should be routed similar to how an Address line would be routed as it needs to connect to all memory devices. For multi-rank systems, it is best to use a fly-by routing topology with minimal stubs from the main trace to individual SDRAM pins as shown in Figure 4.

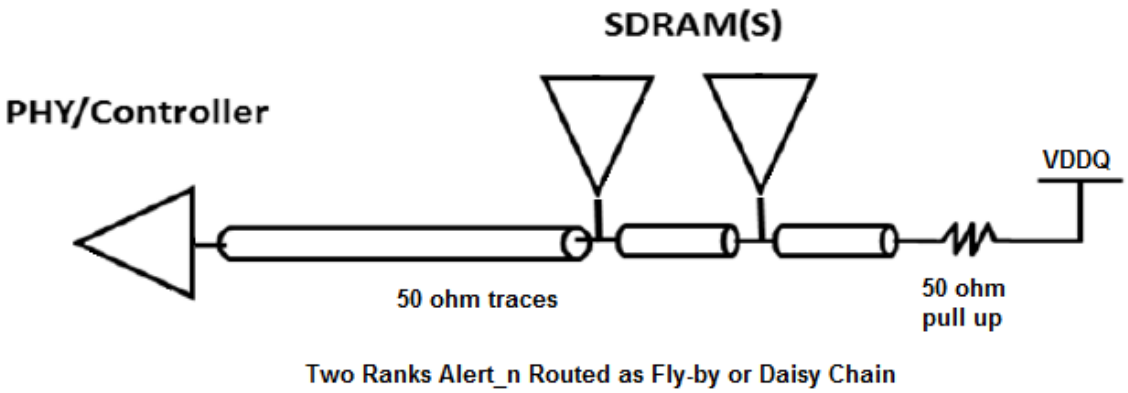

Figure 4: Alert_n signal routing on PCB for Discrete SDRAMs

The Alert_n net is driven by open drain SDRAM IO drivers and requires a 50 ohm pull up to VDDQ on the main board. The pull up resistor should be located at the end of the trace after the last SDRAM as indicated in the diagram. The host controller IO will be a PDDRIO type, and as an input will require a VREF voltage programmed for the middle of the voltage swing as determined by the SDRAM output drive strength (34 ohms) and the 50 ohm pull up resistor as in the calculation below.

$VREF_{ALERT\_N}$ = VDDQ x (1 – ((Rpu/(Ron + Rpu))/2) = VDDQ x (1 – ((50/(34 + 50))/2) = VDDQ x 0.702

For DDR4 VDDQ = 1.2V, therefore, $VREF_{ALERT\_N}$ = 1.2 x 0.702 = 0.843V

The host controller PDDRIO input cell should be configured as a high speed SSTL input with local ODT termination disabled.

UDIMM (Unbuffered DIMM)

For systems that use DDR4 UDIMM, the Alert_n signal is routed as a fly-by trace connecting all SDRAM open drain IO signal pins on one net to the DIMM edge connector. A 51 ohm pull up resistor to VDDQ resides at the very last SDRAM of the daisy chain (SDRAM routed farthest away from the edge connector when routing Command/Address signals in Figure 5).

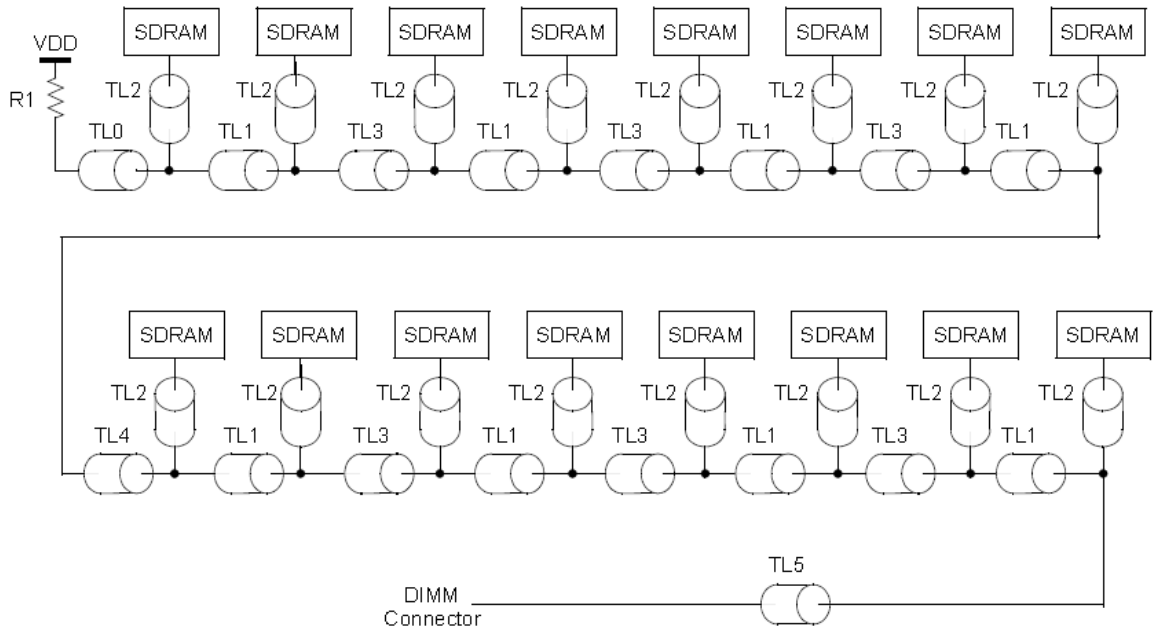

Figure 5: UDIMM Alert_n signal routing for 2 rank

For a single slot UDIMM system (Figure 3), a single 50 ohm trace should be routed from the UDIMM to the host controller Alert_n pin. The host controller IO will be a PDDRIO type, and as an input will require a VREF voltage programmed for the middle of the voltage swing as determined by the SDRAM output drive strength (34 ohms) and the 51 ohm pull up resistor as in the calculation below.

$VREF_{ALERT\_N}$ = VDDQ x (1 – ((Rpu/(Ron + Rpu))/2) = VDDQ x (1 - ((51/(34 + 51))/2) = VDDQ x 0.7

For DDR4 VDDQ = 1.2V, therefore, $VREF_{ALERT\_N}$ = 1.2 x 0.7 = 0.84V

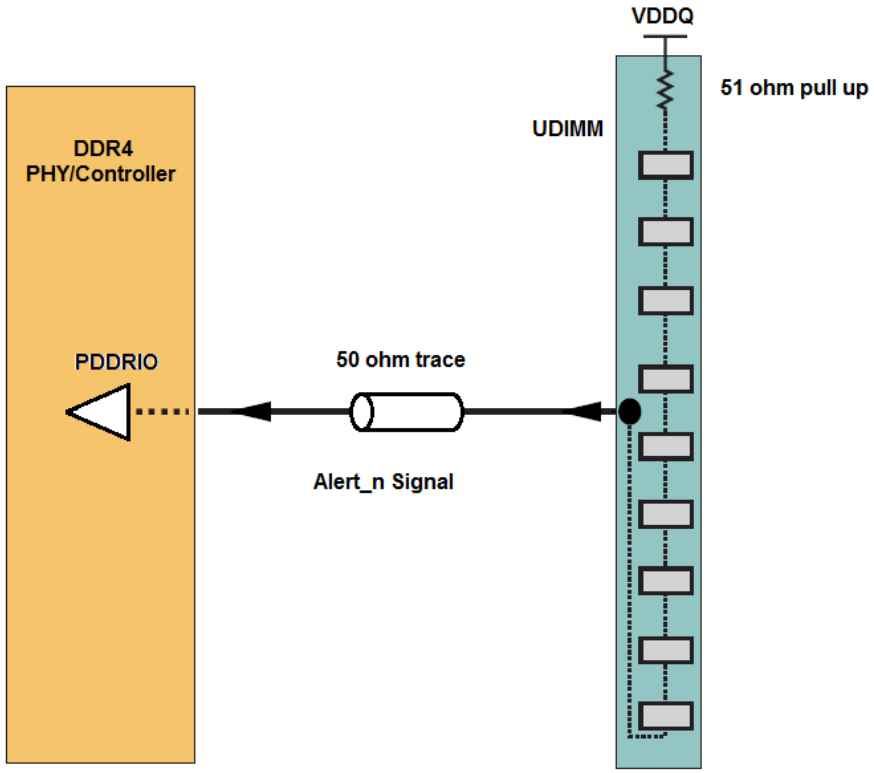

Figure 6: One slot UDIMM Alert_n signal routing

For a two slot UDIMM system (Figure 7) extra precaution needs to be taken because each UDIMM has its own 51 ohm pull up resistor to VDDQ so there will be two 51 ohm pull up resistors on Alert_n signal in parallel. This increases the Vol level that Alert_n reaches such that a higher Vref level is required for the PDDRIO IO receiver at the host controller for the signal to be received properly.

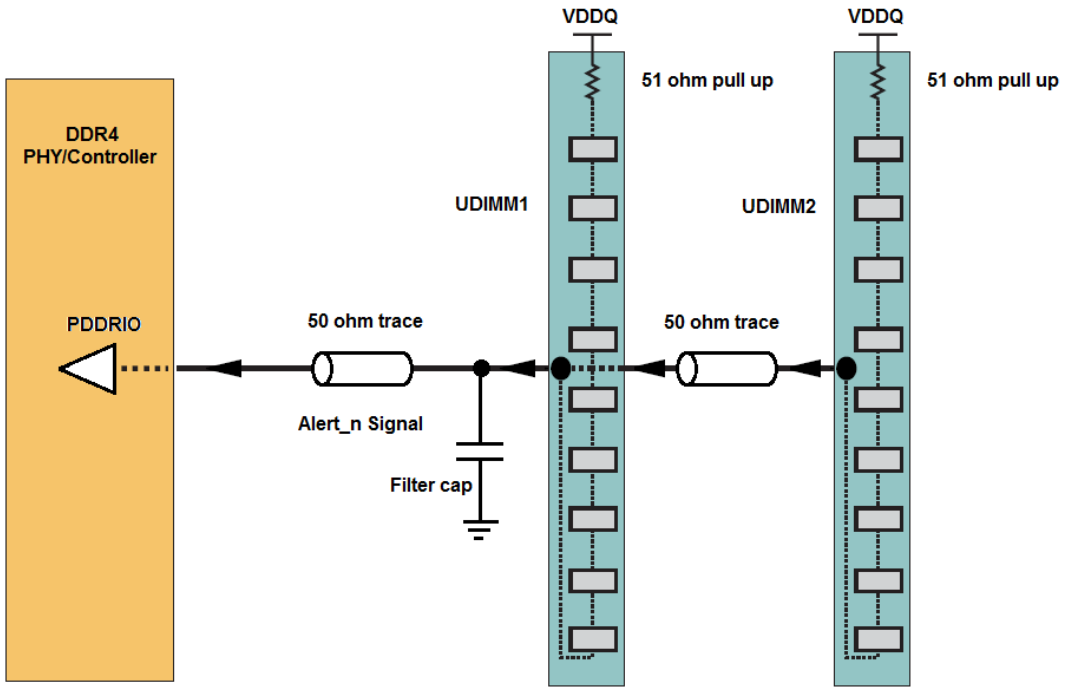

Figure 7: Two slot UDIMM Alert_n signal routing

The host controller IO will be a PDDRIO type, and as an input will require a VREF voltage programmed for the middle of the voltage swing as determined by the SDRAM output drive strength (34 ohms) and the two 51 ohm pull up resistors as in the calculation below.

$VREF_{ALERT\_N}$ = VDDQ x (1 - ((Rpu/(Ron + Rpu))/2) = VDDQ x (1 - ((51/2)/(34 + (51/2))/2) = VDDQ x 0.786

For DDR4 VDDQ = 1.2V, therefore, $VREF_{ALERT\_N}$ = 1.2 x 0.786 = 0.943V.

Due to fast edge rate of the SDRAM output drivers, the heavy distributed SDRAM IO capacitive loading, and long signal trace network, the alert_n signal arriving at the host controller IO input may suffer from reflections and non-monotonic edges as shown in Figure 8. The blue plot shows the edge glitches that occur at the host controller IO input due to reflections on the alert_n trace network. The Gold plot shows the host controller input IO on the core side – some glitches can be seen on the falling edge.

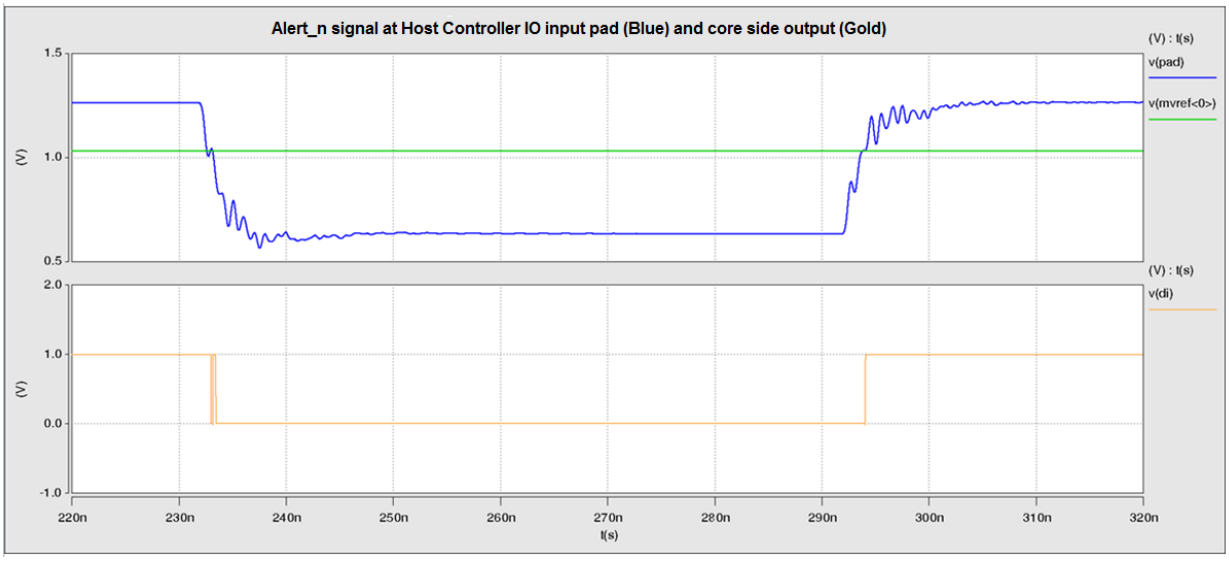

Figure 8: Alert_n input pad signal glitching

To filter the alert_n signal, a 18pF PCB surface mount capacitor is added to the alert_n trace on the main PCB at the first UDIMM connector as shown in Figure 4. This will eliminate non-monotonic edges at the controller IO input and glitches from reaching the core at the host.

The host controller PDDRIO input cell should be configured as a high speed SSTL input with local ODT termination disabled for both 1 slot and 2 slot systems.

RDIMM (Registered DIMM)

In systems using DDR4 RDIMM modules, each RDIMM has a register chip which receives the alert_n signals from all the SDRAM chips and then buffers it with open drain IO driver to the host controller. A 50 ohm trace is routed from the RDIMMs to the host controller Alert_n pin and a 50 ohm pull up resistor is required Figure 9 on the PCB located near the host controller to achieve the proper signal levels as shown in.

The host controller IO will be a PDDRIO type, and as an input will require a VREF voltage programmed for the middle of the voltage swing as determined by the RDIMM register output drive strength (34 ohms) and the 50 ohm pull up resistor as in the calculation below.

$$VREF_{ALERT\_N} = VDDQ \times (1 - (Rpu/(Ron + Rpu))/2) = VDDQ \times (1 - (50/(34 + 50))/2) = VDDQ \times 0.702$$

For DDR4 VDDQ = 1.2V, therefore, $VREF_{ALERT\_N} = 1.2 \times 0.702 = 0.843V$

The host controller PDDRIO input cell should be configured as a high speed SSTL input with local ODT termination disabled.

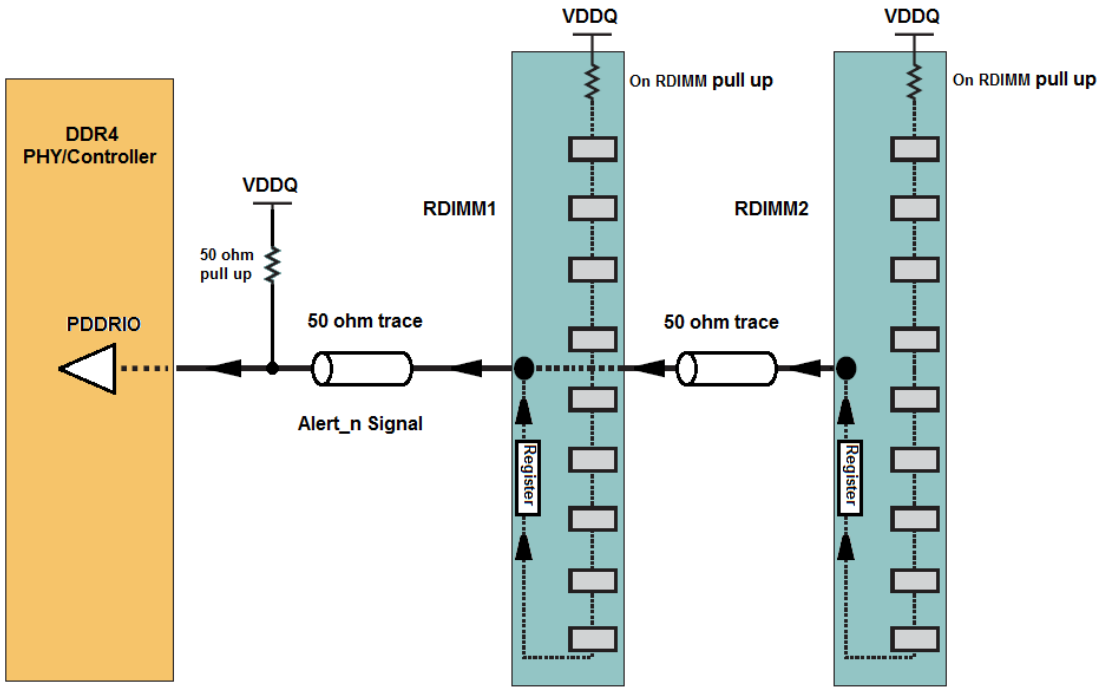

Figure 9: Two slot RDIMM Alert_n signal routing

LRDIMM (Load Reduced DIMM)

LRDIMMs use similar type register chips as the RDIMM so the same system recommendations apply to LRDIMMs as described in the section 1.1.3 for RDIMMs.

DDR3 and DDR3L Features and Benefits

DDR3 operates at a nominal voltage of 1.5V with a maximum bit rate of 2133Mbps. DDR3L is identical in terms of functionality, but operates at a nominal voltage of 1.35V with a top bit rate of 1866Mbps. The most significant feature added with DDR3/DDR3L was the support for Write Leveling which greatly improved the performance of the Command/Address/Control bus by enabling the use of Fly-By termination on unbuffered DIMMs. This is readily implemented on memory down applications as well.

Fly-By Termination

The DDR3 specification introduced write leveling functionality that allows Add/Cmd/Ctrl signals and CK/CK# signals to be routed as long daisy chains using fly-by termination. Support for this is found in specifications, DDR3, LPDDR3 and DDR4. Figure 10 illustrates how these routings are accomplished on an unbuffered DIMM. These same techniques can also be implemented on the surface of the printed circuit board to conserve board layer count. Care must be

taken to adequately match the impedance of this line to the termination at the far end of the net, as this will minimize reflections at the devices along the route. Since the capacitive loads of the DRAMs are distributed along the length of the trace, the effective impedance of the lines will be lowered, therefore higher impedance traces, ~60Ω, should be used to route between the devices. On unbuffered DIMMs, the fly-by nets are typically terminated with values of 35Ω to 40Ω on the single ended signals and roughly twice that on the differential signals. To improve the impedance match, the trace region prior to the daisy chained DRAM region should be dropped to ~40Ω. Stub lengths should be kept as short as possible. This may require additional layers to route signals beneath the devices. This is a complex routing configuration and should be simulated thoroughly prior to implementation.

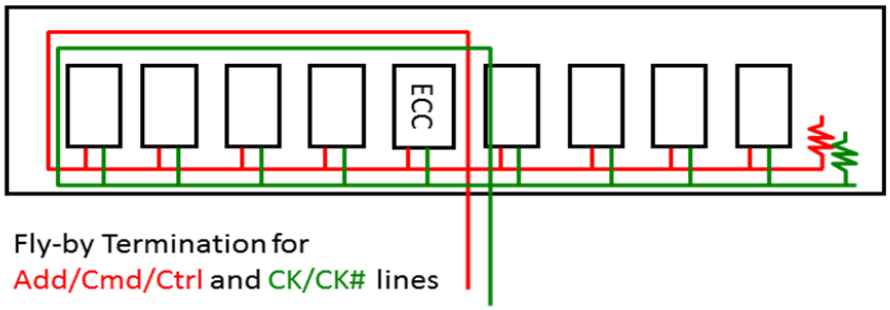

Figure 10: Fly-by Routing Implemented on an Unbuffered DIMM.

Write and Read Leveling

Fly-by termination is used to improve the edge quality of the signals as they are received at high device count memory interfaces. To preserve the relationship between CK/CK# and the DQS/DQS# signals, DDR3 and DDR4 implemented a technique call Leveling. During Write operations (Figure 11), using a programmable delay element, DQS signals are launched with gradually longer delays to each byte along the daisy chain. This is done so the arrival of the rising edges of the strobes coincides with the arrival of the rising edges of the clocks at each SDRAM on the DIMM meeting the tDQSS specification that governs the timing relationship between the received DQS/DQS# pair and the receive CK/CK#.

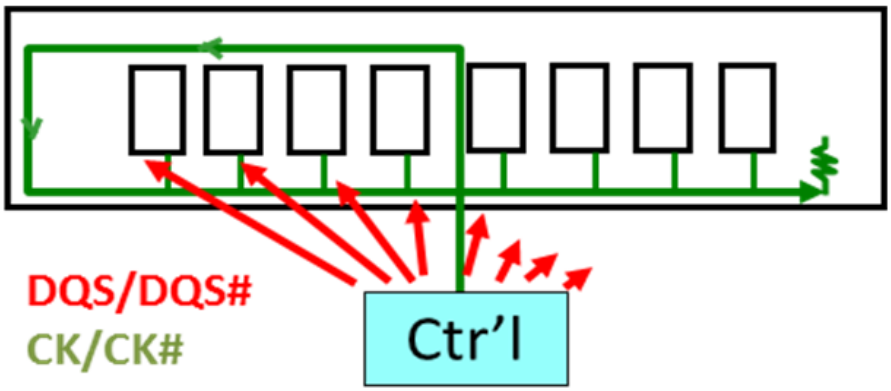

Figure 11: Write Leveling

During Read operations (Figure 12), the controller works in tandem with SDRAM to synchronize arrival of all data bytes in the word at the input to the controller.

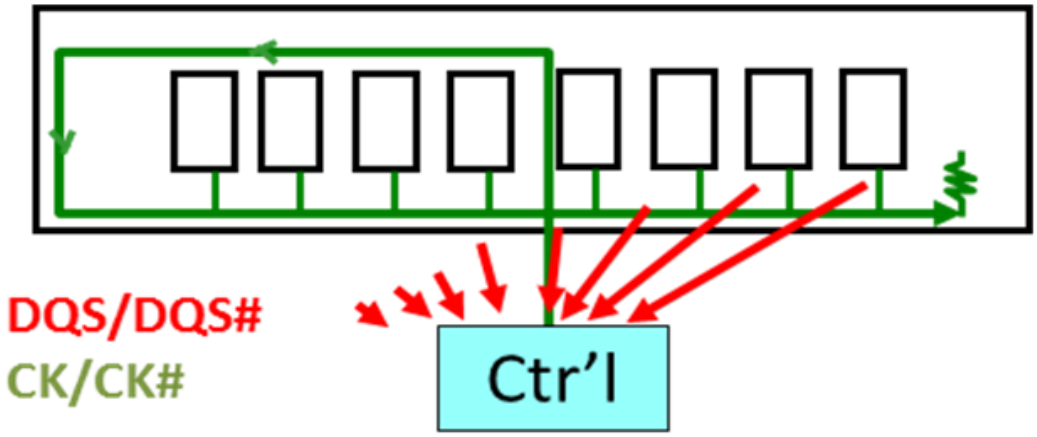

Figure 12: Read Leveling

LPDDR2 and LPDDR3 Features and Benefits

LPDDR2 up to 1067Mbps – Double Data Rate Command/Address

LPDDR2 introduced support for unterminated mobile memory interfaces up to 1067Mbps. One of the power savings was to make the CA bus double data rate and reduce the width of the bus. This operates in much the same manner as the data lanes, but with slightly larger set up and hold requirements.

LPDDR3 to 2133Mbps

LPDDR3 was conceived as a simple data rate extension to LPDDR2. In actual application, several features had to be added to extend the manageable data rate.

Pull-up ODT on DQ, DQS/DQS# and DM

To support higher bit rates, and in recognition of the reality that LPDDR3 devices are often used in applications other the Package-On-Package, ODT values of 240Ω and 120Ω pull up to VDDQ for the data lanes were added to the standard. 60Ω was also added for bit rates of 1866Mbps and above.

Although the CA bus is also double data rate, no provision for ODT on these lanes was included. If this is a board mounted interface, termination resistors should be a mounted on the board to control reflections.

Command/Address Training

DQ per bit deskew and DQS/DQS# centering has been available with Synopsys PHY technology for several years. This is performed through feedback via the bidirectional data lanes. This has not been available on the CA bus because they are unidirectional with no mechanism for feedback.

To accomplish the training of the 10 CA bits, the memory device maps the state of these bits to DQ signals giving skew feedback to the PHY and controller. Status of the 10 CA bits must be read on both the rising and falling edges of the clock requiring 20 DQ signals for all of this information. Since LPDDR3 supports x16 devices as well as x32, the 20 feedback bits must be confined to a single x16 bus. This requires two clock cycles to read back the information as shown in Figure 13.

Table 19 — CA to DQ mapping (CA Training mode enabled with MR41)

CA0	CA1	CA2	CA3	CA5	CA6	CA7	CA8	Clock edge
DQ0	DQ2	DQ4	DQ6	DQ8	DQ10	DQ12	DQ14	CK_t rising edge
DQ1	DQ3	DQ5	DQ7	DQ9	DQ11	DQ13	DQ15	CK_t falling edge

Table 21 — CA to DQ mapping (CA Training mode is enabled with MR48)

CA4	CA9	Clock edge
DQ0	DQ8	CK_t rising edge
DQ1	DQ9	CK_t falling edge

Figure 13: CA bits mapped to DQ bits to be read back to the controller for training purposes.

Write Leveling

Write leveling is usually associated with fly-by routing because of the large flight time differences between the rising edges of DQS/DQS# and CK/CK#. The fly-by routing requires write leveling to assure that the interface meets the +/- ¼ cycle requirement. Usually a short interconnect such as package on package would not introduce enough skew to violate the JEDEC tDQSS specification. Figure 14 shows the footprint of a typical dual channel x32 LPDDR3 device. The CA bus for each channel is located on the opposite side of the die from its associated byte lanes. Consequently, significant process variation can exist between the DQS/DQS# and the CK/CK# pairs. In the event that this variation is great enough to cause violations of the +/- ¼ cycle specification, write leveling can be implemented to address this.

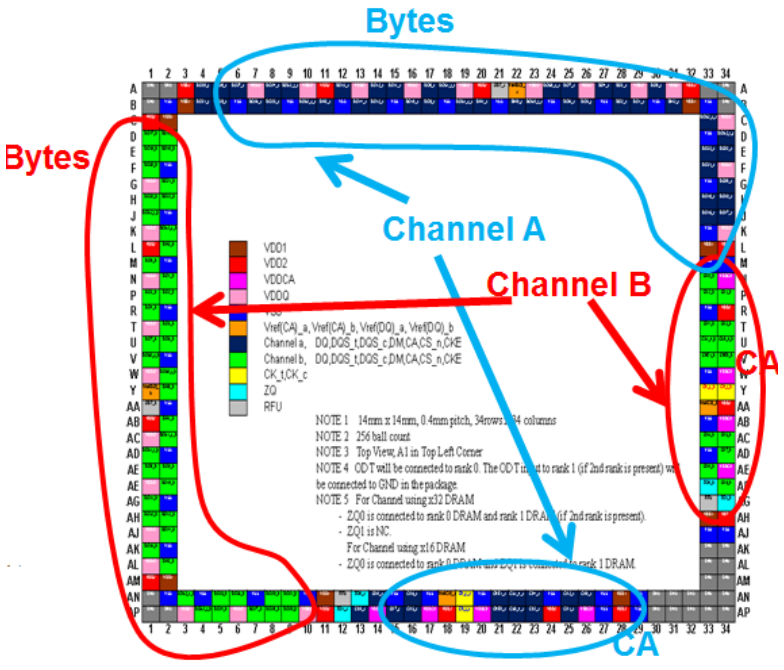

Figure 14: Location of data lane relative to its CA bus.

Protocol Specific Implementation and Routing Guidelines

What follows are recommendations and emphasis on the parameters that are critical for the specific protocols.

DDR4 Specific Routing and Implementation Guidelines

Crosstalk Control

Crosstalk and characteristic impedance of an array of traces are interrelated. To minimize crosstalk, the characteristic impedance of a trace should be determined predominantly by the distance to the reference plane and not the distance to the neighboring traces. To achieve this, the space between traces should be 2X to 3X the height of the trace above the ground plane. Longer routed parallel lengths should have wider spacing.

Figure 15 shows three cases that depict this relationship. Case 1 depicts a typical routing scheme with equal lines and spaces. While the Zo of these lines looks good at 49.9Ω, much of this impedance is determined by the proximity of the neighboring lines. Consequently, there is very high near end crosstalk from multiple aggressors of 30.8%. For a 1.8V signal, this is 473 mV. For Case 2, where the space is doubled, the Zo rises to 54.8Ω and the multi-active crosstalk is cut in half to 15.1%, a more manageable number. In this case, the Zo is determined more by the proximity of the reference plane instead the neighboring traces. Further isolation, shown in Case 3, decreases crosstalk with only a 1Ω increase in Zo. When increasing spacing has no effect on Zo, the traces are said to be isolated.

Note that stripline applications can tolerate narrower spacing within in signal groups. Because the fields from all signals are captured within the same dielectric constant substrate, there are no differences in the mode velocities from different switching patterns. If necessary, spacing can be cut to 1.5X to 2X the height to the nearest reference plane in stripline applications. While this tighter spacing can be used if necessary in stripline, wider spacing is always preferred.

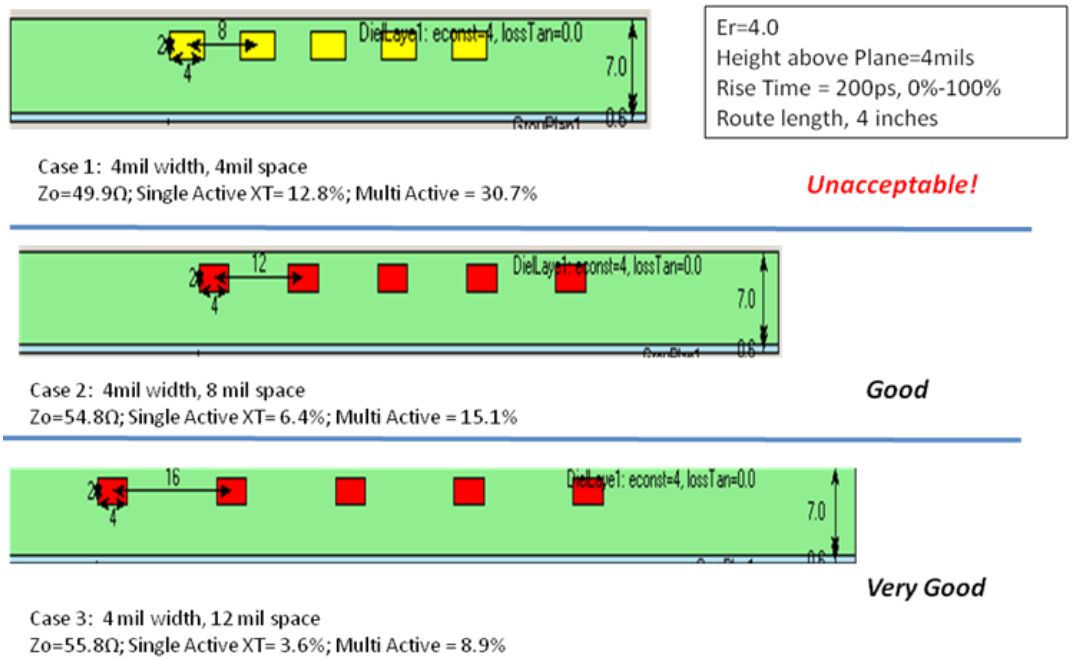

Figure 15: Relationship between Characteristic Impedance and Crosstalk

Crosstalk between dissimilar function groups can have unpredictable effects timing effects and should be avoided. It is recommended that the spacing between byte lanes and the spacing between the byte lanes and the CA region be a minimum of 3X the height above the reference plane. Also, spacing to strobes and clocks must also be increased to assure that crosstalk does not compromise the monotonicity of the system's strobes and clocks.

Stripline vs. Microstrip.

For DDR4 applications that exceed 1866Mbps, it is highly recommended that microstrip configurations be avoided. Because of the mixed dielectric materials in a microstrip configuration, different coupled modes will travel at different velocities causing temporal dispersion at the target device. This increases with routed length. Since signals traveling in stripline see a uniform dielectric, the dispersion is greatly reduced. At high bit rates, timing budgets cannot tolerate the margin loss to this modal dispersion. If Microstrip must be used, it should be confined to short lengths with spacing that is greater than 3X the height to the reference plane.

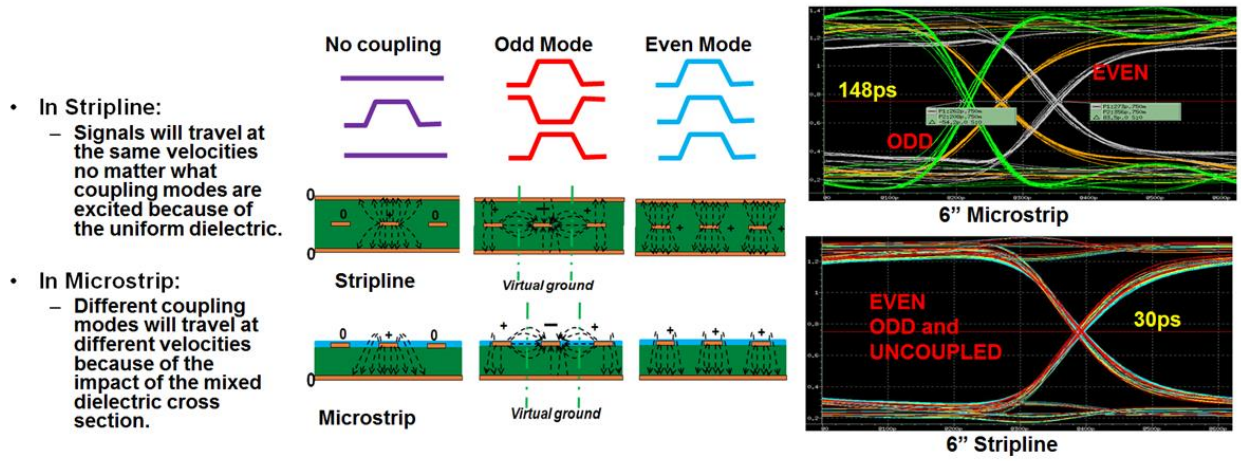

Figure 16: Signal dispersion in microstrip vs. Stripline.

DIMM Routing

DQ and DQS. When routing to two DIMMs, it is preferable that the signal be routed in a TEE configuration. This will optimize the maximum eye opening at both DIMMs on the interface. A daisy chain will use fewer layers and will likely have a larger eye at the second DIMM on the interface, the eye at the first DIMM will be constricted from reflections on the net, possibly compromising performance. The trade-off for using the Tee route is the addition of layers on the board to accommodate the resulting crossovers. If daisy chain routing is used be sure to make any stubs that connect SDRAM pins to the main trunk route as short as possible as any stubs will create reflections and eye closure.

Command/Address Signals – Unbuffered DIMM. With two unbuffered DIMMs on the Command/Address signal, copies of these signals should be routed to each DIMM. This recommendation is based on the terminating resistance that is found on each UDIMM. Typically, the Command/Address nets are terminated with a single resistor at the far end of the fly-by net with the value of ~39Ω. Routing one signal to two UDIMMs will result in an effective termination of 19.5Ω. This will limit the total swing that can be achieved to 416mV assuming 1.14V signaling and 34Ω driver impedance. This may make it difficult to meet the Command/Address set up and hold requirements even with 2T timing implemented.

Routing Skew for DDR4 – Summary and Discussion

There are many trainings available for the DDR4 interface that can remove skew. The implementer should make every effort to control skews as tightly as possible in order to improve overall operating margins when the interface is trained. This is sound engineering practice and can simplify debugging. Table 3 lists recommended skew targets for DDR4. A further discussion of these is found below.

Routing Skew Requirements for DDR4		
Bit Rate / Interface	<2133Mbps	≥2133Mbps
DQ to DQS	+/-15ps	+/-10ps
CA to CK	+/-30ps	+/-25ps
DQS to CK	+/-0.13 *tCK	+/-0.13 *tCK

Table 3: Summary of outing skew requirements for DDR4.

DQ and DQS. For the DDR4 MultiPHY, the deskew range is limited to a total of 300ps across the byte lane. It is always good practice to design an interconnect with very tight skew control, even with per bit training, +/-10ps skew between the DQ and DQS signals for 2133Mbps and above. This can be relaxed below this bit rate. This will allow margins for on die skews and on chip process variation.

Command/Address/Control vs. Clock. There is no deskew functionality built into the single data rate Cmd/Add/Ctrl timing. Consequently, board and package skew needs to be accounted for in the interconnect budget. A routing tolerance of +/-25ps of all of the signals relative to the CK/CK# should be observed. This can be relaxed if the timing budget and simulation results indicate that there is adequate margin.

- Command/Address/Control deskew is available on registered DIMM applications. The RCD chip supports training providing alignment feedback through the Alert signal. This is supported through a software solution in the DDR4 MultiPHY.

DQS/DQS# vs. CK/CK#. For DDR4, the specification requirement is that the DQS/DQS# arrive within 0.27 of a clock cycle from CK/CK#. At 2667Mbps, this is +/-203ps. At the high bit rates associated with DDR4, this is usually managed with Write Leveling. If a user chooses to try to operate without Write Leveling, it is recommended that the routed skew between any DQS pair and the clock pair be kept to ½ of the tDQSS budget.

Note on Terminating Multiple Ranks of DDR4

Because DDR4 is pull up terminated, the combination of source impedance, target ODT impedance and stub ODT impedance will determine the signal swing and the optimum VREF level. During consecutive Read operations from different ranks, there is only one ODT value and one trained VREF level applied to the Host. To maintain maximum eye opening when switching Reads from rank to rank, it is critical that active ranks drive with the same nominal

drive strength. It is also important that when a quiet rank uses ODT to minimize stub reflections, the same values be used for stub termination regardless of which rank is being driven. All of this is needed to maintain a balanced signal swing around the optimum VREF level.

Package Considerations for DDR4

Wire bond packages are not recommended for DDR4 interfaces.

An analysis of the supply impedance should be undertaken to make sure the targets listed previously are met. The implementer should simulate his particular interface with expected switching patterns to assure that the targets listed herein are appropriate to their application. Please refer to "*Power Integrity and Supply Impedance Determination for DDR Interfaces*" application note for guidance on how to determine to proper supply impedance for an interface.

To control crosstalk, the spacing between signals of the same group should be kept to a minimum of 2X the height to the nearest reference plane. Spacing of 3X should be maintained to all differential signals and between signal groups.

DDR3 and DDR3L Specific Routing and Implementation Guidelines

The guidelines for DDR4 also apply to DDR3 and DDR3L. A summary of the skew targets is below.

Routing Skew Requirements for DDR3 and DDR3L		
Bit Rate / Interface	<2133Mbps	2133Mbps
DQ to DQS	+/-15ps	+/-10ps
CA to CK	+/-30ps	+/-25ps
DQS to CK	+/-0.13 *tCK	+/-0.13 *tCK

Table 4: Skew targets for DDR 3 and DDR3L.

Package Considerations DDR3 and DDR3L

Wire bond packages are not recommended for DDR3/DDR3L interfaces that operate above 1600Mbps.

An analysis of the supply impedance should be undertaken to make sure the targets listed previously are met. The implementer should simulate his particular interface with expected switching patterns to assure that the targets listed herein are appropriate to

their application. Please refer to "*Power Integrity and Supply Impedance Determination for DDR Interfaces*" application note for guidance on how to determine to proper supply impedance for an interface.

To control crosstalk, the spacing between signals of the same group should be kept to a minimum of 2X the height to the nearest reference plane. Spacing of 3X should be maintained to all differential signals and between signal groups.

LPDDR3 and LPDDR2 Specific Routing and Implementation Guidelines

In general, the guidelines for DDR4 also apply to LPDDR3 and LPDDR2.

Crosstalk Control.

Since LPDDR3 and LPDDR2 are unterminated or lightly terminated interfaces, extra care should be taken in controlling crosstalk. Mobile memory platform performance depends on a good impedance match between the source impedance and the interconnect. Low crosstalk, which impacts modal impedance, will make the impedance match easier to maintain. The crosstalk control guidance listed in the DDR4 interface section should be followed for LPDDR3 and LPDDR2 as well.

Termination

For interfaces that are mounted on the board and not in PoP, it is highly recommended that on board termination be applied to the CK/CK# signals and to the CA signals for the higher bit rate LPDDR3 interfaces.

Total Routed Length

For mobile interfaces, the total routed length should be kept below 1" on an unterminated interface to keep reflections under control. Longer lengths than this should use the ODT options for LPDDR3 and consider terminating the Command/Address signals on the board.

Routing Skew for LPDDR3 and LPDDR2 – Summary and Discussion

There are many trainings available for the LPDDR3 interface that can remove skew. LPDDR2 is more limited The implementer should make every effort to control skews as tightly as possible in order to improve overall operating margins when the interface is trained. This is sound engineering practice and can simplify debugging. Table 5 lists recommended skew targets for LPDDR3 and LPDDR2. A further discussion of these is found below.

Routing Skew Requirements for LPDDR3 and LPDDR2		
Bit Rate / Interface	<2133Mbps	2133Mbps
DQ to DQS	+/-15ps	+/-10ps
CA to CK	+/-15ps	+/-10ps
DQS to CK	+/-0.12 *tCK	+/-0.12 *tCK

Table 5: Summary of outing skew requirements for LPDDR3 and LPDDR2.

DQ and DQS. For the DDR4 MultiPHY, the deskew range is limited to a total of 300ps across the byte lane. It is always good practice to design an interconnect with very tight skew control, even with per bit training, +/-10ps skew between the DQ and DQS signals for 2133Mbps and above. This can be relaxed below this bit rate. This will allow margins for on die skews and on chip process variation.

Command/Address/Control vs. Clock. For LPDDR3, there is deskew on the double data rate Command/Address bus,. This deskew functionality does not exist for LPDDR2 The same skew guidelines that apply to DQ and DQS also apply to CA vs. CK.

DQS/DQS# vs. CK/CK#. For LPDDR3 and LPDDR2, the specification requirement is that the DQS/DQS# arrive within 0.25 of a clock cycle from CK/CK#. At 2133Mbps, this is +/-234ps; twice that at 1067Mbps. LPDDR3 can use Write Leveling, but LPDDR2 does not have this feature.. If a user chooses to try to operate without Write Leveling, it is recommended that the routed skew between any DQS pair and the clock pair be kept to ½ of the tDQSS budget.

Package Considerations LPDDR3 and LPDDR2

Wire bond packages are not recommended for LPDDR3/LPDDR2 interfaces that operate above 1067Mbps..

An analysis of the supply impedance should be undertaken to make sure the targets listed previously are met. The implementer should simulate his particular interface with expected switching patterns to assure that the targets listed herein are appropriate to their application. Nominally, a 2:1:1 signal :power: ground ratio should be maintained across the interface in a flip chip package for bit rates greater than 1333Mbps. 3:1:1 can be used in lower bit flip chip applications. Wire bond should have a maximum ratio of 2:1:1.

To control crosstalk, the spacing between signals of the same group should be kept to a minimum of 2X the height to the nearest reference plane. Spacing of 3X should be maintained to all differential signals and between signal groups.

PoP (Package on Package) Systems

Mobile memories such as LPDDR3 and LPDDR2 are often implemented in Package on Package configuration because of the compact profile. PoP systems are an interconnect technology for achieving higher density for mobile applications and is a major focus of the JEDEC LPDDR3 SDRAM memory standard JESD209-3.

A typical PoP system is shown in Figure 17.

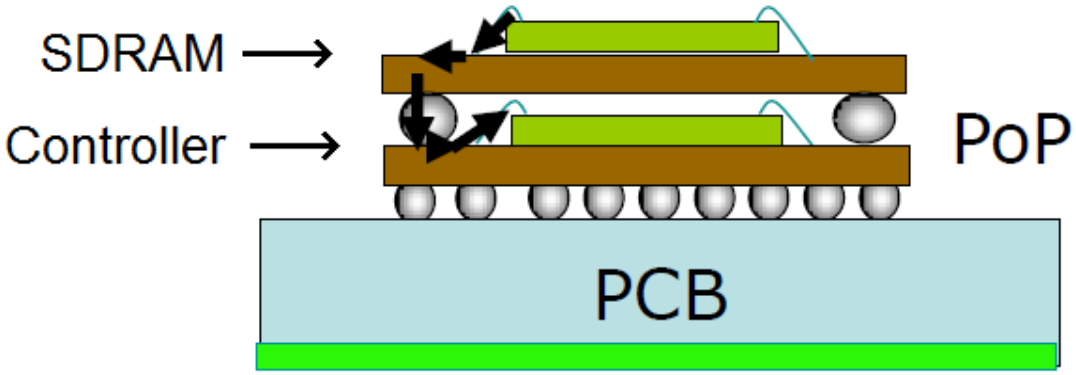

Figure 17: PoP System

The wire bond SDRAM package contains one or 2 dies (1 or 2 ranks stacked) and is mounted on top of the controller device package. The packages are BGA so the balls of the SDRAM package contact pads on the top of the controller package to make the connections between the two. The controller die in the controller package has bond wire connections as well although it could be a flip chip design if higher density of connections is required. The controller BGA package has balls to connect to the PCB. The controller package must supply power to both the controller die and the SDRAM die from the PCB.

Big advantages of this arrangement are higher density and higher DDR interface performance in terms of signal integrity and power savings. The higher signal integrity performance comes from the fact that there is no PCB interconnect in this system so the signals paths are very short. Since the signal paths are very short it may be possible to run the systems at a high rate without signal terminations or low impedance terminations that would consume lots of power. It is still necessary, however, to run the proper signal integrity analysis on the signal paths to determine the proper level of termination (or not) for best signal eye quality, crosstalk, timing, and SSO noise to determine if the DDR interface will perform adequately in the PoP environment, Possible disadvantages are restrictive geometries for SDRAM packaging and controller die size, and, power dissipation in a much denser system which may cause overheating.

PoP System SDRAM Package

A couple of different packages are suggested for use in LPDDR3 PoP systems. One of them is based on LPDDR2 PoP packaging and is a standard 0.4mm ball pitch BGA package with 216balls, 12x12mm in size, with 2 rows of balls on the periphery and an open array. It is dual channel meaning it can support 2 stacked dies (or ranks). Each channel has a 32 data bit interface and 10 address bits. There are two chip selects each, two CKE, one CLKP/N pair each. There is no ODT pin as the SDRAM die(s) have their ODT pins connected to VSS in the package. Figure 18 shows the ball out of this SDRAM PoP package from the top view. There is a

large void of balls in the center of the ball array of the SDRAM package to allow space for the controller die to sit when the SDRAM package is attached to the top of the controller package.

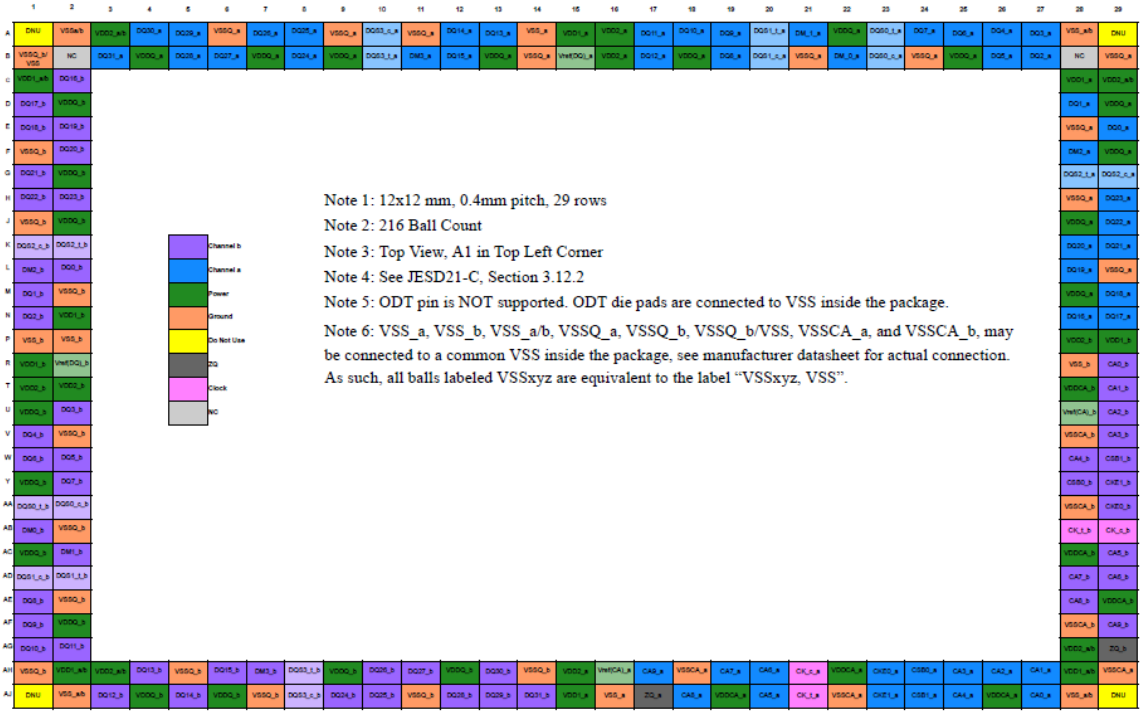

Figure 18: 216 Ball PoP SDRAM package

PoP System Controller Package

There are a large variety of possible package types which can be used for the controller device in a PoP system since the types of applications can be quite varied. The controller package must have exactly the same ball pin out and spacing on the pads on the top of the package as the SDRAM. For our example we will look at a 400-600 pin 0.5mm pitch BGA wire bond package which seems to be a fairly common low cost package. The controller die needs to be smaller than the 10x10mm cavity which is the space remaining due to the open array of balls of the SDRAM package on top of the controller package. The controller package needs to be bigger than the 29 x29 row 0.4mm ball pitch size of the SDRAM package to be able to support the SDRAM package on top. Figure 65 shows an example of a controller PoP package that is a wire bond package. Figure 66 shows an example of a flip chip based controller PoP package.

The controller package needs a large number of power and ground pins to support the power needs of both the SDRAM and controller dies. Carefully analysis of power integrity is needed to ensure the performance of the power networks of through the controller package. In addition, there would possibly be a need for VREF inputs (if generated on the PCB), and connections for ZQ resistors. In Figure 19 and Figure 20 the purple SDRAM balls and controller DDR IOs are

the channel 1 DDR interface. The light blue SDRAM balls and controller DDR IOs are the channel 2 DDR interface. Note the SDRAM interface balls are interleaved between channel 1 and 2. The data byte lanes for channel 1 are on the left and bottom sides of the SDRAM package. The data byte lanes for channel 2 are on the top and right sides of the SDRAM package. The Address/Command/CLK signals for channel 1 are on the right bottom corner of the package. The Address/Command/CLK signals for channel 2 are on the bottom right corner of the package. An example of on die IO rings are shown for the two DDR interfaces in Figure 19 assuming a 32 bit interface with 25um width IO cells (Gen 2 multiPHY).

As mentioned before for the LPDDR3 standard it is possible for data bytes to have a weak pull up termination to VDDQ whereas the Address/Command/Control bus has none. This requires the VrefDQ pins have a different VREF voltage than the VrefCA pins.

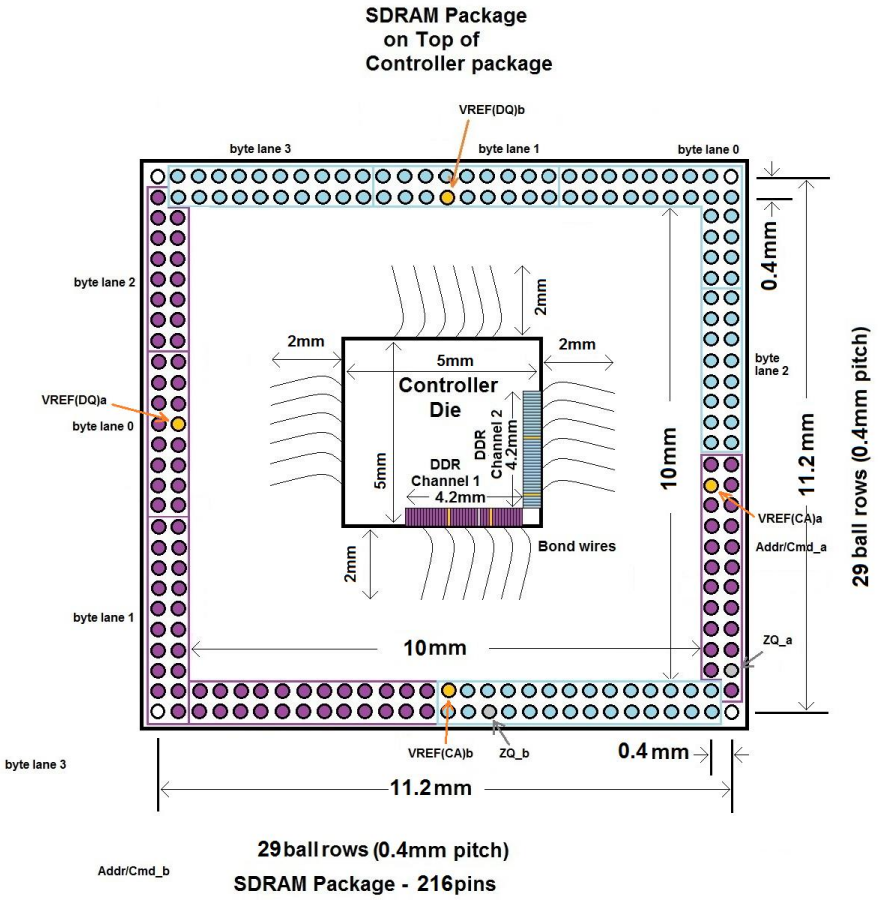

Figure 19: Example Wire Bond Controller PoP package

Referring to Figure 19 there are some of the interesting points from this arrangement:

1. PoP Controller die size will be limited to area available from under the SDRAM package, and area taken up by bond wires so die size will probably max of about 5x5mm.
2. The SDRAM DDR signals are arranged over the periphery of the SDRAM package whereas the DDR IO rings are arranged in a contiguous fashion in a small section of the die edge. Signals in the controller package will need to be routed across the package to the opposite side. This might lead to some signal skews.
3. There is some interleaving of the Address/Command/CLK signals between channel 1 and 2 so there will need to be either bond wire cross-overs or substrate trace cross-overs to escape the signals from the die.

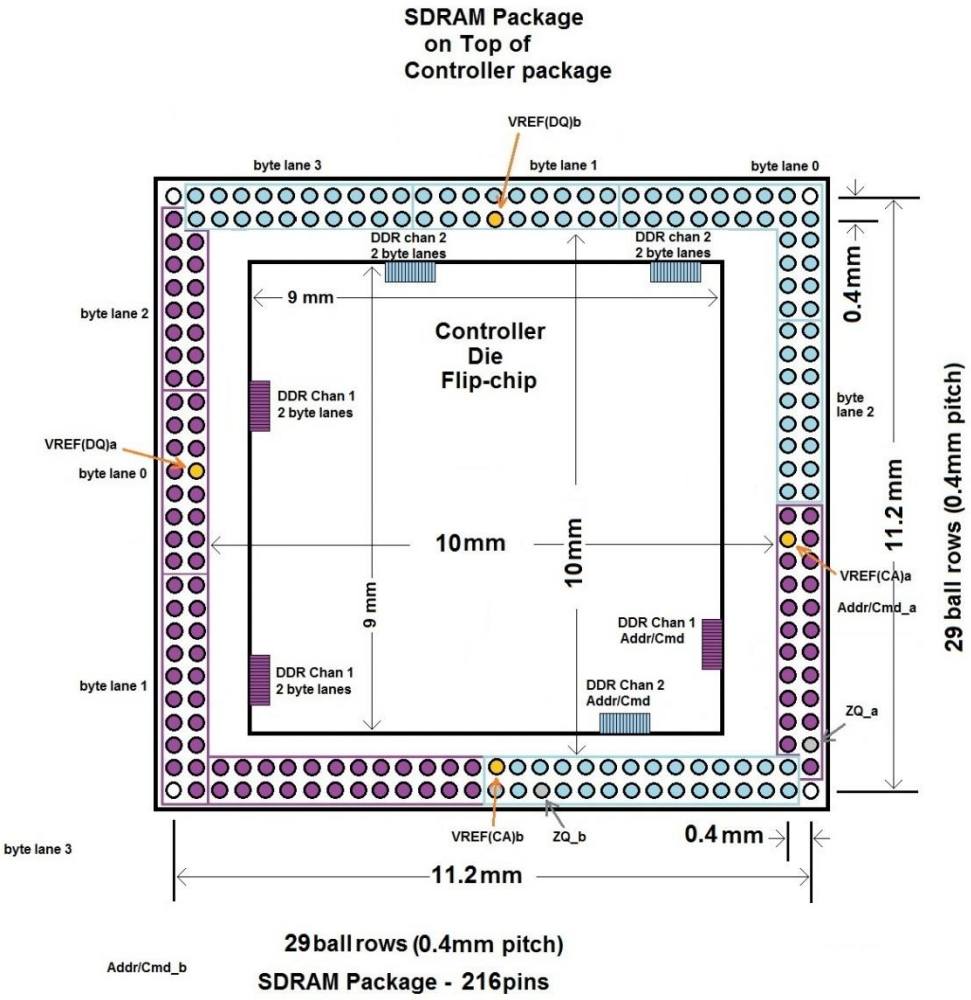

Figure 20: Die Functionality relative to ball out in PoP interface.

Referring to Figure 20, the flip chip PoP system has a flip chip device and package for the controller device and the same SDRAM package for LPDDR memory. The advantages of the flip chip system are:

1. Bigger controller die (9mmx9mm) can be supported since there are no bond wires to route.
2. DDR interface should have higher performance since the inductance of bumps is much lower than bond wires

This is also called a segmented IO ring DDR interface which is supported by the Gen 2 multiPHY IP. In this system the signals of the controller die DDR interface need to align very well with the signals of the SDRAM package so the DDR interface is distributed around the periphery of the controller die to maintain alignment. This means the different byte lanes IOs may be broken up into individual pieces (one or two byte lanes) and same for the Address/command IO ring.

The advantages of this arrangement are:

1. Better alignment of signals on die to SDRAM package balls so easier routing of signals in the package.
2. Higher performance for the signal routes in the package since they are very short

The disadvantages of this arrangement are:

1. Power for the DDR interface has to be distributed to all parts of the controller die. This implies the controller package and PCB need to have DDR IO and PLL power brought in via dedicated planes on the PCB since this power will be interleaved with other interfaces on the periphery of the controller die. In conventional contiguous DDR interface IO rings, a section of the package containing the whole DDR interface shares power in one region of the package and PCB only – easier to implement without extra power planes.
2. Common DDR interface control busses and clocks in the core need to be routed to different edges of the die to connect to the split DDR interface.

VAA_PLL Supply

VAA_PLL supply is used for providing power to the PLLs only in some Designware IP (DDR2/DDR Core, DDR multiPHY, DDR2/3-Lite, mDDR Core, DDR3/2 Core) and to PLLs and IO RX circuits in other Designware IP (Gen 2 multiPHY, DDR4 multiPHY). The guidelines provided cover 5 different system cases depending on the IP mentioned above and how it is used. Scenarios 1 and 2 are provided for background; scenarios 3, 4 and 5 are directly applicable to the DDR4 MultiPHY.

1. **PLL only VAA_PLL Supplies – Not Shared on PCB**
2. **PLL only VAA_PLL Supplies – Shared on PCB**
3. **PLL and IO RX VAA_PLL Supplies – Not shared on PCB**
4. **PLL and IO RX VAA_PLL Supplies – Shared on PCB**
5. **PLL and IO RX VAA_PLL Supplies – PDR=OFF constantly**

PLL only VAA_PLL Supplies – Not Shared on PCB

In this first case VAA_PLL supply is only needed to provide power to the PLL circuits. The VAA_PLL supply is used to provide clean power to the analog portion of the PLL and should be an isolated supply net through the package from the PCB. Decoupling circuits should be included on the PCB to help reduce noise on the VAA_PLL supply. If the VAA_PLL supply on the PCB is not shared with any other circuits on the PCB there is no requirement for more filtering components (like series ferrite bead) other than the decoupling caps as shown here (Figure 21) or on die. In this example there is a large 10uF capacitor and two smaller capacitors (1.0uF and 0.1uF). The small 0.1uF capacitor should be placed as close to the VAA_PLL pin of the package. The 1.0uF can be placed farther out than the 0.1uF capacitor and the 10uF capacitor placement will be less critical. The smaller two capacitors should be placed for every VAA_PLL pin of the package whereas the 10uF could be shared for a few VAA_PLL pins in a more central location.

The VAA_PLL supply net may be routed as a wide signal net trace with adjacent ground net trace which can be used as shielding, and should be spaced away from other noisy nets 3 times the height above the reference plane. Some of the bytes lanes may have a VAA_PLL IO cell in the IO ring. Some of these VAA_PLL nets in the package may be combined and routed to a single package ball. It is recommended that no more than 5 PLLs VAA_PLL nets be combined to one package ball. Target impedance and IR drop should be considered for the VAA_PLL power nets. For example if the PLLs are operating in DDR3-1600 mode (clock = 800MHz) for Gen2 multiPHY, each PLL draws a maximum of 12mA each on VAA_PLL. The max AC supply noise at the PLL should be limited to +/-2.5% nominal VAA_PLL (from databook) or +/-2.5% of 1.8V = +/-45mV or 90mVpp. To a first order the target impedance should be 90mV/(5 * 12mA) = 1.5 ohms. For IR drop the minimum DC supply voltage at the PLL on die should be no less than nominal VAA_PLL – 10% or 1.8V * 0.9 = 1.62V.

On die, PLLs require PVAA_PLL cells in the IO ring to bring VAA_PLL supply to the core and provide ESD clamping to protect this supply. In general, one PVAA_PLL cell is used for each PLL. In flip chip applications each PVAA_PLL should have its own bump. In wirebond packages each PVAA_PLL cell will have its own bondwire. If one PVAA_PLL cell is used to connect to a couple of PLLs, IR drop should be studied to ensure this is acceptable.

PLLs for the DDR PHY macros blocks contain regulators within the PLL block; therefore no additional 1.8V VAA_PLL rail on-die decoupling capacitance is required for the PLLs.

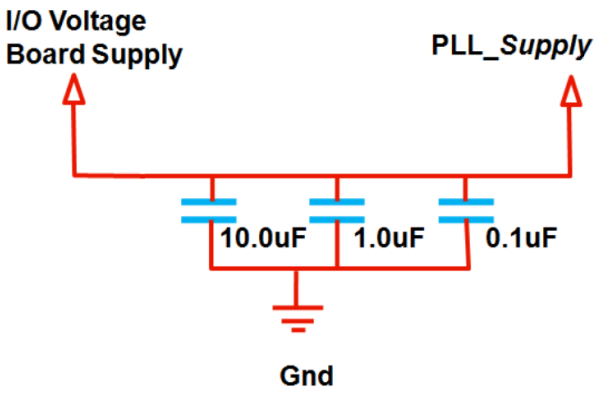

Figure 21: PLL PCB Supply filter - Not shared on PCB

PLL only VAA_PLL Supplies – Shared on PCB

If the VAA_PLL PCB supply is shared with other circuits on the PCB it is recommended to include a ferrite filter circuit on the PCB as shown in the figure below.

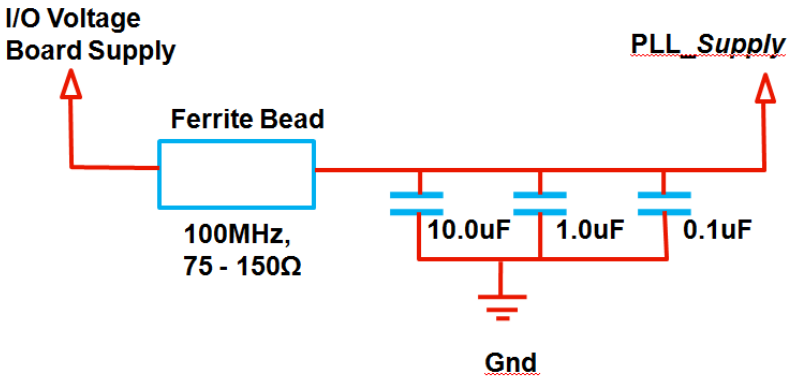

Figure 22: Ferrite bead PCB filter circuit for VAA_PLL

The ferrite is used to prevent noise from the other circuits on the PCB from entering the DDR PLL circuits on chip. Use of the ferrite circuit requires some specific attention on a few points.

The bead material type, DC IR drop limit, maximum DC current limit, and the frequency response of the filter circuit need to be considered.

Ferrite beads come in a couple of types: non-resonant or absorptive beads and high Q or resonant beads. For filtering power supplies the non-resonant or absorptive bead types should be used. Using high Q beads can lead to unwanted power supply resonances.

For the DC IR drop, the ferrite is a series element with a finite DC resistance. A budget for the IR drop of the VAA_PLL supply should be created to determine the amount of DC IR drop that can be tolerated in the ferrite as well as package and on die interconnect. For example if an IR drop budget allows 0.5% IR drop of the VAA_PLL rail for the ferrite bead, the voltage drop must be less than 1.8V x 0.5% = 9mV. If we have 5 PLLs sharing one ferrite bead the DC current will be 5 x 12mA =60mA, if we use the same example with Gen 2 PLL at 800MHz clock. Ferrite bead max DC resistance must be less than or equal to 9mV/60mA = 0.15 ohms.

Ferrite beads are a magnetic circuit and large currents flowing can cause the magnetic circuit to saturate and limit filter effectiveness. It is recommended to keep maximum current through ferrite bead to less than ½ the maximum current rating.

Target impedance and IR drop should be considered for the VAA_PLL power nets. Target impedance of the VAA_PLL supply will be the same as the “Not shared on PCB” case (1.5 ohms) but we now have the series ferrite in the circuit.

The challenge is to attenuate the VAA_PLL supply noise entering from the PCB across as wide as possible range of frequencies while providing a low impedance supply at the range of frequencies the PLL requires. The PLL output frequency is 1600MHz (the 800MHz DDR clock is generated by a divide by 2 circuit in the last flip flop stage of the PHYAC macro for low duty cycle error). The output of the PLL is a 1600MHz clock with harmonics since the output is trapezoidal in nature. The input REFCLK to the PLL is a 400MHz clock (4x step up in PLL) and the PLL has a lower frequency loop bandwidth (<10MHz – need to check with PLL designers). In order to prevent noise from entering the PLL supply the ferrite needs to block noise from less than 10MHz to multiple GHz range.

Many different families of ferrites exist but certain families are optimized for blocking noise in power supplies in this frequency range in a small form factor. One such bead is the BLM15PX121SN1 bead from Murata Erie in a 0402 package. Here is the frequency response of the ferrite bead.

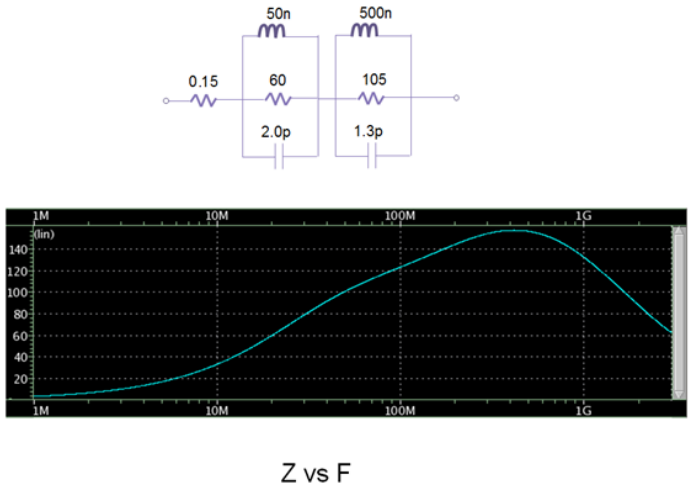

Figure 23: Ferrite bead Impedance vs. Frequency Response

Bead manufacturers usually provide an Hspice model for the bead – in this case we show a simplified equivalent model. On the datasheets for a bead the manufacturers usually specify a bead impedance at a specific frequency such as 120ohm impedance at 100MHz which is the case for our ferrite here. For the purpose of choosing a reasonable bead component for our filter, the response of the ferrite with impedance of approximately 100 to 120ohms @ 100MHz should give us decent broadband filtering coverage for the PLL circuit power.

Assuming we are seeing VAA_PLL PCB AC noise at about 100MHz and it is a maximum of around +/-10% nominal VAA_PLL= 1.8V x +/-10% = +/-90mV or 180 mVpp and our power network impedance equivalent to 90mVpp/60mA = 1.5 ohms from before, the noise seen at the PLL from the PCB would be 180mVpp x (1.5 ohms/(120ohms + 1.5ohms) = 2.22mVpp. At 10MHz the ferrite has an impedance of 32 ohms so PCB noise of 180mVpp would give 180mVpp x (1.5ohms/(1.5ohms + 32ohms) = 8mVpp. At 1.6GHz the ferrite is about 75 ohms so the noise from the PCB would be about 180mVpp x (1.5ohms/(1.5ohms + 75ohms) = 3.5mVpp. The ferrite will provide good broadband coverage.

Next the PCB capacitors need to be added to maintain the VAA_PLL power supply at a low impedance to the PLLs. The values used are 10uF, 1uF and 0.1uF which cover the supply over a range of frequencies. The small 0.1uF capacitor should be placed as close to the VAA_PLL pin of the package. The 1.0uF can be placed farther out than the 0.1uF capacitor and the 10uF capacitor placement will be less critical. The complete PCB filter is shown in figure 87.

As in the "Not shared on PCB" case, the VAA_PLL supply net may be routed as a wide signal net trace with adjacent ground net trace which can be used as shielding, and should be spaced away from other noisy nets 3 times the height above the reference plane. Some of the bytes lanes may have a VAA_PLL IO cell in the IO ring. Some of these VAA_PLL nets in the package

may be combined and routed to a single package ball. It is recommended that no more than 5 PLLs VAA_PLL nets be combined to one package ball.

On die, PLLs require PVAA_PLL cells in the IO ring to bring VAA_PLL supply to the core and provide ESD clamping to protect this supply. In general, one PVAA_PLL cell is used for each PLL. In flip chip applications each PVAA_PLL should have its own bump. In wirebond packages each PVAA_PLL cell will have its own bondwire. If one PVAA_PLL cell is used to connect to a couple of PLLs, IR drop should be studied to ensure this is acceptable.

PLLs for the DDR PHY macros blocks contain regulators within the PLL block, therefore no additional 1.8V VAA_PLL rail on-die decoupling capacitance is required for the PLLs.

PLL and IO RX VAA_PLL Supplies – Not shared on PCB

Some DDR IP, like Designware Gen 2 multiPHY use VAA_PLL for IO RX supply as well as PLL supply. In this case PCB and extra on die decoupling will be required to attenuate the VAA_PLL supply noise from RX IO circuits from exceeding PLL AC ripple limits (+/-2.5% nominal VAA_PLL). The extra current draw of the IO RX must also be considered in the IR drop analysis of the combined VAA_PLL supply for both IO RX and PLL. The IO RX circuit current draw may be dynamically switched by the PHY controlling the PDR pins of the IO (Power Down Receiver = 1 for IO RX power down) depending on write cycle (PDR=1) and read cycles (PDR=0) in order to conserve power on the IO supplies. The worst case scenario for VAA_PLL supply noise is when PDR is dynamically switched which is the case considered here.

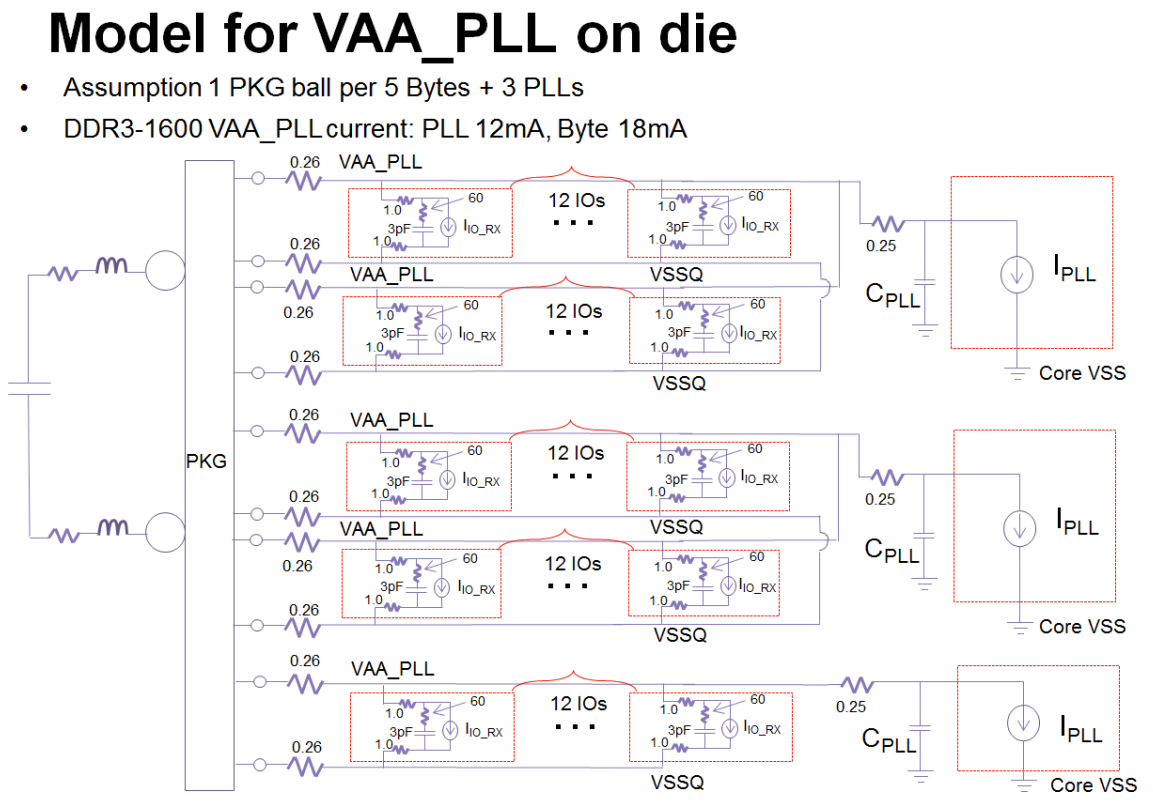

Figure 24: On Die VAA_PLL supply - 5 Byte lanes and 3 PLLs

An example system using Gen 2 multiPHY IP is given in Figure 24which has one VAA_PLL package ball through a flip chip package feeding 5 byte lanes, each with a PVAA_PLL cell and its own bump, Two byte lanes share one PLL except for the last byte lane which has its own PLL. The 5 VAA_PLL bumps in the package are routed together and connect to one ball on the package. The VAA_PLL and VSSQ bumps have RDL of about 0.26 Ohms each connected to the PVAA_PLL and PVSSQ cells in close proximity to each other. The PLL have another 0.26 ohm max routing resistance to the PLL.

The PLLs for Gen 2 MultiPHY use 12mA at 800MHz (DDR3 -1600Mbps system). The IO RX will use about 1.5mA each (DC + AC current calculated from power numbers in the databook) in DDR3-1600 mode. Total current for the IO RX will be 12 x 1.5mA = 18mA. Total current for 5 byte lanes + 3 PLLs will be (5 x 18mA) + (3 x 12mA) = 126mA.

Since the VAA_PLL supply is not shared on the PCB, a series filter element such as the ferrite bead will not be required. Assuming the Voltage regulator on the PCB takes 5% of the IR budget, 5% is left for package and on die routing. Assuming the package IR drop is 1.0%, on die IR drop is allowed to be 4% or 1.8V x 4% = 72mV. IR drop through the bumps and RDL will be (18mA *2 + 12mA) x (0.26ohms x 2) = 25mV. IR drop to the PLL will be an additional (0.26ohms

12mA) = 3.1mV for a total of 25mV + 3.1mV = 28.1mV which is less than the limit (72mV) as an example.

The byte lanes require one PVAA_PLL cell which is located in the center of the byte lane to balance IR drop along the MVAA_PLL bus to the signal IO cells. Each MVAA_PLL bus has a branch of 6 IO cells. The resistance from PVAA_PLL pad to MVAA_PLL bus is 0.292 ohms (Gen 2 multiPHY databook). The horizontal bus resistance per IO cell is 0.292ohms (Gen 2 multiPHY databook). Assuming 2:1:1 signal to power to Ground IO cells so each signal IO is 3 cells away from each other.

Example IR drop Calculation in IO ring

IR drop from PVAA_PLL pad to MVAA_PLL bus = 18mA X 0.292ohms = 5mV

IR drop MVAA_PLL bus from PVAA_PLL cell to sixth signal IO cell =
(6 x 1.5mA) x (0.292ohms X 3 IO cells) +
(5 x 1.5mA) x (0.292ohms X 3 IO cells) +
(4 x 1.5mA) x (0.292ohms X 3 IO cells) +
(3 x 1.5mA) x (0.292ohms X 3 IO cells) +
(2 x 1.5mA) x (0.292ohms X 3 IO cells) +
(1 x 1.5mA) x (0.292ohms X 3 IO cells)
= 27.6mV

Total IR drop from PVAA_PLL bump to last IO cell = 25mV + 5mV + 27.6mV = 57.6mV

This is less than 72mV limit.

More of the budget could be assigned to allow the package or on die IR drop to increase for example.

The VAA_PLL supply net may be routed as a wide signal net trace with adjacent ground net trace which can be used as shielding, and should be spaced away from other noisy nets 3 times the height above the reference plane. Some of the bytes lanes may have a VAA_PLL IO cell in the IO ring. Some of these VAA_PLL nets in the package may be combined and routed to a single package ball. It is recommended that no more than 5 PLLs VAA_PLL nets be combined to one package ball.

For example if the PLLs are operating in DDR3-1600 mode (clock = 800MHz) for Gen2 multiPHY, each PLL draws a maximum of 12mA each on VAA_PLL. The IO RX draw 18mA for one byte on VAA_PLL. For one branch of the VAA_PLL supply network to a PLL it has a current draw of 12mA + (2 x 18mA) = 48mA. The max AC supply noise at the PLL should be limited to +/-2.5% nominal VAA_PLL (from databook) or +/-2.5% of 1.8V = +/-45mV or 90mVpp. To a first order the target impedance should be 90mV/(48mA) = 1.875 ohms.

Figure 25 shows the current draw of one byte lane of IO RX (green) and the current draw of a single PLL (gold). Note that the IO RX are switching a PRBS7 pattern and the IOs are powered up (10 bits wide) and down (10 bits wide) as with alternating write and read bursts where the IO RX are powered down during write bursts (PDR=1).

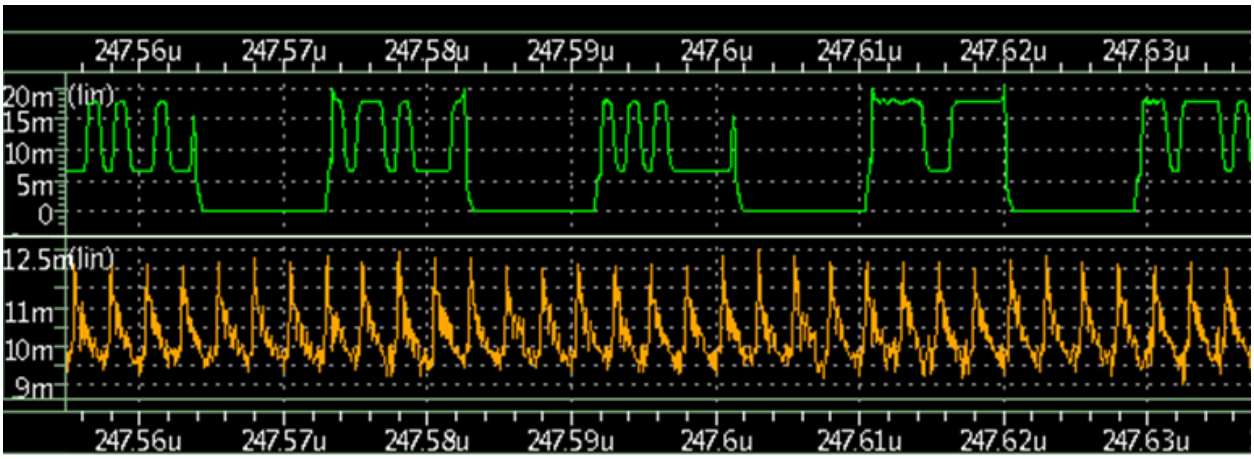

Figure 25: Current profiles of one byte lane IO RX (green) and one PLL (gold) each

Examining the VAA_PLL power supply network in the frequency domain (Figure 92) reveals that target impedance can be met with the following decoupling caps.

PCB decoupling caps: one 10uF, one 2.2nF, one 220pF

On die decoupling caps at IO on VAA_PLL to VSSQ supply net: 10pF capacitance from VAA_PLL to VSSQ per signal IO. For example a byte lane with 11 IOs would require 11 X 10pF/IO = 110pF.

The 10pF/IO on die decap is required to reduce the switching noise on the VAA_PLL net due to the IO RX circuits. The VAA_PLL decap cells need to be added in the space between/around the PHY blocks and the IO cells or in between IO cells. The decap cells should be strapped to the PVAA_PLL bus of the IO cells in a direct manner as possible in higher die layers.

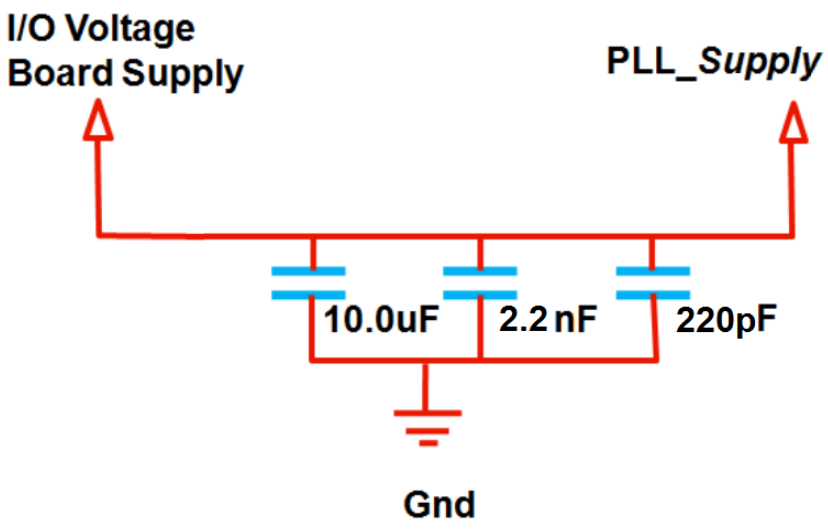

Figure 26: PCB filter for VAA_PLL for RX IO and PLL Not shared on PCB

Only one set of PCB decoupling caps is required per VAA_PLL package ball with the smallest 220pF cap closest to the package ball. The on die decoupling (1.8V compatible) is required right at the PLLs for each PLL as shown in Figure 24.

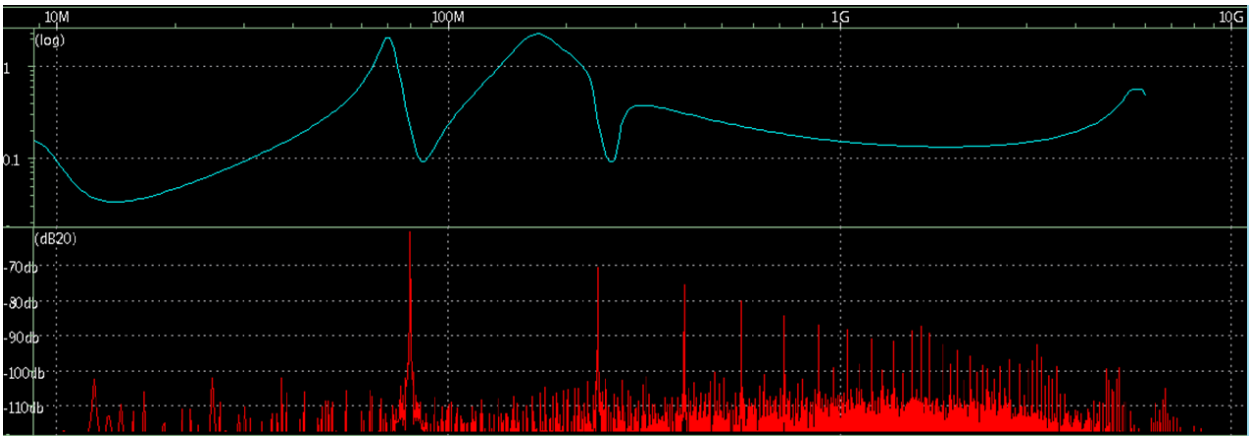

Figure 27: VAA_PLL Impedance and VAA_PLL current FFT vs. frequency plots

The Impedance plot for VAA_PLL (blue) and the FFT of the VAA_PLL current for the IO RX and PLL (red) are shown in Figure 27. Note the largest current spike is from the IO Rx circuits switching on and off every 10 bit periods which is 625psec x 10 bits x 2 = 12.5 nsec or a frequency of 80MHz.

PLL and IO RX VAA_PLL Supplies – Shared on PCB

Reusing the example system using Gen 2 multiPHY IP is given in Figure 24 which has one VAA_PLL package ball through a flip chip package feeding 5 byte lanes, each with a PVAA_PLL cell and its own bump, two byte lanes share one PLL except for the last byte lane which has its own PLL. The 5 VAA_PLL bumps in the package are routed together and connect to one ball on the package. The VAA_PLL and VSSQ bumps have RDL of about 0.26 Ohms each connected to the PVAA_PLL and PVSSQ cells in close proximity to each other. The PLL have another 0.26 ohm max routing resistance to the PLL.

The PLLs for Gen 2 MultiPHY use 12mA at 800MHz (DDR3 -1600Mbps system). The IO RX will use about 1.5mA each (DC + AC current calculated from power numbers in the databook) in DDR3-1600 mode. Total current for the IO RX will be 12 x 1.5mA = 18mA. Total current for 5 byte lanes + 3 PLLs will be (5 x 18mA) + (3 x 12mA) = 126mA.

The VAA_PLL supply is shared on the PCB, so a series ferrite bead will be required. In this case a ferrite was chosen with a lower DC resistance with almost the same frequency response as the bead used in the PLL only – Shared VAA_PLL supply on PCB. A BLM18SG121TN1 ferrite has DC resistance of 0.025 ohm in a slighter bigger 0603 package. IR drop through the bead will be 126mA x 0.025 ohms = 3.2mV. This is 3.2mV/1.8V = 0.18% of the IR drop budget. Assuming the Voltage regulator on the PCB takes 5% of the IR budget, 5% is left for ferrite bead, package, and on die routing. Assuming the package IR drop is 1.0%, on die IR drop is allowed to be 5% - 0.18% - 1.0% = 3.82% or 1.8V x 3.82% = 68.8mV. IR drop through the bumps and RDL will be (18mA *2 + 12mA) x (0.26ohms x 2) = 25mV. IR drop to the PLL will be an additional (0.26ohms x 12mA) = 3.1mV for a total of 25mV + 3.1mV = 28.1mV which is less than the limit (68.8mV).

The byte lanes require one PVAA_PLL cell which is located in the center of the byte lane to balance IR drop along the MVAA_PLL bus to the signal IO cells. Each MVAA_PLL bus has a branch of 6 IO cells . The resistance from PVAA_PLL pad to MVAA_PLL bus is 0.292 ohms (Gen 2 multiPHY databook). The horizontal bus resistance per IO cell is 0.292ohms (Gen 2 multiPHY databook). Assuming 2:1:1 signal to power to Ground IO cells so each signal IO is 3 cells away from each other.

IR drop from PVAA_PLL pad to MVAA_PLL bus = 18mA X 0.292ohms = 5mV

IR drop MVAA_PLL bus from PVAA_PLL cell to sixth signal IO cell =
(6 x 1.5mA) x (0.292ohms X 3 IO cells) +
(5 x 1.5mA) x (0.292ohms X 3 IO cells) +
(4 x 1.5mA) x (0.292ohms X 3 IO cells) +
(3 x 1.5mA) x (0.292ohms X 3 IO cells) +
(2 x 1.5mA) x (0.292ohms X 3 IO cells) +
(1 x 1.5mA) x (0.292ohms X 3 IO cells)
= 27.6mV

Total IR drop from PVAA_PLL bump to last IO cell = 25mV + 5mV + 27.6mV = 57.6mV

This is less than 68.6mV limit.

The same PCB decoupling caps and on die decoupling caps should be used as was recommended for the "PLL and IO RX VAA_PLL Supplies – Not shared on PCB" case.

PCB decoupling caps: one 10uF, one 2.2nF, one 220pF

On die decoupling caps at IO on VAA_PLL to VSSQ supply net: 10pF capacitance from VAA_PLL to VSSQ per signal IO. For example a byte lane with 11 IOs would require 11 X 10pF/IO = 110pF.

The 10pF/IO on die decap is required to reduce the switching noise on the VAA_PLL net due to the IO RX circuits. The VAA_PLL decap cells need to be added in the space between/around the PHY blocks and the IO cells or in between IO cells. The decap cells should be strapped to the PVAA_PLL bus of the IO cells in a direct manner as possible in higher die layers.

The PCB filter circuit is shown in Figure 28.

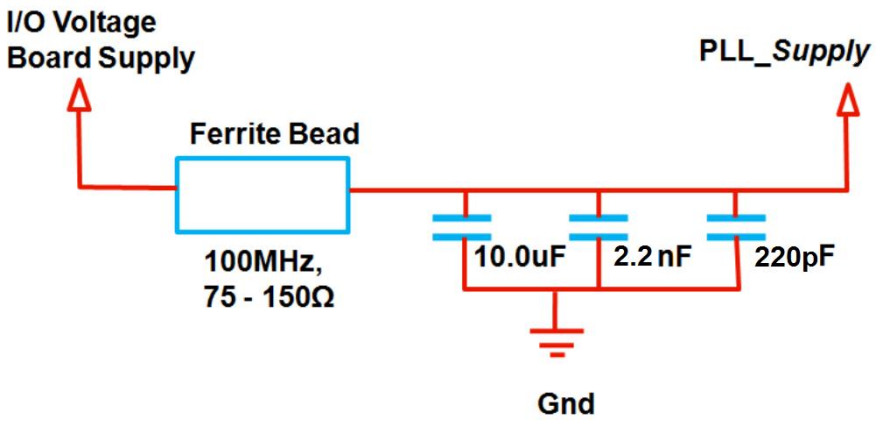

Figure 28: PCB filter for PLL and IO RX VAA_PLL Supplies - Shared on PCB

PLL and IO RX VAA_PLL Supplies – PDR=OFF constantly

In DDR systems where VAA_PLL supplies are used for both PLLs and IO RX, and, power savings are not required for IO RX power, the PDR pin of the IO RX can be left = 0 which leaves the IO RX powered up all the time. In this case the ac noise on the VAA_PLL supply due to IO RX switching currents is considerably reduced. This is because only IO RX AC currents are

switched, not AC and DC currents. For this system, no extra on –die VAA_PLL decoupling capacitance is required other than what is currently provided in the signal and power cells of the IO ring to sufficiently reduce the VAA_PLL supply noise to acceptable levels.

The guidelines established in the previous two sections for on PCB filter and bead in the case of "PLL and IO RX VAA_PLL Supplies – Shared on PCB" and for PCB filter in the case of "PLL and IO RX VAA_PLL Supplies – Not Shared on PCB" should still be adhered to even if PDR=0 constantly.

Note in all cases data from the proper databook should be used for the exact IP in the exact operating modes as required for a particular system. Both frequency domain and transient power supply network analysis should be performed to ensure the power network provides adequate performance.

Other Implementation Topics

Read Post-Amble Glitch

At the end of a read burst, when the SDRAM is no longer driving and the bus returns to its tri-state condition, there is the opportunity for a glitch to ring back and violate the switching threshold for the DQS or DQS#, potentially causing a Read data violation. To prevent these violations from occurring, a robust read gating circuit must be in place, supported by interconnect considerations to assure false data is not recorded. Figure 29 illustrates what a glitch typically looks like. Whether a glitch will be created can depend on the overall routed length of the interconnect, and the Output Disable delay time of the particular SDRAM device. Output Disable delays will vary from device to device.

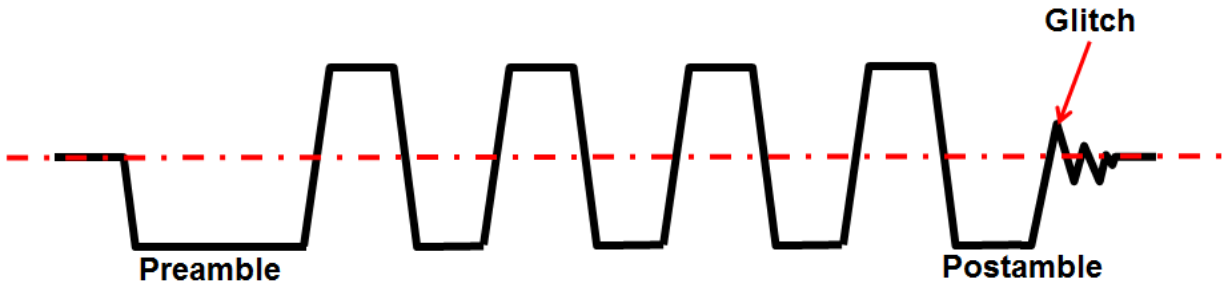

Figure 29: Illustration of glitch that can occur during Read Post-Amble

Impact of Routed Length on Read Post-Amble Glitch

Whether a glitch large enough to calls a false DQS toggle depends on the routed length of the electrical path between the host and the SDRAM. Figure 30 shows that on this example DDR3 interface, there is a delay of approximately 2.75n from the time when the output is disabled *for this particular SDRAM* to when the bus begins to tri-state. If the refection of the last DQS edge arrives back at the SDRAM before this net is tri-stated, a violating glitch will not be created. If the reflected signal arrives after the net has been tri-stated, the signal will hit a high impedance at the SDRAM and its amplitude will be doubled and reflected back to the host where a violation may occur.

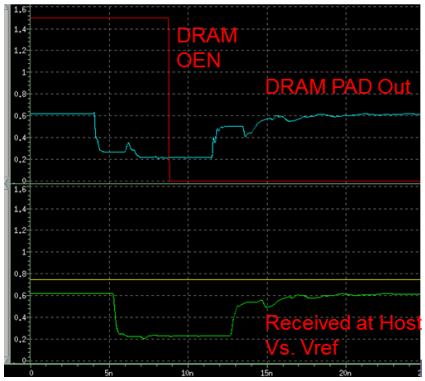

Figure 30: Delay between disable of SDRAM output to when the bus is tri-stated

Figure 31 shows how a violating glitch gets recreated as routed length grows. The waveforms for 1", 3" and 6" show the disable waveforms and the reflected DQS waveforms at the SDRAM pad and then back at the host pad. At 6", there is a clear violation that will cause a glitch.

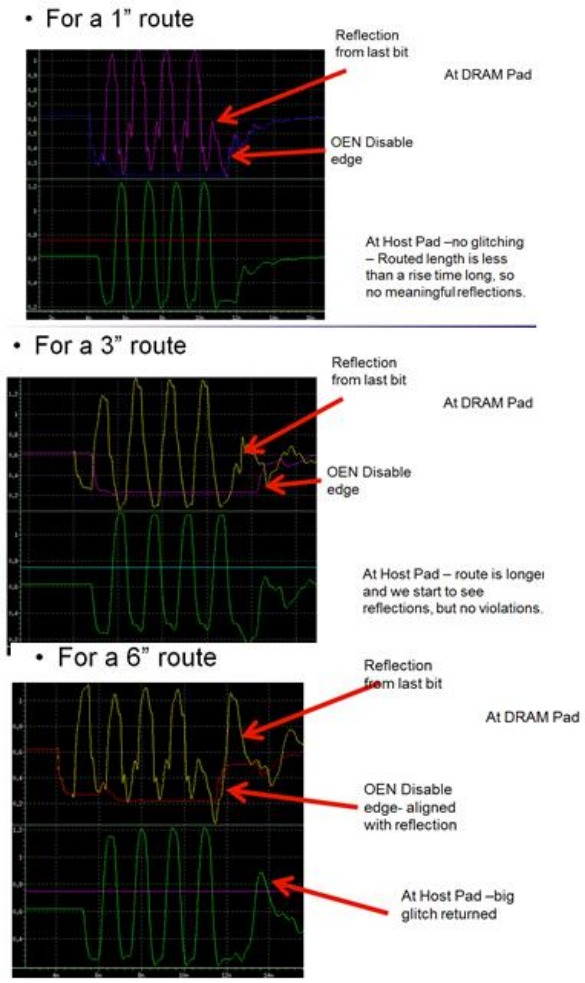

Figure 31: Glitch creation as a function of routed length

Note *Warning: The delays associated with tri-state and the time it takes to show up at the SDRAM pad can vary greatly between devices. The example here was ~2.75ns*

Suppression Methodology

The primary method for avoiding false Read data bits is Read gating which sets the window for when Read data can be captured. A more in depth discussion of Read Gating can be found in the PUB databook for the IP technology in question. In order to make this gating more effective, interconnect techniques can be used to either bias the DQS so the glitch does not violate the thresholds creating the opportunity for a false bit capture or using series resistance to squelch the glitch height. The DDR4 MultiPHY implements robust gating solution that duplicates the roundtrip Write/Read delay, precisely setting the gate and eliminated the need bias resistors on DDR3/DDR3L and DDR4 interfaces. LPDDR2 and LPDDR3 interfaces should still implement the bias during initial training since the initial.

Biasing DQS and DQS#

In order to improve the robustness of the Read DQS gating, pull down and pull up bias resistance is available in the PDIFF cells. Glitch suppression resistors are enabled when TE is high, OE is low, and at least one bit of DQSR[2:0] or DQSR[2:0] is nonzero.

They are automatically disabled in drive mode, when OE is high.This cell places a pull down bias resistor on the DQS net and a pull up bias resistor on the DQS# net. The available values of bias from 2.5KΩ to 355Ω. The resistors serve to pull the tri-stated signal level away from the switching threshold in order to avoid detection of false DQS edges.

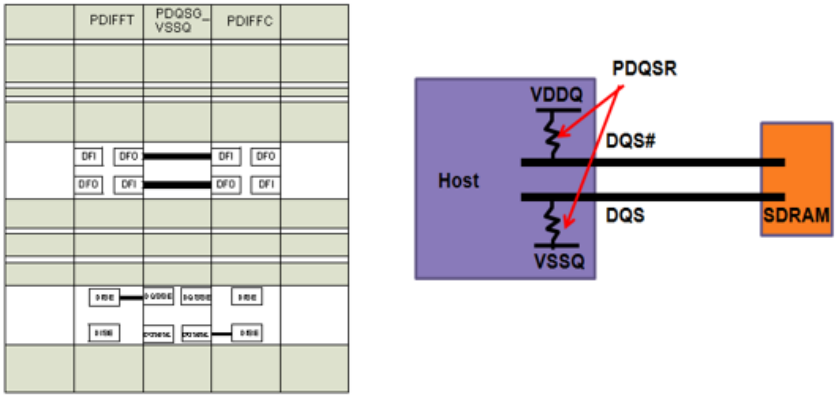

Figure 32: Bias Resistance placed on DQS and DQS# within the PDIFF Cells.

Series Resistance on DQS and DQS#

In some scenarios the amplitude of the Read post-amble glitch may become large and difficult to manage effectively with the bias resistance in the PDQS cell. In those cases, the implementation of series resistance on the DQS and DQS# should be considered. Placed near the balls of the host package, these can be used to significantly reduce the amplitude of the glitch. A typical value for these resistors would be 15Ω. Inclusion of the series resistance may also allow the implementer to use a higher bias resistance in the PDQS cell.

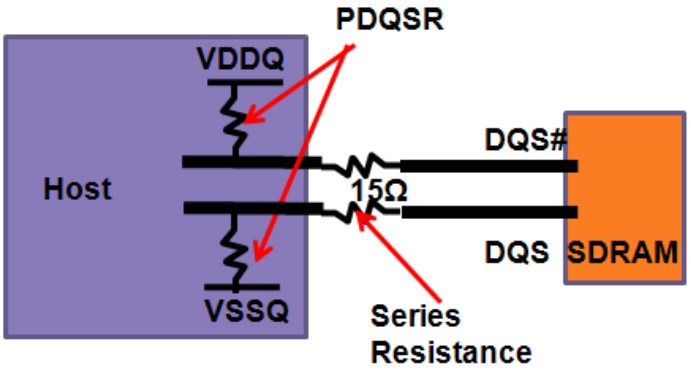

Figure 33: Placement of series resistance near package balls.

Timing Budgets for the DDR4 MultiPHY

Note

This section includes timing budgets for the supported protocols of the DDR4 MultiPHY IP. Some of the parameters included in the budget are process specific. An example of such a parameter would be power supply induced jitter, PSIJ. This can vary a small amount from process to process. The values included in this are based on the TSMC 28HPM process. When implementing the IP in other processes, these budgets are useful in determining the initial performance range of a particular interconnect environment.

When implementing a DDR interface, the primary determinant of overall functionality is whether the timing budget closes at the target bit rate. There are three primary components to any timing budget:

1. SDRAM Contributions
2. PHY Contributions
3. Interconnect Contributions

All of these contributors will erode the source synchronous timing of the SDRAM interface. SDRAM contributions should be obtained from the databook of the vendor of the SDRAM to be used. Values from JEDEC standards can also be used if they are available, though the vendor datasheets are always preferred.

Interconnect contributions are application specific and are the responsibility of the interface implementer. These contributions include crosstalk, skew, simultaneous switching noise, intersymbol interference, reflections, etc. These should be determined through measurement or simulation. Note that the maximum bit rates supported by JEDEC protocols typically represent point to point interconnect implementations. Interconnect environments other than point to point, such as multiple DIMM implementations, will result in a final supported bit rate lower than the maximum outlined in the JEDEC protocol.

PHY contributions include all those effects associated with the PLL, macro blocks and I/O during transmitting and receiver operations. These effects include skews, pulse width distortion, jitter effects and training errors. These effects are detailed within the timing budgets found in the foregoing sections. The budgets listed include all of the PHY components for each operation as well as the SDRAM contributions. These elements will be summed. The margin that remains will apply to the interconnect contributions.

This section will include budgets for DDR4-2667Mbps, DDR3-2133Mbps, DDR3L-1866Mbps, LPDDR3-2133Mbps and LPDDR2-1067Mbps.

DDR4 Protocol Timing Budgets-2667Mbps

Write Transaction Budget

Write transactions are driven from the host to the SDRAM. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when generating the DQ and DQS/DQS# signals and centering the strobe. These elements are related to the PLL, the Hard Macros (DATX8 or DATX4X2) and the I/O.

PLL

- PLL output period jitter. This is jitter on the rising edges of the X4X2, 2667MHz output that generates the rising and falling edges of the 2667Mbps DQ and DQS/DQS# signals. The negative peak period jitter will reduce the data valid window.

Hard Macro

- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the DQ vs. DQS/DQS#.
  - Register delay mismatch. The simulated PSIJ result also includes Clock to Q delay differences between the rising and falling edges of the DQ and DQS/DQS#.
- Training errors – This includes initial alignment error from per bit deskew and strobe centering, tap delay variation from ideal (INL) and VT drift of strobe centering between updates.

IO

- IO rise/fall skew. This captures the rising and falling edge delay differences measured at the output of the IO structure.

The eyes are captured at the SDRAM. Write timing does not use traditional set up and hold, but uses a rectangular mask of approximately 0.22UI. This opening will vary with the specified bit rate. When the mask is not violated, the interface should support operation at BER=1E-16.

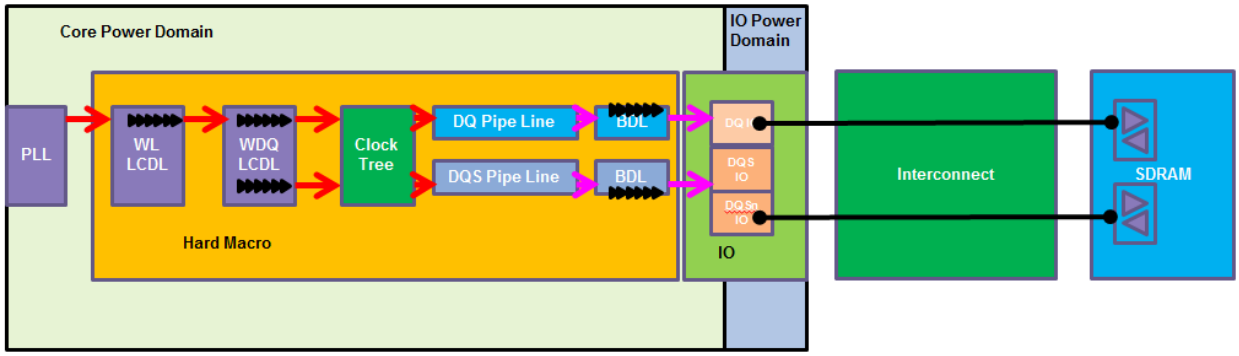

Figure 34: Illustration of PHY components for Write Budget.

PHY and SDRAM timing budget contributions for DDR4 Write operation at 2667Mbps						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT_DQ	PLL Clock Source Jitter	Output Perid Jitter. This is based on ps-RMS multiplied by 16.444 to support BER=1e-16. Based on CK/CK# spec, RJ should max out at approximately 0.1UI for this BER. That is 37.5ps at 2667Mbps. The negative peak, -18.75ps, should be applied against the Write budget.	9	9	Variable Offset (PLL)
	T_PSIJ_W	**PowerSupply Induced Jitter**	**This is the relative jitter between the DQ and DQS/DQS# signals that erodes the set up and hold margins. This is characterized at thecore side input to the I/O cell during Write operations. This is a result of multitone noise of +/-2% of the core voltage. This simulation is performed under worst case PVT conditions. This result includes the PSIJ effects as well as any pulse width distortion introduced by differences of rising and falling edge delays within a single macro path.**	26	26	Mostly variable offset. Small static component from pulse width distortion of the macro paths. (Hard Macro)
	T_DL_ERR	**DDL Placement Error**	**Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity. 10ps average delay in worst case PVT corner. 1 tap could apply to set up or hold.**	10	0	Static Offset (Hard Macro)
	T_DL_VT_DRIFT	**VT Drift**	**Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. 1 tap could apply to set up or hold.**	0	10	Variable Offset (Hard Macro)
	T_DL_INL	**Tap Delay variation**	**This assums that there is 10ps of difference between the average tap delay and the maximum tap delay.**	10	0	Static Offset (Hard Macro)
	T_SK_I/O	**I/O Rise/Fall Skew**	**Propagation delay differences between rising and falling edges within the I/O Write path. The effect is pulse width distortion that can impact both set up and hold, depending upon the data pattern.**	6	6	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Transmitter (PHY) Uncertainty				62	52	30% of Budget consumed by PHY
Receiver Contributions	T_Mask_W	**Input Eye Mask**	**SDRAM Receiver Window Requirements - 0.22UI to support BER=1e-16.**	41	41	Static offset
Total Receiver (SDRAM) Uncertainty				41	41	22% of Budget consumed by SDRAM
			Total Contributions for End to End Timing	103	93	Total Budget Consumed, 52%
			Absolute Worst Case Margin at 2667 MBPS (Budget = 188 ps.) (Varies with Bit Rate)	85	95	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
			Set up and hold contributions after strobe is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).	95	85	

Table 6: Write Budget for DDR4

Read Transaction Budget

Read transactions are driven from the SDRAM to the Host. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when capturing the DQ and DQS/DQS# signals and centering the strobe. These elements are related to the Hard Macros (DATX8 or DATX4X2) and the I/O.

Hard Macro

- First Flop Set Up and Hold – This is the window required to capture the DQ signals with the rising edges of the DQS and DQS#
- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the DQ vs. DQS/DQS#.
- Training errors – This includes initial alignment error from per bit deskew and strobe centering, tap delay variation from ideal (INL) and VT drift of strobe centering between updates.

IO

- IO rise/fall skew. This captures the rising and falling edge delay differences measured at the core output of the IO structure.
- IO Intersymbol Interference. This captures the impact of ISI from the receiver path on timing.
- Vref Uncertainty. Vertical differences from the ideal Vref across the byte vs. the trained Vcent level will result in small timing contributions captured here.

The output timing from the SDRAM is captured with a data valid window spec. Additionally, the SDRAM output data valid window spec must be derated by the negative peak input period jitter.

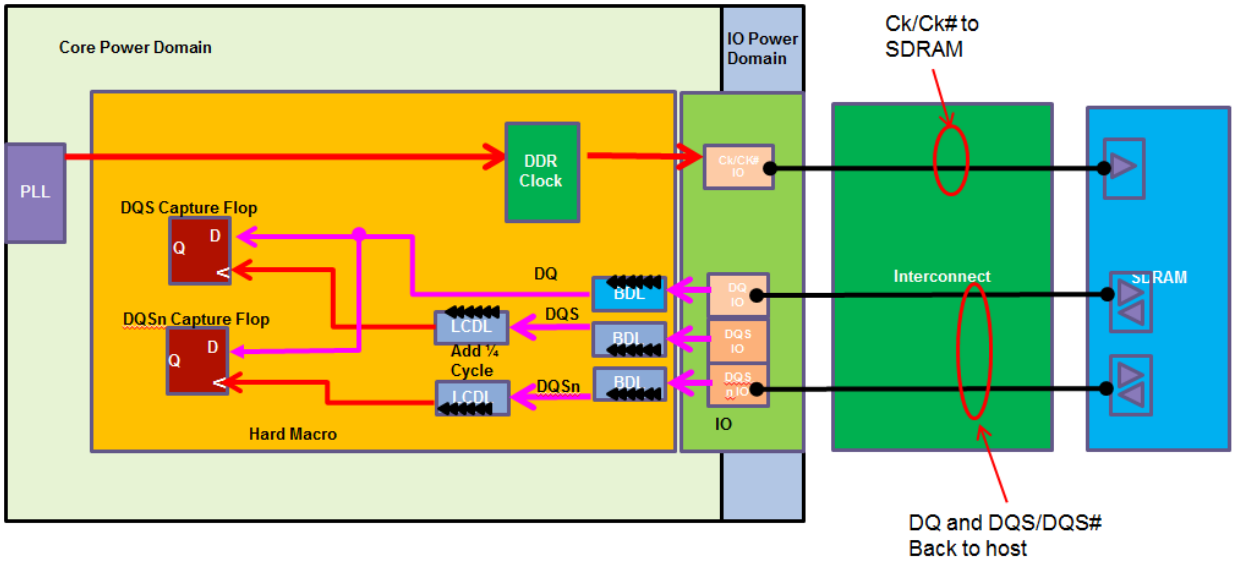

Figure 35: Illustration of PHY components for Read Budget.

PHY and SDRAM timing budget contributions for DDR4 Read operation at 2667Mbps						
Skew and Jitter Components		Parameter Name	Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable			Set Up Contribution	Hold Contribution	
Transmitter Contributions	**T_DV_p**	**Data valid Window per pin**	**This value assumes data training and no data bus inversion. The data valid window is 0.72UI (varies with bit rate). The uncertainty that defines the DVW is applied to the budget.**	52	52	Static Offset (SDRAM)
	T_SD_RJIT	**Input Period Jitter Derating**	**Derating for CK/CK# input negative period jitter. Specification max of -0.1UI applied This budget assumes the specification is met.**	19	19	Variable (PHY and Inteconnect)
Total Transmitter (SDRAM) Uncertainty				71	71	Budget consumed by SDRAM, 38%
Receiver Contributions	T_SUH	**Flip Flop Set Up and Hold**	**Set Up and Hold requirement at the Receive flip flop during Read operations.**	19	19	Static Offset (Hard Macro)
	T_DL_ERR	**Delay Line Placement Error**	**Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity.**	10		Static Offset (Hard Macro)
	T_DL_VT_DRIFT	**VT Drift of the delay line.**	**Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. Assume the placement can drift either way.**		10	Variable (Hard Macro)
	T_DL_INL	**Tap Delay variation**	**This assumes that there is 10ps of difference between the average tap delay and the maximum tap delay.**	10	0	Static Offset (Hard Macro)
	T_PSIJ_R	Power Supply Induced Jitter	**Relative jitter between DQ and DQS from +/- 2% multitone noise on the Read macro receive path from the I/O to the first flop**	10	10	Variable (Hard Macro)
	T_VR_UNC	**Vref Uncertainty**	**Set Up and Hold penalty associated with VREF step size training granularity.**	4	4	Variable (IO)
	T_SK_IO_In	I/O Rise/Fall Skew	**Propagation delay differences between rising and falling edges within the I/O Read path. The effect is pulse width distortion that can impact both set up and hold.**	2	2	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
	T_SK_ISI	I/O intersymbol interference	**ISI from the reciever path seen at the core side outout of the receiver.**	3	3	Variable Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Receiver (PHY) Uncertainty				58	48	Budget Consumed by PHY, 28%
			Total Contributions for End to End Timing	129	119	Total Budget Consumed, 66%
			Absolute Worst Case Margin at 2667 MBPS (Budget = 188 ps.) (Varies with Bit Rate)	58	68	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
			Set up and hold contributions after strobe is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).	68	58	

Table 7: Read Budget for DDR4

Command/Address /Control Transaction Budget

Cmd/Add/Ctrl transactions are driven from the host to the SDRAM. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when generating the DQ and DQS/DQS# signals and centering the strobe. These elements are related to the PLL, the Hard Macro (PHYAC) and the I/O.

PLL

- PLL output period jitter. This is jitter on the rising edges of the X4X2, 2667MHz output that generates the rising and falling edges of the 1333MHz CA and Ck/Ck# signals. The negative peak period jitter will reduce the data valid window.

Hard Macro

- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the CA vs. Ck/Ck#.
  - Register delay mismatch. The simulated PSIJ result also includes Clock to Q delay differences between the rising and falling edges of the CA and Ck/Ck#.
- PHY Skew – There is no training on the Cmd/Add/Ctrl bus, so skew within the hard macro must be accounted for. Per the implementation guide this is limited to 4% of a clock cycle including OCV effects per the IP implementation guide.

IO

- IO rise/fall skew. This captures the rising and falling edge delay differences measured at the output of the IO structure.
- Process Variation Effects captures the variation in output delay associated with variation of silicon process across the CA bus.

The eyes are captured at the SDRAM. CA timing uses traditional set up and hold values based on AC and DC threshold levels. Additionally, a derating effect must be applied when the input slew rate exceeds 1V/ns.

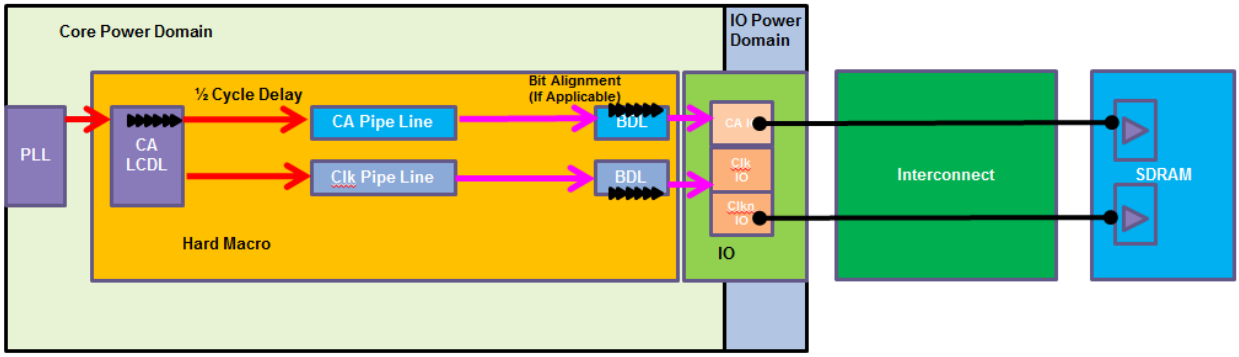

Figure 36: Illustration of PHY components for Cmd/Add/Ctrl Budget.

PHY and SDRAM timing budget contributions for DDR4 Single Data Rate Command/Address operation at 2667Mbps						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT_CA	**PLL Clock Source Jitter**	**Output Jitter from PLL. The negative peak period jitter will reduce the data valid window. This value is divided between set up and hold.**	3	3	Variable (PLL)
	T_PSIJ_CA	**PowerSupply Induced Jitter**	**This is the relative jitter between the CA signals and the rising edge of the CK/CK## signals that erodes the set up and hold margins. This is characterized at thecore side input to the I/O cell during CA operations. This is a result of multitone noise of +/-2% of the core voltage. This simulation is performed under worst case PVT conditions. This result includes the PSIJ effects as well as any pulse width distortion introduced by differences of rising and falling edge delays within a single macro path.**	29	29	Mostly variable offset. Small static component from pulse width distortion of the macro paths. (Hard Macro)
	T_SK	**PHY Skew between CK/CK# and CA signals**	**This accounts for skew variations in PHY cell placement. 4% of a clock cycle total**	15	15	Static Offset (Hard Macro)
	T_PROC_SK	**Process Variation Effects**	**This value captures the timing effects of local process variation that can occur across a CA lane.**	25	25	Static Offset (IO)
	T_SK_I/O	I/O Rise/Fall Skew	**Propagation delay differences between rising and falling edges within the I/O Write path. The effect is pulse width distortion that can impact both set up and hold, depending upon the data pattern.**	6	6	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Transmitter Uncertainty				75	75	Budget consumed by PHY, 20%
Receiver Contributions	T_SU_CA, T_H_CA	CA Setup/hold	Set up and Hold Specifications at AC90 and DC65	55	80	Static Offset.
	T_SD_DER_CA, T_H_DER_CA	Set up and Hold Derating	Derating factor applied to set up and hold specification to account for slew rates greater than specification	45	33	
Total Receiver Uncertainty				100	113	Budget consumed by SDRAM, 28%.
				175	188	Total Budget Consumed, 48%
Absolute Worst Case Margin at 2667 MBPS (SDR Budget = 375 ps.)				200	187	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.

Table 8: Cmd/Add/Ctrl Budget for DDR4

tDQSS (DQS/DQS# to CK/CK#) Transaction Budget

tDQSS spec describes DQS rising edge to CLK rising edge alignment during transactions are driven from the host to the SDRAM, which can be improved by Write Leveling training. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. There are separate PHY blocks in this transaction. The clock is driven from the PHYAC block while each of the DQS pairs are driven from separate DATX8 blocks. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when generating the CK/CK# and DQS/DQS# and then aligning them with the write leveling functionality. These elements are related to the PLL and the Hard Macro.

PLL

- PLL output period jitter. This is jitter on the rising edges of the X4X2, 2667MHz output. Since there are two PLLs we will add the jitter from both of them in a square root of the sum of the squares manner

Hard Macro

- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the DQS/DQS# relative to the CK/CK#. There is period jitter on both of these, so they are added in an RSS manner as well.
- Training errors – This includes initial alignment error from write leveling, tap delay variation from ideal (INL) and VT drift of strobe alignment between updates.

tDQSS timing requires that the DQS/DQS# rising edges arrive within 0.27 of a clock cycle of the CK/CK# rising edges. To aid this, Write Leveling is used. In order for this to work, the SDRAM will consume +/- 0.13UI of the available budget to assure alignment.

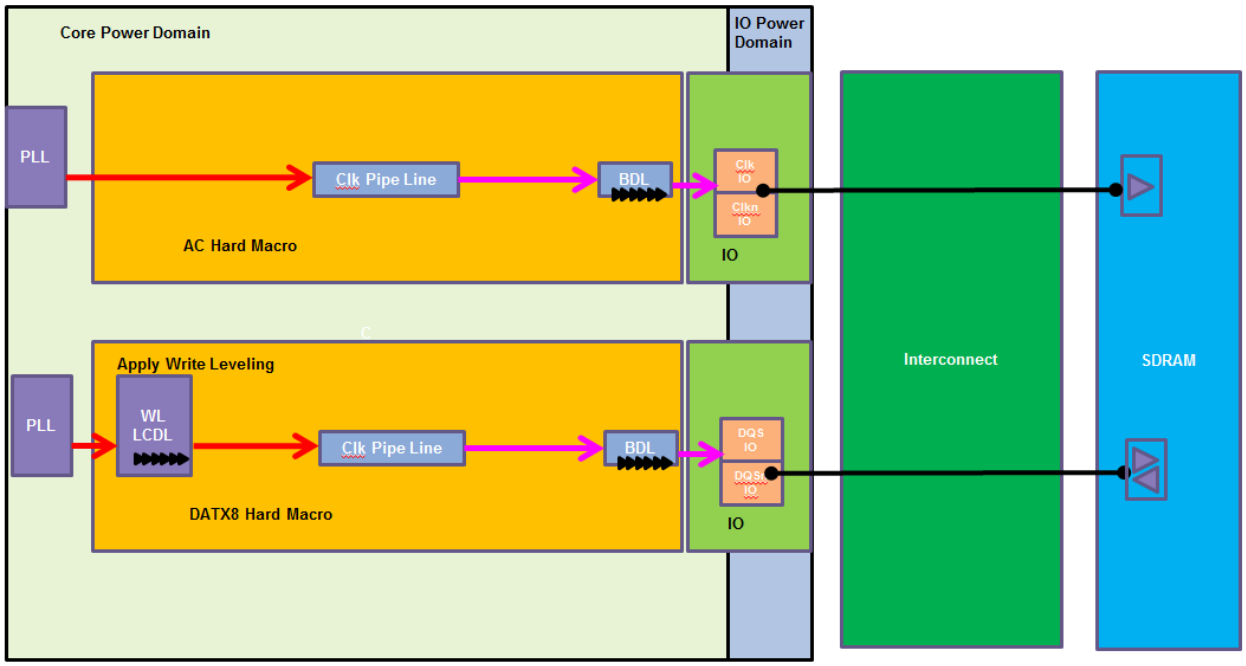

Figure 37: Illustration of PHY components for tDQSS Budget.

PHY and SDRAM timing budget contributions for DDR4 Write Leveling operation at 2667Mbps.						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT (CK and DQS)	**PLL Clock Source Jitter**	**This assumes an ideal reference clock source. +/- 6ps period jitter for each, added as RSS.**	8	8	Variable (PLL)
	T_DIST_NOISE (CK and DQS)	PHY Clock Distribution Noise	Noise induced p-p period jitter on the clock tree for CK and DQS path. +/-28ps period jitter on each path, added as RSS.	40	40	Variable (Hard Macro)
	T_DL_ERR	**DDL Placement Error**	**Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity.**	10		Static Offset (Hard Macro)
	T_DL_VT_DRIFT	**VT Drift**	**Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. Assume the placement can drift either way.**		10	Static Offset (Hard Macro)
	T_DL_INL	**Tap Delay variation**	**This assums that there is 10ps of difference between the average tap delay and the maximum tap delay.**	10	0	Static Offset (Hard Macro)
	T_Comp_Error	**Uncompensated Delay Differences**	**Account for uncompensated VT differences that can aoccur across a large die.**	10	10	Variable (Hard Macro)
Total Transmitter Uncertainty				78	68	Budget consumed by PHY, 36%
Receiver Contributions	**T_WL_SUH**	**Write Leveling Set Up and Hold**	**Set Up and Hold requirement for CK/CK# relative to DQS/DQS# 0.13UI**	97	97	Static Offset
Total Receiver Uncertainty				97	97	Budget consumed by SDRAM, 48%
Total Contributions for End to End Timing				176	166	Total Budget Consumed, 84%
Absolute Worst Case Margin at 1333MHz (Budget = 203 ps., 0.27 of a Clock Cycle.)				27	37	The % of the available budget that remains will be available for inteconnect induced jitter. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Absolute Worst Case Margins with Strobe Alignment				37	27	

Table 9: tDQSS Budget for DDR4

DDR3 Protocol Timing Budgets-2133Mbps

Write Transaction Budget

Write transactions are driven from the host to the SDRAM. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when generating the DQ and DQS/DQS# signals and centering the strobe. These elements are related to the PLL, the Hard Macros (DATX8 or DATX4X2) and the I/O.

PLL

- PLL output period jitter. This is jitter on the rising edges of the X4X2, 2133MHz output that generates the rising and falling edges of the 2133Mbps DQ and DQS/DQS# signals. The negative peak period jitter will reduce the data valid window.

Hard Macro

- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the DQ vs. DQS/DQS#.
  - Register delay mismatch. The simulated PSIJ result also includes Clock to Q delay differences between the rising and falling edges of the DQ and DQS/DQS#.
- Training errors – This includes initial alignment error from per bit deskew and strobe centering, tap delay variation from ideal (INL) and VT drift of strobe centering between updates.

IO

- IO rise/fall skew. This captures the rising and falling edge delay differences measured at the output of the IO structure.

The eyes are captured at the SDRAM. Traditional set up and hold timing is used for the DDR3 protocol. Additionally, there is a derating factor that is applied to adjust for slew rates greater than 2V/ns at 2133Mbps. These budgets assume a maximum slew rate derating per the JEDEC derating tables.

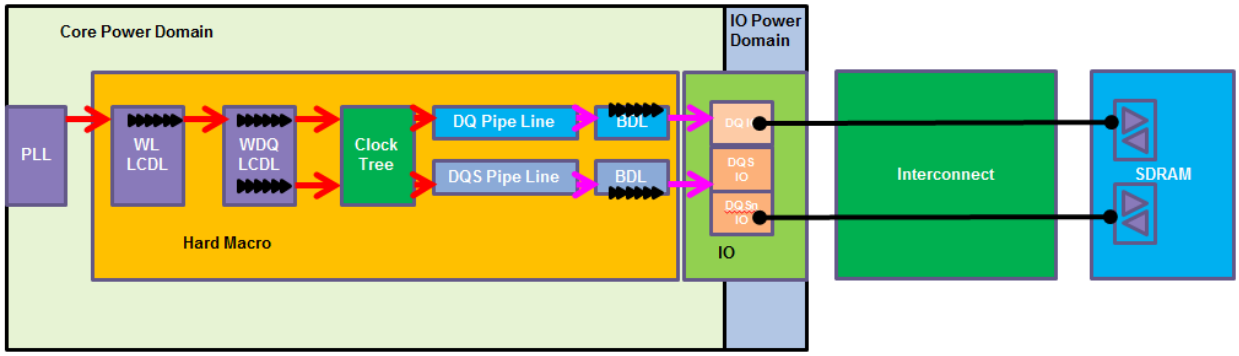

Figure 38: Illustration of PHY components for Write Budget.

PHY and SDRAM timing budget contributions for DDR3 Write operation at 2133Mbps						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT_DQ	PLL Clock Source Jitter	Output Perid Jitter. This is the output negative period jitter over 200 cycles. This is -7.5ps to be divided between set up and hold.	4	4	Variable Offset (PLL)
	T_PSIJ_W	PowerSupply Induced Jitter	This is the relative jitter between the DQ and DQS/DQS# signals that erodes the set up and hold margins. This is characterized at thecore side input to the I/O cell during Write operations. This is a result of multitone noise of +/-2% of the core voltage. This simulation is performed under worst case PVT conditions. This result includes the PSIJ effects as well as any pulse width distortion introduced by differences of rising and falling edge delays within a single macro path.	26	26	Mostly variable offset. Small static component from pulse width distortion of the macro paths. (Hard Macro)
	T_DL_ERR	DDL Placement Error	Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity. 10ps average delay in worst case PVT corner. 1 tap could apply to set up or hold.	10	0	Static Offset (Hard Macro)
	T_DL_VT_DRIFT	VT Drift	Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. 1 tap could apply to set up or hold.	0	10	Variable Offset (Hard Macro)
	T_DL_INL	Tap Delay variation	This assums that there is 10ps of difference between the average tap delay and the maximum tap delay.	10	0	Static Offset (Hard Macro)
	T_SK_I/O	I/O Rise/Fall Skew	Propagation delay differences between rising and falling edges within the I/O Write path. The effect is pulse width distortion that can impact both set up and hold, depending upon the data pattern.	3	3	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Transmitter (PHY) Uncertainty				53	43	20% of Budget consumed by PHY
Receiver Contributions	T_SUH	Set Up and Hold	Set Up and Hold Requirement at AC135, DC100 with 2V/ns slew rate	53	55	Static offset
	T_Derate	Derating Factor	Derating factor for input slew rate greater than 2V/ns.	34	25	Static Offset.
Total Receiver (SDRAM) Uncertainty				87	80	37% of Budget consumed by SDRAM
Total Contributions for End to End Timing				140	123	Total Budget Consumed, 57%
Absolute Worst Case Margin at 2133 MBPS (Budget = 234 ps.) (Varies with Bit Rate)				94	111	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Set up and hold contributions after strobe is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).				104	101	

Table 10: Write Budget for DDR3

Read Transaction Budget

Read transactions are driven from the SDRAM to the Host. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when capturing the DQ and DQS/DQS# signals and centering the strobe. These elements are related to the Hard Macros (DATX8 or DATX4X2) and the I/O.

Hard Macro

- First Flop Set Up and Hold – This is the window required to capture the DQ signals with the rising edges of the DQS and DQS#
- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the DQ vs. DQS/DQS#.
- Training errors – This includes initial alignment error from per bit deskew and strobe centering, tap delay variation from ideal (INL) and VT drift of strobe centering between updates.

IO

- IO rise/fall skew. This captures the rising and falling edge delay differences measured at the core output of the IO structure.
- IO Intersymbol Interference. This captures the impact of ISI from the receiver path on timing.
- Vref Uncertainty. Vertical differences from the ideal Vref across the byte vs. the trained Vcent level will result in small timing contributions captured here.

The output timing from the SDRAM is captured with an output skew spec, tDQSQ, and a data hold spec, tQH. This is a very conservative timing methodology for the SDRAM as these are maximum values across all devices and PVT corners.

Additionally, the SDRAM output data valid window spec must be derated by the negative peak input period jitter.

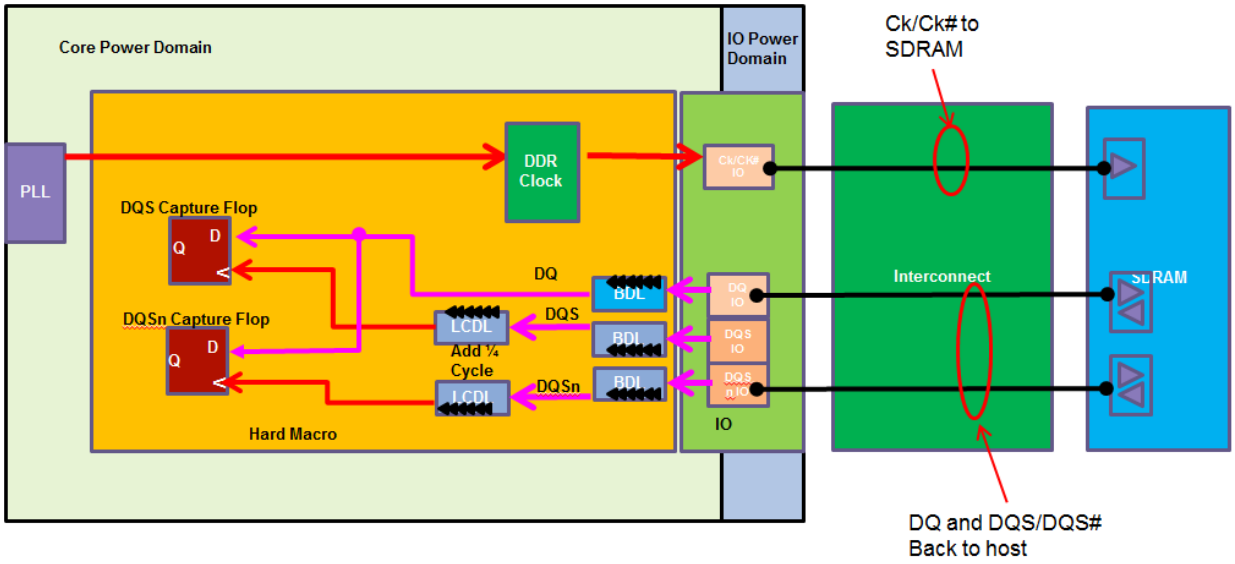

Figure 39: Illustration of PHY components for Read Budget.

PHY and SDRAM timing budget contributions for DDR3 Read operation at 2133Mbps						
Skew and Jitter Components		Parameter Name	Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable			Set Up Contribution	Hold Contribution	
Transmitter Contributions	**T_DV_p**	**Data valid Window per pin**	**The set up contirbution is the SDRAM output skew spec, tDQSQ. The hold element is 0.12*tCK. Based on the output hold requirement tQH=0.38*tCK.**	75	113	Static Offset (SDRAM)
	T_SD_RJIT	**Input Period Jitter Derating**	**Derating for CK/CK# input negative period jitter. Specification max of -50ps applied. This budget assumes the specification is met.**	25	25	Variable (PHY and Inteconnect)
Total Transmitter (SDRAM) Uncertainty				100	138	Budget consumed by SDRAM, 51%
Receiver Contributions	T_SUH	**Flip Flop Set Up and Hold**	**Set Up and Hold requirement at the Receive flip flop during Read operations.**	19	19	Static Offset (Hard Macro)
	T_DL_ERR	**Delay Line Placement Error**	**Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity.**	10		Static Offset (Hard Macro)
	T_DL_VT_DRIFT	**VT Drift of the delay line.**	**Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. Assume the placement can drift either way.**		10	Variable (Hard Macro)
	T_DL_INL	**Tap Delay variation**	**This assumes that there is 10ps of difference between the average tap delay and the maximum tap delay.**	10	0	Static Offset (Hard Macro)
	T_PSIJ_R	Power Supply Induced Jitter	**Relative jitter between DQ and DQS from +/- 2% multitone noise on the Read macro receive path from the I/O to the first flop**	10	10	Variable (Hard Macro)
	T_VR_UNC	**Vref Uncertainty**	**Set Up and Hold penalty associated with AC Noise on VREF**	4	4	Variable (IO)
	T_SK_IO_In	I/O Rise/Fall Skew	**Propagation delay differences between rising and falling edges within the I/O Read path. The effect is pulse width distortion that can impact both set up and hold.**	1	1	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
	T_SK_ISI	I/O intersymbol interference	**ISI from the reciever path seen at the core side outout of the receiver.**	2	2	Variable Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Receiver (PHY) Uncertainty				56	46	Budget Consumed by PHY, 22%
Total Contributions for End to End Timing				156	184	Total Budget Consumed, 73%
Absolute Worst Case Margin at 2133 MBPS (Budget = 234 ps.) (Varies with Bit Rate)				78	51	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Set up and hold contributions after strobe is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).				68	61	

Table 11: Read Budget for DDR3

Command/Address /Control Transaction Budget

Cmd/Add/Ctrl transactions are driven from the host to the SDRAM. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when generating the DQ and DQS/DQS# signals and centering the strobe. These elements are related to the PLL, the Hard Macro (PHYAC) and the I/O.

PLL

- PLL output period jitter. This is jitter on the rising edges of the X4X2, 2133MHz output that generates the rising and falling edges of the 1067MHz CA and Ck/Ck# signals. The negative peak period jitter will reduce the data valid window.

Hard Macro

- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the CA vs. Ck/Ck#.
  - Register delay mismatch. The simulated PSIJ result also includes Clock to Q delay differences between the rising and falling edges of the CA and Ck/Ck#.
- PHY Skew – There is no training on the Cmd/Add/Ctrl bus, so skew within the hard macro must be accounted for. Per the implementation guide this is limited to 4% of a clock cycle including OCV effects per the IP implementation guide.

IO

- IO rise/fall skew. This captures the rising and falling edge delay differences measured at the output of the IO structure.
- Process Variation Effects captures the variation in output delay associated with variation of silicon process across the CA bus.

The eyes are captured at the SDRAM. CA timing uses traditional set up and hold values based on AC and DC threshold levels. Additionally, a derating effect must be applied when the input slew rate exceeds 1V/ns.

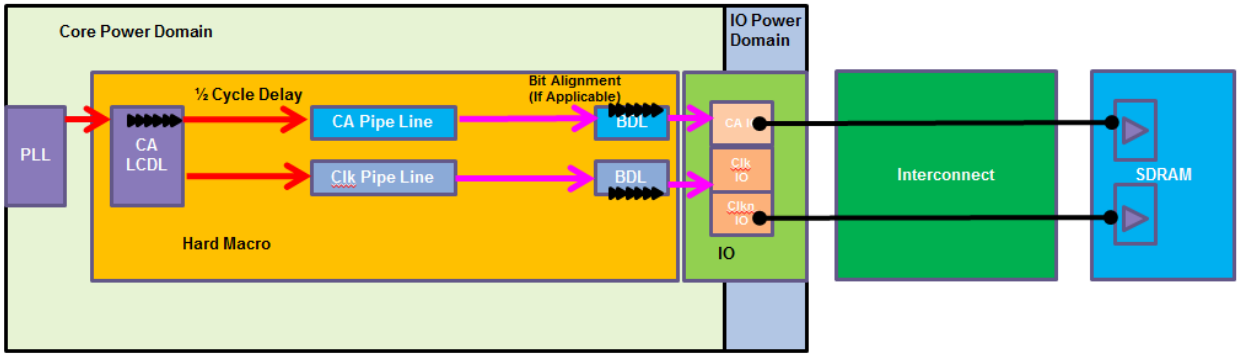

Figure 40: Illustration of PHY components for Cmd/Add/Ctrl Budget.

PHY and SDRAM timing budget contributions for DDR3 Single Data Rate Command/Address operation at 2133Mbps						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT_CA	**PLL Clock Source Jitter**	**Output Jitter from PLL. The negative peak period jitter will reduce the data valid window. This value is divided between set up and hold.**	4	4	Variable (PLL)
	T_PSIJ_CA	**PowerSupply Induced Jitter**	**This is the relative jitter between the CA signals and the rising edge of the CK/CK## signals that erodes the set up and hold margins. This is characterized at thecore side input to the I/O cell during CA operations. This is a result of multitone noise of +/-2% of the core voltage. This simulation is performed under worst case PVT conditions. This result includes the PSIJ effects as well as any pulse width distortion introduced by differences of rising and falling edge delays within a single macro path.**	29	29	Mostly variable offset. Small static component from pulse width distortion of the macro paths. (Hard Macro)
	T_SK	**PHY Skew between CK/CK# and CA signals**	**This accounts for skew variations in PHY cell placement. 4% of a clock cycle total**	19	19	Static Offset (Hard Macro)
	T_PROC_SK	**Process Variation Effects**	**This value captures the timing effects of local process variation that can occur across a CA lane.**	25	25	Static Offset (IO)
	T_SK_I/O	I/O Rise/Fall Skew	**Propagation delay differences between rising and falling edges within the I/O Write path. The effect is pulse width distortion that can impact both set up and hold, depending upon the data pattern.**	3	3	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Transmitter Uncertainty				76	76	Budget consumed by PHY, 16%
Receiver Contributions	T_SU_CA, T_H_CA	CA Setup/hold	Set up and Hold Specifications at AC135 and DC100	60	95	Static Offset.
	T_SD_DER_CA, T_H_DER_CA	Set up and Hold Derating	Derating factor applied to set up and hold specification to account for slew rates greater than specification	68	50	
Total Receiver Uncertainty				128	145	Budget consumed by SDRAM, 30%.
Total Contributions.				204	221	Total Budget Consumed, 46%
Absolute Worst Case Margin at 2133 MBPS (SDR Budget = 469 ps.)				265	248	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.

Table 12: Cmd/Add/Ctrl Budget for DDR3

tDQSS (DQS/DQS# to CK/CK#) Transaction Budget

tDQSS spec describes DQS rising edge to CLK rising edge alignment during transactions are driven from the host to the SDRAM, which can be improved by Write Leveling training. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. There are separate PHY blocks in this transaction. The clock is driven from the AC block while each of the DQS pairs are driven from separate DATX8 blocks. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when generating the CK/CK# and DQS/DQS# and then aligning them with the write leveling functionality. These elements are related to the PLL and the Hard Macro.

PLL

- PLL output period jitter. This is jitter on the rising edges of the X4X2, 2133MHz output. Since there are two PLLs we will add the jitter from both of them in a square root of the sum of the squares manner

Hard Macro

- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the DQS/DQS# relative to the CK/CK#. There is period jitter on both of these, so they are added in an RSS manner as well.
- Training errors – This includes initial alignment error from write leveling, tap delay variation from ideal (INL) and VT drift of strobe alignment between updates.

tDQSS timing requires that the DQS/DQS# rising edges arrive within 0.27 of a clock cycle of the CK/CK# rising edges. To aid this, Write Leveling is used. In order for this to work, the SDRAM will consume +/- 125ps the available budget to assure alignment.

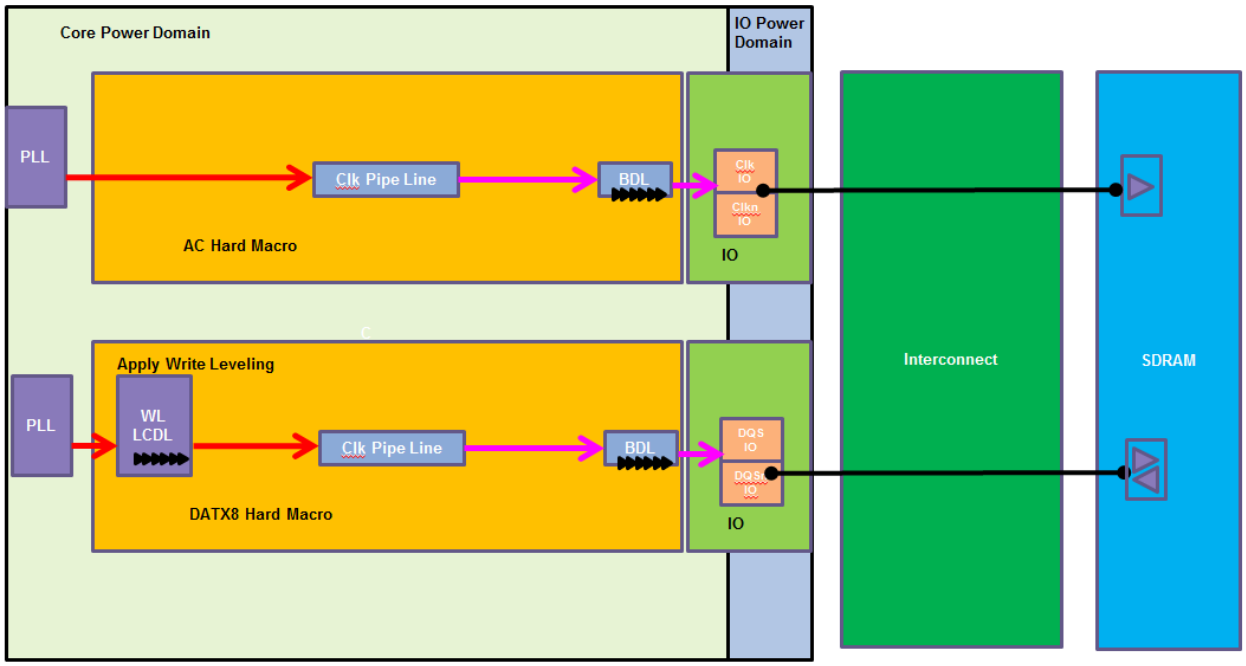

Figure 41: Illustration of PHY components for tDQSS Budget.

PHY and SDRAM timing budget contributions for DDR3 Write Leveling operation at 2133Mbps.						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT (CK and DQS)	**PLL Clock Source Jitter**	**This assumes an ideal reference clock source. +/- 7.5ps period jitter for each, added as RSS.**	11	11	Variable (PLL)
	T_DIST_NOISE (CK and DQS)	PHY Clock Distribution Noise	Noise induced p-p period jitter on the clock tree for and DQS path. +/-29ps period jitter on each path, added as RSS.	41	41	Variable (Hard Macro)
	T_DL_ERR	**DDL Placement Error**	**Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity.**	10		Static Offset (Hard Macro)
	T_DL_VT_DRIFT	**VT Drift**	**Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. Assume the placement can drift either way.**		10	Static Offset (Hard Macro)
	T_DL_INL	**Tap Delay variation**	**This assums that there is 10ps of difference between the average tap delay and the maximum tap delay.**	10	0	Static Offset (Hard Macro)
	T_Comp_Error	**Uncompensated Delay Differences**	**Account for uncompensated VT differences that can aoccur across a large die.**	10	10	Variable (Hard Macro)
Total Transmitter Uncertainty				82	72	Budget consumed by PHY, 30%
Receiver Contributions	**T_WL_SUH**	**Write Leveling Set Up and Hold**	**Set Up and Hold requirement for CK/CK# relative to DQS/DQS#**	125	125	Static Offset
Total Receiver Uncertainty				125	125	Budget consumed by SDRAM, 49%
Total Contributions for End to End Timing				207	197	Total Budget Consumed, 79%
Absolute Worst Case Margin at 1067MHz (Budget = 253 ps., 0.27 of a Clock Cycle.)				46	56	The % of the available budget that remains will be available for inteconnect induced jitter. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Absolute Worst Case Margins with Strobe Alignment				56	46	

Table 13: tDQSS Budget for DDR3

DDR3L Protocol Timing Budgets-1866Mbps

DDR3L protocol has the same structure for all budgets as the DDR3. The budget tables for DDR3L are included below. For an in depth description of the budget structure, please refer to the DDR3 section above.

Write Transaction Budget

PHY and SDRAM timing budget contributions for DDR3L Write operation at 1866Mbps						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT_DQ	PLL Clock Source Jitter	Output Perid Jitter. This is the output negative period jitter over 200 cycles. This is -9ps to be divided between set up and hold.	5	5	Variable Offset (PLL)
	T_PSIJ_W	PowerSupply Induced Jitter	This is the relative jitter between the DQ and DQS/DQS# signals that erodes the set up and hold margins. This is characterized at thecore side input to the I/O cell during Write operations. This is a result of multitone noise of +/-2% of the core voltage. This simulation is performed under worst case PVT conditions. This result includes the PSIJ effects as well as any pulse width distortion introduced by differences of rising and falling edge delays within a single macro path.	26	26	Mostly variable offset. Small static component from pulse width distortion of the macro paths. (Hard Macro)
	T_DL_ERR	DDL Placement Error	Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity. 10ps average delay in worst case PVT corner. 1 tap could apply to set up or hold.	10	0	Static Offset (Hard Macro)
	T_DL_VT_DRIFT	VT Drift	Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. 1 tap could apply to set up or hold.	0	10	Variable Offset (Hard Macro)
	T_DL_INL	Tap Delay variation	This assums that there is 10ps of difference between the average tap delay and the maximum tap delay.	10	0	Static Offset (Hard Macro)
	T_SK_I/O	I/O Rise/Fall Skew	Propagation delay differences between rising and falling edges within the I/O Write path. The effect is pulse width distortion that can impact both set up and hold, depending upon the data pattern.	5	5	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Transmitter (PHY) Uncertainty				56	46	19% of Budget consumed by PHY
Receiver Contributions	T_SUH	Set Up and Hold	Set Up and Hold Requirement at AC130, DC90 with 2V/ns slew rate	70	75	Static offset
	T_Derate	Derating Factor	Derating factor for input slew rate greater than 2V/ns.	33	23	Static Offset.
Total Receiver (SDRAM) Uncertainty				103	98	38% of Budget consumed by SDRAM
Total Contributions for End to End Timing				159	144	Total Budget Consumed, 57%
Absolute Worst Case Margin at 1866 MBPS (Budget = 268 ps.) (Varies with Bit Rate)				109	124	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Set up and hold contributions after strobe is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).				119	114	

Table 14: Write Budget for DDR3L

Read Transaction Budget

PHY and SDRAM timing budget contributions for DDR3L Read operation at 1866Mbps						
Skew and Jitter Components		Parameter Name	Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable			Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_DV_p	Data valid Window per pin	The set up contirbution is the SDRAM output skew spec, tDQSQ. The hold element is 0.12*tCK. Based on the output hold requirement tQH=0.38*tCK.	85	129	Static Offset (SDRAM)
	T_SD_RJIT	Input Period Jitter Derating	Derating for CK/CK# input negative period jitter. Specification max of -60ps applied. This budget assumes the specification is met.	30	30	Variable (PHY and Inteconnect)
Total Transmitter (SDRAM) Uncertainty				115	159	Budget consumed by SDRAM, 51%
Receiver Contributions	T_SUH	Flip Flop Set Up and Hold	Set Up and Hold requirement at the Receive flip flop during Read operations.	19	19	Static Offset (Hard Macro)
	T_DL_ERR	Delay Line Placement Error	Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity.	10		Static Offset (Hard Macro)
	T_DL_VT_DRIFT	VT Drift of the delay line.	Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. Assume the placement can drift either way.		10	Variable (Hard Macro)
	T_DL_INL	Tap Delay variation	This assumes that there is 10ps of difference between the average tap delay and the maximum tap delay.	10	0	Static Offset (Hard Macro)
	T_PSIJ_R	Power Supply Induced Jitter	Relative jitter between DQ and DQS from +/- 2% multitone noise on the Read macro receive path from the I/O to the first flop	10	10	Variable (Hard Macro)
	T_VR_UNC	Vref Uncertainty	Set Up and Hold penalty associated with AC noise on VREF.	4	4	Variable (IO)
	T_SK_IO_In	I/O Rise/Fall Skew	Propagation delay differences between rising and falling edges within the I/O Read path. The effect is pulse width distortion that can impact both set up and hold.	2	2	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
	T_SK_ISI	I/O intersymbol interference	ISI from the reciever path seen at the core side outout of the receiver.	1	1	Variable Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Receiver (PHY) Uncertainty				56	46	Budget Consumed by PHY, 19%
Total Contributions for End to End Timing				171	205	Total Budget Consumed, 70%
Absolute Worst Case Margin at 1866 MBPS (Budget = 268 ps.) (Varies with Bit Rate)				96	63	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Set up and hold contributions after strobe is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).				76	83	

Table 15: Read Budget for DDR3L

Command/Address /Control Transaction Budget

PHY and SDRAM timing budget contributions for DDR3L Single Data Rate Command/Address operation at 1866Mbps						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT_CA	**PLL Clock Source Jitter**	**Output Jitter from PLL. The negative peak period jitter will reduce the data valid window. This value is divided between set up and hold.**	5	5	Variable (PLL)
	T_PSIJ_CA	**PowerSupply Induced Jitter**	**This is the relative jitter between the CA signals and the rising edge of the CK/CK## signals that erodes the set up and hold margins. This is characterized at thecore side input to the I/O cell during CA operations. This is a result of multitone noise of +/-2% of the core voltage. This simulation is performed under worst case PVT conditions. This result includes the PSIJ effects as well as any pulse width distortion introduced by differences of rising and falling edge delays within a single macro path.**	29	29	Mostly variable offset. Small static component from pulse width distortion of the macro paths. (Hard Macro)
	T_SK	**PHY Skew between CK/CK# and CA signals**	**This accounts for skew variations in PHY cell placement. 4% of a clock cycle total**	21	21	Static Offset (Hard Macro)
	T_PROC_SK	**Process Variation Effects**	**This value captures the timing effects of local process variation that can occur across a CA lane.**	25	25	Static Offset (IO)
	T_SK_I/O	I/O Rise/Fall Skew	**Propagation delay differences between rising and falling edges within the I/O Write path. The effect is pulse width distortion that can impact both set up and hold, depending upon the data pattern.**	5	5	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Transmitter Uncertainty				80	80	Budget consumed by PHY, 15%
Receiver Contributions	T_SU_CA, T_H_CA	CA Setup/hold	Set up and Hold Specifications at AC135 and DC90	65	110	Static Offset.
	T_SD_DER_CA, T_H_DER_CA	Set up and Hold Derating	Derating factor applied to set up and hold specification to account for slew rates greater than specification	68	45	
Total Receiver Uncertainty				133	155	Budget consumed by SDRAM, 27%.
Total Contributions.				213	235	Total Budget Consumed, 42%
Absolute Worst Case Margin at 1866 MBPS (SDR Budget = 536 ps.)				322	300	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.

Table 16: Cmd/Add/Ctrl Budget for DDR3L

tDQSS (DQS/DQS# to CK/CK#) Transaction Budget

PHY and SDRAM timing budget contributions for DDR3L Write Leveling operation at 1866Mbps.						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT (CK and DQS)	**PLL Clock Source Jitter**	**This assumes an ideal reference clock source. +/- 9ps period jitter for each, added as RSS.**	13	13	Variable (PLL)
	T_DIST_NOISE (CK and DQS)	PHY Clock Distribution Noise	Noise induced p-p period jitter on the clock tree for and DQS path. +/-29ps period jitter on each path, added as RSS.	41	41	Variable (Hard Macro)
	T_DL_ERR	**DDL Placement Error**	**Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity.**	10		Static Offset (Hard Macro)
	T_DL_VT_DRIFT	**VT Drift**	**Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. Assume the placement can drift either way.**		10	Static Offset (Hard Macro)
	T_DL_INL	**Tap Delay variation**	**This assums that there is 10ps of difference between the average tap delay and the maximum tap delay.**	10	0	Static Offset (Hard Macro)
	T_Comp_Error	**Uncompensated Delay Differences**	**Account for uncompensated VT differences that can aoccur across a large die.**	10	10	Variable (Hard Macro)
Total Transmitter Uncertainty				84	74	Budget consumed by PHY, 27%
Receiver Contributions	**T_WL_SUH**	**Write Leveling Set Up and Hold**	**Set Up and Hold requirement for CK/CK# relative to DQS/DQS#**	140	140	Static Offset
Total SDRAM Uncertainty				140	140	Budget consumed by SDRAM, 48%
Total Contributions for End to End Timing				224	214	Total Budget Consumed, 76%
Absolute Worst Case Margin at 933MHz (Budget = 289 ps., 0.27 of a Clock Cycle.)				65	75	The % of the available budget that remains will be available for inteconnect induced jitter. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Absolute Worst Case Margins with Strobe Alignment				75	65	

Table 17: tDQSS Budget for DDR3L

LPDDR3 Protocol Timing Budgets-2133Mbps

Write Transaction Budget

tDQSS spec describes DQS rising edge to CLK rising edge alignment during transactions are driven from the host to the SDRAM, which can be improved by Write Leveling training. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when generating the DQ and DQS/DQS# signals and centering the strobe. These elements are related to the PLL, the Hard Macro (DATX8) and the I/O.

PLL

- PLL output period jitter. This is jitter on the rising edges of the X4X2, 2133MHz output that generates the rising and falling edges of the 2133Mbps DQ and DQS/DQS# signals. The negative peak period jitter will reduce the data valid window.

Hard Macro

- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the DQ vs. DQS/DQS#.
  - Register delay mismatch. The simulated PSIJ result also includes Clock to Q delay differences between the rising and falling edges of the DQ and DQS/DQS#.
- Training errors – This includes initial alignment error from per bit deskew and strobe centering, tap delay variation from ideal (INL) and VT drift of strobe centering between updates.

IO

- IO rise/fall skew. This captures the rising and falling edge delay differences measured at the output of the IO structure.

The eyes are captured at the SDRAM. Traditional set up and hold timing is used for the LPDDR3 protocol. Additionally, there is a derating factor that is applied to adjust for slew rates greater than 2V/ns at 2133Mbps. These budgets assume a maximum slew rate derating per the JEDEC derating tables.

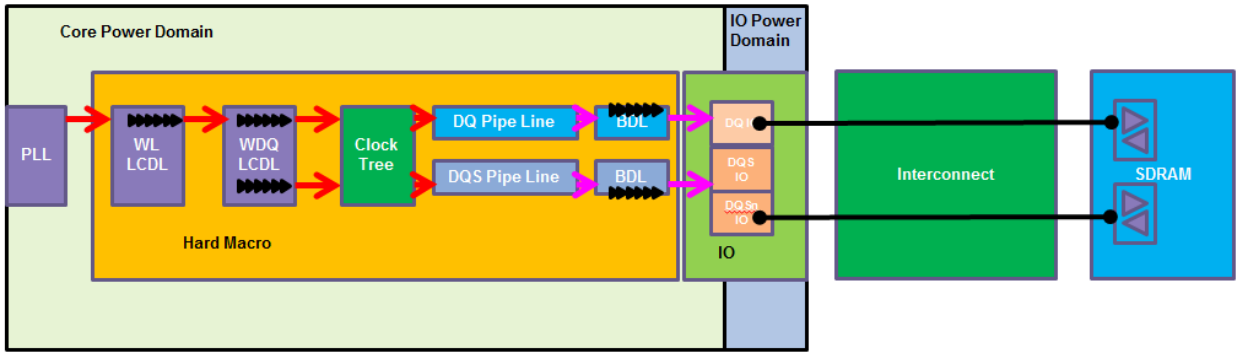

Figure 42: Illustration of PHY components for Write Budget.

PHY and SDRAM timing budget contributions for LPDDR3 Write operation at 2133Mbps						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT_DQ	PLL Clock Source Jitter	Output Perid Jitter. This is the output negative period jitter over 200 cycles. This is -7.5ps to be divided between set up and hold.	4	4	Variable Offset (PLL)
	T_PSIJ_W	PowerSupply Induced Jitter	This is the relative jitter between the DQ and DQS/DQS# signals that erodes the set up and hold margins. This is characterized at thecore side input to the I/O cell during Write operations. This is a result of multitone noise of +/-2% of the core voltage. This simulation is performed under worst case PVT conditions. This result includes the PSIJ effects as well as any pulse width distortion introduced by differences of rising and falling edge delays within a single macro path.	26	26	Mostly variable offset. Small static component from pulse width distortion of the macro paths. (Hard Macro)
	T_DL_ERR	DDL Placement Error	Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity. 10ps average delay in worst case PVT corner. 1 tap could apply to set up or hold.	10	0	Static Offset (Hard Macro)
	T_DL_VT_DRIFT	VT Drift	Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. 1 tap could apply to set up or hold.	0	10	Variable Offset (Hard Macro)
	T_DL_INL	Tap Delay variation	This assums that there is 10ps of difference between the average tap delay and the maximum tap delay.	10	0	Static Offset (Hard Macro)
	T_SK_I/O	I/O Rise/Fall Skew	Propagation delay differences between rising and falling edges within the I/O Write path. The effect is pulse width distortion that can impact both set up and hold, depending upon the data pattern.	4	4	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Transmitter (PHY) Uncertainty				54	44	21% of Budget consumed by PHY
Receiver Contributions	T_SUH	Set Up and Hold	Set Up and Hold Requirement at AC135, DC100 with 2V/ns slew rate	48	65	Static offset
	T_Derate	Derating Factor	Derating factor for input slew rate greater than 2V/ns.	34	25	Static Offset.
Total Receiver (SDRAM) Uncertainty				82	90	37% of Budget consumed by SDRAM
Total Contributions for End to End Timing				136	134	Total Budget Consumed, 58%
Absolute Worst Case Margin at 2133 MBPS (Budget = 234 ps.) (Varies with Bit Rate)				99	101	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Set up and hold contributions after strobe is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).				99	101	

Table 18: Write Budget for LPDDR3

Read Transaction Budget

Read transactions are driven from the SDRAM to the Host. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when capturing the DQ and DQS/DQS# signals and centering the strobe. These elements are related to the Hard Macro (DATX8) and the I/O.

Hard Macro

- First Flop Set Up and Hold – This is the window required to capture the DQ signals with the rising edges of the DQS and DQS#
- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the DQ vs. DQS/DQS#.
- Training errors – This includes initial alignment error from per bit deskew and strobe centering, tap delay variation from ideal (INL) and VT drift of strobe centering between updates.

IO

- IO rise/fall skew. This captures the rising and falling edge delay differences measured at the core output of the IO structure.
- IO Intersymbol Interference. This captures the impact of ISI from the receiver path on timing.
- Vref Uncertainty. Vertical differences from the ideal Vref across the byte vs. the trained Vcent level will result in small timing contributions captured here.

The output timing from the SDRAM is captured with an output skew spec, tDQSQ, and a data hold spec, tQH. (LPDDR2 uses a factor called the Hold Skew Factor, tQHS, to define the hold contribution). This is a very conservative timing methodology for the SDRAM as these are maximum values across all devices and PVT corners.

Additionally, the SDRAM output data valid window spec must be derated for any negative peak input period jitter that exceeds the specification.

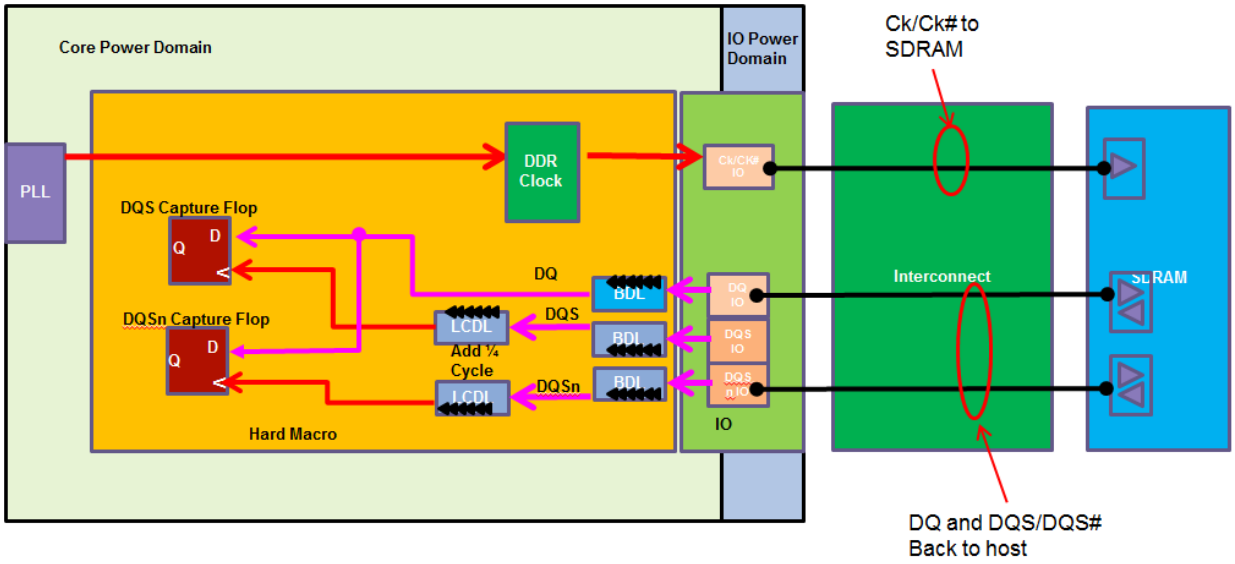

Figure 43: Illustration of PHY components for Read Budget.

PHY and SDRAM timing budget contributions for LPDDR3 Read operation at 2133Mbps						
Skew and Jitter Components		Parameter Name	Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable			Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_DV_p	Data valid Window per pin	The set up contirbution is the SDRAM output skew spec, tDQSQ. The hold element is 0.12*tCK. Based on the output hold requirement tQH=0.38*tCK.	100	113	Static Offset (SDRAM)
	T_SD_RJIT	Input Period Jitter Derating	Derating for CK/CK# input negative period jitter. When the input period jitter exceeds the negative peak spec of -50ps, the excess must be applied here.	0	0	Variable (PHY and Inteconnect)
Total Transmitter (SDRAM) Uncertainty				100	113	Budget consumed by SDRAM, 45%
Receiver Contributions	T_SUH	Flip Flop Set Up and Hold	Set Up and Hold requirement at the Receive flip flop during Read operations.	19	19	Static Offset (Hard Macro)
	T_DL_ERR	Delay Line Placement Error	Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity.	10		Static Offset (Hard Macro)
	T_DL_VT_DRIFT	VT Drift of the delay line.	Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. Assume the placement can drift either way.		10	Variable (Hard Macro)
	T_DL_INL	Tap Delay variation	This assumes that there is 10ps of difference between the average tap delay and the maximum tap delay.	10	0	Static Offset (Hard Macro)
	T_PSIJ_R	Power Supply Induced Jitter	Relative jitter between DQ and DQS from +/- 2% multitone noise on the Read macro receive path from the I/O to the first flop	10	10	Variable (Hard Macro)
	T_VR_UNC	Vref Uncertainty	Set Up and Hold penalty associated with AC noise on the VREF.	4	4	Variable (IO)
	T_SK_IO_In	I/O Rise/Fall Skew	Propagation delay differences between rising and falling edges within the I/O Read path. The effect is pulse width distortion that can impact both set up and hold.	2	2	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
	T_SK_ISI	I/O intersymbol interference	ISI from the reciever path seen at the core side outout of the receiver.	1	1	Variable Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Receiver (PHY) Uncertainty				56	46	Budget Consumed by PHY, 22%
Total Contributions for End to End Timing				156	159	Total Budget Consumed, 67%
Absolute Worst Case Margin at 2133 MBPS (Budget = 234 ps.) (Varies with Bit Rate)				78	76	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Set up and hold contributions after strobe is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).				78	76	

Table 19: Read Budget for LPDDR3

Command/Address /Control Transaction Budget

For LPDDR3, the CA is double data rate. There are also provisions to apply per bit deskew to the bus, so the budget is identical to the Write budget in structure. Cmd/Add/Ctrl transactions are driven from the host to the SDRAM. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when generating the CA and CK/CK# signals and centering the strobe. These elements are related to the PLL, the Hard Macro(PHYAC) and the I/O.

PLL

- PLL output period jitter. This is jitter on the rising edges of the 4X, 2133MHz output that generates the rising and falling edges of the 1067MHz CA and Ck/Ck# signals. The negative peak period jitter will reduce the data valid window.

Hard Macro

- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the CA vs. Ck/Ck#.
  - Register delay mismatch. The simulated PSIJ result also includes Clock to Q delay differences between the rising and falling edges of the CA and Ck/Ck#.
- Training errors – This includes initial alignment error from per bit deskew and strobe centering, tap delay variation from ideal (INL) and VT drift of strobe centering between updates.
  - Note for LPDDR2, there is no training available for the CA bus.

IO

- IO rise/fall skew. This captures the rising and falling edge delay differences measured at the output of the IO structure.
- Process Variation Effects captures the variation in output delay associated with variation of silicon process across the CA bus.

The eyes are captured at the SDRAM. CA timing uses traditional set up and hold values based on AC and DC threshold levels. Additionally, a derating effect must be applied when the input slew rate exceeds 1V/ns.

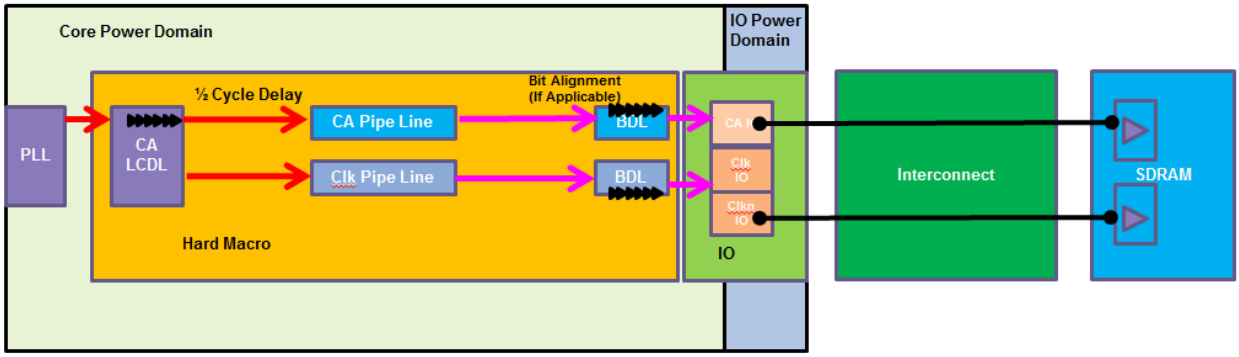

Figure 44: Illustration of PHY components for Cmd/Add/Ctrl Budget.

PHY and SDRAM timing budget contributions for LPDDR3 DDR Command/Address operation at 2133Mbps						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT_CA	PLL Clock Source Jitter	Output Perid Jitter. This is the output negative period jitter over 200 cycles. This is -7.5ps to be divided between set up and hold.	4	4	Variable Offset (PLL)
	T_PSIJ_CA	PowerSupply Induced Jitter	This is the relative jitter between the CA and CK/CK# signals that erodes the set up and hold margins. This is characterized at thecore side input to the I/O cell during Write operations. This is a result of multitone noise of +/-2% of the core voltage. This simulation is performed under worst case PVT conditions. This result includes the PSIJ effects as well as any pulse width distortion introduced by differences of rising and falling edge delays within a single macro path.	26	26	Mostly variable offset. Small static component from pulse width distortion of the macro paths. (Hard Macro)
	T_DL_ERR	DDL Placement Error	Granularity of placement of CA vs. CK based on BDL and LCDL tap granularity. 10ps average delay in worst case PVT corner. 1 tap could apply to set up or hold.	10	0	Static Offset (Hard Macro)
	T_DL_VT_DRIFT	VT Drift	Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. 1 tap could apply to set up or hold.	0	10	Variable Offset (Hard Macro)
	T_DL_INL	Tap Delay variation	This assums that there is 10ps of difference between the average tap delay and the maximum tap delay.	10	0	Static Offset (Hard Macro)
	T_SK_I/O	I/O Rise/Fall Skew	Propagation delay differences between rising and falling edges within the I/O Write path. The effect is pulse width distortion that can impact both set up and hold, depending upon the data pattern.	4	4	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Transmitter (PHY) Uncertainty				54	44	21% of Budget consumed by PHY
Receiver Contributions	T_SUH	Set Up and Hold	Set Up and Hold Requirement at AC135, DC100 with 2V/ns slew rate	48	65	Static offset
	T_Derate	Derating Factor	Derating factor for input slew rate greater than 2V/ns.	34	25	Static Offset.
Total Receiver (SDRAM) Uncertainty				82	90	37% of Budget consumed by SDRAM
Total Contributions for End to End Timing				136	134	Total Budget Consumed, 58%
Absolute Worst Case Margin at 2133 MBPS (Budget = 234 ps.) (Varies with Bit Rate)				99	101	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Set up and hold contributions after clock is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).				99	101	

Table 20: Cmd/Add/Ctrl Budget for LPDDR3

tDQSS (DQS/DQS# to CK/CK#) Transaction Budget

tDQSS transactions are driven from the host to the SDRAM. This budget includes all of the PHY timing components as well as the SDRAM specs that affect timing. There are separate PHY blocks in this transaction. The clock is driven from the AC block while each of the DQS pairs are driven from separate DATX8 blocks. When these are summed, the margin that remains is what is available for interconnect uncertainty.

The PHY timing components cover all of the elements that can erode the margins when generating the CK/CK# and DQS/DQS# and then aligning them with the write leveling functionality. These elements are related to the PLL and the Hard Macro.

PLL

- PLL output period jitter. This is jitter on the rising edges of the 2X, 2667MHz output. Since there are two PLLs we will add the jitter from both of them in a square root of the sum of the squares manner

Hard Macro

- Power Supply Induced Jitter – This includes the jitter impact of +/-2% of VDD multitone noise on the placement of the DQS/DQS# relative to the CK/CK#. There is period jitter on both of these, so they are added in an RSS manner as well.
- Training errors – This includes initial alignment error from write leveling, tap delay variation from ideal (INL) and VT drift of strobe alignment between updates.
    - Write Leveling is not available for LPDDR2.

tDQSS timing requires that the DQS/DQS# rising edges arrive within 0.25 of a clock cycle of the CK/CK# rising edges. To aid this, Write Leveling is used. In order for this to work, the SDRAM will consume +/- 135ps the available budget to assure alignment.

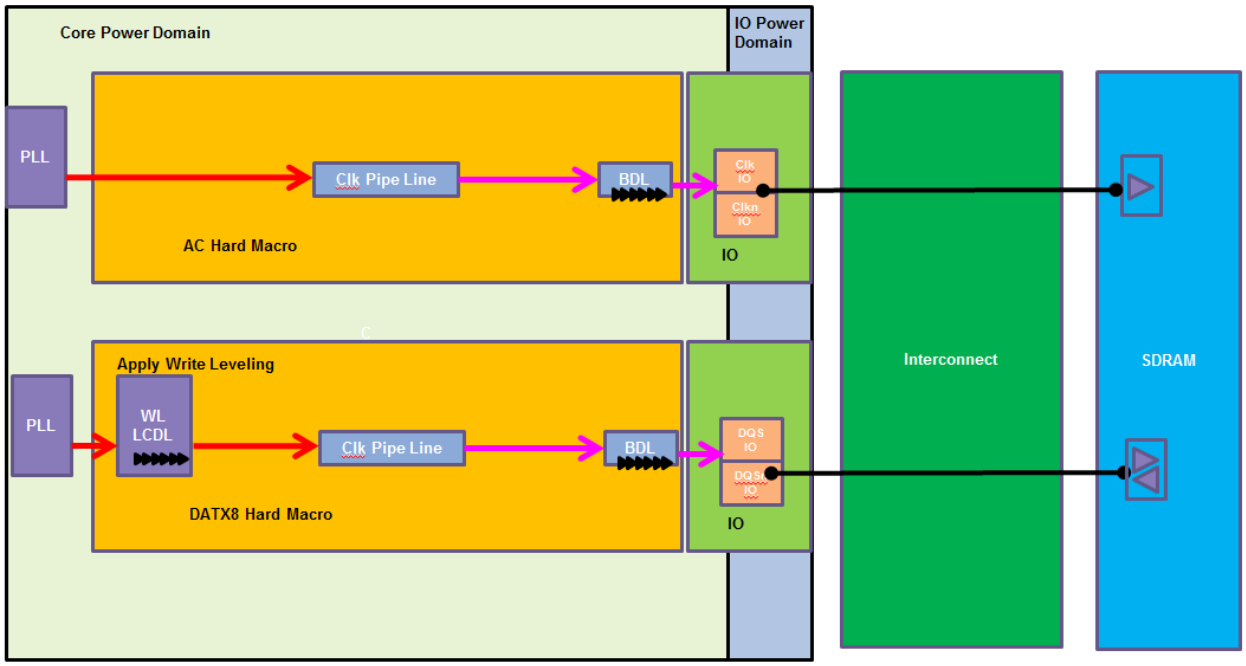

Figure 45: Illustration of PHY components for tDQSS Budget.

PHY and SDRAM timing budget contributions for LPDDR3 Write Leveling operation at 2133Mbps.						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT DQS	**PLL Clock Source Jitter**	**This assumes an ideal reference clock source. +/- 7.5ps period jitter.**	8	8	Variable (PLL)
	T_DIST_NOISE (DQS)	PHY Clock Distribution Noise	Noise induced p-p period jitter on the clock tree for and DQS path. +/-29ps period jitter.	29	29	Variable (Hard Macro)
	T_DL_ERR	**DDL Placement Error**	**Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity.**	10		Static Offset (Hard Macro)
	T_DL_VT_DRIFT	**VT Drift**	**Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. Assume the placement can drift either way.**		10	Static Offset (Hard Macro)
	T_DL_INL	**Tap Delay variation**	**This assums that there is 10ps of difference between the average tap delay and the maximum tap delay.**	10	0	Static Offset (Hard Macro)
	T_Comp_Error	**Uncompensated Delay Differences**	**Account for uncompensated VT differences that can aoccur across a large die.**	10	10	Variable (Hard Macro)
Total Transmitter Uncertainty				67	57	Budget consumed by PHY, 26%
Receiver Contributions	**T_WL_SUH**	**Write Leveling Set Up and Hold**	**Set Up and Hold requirement for CK/CK# relative to DQS/DQS#**	135	135	Static Offset
Total Interconnect Uncertainty				135	135	Budget consumed by SDRAM, 57%
Total Contributions for End to End Timing				202	192	Total Budget Consumed, 83%
Absolute Worst Case Margin at 1067MHz (Budget = 234 ps., 0.25 of a Clock Cycle.)				33	43	The % of the available budget that remains will be available for inteconnect induced jitter. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Absolute Worst Case Margins with Strobe Alignment				43	33	

Table 21: tDQSS Budget for DDR3

LPDDR2 Protocol Timing Budgets-1067Mbps

LPDDR2 protocol is similar to LPDDR3 with two differences that impact the budgets. While Command/Address is double data rate, like LPDDR3, there is no provision for training of bit skew, so the PHY skews and OCV effects must be accounted for. Secondly, the tDQSS budget does not have a provision for Write Leveling, so the routing skews must be managed to keep the skew between CK/CK# within ¼ of a clock cycle of the DQS/DQS# signals. The budget tables for LPDDR2 are included below.

Write Transaction Budget

PHY and SDRAM timing budget contributions for LPDDR2 Write operation at 1067Mbps						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT_DQ	PLL Clock Source Jitter	Output Perid Jitter. This is the output negative period jitter over 200 cycles. This is -20ps to be divided between set up and hold.	10	10	Variable Offset (PLL)
	T_PSIJ_W	PowerSupply Induced Jitter	This is the relative jitter between the DQ and DQS/DQS# signals that erodes the set up and hold margins. This is characterized at thecore side input to the I/O cell during Write operations. This is a result of multitone noise of +/-2% of the core voltage. This simulation is performed under worst case PVT conditions. This result includes the PSIJ effects as well as any pulse width distortion introduced by differences of rising and falling edge delays within a single macro path.	26	26	Mostly variable offset. Small static component from pulse width distortion of the macro paths. (Hard Macro)
	T_DL_ERR	DDL Placement Error	Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity. 10ps average delay in worst case PVT corner. 1 tap could apply to set up or hold.	10	0	Static Offset (Hard Macro)
	T_DL_VT_DRIFT	VT Drift	Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. 1 tap could apply to set up or hold.	0	10	Variable Offset (Hard Macro)
	T_DL_INL	Tap Delay variation	This assums that there is 10ps of difference between the average tap delay and the maximum tap delay.	10	0	Static Offset (Hard Macro)
	T_SK_I/O	I/O Rise/Fall Skew	Propagation delay differences between rising and falling edges within the I/O Write path. The effect is pulse width distortion that can impact both set up and hold, depending upon the data pattern.	4	4	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Transmitter (PHY) Uncertainty				60	50	23% of Budget consumed by PHY
Receiver Contributions	T_SUH	Set Up and Hold	Set Up and Hold Requirement at AC220, DC130 with 1V/ns slew rate	-10	80	Static offset
	T_Derate	Derating Factor	Derating factor for input slew rate greater than 1V/ns.	110	65	Static Offset.
Total Receiver (SDRAM) Uncertainty				100	145	26% of Budget consumed by SDRAM
Total Contributions for End to End Timing				160	195	Total Budget Consumed, 49%
Absolute Worst Case Margin at 1067 MBPS (Budget = 469 ps.) (Varies with Bit Rate)				309	274	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Set up and hold contributions after strobe is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).				289	294	

Table 22: Write Budget for LPDDR2

Read Transaction Budget

PHY and SDRAM timing budget contributions for LPDDR2 Read operation at 1067Mbps						
Skew and Jitter Components		Parameter Name	Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable			Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_DV_p	Data valid Window per pin	The set up contirbution is the SDRAM output skew spec, tDQSQ. The hold element is tQHS, hold skew factor.	200	230	Static Offset (SDRAM)
	T_SD_RJIT	Input Period Jitter Derating	Derating for CK/CK# input negative period jitter. When the input period jitter exceeds the negative peak spec of -90ps, the excess must be applied here.	0	0	Variable (PHY and Inteconnect)
Total Transmitter (SDRAM) Uncertainty				200	230	Budget consumed by SDRAM, 46%
Receiver Contributions	T_SUH	Flip Flop Set Up and Hold	Set Up and Hold requirement at the Receive flip flop during Read operations.	19	19	Static Offset (Hard Macro)
	T_DL_ERR	Delay Line Placement Error	Granularity of placement of DQ vs. DQS based on BDL and LCDL tap granularity.	10		Static Offset (Hard Macro)
	T_DL_VT_DRIFT	VT Drift of the delay line.	Variation of Tap placement with Voltage and Temperature. 2 Taps on Master yields 1 tap drift on slave. Assume the placement can drift either way.		10	Variable (Hard Macro)
	T_DL_INL	Tap Delay variation	This assumes that there is 10ps of difference between the average tap delay and the maximum tap delay.	10	0	Static Offset (Hard Macro)
	T_PSIJ_R	Power Supply Induced Jitter	Relative jitter between DQ and DQS from +/- 2% multitone noise on the Read macro receive path from the I/O to the first flop	10	10	Variable (Hard Macro)
	T_VR_UNC	Vref Uncertainty	Set Up and Hold penalty associated with AC Noise on VREF	4	4	Variable (IO)
	T_SK_IO_In	I/O Rise/Fall Skew	Propagation delay differences between rising and falling edges within the I/O Read path. The effect is pulse width distortion that can impact both set up and hold.	2	2	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
	T_SK_ISI	I/O intersymbol interference	ISI from the reciever path seen at the core side outout of the receiver.	1	1	Variable Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Receiver (PHY) Uncertainty				56	46	Budget Consumed by PHY, 22%
Total Contributions for End to End Timing				256	276	Total Budget Consumed, 73%
Absolute Worst Case Margin at 1067 MBPS (Budget = 469 ps.) (Varies with Bit Rate)				213	193	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.
Set up and hold contributions after strobe is centered within the eye. Centering will be within the accuracy of one tap (T_DL_ERR).				203	203	

Table 23: Read Budget for LPDDR2

Command/Address /Control Transaction Budget

PHY and SDRAM timing budget contributions for LPDDR2 Double Data Rate Command/Address operation at 1067Mbps						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT_CA	**PLL Clock Source Jitter**	**Output Jitter from PLL. The negative peak period jitter will reduce the data valid window. This value is divided between set up and hold.**	10	10	Variable (PLL)
	T_PSIJ_CA	**PowerSupply Induced Jitter**	**This is the relative jitter between the CA signals and the rising edge of the CK/CK## signals that erodes the set up and hold margins. This is characterized at thecore side input to the I/O cell during CA operations. This is a result of multitone noise of +/-2% of the core voltage. This simulation is performed under worst case PVT conditions. This result includes the PSIJ effects as well as any pulse width distortion introduced by differences of rising and falling edge delays within a single macro path.**	29	29	Mostly variable offset. Small static component from pulse width distortion of the macro paths. (Hard Macro)
	T_SK	**PHY Skew between CK/CK# and CA signals**	**This accounts for skew variations in PHY cell placement. 4% of a clock cycle total**	37	37	Static Offset (Hard Macro)
	T_PROC_SK	**Process Variation Effects**	**This value captures the timing effects of local process variation that can occur across a CA lane.**	25	25	Static Offset (IO)
	T_SK_I/O	I/O Rise/Fall Skew	**Propagation delay differences between rising and falling edges within the I/O Write path. The effect is pulse width distortion that can impact both set up and hold, depending upon the data pattern.**	4	4	Static Offset (IO) (This value will be contained within the results of interconnect simulations. Be careful not to double count this effect.)
Total Transmitter Uncertainty				96	96	Budget consumed by PHY, 20%
Receiver Contributions	T_SU_CA, T_H_CA	DDR CA Setup/hold	Set up and Hold Specifications at AC220 and DC130	0	90	Static Offset.
	T_SD_DER_CA, T_H_DER_CA	Set up and Hold Derating	Derating factor applied to set up and hold specification to account for slew rates greater than specification	110	65	
Total Receiver Uncertainty				110	155	Budget consumed by SDRAM, 28%.
Total Contributions.				206	251	Total Budget Consumed, 48%
Absolute Worst Case Margin at 1067 MBPS (SDR Budget = 469 ps.)				263	218	The % of the unit interval that remains will be available for inteconnect uncertainty. In order to determine the interconnect uncertainty the user should simulate the subject interface for Crosstalk, Simultaneous Switching effects, intersymbol interference, reflections, etc. This analysis should be done over a range of PVT conditions from Worst Case to Best Case.

Table 24: Cmd/Add/Ctrl Budget for LPDDR2

tDQSS (DQS/DQS# to CK/CK#) Transaction Budget

PHY and SDRAM timing budget contributions for LPDDR2 tDQSS budget at 1067Mbps.						
Skew and Jitter Components			Description	Worst Case Uncertainty Contributions		Timing nature of uncertainty
	Variable	Parameter Name		Set Up Contribution	Hold Contribution	
Transmitter Contributions	T_OJITT (DQS)	**PLL Clock Source Jitter**	**This assumes an ideal reference clock source. +/- 20ps period jitter.**	20	20	Variable (PLL)
	T_DIST_NOISE (CK and DQS)	PHY Clock Distribution Noise	Noise induced p-p period jitter on the clock tree for and DQS path. +/-29ps period jitter.	29	29	Variable (Hard Macro)
	T_SK	**PHY Skew between CK/CK# and DQS/DQS# signals**	**This accounts for skew variations in PHY cell placement. 8% of a clock cycle total**	75	75	Static Offset (Hard Macro)
	T_PROC_SK	**Process Variation Effects**	**This value captures the timing effects of local process variation that can occur across a CA lane.**	25	25	Static Offset (IO)
Total Transmitter Uncertainty				149	149	Budget consumed by PHY, 32%
Absolute Worst Case Margin at 533MHz (Budget = 469 ps., 0.25 of a Clock Cycle.)				226	320	This is the margin that remains for routing skews to meet the tDQSS budget for LPDDR2.

Table 25: tDQSS Budget for LPDDR2