SYNOPSYS®

Designware Cores DDR4 multiPHY Implementation Guide

DWC DDR4 multiPHY

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Revision History

Version	Date	Note
1.70	February 2017	Updated: ESD Protection Scheme
1.60	November 2015	Updated: PHY-Specific Clocks Checklist Information ESD Discharge Resistance
1.50	October 2015	Updated: PLL Power Routing General Routing Guidelines Table 17: Skew Summary o bypass_clks1, bypass_clks2 o zctrl_strict
1.40	April 2015	Updated: DQS/DQS_b Connections Skew Requirement Summary Impedance (ZQ) Calibration Table 17: Skew Summary o dx_to_io o RET/RET_B pin o Bypass_clock1 zctrl_strict Group Start and End Points zctrl_relaxed Group Start and End Points dx_to_io Group Start and End Points
1.30	January 15, 2015	Updated: Figure 1: DDR4 multiPHY Overview Core Power Requirements Grounding Introduction o Caution: The information in this document applies to the D4M and D4MV I/O libraries. It does not apply to the D4MU I/O library.
1.20	December 3, 2014	Updated: Retention Latch Enable Input Pin Requirement o Note: A maximum skew of 300ps is allowed between Data Retention Input pins (RET and RET_B) Timing Constraints Dont_touch and Special NetsDont_touch and Special Nets o pll_ato_at is considered a high voltage net. Refer to the technology guidelines for width and spacing requirements Checklist Information o Note: The path delays for these signals between PHY and SSTL should be measured and verified. Checklist Information o pll_analog_test_out (ATO) spacing requirement is technology rule dependent since it is considered a high-voltage signal
1.10	September 25, 2014	Added: Appendix – Implementation Checklist

1.00	March 25, 2014	Updated: DQS/DQS_b Connections Added: Spacing of Standard Cells from SSTL cells
0.5	October 9, 2013	Updated D3M to DXX Removed section 6.2 as it is the same as Synopsys Milkyway Library Setup Removed duplicate lines from Synopsys Milkyway Library Setup Updated the library name to generic dxx and <pvt> in section Synopsys Milkyway Library Setup Updated the Introduction page Dont_touch and Special Nets
0.4	August 2013	Updated: Planning Added: Floorplanning Considerations for the PUB Removed: LPDDR3 Interface Example DDR3 Interface Example
0.3	July 2013	Preliminary release: Subject to change
0.2	May 31, 2013	Preliminary release: Subject to change
0.1	January 25, 2013	Preliminary release: Subject to change

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1 Introduction

This document provides the designer with detailed information on the electrical, timing and physical implementation aspects of Synopsys DDR4 multiPHY solution. Specifically it includes guidelines for system planning, clocking, timing, synthesis, and physical implementation.

The complete Synopsys DDR4PHY solution consists of both hard and soft IP components. There are few physical implementation requirements for the soft IP component. Therefore the focus in the physical Implementation chapter is on the hard IP components. To aid with the soft IP component there are separate chapters for timing and synthesis.. Timing guidelines for Synopsys memory controllers are described in separate documents

It is important to have a general understanding of the various components before reading this document. Reviewing the various component datasheets before reading this document is encouraged. There may be implementation notes in the component datasheets which are not covered in this document.

A typical SDRM system normally contains:

1 Address Command Lanes

- 1 DDRPHYAC (AC) PHY (hard IP),
- respective SSTL IO (hard IP)
- 1 PLL (hard IP)

1 - 9 Data Byte lanes

- 1 DDRPHYDATX8 (DX) PHY Macro (hard IP)
- Repective SSTL IOs (hard IP)
- either shared or individual PLL per lane (hard IP)

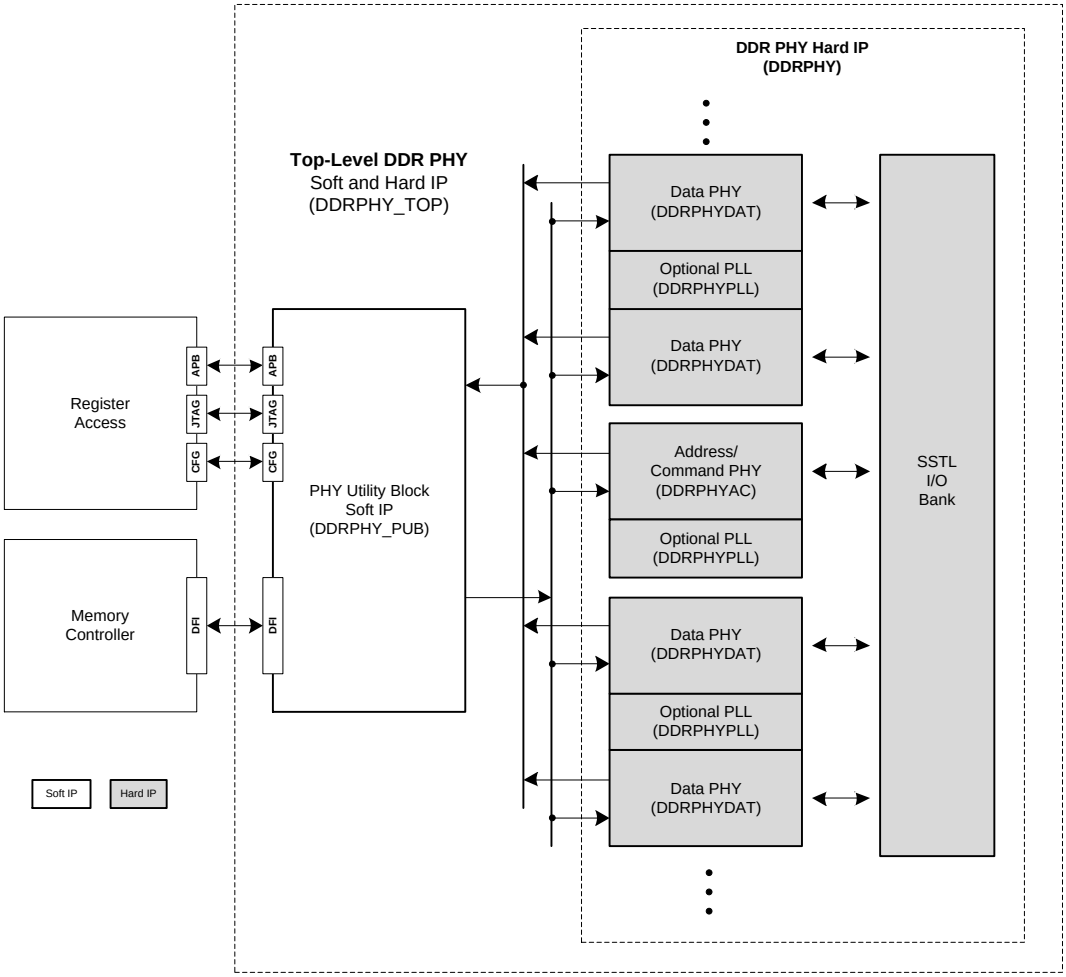
1 PHY Utility Block (PUB) (Soft IP)

1 Memory Controller (Soft IP)

Figure 1 shows how the PHY is used in a typical SDRAM system. The full PHY IP solution consists of five components. Four of these are hard IP and include the SSTL I/O library, a PHY macro for the data lane (DDR4PHYDATX8, hereafter known as DATX8), PHY macro for the address/command lane (DDR4PHYAC, hereafter known as AC), and the optional PLL.. System operating at 1066 Mbps or below may opt to forego the PLLs. The fith component, a soft macro (DDR4PUB, hereafter known as PUB) provides configuration, control and other utility functions for all the four PHY hard macros.

Caution: The information in this document applies to the D4M and D4MV I/O libraries. It does not apply to the D4MU I/O library.

Figure 1: DDR4 multiPHY Overview



Any successful design implementation begins with proper planning. This document will begin by presenting planning methods to the reader, using an example for reference. Proper planning simplifies the actual design. Please note that the example provided in this document is for illustration purposes only. The designer should not rely on the information provided with this example. The component datasheets may contain more recent data than that presented in this document. The designer should always use the latest information available in the component data files and datasheets.

The following chapters review the design requirements for an example 72 bit DDR4 design interface and aspects of the designtht need to be considered throughout the design process from design planning to chip finishing.

2 Planning

2.1 General Design Requirements

The main component of the planning phase is determining the size of the DDR interface. This includes determining, among other things, the width of the data interface, the number of address bits supported, number of ranks used, and power/ground signals. For the timing and clocking planning, the focus is mainly on the maximum frequency used, the timing mode of the PHY (rise-to-rise or rise-to-fall), and the timing margins desired. For the physical implementation, the planning process is highly focused on the pad frame. Once the pad frame is realized, all other elements are easily added. The pad frame is driven by a number of items, including the exact interface configuration, the type of package, the number of power pins required, and so on. Table 1 provides a summary of the information required to complete the planning process.

Table 1:General Design Requirements

Item	Answer	Notes
# of address pins		Affects number of A[x] pins required
# of Ranks		Affects whether ODT pins are required in LPDDR3 systems. Some POP LPDDR3 SDRAM use ODT pins, some do not use ODT or have them internally tied to VSSQ in SDRAM, Discrete LPDDR3 SDRAM have ODT pins. (No LPDDR2 devices have ODT pins).”
CS_b pin (single rank systems only)		For single-rank systems, the CS_b output is optional as the CS_b input of the SDRAMs can be tied low on the PCB
Parity and Alert_n and functions required		May require Parity and Alert_n pins on interface in DDR4 mode
# of CK/CK_b output pairs		One pair for most systems Two pair to two rank systems Unbuffered DDR2 DIMMs may require three pairs
# of data pins		For instance, 32-bit interface
PLL sharing between data byte lanes		Affects number of PVAA_PLL required for data byte lanes
# of isolated bus segments		Affects numbers of PEND, PVREF, PRETPOCX or PRETPOCC cells required.
# of SSTL PVT groups		Typically one PVT compensation group is adequate, but in the case where the interface is large and not closely grouped the user may wish to break the total interface into 2 or more dedicated PVT groups. All groups can be fed from a single external resistor compensation cell. Normally, 32-bit systems use a single common PVT group. However, it is worth considering a separate PVT group for the Command Lane so that the SI environment of the Command Lane and Byte Lanes can be separately tuned. For example, if system power dissipation is a critical factor and the Command Lane is being operated without termination it may improve SI to operate the Command Lane and Byte Lanes with different drive strength values.
Reference clock source and type		Input needed if off-chip source used Single-ended or differential Signal type: SSTL, HSTL, PECL, and so on Note: most systems use an on-chip clock source.
Pop or Discrete SDRAM		Affects whether ODT pins are required in LPDDR3 systems. POP LPDDR3 SDRAM do not use ODT or have them internally tied to VSSQ in SDRAM, Discrete LPDDR3 SDRAM have ODT pins. (No LPDDR2 devices have ODT pins.)
Reference clock and SDRAM clock frequency requirements		For instance, 166 MHz to 53XXHz reference clock for a 33XXHz to 1066MHz SDRAM clock
Package type		For instance flip chip or wire bond BGA

Item	Answer	Notes
Pad pitch requirement		Recommend using minimum
Bond pad configuration (if wire bond)		Minimum pitch requires 2-tier staggered
Core power requirements (full chip)		Core power pads normally exist in this area of the pad frame What is the chip's power consumption What are the IR drop limits
Test pin requirements		Dedicated test pin for PLL, possibly also for PHY
External Vref generation for SDRAM		Dedicated pins to generate VREF signal to SDRAMs
Per data byte local Internal VREF cells required		In DDR4 mode one PVREF cell per data byte may be required on the DDR interface
Per Rank local internal VREF support		In DDR4 mode an additional PVREF_DAC cell may be required per data byte to support multi-rank VREF switching on the DDR interface
Interface to support both DDR3 and DDR4 modes		Specific pins functions to be muxed between DDR3 and DDR4 modes on the same interface
CKE retention mode required (SDRAM self refresh)		PCKE and PRETOCC or PRETPOCX cells required for CKE retention mode (SDRAM self refresh)
CKE Retention mode with VDDQ IO supply power down		Extra PFILL5_ISO (to cut VDDQ), PVREF, PVDDQ, PVSSQZB_ZQ cells required to support CKE retention with VDDQ IO supply power down. Package VDDQ supply need to be isolated as well to support CKE retention island with VDDQ IO power down
CKE retention with core VDD power down		Require PRETPOCX, or, PRETPOCC cell with un-powered down VDD core supplied core latch control logic if VDD core is to be powered down in CKE retention mode

2.2 DDR4 Interface Examples

An example design, with the following parameters, will be used for illustration purposes: a 72 bit DDR4 interface in a flip chip example in a single row 25um IO pitch. Designers should replace these with their own design parameters:

Table 2:Flip Chip Examples

Flip Chip Example
72 bit data interface (8 byte lanes with 1 ECC byte)
Sharing one PLL for two data byte lanes (PLL sharing)
18 bit address A[17:0], 2 BG, 2 BA, 1 Activate
Parity and Alert_n pins required
2 rank, two CS_b, two ODT, 2 CLKP/N, 2 CKE output pins
No VREF generators for external SDRAM (VREFca for SDRAM provided on board)
Per data byte and per rank local VREF support required
CKE retention with VDDQ power down mode required
1 SDRAM_RESET_n pin
On-chip reference clock
2 SSTL/PVT groups – one for data, one for Address/Command
1066MHz/213XXbps SDRAM operating frequency
DDR4 UDIMM SDRAM
Flip chip (FC) package
25um pad pitch

Based on our example design parameters, we start with the following information:

Table 3:Design Parameters

Flip Chip Example Command Lane - 36 signal slots: 18 A, 2 CS_b, 2 CKE, 2 ODT, 2 CK/CK_b, 2 BG, 2 BA, 1 ACT, 1 Parity, 1 Alert_n, 1 SDRAM_RESET_n - 1 SSTL PVT compensation PZQ slot - 37 x 25um = 925um total length, not including core and IO power supply slots Byte Lane - 11 signal slots: 8 DQ, DM, DQS/DQS_b - 1 DQSG Read DQS Gate located between the DQS/DQS_B cells - 12 x 25um = 300um total length, not including core and IO power supply slots 1 Command Lane + 9 Byte Lanes - 3625um total length, not including core and IO power supply slots

Note: Use of PDIFF I/O cells. The PDIFF cell is intended for use in pairs to input differential signals. The recommended uses of the PDIFF cell are:-

1. To receive an external differential clock in the event the source clock for the memory interface and controller is an external differential clock instead of the more traditional on-die source.
2. For DQS/DQSb signals
3. PDDRIO I/O cells should be used for most DDR output and I/O signals including CK/CKb

2.2.1 I/O Signal to Power Ratio (VDDQ/VSSQ)

The I/O signal-to-power ratio is the number of signal slots a single VDDQ/VSSQ pair can support. Numerous effects must be taken into account in this analysis, signal integrity including SSO (Simultaneously Switching Output) noise and IO supply decoupling capacitance, IR drop, electro-migration (EM) limits, and ESD performance. The final signal-to-power ratio is dependent on the maximum operating frequency, the package type and expected package parasitics (RLC), and the anticipated external memory subsystem to be driven.

When possible, the best case recommendation is a 2:1 signal-to-power ratio (such as, 2 signal slots for each VDDQ/VSSQ power pair). This ratio provides good electrical and timing performance in the majority of package types and external memory subsystems. It is beneficial to use this ratio when possible. For staggered bond pad configurations, many package assembly houses mandate power connections are on outer bond pads which permits down-bonding to rings within the package substrate. As shown in **Error! Reference source not found.**, a 2:1 ratio can easily meet this requirement.

No matter the operating frequency or if the user is planning a flip-chip or wire-bond package, the user must treat the signal:power ratio and the package design as a critical aspects of the overall system and perform the proper analysis to ensure their planned design is sufficient for the intended application. To aid in these decisions, Synopsys provides an application guide for DDR SDRAM systems, "Guidelines for Implementing Signaling Environments for DDRn Interfaces: PCB, Package,Power, and Timing Budgets ". This guide contains information on signal:power ratio selection and package design. The user is required to reference the noted application guide as part of their development activities.

Returning to the example design, a 2:1 signal to power ratio is specified for the Byte Lanes and 3:1 signal to power ratio for the Command Lane. The reason why the Command Lane has the higher signal-to-power ratio then the Bytes Lanes is the Command lane is single data rate signaling and the Byte Lanes are dual data rate.

Note: There are two different VDDQ IO power cells in the DDR4 multi-phy library. PVDDQ_CAP and PVDDQ_ESD. PVDDQ_ESD cells have VDDQ-VSS diode clamps for ESD protection whereas PVDDQ_CAP have no ESD clamps but extra VDDQ-VSSQ decoupling capacitance. In section 2.2.9 VDDQ ESD Calculation, a method is described for the calculation of adequate numbers of VDDQ_ESD cells in the IO pad frame since it requires that all the other cells of the

pad frame need to be defined before such a calculation can be performed. The total number of PVDDQ_ESD and PVDDQ_CAP cells required for the interface are indicated in this section

Table 4:Flip Chip Example

Flip Chip Example

Command Lane

- 36 signal slots + 1 PVT compensation slot = 12 VDDQ/VSSQ pairs (24 total supply slots) with a 3:1:1 ratio (Signal:Power:Ground)
- 925um + (24 * 25um) = 1525um total length, not including core power supply slots

Byte Lane

- 11 signal slots = 5 VDDQ/VSSQ pairs (10 total supply slots) with a 2:1:1 ratio (Signal:Power:Ground)
- 300um + (10 * 25um) = 550um total length, not including core power supply slots

1 Command Lane + 9 Byte Lanes

- = 1525 + 9 * 550um = 6475, not including core power supply slots

2.2.2 VAA_PLL Power Requirements

VAA_PLL power cells are required for supplying current to PLLs in core at a voltage of 2.5V to 1.5V referenced to VSS. In addition, VAA_PLL is required for supplying current to the IO RX circuits at 1.8V referenced to VSSQ.

Since both Command lane and Data Byte lanes require VAA_PLL cells for both PLL supply and IO RX supply it is best to perform a VAA_PLL cell EM limit and VAA_PLL power bus IR drop calculation to determine the required number of VAA_PLL cells.

The Data Bytes lanes can have either one PLL each or one PLL shared between two Byte lanes. So a Data Byte lane where the PLL is not shared with another byte lane the VAA_PLL supply cell(s) needs to supply current to one PLL and the signal IO RX for one byte lane. A design with one PLL per two Data Byte lanes (shared PLL) VAA_PLL cells need to supply current to one PLL and the signal IO RX for two byte lanes. To implement a design for best VAA_PLL power bus IR drop for signal IO receiver's supply it is recommended to locate VAA_PLL cells in the middle of the byte lanes. For best PLL VAA_PLL power bus IR drop results a VAA_PLL cell should be located closest to the PLL which is typically located to one edge of the byte lane. In the case of shared PLL the PLL is located between the two byte lanes so a VAA_PLL cell would be ideally located there. If it is determined by EM limit and IR drop calculations that more than one VAA_PLL cell per byte lane is required then both signal IO RX VAA_PLL cell and PLL supply VAA_PLL recommended cell locations can be satisfied. If a case arises where only one VAA_PLL cell would be required for both signal IO RX and PLL supply for a byte lane it would be best to locate the VAA_PLL cell in the middle of the byte lane.

The Command Lane VAA_PLL cells need to supply one PLL plus the signal IO RX (although this is only used in loop back mode). Usually more than one VAA_PLL cell will be required so they should be evenly distributed throughout the Command lane IOs.

VAA_PLL cells for the signal IO RX use VSSQ for the ground return. Since large numbers of VSSQ cells are provided in the interface to meet VDDQ/VSSQ cell requirements, no new additional VSSQ cells are usually required for VAA_PLL. VAA_PLL cells used for PLL supply use VSS for the ground return. It would be best to place any VAA_PLL cell that is closest to the PLL next to VSS cells used for VDD supply return to ensure lowest inductance supply. Depending on EM limit calculations for VDD/VSS cells it may be necessary to add a local VSS cell to supply the additional current required through the VAA_PLL cell for the PLL.

Calculations for our examples are shown below with VAA_PLL = 1.8V nominal.

Note: Example calculations are shown with values that may or may not be the exact power values, EM limits, interconnect resistance for the IO cells in a particular library. Refer to the the current data books for the metal stackup and cell library that are used in the design for the most accurate data.

Table 5:Flip Chip Example

Flip Chip Example
4 Byte lane pairs share PLLs, one extra byte lane has it own PLL or shared with AC
AC, DATX8 IO RX powered by VAA_PLL/VSSQ
1066MHz/2133bps SDRAM operating rate, 100% switching activity factor (worst case)
Flip chip packaging
Assume SSTL loop-back mode is active

Table 6:Example VAA_PLL Power Requirements – Flip Chip IC

Lane	Calculation	Supply Requirements
Each Byte Lane	**Determining maximum VAA_PLL currents from PLL and IOs for Byte lane** **PLL is shared between two byte lanes** PLL Current (referenced to VSS) from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 = Max IVDD_PLL parameter from Power Dissipation table in DDR4 section o =13.5mA IO current (per IO) assumes RX are powered up, IO in receive mode with ODT enabled and TX output driver disabled (gives maximum current) SSTL DC current: = (PRCV_VAA_PLL from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 DC transmit Mode power Dissipation table in DDR4 section) / Max VAA_PLL o =2mW/1.89V = 1.06mA SSTL AC current: = (PRCVAA_PLL_AC from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 DDR4 mode (PDR=0 AC power table)uW/MHz*Switching frequency/Max VAA_PLL o =0.04*uW/MHz*1066MHz/1.89V = 0.0226mA o Current per IO = SSTL DC current + SSTL AC current = 1.06mA+0.0226mA = 1.08mA Total byte Lane IO current = 11 SSTL IO current = 11IOs * (SSTL DC current + SSTL AC current) o 11*(1.06mA+0.0226mA) = 11.91mA Total current for 2 Byte lanes = PLL current + 2*Byte Lane IO current (let us call this quantity TC2B) o Total 2 Byte Lanes = TC2B = 13.5mA + 2*11.91mA = 37.32mA **Vertical metal EM limit** VAA_PLL SSTL cell EM limits = IEM_VAA for Pad to MVAA_PLL vertical metal current limit and IEM_MVAA_PLL for MVAA_PLL horizontal bus metal current limit from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 EM Compliance table The number of PVAA_PLL cells needed based on vertical metal limit = TC2B/IEM_VAA o So in this case = 37.32mA/295mA = 0.126 < 1 so one cell would be sufficient **Horizontal metal EM limit** If we assume n VAA_PLL cells and place them equally distributed along the length of the IOs they are supplying current to - each IO segment physically divided by the VAA_PLLs will be carrying 1/(2n) of the total current assuming the current is equally distributed to each segment. Therefore the current on each segment must be less than the horizontal metal EM limit or TC2B/(2n) < IEM_MVAA_PLL Solving for the number of cells needed we have n > TC2B/(2*IEMVAA_PLL) o So in our case n > 37.32mA/(2*40mA) = 0.4665 or 1 cell should be sufficient. **VAA_PLL IR Drop** Assume 2.5% * 1.8V = 45mV is acceptable on die IR drop limit. Assume bump to VAA_PLL cell resistance = 0.5 ohm (replace this with the bump to IO pad resistance from your layout) VAA_PLL vertical metal resistance = R_VAA from the Power Grid Support table in the DesignWare Cores DDR4 multiPHY databook for	Add 1 VAA_PLL cell per byte lane

Lane	Calculation	Supply Requirements
	TSMC28HPM18 ○ 0.26 ohms Horizontal metal resistance = R_MVAA_PLL from the Power Grid Support table in the DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 = 0.19 ohms in each cell. IO pitch is 25um Assuming a Sig:pwr:ground cell ratio in the byte lane to be 2:1:1 for 11 signal cells for IR drop purposes. Since the signal:power:ground cell ratio is 2:1:1 with 11 signal cells we have 5 power and 5 ground for a total of 19 cells. Each signal cell will be 19/11 = 1.73 cells away from each other on average. Assuming one PVAA_PLL cell for the entire 2 byte lanes plus PLL the IR drop across one byte lane IR Drop from bump to PVAA_PLL cell = TC2B*0.5 = 37.32mA*0.5 ohm = 18.66mV IR Drop PVAA_PLL cell vertical= TC2B*R_VAA = 37.32mA*0.26 ohm = 9.70mV IR Drop from bump to MVAA_PLL rail = 18.66mV + 9.70mV = 28.36mV ○ Current gets split over two MVAA_PLL IO segments each with ½ the signal IOs ○ IR Drop to signal cell one = 10*current per IO*Total resistance per IO pitch*1.73 IO slots = 10*1.08mA*0.19*1.73 = 3.55mV ○ IR Drop to signal cell two = 9*current per IO*Total resistance per IO pitch*1.73 IO slots = 9*1.08mA*0.19*1.73 = 3.19mV ○ IR Drop to signal cell three = 8*current per IO*Total resistance per IO pitch*1.73 IO slots = 8*1.08mA*0.19*1.73 = 2.84mV ○ IR Drop to signal cell four = 7*current per IO*Total resistance per IO pitch*1.73 IO slots = 7*1.08mA*0.19*1.73 = 2.48mV ○ IR Drop to signal cell five = 6*current per IO*Total resistance per IO pitch*1.73 IO slots = 6*1.08mA*0.19*1.73 = 2.1XXV ○ IR Drop to signal cell six = 5*current per IO*Total resistance per IO pitch*1.73 IO slots = 5*1.08mA*0.19*1.73 = 1.77mV ○ IR Drop to signal cell seven = 4*current per IO*Total resistance per IO pitch*1.73 IO slots = 4*1.08mA*0.19*1.73 = 1.42mV ○ IR Drop to signal cell eight = 3*current per IO*Total resistance per IO pitch*1.73 IO slots = 3*1.08mA*0.19*1.73 = 1.06mV ○ IR Drop to signal cell nine = 2*current per IO*Total resistance per IO pitch*1.73 IO slots = 2*1.08mA*0.19*1.73 = 0.71mV ○ IR Drop to signal cell ten = 1*current per IO*Total resistance per IO pitch*1.73 IO slots = 1*1.08mA*0.19*1.73 = 0.35mV ○ Total IR drip on horizontal IO ring = 3.55 + 3.19 + 2.84 + 2.48 + 2.13 + 1.77 + 1.42 + 1.06 + 0.71 + 0.35 = 19.51mV ○ Total IR drop to last IO cell = 28.36 + 19.51 = 47.87mV This is clearly more than the IR drop limit (45mV) so we need to try with two PVAA_PLL cells in the IO ring **Calculations with 2 VAA_PLL cells (one per each byte lane)** **VAA_PLL IR Drop** With two PVAA_PLL cells the currents are divided in half and each PVAA_PLL cells feeds one byte lane + 1/2 PLL current. IR Drop from bump to PVAA_PLL cell = TC2B/2*0.5 = 37.32mA/2*0.5 ohm = 9.3XXV IR Drop PVAA_PLL cell vertical= TC2B/2*R_VAA = 37.32mA/2*0.26 ohm = 4.85mV IR Drop from bump to MVAA_PLL rail = 9.3XXV + 4.85mV = 14.18mV ○	

Lane	Calculation	Supply Requirements
	Current gets split over four MVAA_PLL IO segments each with 1/4 the signal IOs o IR Drop to signal cell one = 5*current per IO*Total resistance per IO pitch*1.73 IO slots = 5*1.08mA*0.19*1.73 = 1.77mV o IR Drop to signal cell two = 4*current per IO*Total resistance per IO pitch*1.73 IO slots = 4*1.08mA*0.19*1.73 = 1.42mV o IR Drop to signal cell three = 3*current per IO*Total resistance per IO pitch*1.73 IO slots = 3*1.08mA*0.19*1.73 = 1.06mV o IR Drop to signal cell four = 2*current per IO*Total resistance per IO pitch*1.73 IO slots = 2*1.08mA*0.19*1.73 = 0.71mV o IR Drop to signal cell five = 1*current per IO*Total resistance per IO pitch*1.73 IO slots = 1*1.08mA*0.19*1.73 = 0.35mV o Total IR drip on horizontal IO ring = 1.77 + 1.42 + 1.06 + 0.71 + 0.35 = 5.32mV o Total IR drop to last IO cell = 14.18 + 5.32 = 19.5mV Since 19.5mV< 45mV, two PVAA_PLL cells should be OK for 2 byte lanes plus PLL **PLL is not shared between two byte lanes (one PLL and one byte lane for one PVAA_PLL cell)** Total byte Lane IO current = 11 SSTL IO current = 11IOs * (SSTL DC current + SSTL AC current) o 11*(1.06mA+0.0226mA) = 11.91mA Total current for 1 Byte lanes = PLL current +one Byte Lane IO current (let us call this quantity TC1B) o Total Byte Lane Current = TC1B = 13.5mA + 11.91mA = 25.41mA **Vertical metal EM limit** VAA_PLL SSTL cell EM limits = IEM_VAA for Pad to MVAA_PLL vertical metal current limit and IEM_MVAA_PLL for MVAA_PLL horizontal bus metal current limit from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 EM Compliance table The number of PVAA_PLL cells needed based on vertical metal limit = TC1B/IEM_VAA o So in this case = 25.41mA/295mA = 0.086 < 1 so one cell would be sufficient **Horizontal metal EM limit** If we assume n VAA_PLL cells and place them equally distributed along the length of the IOs they are supplying current to - each IO segment physically divided by the VAA_PLLs will be carrying 1/(2n) of the total current assuming the current is equally distributed to each segment. Therefore the current on each segment must be less than the horizontal metal EM limit or TC1B/(2n) < IEM_MVAA_PLL Solving for the number of cells needed we have n > TC1B/(2*IE-MVAA_PLL) o So in our case n > 25.41mA/(2*40mA) = 0.318 or 1 cell should be sufficient. **VAA_PLL IR Drop** Assume 2.5% * 1.8V = 45mV is acceptable on die IR drop limit. Assume bump to VAA_PLL cell resistance = 0.5 ohm (replace this with the bump to IO pad resistance from your layout) VAA_PLL vertical metal resistance = R_VAA from the Power Grid Support table in the DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 o 0.26 ohms	

Lane	Calculation	Supply Requirements
	Horizontal metal resistance = R_MVAA_PLL from the Power Grid Support table in the DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 = 0.19 ohms in each cell. IO pitch is 25um We are assuming a Sig:pwr:ground cell ratio in the byte lane to be 2:1:1 for 11 signal cells for IR drop purposes. Since the signal:power:ground cell ratio is 2:1:1 with 11 signal cells we have 5 power and 5 ground for a total of 19 cells. Each signal cell will be 19/11 = 1.73 cells away from each other on average. Assuming one PVAA_PLL cell for the entire 1 byte lanes plus PLL the IR drop across one byte lane split into two since PVAA_PLL will be placed in the middle of the byte lane for best IR drop IR Drop from bump to PVAA_PLL cell = TC1B*0.5 = 25.41mA*0.5 ohm = 12.7mV IR Drop PVAA_PLL cell vertical= TC1B*R_VAA = 25.41mA*0.26 ohm = 6.61mV IR Drop from bump to MVAA_PLL rail = 12.7mV + 6.61mV = 19.31mV o Current gets split over two MVAA_PLL IO segments each with ½ the signal IOs o IR Drop to signal cell one = 5*current per IO*Total resistance per IO pitch*1.73 IO slots = 5*1.08mA*0.19*1.73 = 1.77mV o IR Drop to signal cell two = 4*current per IO*Total resistance per IO pitch*1.73 IO slots = 4*1.08mA*0.19*1.73 = 1.42mV o IR Drop to signal cell three = 3*current per IO*Total resistance per IO pitch*1.73 IO slots = 3*1.08mA*0.19*1.73 = 1.06mV o IR Drop to signal cell four = 2*current per IO*Total resistance per IO pitch*1.73 IO slots = 2*1.08mA*0.19*1.73 = 0.71mV o IR Drop to signal cell five = 1*current per IO*Total resistance per IO pitch*1.73 IO slots = 1*1.08mA*0.19*1.73 = 0.35mV o Total IR drip on horizontal IO ring = 1.77 + 1.42 + 1.06 + 0.71 + 0.35 = 5.32mV o Total IR drop to last IO cell = 19.31 + 5.32 = 24.6XXV Since 24.6XXV< 45mV, one PVAA_PLL cell should be OK for one byte lane plus PLL	
Command Lane	**Determining maximum VAA_PLL currents from PLL and IOs for Command Lane** **One PLL for the Command/Address** PLL Current (referenced to VSS) from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 = Max IVDD_PLL parameter from Power Dissipation table in DDR4 section o =13.5mA IO current (per IO) assumes TX and RX are powered up, IO in loop back mode with ODT disabled and TX output driver enabled. SSTL DC current: = (PRCV_VAA_PLL from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 DC transmit Mode power Dissipation table in DDR4 section) / Max VAA_PLL o =2mW/1.89V = 1.06mA SSTL AC current CLK: = (PRCVAA_PLL_AC from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 DDR4 mode (PDR=0 AC power table)uW/MHz*Switching frequency/Max VAA_PLL o =0.04*uW/MHz*1066MHz/1.89V = 0.0226mA o Current per IO = SSTL DC current + SSTL AC current = 1.06mA+0.0226mA = 1.08mA SSTL AC current non-CLK: = (PRCVAA_PLL_AC from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 DDR4 mode (PDR=0 AC power table)uW/MHz*Switching frequency/Max VAA_PLL	Add 2 VAA_PLL cells for the Command Lane

Lane	Calculation	Supply Requirements
	○ =0.04*uW/MHz*53XXHz/1.89V = 0.011XXA ○ Current per IO = SSTL DC current + SSTL AC current = 1.06mA+0.011XXA = 1.071XXA Total Command Lane IO current = 4 CLK +(37-4) non-CLK SSTL IO current = 4 * 1.08mA + 33 * 1.071XXA = 39.67mA Total current for Command Lane = PLL current + IO current (Let us call this quantity TCCL) ○ Total Command Lane current = TCCL = 13.5mA + 39.67mA = 53.17mA **Vertical metal EM limit** VAA_PLL SSTL cell EM limits = IEM_VAA for Pad to MVAA_PLL vertical metal current limit and IEM_MVAA_PLL for MVAA_PLL horizontal bus metal current limit from DesignWare Cores Gen 2 DDR multiPHY databook for TSMC28HPM18 EM Compliance table The number of PVAA_PLL cells needed based on vertical metal limit = TCCL/IEM_VAA ○ So in this case = 53.17mA/250mA = 0.213 < 1 so one cell would be sufficient **Horizontal metal EM limit** If we assume n VAA_PLL cells and place them equally distributed along the length of the IOs they are supplying current to - each IO segment physically divided by the VAA_PLLs will be carrying 1/(2n) of the total current assuming the current is equally distributed to each segment. Therefore the current on each segment must be less than the horizontal metal EM limit or TCCL/(2n) < IEM_MVAA_PLL Solving for the number of cells needed we have n > TCCL/(2*IE-MVAA_PLL) ○ So in our case n > 53.17mA/(2*40mA) = 0.665 or 1 cell should be sufficient. Note that EM limit for the bump (process dependent) should also be checked. In this it is assumed to be OK. **VAA_PLL IR Drop** Assume 2.5% * 1.8V = 45mV is acceptable on die IR drop limit. Assume bump to VAA_PLL cell resistance = 0.5 ohm VAA_PLL vertical metal resistance = R_VAA from the Power Grid Support table in the DesignWare Cores Gen 2 DDR multiPHY databook for TSMC28HPM18 = 0.26 ohms Horizontal metal resistance = R_MVAA_PLL from the Power Grid Support table in the DesignWare Cores Gen 2 DDR multiPHY databook for TSMC28HPM18 = 0.19 ohms in each cell. IO pitch is 25um Assuming a Sig:pwr:ground cell ratio in the Command lane to be 3:1:1 for 37 signal cells for IR drop purposes. Assuming one PVAA_PLL cell for the entire Command lane plus PLL ○ IR Drop from bump to PVAA_PLL cell = TCCL*0.5 = 53.17mA*0.5 ohm = 26.59mV ○ IR Drop PVAA_PLL cell vertical = TCCL*0.26 = 53.17mA*0.26 ohm = 13.82mV ○ IR Drop from bump to MVAA_PLL rail = 26.59mV + 13.82mV = 40.41mV MVAA_PLL current gets split over two MVAA_PLL segments each with ½ the signal IOs Since the signal:power:ground cell ratio is 3:1:1 with 18 signal cells we have 6 power and 6 ground for a total of 30 cells. Each signal cell will be 30/18 = 1.66 cells away from each other on average.	

Lane	Calculation	Supply Requirements
	○ IR Drop to signal cell one = 18*current per IO*Total resistance per IO pitch*1.66 IO slots = 18*1.071XXA*0.19*1.66 = 27mV + 6.9mV = 6.08mV ○ Total IRdrop so far is 40.41mV + 6.08mV = 46.49mV This is more than the IR drop limit so we need to try with 2 PVAA_PLL in the IO ring **Calculations with 2 VAA_PLL cells and two bumps** With two PVAA_PLL cells the currents are divided in half and each PVAA_PLL cells feeds one half Command lane + 1/2 PLL current. ○ IR Drop from bump to PVAA_PLL cell = TCCL/2*0.5 = (53.17/2)mA*0.5 ohm = 13.29mV ○ IR Drop PVAA_PLL cell vertical = TCCL/2*0.26 = (53.17/2)mA*0.26 ohm = 6.91mV ○ IR Drop from bump to MVAA_PLL rail = 13.29mV + 6.91mV = 20.2mV MVAA_PLL current gets split over four MVAA_PLL segments each with 1/4 the signal IOs (37/4 = 9 cells) IR Drop to signal cell one = 9*current per IO*Total resistance per IO pitch*1.66 IO slots = 9*1.071XXA*0.19*1.66 = 3.04mV IR Drop to signal cell two = 8*current per IO*Total resistance per IO pitch*1.66 IO slots = 8*1.071XXA*0.19*1.66 = 2.70mV IR Drop to signal cell three = 7*current per IO*Total resistance per IO pitch*1.66 IO slots = 7*1.071XXA*0.19*1.66 = 2.37mV IR Drop to signal cell four = 6*current per IO*Total resistance per IO pitch*1.66 IO slots = 6*1.071XXA*0.19*1.66 = 2.027mV IR Drop to signal cell five = 5*current per IO*Total resistance per IO pitch*1.66 IO slots = 5*1.071XXA*0.19*1.66 = 1.69mV IR Drop to signal cell six = 4*current per IO*Total resistance per IO pitch*1.66 IO slots = 4*1.071XXA*0.19*1.66 = 1.35mV IR Drop to signal cell seven = 3*current per IO*Total resistance per IO pitch*1.66 IO slots = 3*1.071XXA*0.19*1.66 = 1.01mV IR Drop to signal cell eight = 2*current per IO*Total resistance per IO pitch*1.66 IO slots = 2*1.071XXA*0.19*1.66 = 0.68mV IR Drop to signal cell nine = 1*current per IO*Total resistance per IO pitch*1.66 IO slots = 1*1.071XXA*0.19*1.66 = 0.34mV Total IO drop horizontal PVAA_PLL bus = 15.21mV Total IR drop = 20.2mV + 15.21mV = 35.41 Since 35.41mV< 45mV, two PVAA_PLL cells should be OK for Command lane plus PLL	
Totals	Command Lane - 1525um + 2 VAA_PLL cells + 1 VSS (for PLL) - 1525um + (3 * 25um) = 1600um total length, not including core power supply slots Byte Lane - Require 1 VAA_PLL cell + 1 VSS (for PLL) - 550um per byte lane + (2 * 25um) = 600um total length, not including core power supply slots 1 Command Lane + 9 Byte Lanes - 1600um + (9 * 600um) = 7000um total length, not including core power supply slots	

2.2.3 Core Power Requirements

As can be seen from the calculations thus far, the memory interface will require a considerable linear length on the pad frame. For most wire bond designs, it is not possible to meet the core logic power grid requirements (IR drop, EM) if there are no dedicated core VDD/VSS power pads within the pad frame length occupied by the memory interface. Core power is also required in this area to supply power to the PHY elements, including the DDR3PHYAC, DDR3PHYDATX8, and core logic of the SSTL.

There are two common types of core power distribution in today's IC designs: distribution from the center and distribution from the die-edge pad frame. Center distribution is only possible with flip-chip designs. Pad frame distribution is a requirement of wire bond designs.

Assuming a design with distribution from the pad frame, the typical power planning process starts by determining the total worst-case core power consumption of the design, determining how many core power pads are required to support that power consumption, then determining the proper core power pad distribution within the pad frame to ensure proper supply of the core power grid. The determination of worst-case core power would include the customer's ASIC logic, other hard-IP blocks, and the memory controller RTL and hard-IP PHY components.

Note: The frequency of PVDD cells in the pad ring may be dependent on the core clamp ESD approach that is taken. If VDD supply clamps are placed in the core of the chip, then no PVDD cells are required in the pad ring. If the core clamps are placed in the peripheral IO ring, then the guideline is at least one per Byte lane, and 2 per Command lane. In either case, the number of required VSS ground cells in the IO ring is determined by the VSS rail effective resistance from an IO to multiple VSS bump/bond pads carrying ESD discharge current; this resistance must meet ESD discharge path resistance rules as defined by the foundry (e.g. <1 ohm)..

The following tables are provided as an example to assist the designer in determining pad frame core power pad requirements for a flip chip design. It is assumed that the core power of the PHY (PLL, PHYAC, DATX8 macros) components will be supplied by bumps in the center of the die. The tables provide the current that must be supplied from the center of the die to the DDRn hard IP components for a Flip Chip design. The user should use these tables for illustrative purposes only. The user must refer to the AC/DC specifications for each component and taking into account the desired operating frequency determine the core power consumption for their application. Following this, the user must refer to the IR drop and electro-migration tables for the SSTL cells to determine their appropriate required number of core power/ground cells.

Table 7:PHY Supply Requirements - Flip Chip Examples

Flip Chip Example
Core-side of SSTL I/Os powered by VDD/VSS IO cells
PLL, PHYAC, DATX8 macros powered by core VDD/VSS bumps in center of die
1066MHz/2133bps SDRAM operating rate, 100% switching activity factor (worst case)
Flip chip packaging
Maintain an IR drop to the AC and DATX8 of less than 2.5% per VDD or VSS connection
Assume SSTL loop-back mode is active
Configuration of Byte Lane and Command Lane signals as per our previous description

Table 8: Example Core Power Requirements – Flip Chip ICLane

Lane	Flip chip Calculation	Supply Requirements
Each Byte Lane	**Determining maximum VDD currents from DATX8 PHY, PLL and IOs for Byte lane** DATX8 PHY VDD Worst case current from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 = 54.16mW/0.99V = 54.7mA PLL VDD Worst case Current (referenced to VSS) from DesignWare Cores Gen DDR4 multiPHY databook for TSMC28HPM18 = 1.2mA **PLL is shared between 2 byte lanes** Total core supply current from die center bumps for 2 DATX8 macros + PLL = 2* 54.7mA +1.2mA = 110.6mA **One PLL for a byte lane** Total core supply current from die center bumps for 1 DATX8 macro + PLL = 54.7mA +1.2mA = 55.9mA For the example DDR Interface there are 9 data byte lanes so 4 data lane pairs that share a PLL each plus one byte lane with its own PLL Total core current for DATX8 and PLLs = 4*110.6mA + 55.9mA = 498.XXA **IO core current supplied by VDD/VSS cells** IO current (per IO) assumes TX and RX are powered up, IO in receive mode with ODT enabled and TX output driver enabled (loop back mode) SSTL TX DC current: = (PDRV VDD from DesignWare Cores Gen DDR4 multiPHY databook for TSMC28HPM18 DC Drive Mode power Dissipation table in DDR4 section) / Max VDD=776.9uW/0.99V = 0.785mA SSTL TX AC current: = (PDRV_AC from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 LPDDR3 mode (PDR=0 AC power table)uW/MHz*Switching frequency/Max VDD =2.24uW/MHz*1066MHz/0.99V = 2.41mA Current per IO = SSTL DC current + SSTL AC current = 0.785mA + 2.41mA = 3.195mA Total byte Lane IO current = 11 SSTL IO current = 11IOs * (SSTL current) =11*(3.195mA) = 35.15 mA **Vertical metal EM limit IO VDD supply** VDD SSTL cell EM limits = IEM_VDD for Pad to MVDD vertical metal current limit and IEM_MVDD for MVDD horizontal bus metal current limit from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 EM Compliance table The number of PVDD cells needed based on vertical metal limit = 45.76mA/IEM_VDD o So in this case = 45.76mA/250mA = 0.183 < 1 so one cell would be sufficient **Horizontal metal EM limit** If we assume n VDD cells and place them equally distributed along the length of the IOs they are supplying current to - each IO segment physically divided by the VDD will be carrying 1/(2n) of the total current assuming the current is equally distributed to each segment. Therefore the current on each segment must be less than the horizontal metal EM limit or 45.76/(2n) < IEM_MVDD Solving for the number of cells needed we have n > 45.76/(2*IEM_VDD) o So in our case n > 45.76mA/(2*40mA) = 0.572 or 1 VDD cells should be sufficient. **VDD IR Drop.** Assume 2.5% * 0.99V = 24.75mV is acceptable on die IR drop limit. VDD vertical metal resistance = R_VDD from the Power Grid Support table in the DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 0.26 ohms	Add 2 VDD cells per byte lane

Lane	Flip chip Calculation	Supply Requirements
	Horizontal metal resistance = R_MVDD from the Power Grid Support table in the DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 = 0.2 ohms in each cell. IO pitch is 25um Assuming a Sig:pwr:ground cell ratio in the byte lane to be 2:1:1 for 11 signal cells for IR drop purposes. Since the signal:power:ground cell ratio is 2:1:1 with 11 signal cells we have 5 power and 5 ground for a total of 19 cells. Each signal cell will be 19/11 = 1.73 cells away from each other on average. Assuming one PVDD IO cell for the entire byte lane Assume bump to VDD cell resistance = 0.5 ohm (replace this with the bump to IO pad resistance from your layout) IR Drop from bump to PVDD IO cell = 35.15mA*0.5 = 17.57mV IR Drop PVDD cell vertical= IVDD*R_VDD = 35.15mA*0.26 ohm = 9.14mV IR Drop from bump to MVDD rail = 17.57mV + 9.14mV = 26.7mV This IR drop is bigger than 24.75mV, so we try two VDD cells and recalculate the IRdrop Assuming two PVDD IO cells for the entire byte lane so each cell gets ½ half the VDD IO current Assume bump to VDD cell resistance = 0.5 ohm (replace this with the bump to IO pad resistance from your layout) IR Drop from bump to PVDD IO cell = (35.15mA/2)*0.5 = 8.79mV IR Drop PVDD cell vertical= IVDD*R_VDD = (35.15mA/2)*0.26 ohm = 4.57mV IR Drop from bump to MVDD rail = 8.79mV + 4.57mV = 13.36mV Current gets split over four MVDD IO segments each with 1/4the signal IOs o IR Drop to signal cell one = 3*current per IO*Total resistance per IO pitch*1.73 IO slots = 3*3.195mA*0.2*1.73 = 3.32mV o IR Drop to signal cell two = 2*current per IO*Total resistance per IO pitch*1.73 IO slots = 2*3.195mA*0.2*1.73 = 2.21mV o IR Drop to signal cell three = 1*current per IO*Total resistance per IO pitch*1.73 IO slots = 1*3.195mA*0.2*1.73 = 1.11mV o Total IR drip on horizontal IO ring = 3.32 + 2.21 + 1.11 = 6.64mV o Total IR drop to last IO cell = 13.36 + 6.64 = 20mV Since byte lane IR drop< 24.75mV, 2 VDD cells should be OK for a byte lane	
Command Lane	**Determining maximum VDD currents from PLL and PHYAC and IOs for Command Lane** PHYAC VDD Worst case current from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 = 60.61mW/0.99V = 61.22mA PLL VDD Worst case Current (referenced to VSS) from DesignWare Cores Gen DDR4 multiPHY databook for TSMC28HPM18 = 1.2mA **One PLL is used for PHYAC** Total core supply current from die center bumps for PHYAC macro + PLL = 61.22mA +1.2mA = 110.6mA Total core supply current from die center bumps for 1 DATX8 macro + PLL = 54.7mA +1.2mA = 62.42mA **IO core current supplied by VDD/VSS cells** IO current (per IO) assumes TX and RX are powered up, IO in receive mode with ODT enabled and TX output driver enabled (loop back mode) SSTL TX DC current: = (PDRV VDD from DesignWare Cores Gen DDR4 multiPHY databook for TSMC28HPM18 DC Drive Mode power Dissipation table in DDR4 section) / Max VDD=776.9uW/0.99V = 0.785mA SSTL TX AC current: = (PDRV_AC from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 LPDDR3 mode (PDR=0 AC power table)uW/MHz*Switching frequency/Max VDD	Add 4 VDD cells for the Command Lane

Lane	Flip chip Calculation	Supply Requirements
	=2.24uW/MHz*53XXHz/0.99V = 1.21mA Current per IO = SSTL DC current + SSTL AC current = 0.785mA + 1.21mA = 2.0mA Total Command Lane IO current = 37 SSTL IO current = 37IOs * (SSTL current) =37*(2.0mA) = 74 mA **Vertical metal EM limit IO VDD supply** VDD SSTL cell EM limits = IEM_VDD for Pad to MVDD vertical metal current limit and IEM_MVDD for MVDD horizontal bus metal current limit from DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 EM Compliance table The number of PVDD cells needed based on vertical metal limit = 106.2mA/IEM_VDD o So in this case = 74mA/250mA = 0.296 < 1 so one cell would be sufficient **Horizontal metal EM limit** If we assume n VDD cells and place them equally distributed along the length of the IOs they are supplying current to - each IO segment physically divided by the VDD will be carrying 1/(2n) of the total current assuming the current is equally distributed to each segment. Therefore the current on each segment must be less than the horizontal metal EM limit or 106.2/(2n) < IEM_MVDD Solving for the number of cells needed we have n > 74/(2*IEM_VDD) o So in our case n > 74mA/(2*40mA) = 0.925 which is close to one but we should try with 2 VDD cells to be safe. **VDD IR Drop.** Assume 2.5% * 0.99V = 24.75mV is acceptable on die IR drop limit. VDD vertical metal resistance = R_VDD from the Power Grid Support table in the DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 0.26 ohms Horizontal metal resistance = R_MVDD from the Power Grid Support table in the DesignWare Cores DDR4 multiPHY databook for TSMC28HPM18 = 0.2 ohms in each cell. IO pitch is 25um Since the signal:power:ground cell ratio is 3:1:1 with 37 signal cells we have 12 power and 12 ground for a total of 61 cells. Each signal cell will be 61/37 = 1.65 cells away from each other on average. Assuming two PVDD IO cell for the command address lane so current through each PVDD cell = 74mA/2 = 37mA Assume bump to VDD cell resistance = 0.5 ohm (replace this with the bump to IO pad resistance from your layout) IR Drop from bump to PVDD IO cell = 37mA*0.5 = 18.5mV IR Drop PVDD cell vertical= IVDD*R_VDD = 37mA*0.26 ohm = 9.62mV IR Drop from bump to MVDD rail = 18.5mV + 9.62mV = 28.12mV This IR drop is bigger than 24.75mV, so we try with three VDD cells and recalculate the IRdrop Assuming three PVDD IO cells for the command/address lane so each cell gets 1/3 the VDD IO current Assume bump to VDD cell resistance = 0.5 ohm (replace this with the bump to IO pad resistance from your layout) IR Drop from bump to PVDD IO cell = (74mA/3)*0.5 = 12.XXV IR Drop PVDD cell vertical= IVDD*R_VDD = (74mA/3)*0.26 ohm =6.41 mV IR Drop from bump to MVDD rail = 12.XXV + 6.41mV = 18.71mV MVDD Current gets split over six MVDD IO segments each with 1/6 the signal IOs (37/6 = 6 cells) o IR Drop to signal cell one = 6*current per IO*Total resistance per IO	

Lane	Flip chip Calculation	Supply Requirements
	pitch*1.65 IO slots = 6*2mA*0.2*1.65 = 3.96mV o IR Drop to signal cell two = 5*current per IO*Total resistance per IO pitch*1.65 IO slots = 5*2mA*0.2*1.65 = 3.XXV o IR Drop to signal cell three = 4*current per IO*Total resistance per IO pitch*1.65 IO slots = 4*2mA*0.2*1.65 = 2.64mV o IR Drop to signal cell four = 3*current per IO*Total resistance per IO pitch*1.65 IO slots = 3*2mA*0.2*1.65 = 1.98mV o IR Drop to signal cell five = 2*current per IO*Total resistance per IO pitch*1.65 IO slots = 2*2mA*0.2*1.65 = 1.32mV o IR Drop to signal cell six = 1*current per IO*Total resistance per IO pitch*1.65 IO slots = 1*2mA*0.2*1.65 = 0.66mV o Total IR drip on horizontal IO ring = 3.96 + 3.3 + 2.64 + 1.98 + 1.32 + 0.66 = 13.86mV o Total IR drop to last IO cell = 18.7 + 13.86 = 32.56mV This IR drop is bigger than 24.75mV, so we try four VDD cells and recalculate the IRdrop Assuming four PVDD IO cells for the command/address lane so each cell gets 1/4 the VDD IO current Assume bump to VDD cell resistance = 0.5 ohm (replace this with the bump to IO pad resistance from your layout) IR Drop from bump to PVDD IO cell = (74mA/4)*0.5 = 9.25mV IR Drop PVDD cell vertical= IVDD*R_VDD = (74mA/4)*0.26 ohm =4.81 mV IR Drop from bump to MVDD rail = 9.25mV + 4.81mV = 14.06mV MVDD Current gets split over eight MVDD IO segments each with 1/8 the signal IOs (37/8 = 4.63 or 5 cells) o IR Drop to signal cell one = 5*current per IO*Total resistance per IO pitch*1.65 IO slots = 5*2mA*0.2*1.65 = 3.XXV o IR Drop to signal cell two = 4*current per IO*Total resistance per IO pitch*1.65 IO slots = 4*2mA*0.2*1.65 = 2.64mV o IR Drop to signal cell three = 3*current per IO*Total resistance per IO pitch*1.65 IO slots = 3*2mA*0.2*1.65 = 1.98mV o IR Drop to signal cell four = 2*current per IO*Total resistance per IO pitch*1.65 IO slots = 2*2mA*0.2*1.65 = 1.32mV o IR Drop to signal cell five = 1*current per IO*Total resistance per IO pitch*1.65 IO slots = 1*2mA*0.2*1.65 = 0.66mV o Total IR drip on horizontal IO ring = 3.3 + 2.64 + 1.98 + 1.32 + 0.66 = 9.9mV o Total IR drop to last IO cell = 14.06 + 9.9 = 23.96mV Since Command Lane IR drop< 24.75mV, 4 VDD cells should be OK for a Command lane	
Totals	Assume Peripheral ESD Protection for the IO VDD nets therefore a minimum 2 VDD/VSS pairs are required in the Command Lane and 1 VDD/VSS pair is required in the Data byte lanes Command Lane - 1600um total length, not including core power supply slots - 4 VDD/VSS pairs are required for DDR IP - 1600um + (4 * 25um) + (4 *25um) = 1800um Byte Lanes - 600um byte lane total length, not including core power supply slots - 2 VDD/VSS pairs are required for DDR IP - 600um + (2 * 25um) + (2 *25um) = 700um	

Lane	Flip chip Calculation	Supply Requirements
	1 Command Lane + 9 Byte Lanes - 1800um + 9 *700um = 8100um total length	

2.2.4 Internal VREF Requirements

Internal VREF cell is required in the pad frame to supply the comparator reference for the SSTL inputs. VREF can be sensitive to noise if undriven for long distances which could impact receive performance at high data rates.

The recommendation for VREF insertion is one VREF slot for every XXm of pad frame length, approximately centered within the XXm section. This results in a maximum distance from the VREF pad of 1.5mm. When determining the drive distance around the edge of the die, the corner cell is included in the calculation.

DDR4 mode also has a special requirement that the data byte lanes may require an offset VREF reference voltage due to the fact the input ODT termination is a pullup to VDDQ (not pullup/pulldown as in DDR3). This requires a VREF voltage that is higher than VDDQ/2. The exact equation is VREF = (2Ron +Rodt)/(Ron + Rodt) * (VDDQ/2) where Ron is the drive strength of the TX IO (SDRAM) and RODT is the (local) ODT termination to VDDQ of the receiver. For this reason the data byte lanes should have a different PVREF cell and MVREF bus than the Command lane. In addition, since the impedance of the output drivers of each SDRAM chip has a tolerance which will effect optimal VREF level, it is recommended that the local VREF level at the SOC SSTL receivers for data byte lanes use a different VREF level per byte. Therefore a PVREF cell is required per byte in the data lanes. Each PVREF cell has an internal programmable VREF level generator that can be programmed to the optimal VREF settling per byte. To isolate the MVREF bus of one byte lane to the next PVSSQZB_ZQ cut cells are required at the borders of each data byte lane and between data byte lanes and command address lane. Since the data byte lanes will have PVSSQ cells already, two of those cells can be converted to PVSSQZB_ZQ cells with no increase in IO ring cell count.

In systems where multiple ranks of memories are supported, and since each rank will be made up with different SDRAM chips with tolerance on the output drive strength, the local SSTL receivers need to have a different VREF level per rank and per data byte. To address this situation an additional PVREF_DAC cell is required in each byte lane. This will allow support of up to 4 ranks with a different VREF level for each. There are four internal VREF generator (independently programmable) circuits in the PVREF_DAC cell to supply a different VREF level per rank. The PHY logic will know which rank is being addressed and select the appropriate VREF level for that rank. Also note that the PVREF_DAC cell has VSS on its pad so this provides another connection to MVSS bus from off die.

Note that for DDR4 mode, SDRAM chips have their own internal programmable VREF generator for data SSTL inputs on die. So there is no requirement to generate VREF for the SDRAM. Likewise local data byte lane VREF generation for SOC SSTL receivers will be supported as described earlier. VREF for command/address is required for the SDRAM and for local SSTL receivers in the SOC from an external source which should be set to VDDQ/2.

The calibration cell PZQ should also have its own VREF cell in the form of a PZCTRL cell. The MVREF and ZIOH busses of these islands (Data bytes, Command, Calibration) should be isolated from each other. This can be done most easily by placing the PZQ and PZCTRL cells in between command lane and data byte lanes. The PZQ and PZCTRL cells cut the ZIOH and MVREF busses making 3 separate ZIOH/MVREF islands. If PZQ and PZCTRL cells placed next to each other their own ZIOH/MVREF island is formed by abutment.

Returning to our example designs:

Table 9:VREF Flip Chip Example

Flip Chip Example

Command Lane

- 1800um total length
- Calculating total PVREF cells required by length
- 1800/3000um = 0.6 or 1 cell should be sufficient
- Also 1 PZCTRL cell is required for IO calibration which is placed next to the PZQ cell in the Command lane
- Total length = 1800 + 25um + 25um = 1850um

Byte Lane

- 700um total length
- We require one PVREF cell and one PVREF_DAC cell per byte lane and two PVSSQ cells will be converted to PVSSQZB_ZQ cells.

2.2.5 Dedicated Test Pin Requirement

It is highly suggested to add dedicated test pins for the PHY. This enables direct access for testing and characterization purposes, along with the ability to monitor the PHY during normal operation. The PHY contains three test outputs including two digital test outputs and one analog test output. The digital test outputs need to be viewed simultaneously.

The two digital test outputs (use PDDRIO SSTL cells) from each PLL block and the delay oscillator test out from each PHY block are connected back to the PUB soft-IP (verilog RTL) block for multiplexing, then the final two digital test outputs come from the PUB block. Two output pins can be dedicated to these signals. If this is not feasible, an alternate test access would be to use the test MUX which is embedded in the SSTL to permit a functional pin to be used for test signal access, although this could interfere with normal operation when connected to an SDRAM so the user should take this into consideration as these may only be accessible when not connected to an SDRAM. The designer should ensure the logic path and the output pins for these two digital signals can properly pass 53XXHz clock signals (for a 213XXbps SDRAM system).

One analog signal pin (PAIO cell in the SSTL I/O Library) can be shared for all PLLs of the PHY. The PLLs include a programmable setting to tri-state the analog test output. Thus all PLLs can be connected to a common net and PLLs are selected one at a time to drive the net. This would be a dedicated pin for PLL testing. Since this is an analog signal, the user should ensure this net does not have any logic or buffering added/inserted during the ASIC design flow.

Ideally these test pins would be located near the end of the command/address lane

Returning to the example designs:

Table 10:Test Pin Flip Chip Examples

Flip chip Example
Adding 3 dedicated test pins for the entire PHY, our new total interface size becomes; 1 Command Lane + 9 Byte lanes + 3 test cells 1850um + 9 * 750um + 3 * 25um = 8675um

2.2.6 Retention Latch Enable Input Pin Requirement

The SSTL I/O library has cells that can be used for SDRAM data retention mode (self refresh power down). In this mode, the I/O ring supports a retention function that may be used to retain a known state on the CKE signal to the SDRAM while the host IC is placed in a low power mode, specifically when the core VDD supply is powered down. The general concept is that an external input signal (Data_Retention_N) is driven low to latch the state of specific signals driven to the SDRAM (CKE, SDRAM_RESET_n) putting the SSTL I/O cells into retention mode shortly before the core VDD supply is powered down.

A special Retention Latch Enable Input cell is required to receive and distribute the Data_Retention_N signal by abutment.

PRETPOCX or PRETPOCC cell

Note: A maximum skew of 300ps is allowed between Data Retention Input pins (RET and RET_B)

In addition, the VDDQ IO supply of the other signals of the DDR interface can be powered down to save power in the CKE retention mode. However, an island of signals (CKE, SDRAM_RESET_n) must have VDDQ powered up during the CKE retention mode. This island needs to have its VDDQ power bus (MVDDQ) isolated (through package and PCB as well) from the VDDQ supply to the rest of the DDR interface IO which are powered down. The VDDQ isolation is achieved by the use of two PFILL5_ISO cells surrounding the CKE retention island as well as two VDDQ_ESD cells need to be in the island for VDDQ supply and ESD protection needs. The drive strength settings of the CKE and SDRAM_RESET_n IO cells need to be maintained in the CKE retention island so a PVREF cell needs to be added to the CKE retention island. Since the ZIOH bus of the CKE retention island needs to be isolated from the non-retention IO bus two PVSSQZB_ZQ cells need to be located on the borders of the CKE retention island. Since PVSSQ cells are required in the Address/command lane two PVSSQ cells can be assigned to PSSQZB_ZQ cells.

DDR4 mode has an additional pin Alert_n on the DDR interface which is an input from the SDRAM. It is recommended that this IO cell be placed in the CKE retention island when VDDQ is isolated since this input will be driven by a termination to VDDQ on the PCB. If the Alert_n pin were located in the Command/address IO ring outside the CKE retention VDDQ isolated IO ring and VDDQ supply is removed this will cause current to flow through the protection diodes of the Alert_n IO and unintentionally power the Command/Address IO ring.

The Alert_n pin is an input signal which is VDDQ terminated and requires a VREF reference. The value of VREF required for the Alert_n input depends on the resistance value of the termination on the Alert_n net. Since this VREF value can be different than the rest of the Address/Command VREF (VDDQ/2) and the data byte VREF values, the VREF value for the Alert_n IO should be created by the internal generator (MVREF) of the PVREF cell in the CKE retention island. In addition, it is recommended to isolate the pad of this PVREF cell from an externally generated PCB VREF to avoid contention. It can simply be disconnected on the PCB or the internal pad switch (ENPAD) of the PVREF cell can be used to disconnect the pad from the internal VREF generator.

If the rest of the Address/Command IO cells outside the CKE retention region are powered down and are still driven by an external VREF source on the PCB, this could cause unintended current to flow into the IO VDDQ supply through PVREF cell IO protection diodes. If this connection needs to be maintained, it is recommended to power down the external VREF signal to the Address/Command PVREF cells outside the CKE retention island. Another possibility is to use the internal PVREF generators of the PVREF cells for the Address/Command IO cells outside the CKE retention island and not connect the PVREF pads to any VREF source on the PCB. Also keep in mind the SDRAM requires a valid VREF input (VDDQ/2) during self refresh power down mode since its CKE input uses VREF as a reference.

Please refer to the PHY databook Retention Latch Enable Input Power On Clear (DWC_D4M_PRETPOCX) for more implementation details.

Returning to the example design, adding data retention capability with VDDQ isolation:

Table 11:Retention Latch Enable Flip Chip Example

Flip chip Example 1 Command Lane + 9 Byte lanes - 8675um total length Flip chip Example Adding 1 PRETPOCX cell, 2 PFILL5_ISO cells, 1 PVREF cell Note that two existing PVSSQ cells will be converted to PVSSQZB_ZQ cells (no additional cells) and two PVDDQ cells will be converted to PVDDQ_ESD (no additional cells) New total interface size becomes: 1 Command Lane + 9 Byte lanes + 1 PRETPOCX + 2 PFILL5_ISO + 1 PVREF = 8675um + 25um + (2 * 5um) + 25um = 8735um total length

2.2.7 SSTL PVT Groups

The purpose of SSTL I/O PVT compensation is to account for Process, Voltage, and Temperature variations to achieve more consistent / predictable signaling on the external system interface. Due to effects such as OCV / ACLV, local heating effects, and local IR drops, it may be desirable to divide the interface into multiple PVT groups such that each group of I/Os can have its own local PVT compensation. The selection of groupings is not straight-forward as many considerations are the result of the process and the user's design/floorplan.

Some recommendations can be driven by certain design considerations, for example if SSTL cells were oriented in different directions, this could be a choice for grouping. In general, with a 32-bit/48-bit interface one PVT compensation group is sufficient. Even when wrapping around die corners with these interface sizes, unless the customer knows of some special chip logic which will create considerably different temperature differences at different parts of the die, one PVT compensation group is sufficient. A 64-bit/72bit interface consumes a larger amount of die area and is a typical candidate for division into 2 PVT groups.

There may be special cases where even higher numbers of PVT groups (i.e. 3 or 4) may be desirable. An example of such a case may be the implementation by the user of independent islands of SSTL cells on the die, which could be found in some flip-chip applications. In such a case, it may make sense for independent PVT control of each island due to the remote nature of the SSTL cell islands.

If there are multiple PVT compensation islands instantiated in a system, a break must occur (i.e. insertion of a PVT break cell like PVSSQZB, PZCTRL, or PZQ) to separate the different sets of level-shifted PVT adjustment signals (ZIOH).

2.2.8 Pin Muxing Considerations Between DDR4/DDR3 Modes

In some designs the DDR interface might need to support both DDR3 and DDR4 modes. The data byte lanes will remain the same for both modes but there are some pin differences between DDR3 and DDR4 mode for the Address/Command pins. There are some new signals in the DDR4 mode of operation which are not muxed with DDR3 mode pins. They are Alert_n (input), Parity, and BG1 with their own new pins. The rest of the new DDR4 Address/command signals pins are muxed function between DDR3 and DDR4 to save pins on the interface. A table is provided to show which signals are muxed and not muxed between DDR3 and DDR4 modes. Highlighted signals (bold outline) are the new DDR4 mode signals.

Table 12:Address/Command DDR3/DDR4 pin muxing

Address/Command DDR3/DDR4 pin muxing

DDR3	DDR4
a[13]	a[13]
a[14]	a[14]
a[15]	a[15]
a[12]	a[12]
a[11]	a[11]
a[10]	a[10]
a[9]	a[9]
a[8]	a[8]
a[7]	a[7]
a[6]	a[6]
a[5]	a[5]
a[4]	a[4]
a[3]	a[3]
a[2]	a[2]
a[1]	a[1]
a[0]	a[0]
	bg1
	par
ck[1]	ck[1]
ck_n[1]	ck_n[1]
ck[0]	ck[0]
ck_n[0]	ck_n[0]
ba[2]	bg0
ba[1]	ba[1]
ba[0]	ba[0]
cke[0]	cke[0]
odt[0]	odt[0]
cs_n[0]	cs_n[0]
we_n	a[16]
cas_n	a[17]
ras_n	act_n
cke[1]	cke[1]
cs_n[1]	cs_n[1]
odt[1]	odt[1]
	alert_n

2.2.9 VDDQ ESD Calculation

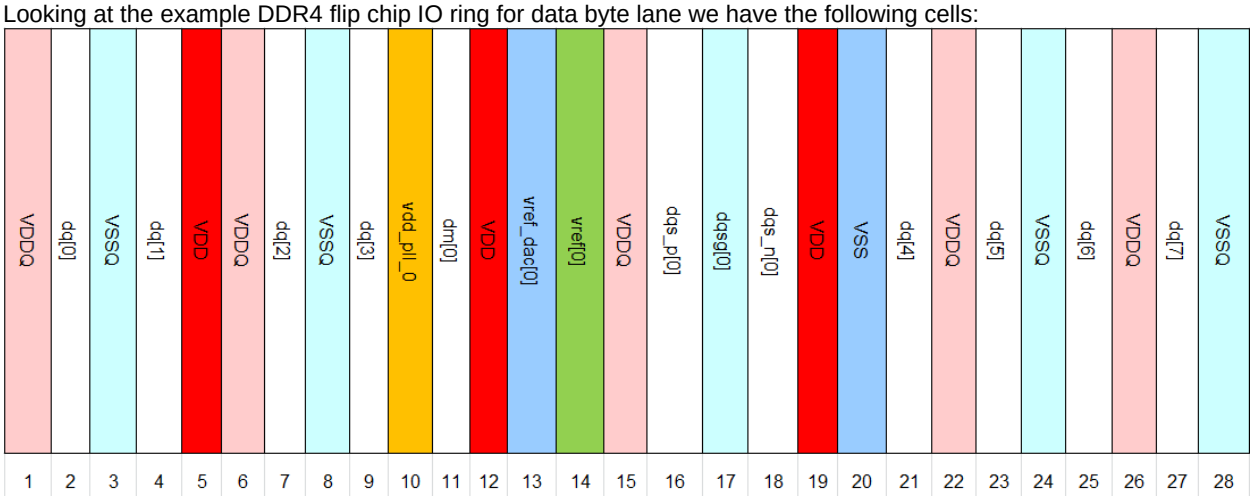
The IO cell library has two different PVDDQ cells; PVDDQ_ESD and PVDDQ_CAP. The PVDDQ_ESD cell contains ESD clamps for ESD protection and the PVDDQ_CAP does not have the clamps but has extra VDDQ-VSSQ decoupling cap in its space. Up until this point we have determine required number of cells based on SI/EM/IRdrop limits of the cells. To determine adequate numbers of PVDDQ_ESD cells required for ESD requirements refer to Section 4.7.4 in the ESD section.

ESD Requirements for the MVDDQ net show that the bus resistance must be less than 0.5 ohm from signal IO to ESD clamp cell if the clamp cell is only on one side of the signal IO cell, or less than 1 ohm to nearest clamp cell if IO clamp cells are on both sides of the signal IO cell. MVDDQ horizontal bus resistance R_MVDDQ is 0.04ohms in power Grid Support table 6-81 of the DDR4 multiphy databook.

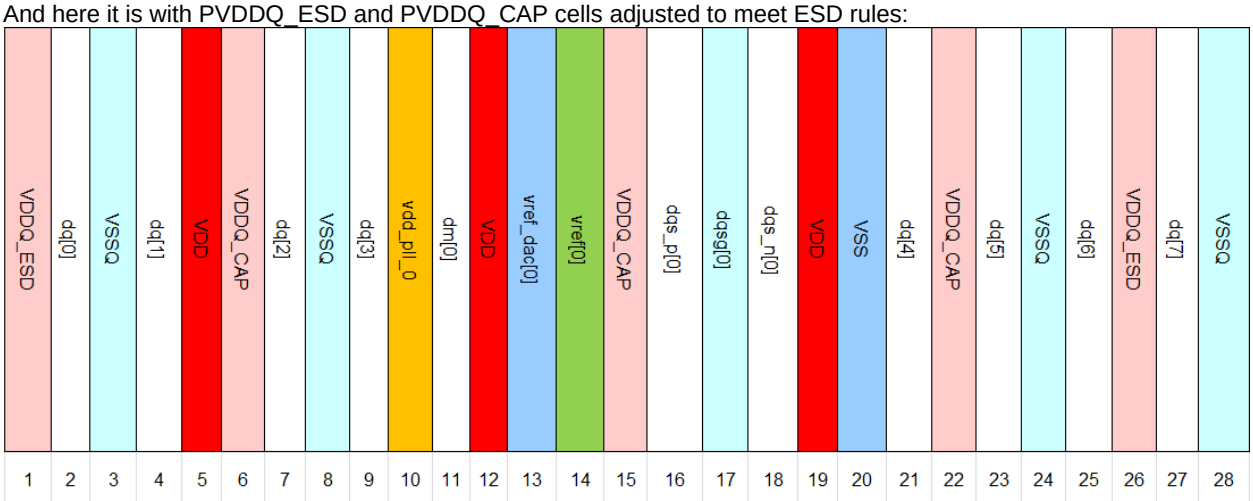
For signal IOs at the end of the IO ring Max cell distance to nearest clamp = 0.5/0.04 = 12.5 or 12 cells away.

For signal IOs in the interior of the IO ring Max cell distance to nearest clamp = 1/0.04 = 25 cells away.

Looking at the example DDR4 flip chip IO ring for data byte lane we have the following cells:



And here it is with PVDDQ_ESD and PVDDQ_CAP cells adjusted to meet ESD rules:



Note we placed VDDQ_ESD cells near the ends of the IO ring segment. Also note that any signal IO cell in the IO ring is within 12 cells of the nearest VDDQ_ESD cell. The rest of the VDDQ cells are VDDQ_CAP to maximize decoupling caps for VDDQ-VSSQ.

The same analysis should be applied to the Address/command lane as well.

2.2.10 VDDQ - VSSQ Decoupling Capacitance

The most effect type of power supply decoupling capacitance for high frequency IO supply noise is on-die decoupling capacitance. The VDDQ-VSSQ IO supply is the noisiest IO supply in the DDR interface. The IO cells of the DDR interface contain a good amount of VDDQ-VSSQ IO supply decoupling capacitance within their structures. Decoupling capacitance for other IO supplies (PVAA_PLL, VDD) are also contained within the IO cells, as well as for VREF reference signal within the IO ring. This is given by the Decoupling Capacitance table in the DC and AC Characteristics section of the SSTL I/O Library section of the databook. Determining an adequate amount of decoupling depends on many factors – DDR interface standard and rate of operation, drive strength and termination schemes, PCB, package, and on die power supply interconnect networks, Signal:power:ground IO cell ratios, decoupling capacitance at PCB, possibly package – but not preferred) and on die.

A methodology for determining adequate amounts of decoupling is described in the "Guidelines for Implementing Signaling Environments for DDRn Interfaces: PCB, Package,Power, and Timing Budgets" Application note document. This method does require that simulations of the power supply interconnect in the frequency domain and time domain are required to give confidence in the desired solution. There are trade offs between the amount of decoupling required and the amount actually available in the layout due to silicon area available for decoupling caps.

A starting point would be to come up with a proposed IO ring based on an assumption of the number of signal:power:ground cells required (a best case of 2:1:1 is a good starting point) in the interface as was done earlier. Once all the cells of the interface are determined taking into account desired functionality, Signal:power:ground ratios, and IO cell ESD, IR drop, and EM limit requirements, an estimate of the amount of decoupling capacitance available can be determined. Usually this can be partitioned in the localized IO cell groups such as byte lane segments and Address/Command lane segments to ease the analysis. This is not a bad assumption as at higher frequencies the IO supply currents will tend to remain localized to the cell locations where are used due to currents following paths of least inductance.

The power integrity analysis is then done with this amount of decoupling to see if it is adequate for AC noise specs of the DDR interface. If it is then the work is done. If not there are snapcaps cells available that can be bolted on to the die edge side of the IO cells to increase the amount of VDD/VSSQ IO supply decoupling capacitance. The snapcaps will be bolted on in rows connecting to all cells of the DDR interface to make the best use of all the area underneath the IO cells for decoupling. There are specific cells for connection to VDDQ cells, VSSQ cells, and all the rest. Multiple rows of snapcaps can be used for more decoupling. The databook gives examples of snapcap usage and decoupling caps per cell.

The power integrity analysis is then done again with the amount of decoupling to see if it is adequate for AC noise specs of the DDR interface.

3 Floorplanning

3.1 General Lane Configuration

Figure 2 provides examples of proper lane floor planning. Consider the Following guidelines

For DDR4 DIMM applications, the user may find easier die / package / PCB routing with the command lane centred in the byte lanes

- In a 72-bit system, 4 or 5 byte lanes placed on each side of the command lane
- Helps minimize clock to pin skew
- Improved matching to the pin out of the SDRAMs
- For high-speed discrete on board memory applications, the user may find easier die / package / PCB routing with the command lane on one end of the interface instead of in the center

The SDRAM Interface is permitted to wrap around a corner

- Complete lane units can be placed on different sides of the IC

For LPDDR3 discrete or DDR3 DIMM applications, the user may find easier die / package / PCB routing with the command lane centred in the byte lanes

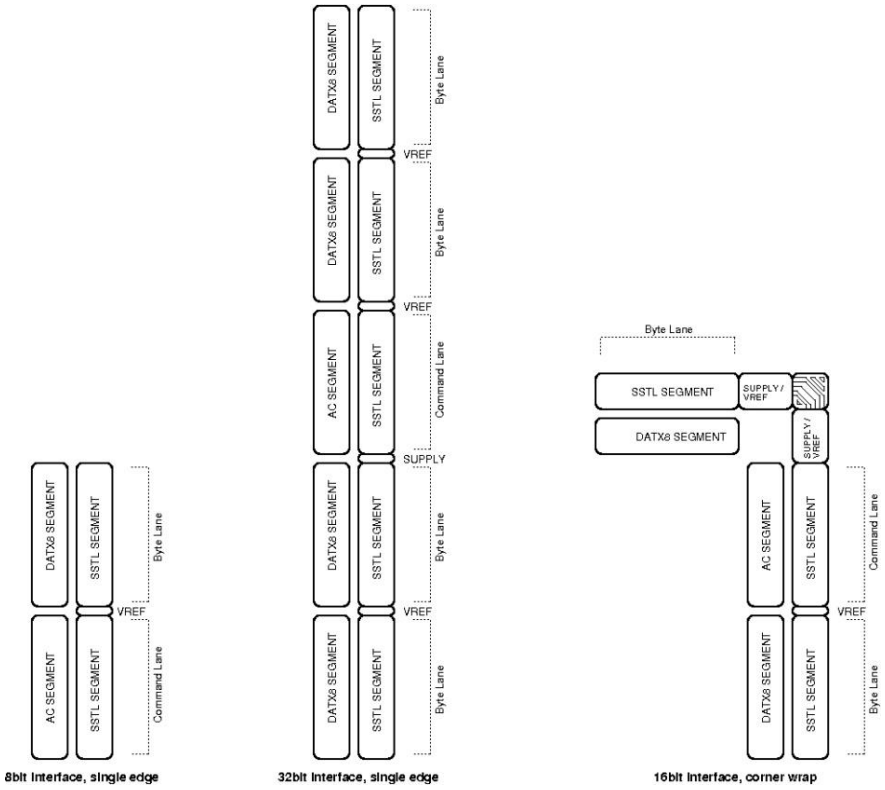
- In a 32-bit system, two byte lanes placed on each side of the command lane
- Helps minimize clock to pin skew
- Improved matching to the pin out of the SDRAMs
- For high-speed LPDDR3 POP applications, the user may find easier die / package / PCB routing with the command lane on one end of the interface instead of in the center

The SDRAM Interface is permitted to wrap around a corner

- Complete lane units can be placed on different sides of the IC

As can be seen from the corner wrap example provided in Figure 2, due to the combined height of the AC and/or DATX8, there is some slot padding required at the corners. It would be possible to place one lane tight to the corner, but not two lanes tight to the same corner.

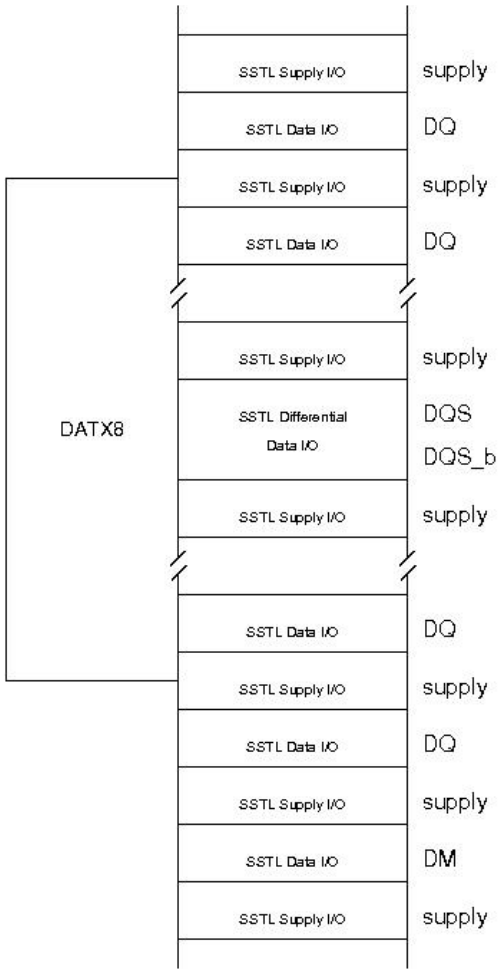
Figure 2: DDR4 multiPHY Floorplanning Examples



3.2 Byte Lane

The DQS/DQS_b signals are effectively the clocks of the byte lane. The goal of byte lane floorplanning is to minimize strobe to data pin skew. Ideally, the DQS/DQS_b strobes should be placed in the center of the lane, as shown in Figure 3, which is fine for applications such as DDR4.

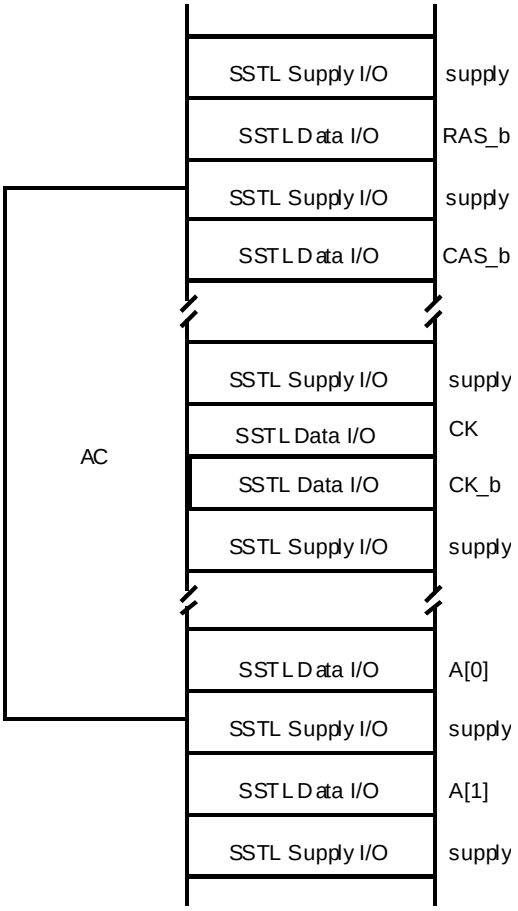
Figure 3: DDR4 Byte Lane Floorplan



3.3 Command Lane

The CK/CK_b signals are the Clocks of the Command lane. The goal of Command lane floorplanning is to minimize Clock to data pin skew. As such, the CK/CK_b clocks should be placed in the center of the Lane, as shown in the following figure. Half of the address/Command slots are then placed on each side of the clock pair.

Figure 4: Command Lane Floorplan

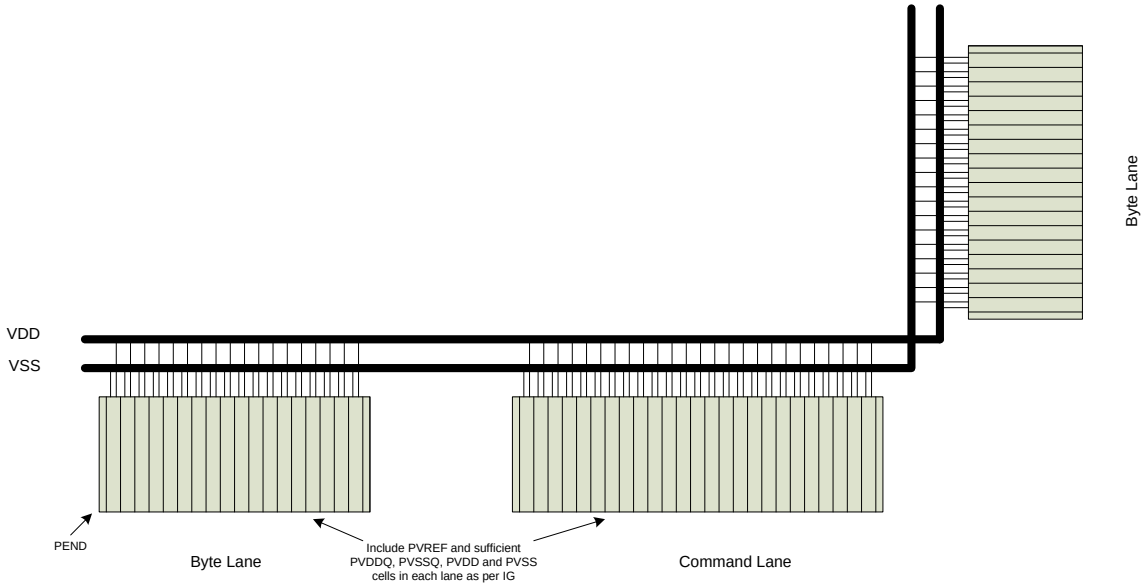


3.4 Isolated Byte Lane and A/C Lane Placement

Traditionally, the SSTL library cells required for a DDRn interface are placed in a continuous peripheral pad frame with the byte lanes and A/C lanes abutted end to end. The extreme ends of the pad frame are terminated using PEND cells. This arrangement is suitable for wire bond designs and for FC design where RDL routing is used to break out to bump pads. There is an alternative SSTL library cell placement method for IO ring design Isolated Lane Placement.

In Isolated Lane Placement, the SSTL library cells for individual lanes are abutted as before, but the lanes no longer have to be abutted to each other. This method allows the lanes to be placed with more freedom – for instance, they can be located in isolated segments in the IO pad frame or embedded into the core logic with gaps between them to allow for routing channels. Such a placement may simplify IO package routing and/or the RDL distribution layout to assist with overall SoC floorplanning, but there are additional concerns which must be addressed carefully as detailed below.

Figure 5: Example Isolated Byte Lane and A/C Lane Placement



Isolated Lanes

There are a number of supply and signal nets that are normally routed throughout the DDRn interface pad frame by abutment. When the isolated lane placement method is used it is possible to omit the continuation of these nets between the isolated islands provided the following rules are followed. This increases the flexibility of the SoC floorplanning.

MVDDQ/MVSSQ: Do not connect the IO power/gnd busses between physically isolated lanes, but ensure each lane has the required number of PVDDQ/PVSSQ cells as defined in the Implementation Guide (IG).

MVDD/MVSS: Do not connect the core power/gnd busses between physically isolated lanes, but ensure each lane has the required number of PVDD/PVSS cells as defined in the IG. Also, it is essential to fully connect all MVDD/MVSS pins on all the SSTL cells to the local core VDD and VSS grid to ensure full SI and CDM performance and minimize interface clock jitter.

MVREF and ZIOH[63:0]: Do not connect these signals between physically isolated lanes. Instead, include a PVREF cell in each lane. All the PVREF cells can be driven by a common off-chip VREF signal. This signal can be routed through 1 package ball and 1 or more FC bumps in a star topology.

LENH (and POCH for D3F libraries): Do not connect these signals between physically isolated lanes. Use a PRETPOCC or PRETPOCX cell in each isolated segment to drive the LENH and POCH signals to a known state.

3.4.1 Termination of Isolated Lanes

The PEND cell should be used to terminate both ends of each isolated lane.

3.4.2 Spacing of Standard Cells from SSTL cells

When the SSTL library cells are embedded into the core of the SoC care must be taken to leave a space between the bottom edge of the SSTL cells and any other cell. The following list describes the spacing rules:

40/45nm and smaller process nodes – 20um spacing

Process nodes larger than 40/45nm – refer to Synopsys

Note: The "bottom edge" is the PAD pin edge of the /IO.This rule does not include periferal I/O usage when the I/O on the edge of the die.

3.5 DQS/DQS_b Connections

DQS/DQS_b differential signals require a PDQSG_VSSQ cell between the PDIFF I/O cells (see Figure 6). The PDQSG_VSSQ cell is required to provide a matched IO path delay (loop back from TX to RX at the pad) for the Read DQS gate signal for Read operations. The DFO/DFI pins are located on both sides of the PDIFF cell, in reverse order such that two PDIFF cells placed beside each other with the same orientation will properly connect by abutment with no external routing required. All other SSTL I/O library cells and PDQSG_VSSQ cell contain a routing void in the area where these pins are located such that when filler or power cells separate the pair of cells, an auto router can automatically connect the DFI/DFO signals without requiring an additional metal layer above the highest metal layer used by the SSTL library.

In some cases (like for DDR3) a pull-down/pull-up is resistor may be required on DQS/DQS_b to assist in Read DQS pre and post amble glitch reduction. This function is implemented in the PDIFF cells and can be enabled via control bits DQSR[3;0] on the PDIFF cell control pins.

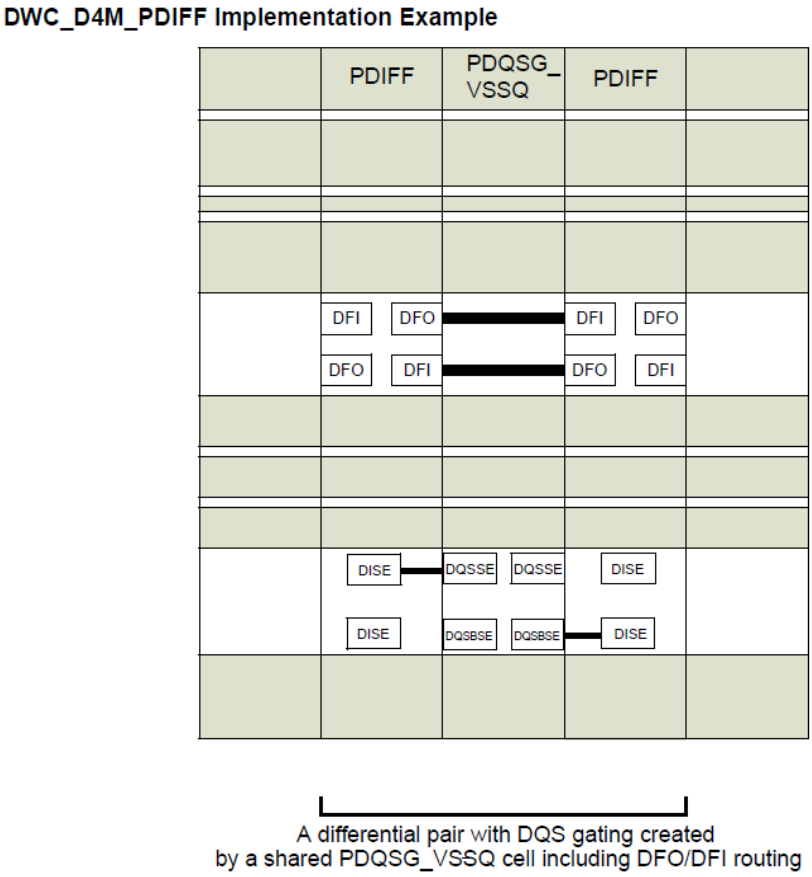
For modes with pull-up termination, like DDR4, a different glitch suppression mechanism is available. In addition to the differential receiver, PDIFF has a single-ended receiver to detect when DQS and DQS_b are high. The output of these single-ended receivers, DISE, must be routed to the DQSSE and DQSBSE inputs in the PDQSG_VSSQ cell. To facilitate these routes, a horizontal channel is provided in every library cell, and these signal pins are on the sides of PDIFF and PDQSG_VSSQ. These signals should be routed just like the DFI/DFO signals. Also note that the signal MVREFSE is an isolated VREF level signal that is used by the single-ended receivers in the PDIFF cells to detect the DQS and

DQS_b high condition. The MVREFSE signal is generated by an independent VREF generator in the PVREF cell and is connected to the PDIFF cells by abutment of all the cells in the data byte lane.

It requires a either manually connection or an auto reouter to connect DFO to DFI, DISE to DQSSE and DISE to DQSBSE as shown in Figure 6.

Please refer to the SSTL I/O chapter in the DWC DDR4 multiPHY Databook for additional information on the PDIFF and PDQSG_VSSQ cells.

Figure 6: PDIFF/PDQSG_VSSQ Connection



3.6 PDRH18 Connections

PDRH18 is an input signal on all signal IO cells and is generated by PVREF cells. PDRH18 is asserted high when the power net MVAA_PLL is powered up and MVDDQ is powered down. Such a condition can occur when the DDR interface is placed into a CKE retention mode whereby the SDRAM is kept in self refresh mode by IO signals in the CKE retention island. IO cells outside the CKE retention island can have their MVDDQ supply powered down to save power, however, it might be possible that the MVAA_PLL supply is still powered up. So to save more power on IO receiver circuits (that are supplied by MVAA_PLL), they are put into a power down state when PDRH18 is high. It may also be possible that MVAA_PLL power supply could be powered down in CKE retention mode to also save on IO receive power but keep in mind that PLL circuits are also powered by MVAA_PLL and may require a certain time to ramp up to lock state when MVAA_PLL is reapplied

3.7 PLL Power Routing

The PLL shares the core VSS connection and core VDD connections with the chip logic core VSS and VDD, respectively. Dedicated VSS and VDD slots for the PLL are not required. The PLL requires a dedicated analog power supply pin (pll_vdd). pll_vdd is supplied by using PVAA_PLL IO cells.

Note: All PLL_VDD,VDD and VSS pins on the PLL are required to be connected to pll_vdd rail and core PG grid

The PLL is verified to operate with 10% voltage drop from nominal pll_vdd. Assuming an external board supply of ±5%, this leaves 5% for package and die. Assuming a negligible package drop, this leaves 5% for the die. Permitting a simultaneous rise in VSS and a drop in pll_vdd/ (worst case assumption) leaves 2.5% maximum IR drop for the pll_vdd supply to the PLL. Table 13: shows example calculations to determine the PLL power routing requirements. Designers should use this as an example only and perform their own calculation for their design based on their design parameters, the latest available foundry process information, and the power specifications in the PHY data book.

Note: The 1.8V information is similar to the information in Table 13: but is currently TBD.

Table 13:PLL Routing Requirements with Respect to 2.5V supply

Item	DDR3PHYAC		DDR3PHYDATX8	
	PLL 2.5V Power	**PLL 2.5V Ground**	**PLL 2.5V Power**	**PLL 2.5V Ground**
VDD nominal	2.5V	2.5V	2.5V	2.5V
2.5% VDD	62.5mV	62.5mV	62.5mV	62.5mV
Estimated PLL current consumption (1600Mbps)	28.6mW / 2.75V = 10.4mA	28.6mW / 2.75V = 10.4mA	28.6mW / 2.75V = 10.4mA	28.6mW / 2.75V = 10.4mA
Maximum supply impedance to PLL	62.5mV / 10.4mA = 6.0 Ω	62.5mV / 10.4mA = 6.0 Ω	62.5mV / 10.4mA = 6.0 Ω	62.5mV / 10.4mA = 6.0 Ω
Estimated impedance of power supply slot & bond pad[1]	0.36Ω	0.36Ω	0.36Ω	0.36Ω
Maximum impedance of connection from supply slot to PLL	(6 – 0.36) = 5.6Ω	(6 – 0.36) = 5.6Ω	(6 – 0.36) = 5.6Ω	(6 – 0.36) = 5.6Ω
Estimated distance of PLL power supply pin	150um	150um	50um	50um
Assumed metal sheet resistance	0.119 Ω sq	0.119 Ω sq	0.119 Ω sq	0.119 Ω sq
Required minimum equivalent metal width from supply slot to PLL	(150um x Ω sq) /5.6 Ω = 3.2 um	(150um x Ω sq) /5.6Ω = 3.2 um	(50um x Ω sq) /5.6Ω = 1.1 um	(50um x Ω sq) /5.6Ω = 1.1 um

Notes:

1. Assuming wire bond design.
2. This example applies to a 2.5V pll power supply, other ports may use a 1.8V, or 1.5V supply.

Table 13: indicates the minimum power routing equivalent widths when using a metal layer with sheet resistance of 0.119 Ohm/sq. It is highly recommended to implement PLL power routing wider than shown above to further reduce the supply IR drops. In order to meet the assumption of negligible package drop and to avoid supply coupling, each dedicated pll_vdd supply pad should be routed separately to the closest pll_vdd plane. If there is no pll_vdd plane in the package substrate, separate package pins should be used for each pll_vdd supply.

3.8 General Routing Guidelines

The following are general routing guidelines for the AC and DATX8.

Note: All AC/DX VDD and VSS connections pins are required to be connected to core PG grid

For details, refer to Figure 7 and **Error! Reference source not found.** for pin locations and metal layers (power is only in M5)

Five (all thin) metals are used inside the AC and DX for all routing. In both macros,

- M5 is used exclusively for power routing.
- M1-M4 are used for signal and power routing.

Core power/ground pins are accessible in M5 rails and straps that run both vertical and horizontal allowing access to power connections from any direction. .In other words, power must be connected from above (M6+) down to M5. .It is strongly recommended that every available M5 supply rail pin across each of the PHY macros be connected in this way.

- The ring widths are 4.5um wide, therefore, many connections into the ring are recommended.

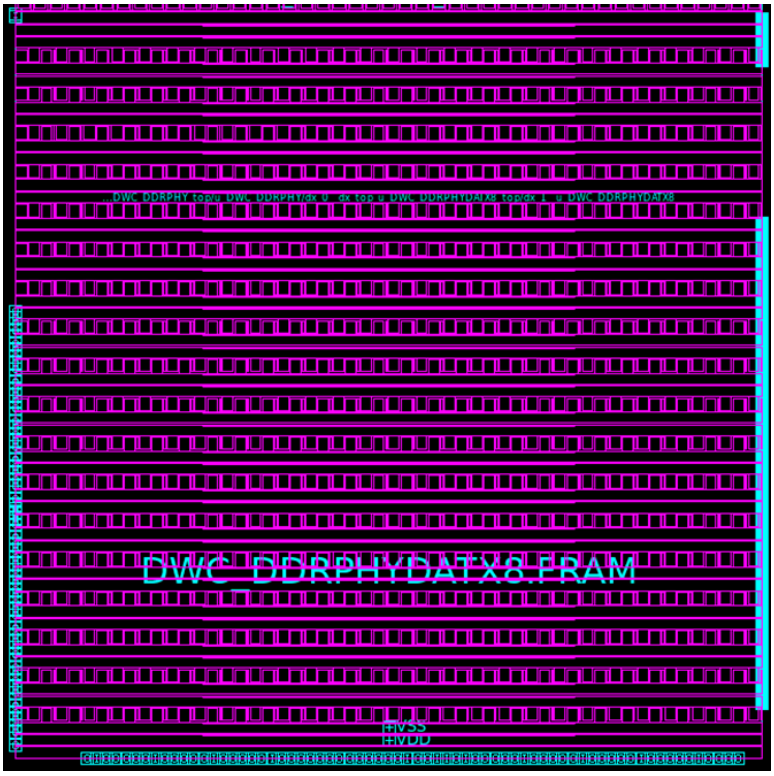
Signal pins are on the boundaries of the PHY and they are 0.1um wide.

All input pins have an antenna diodes attached to them near the PHY boundary.

This example shows vertical M5 PG pins. The orientation of the M5 PG pins is dependent on the metallization rules of the process and customers should verify the metal orientation in the DDR4 multiPHY Databook.

Note: DATX8 and AC macros have similar power pins.

Figure 7: Example Power Pins



3.9 Cell Rotation and Flipping Considerations

In general, there are no restrictions to rotating or flipping any cell in the Synopsys DDR4 MULTIPHY IP (PHYAC, PHYDATX8, and SSTL library cells). However, there are some rules and guidelines that should be followed to make SoC layout as smooth as possible:

Designs in orientation sensitive processes must follow the rules contained in Section 3.9
It is good practice to rotate SSTL library cells rather than flipping them in order to place them on all four sides of a die.

3.9.1 Exceptions to the No-flip Recommendation

There are a few SSTL library cells which must be flipped. These cells are used at both ends of a segment or sub-segment of SSTL cells. As delivered, they can be placed at the right hand end, but must be flipped about their vertical axis in order to be placed at the left hand end:

D3x_PEND: Used to define both ends of a DDR interface segment
D3x_PSCAP_END: Used to define both ends of a row of PSCAP_xxx cells
D3x_PPADCWxx_END: Used to define both ends of a segment of PPCADCWxx_xxx bond pads
D3F_PFILL5_ISO: Used to define both ends of a VDDQ retention island when using the CKE retention mode. It only requires to be flipped for use at the left hand end in the D3F SSTL library.

3.10 Floorplanning Considerations for Gate Orientation Sensitive Processes

3.10.1 Introduction

At 32nm process nodes and below, many foundries require, or strongly recommend, that the gates of core voltage devices be oriented in only one direction. In such cases, the Synopsys DDR4 MULTIPHY hard IP is designed to allow this requirement to be followed regardless of which die edge is used for the DDR PHY interface. This section explains how the user must select and orient the PHY, PLL and I/O cells depending on the die side to which they are adjacent.

3.10.2 Overview

Synopsys DDR PHY IP for gate orientation sensitive processes is designed assuming the SoC will be laid out with the core poly gates orientated vertically. If the user wishes to orient the core poly gates horizontally in the layout then they must apply a 90 degree rotation to each hard IP macro before using the following guidelines.

Each hard IP macro uses a single core voltage gate orientation. With the exception of the _EW I/O cells they are delivered with the core gates orientated vertically. The user must follow strict rules to maintain the correct gate orientation while minimizing the routing distance between the PHY macros and the I/O cells.

The user should consult the DDR PHY databook for the process node they are using to establish if the PHY macros and/or the IO cells are orientation sensitive. Note that it is possible for the PHY macros to be orientation sensitive while the IO cells are not. This is due to the fact that the foundry orientation rules only apply to core gates below a certain length. It is only necessary to follow the orientation rules contained in this section for the macros or cells that are noted as orientation sensitive in the appropriate DDR PHY databook.

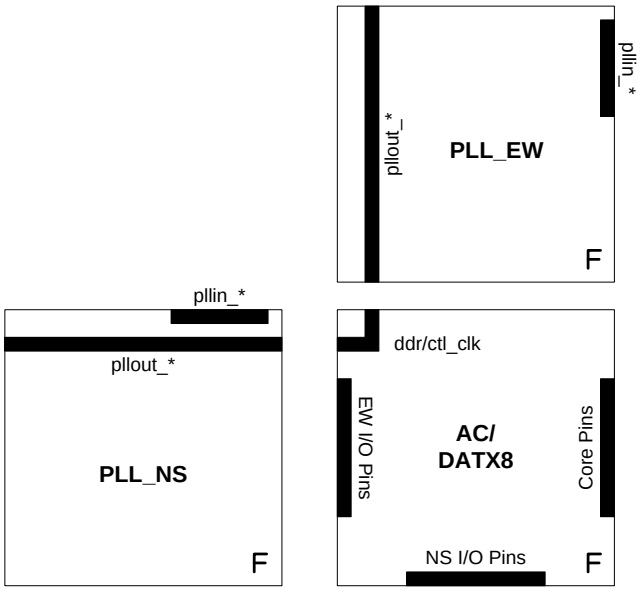
3.10.3 PHYPLL, PHYAC and PHYDATX8 Macros

Only one instance of each of the PHYAC and PHYDATX8 macros is provided but they have duplicate pins for signals to the I/O cells on two sides – standard pins are on the south side and alternative pins (named with a _e suffix) are on the east side. The user should use the PHY pins located closest to the die edge being used for the interface lane I/O cells. The unused pin of these two available pin locations is normally required to be fixed to a specific state (refer to the PHY databook for further information).

The PLL macro has two cells, one for use on the south or north side of the die (PLL_NS), and the other for use on the east or west side of the die (PLL_EW). The PLL always connects to the AC or DATX8 macro by abutment.

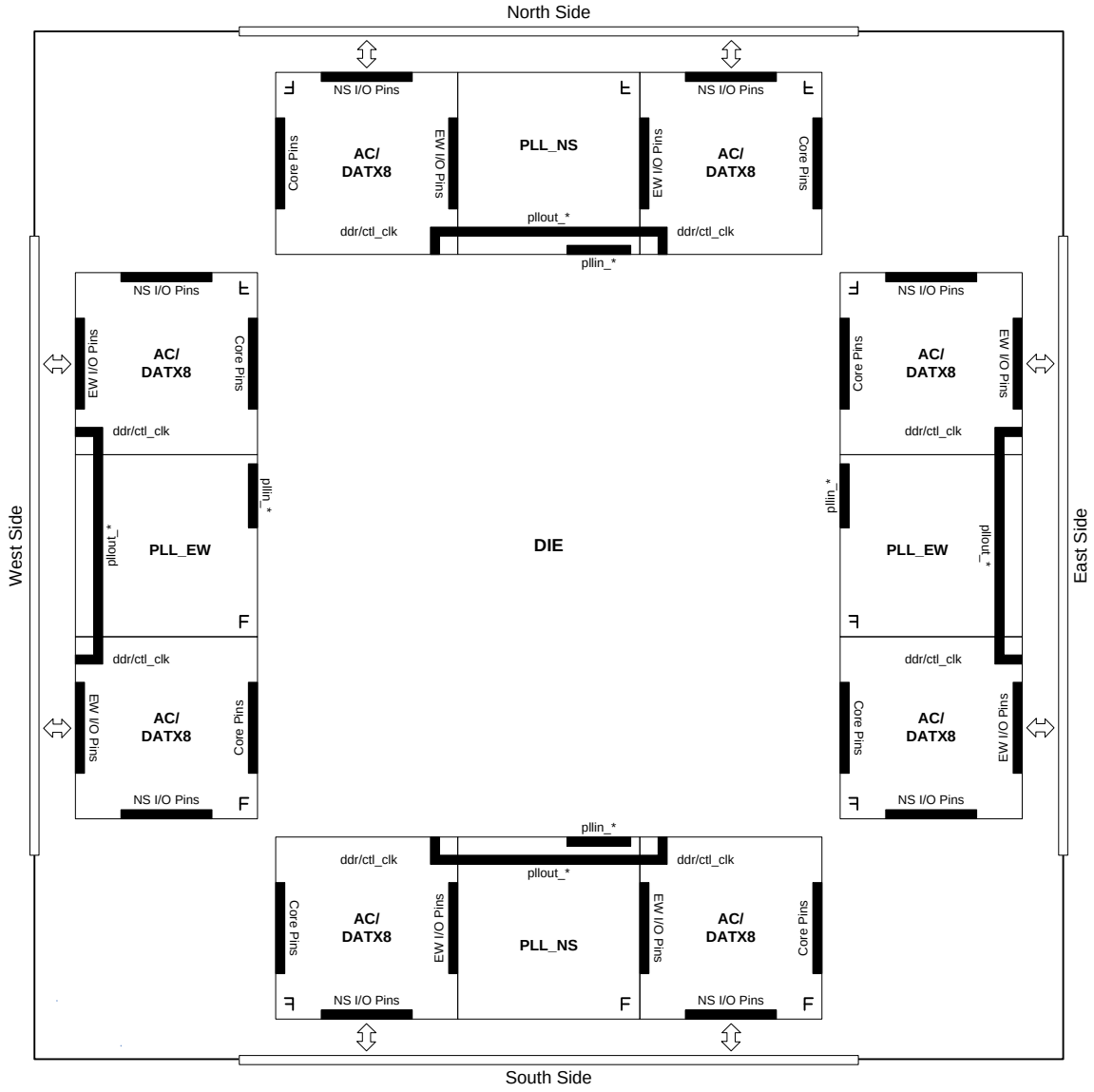
Figure 8 shows the macros and the position of the different groups of pins. The PLL pllin_* pins are the input (pllin_x1 and pllin_x4x2) clocks of the PLL and connect to the core. The PLL pllout_* pins are the output (pllout_x1 and pllout_x4x2) clocks of the PLL and connect by abutment to the AC or DATX8 input (ctl_clk and ddr_clk) clocks. The core pins on the AC and DATX8 connect to the core (PUB) signals. The NS I/O pins on AC and DATX8 are used to connect to the I/Os for SDRAM signals on the north or south side of the die. Similarly, the EW I/O pins on AC and DATX8 are used to connect to the I/Os for SDRAM signals on the east or west side of the die

Figure 8: PHYPLL, PHYAC, and PHYDATX8 Pin Position



All the three macros can only be flipped on the vertical or the horizontal axis depending on the side of the die that they are to be used. The macros must never be rotated. Figure 9 shows all the valid flipping and abuttment depending on which the side of the die the macros are used. The letter **F** inside the macro indicates the type of flipping required. Note that the diagram shows the cases where the PLL is shared between two macros. If the PLL is not shared, then it only needs to abut to the macro that is used for that PLL.

Figure 9: PHYPLL, PHYAC, and PHYDATX8 Flipping and Abutment



3.10.4 I/O Cells

Since the DDR4 MULTIPHY I/O library is designed to be used in a peripheral ring, the I/O cells are normally rotated 0, 90, 180, or 270 degrees (as required) so that their pad pin is adjacent to die edge and their long edges abut. A subset of the I/O cells contain core voltage devices, so, for orientation sensitive processes, there now has to be two versions of these cells. One version has the cell name suffix _NS: it is delivered with its core poly gates orientated vertically and should only be used on the north or south side of the layout. The other version has the cell name suffix _EW: it is delivered with its core poly gates oriented horizontally and should only be used on the east or west side of the layout. I/O cells whose names don't have the _NS or _EW suffix can be used on any side of the die. Note that utility I/O cells such as bond pads, SnapCaps, corner cells and fillers are not orientation sensitive. Be aware that the AC performance of a _NS cell can differ slightly from its _EW version. Separate .lib files are supplied for each version so that the user's timing simulations will reflect any difference.

In some Synopsys DDR PHY IP products there is a "No Flip" rule applied to the I/O library cells. While this is not required for the DDR4 MULTIPHY IP products, it is prudent for users to apply this rule at all times so that they can move seamlessly between DDR3/2, DDR2/3-lite, DDR2/3-L/mDDR, and DDR MultiPHY products.

The rules for using the _NS and _EW I/O cells are as follows:

_NS: use as delivered for the south side or rotate 180 degrees for use on the north side

_EW: use rotated 90 degrees for the east side or rotate 270 degrees for use on the west side

3.10.4.1 Exceptions

There are some exceptions to the "No Flip" rule to avoid the need for unnecessary additional cells. For example, the PEND cell (and PFILL5_ISO cell, when it exists) have to be flipped so they can correctly terminate either end of a DDR I/O segment or VDDQ retention island respectively.

3.11 Floorplanning Considerations for the PUB

When floorplanning for the PUB, the key constraint is to make sure that there is enough area to hold the PUB's logic. Once the required area is confirmed, a standard timing-driven placement tool can be used to place most of the logic automatically within that area. Refer to the the DDR4 PUB Databook for area information.

Note: A module-by-module regioning within the PUB is not recommended.

3.11.1 Placement Rule Exception with the PUB

There is an exception to the placement rules for the PUB: the pipeline flops created by the `DWC_DFI_IN_PIPE and `DWC_DFI_OUT_PIPE should be placed between the main PUB area and the AC/ DATX8 macros that the flops communicate with.

Ideally, the flops should be placed freely by a timing-driven placement, allowing them to be put anywhere across the entire PHY/PUB region. However, if this is not possible, the flops can be placed approximately midway between the PUB area and the AC/ DATX8 they connect to. Depending on STA results, the flops may require manual adjustment in either direction.

The following flops fall into this category:

u_DWC_ddr3phy_dfi/ac_ctl/ctl_*_px*[2]*

u_DWC_ddr3phy_dfi/dx_ctl/O_ctl_*

u_DWC_ddr3phy_dfi/dx_ctl/dq_rtt_en*

ctl_qs_gate_wl_mode*[n:0]

in_dfi_lp_req*

u_DWC_ddr3phy_dfi/dx_ctl/dx_rd_*_u_dx_rd/in_bl_dx_phy_q*

sdr_dfi_rddata_valid_* (when SDR-ONLY or HDR_SDR mode)

sdr_dfi_rddata_* (when SDR-ONLY or HDR_SDR mode)

dfi_rddata_valid_* (when HDR-ONLY or HDR_SDR mode)

dfi_rddata_* (when HDR-ONLY or HDR_SDR mode)

Note: All names are pseudo-coded and are relative to DWC_ddrphy_pub.v. Exact names depend on synthesis tool and tool settings:

4 ESD Protection Scheme

4.1 Overview

Synopsys' IP is protected from ESD events that could potentially occur on any pin of a package. Three ESD test models encapsulate various environments in which an ESD event could occur and through proper design strategy, be sufficiently protected against damage. The Human-Body Model (HBM), Machine Model (MM), and Charge-Device Model (CDM) are considered and proven through silicon test vehicles.

4.2 Important Considerations

To ensure that ICs designed using the I/O pad cells in this library have low risk of ESD failure due to ESD discharges, the following points should be considered:

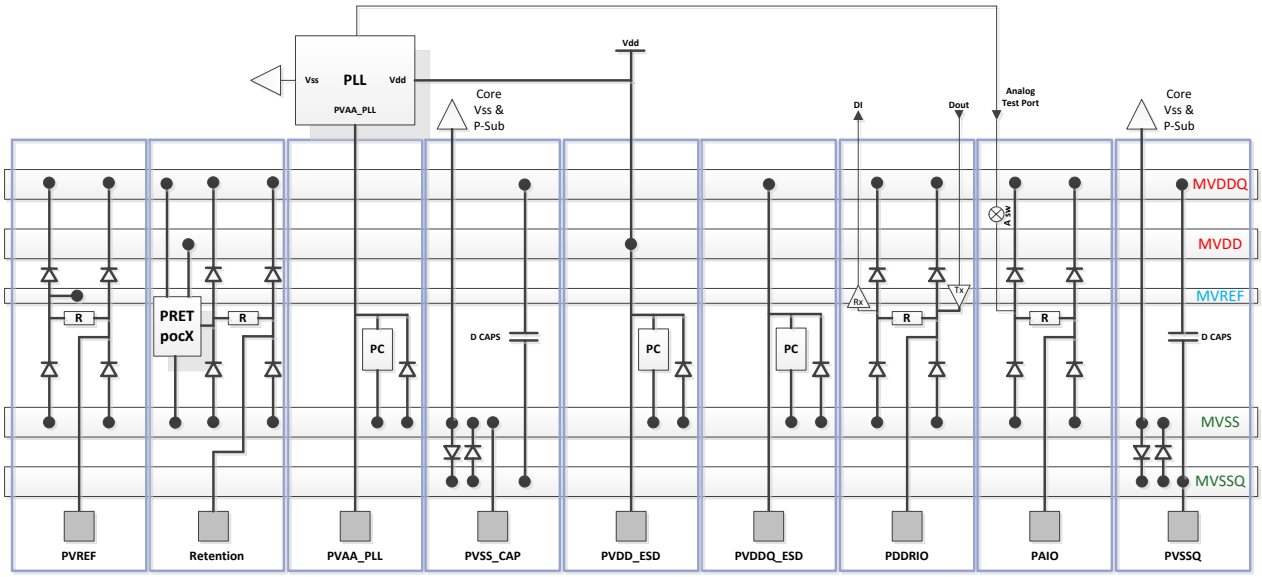
1. All possible paths for ESD discharges of either polarity between any external pin (ESD arcs) need to be considered in the design. Careful attention must be given to a balanced configuration for I/O pad cell placement. The goal is to achieve uniform ESD performance throughout the I/O ring.
2. Ideally, the power supply rails in the I/O ring will not be broken. However, this is sometimes unavoidable and separate segments of I/O ring are created where one or more supply rings are broken. In this case all possible ESD arcs must be considered.
3. The ESD protection scheme in this library assumes MVSS will be continuously connected throughout the entire I/O ring. This ensures all possible ESD arcs are covered when other I/O supply rings are broken. Breaking supply rings must be done with the special breaker pad cells included in this library. Note that the breaker pad cells do not contain ESD elements. They simply maintain the integrity of the remaining bus structures in the I/O ring while breaking specific I/O ring signals.
4. Breaking the MVSS I/O ring is strongly discouraged. If this is done, ESD discharges between I/O cells on either side of the break will almost certainly result in ESD failure. In some packages (for example, BGA), the MVSS pins will be tied together off-chip. In this case, the package will complete the MVSS path and ESD may be good in packaged parts even with a MVSS break on-chip. Care must be taken to ensure the series resistance of the chip connections (bondwire + package + PCB trace) is taken into account. Following the ESD guidelines listed in Section 4.7 ESD Guidelines will ensure that the complete design is acceptably robust.
5. The type of package used may also affect ESD performance. The energy spectrum for HBM and MM discharges is low (below about 2.1MHz and 12MHz respectively). This means that ground plane capacitance in BGA style packages may absorb some energy from ESD discharges. In addition, separate power domains may be rejoined in the package (for example in many BGA, PGA, and MCM packages). As a result, ESD robustness of some packaged devices may be substantially higher than that of bare die or other less robust packages.
6. CDM discharges are a more complex phenomenon. Most of the energy of these discharges is near the resonant frequency of the package (including on-chip capacitances). This type of discharge most often occurs on corner pins/bumps on packages. CDM robustness can be improved by ensuring these corner pins are power supplies connected to large on-chip capacitances. For example, PAIO, PDDRIO, PDIFF, PRETPOCX, PVREF and PZQ I/O pad cells include secondary ESD protection devices designed to absorb typical CDM discharges.
7. The MVSS rail in this I/O pad library connects directly to the chip substrate (P-sub) through a large number of contacts spread throughout the I/O ring. The core of the chip also connects its ground rail (VSS) to the same substrate. For uncompromised CDM robustness it is highly recommended that the I/O ring MVSS rail be integrated with the core VSS rail through redundant strapping. The ground connections can be made from MVSS ports on the core-side of each I/O pad cell in the I/O ring.

9. On-chip, the I/O ground rail (MVSSQ) has no connections to the chip substrate and is DC isolated from the MVSS ground. Anti-parallel diodes built into the PVSSQ and PVSS ground pad cells provide mutual clamping between the separate ground domains, limiting voltage differences to approximately 1V. The anti-parallel diodes are especially important for bare die, providing a safeguard against CDM damage. Note that, the I/O and core logic grounds are usually bonded to a common ground plane in the package and/or PCB, essentially shunting the anti-parallel diodes.
10. Separate core supply domains (MVDD/VDD) for devices in the I/O ring and interfacing devices in the chip core are not recommended. Thin oxide gates connected across core power domains are extremely susceptible to CDM damage. To ensure CDM robustness in the design, it is highly recommended that the I/O ring MVDD rail be integrated with the interfacing core logic VDD rail through redundant strapping. The core supply connections can be made from MVDD ports on the core-side of each I/O pad cell in the I/O ring.

4.3 ESD Constellation

The following information is provided to further understanding of the ESD scheme in this library. Figure 10 illustrates a complete DDR interface ESD constellation with PVREF, PRETPOC, PDDRIO, PAI/O and complete set of power and ground pad cells. The ESD Clamps are contained within the power cells. Corner cells containing only decoupling capacitance are not represented.

Figure 10: ESD Constellation



4.3.1 Pad Cell Details

The following pad cell definitions reference the pad cell circuit functions depicted in the ESD Constellation diagram (see Figure 10).

4.3.1.1 PVSS_CAP

The PVSS_CAP core ground cell connects external ground to the internal MVSS ground rail. Anti-parallel ESD diodes within the cell provide mutual clamping for the separate MVSS and MVSSQ ground domains. The remainder of the cell contains I/O decoupling capacitance. Decoupling capacitors are connected between the MVDDQ and MVSSQ abutment rails passing through the cell.

4.3.1.2 PVSSQ

The PVSSQ I/O ground cell connects external ground to the internal MVSSQ ground rail. The PVSSQ I/O ground pad cell is identical to the PVSS pad cell except for the pad connection.

4.3.1.3 PVDD_ESD

The PVDD_ESD core power pad cell connects external VDD to the internal MVDD supply rail. Core supply ESD protection is provided by a built-in ESD clamp circuit and ground clamp diode.

4.3.1.4 PVDDQ_ESD

The PVDDQ_ESD I/O power pad cell connects external VDDQ to the internal MVDDQ supply rail. I/O supply ESD protection is provided by a built-in ESD clamp circuit and ground clamp diode. The principle function of the MVDDQ rail clamp is to protect I/O signal pad cells via the primary ESD diodes built into them.

4.3.1.5 PVDDQ_CAP

The PVDDQ_CAP I/O power pad cell connects external VDDQ to the internal MVDDQ supply rail. The PVDDQ_CAP power pad cell has no built-in ESD clamp circuit. This version of the I/O power cell contains only I/O decoupling capacitance. The decoupling capacitors are connected between the MVDDQ and MVSSQ abutment rails passing through the cell.

4.3.1.6 PVAA

The PVAA power cell is an isolated analog supply containing a core supply ESD clamp and a reverse biased ESD diode to MVSS. This pad cell is identical to the PVDD pad cell except that it does not connect to the MVDD core power rails.

4.3.1.7 PVAA_PLL

The PVAA_PLL power cell is an isolated analog supply containing a PLL supply ESD clamp and a reverse biased ESD diode to MVSS. This pad cell is identical to the PVDDQ pad cell except that it does not connect to the MVDDQ I/O power rails.

4.3.1.8 I/O Signal Cells

All I/O signal cells contain reverse biased ESD diodes to MVSS and MVDDQ. ESD protection is provided, remotely, by the ESD clamps built into the PVDDQ_ESD I/O power pad cells that are distributed throughout the I/O ring. During an ESD event the ESD clamps short the MVDDQ rail to ground to discharge the I/O pad via the primary diode.

4.3.1.9 PVAA18

The PVAA power cell is an isolated analog supply containing an ESD clamp (between VAA18 and MVSS) and a reverse biased ESD diode to MVSS. This pad cell is similar to the PVAA cell except that it has an ESD clamp suitable for IO ring voltages (up to 1.8V nominal) instead being limited to normal core voltage levels.

4.3.1.10 PVDD_CAP

The PVDD_CAP I/O power pad cell connects external VDD to the internal MVDD supply rail. The PVDD_CAP power pad cell has no built-in ESD clamp circuit. This version of the core power cell contains only I/O decoupling capacitance, instead of a clamp. The decoupling capacitors are connected between the MVDDQ and MVSSQ abutment rails passing through the cell.

4.3.1.11 PVSS_ESD

The PVSS core ground cell connects external ground to the internal MVSS ground rail. Anti-parallel ESD diodes within the cell provide mutual clamping for the separate MVSS and MVSSQ ground domains. The cell also includes a supply clamp between MVDDQ and MVSS.

4.3.1.12 PVSSZB

The PVSSZB cell is used to break the impedance control bus (ZIOH). It also provides a core ground connection bewteen external ground and the internal MVSS ground rail. It contains the same anti-parrallel ESD diodes and MVDDQ-MVSSQ decoupling capacitors as the PVSS_CAP cell.

4.3.1.13 PVSSZB_ZQ

The PVSSZB cell is used to break both the impedance control bus (ZIOH) and the input reference voltage bus (MVREF). It also provides a core ground connection bewteen external ground and the internal MVSS ground rail. It contains the same anti-parrallel ESD diodes and MVDDQ-MVSSQ decoupling capacitors as the PVSS_CAP cell.

4.4 HBM and MM Immunity

The SSTL Library uses active, RC triggered, voltage level maintenance ESD rail clamps and steering diodes in the signal I/Os to provide immunity to HBM and MM ESD events. The clamps are located in the power pad cells and the steering diodes are located in the signal and ground pad cells.

Depending on the polarity of the ESD event, and which pin types it occurs across, one of the the following events can occur:

1. The ESD event will be steered onto the power rail, causing the trigger circuit to fire and short the power rail to the core ground rail (MVSS)
2. The ESD event will be steered directly to the core ground rail (MVSS)

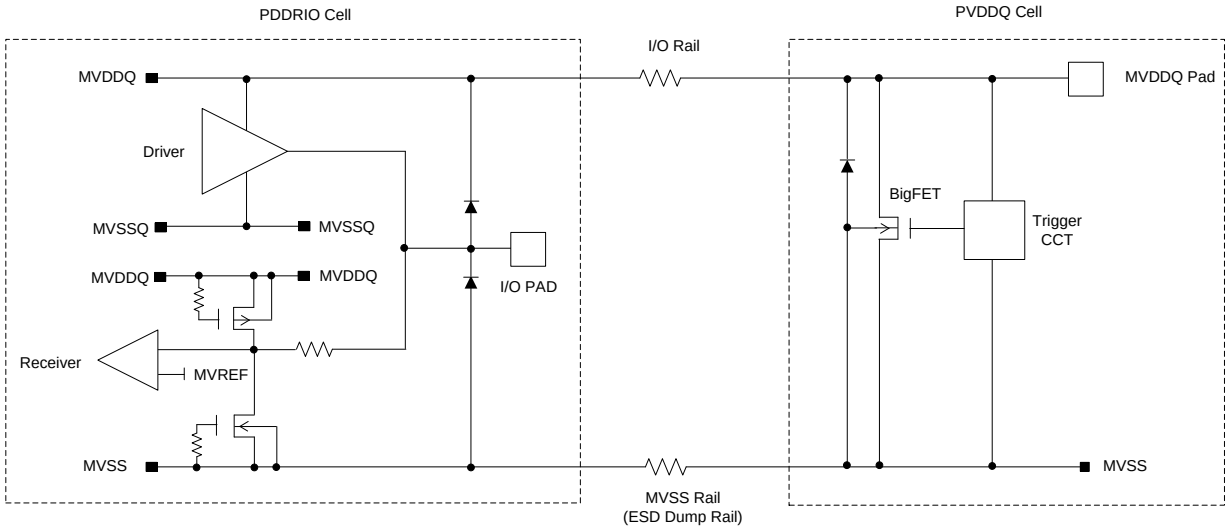
The clamp circuits for each power rail are customized to protect the following relevant devices:

1. VDD, VAA: Gate voltage applied to core devices less than 4V (thin-oxide devices)
2. VDDQ, VAA_PLL: Gate voltage applied to I/O devices less than 8V (thick-oxide devices)
3. Spikes of gate voltage (1 and 2) of short duration (<300ns) are allowed

Note: The primary discharge rail for ESD events is MVSS (core ground).

Figure 11 illustrates the I/O ESD protection scheme using remote ESD clamps. The effectiveness of this ESD protection scheme depends largely on power rail and ground rail resistances. For more information, refer to Sections 4.5 CDM Immunity and 4.6 ESD Discharge Resistance.

Figure 11: A typical I/O pad shown with remote MVDDQ rail clamp



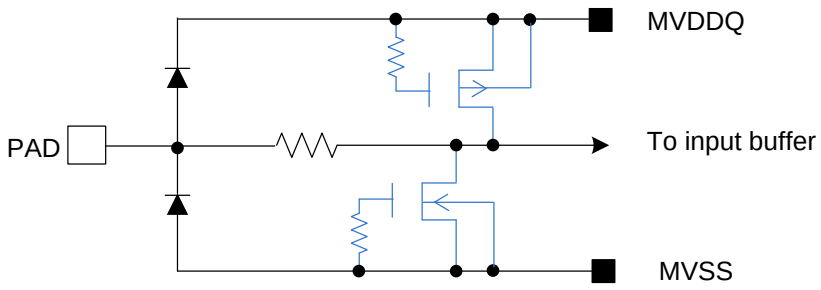
4.5 CDM Immunity

Unlike HBM or MM which replicates the static electrical discharge from a human body or machine through the device to ground, the CDM test model simulates the static discharging that occurs in production equipment and handling. Fundamentally, the static charge builds up on the package or lead frame which may discharge through a pin and travels through a path to ground causing damage along the way. CDM events typically cause gate dielectric breakdown in unprotected mosfets. The amount of charge that can build up is a function of the parasitic capacitance (and impedance) of the device body or package. The body capacitance for standard small packages is 6.8pF and for standard large packages is 55pF. The test that is performed relies on the package being charged up to the test voltage by field induction and then discharged through various pins to ground. Peak current flowing will be proportional to the body capacitance and the test voltage. The 500V JEDEC compliant CDM ESD spec relies on an RLC model that discharges the body capacitance through an arc resistance of 20 ohms, at the package pin, into a series inductance of 5nH to ground. For standard small packages (6.8pF), peak CDM currents of 5.75A +/-15% will flow from the test pins to ground during discharge. For standard large packages (55pF), peak CDM currents of 11.5A +/-15% will flow from the test pins to ground during discharge. JEDEC JESD22-C101 defines the 500V CDM current pulse waveform as having a rise time of less than 400ps and a pulse width of 1ns +/- 0.5ns, at the midpoint of the pulse.

Depending on design, CDM ESD protection circuits can also provide secondary protection for HBM and MM events. Figure 12 shows secondary power rail clamping is provided by the bulk diodes of the P and N mosfets which are wired in a grounded-gate configuration for CDM protection.

Figure 12 shows the protection used for an I/O pad to input buffers.

Figure 12: Avalanche Transistors providing CDM protection for inputs (highlighted in blue).



4.5.1 ESD Paths

The following figures provide some examples of ESD discharge paths.

Figure 13: Current path in a negative ESD strike

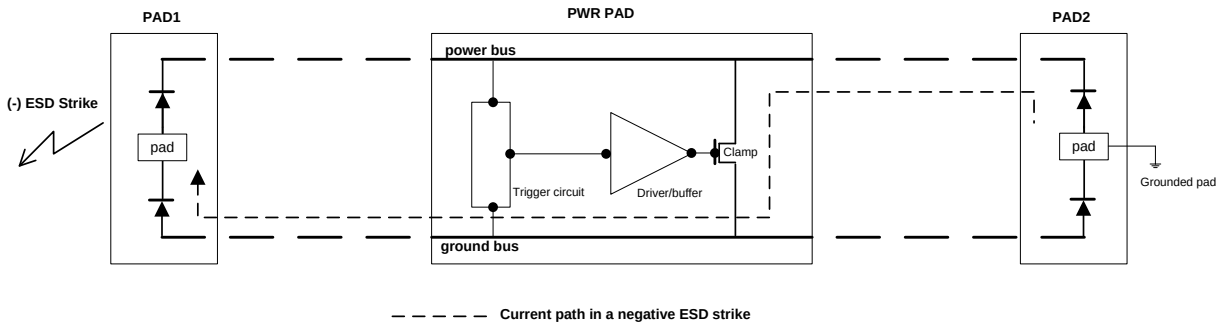


Figure 14: Current path in a positive ESD strike

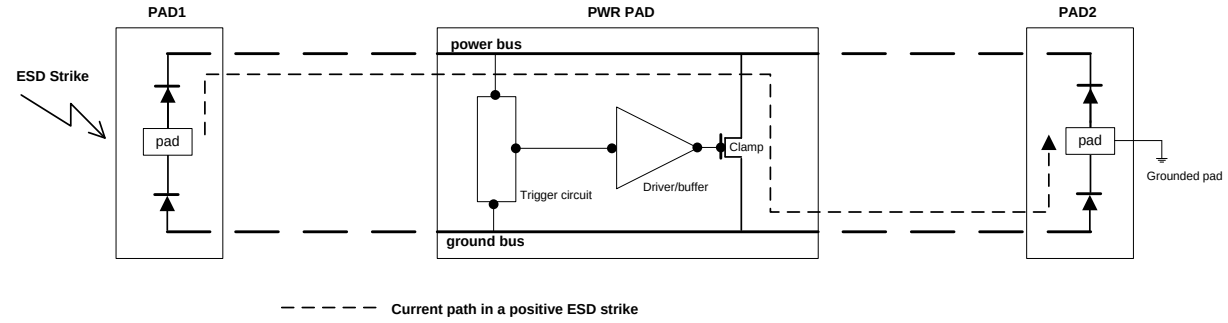
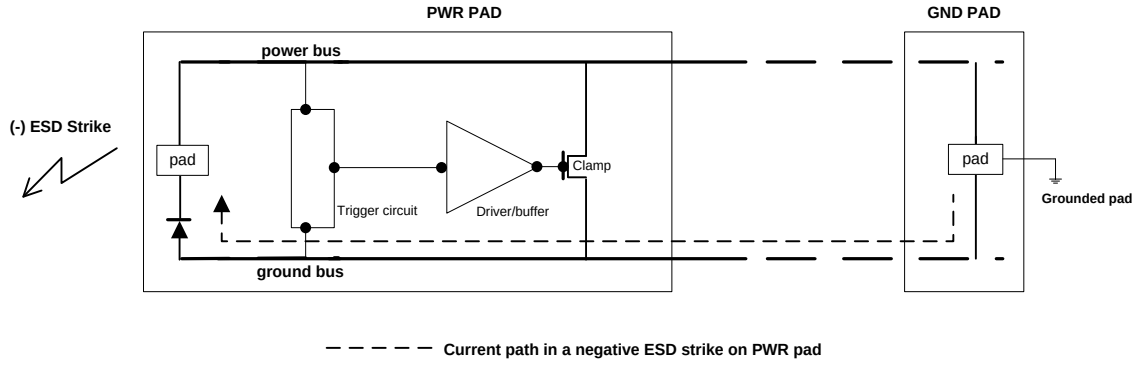


Figure 15: Current path in a negative ESD strike on a power pad



A positive ESD event between a power pad and ground (MVSS or MVSSQ) is clamped locally at the pad. There is no need to add anti-parallel ESD diodes to other power rails at the die level provided MVSS is the common ESD discharge rail.

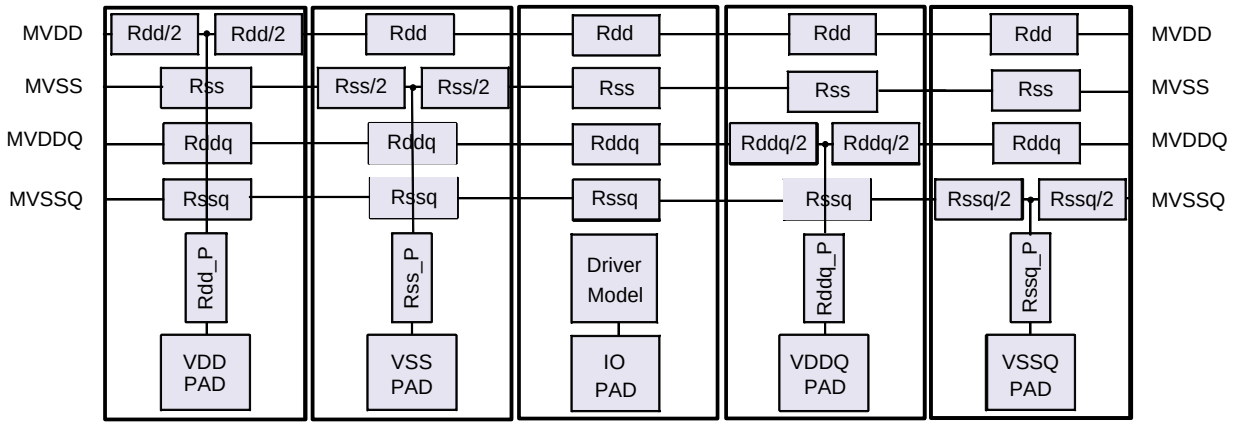
4.6 ESD Discharge Resistance

The ESD scheme in this library relies on two kinds of ESD clamps: Core VDD clamps and I/O VDDQ clamps. Signal I/O cells use clamping diodes to pass ESD discharges to the MVSS, MVDD or MVDDQ I/O ring and the ESD clamps absorb the energy. In operation the ESD clamps behave like resistors which shunt the ESD current to ground and limit the maximum voltage drop on-chip caused by the ESD discharge. When multiple ESD clamps are distributed around the I/O ring they share the ESD discharge current in parallel.

ESD performance depends largely on the total loop resistance of the ESD clamps to the signal I/O cells. The ESD Constellation diagram (see Figure 10) provides sufficient information to define and analyze all ESD discharge loops.

Figure 16 shows how the power and ground rails are modeled in I/O cells that are representative of the entire library.

Figure 16: Power and Ground Rail Resistance Model



The following tables provide the power and ground resistances for a 25um pitch I/O cell library.

Note: Technology specific values for resistance override those provided in the Implementation guide

Table 14:I/O Cell Rail Resistance

Power Rail	Model Resistor	Metal m /um	25um Cell m	ESD Rule (Refer to Table 16:)
MVDD	Rdd	23.16	579	-
MVSS	Rss	3.72	93	yes
MVDDQ	Rddq	1.40	35	yes
MVSSQ	Rssq	2.08	52	yes
MVAA_PLL	Raaq	11.68	292	-

Table 15:I/O PAD Net Resistance

PAD	Model Resistor	Value m
MVDD	Rdd_P	276
MVSS	Rss_P	273
MVDDQ	Rddq_P	271
MVSSQ	Rssq_P	270

MVAA_PLL	Raaq_P	275

4.7 ESD Guidelines

4.7.1 Grounding

For optimal ESD protection, it is very important to observe high quality grounding throughout the I/O ring of the chip. Redundant strapping and distributive grounding to p-substrate bulk is key to hardening the chip against CDM damage. Following the signal/power/ground ratio rules not only ensures good interface SI, it will also ensure signal pins are close enough to ESD clamps in the power pins to satisfy recommended grounding and ESD rules.

The following grounding practices are recommended:

1. All metal ground rails that provide well taps to the common P-substrate in the chip should be connected together, either by unbroken runs of metal, or with redundant metal strapping.
2. The DDR interface I/O ground (MVSSQ) and all core grounds (MVSS and VSS) should be bonded together in the package to a common ring and/or plane. If PVSS_PLL cell is used for PLL grounding, the preferred implementation is to have MVSS_PLL bonded to this common ring and/or plane as well.
3. Use wide metal to avoid IR drop, strapped if need be with higher levels of metal.
4. Increase number of vias/contacts into the common P-substrate throughout the design and, especiall, at the ESD location.
5. Use flip-chip and high MVSS pad count.
6. The MVSS rail in the SSTL library must be strongly connected to the SoC core ground grid. Connect the wide pins in the PVSS power supply cell into the core ground grid and also connect every core side MVSS pin on all SSTL cells into the core ground grid. This promotes good SI and good CDM performance as well as good HBM and MM performance.
7. The MVSS rail in the SSTL library must be strongly connected to the primary ESD discharge rail for the other I/O on the die. This is usually the core ground rail. Connect across directly where the SSTL cells meet the other I/O cells as well as via the core ground grid (as per previous point).

4.7.2 Placement

The following I/O cell placement rules are recommended to ensure that power and ground rail resistances are within acceptable boundaries for good ESD performance:

1. Avoid placing I/O signal cells at the ends of power and ground runs or near breaks in the I/O ring. Each I/O signal cell should have Power and Ground cells on either side of it. Where this is not possible, the ESD resistance rules must be halved.
2. Avoid placing I/O signal cells adjacent to corner cells. Where this is unavoidable, the ESD resistance rules should be halved. It is highly recommended that cells adjacent to corner cells be power and ground cells. This is especially important for good CDM ESD performance.
3. Alternate PVDDQ_ESD power cells with PVDDQ_CAP power cells in the I/O ring such that they:
    a. Are uniformly distributed throughout the ring
    b. Are approximately equal in number.
    c. Still meet the ESD resistance rules.

4.7.3 Clamp Strength

Generally, a minimum of two ESD clamp cells are required in any power domain or in any isolated power island to meet minimum ESD performance criteria for the library. Reduced ESD performance will occur if only one ESD clamp cell is used. This rule applies to:

1. PVDDQ_ESD cells in an isolated VDDQ island
2. PVDD_ESD cells in an isolated VDD island (rare)
3. PVAA cells which do not share MVAA bussing
4. PVAA_PLL cells which do not share MVAA_PLL bussing

4.7.4 Rail Resistance

For good, uniform ESD performance throughout any DDR I/O interface, it is very important that I/O cell placement in the interface be organized to meet the ESD rail resistance rules shown in Table 16:. The resistance rules assume that I/O signal cells are surrounded by power and ground cells in a distributed system. In the case of I/O with power and ground only on one side, half resistance rules will apply.

Table 16:ESD Rail Resistance Rules

ESD Rule	Maximum Resistance to I/O ( )		Clamp Loop Resistance to I/O ( )
	Both Sides	One Side	
MVSS	1.0	0.5	1.0
MVDDQ	1.0	0.5	
MVSSQ	1.0	0.5	N/A

Ultimately, ESD performance depends on clamp loop resistance to the I/O. In the case where PVDDQ_ESD and PVSS cells are place on each side of an I/O cell, the loop resistances of the ESD clamps on either side of the I/O cell operate in parallel with the two clamps. With maximum MVDDQ and MVSS rail resistance to the IO, on each side, the parallel loop resistance works out to be the following:

(Rss1+Rddq1)*(Rss2+Rddq2) / (Rss1+Rddq1+Rss2+Rddq2) = (1.0+1.0)*(1.0+1.0) / (1.0+1.0+1.0+1.0) = 1.0

The same loop resistance is obtained with a single ESD clamp on one side of the I/O, if the half-resistance rules are applied. Cases where the I/O is surrounded by ESD clamp cells, but the rail resistances on one side are greater than 1.0 , the clamp loop resistance criteria can still be met if the rail resistances on the other side of the I/O are sufficiently low.

With distributed ESD clamps, each ESD clamp along the I/O ring reinforces the other, but with diminishing effect the further it is from the I/O cell being protected. To account for this effect a much more detailed analysis of the ESD constellation is required.

5 Chip Finishing

5.1 Dont_touch and Special Nets

Certain nets in the design are designed to be connected without any buffering or with very controlled buffering. Some EDA tools like to try to buffer nets when not required and need to be instructed not to do so. The Following is a list of nets which designers should ensure that their synthesis and place-and-route tools are not altering in any way

PHY-to-I/O signals

- These signals should not normally be buffered. If these signals have to be buffered, their buffering must be balanced across all PHY-to-I/O signals to minimize skew.

PLL Analog output (pll_ato_at)

- This signal, although it may be connected to many PLLs, is an analog signal that cannot be buffered.
- This signal should be routed with a maximum interconnect impedance of 25k Ohms between any one PLL and the analog I/O cell (PAIO). The purpose of this recommendation is to limit the measurement error due to the interconnect IR drop.
- pll_ato_at is considered a high voltage net. Refer to the technology guidelines for width and spacing requirements.

pll_vdd

- This signal needs special attention due to the resistance requirements of the PLL
- The PLL uses a core VDD supply as well. Care should be taken to avoid allowing the VDD interconnect to the PLL from being subjected to unnecessary crosstalk or noise sources (ie superfluously routed VDD lines over very noisey sources that could couple additional noise in).

VREF, ZIOH, LENH and POCH

- These signals are internal to the I/O ring and are connected by abutment
- These signals should be treated as analog signals and not permitted to be buffered

5.2 SSTL I/O Library Usage

The SSTL I/O library contains power, ground, I/O, differential, endcap, filler, corner and pad cells. Refer to the SSTL data book for the cell descriptions and specifications.

5.3 LVS Notes

5.3.1 Cells without Devices

The LVS netlist contains calls to various cells including some cells that do not contain LVS-able devices. When a tool such as Calibre LVS extracts the layout, it may ignore hierarchical levels that do not contain devices. Thus, when the LVS comparison is made, it sees the presence of some cells in the source netlist and their absence in the extracted netlist. In order to work around this, within Calibre the LVS BOX command is used. While that level of hierarchy is still extracted, this command instructs Calibre to ignore the contents of the cell even if the contents are empty and look at only the pin connectivity of the cell. If the designer has calls in the netlist to any cells that do not have a device in layout, an LVS BOX statement must be used. Here is an example list of cells within the Synopsys PHY that do not contain discrete devices:

SSTL Library

- SNPS_DXX_PFILL1
- SNPS_DXX_PFILL_1
- SNPS_DXX_PFILL_5

If Hercules is used for LVS, no special LVS BOX or equivalent statements are needed to deal with cells without devices.

5.4 Advanced Process Rules

Due to the increasing complexities of density fill rules including window sizes, window stepping sizes, and max/min density requirements, the hard-IP components have been designed to allow the user to complete density fill at the chip level using such EDA tools such as Synopsys Hercules. This helps to prevent exceeding the maximum density rules within a particular window when the hard-IP elements of this solution are placed within the customers design and then surrounded by the customers logic routing. This methodology complies with the foundries recommendation of performing density fill at the chip level instead of at the block or cell levels.

All of the hard-IP components include process antenna protection diodes on all input pins. This is reflected within the LEF Files.

6 Guidelines Specific to Synopsys IC Compiler and Astro

6.1 Synopsys Milkyway Library Setup

To set up the Synopsys DDR4 MULTIPHY components for use in Synopsys tools Milkyway, libraries are required to be defined with the desired technology file. One way to generate the Synopsys Milkyway library is to use the supplied LEF Files. The following is a sample procedure for the SSTL I/O library. A similar procedure is also followed for the AC and DATX8 components, however, for these two libraries; the auLoadCLF step should be omitted.

```
cmCreateLib
setFormField "Create Library" "Library Name" "SNPS_I/O.mdb"
setFormField "Create Library" "Technology File Name" "../tech/astroTechFile.tf"
setFormField "Create Library" "Set Case Sensitive" "1"
formOK "Create Library"

read_lef
setFormField "Read LEF" "Library Name" "SNPS_I/O.mdb"
setFormField "Read LEF" "Cell LEF Files" "../lef/snps_dXX_io_merged.lef"
setFormField "Read LEF" "Overwrite Existing Technology" "1"
formOK "Read LEF"

auExtractBlockagePinVia
setFormField "Extract Blockage" "Library Name" "SNPS_I/O.mdb"
formButton "Extract Blockage" "extractBlkg"
setFormField "Extract Blockage" "preserve all metal blockage" "1"
setFormField "Extract Blockage" "Treat All Blockage as Thin Wire" "1"
setFormField "Extract Blockage" "Merge Blockage" "0"
formOK "Extract Blockage"

read_lib
readLibForm "logical"
gePrepLibs
setFormField "Library Preparation" "Library Name" "SNPS_I/O.mdb"
formButton "Library Preparation" "importLMDB"
formButton "Library Preparation" "selectDB"
setFormField "Library Preparation" "Min DB To Import" "../synop-
sys/snps_dxxXX_io_ddr3_34_60_bc_<pvt>.db"
setFormField "Library Preparation" "Max DB To Import" "../synop-
sys/snps_dxxXX_io_ddr3_34_60_wc_<pvt>.db"
setFormField "Library Preparation" "Typical DB To Import" "../synop-
sys/snps_dxxXX_io_ddr3_34_60_tc_<pvt>..db"
formOK "Library Preparation"

auLoadCLF
setFormField "Load CLF File" "Load CLF File Without Timing Related Information" "1"
setFormField "Load CLF File" "CLF File Name" "../lef/snps_sstl.clf"
setFormField "Load CLF File" "Library Name" "SNPS_I/O.mdb"
formOK "Load CLF File"

cmMarkCellType
setFormField "Mark Cell Type" "Cell Type" "corner"
setFormField "Mark Cell Type" "Library Name" "SNPS_I/O.mdb"
setFormField "Mark Cell Type" "Cell Name" "SNPS_DXXXX_PCORNER.*"
setFormField "Mark Cell Type" "pattern match" "1"
formOK "Mark Cell Type"

auStreamIn
setFormField "Stream In Data File" "Stream File Name" "../gds/snps_dXX_io.gds"
setFormField "Stream In Data File" "Library Name" "SNPS_I/O.mdb"
formOK "Stream In Data File"

quit
```

The library deliverables do not have any CLF. The user can create one and name it snps_sstl.clf. An example CLF may have only one line to indicate the I/O cell orientation as follows:

```
definePad "SNPS_DXX_PDDRIO" "0"
definePad "SNPS_DXX_PFILL1" "0"
```

```
        definePad "SNPS_DXX_PDQSG" "0"
        definePad "SNPS_DXX_PFILL5" "0"
        definePad "SNPS_DXX_PFILL_1" "0"
        definePad "SNPS_DXX_PFILL_5" "0"
        definePad "SNPS_DXX_PVAA" "0"
        definePad "SNPS_DXX_PVAA_PLL" "0"
        definePad "SNPS_DXX_PVDDQ_CAP" "0"
        definePad "SNPS_DXX_PVDDQ_ESD" "0"
        definePad "SNPS_DXX_PVDD_CAP" "0"
        definePad "SNPS_DXX_PVDD_ESD" "0"
        definePad "SNPS_DXX_PVREF" "0"
        definePad "SNPS_DXX_PVREFE" "0"
        definePad "SNPS_DXX_PVSSQ" "0"
        definePad "SNPS_DXX_PVSSQZB" "0"
        definePad "SNPS_DXX_PVSS" "0"
        "
        definePad "SNPS_DXX_PDIFF" "0"
        definePad "SNPS_DXX_PCORNER" "0"
        definePad "SNPS_DXX_PAIO" "0"
        definePad "SNPS_DXX_PEND" "0"
        definePad "SNPS_DXX_PEND_P" "0"
        definePad "SNPS_DXX_PZQ" "0"
        definePad "SNPS_DXX_PZCTRL" "0"
        definePad "SNPS_DXX_PRETPOCX" "0"
        definePad "SNPS_DXX_PRETPOCC" "0"
        definePad "SNPS_DXX_PFILL5_ISO" "0"
        definePad "SNPS_DXX_PFILL5_ISO_VDDQVSSQ" "0"
        definePad "SNPS_DXX_PVSSQZB" "0"
        definePad "SNPS_DXX_PVSSQZB_ZQ" "0"
        definePad "SNPS_DXX_PPADW035" "0"
        definePad "SNPS_DXX_PPADWI35" "0"
XX
```

7 Timing Constraints

All constraints required for synthesizing and timing the DDR4 multiPHY IP are included and tested in the constraints file that is shipped with the IP. An example design is also included in the release so that these constraints can be tested on the example design. The example design, including how to run synthesis and STA on it, is described in detail in Section 8.

There are two groups of constraints. The first group consists of general clock constraints required at the chip level to correctly constrain the DDR3 PHY. The second group consists of core PHY constraints that are independent of the chip design and must be applied directly onto the PHY instantiation.

7.1 Clock Definitions and Constraints

To correctly time the interface between the controller and the PHY. There are five clocks that need to be defined for the PHY. The constraints file shows how these clocks are defined and constrained.

7.1.1 Input (Reference and Memory Controller) Clock

This is the main clock source for the chip and may be either a primary input pin or the output of a chip-level PLL. This is defined in the constraints as `CTL_CLK`. It is used to drive the PUB registers that interface to the PHY. It is also used as the input to the PHY PLL, and hence the root for the) PHY clocks (`AC_CTL_CLK, AC_DDR_CLK, DXn_CTL_CLK, DXn_DDR_CLK`) .

7.1.2 PHY Clocks

These are the clocks that drives the PHY registers that interface to the memory controller. The PHY clocks are defined in the constraints as `AC_CTL_CLK, AC_DDR_CLK, DXn_CTL_CLK, and DXn_DDR_CLK` and are created as a generated clocks at the PLL outputs with `CTL_CLK` as their source and a multiplier factor of 1 for AC/DXn_CTL_CLK and multiplier of 4 for the DAC/DXn_DDR_CLK.

Refer to the PHY Utility Block (PUB) Databook for clock relationships in ATPG mode.

7.1.3 Configuration Clock

The configuration clock is used to clock the PUB. It can be an independent clock asynchronous to the main memory controller clock (`CTL_CLK`), or it may be synchronized to the later depending on the implementation of the controller. The constraints provided for the example chip design assume as independent configuration clock input and is therefore defined on the primary configuration clock pin of the design (`cfg_clk`). When using the Synopsys memory controllers (PCTL or MCTL), refer to the controller databook and application notes on how the configuration clock should be defined and constrained.

7.1.4 ATPG Clock

The ATPG clock is used during scan test mode and is normally an independent clock asynchronous to the controller and configuration clocks. The constraints provided for the example chip design assume as independent ATPG clock input and is therefore defined on the primary configuration clock pin of the design (`cfg_clk`).

7.1.5 Controller-PHY Interface Clock Uncertainty Margins

The interface between the memory controller/PUB and the PHY is clocked by the CTL_CLK in the controller/PUB and AC/DXn_CTL_CLK in the PHY. There are two categories of clock uncertainty margins that need to be applied on this interface, i.e. from CTL_CLK to AC/DXn_CTL_CLK and vice-versa. The first category is mandatory and is used to model the effect of the following PHY design parameters:

PLL phase error: This is the phase error between the PHY PLL reference clock and the PLL feedback clock. The error affects the alignment of the CTL_CLK to the AC/DXn_CTL_CLK and therefore is included as clock uncertainty between these two clocks. Its value is specified in the PHY databook as t_{PHERR}.

PLL Jitter: This is the PHY PLL output jitter and affects the placement of the AC/DXn_CTL_CLK relative CTL_CLK. It is therefore included as clock uncertainty between these two clocks. Its value is frequency dependent and is specified in the PHY data-book as t_{OJITT}.

The total mandatory clock uncertainty between CTL_CLK and AC/DXn_CTL_CLK is equal to (t_{PHERR} + t_{OJITT}). While some of the parameters are frequency dependent, it is recommended to use the maximum values across the desired frequency range since this uncertainity will affect hold timing as well.

The user may choose to add extra margins on top of these mandatory PHY margins. This category of margins is optional and depends on the design methodology used in the rest of the user chip design. Examples of such margins are included in the sample constraints provided and include design-wide extra setup and hold margins. Some of these margins are applied only on pre-layout synthesis/STA to account for clock skew that will be introduced after the clock trees are implemented.

7.1.6 Clock Tree Distribution and CTS Sync-point

Skew for ddr_clk arrival time at each DATX8 ddr_clk pin (timed through the PLL, if PLLs are used in the design) is recommended to be within +/-50 ps of the ddr_clk arrival time at the AC ddr_clk pin. There should be no more than 8% tCK skew between any DQS/DQSN I/O pDOUT pin and any CK/CKN I/O DOUT pin. This can mean that one DQS is 8% tCK longer than CK and another DQS is 8% tCK shorter than CK.

Measurement should be made in an accurate timing mode without OCV, using max_rise and max_ falland be compared only within each corner, not across corners. For example, compare CK in FF to DQS and FF but do not compare CK in FF to DQS in SS.

For designs that support PLL bypass mode or designs that do not use PLLs, ddr_clk should arrive at DATX8 or AC aligned with ctl_clk arrival at that same instance or up to t_{skew_margin} earlier than ctl_clk; ddr_clk should never arrive later than ctl_clk to a given DATX8 or AC instance. For information on the t_{skew_margin} value, refer to the DDR4 multiPHY Databook.

There are no skew requirements to consider for ctl_rd_clk. This is an independently-controllable input to DATX8 and AC used to clock outputs from these blocks back to the PUB. Ctl_rd_clk is not generated by a PLL. It uses a pin separate from ctl_clk specifically to enable the user to apply useful skew to this clock, making it easier to satisfy setup and hold requirements on synchronous paths from the DATX8 or AC back to the PUB.

When using ICC for clock tree synthesis, clock tree sync points can be defined as follows:

Define a stop pin for AC & DATX8 PHY macro ctl_clk and ddr_clk input
Define a floating pin for AC & DATX8 macro PLL pllin_x1 input
Define a floating pin for AC & DATX8 macro ctl_rd_clk input

The floating pin max-delay calculations below are considered a starting point, and more iterations may be required for CTS adjustment.

Floating pin max-delay may be calculated by the following:

ctl_rd_clk

- Open DATX8 WC .lib, search by "bus (phy_q)" and then locate "pin("phy_q[*]")"
- Scroll down till you find "related_pin : "ctl_rd_clk""
- Get the first value from Cell_rise delay table
- Divide it by 3 (ctl_rd_clk -> phy_q[*] path is relatively longer)

pllin_x1

- Open PLL WC .lib, search by "pin("pllout_x1")"

- Scroll down till you find "related_pin : "pllin_x1""
- Get the first value from Cell_rise delay table

7.2 PHY Constraints

7.2.1 Interconnect Skew between PHYAC/PHYDATX8 and I/Os

7.2.1.1 Skew Requirement Summary

Synopsys recommends the following:

The I/O order should align with the PHY macro pins to avoid crossing routes (especially in the CA lane). The define file provides a description of command and address lane signal assignments which, at the RTL stage, can be adjusted to match the I/O ring order.

The distance between PHY macros and I/O ring requires sufficient routing resources for the balanced routes. The metal layers used should also match for all nets.

Using no more than four clock buffers or four pairs of inverters (and fewer if possible) on all skew-balanced paths between PHY macros and I/Os. It is also recommended that within a signal group (with AC or within DATX8) the same numbers of buffers or inverters are used on all paths.

All paths should use uniform Vt buffers or inverters in a single power domain.

The tightest paths (4% tCK requirement) should also use exactly the same cells on each path within a skew-balanced group.

Measurement should be made in an accurate timing mode (“-pba_mode” for PrimeTime) without OCV, using max_rise and max_fall (no min measurement required) and compared only within each corner, not across corners. For example, compare CK in FF to DQS in FF; compare CK in SS to DQS in SS; do NOT compare CK in FF to DQS in SS.

In the skew constraints, tCK refers to the minimum supported DRAM clock period. The DRAM clock is half the period of the ctl_clk in an HDR system. OCV should not be included when reporting arrival times for balancing skews. Skew requirements must be satisfied for both rising and falling edges in all mission-mode timing corners.

The skew-balanced paths mean the routes (including added buffers or inverters if applicable) between PHY macro input/output pins and core side input/output pins of I/O cells.

Table 17: Skew Summary

Signal Group	Condition	Group Description	Skew Window Requirement (w/o OCV)	Transition Requirement[1]
pll_ddr_clk_out	Always (recommendation only)	Root clock tree balancing. From clock tree source to pllout_x4x2 output of all PLLs	50 ps guideline. NOT a sign-off check (For sign-off, meet ck_dqs group check below)	The lesser of 10% tCK or 100 ps
ck_dif	Always	Differential clock pairs, skew balanced only between CK/CKN, From clock tree source to DOUT pin of IO cell	10 ps for all 4 measurements of CK-rise, CK-fall, CKN-rise, and CKN-fall in each pair independently	The lesser of 10% tCK or 100 ps
dqsout_dif	Always	Differential DQS pairs, skew balanced only between DQS/DQSN. From clock tree source to DOUT pin of IO cell	10 ps for all 4 measurements of DQS-rise, DQS-fall, DQSN-rise, and DQSN-fall in each pair independently	The lesser of 10% tCK or 100 ps
ck_dqs	Always	All CK/CKN pairs to each DQS/DQSN pair. From clock tree source to DOUT pin of IO cell	8% tCK measure rising edge of CK and DQS, falling edge of CKN & DQSN.	The lesser of 10% tCK or 100 ps
dqsin_dif	Always	Differential DQS pairs, skew balanced only between DQS/DQSN in each pair independently	10 ps on rising edges of qs/qs_n.	The lesser of 10% tCK or 100 ps
ac_signals	Always	Critical signals from AC to IOs.	4% tCK	The lesser of 10% tCK or 100 ps
dx_signals	Always	Critical signals from DATX8 to IOs.	4% tCK per DATX8 group	The lesser of 10% tCK or 100 ps
ac_to_io	Always	Critical and IO ocntrols from AC to IOs	8% tCK	The lesser of 10% tCK or 100 ps
dx_to_io	Always	Critical and I/O controls from DATX8 to I/Os	8% tCK per DATX8 group	The lesser of 10% tCK or 100 ps
io_to_ac	Always	Critical and less-critical signals from IO DI pins to AC macro inputs	8% tCK	The lesser of 10% tCK or 100 ps
io_to_dx	Always	Critical signals from IO DI pins to DATX8 macro inputs	4% tCK per DATX8 group	The lesser of 10% tCK or 100 ps

[1] If buffers or inverters are used on skew-matched paths, then transition requirements must be met on ALL nets in that path

Signal Group	Condition	Group Description	Skew Window Requirement (w/o OCV)	Transition Requirement[1]
zctrl_strict	When CK is running during PVT updates (=dfi_ctrlupd_req or dfi_phyupd_ack from controller)	From PUB FFs to VREF cell within AC_io.v	100 ps in fastest corner 200 ps in slowest corner	Standard STA max_trans
	CK not running and/or DRAM in self refresh during PVT updates		None, meet max_delay (4 CTL_CLK cycles) and max_trans only	Standard STA max_trans
zctrl_relaxed	Always	From PUB FFs to ZCTRL[27:14,9:7,2:0] of above VREF cell; ZCTRL[27:0] to all other VREF/VREFE cells	None, meet max_delay (4 CTL_CLK cycles) and max_trans only	Standard STA max_trans
pub_to_acio	Always	From PUB FFs to TE & PDR pin of AC IOs	None	Standard STA max_trans
RET/RET_B pin of *PRETPOC* IO cell	Always	Differential data retention inputs	Max. 300 ps between RET/RET_B	Standard STA max_trans
bypass_clks1	No PLL	Same AC/DATX8 instance ddr_clk & ctl_clk arrival time	0>= [ddr_clk_arrival time - ctl_clk arrival time] >= $t_{skew\_xmargin}$ $t_{skew\_xmargin}$ depends on the formula in Section 5.2.6.1.1 Extra Margin for the Extra Delay of ctl_clk in the DDR4 multPHY Databook	The lesser of 10% tCK or 100 ps
bypass_clks2 Max speed is less than 1066	PLL bypass	Same AC/DATX8 instance ddr_clk & ctl_clk arrival time	0>= [ddr_clk_arrival time - ctl_clk arrival time] >= $t_{skew\_xmargin}$ $t_{skew\_xmargin}$ depends on the formula in Section 5.2.6.1.1 Extra Margin for the Extra Delay of ctl_clk in the DDR4 multPHY Databook	The lesser of 10% tCK or 100 ps

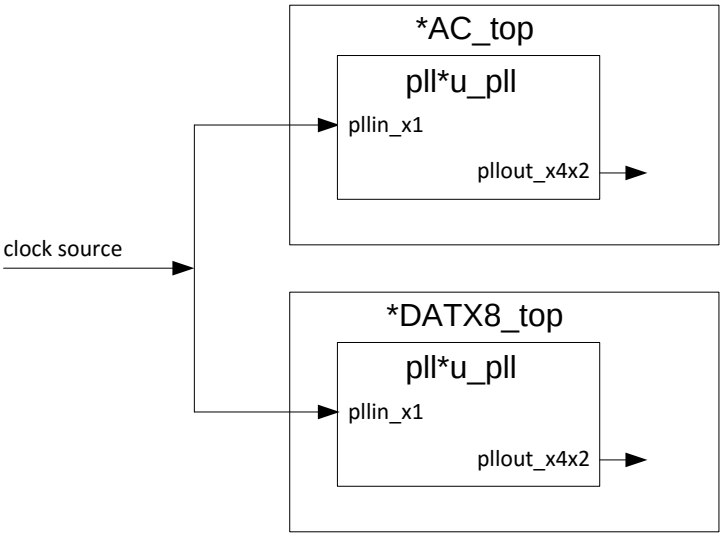
7.2.1.2 pll_ddr_clk_out Group Start and End Points

The skew target listed for this group is a guideline only. It is intended to create a good starting point at the initial CTS stage and help the user to achieve the required guideline for the ck_dqs group. It is acceptable to deviate from this pll_ddr_clk_out guideline in order to meet the ck_dqs requirement.

Start Point:
clock source through phy_ctl_clk
End Points
*AC_top/pll*u_pll/pllin_x1

DATX8_top/pll*u_pll/pllin_x

Figure 17: pll_ddr_clk_out Group Start and End Points

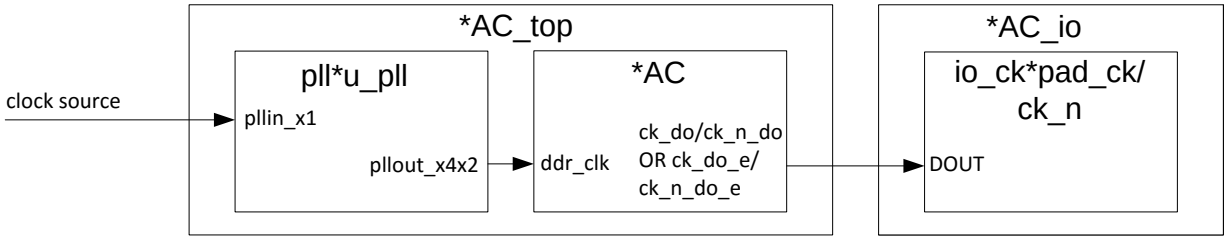


7.2.1.3 ck_dif Group Start and End Points

The check helps to ensure the DRAM's DCD and Vix requirements are met on the listed differential pairs.

Start Points:
clock source
Through:
* AC macro output pins:
ck_do[*]
ck_n_do[*]
OR
ck_do_e[*]
Ck_n_do_e[*]
End Points:
*AC_io/io_ck*pad_ck/DOUT
*AC_io/io_ck*pad_ck_n/DOUT

Figure 18: ck_dif Group Start and End Points

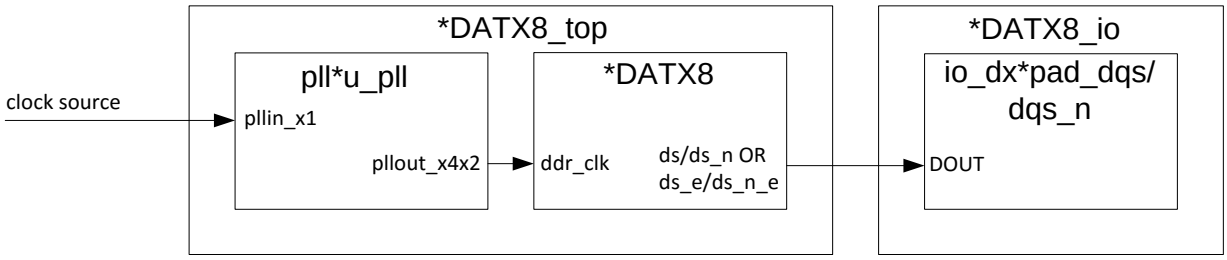


7.2.1.4 dqsout_dif Group Start and End Points

The check helps to ensure the DRAM's DCD and Vix requirements are met on the listed differential pairs.

Start Points:
clock source
Through:
* DATX8 macro output pins:
ds, ds_n
OR
ds_e, ds_n_e
End Points:
*DATX8_io/io_dx*pad_dqs/DOUT
*DATX8_io/io_dx*pad_dqs_n/DOUT

Figure 19: ck_dif Group Start and End Points



7.2.1.5 ck_dqs Group Start and End Points

The check helps to ensure that the DRAM's tDQSS timing requirement is met.

Note: Non-leveled is assumed for bit rates up to 1066 Mbps (including all LPDDR2 uses). Leveling is assumed to be available for higher bit rates.

Start Point:
Clock source through phy_ctl_clk
End Points:
Same as ck_dif and dqsout_dif

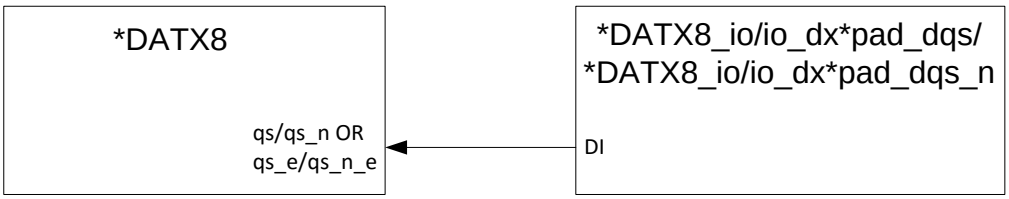
For this check only, it is sufficient to check only the following edges:
1. Rising edge of io_dx*pad_dqs
2. Falling edge of io_dx*pad_dqs_n
3. Rising edge of io_ac*pad_ck
4. Falling edge of io_ac*pad_ck_n

7.2.1.6 dqsin_dif Group Start and End Points

The check helps to ensure optimal read capture timings into the DATX8 macros.

Start Points:
*DATX8_io/io_dx*pad_dqs/DI
*DATX8_io/io_dx*pad_ds_n/DI
End Points:
DATX8 macro input pins:
qs, qs_n
OR
qs_e, qs_n_e

Figure 20: dqsin_dif Group Start and End Points



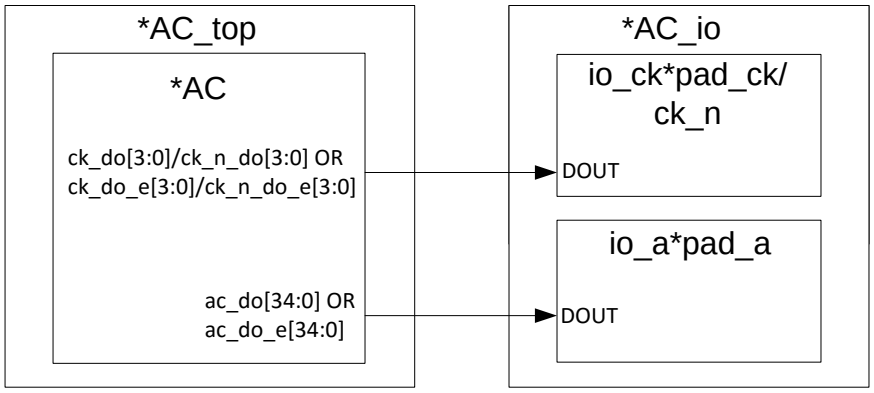
7.2.1.7 ac_signals Group Start and End Points

The check helps to ensure optimal setup/hold timings on AC signals to the DRAM devices.

Note: Bit deskew is only on LPDDR3 and only for CA[9:0]. The timings assume bit deskew only for these cases.

Start Points:
AC macro output pins:
ck_do[3:0], ck_n_do[3:0], ac_do[34:0]
OR
ck_do_e[3:0], ck_n_do_e[3:0], ac_do_e[34:0]
End Points:
*AC_io/io_ck*pad_ck/DOUT
*AC_io/io_ck*pad_ck_n/DOUT
*AC_io/io_a*pad_a/DOUT

Figure 21: ac_signals Group Start and End Points



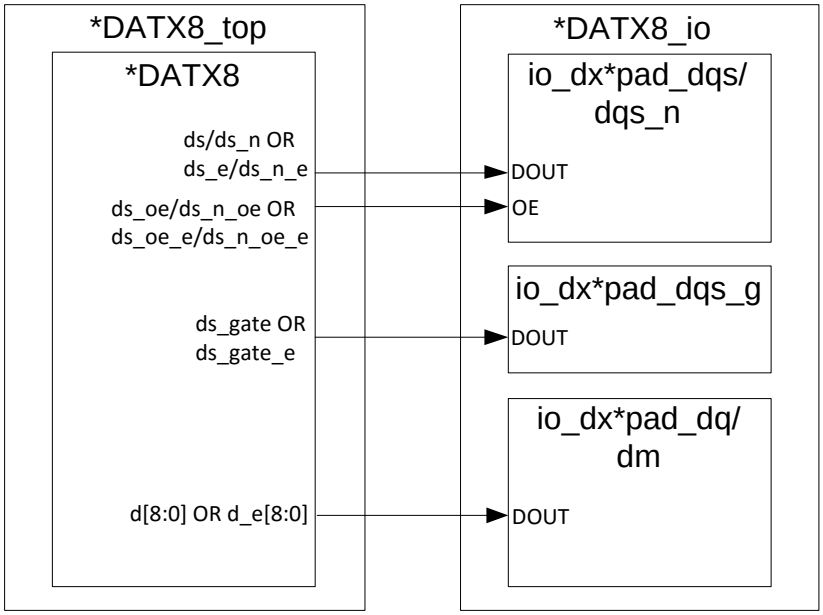
7.2.1.8 dx_signals Group Start and End Points

The check helps to ensure optimal data setup/hold at the DRAM.

Note: Bit deskew is available and assumed for these signals in all cases.

Start Points:
DATX8 macro output pins:
ds, ds_n, ds_oe, ds_n_oe, ds_gate, d[8:0]
OR
ds_e, ds_n_e, ds_oe_e, ds_n_oe_e, ds_gate_e, d_e[8:0]
End Points:
*DATX8_io/io_dx*pad_dqs/DOUT (or OE)
*DATX8_io/io_dx*pad_dqs_n/DOUT (or OE)
*DATX8_io/io_dx*pad_dq/DOUT
*DATX8_io/io_dx*pad_dm/DOUT
*DATX8_io/io_dx*pad_dqs_g/DOUT

Figure 22: dx_signals Group Start and End Points

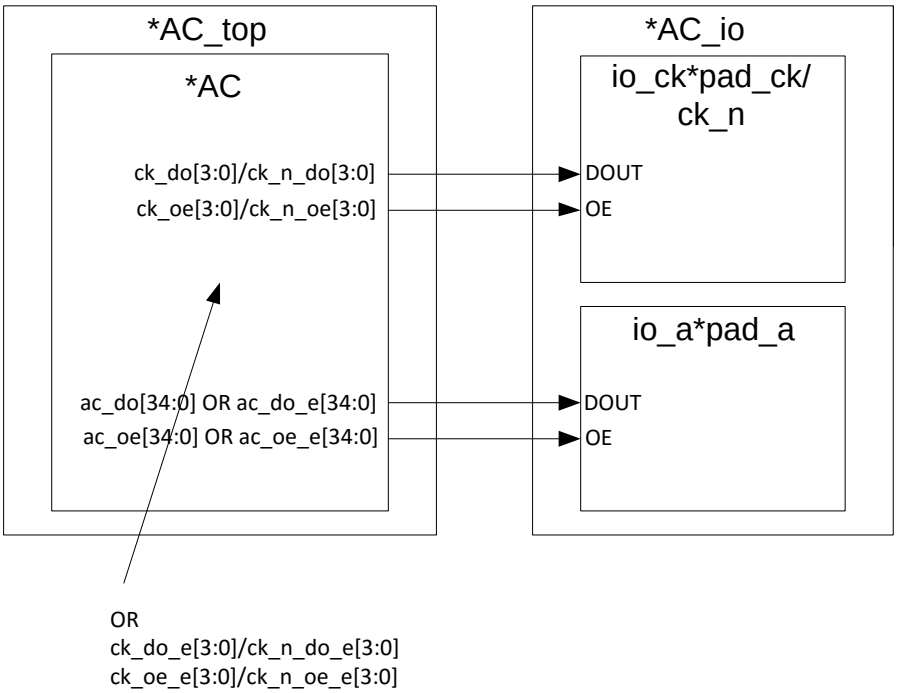


7.2.1.9 ac_to_io Group Start and End Points

The check ensures that controls to the DRAM can applied as intended. These are important for the following cases

Start Points:
AC macro output pins:
ck_do[3:0], ck_n_do[3:0], ac_do[34:0]
ck_oe[3:0], ck_n_oe[3:0], ac_oe[34:0]
OR
ck_do_e[3:0], ck_n_do_e[3:0], ac_do_e[34:0]
ck_oe_e[3:0], ck_n_oe_e[3:0], ac_oe_e[34:0]
End Points:
*AC_io/io_ck*pad_ck/DOUT (or OE)
*AC_io/io_ck*pad_ck_n/DOUT (or OE)
*AC_io/io_a*pad_a/DOUT (or OE)

Figure 23: ac_to_io signals Group Start and End Points



7.2.1.10 dx_to_io Group Start and End Points

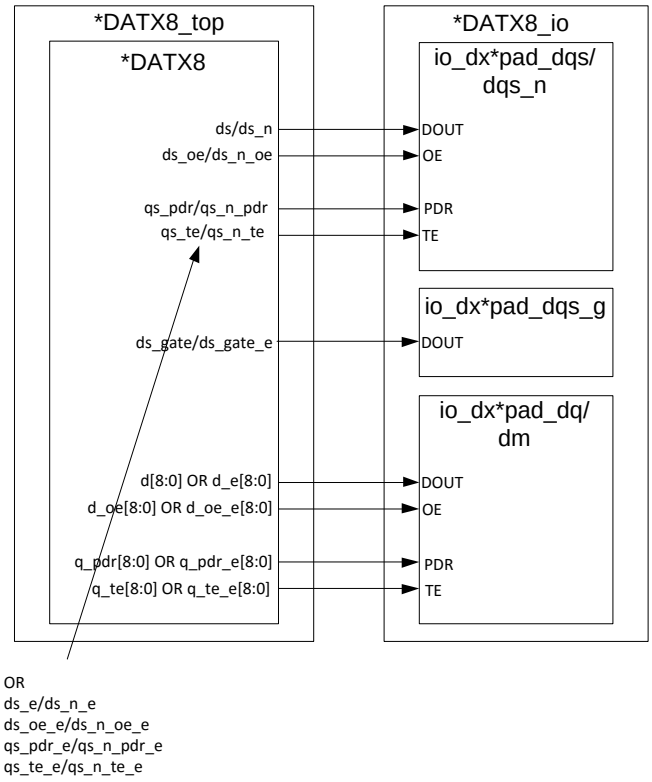
The check ensures that PDR, OE, and TE controls to the DRAM can applied as intended. These are important for the following cases:

OE is applied dynamically at the start/end of each transaction. By design, the D_OE is generated more than 1/8 tCK and up to 5/8 tCK after the DQS to ensure correct data at the DRAM thus the DWC_DDRPHY-DATX* includes a ¼ tCKmax skew between the D/DS/DS_OE pins and the D_OE pin. The ¼ tCKmax is calculated at the maximum frequency. (0000164:0000200 ps @ 600MHz/2400Mb/s) which results is a 25% tCK maximum skew between the D_OE and D/DS/DS_N/DS_OE.

PDR and TE are toggled dynamically at the start/end of each read data burst

Start Point:
DATX8 macro output pins:
ds, ds_n, ds_oe, ds_n_oe,
d[8:0], d_oe[8:0]
qs_pdr, qs_n_pdr, q_pdr[8:0]
qs_te, qs_n_te, q_te[8:0]
OR
ds_e, ds_n_e, ds_oe_e, ds_n_oe_e,
d_e[8:0], d_oe_e[8:0]
qs_pdr_e, qs_n_pdr_e, q_pdr_e[8:0]
qs_te_e, qs_n_te_e, q_te_e[8:0]
End Point
*DATX8_io/io_dx*pad_dqs/DOUT (or PDR, OE, TE)
*DATX8_io/io_dx*pad_dqs_n/DOUT (or PDR, OE, TE)
*DATX8_io/io_dx*pad_dq/DOUT (or PDR, OE, TE)
*DATX8_io/io_dx*pad_dm/DOUT (or PDR, OE, TE)
*DATX8_io/io_dx*pad_dqs_g/DOUT

Figure 24: dx_to_io Group Start and End Points

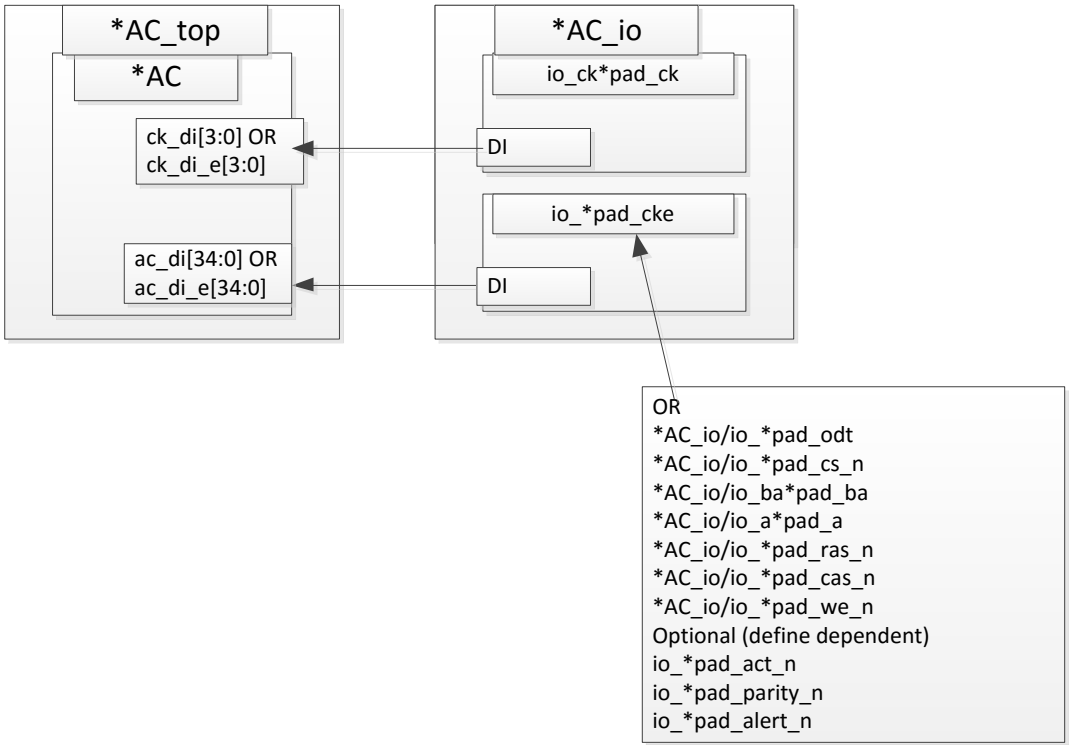


7.2.1.11 io_to_ac Group Start and End Points

This check ensures that AC loopback will function as intended.

Start Points:
*AC_io/io_ck*pad_ck/DI
*AC_io/io_*pad_cke/DI
*AC_io/io_*pad_odt/ DI
*AC_io/io_*pad_cs_n/DI
*AC_io/io_ba*pad_ba/DI
*AC_io/io_a*pad_a/DI
*AC_io/io_*pad_ras_n/DI
*AC_io/io_*pad_cas_n/DI
*AC_io/io_*pad_we_n/DI
End Points:
AC macro input pins:
ck_di[3:0], ac_di[34:0]
OR
ck_di_e[3:0], ac_di_e[34:0]

Figure 25: io_to_ac Group Start and End Points

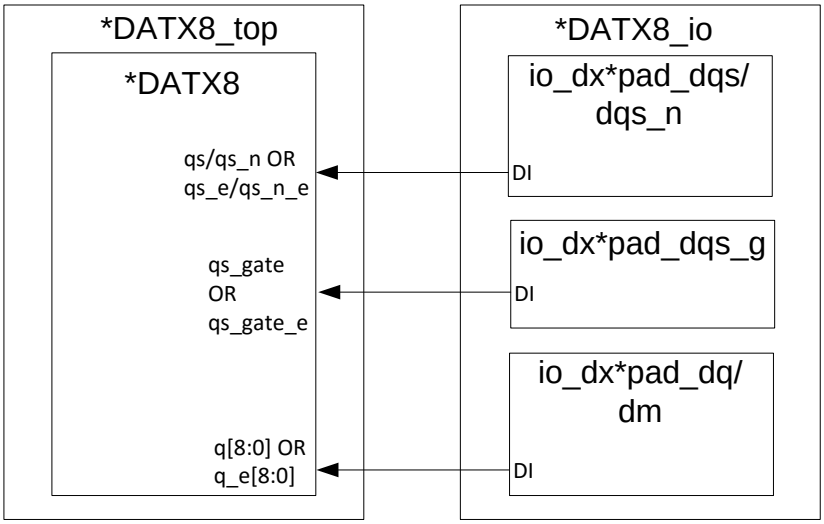


7.2.1.12 io_to_dx Group Start and End Points

The check ensures optimal read setup/hold at the DATX8 macro. It also ensures optimal read gate timing at the macro.

Start Points:
*DATX8_io/io_dx*pad_dq*/DI
*DATX8_io/io_dx*pad_dm/DI
*DATX8_io/io_dx*pad_dqs/DI
*DATX8_io/io_dx*pad_dqs_n/DI
*DATX8_io/io_dx*pad_dqs_g/DI
End Points:
DATX8 macro input pins:
qs, qs_n, qs_gate, q[8:0]
OR
qs_e, qs_n_e, qs_gate_e, q_e[8:0]

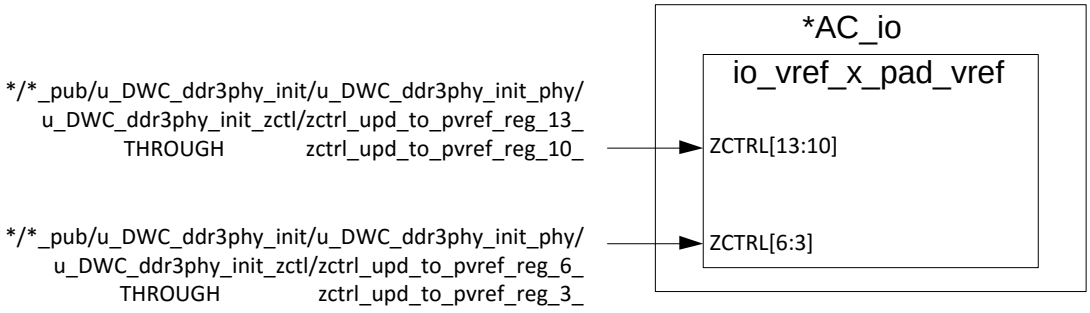
Figure 26: io_to_dx Group Start and End Points



7.2.1.13 zctrl_strict Group Start and End Points

This check ensures that CK port will not jitter or glitch when VT updates are performed.

Figure 27: zctrl_strict Group Start and End Points



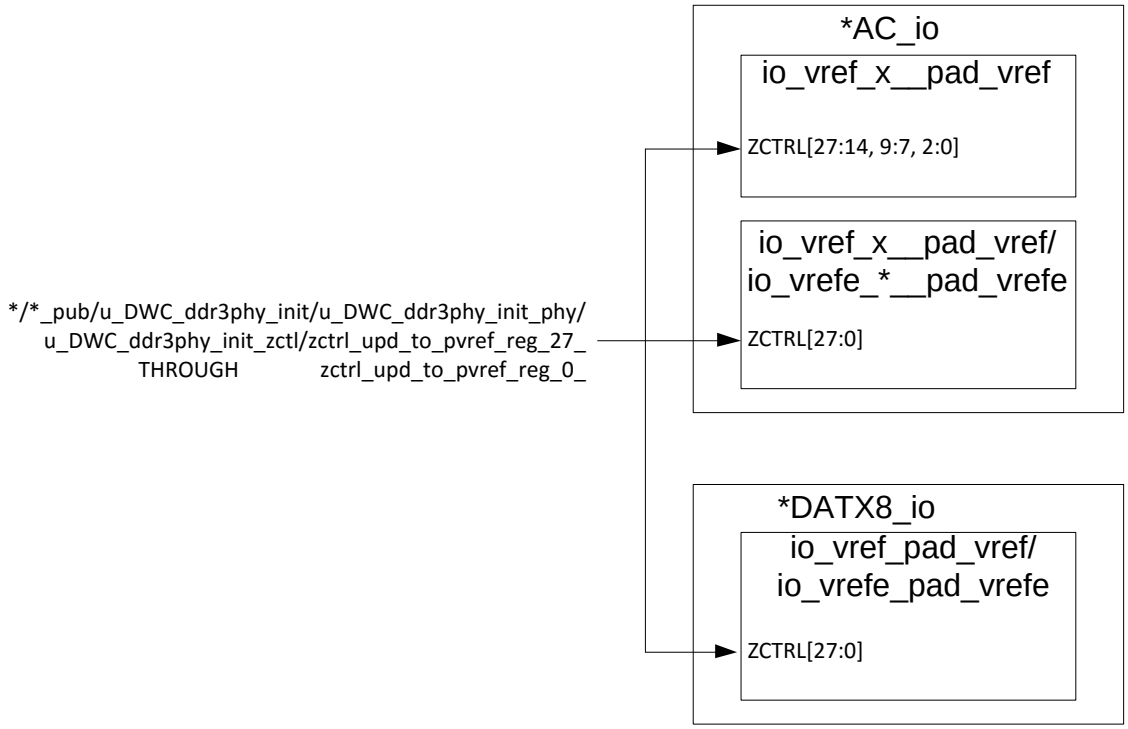
Note: In io_vref_x_pad_vref, the x value means the PVREF SSTL IO associated to the CK port.

7.2.1.14 zctrl_relaxed Group Start and End Points

These bits are non-critical. They are allowed several cycles to update during PVT updates (while the interface is idle, except for the clock.)

Start Points:
PUB FFs.
End Points:
*AC_io/io_vref_x__pad_vref/ZCTRL[27:14,9:7,2:0]
*AC_io/io_vref_N__pad_vref/ZCTRL[27:0]
Note: N <> 0
*AC_io/io_vrefe_*__pad_vrefe/ZCTRL[27:0]
*DATX8_io/io_vref_pad_vref/ZCTRL[27:0]
*DATX8_io/io_vrefe_pad_vrefe/ZCTRL[27:0]

Figure 28: zctrl_relaxed Group Start and End Points



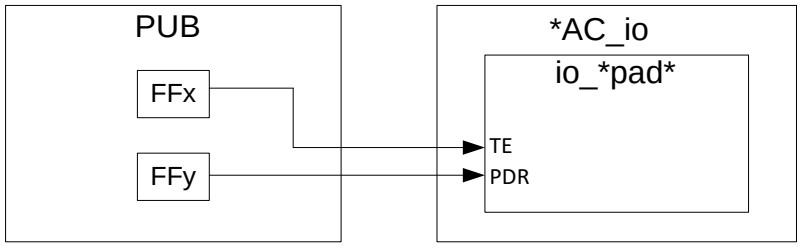
Note: In io_vref_x_pad_vref, the x value means the PVREF SSTL IO associated to the CK port.

7.2.1.15 pub_to_acio Group Start and End Points

This group are all static control signals that are toggled only during initialization.

Start Points:
PUB FFs
End Points:
*AC_io/io_ck*pad_ck/TE (or PDR)
*AC_io/io_ck*pad_ck_n/TE (or PDR)
*AC_io/io_a*pad_a/TE (or PDR)

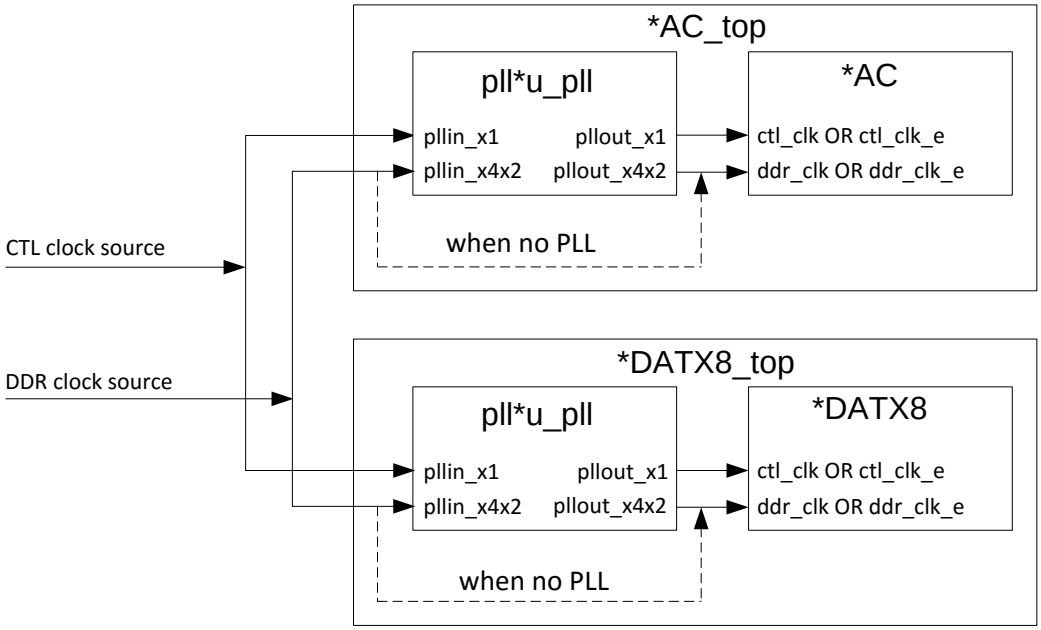
Figure 29: pub_to_acio Group Start and End Points



7.2.1.16 16 bypass_clks Group Start and End Points

Start Points:
clock source(s) through phy_ctl_clk and phy_ddr_clk.
End Points:
*u_DWC_DDR3PHYAC/ddr_clk, *u_DWC_DDR3PHYAC/ctl_clk
OR
*u_DWC_DDR3PHYDATX8/ddr_clk, *u_DWC_DDR3PHYDATX8/ctl_clk

Figure 30: bypass_clks Group Start and End Points



7.2.2 Impedance (ZQ) Calibration

Impedance controller signals should be constrained as a multi-cycle path relative to the configuration clock. It is required that the control and status of the zcomp coming from the ZQ I/O settle within half a clock period of the ZCTRL clock so that the impedance controller can use that status to increase/decrease the control value. This half clock period corresponds to the loop bandwidth of the ZQ calibration. The ZCKSEL field in the PIR register specifies the divide ratio by which the configuration clock is divided down to produce the clock used by the ZCTRL. This divided clock is generated using an enable signal. The logic itself is clocked directly by the configuration clock.

The ZQ calibration multi-cycle path specified in the provided constraints file assume a default divide ratio of 32 and therefore is set to 32/2 = 16 clock cycles. The user may need to modify this value if the divide ratio is set to other values.

A skew specification of 100ps is required for some PVREF.ZCTRL bits driving ZIOH drive strength control bus to the I/O section with CK/CKB I/O cells. PVREF.ZCTRL[13:10] and PVREF.ZCTRL[6:3] bits may be treated as separate groups and the specification can be applied separately to each group. In that case, each I/O section with a clock driver, only two 4-bit busses require skew matching.

Note: When there are two PVREF cells in one ZIOH island, the maximum skew balance between the cells is 200ps.

The provided constraints on the ZCTRL paths from the configuration register to the PVREF IO cells include set_max_path and multicycle path and require manual skew checks. These paths will require additional adjustments to meet the skew requirements if they are buffered automatically. One option is to set_dont_touch on these nets during synthesis and create a matching buffer tree during the place and route stage based on the placement of the related configuration registers.

To check the skew to the I/Os during static timing analysis, an output delay constraint is set through the pins going to the I/Os. This allows the paths through the PUB outputs to be timed to the IOs. Because of the big delay through the PHY and to the SSTL I/O, these paths are set as multi-cycle paths. Note that the value of the output delay constraint and the value of the multi-cycle constraint are not as relevant in the skew analysis. To determine skew, use a simple report timing on these paths and compare the arrival times. The user would then inspect the report either manually or using a higher level script to determine if the skew is within the acceptable range

7.2.3 PHY Static Signals

The PHY contains several control and status signals that are either static or non-timing critical. Rather than setting them as false paths, these signals must be constrained with a maximum delay constraint to prevent ASIC tools from buffering them excessively. In some cases this maximum delay constraint is set to also satisfy the usage of these signals by the PHY Utility Block.

In most cases, this maximum delay is set to 4 times the configuration clock period, which should normally be easy enough to meet. The provided constraints file includes all such constraints for all PHY static signals. These include:

DDL delay select signals

DDL calibration signals

DDL digital test signals

I/O static control signals

PLL static control and status signals

Other miscellaneous PHY static control and status signals

7.2.4 PHY Ideal Networks

PHY ideal networks include signals that should not be buffered by synthesis or place-and-route tools. These signals are therefore constrained as don't touch and as ideal networks. They include the following signals:

PHY PLL analog test output (ato/pll_ato)

VREF signals that connect by abutment in the I/O ring

ZIOH signals that connect by abutment in the I/O ring

LENH signals that connect by abutment in the I/O ring

7.2.5 PHY-Specific Clocks

Apart from general clocks created at the chip level that affect the core side of the PHY (Section **Error! Reference source not found.**), there are PHY-specific clocks that are on the SDRAM side of the PHY. These clocks are created mainly to analyze the skew for the signal paths from the I/Os to the PHYAC/PHYDATX8. There are two groups of these clocks:

Read Data Strobe (DQS) Clocks: These clocks are created on the DQS pins and are used for timing the DQ pins for the read path (I/O to PHYDATX8). To correctly time the DQ pins, an input delay is set on them relative to the DQS clock. For a real fixed-configuration design, DQS clocks must be defined for each PHYDATX8.

Loopback Clocks: These are clocks created on the PHYAC CK input (ck_di) pins and are used for timing the PHYAC loopback path. Since these clocks are simply looped back from the PHYAC CK outputs, they are created as generated clocks and share the same clock source as the main PHY clock (Section **Error! Reference source not found.**).

Paths on both these two groups of clocks should not be touched by synthesis and therefore the clocks are created only for static timing analysis. These clocks are also propagated so that the delays on the clocks match the data since these clocks do not have external clock trees.

7.2.6 PHY Top Module Mode Pins

PHY mode pins need to be constrained depending on the PHY mode used during synthesis and/or STA. These constraints include:

Setting the PHY `atpg_mode` pin to 0 or 1 if in PHY mission mode or PHY ATPG mode, respectively.

7.2.7 PHY Utility Block Asynchronous Paths

Paths inside the PUB that are between the controller clock and the configuration clock are asynchronous and should be constrained with either false paths, maximum delays, or multi-cycle paths depending on the chip-level constraint methodology. In this example design, these paths have been constrained using maximum delay inside the `ddr3phy_chip_clocks` procedure. It is recommended to use either maximum delay or multi-cycle path so that excessive buffering on these nets is avoided.

8 Example Synthesis and STA

8.1 General Overview

The DDR4 MULTIPHY deliverables include an example design as well as example synthesis and STA scripts and constraints that can be used as guidelines for the synthesis and STA of the DDR4 MULTIPHY in the user design.

The synthesis has been tested using Synopsys Design Compiler. There are no known forward-compatibility issues. Backward compatibility to previous versions of Synopsys tools is not guaranteed.

The complete interface and control solution consists of a soft-IP memory controller (modeled in the example file as simple registers), soft-IP PHY Utility Block (PUB), and four hard-IP blocks, namely the DDR3PHYAC, DDR3PHY-DATX8, DDR3PHYPLL, and SSTL I/Os. All the four types of hard macros are instantiated in the DDR3PHY module. All these components are instantiated and connected in the top-level sample chip design, which is used for trial synthesis and STA as well as functional verification.

The Synopsys scripts are established in such a way that they are universal to Design Compiler (DC) and Prime Time (PT) by using a variable that selects the tool being used. The design constraints are universal to both synthesis and STA. There exist separate scripts to execute the synthesis and STA tasks. STA will run properly under both DC and PT, however, PT is recommended where possible as DC is not a recognized sign-off quality STA engine.

8.2 Example Design

The installation kit contains example design files for use with the verification environment as well as the synthesis and STA. The example design is a 32-bit DDR interface but can easily be configured to any width by changing the compiler directive DWC_NO_OF_BYTES in DWC_DDR3PHY_define.v. In top level design file DWC_DDR3PHY_chip.v, a parameter pNO_OF_BYTES is defined based on DWC_NO_OF_BYTE, and later is used to select the number of PHYDATX8's to be instantiated (DDR interface width is equal to 8*pNO_OF_BYTES). The following sections describe the Verilog modules used in the example design. Verilog module names match the corresponding file names.

8.2.1 DWC_DDR3PHY_chip

The DWC_DDR3PHY_chip is the top level block and instantiates DWC_DDR3PHY_top as well as the registers that mimic the controller registers that interface to the PHY, while DWC_DDR3PHY_top instantiates DWC_DDR3PHY block and DWC_ddr3phy_pub block.

The input/output interface is comprised of the following categories of signals:

SDRAM interface pins – connections to external DDR3/2 SDRAM

PHY test outputs – analog and digital test outputs for the PHY

Connection to an external resistor for impedance control

Controller interface to the DDR3PHY instantiated at a higher level

Configuration interface

PHY scan interface

Miscellaneous system level signals such as clocks, resets, and static configuration control

8.2.2 DWC_ddr3phy_pub

The `DWC_ddr3phy_pub` block is the soft-IP RTL for the DDR3PHY Utility Block (PUB).

8.2.3 DWC_DDR3PHY

The DWC_DDR3PHY block instantiates one DWC_DDR3PHYAC_top block and one or more DWC_DDR3PHY-DATX8_top blocks. DWC_DDR3PHYAC_top instantiates DWC_DDR3PHYAC hard macro block and

DWC_DDR3PHYAC_io block. DWC_DDR3PHYDATX8_top instantiates one or more DWC_DDR3PHYDATX8 hard macro and DWC_DDR3PHYDATX8_io block.

8.2.4 DWC_DDR3PHYAC_io and DWC_DDR3PHYDATX8_io

These two blocks instantiates all I/Os associated with the DDR3 PHY which includes:

SDRAM interface SSTL I/Os for control and data

Digital and analog test output IOs

PZQ I/O instantiation(s) for connection to an external resistor for impedance control

Power I/O instantiations

8.3 Scripts and Constraints Files

The following describe the scripts and constraints used with the example design.

8.3.1 Synthesis Script

The file `syn/DWC_DDR3PHY_chip_synth.scr` is the synthesis script. It does the following:

Sources the setup file (`tcl/DWC_DDR3PHY_setup.tcl`) and constraints file (`tcl/DWC_DDR3PHY_ constr.tcl`)

Reads the Verilog RTL files

Sets up the clocks and constrains the design

Compiles (synthesizes) the design

Generates different timing and design reports

Trial synthesis was performed with Synopsys Design Compiler with the Test Compiler license. Synthesis is run from the `syn` directory. It is recommended to use the following command to run Design Compiler synthesis:

```
dc_shell-t -f DWC_DDR3PHY_chip_synth.scr | tee ../reports/syn/run.log
```

After the run, the log file and timing and design reports are created and put in the `../reports/syn` directory.

8.3.2 STA Script

The file `sta/DWC_DDR3PHY_chip_sta.scr` is the STA script. It does the following:

Sources the setup file (`tcl/DWC_DDR3PHY_chip_setup.tcl`) and constraints file (`tcl/DWC_DDR3PHY_chip_constr.tcl`)

Reads the Verilog gate-level netlist created by synthesis

Sets up the clocks and constrains the design

Generates different timing and design reports

Trial static timing analysis was performed with Synopsys Prime Time. STA is run from the `sta` directory. It is recommended to use the following command to run Prime Time STA:

```
pt_shell -f DWC_DDR3PHY_chip_sta.scr | tee ../reports/sta/run.log
```

After the run, the log file and timing and design reports are created and put in the `../reports/sta` directory. Synthesis must be run first before running STA. Note that minor hold-time violations may appear in the synthesis output. This is because hold time violations are not addressed until after placement, initial optimization, and clock-tree synthesis.

8.3.3 Setup Files

The setup file (`tcl/DWC_DDR3PHY_chip_setup.tcl`) establishes general options for the Synopsys environment, including setting synthesis/STA options, defining naming conventions, and defining various settings specific to the process technology. Process-specific settings include, among other things, paths to the design libraries, names of design libraries, names of wire-load models, as well certain timing parameters such as PLL feedback skew and minimum clock period.

By default, synthesis and STA are run with worst case PVT conditions using the PHY mission rise-to-fall mode. The setup file includes variables that allow the user to run synthesis and STA for other PVT conditions and other PHY modes. It also allows the user to set the frequency for which to synthesize and time the design. Section 8.4.2 describes how to set these variables.

The setup file is reflective of Synopsys' standard flow and are sourced in the synthesis and STA scripts. It is recommended that the client utilize these files to replicate the synthesis and STA at their site for testing purposes. The client may choose to use their own established flows for the design of the final application, in this case please be aware to pass the appropriate variables down to the constraints file.

8.3.4 Timing Constraints File

The constraints file (`tcl/DWC_DDR3PHY_constr.tcl`) is used to constrain the design for synthesis and STA. It has four procedures that are called from the synthesis and STA scripts:

`ddr3phy_chip_clocks`: Defines the clock constraints for the chip. Some of these clock constraints are specific to the example chip design and are unrelated to the DDR3PHY, while others are required at the chip level to correctly constrain the DDR3PHY.

`ddr3phy_chip_constraints`: Defines the constraints for the example chip design. Some of these constraints are specific to the example chip design and are unrelated to the DDR3PHY, while others are required at the chip level to correctly constrain the DDR3PHY.

`ddr3phy_pub_constraints`: Defines the constraints for the DDR3PHY Utility Block (PUB). These are just bare minimum PUB constraints to correctly synthesize and time the example design. For a full set of PUB constraints, refer to the PUB installation.

`ddr3phy_constraints`: Defines a full set of PHY constraints.

The PHY constraints procedure (`ddr3phy_constraints`) can be used directly in the chip-level synthesis and STA by setting the variables for the PHY instance names and setting a few self-documenting variables as follows:

phy_inst: Set to the instance name of the DDR3PHY module instantiation in chip logic, like ${phy_top_inst}/u_DWC_DDR3PHY

ac_inst: Set to ${phy_inst}/${phy_ac_top}/u_DWC_DDR3PHYAC.

dx_inst: Set to ${phy_inst}/${phy_dx_top}/dx*u_DWC_DDR3PHYDATX8.

io_inst: Set to ${phy_inst}/*_top/*_io

phy_mode: Set to PHY mode as described in Section 8.4.2.

mctl_clk_period: Set to the controller clock period.

cfg_clk_period: Set to the configuration clock period.

sta: Set to 0 during synthesis and set to 1 during static timing analysis.

For examples of how these variables are set and used, refer to the example synthesis, STA, and constraints files described in Section 8.3.

8.4 Running Example Synthesis and STA

The Synopsys flow assumes the client does not have any `.synopsys_dc.setup` or `.synopsys_pt.setup` files in either their work directory or home directory. If these do exist, please temporarily disable them (i.e. rename them) when reproducing the results utilizing the Synopsys scripts to prevent potential conflicts.

8.4.1 Design Kit Installation

For the suggested design kit installation, refer to the DesignWare Cores DDR3 PHY Design Kit Installation Guide. Portions of this document assume the suggested installation has been followed.

If the IP is installed at directory `$IP_DIR`, then the following variables are used to point to specific PHY component directories. These variables are used in subsequent sections.

`$PHY_DIR: $IP_DIR/synopsys/ddr3_sdram/phy_top/current` (DDR3PHY directory)

`PUB: $IP_DIR/synopsys/ddr3_sdram/pub/current` (DDR3PHY PUB directory)

`$AC_DIR: $IP_DIR/synopsys/ddr3_sdram/ac/current` (DDR3PHYAC directory)

`$DX_DIR: $IP_DIR/synopsys/ddr3_sdram/datx8/current` (DDR3PHYDATX8 directory)

`$PLL_DIR: $IP_DIR/synopsys/ddr3_sdram/pll/current` (DDR3PHYPLL directory)

`$I/O_DIR: $IP_DIR/synopsys/ddr3_sdram/sstl/current` (DDR3PHY SSTL I/O directory)

The RTL files and synthesis/STA constraints and scripts for the example design are located in the PHY directory (`$PHY_DIR`).

8.4.2 Directory and Environment Setup

After installing the IP files:

1. Within your work area (`$WORK_DIR`), create three directories, `syn`, `sta` and `tcl`. These directories are used for synthesizing the IP, running STA, and holding scripts and constraints:

```
cd $WORK_DIR
mkdir syn
mkdir sta
mkdir tcl
```

2. Copy the setup and script files from the PHY directory. The setup files are used to specify the directories and the technology. Also copy the configuration file `DWC_DDR3PHY_chip_define.v`. These files are likely to require editing and are copied in the working area for convenience and to preserve the original copy in the build.

```
cp $PHY_DIR/example/sta/DWC_DDR3PHY_chip_sta.scr sta/.
cp $PHY_DIR/example/syn/DWC_DDR3PHY_chip_synth.scr syn/.
cp $PHY_DIR/rtl/DWC_DDR3PHY _define.v syn/.
cp $PHY_DIR/tcl/DWC_DDR3PHY_chip_setup.tcl tcl/.
cp $PHY_DIR/tcl/DWC_DDR3PHY_chip_constr.tcl tcl/.
chmod u+w sta/*
chmod u+w syn/*
chmod u+w tcl/*
```

3. Edit the set up file `DWC_DDR3PHY_chip_setup.tcl`. There are many self-documenting variables in the process file that may need to be set. The following describes the variables that may have to be set. Variables not listed here should not be modified.

tCTLCLK: Controller clock period. Set this to the controller clock period at which to synthesize the design. Valid values are described in the databook electrical specifications under the clock parameter t_{CTLCLK}. Default is set to the minimum clock period (i.e. maximum frequency) for which the IP is designed in the particular process.

tBYPCLK: PLL-bypass mode clock period. Default value is 10.

tATPGCLK: ATPG clock period. Default value is 10.

STD_CELL_DIR: Set to the directory where the target standard cells for synthesis are located.

PHY_UTILITY_BLOCK: Set to the RTL directory of the DDR3PHY Utility Block (PUB).

STD_CELL_LIBNAME_WC: Set to the standard cell library name for worst case conditions.

STD_CELL_LIBNAME_TC: Set to the standard cell library name for typical case conditions.

STD_CELL_LIBNAME_BC: Set to the standard cell library name for best case conditions.

PLL_LIBNAME_WC: Set to the PLL library name for worst case conditions.

PLL_LIBNAME_TC: Set to the PLL library name for typical case conditions.

PLL_LIBNAME_BC: Set to the PLL library name for best case conditions.

AC_LIBNAME_WC: Set to the AC macro library name for worst case conditions.

AC_LIBNAME_TC: Set to the AC macro library name for typical case conditions.

AC_LIBNAME_BC: Set to the AC macro library name for best case conditions.

DX_LIBNAME_WC: Set to the DATX8 macro library name for worst case conditions.

DX_LIBNAME_TC: Set to the DATX8 macro library name for typical case conditions.

DX_LIBNAME_BC: Set to the DATX8 macro library name for best case conditions.

IO_LIBNAME_WC: Set to the IO library name for worst case conditions.

IO_LIBNAME_TC: Set to the IO library name for typical case conditions.

STD_LIBNAME_BC: Set to the IO library name for best case conditions.

use_wireload_model: Set to 0 if not using wire load model. Default is 1.

WIRELOAD_MIN_NAME: Set to the minimum wire load model name.

WIRELOAD_MAX_NAME: Set to the maximum wire load model name.

max_wireload_model: Set to 1 if using maximum wire load. Otherwise, set to 0 (default value).

DRIVING_CELL_NAME: Set to the name of buffer used as input driver.

PVT: The operating conditions. Valid values are wc (worst case), bc (best case) or tc (typical case). Default is wc.

phy_mode: The operating mode of the PHY. Valid values are MISSION_RF, MISSION_RR and ATPG (ATPG test mode). Default is MISSION_RF.

- For PHY ATPG mode, the rr_mode port of PHY (DWC_DDR3PHY) needs to be set to 1 and this is done through tieing rr_mode to 1 inside of PUB."

pll_mode: Valid values are pll (when PLL is used), pll_bypass (when PLL is bypassed). Default value is pll.

Loopback_mode: Valid values are 1 (PHY loopback mode), 0 (No loopback). Default value is 0.

8.4.3 Running Synthesis

To run synthesis, go to the `syn` directory in your work area and run synthesis using Design Compiler as follows:

```
cd $WORK_DIR/syn
dc_shell-t –f DWC_DDR3PHY_chip_synth.scr | tee ../reports/syn/run.log
```

After the run, the log file and timing and design reports are created and put in the `../reports/syn` directory.

8.4.4 Running STA

To run STA, go to the `sta` directory in your work area and run STA using Prime Time as follows:

```
cd $WORK_DIR/sta
pt_shell –f DWC_DDR3PHY_chip_sta.scr | tee ../reports/sta/MISSION_RF run.log
```

After the run, the log file and timing and design reports are created and put in the `../reports/sta/MISSION_RF` directory. Synthesis must be run first before running STA. Note that minor hold-time violations may appear in the synthesis output. This is because hold time violations are not addressed until after placement, initial optimization, and clock-tree synthesis.

8.4.5 Messages

All messages produced by Synopsys scripts will contain the prefix `DDR_IP_INFO:` This makes it easier to differentiate between script messages and EDA tool messages.

9 Appendix – Implementation Checklist

9.1 Overview

This appendix provides a series of checks to should perform on the DDR PHY and I/O portion of the design database. Primarily intended as a check of the final design database before proceeding to mask creation (the point typically referred to as “tape-out” or “foundry tape-in”), refer to this checklist during the development stage to avoid leaving potential problems until very late in the chip development cycle.

The checklist provided here is not meant to be a complete list of items. The items in this list are topics that have been identified as having a higher probability of potential error, and are noted to ensure they are reviewed. Continue to perform all of the normal checks considered necessary in preparing a design for tape-out, in addition to what is contained in this document.

9.2 Checklist Information

Item	DDR4 multiPHY	Description
dont_touch nets	●	MVREF No buffering of this voltage reference net, which is used only for SSTL cells
dont_touch nets	●	MVREFSE No buffering of this voltage reference net, which is used only for SSTL cells
dont_touch nets	●	Signal bus: ZIOH No buffering of this high-voltage signal bus, which is used only for SSTL cells
dont_touch nets	●	LENH No buffering allowed of this latch enable net, which is used only for SSTL cells.
dont_touch nets	●	POCH No buffering allowed of this power-on clear net, which is used only for SSTL cells.
dont_touch nets	●	PDR18 No buffering allowed of this high-voltage signal, which is used only for SSTL cells.

Item	DDR4 multiPHY	Description
dont_touch nets	●	Signals between PHYAC/PHYDATX8 and SSTL No buffering or limited buffering of the signal nets passing between PHY blocks and SSTL (refer to Section 7.2 PHY Constraints) In some special cases, it may be necessary due to users design constraints to add some buffering. In this case, the user must contact Synopsys support to discuss the implementation plans.
ideal nets	●	Set ideal nets on shared nets between differential I/Os and DQS gate cells (DISE, DQSSE, and DQSBSE). These nets need to be routed by the tools. Routing channels are built into the SSTL cells to allow for this routing to be efficiently accomplished. ASIC tools should not buffer these signals
ideal nets	●	Set ideal nets on shared nets between differential I/Os (DFI, DFO). These nets may need to be routed by the tools if the two I/O cells are not abutting. The abutment of these two cells is dependent on the pad frame design. Routing channels are built into all of the ITM cells to allow for this routing to be efficiently accomplished if required. ASIC tools should not buffer these signals.
no_route nets	●	MVREF Normally no routing is required on this net as it is connected by abutment. There may be special SSTL ports where routing is required on this net. Check your databook and physical views to confirm if routing is required by your specific port or not.
no_route nets	●	MVREFSE No routing is required on this net as it is connected by abutment.
no_route nets	●	signal bus: ZIOH Normally no routing is required on this signal bus as it is connected by abutment. There may be special SSTL ports where routing is required on this bus. Check your databook and physical views to confirm if routing is required by your specific port or not.
no_route nets	●	PLL ddr_clk ; ctl_clk ; No routing is required on these PLL nets as they are connected by abutment.

Item	DDR4 multiPHY	Description
multi-driven nets	●	A multi-driven net on the SSTL cell “PVREF” ZIOH bus and MVREF outputs will be encountered when more than one PVREF cell is instantiated in the interface. This is allowed. When there are two or more PVREF SSTL cells instantiated in the SDRAM interface, the outputs of these cells connect to the same ZIOH bus and MVREF nets (which are embedded within the SSTL cell layouts and connected by abutment) to create multi-driven nets.
multi-driven nets	●	A multi-driven net on the SSTL cell “PVREF” ZIOH bus and MVREFSE outputs will be encountered when more than one PVREF cell is instantiated in the interface. This is allowed. When there are two or more PVREF SSTL cells instantiated in the SDRAM interface, the outputs of these cells connect to the same ZIOH bus and MVREFSE nets (which are embedded within the SSTL cell layouts and connected by abutment) to create multi-driven nets.
abutment	●	The PLL, if used, must be abutted to the AC and/or DATX8. This ensures the PLL/AC/DATX8 interface will perform as intended.
signal association	●	The DQ and DM need to be kept associated with their respective DQS signal. For example, in a 16-bit system there is DQ[15:0] and DQS[1:0]. DQ[7:0] should be kept together with DQS[0]. It is not acceptable to have, for example, DQ[4] being sampled with DQS[1].
PLL supply	●	vdd_pll Minimize routing resistance for lowest IR drop and EM compliance. Refer to supply routing guideline in Implementation Guide.
analog signal	●	pll_ato No buffering of this analog signal, which is to be connected to SSTL analog signal cell (or left floating if you choose not to have test access to this signal) Suggested routing this line using wire width of 4x minimum width wire (Mx). Refer foundry design rule document for any additional spacing and width requirements for analog high voltage nets.
analog signal	●	pll_analog_test_out (ATO) spacing requirement is technology rule dependent since it is considered a high-voltage signal.

Item	DDR4 multiPHY	Description
timing	●	Reference clock skew. Clock tree skew between clock input pins (ctl_clk) of all the PHY blocks should be less than or equal to the value as specified in the Implementation Guide.
timing	●	Match PHY/SSTL interface routing delays. The delay of all timing-critical signals connecting between the PHY blocks (PHYAC, PHYDATX8) and the SSTL I/Os should be matched within the interval as specified in the Implementation Guide across all PHY blocks (the entire interface). Critical signals include all ADDR/CMD/CLK (output only), all DQ/DM/DQS (input and output), and the DQ/DM/DQS output enable signals. **Note:** The path delays for these signals between PHY and SSTL should be measured and verified. **Note:** To implement at speed loopback, the IO->AC skew must be controlled.
timing	●	Do not violate PHY/SSTL interface maximum capacitance ("max_cap") constraints. The PHY blocks and SSTL I/O cells have been carefully characterized to provide the maximum allowable max_cap parameters in the .lib/.db files for the timing-critical signals passing between PHY and SSTL. Violating these values will not permit the interface to operate as intended.
timing	●	PLL jitter margin. At the chip-level, the STA timing constraints should be setup with an allowance for the embedded or abutting PLL output jitter for timing paths between controller and PHY block (PHYAC, PHYDATX8). As an example, if we assume the embedded or abutting PLL output jitter is +/-100ps, then the jitter allowance between controller and PHY should be 100ps on setup timing and 100ps on hold timing.
timing	●	PLL phase error margin. At the chip-level, the STA timing constraints should be setup with an allowance for the embedded or abutting PLL delay compensation phase error for timing paths between controller and PHY block (PHYAC, PHYDATX8). As an example, if we assume the embedded or abutting PLL phase error is +/-100ps, then the phase error timing allowance between controller and PHY should be 100ps on setup timing and 100ps on hold timing.
timing	●	Signal transition times between AC and SSTL I/O, and DATX8 and SSTL I/O must be <= 150ps

Item	DDR4 multiPHY	Description
SSTL impedance PVT update	●	Impedance control groups. In some situations, you may wish to break the interface into more than one group for SSTL automatic PVT updating. If this is the case, the impedance control bus ZIOH should not be connected together between the separated groups. The impedance controller (zctrl) has multiple code registers for each of the various impedance control groups.The impedance controller is a configuration option of the PUB / PUBL for the PHYs. This same requirement applies also to multiple separate interfaces on the same die.
SSTL impedance PVT update	●	Impedance control bus connectivity. The SSTL impedance control is driven from the PUB/PUBL/PUBM2 logic to the PVREF SSTL cells, where it is decoded, level shifted, and then driven out as the ZIOH bus, which is embedded within the SSTL cells. It is common to have more than one PVREF cell in the interface, creating a multi-driven net on ZIOH bus. You must ensure that the connectivity from the impedance control logic 'zctrl' (embedded within PUB / PUBL) to the PVREF cells is correct, and is the same connection for every PVREF cell in an impedance control group.
ESD	●	The I/O cells related to this IP will normally exist in the chip with other I/O cells being implemented by the user for other chip functions. The common ESD reference for these Synopsys DDR products is the core ground (such as, VSS or MVSS). You must ensure there is an ESD discharge path available between the core ground of these Synopsys I/Os and whatever the ESD reference is for the other IO cells used on their chip.
die pad frame	●	Must review the application note Guidelines for Implementing Signaling Environments for DDRn Interfaces: PCB, Package, Power, and Timing Budgets prior to tape out. This document contains information on die pad frame design.
package	●	Must review the application note Guidelines for Implementing Signaling Environments for DDRn Interfaces: PCB, Package, Power, and Timing Budgets prior to tape out and prior to package design signoff. Package design has a direct impact on the performance of the IP and the DDR subsystem.

Item	DDR4 multiPHY	Description
PCB	●	Must review the application note Guidelines for Implementing Signaling Environments for DDRn Interfaces: PCB, Package, Power, and Timing Budgets prior to tape out and prior to PCB design signoff. PCB design has a direct impact on the performance of the DDR subsystem.
Signal and Power integrity	●	It is required to perform a SPICE-level signal and power integrity analysis of the entire memory sub-system including die, package, PCB, and external memory configuration. This analysis is to be run for each intended configuration and combination of die, package, pcb, and external memory configuration when more than one configuration or combination is to be used. It is strongly recommended to provide the signal and power integrity report to Synopsys for visual review. Customers should expect uncertainty in the operation of the memory channel if a detailed signal and power integrity analysis has not been performed.
PHY / memory controller interface	●	When connecting to a 3rd-party controller, the preferred method of connecting to the PHY is through the DFI interface of the PHY Utility Blocks (PUB, PUBL or PUBM2). The DFI interface will manage most of the interfacing requirements for the PHY-controller interface. The PUB/PUBL/PUBM2 DFI interface is user-configurable, allowing variation in 3rd-party controller DFI interface requirements. When connecting to a 3rd-party controller and not using the PUB/PUBL/PUBM2, extreme caution must be exercised when interfacing the PHY product from one supplier with the memory controller product of a different supplier to ensure all the requirements of the PHY are properly addressed by the controller. If not using the PUB/PUBL/PUBM2 when connecting the PHY to a 3rd-party controller, the customer must contact Synopsys to discuss what is required from the controller.
equivalency checking	●	When performing equivalency checking, the user should treat all the PHY components (including IO cells) as black-boxes. This will force the equivalency tools to ensure the various PHY components are properly connected. If the user did not do this, the tools may incorrectly allow some transformation of the connections around the PHY based on logic equivalence that in some cases will result in an incorrect implementation.

Item	DDR4 multiPHY	Description
design for test	●	The PHY solution provides digital test output signals (DTO) for test purposes. The user must understand the required bandwidth of these signals; normally it is equal to the maximum operating clock frequency of the memory controller. The bandwidth of the paths for these DTO signals (logic, buffering, and IO cells) must be capable of supporting the speed of the DTO signals.
timing / design for test	●	The PHY may be provided with either a lib/db file that contains the relevant timing arcs for both mission mode and test (PLL bypass) mode depending on the value of an input pin, or the PHY may be provided with specific lib/db files for mission mode and test (PLL bypass) mode separately. User must review the lib/db files provided with the PHY design kit to ensure the correct lib/db file is being used for the timing analysis of each mode.
design for test	●	The PHY has requirements that specific input signals be fixed to specific states for logic scan testing, and possibly for other test modes also. The user must review the 'Design For Test' section of the PUB databook and follow the input signal state requirements. If there are any questions about these requirements, please contact Synopsys.
design for test	●	The PHY is supported by a PHY Utility Block (PUB/PUBM2) which may be implemented by the user directly or it may be contained within certain revisions of the Synopsys memory controllers. Either stand-alone or embedded in a memory controller, there will be an input pin to signal test mode, scan mode, or atpg mode (the name may vary between implementations). This signal must be asserted when performing logic scan testing of the RTL logic or of the PHY. This input will ensure the RTL logic is in the proper state for scan testing, and will also ensure the IO cells are driven to a fixed nominal impedance state suitable for PHY scan testing or for general chip test purposes.