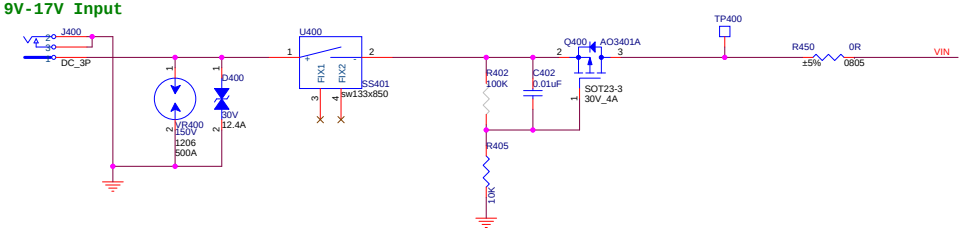
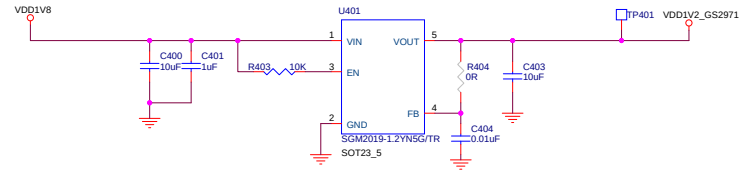
POWER INPUT

9V-17V Input

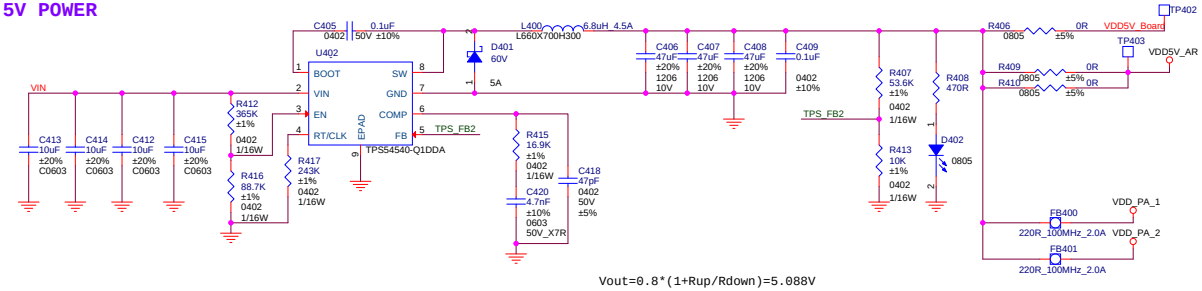


1.2V For SKY MODE



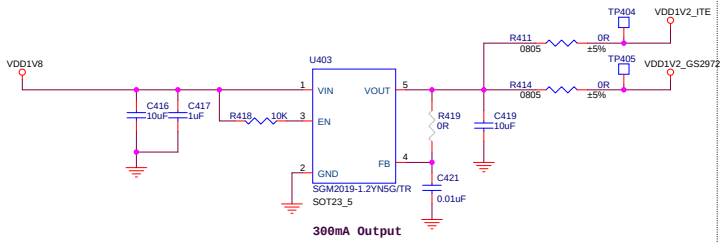
300mA Output

5V POWER



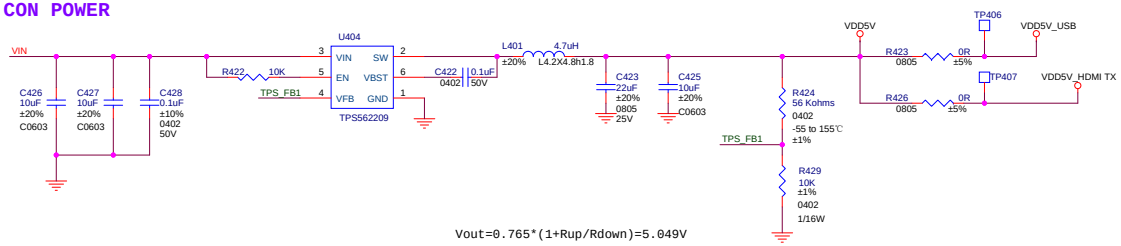
Vout=0.8*(1+Rup/Rdown)=5.088V

1.2V For Ground MODE



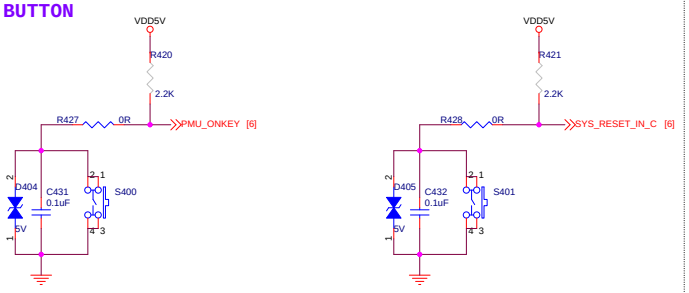
300mA Output

5V CON POWER

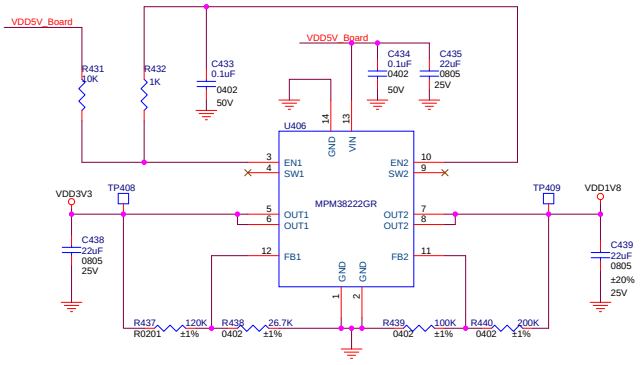


Vout=0.765*(1+Rup/Rdown)=5.049V

RESET BUTTON



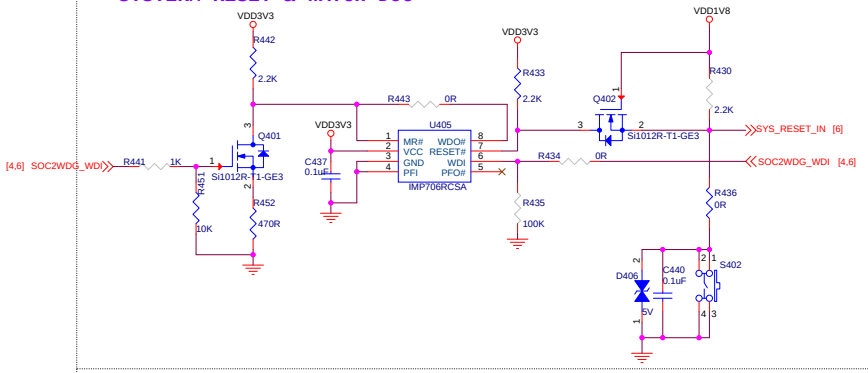
3.3V & 1.8V Power Supply



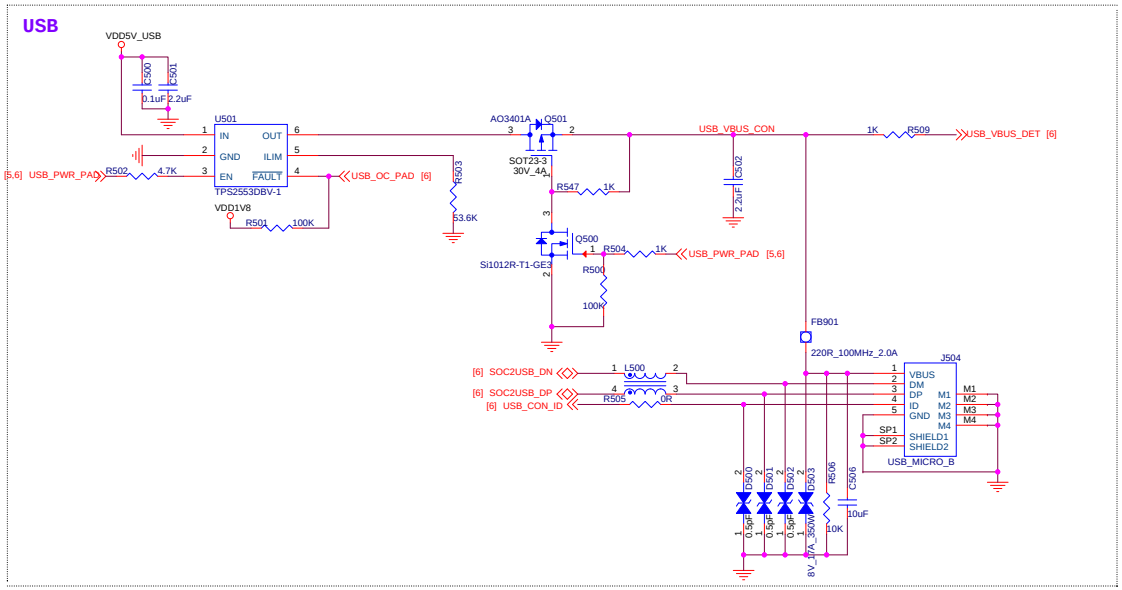
Vout=0.608*(1+Rup/Rdown)=3.340V

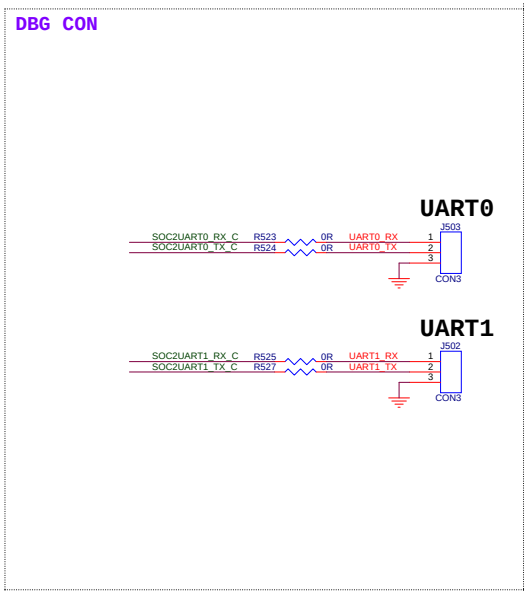
Vout=0.608*(1+Rup/Rdown)=1.824V

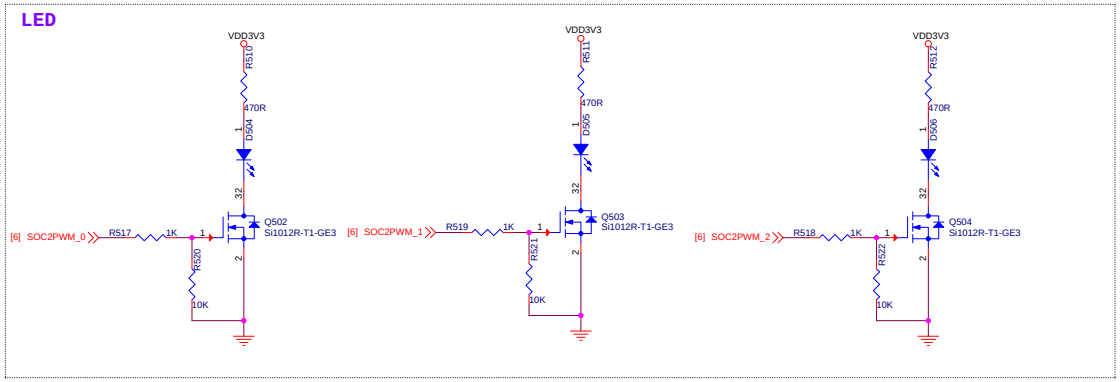
SYSTERM RESET & WATCH DOG

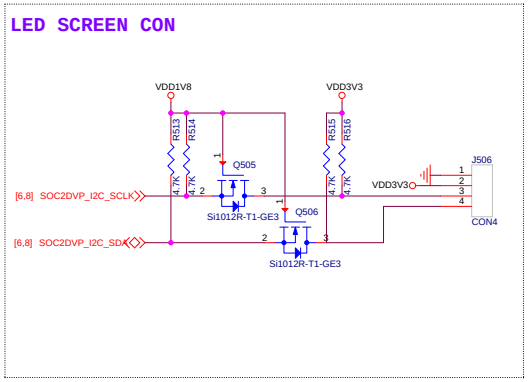


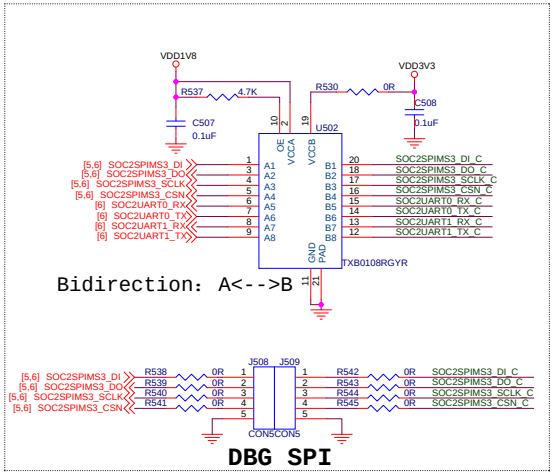
artosyn ARTOSYN CONFIDENTIAL		
Designed by Wuping Wang	Project Name AR_LD_INTERFACE	Rev 1.0.0
Date 2018.02.28	Size C	Page Title P04_POWER&RST
Dept: R&D, ARTOSYN		Sheet [4] of [11]

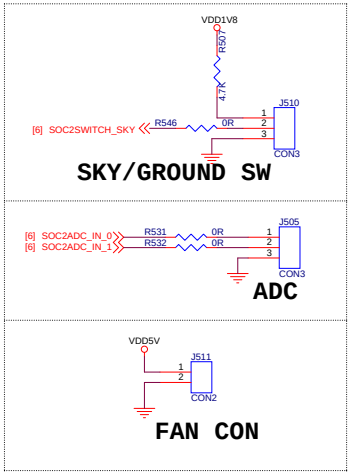


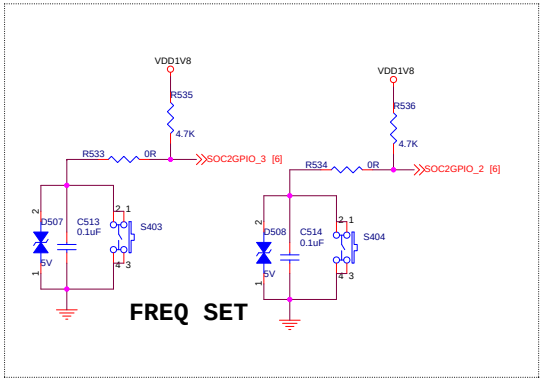


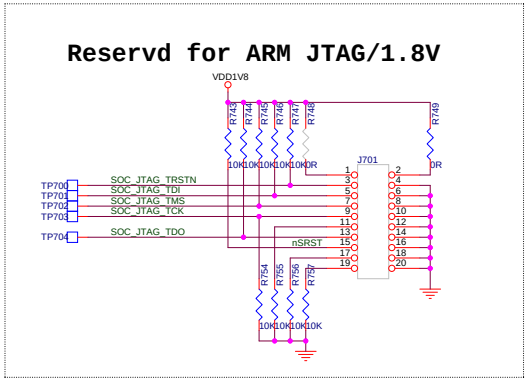






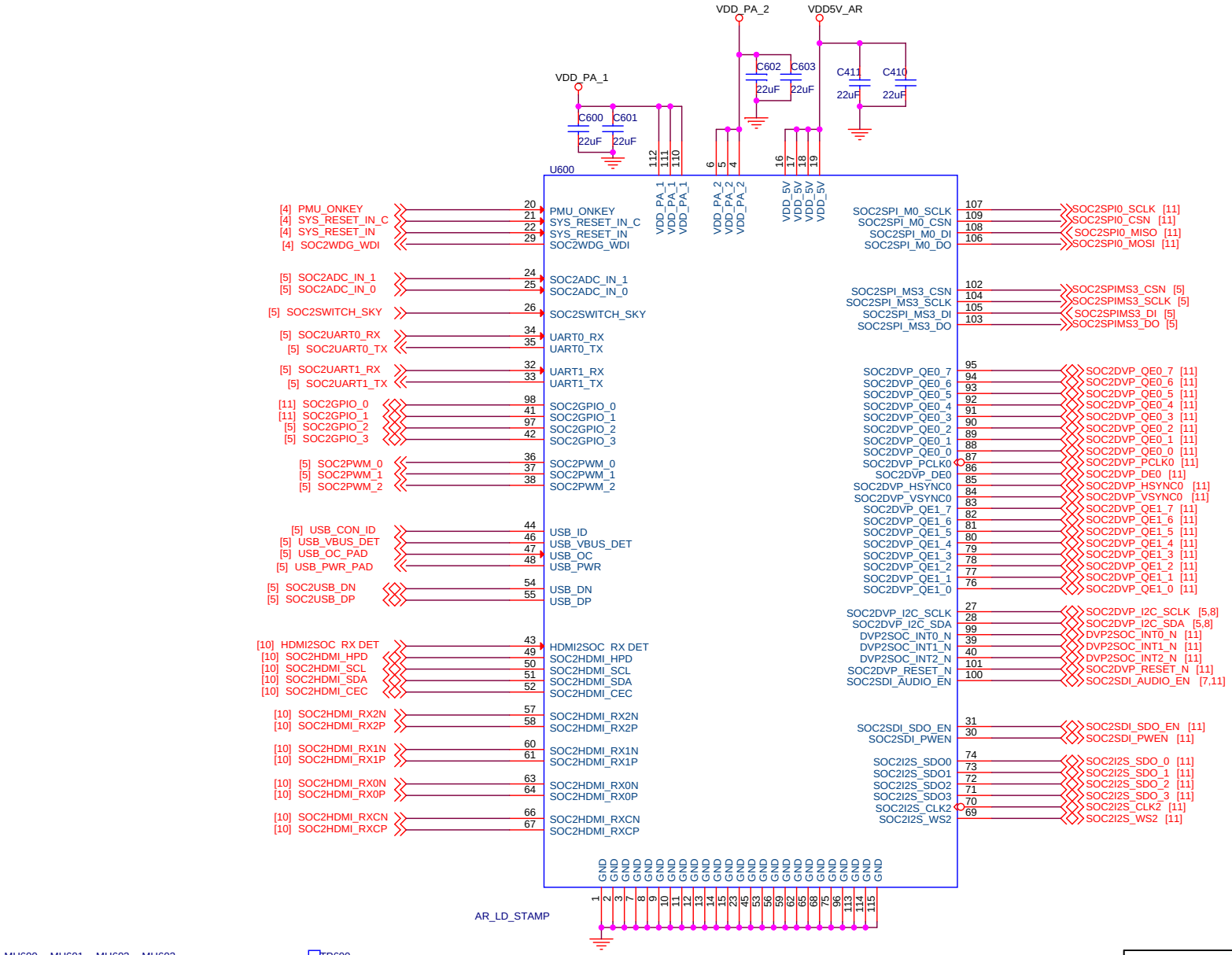






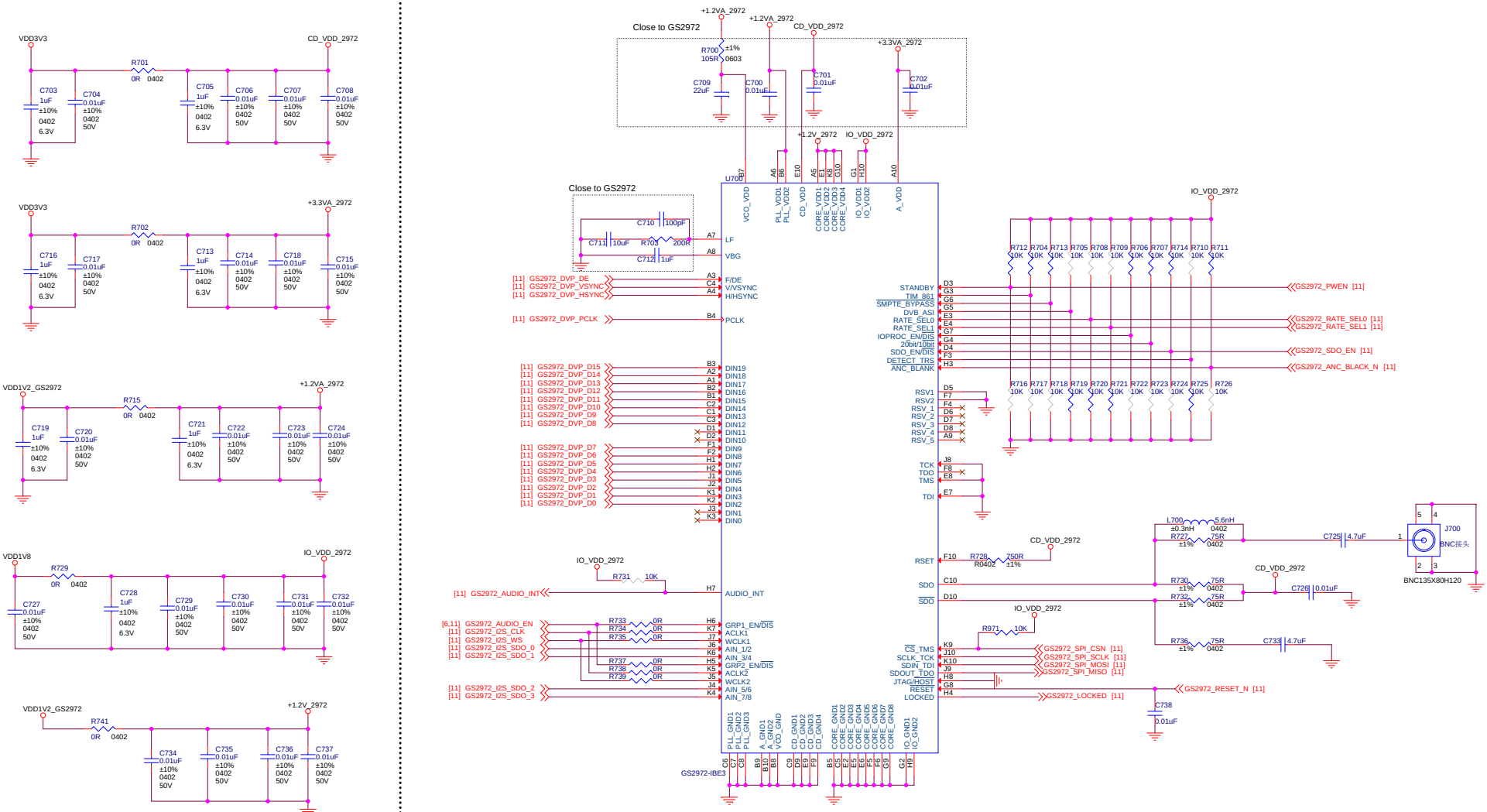
ARTOSYN CONFIDENTIAL

Designed by Wuping Wang	Project Name AR_LD_INTERFACE	Rev 1.0.0
Date 2018.02.28	Size C	Page Title P06_Sirius_Power2
Dept: R&D, ARTOSYN		Sheet [5] of [11]



artosyn **ARTOSYN CONFIDENTIAL**

Designed by Wuping Wang	Project Name AR_LD_INTERFACE	Rev 1.0.0
Date 2018.02.28	Size B	Page Title P06_AR_LD_MOUDLE
Dept: R&D, ARTOSYN		Sheet 6 of 11



MODE	20bit/10bit	SMPTE_BYPASS	DVB_ASI	STANDBY
SMPTE/20bit mode	1	1	0	\
data through/20bit mode	1	0	0	\
SMPTE/10bit mode	0	1	0	\
data through/10bit mode	0	0	0	\
DVB-ASI/10bit mode	0	0	1	\
STANDBY	\	\	\	1(POWER DOWN)

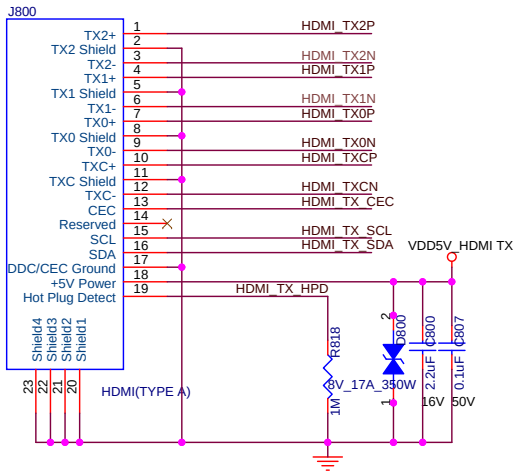
MODE	TIM_861	DETECT_TRS
DE/HSYNC/VSYNC	1	0
F/H/V	0	0
DETECT_TRS	1	1

RATE_SEL0	RATE_SEL1	Data Rate
0	0	1.485 or 1.485/1.001Gb/s
0	1	2.97 or 2.97/1.001Gb/s
1	X	270Mb/s

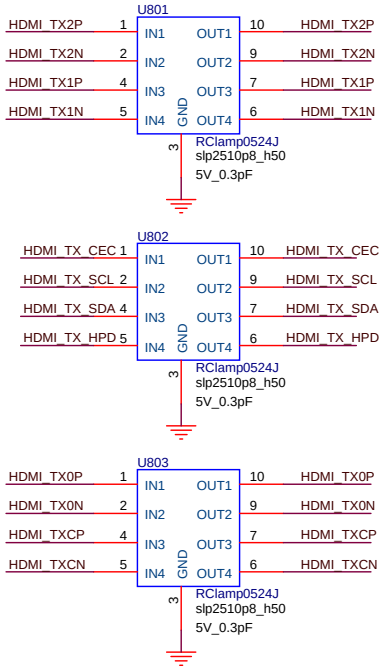
artosyn ARTOSYN CONFIDENTIAL

Designed by Wuping Wang	Project Name AR_LD_INTERFACE	Rev 1.0.0
Date 2018.02.28	Size C	Page Title P07_GROUND GS2972
Dept: R&D, ARTOSYN		Sheet [7] of [11]

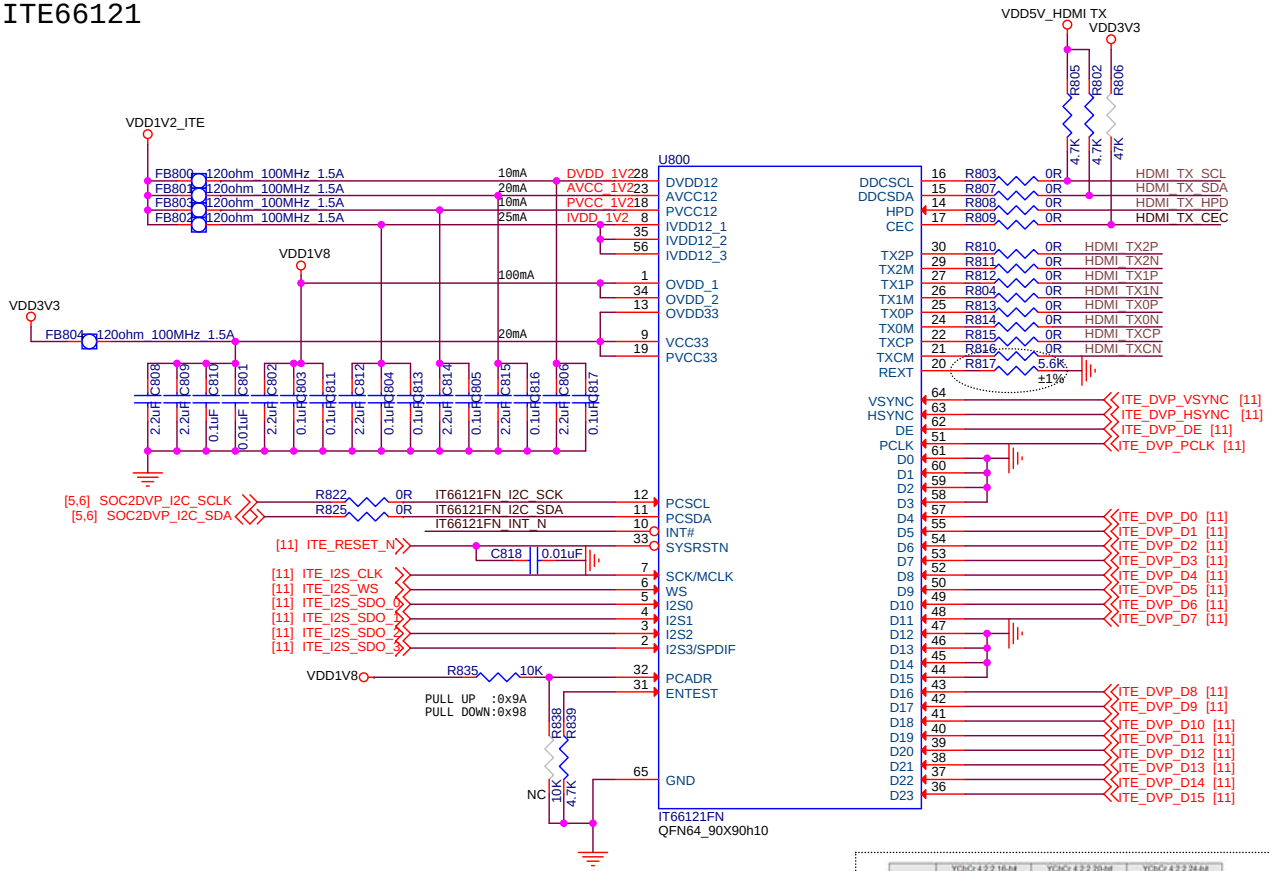
HDMI TX Connect



HDMI ESD



ITE66121



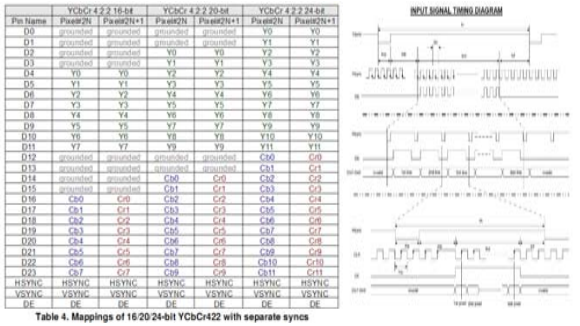
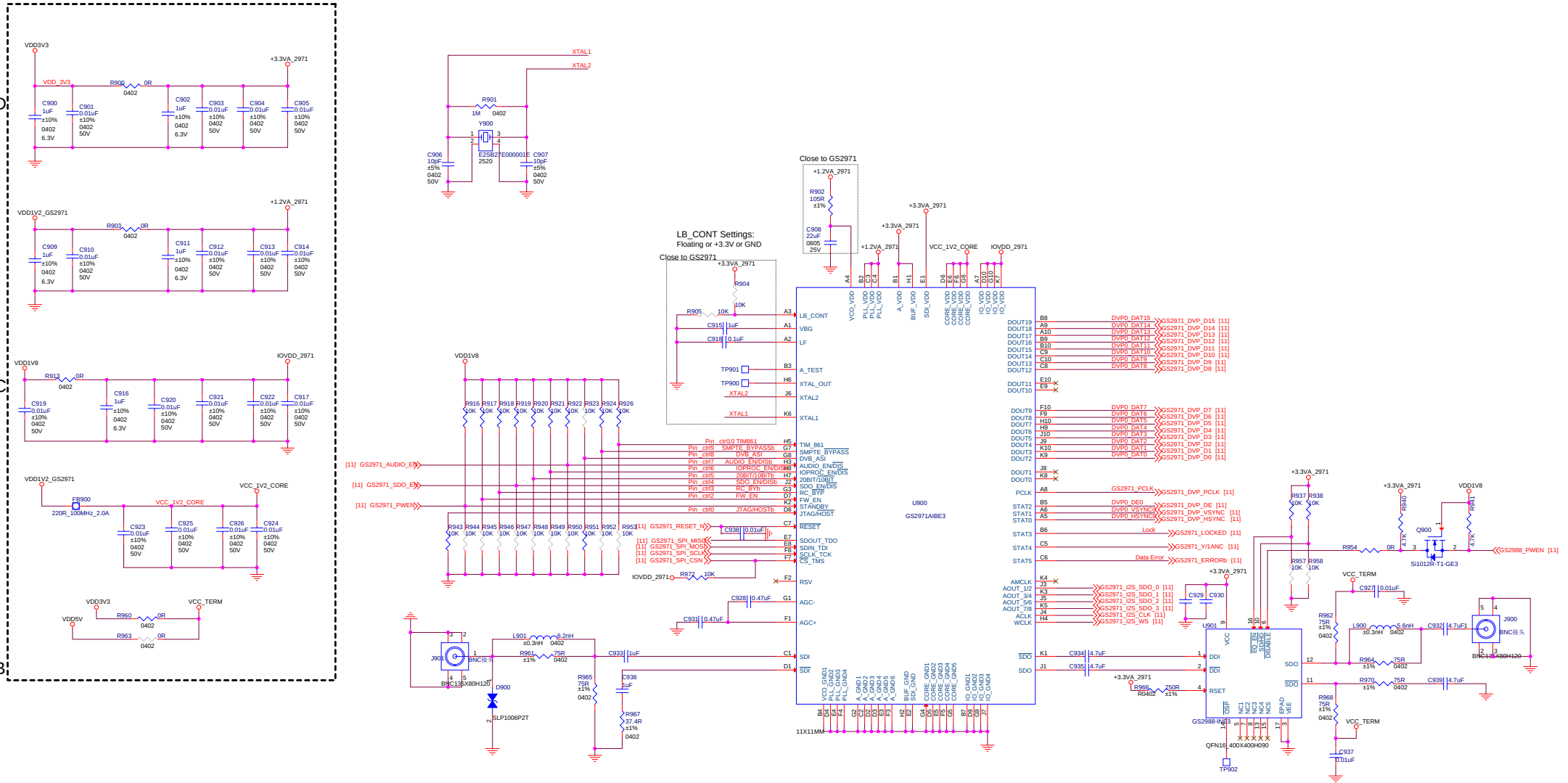


Table 4. Mappings of 16/20/24-bit YCbCr422 with separate syncs

ARTOSYN CONFIDENTIAL

Designed by Wuping Wang	Project Name AR_LD_INTERFACE	Rev 1.0.0
Date 2018.02.28	Size B	Page Title P08_GROUND_HDMI_TX_IT66121
Dept: R&D, ARTOSYN		Sheet 8 of 11



MODE	20bit/10bit	SMPTE_BYPASS	DVB_ASI	STANDBY
SMPTE/20bit mode	1	1	0	\
data through/20bit mode	1	0	0	\
SMPTE/10bit mode	0	1	0	\
data through/10bit mode	0	0	0	\
DVB-ASI/10bit mode	0	0	1	\
STANDBY	\	\	\	1(POWER DOWN)

Notes:

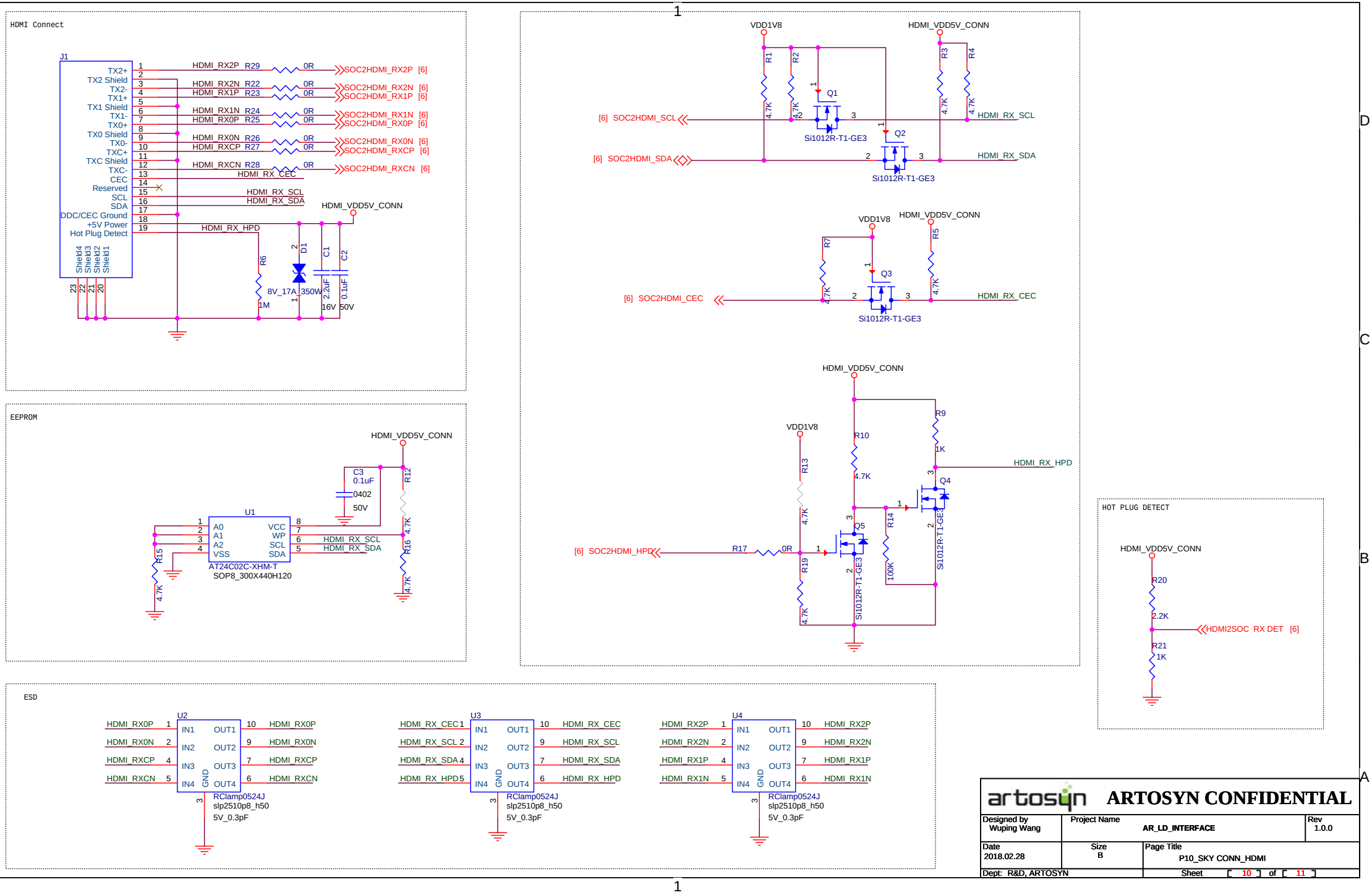
1. This board is GS2960/1 compatible;
2. DNP(Do Not Populate);
3. Power consumption:

Device	+1.2V	+3.3V
GS2970_1	217	75
GS2974	0	65
GS2978	0	51
Total	217mA	191mA

4. SQT and TMM series connectors are rated for 3A from 20C-80C, with operation temp range of -65-+125C
5. IOVDD_2970 can be +3.3v, which is supplied by this board through a 1-ohm jumper, or different voltage supplied by the output board connected to it, in which case the 1-ohm jumper shall be removed;
6. The value of the serial resistors on video output port will be determined by board signal integrity test;
7. Use BNC ground as the ground test points;
8. Lable the connectors, LEDs, DIP switches and jumpers. Lable some critical signals on the connectors;
9. Minimum of 3x trace width spacing for GS2970_DOUT10~19, GS2970_PCLK;
10. Analog power and ground isolation(refer to PCB layout guide).
11. Critital 3G signal layout(refer to PCB layout guide);
12. Impedance controlled signals(refer to PCB layout guide).
13. Via size test points should be as close as possible to the pins;

ARTOSYN CONFIDENTIAL

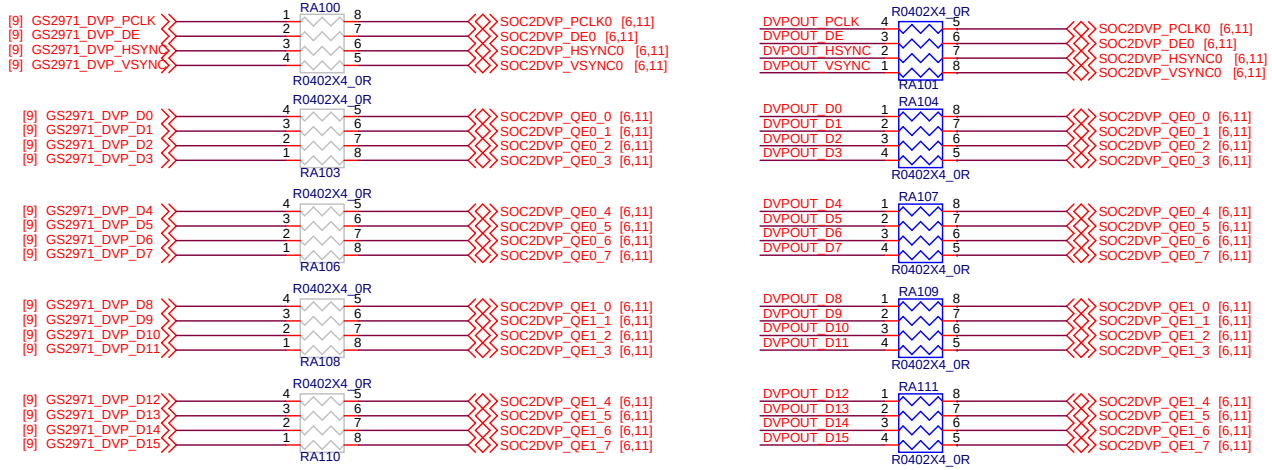
Designed by Wuping Wang	Project Name AR_LD_INTERFACE	Rev 1.0.0
Date 2018.02.28	Size A2	Page Title P09 SKY HDSDI GS2971
Dept: R&D, ARTOSYN		Sheet [9] of [11]



artosyn ARTOSYN CONFIDENTIAL		
Designed by Wuping Wang	Project Name AR_LD_INTERFACE	Rev 1.0.0
Date 2018.02.28	Size B	Page Title P10_SKY CONN_HDMI
Dept: R&D, ARTOSYN		Sheet 10 of 11

DVP INOUT

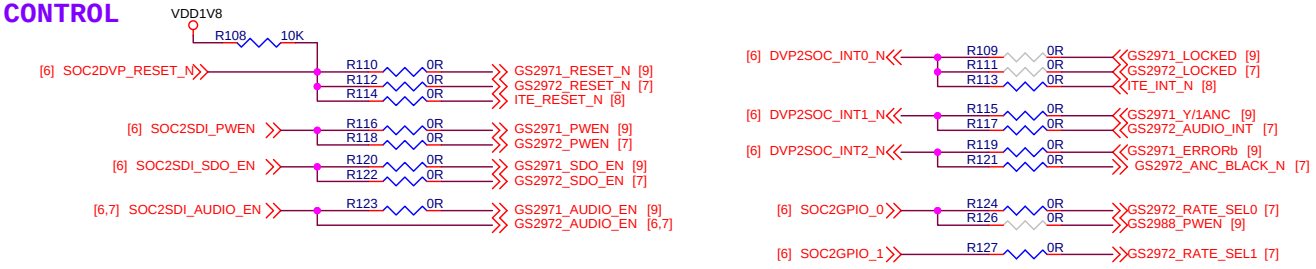
place the RA100/RA103/RA106/RA108/RA110, disable RA101/RA104/RA107/RA109/RA111 when using the SKY Mode;
place the RA101/RA104/RA107/RA109/RA111, disable RA100/RA103/RA106/RA108/RA110 when using the Ground Mode;



DVP OUTPUT

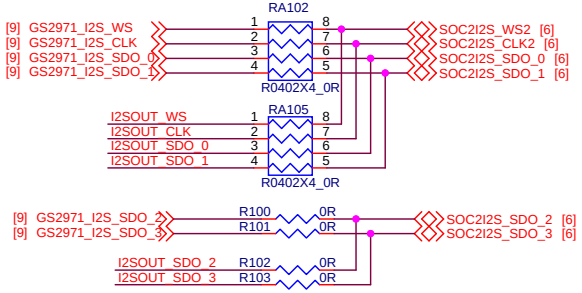
place the RA114/RA116/RA118/RA121/RA123, disable RA115/RA117/RA119/RA122/RA124 when using the GS2972;
place the RA115/RA117/RA119/RA122/RA124, disable RA114/RA116/RA118/RA121/RA123 when using the ITE66121;

CONTROL



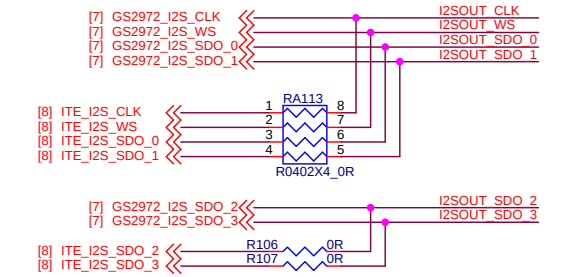
I2S INPUT

place the RA102/R100/R101, disable RA105/R102/R103 when using the SKY Mode;
place the RA105/R102/R103, disable RA102/R100/R101when using the Ground Mode;

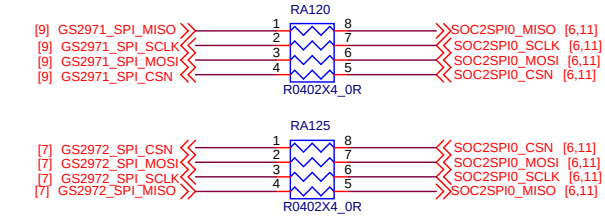


I2S OUTPUT

place the RA112/R104/R106, disable RA113/R106/R107 when using the GS2972;
place the RA113/R106/R107, disable RA112/R104/R106 when using the GS2972;



SPI



ARTOSYN CONFIDENTIAL

Designed by Wuping Wang	Project Name AR_LD_INTERFACE	Rev 1.0.0
Date 2018.02.28	Size B	Page Title P11 DVP&I2S PIN SHARE
Dept: R&D, ARTOSYN		Sheet [11] of [11]