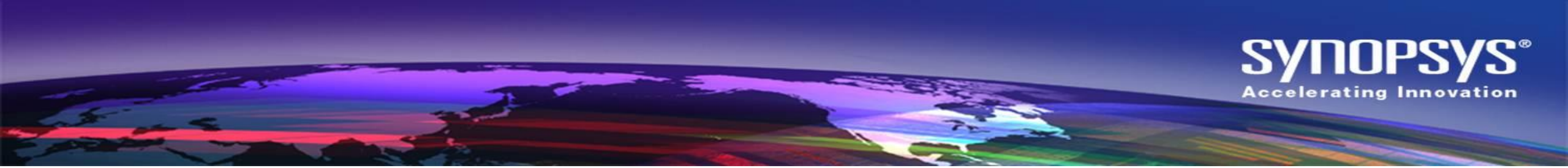


Artosyn Inc

DDR IO ring review report

JIANGWAN2

2017, June 7th

Outline

- IO ring capacitance analysis
- IO ring overview
- Floating rails
- PDIFF cell analysis
- Calibration pair analysis
- Power/ground distribution analysis
- DDR4 functionality

IO ring capacitance analysis
TSMC28HPC18

- IO cells decoupling capacitance per section, per rail pair

Total cap [pF]	DBYTE0	DBYTE1	DBYTE2	DBYTE3	DBYTE4	DBYTE5	DBYTE6	DBYTE7	PHY_AC
MVDDQ – MVSSQ	464.29	478.99	491.33	483.71	491.33	478.99	491.33	478.99	1800.56
MVDD – MVSS	36.41	35.51	37.31	36.00	37.45	35.65	37.45	35.65	110.99
MVREF – MVSSQ	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MVREF – MVDDQ	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MVSS–MVAA_PLL	37.04	23.29	37.04	23.29	37.04	23.29	37.04	23.29	71.94

- SnapCap decoupling capacitance per section, per rail pair

Total cap [pF]	DBYTE0	DBYTE1	DBYTE2	DBYTE3	DBYTE4	DBYTE5	DBYTE6	DBYTE7	PHY_AC
MVDDQ – MVSSQ	361.08	350.46	371.70	361.08	371.70	350.46	371.70	350.46	1040.76
MVDD – MVSS	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MVREF – MVSSQ	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MVREF – MVDDQ	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MVSS–MVAA_PLL	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

- IO cells decoupling capacitance per section, per rail pair

Total cap [pF]	DBYTE0	DBYTE1	DBYTE2	DBYTE3	DBYTE4	DBYTE5	DBYTE6	DBYTE7	PHY_AC
MVDDQ – MVSSQ	825.37	829.45	863.03	844.79	863.03	829.45	863.03	829.45	2841.32
MVDD – MVSS	36.41	35.51	37.31	36.00	37.45	35.65	37.45	35.65	110.99
MVREF – MVSSQ	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MVREF – MVDDQ	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
MVSS–MVAA_PLL	37.04	23.29	37.04	23.29	37.04	23.29	37.04	23.29	71.94

IO ring overview
Used cells

- List of used cells in the IO ring

	Sections								
Unique used cell list (sorted)	DBYTE0	DBYTE1	DBYTE2	DBYTE3	DBYTE4	DBYTE5	DBYTE6	DBYTE7	PHY_AC
DWC_D4MV_PAIO_EW	0	0	0	0	0	0	0	0	1
DWC_D4MV_PCKE_EW	0	0	0	0	0	0	0	0	3
DWC_D4MV_PCORNER	0	0	0	0	0	0	0	0	1
DWC_D4MV_PDDRIO_EW	9	9	9	9	0	0	0	0	33
DWC_D4MV_PDDRIO_NS	0	0	0	0	9	9	9	9	0
DWC_D4MV_PDIFF_EW	2	2	2	2	0	0	0	0	0
DWC_D4MV_PDIFF_NS	0	0	0	0	2	2	2	2	0
DWC_D4MV_PDQSG_VSSQ_EW	1	1	1	1	0	0	0	0	0
DWC_D4MV_PDQSG_VSSQ_NS	0	0	0	0	1	1	1	1	0
DWC_D4MV_PEND_EW	1	0	0	0	0	0	0	1	0
DWC_D4MV_PRETPOCC_EW	0	0	0	0	0	0	0	0	1
DWC_D4MV_PVAA_PLL_EW	2	1	2	1	0	0	0	0	3
DWC_D4MV_PVAA_PLL_NS	0	0	0	0	2	1	2	1	0
DWC_D4MV_PVDDQ_CAP_EW	4	5	4	5	0	0	0	0	13
DWC_D4MV_PVDDQ_CAP_NS	0	0	0	0	4	5	4	5	0
DWC_D4MV_PVDDQ_ESD_EW	3	2	3	2	0	0	0	0	9
DWC_D4MV_PVDDQ_ESD_NS	0	0	0	0	3	2	3	2	0
DWC_D4MV_PVDD_CAP_EW	1	1	1	1	0	0	0	0	2
DWC_D4MV_PVDD_CAP_NS	0	0	0	0	1	1	1	1	0
DWC_D4MV_PVDD_ESD_EW	1	1	1	1	0	0	0	0	2
DWC_D4MV_PVDD_ESD_NS	0	0	0	0	1	1	1	1	0
DWC_D4MV_PVREFE_EW	0	0	0	1	0	0	0	0	1
DWC_D4MV_PVREF_DAC_EW	1	1	1	1	0	0	0	0	0
DWC_D4MV_PVREF_DAC_NS	0	0	0	0	1	1	1	1	0
DWC_D4MV_PVREF_EW	1	1	1	1	0	0	0	0	1
DWC_D4MV_PVREF_NS	0	0	0	0	1	1	1	1	0
DWC_D4MV_PVSSQ_EW	6	6	6	6	0	0	0	0	21
DWC_D4MV_PVSSQ_NS	0	0	0	0	6	6	6	6	0
DWC_D4MV_PVSSZB_ZQ_EW	0	1	1	1	0	0	0	0	1
DWC_D4MV_PVSSZB_ZQ_NS	0	0	0	0	1	1	1	1	0
DWC_D4MV_PVSS_CAP_EW	2	1	2	1	0	0	0	0	4
DWC_D4MV_PVSS_CAP_NS	0	0	0	0	2	1	2	1	0
DWC_D4MV_PVSS_ESD_EW	1	1	1	1	0	0	0	0	1
DWC_D4MV_PVSS_ESD_NS	0	0	0	0	1	1	1	1	0
DWC_D4MV_PZCTRL_EW	0	0	0	0	0	0	0	0	1
DWC_D4MV_PZQ_EW	0	0	0	0	0	0	0	0	1
Total	35	33	35	34	35	33	35	34	99

IO ring overview
Cells by category

- Number of cells by section, by category

Cell category	DBYTE0	DBYTE1	DBYTE2	DBYTE3	DBYTE4	DBYTE5	DBYTE6	DBYTE7	PHY_AC	Total
IO	11	11	11	11	11	11	11	11	33	**121**
PDIFF	2	2	2	2	2	2	2	2	0	**16**
Special IO	0	0	0	0	0	0	0	0	3	**3**
VDDQ	7	7	7	7	7	7	7	7	22	**78**
VSSQ	7	7	7	7	7	7	7	7	22	**78**
VDD	2	2	2	2	2	2	2	2	4	**20**
VSS	3	3	4	3	4	3	4	3	6	**33**
VAA_PLL	2	1	2	1	2	1	2	1	3	**15**
VREFI	2	2	2	2	2	2	2	2	1	**17**
VREFE	0	0	0	1	0	0	0	0	1	**2**
Calibration	0	0	0	0	0	0	0	0	2	**2**
PDQSG_VSSQ	1	1	1	1	1	1	1	1	0	**8**
Fillers	0	0	0	0	0	0	0	0	0	**0**
POC	0	0	0	0	0	0	0	0	1	**1**
Analog	0	0	0	0	0	0	0	0	1	**1**
End	1	0	0	0	0	0	0	1	0	**2**
Uncategorized cells	0	0	0	0	0	0	0	0	1	

IO ring overview

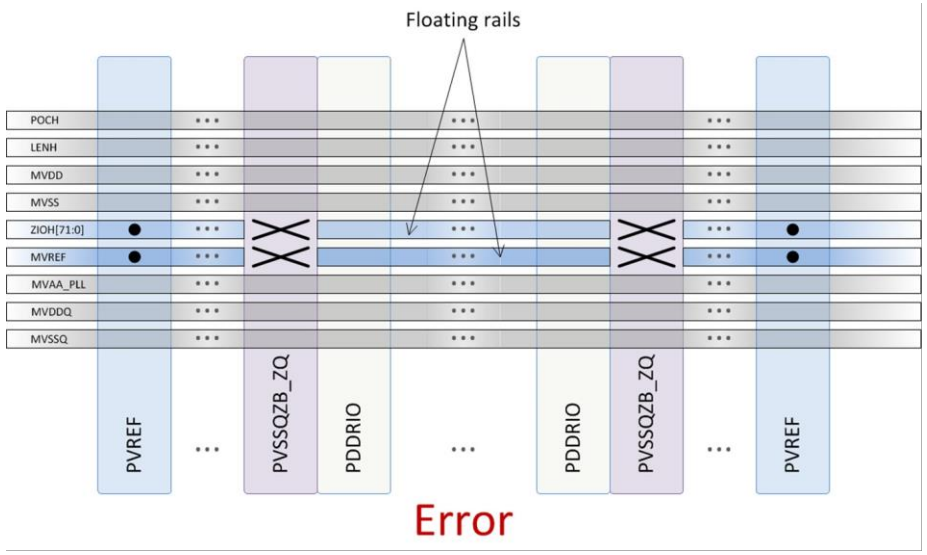
Power cells

- The following table contains the S:P:G for IO supply domain
- The S:P:G ratios always need to be analyzed according to SNPS guidelines stated in DDRn_Package_PCB_Guidelines, for the actual interface configuration
- Core domain S:P:G are also presented just for convenience

Ratio	DBYTE0	DBYTE1	DBYTE2	DBYTE3	DBYTE4	DBYTE5	DBYTE6	DBYTE7	PHY_AC	Total
IO supply: S:P	1.57	1.57	1.57	1.57	1.57	1.57	1.57	1.57	1.50	**1.55**
IO supply: S:G	1.57	1.57	1.57	1.57	1.57	1.57	1.57	1.57	1.50	**1.55**
Core supply: S:P	5.50	5.50	5.50	5.50	5.50	5.50	5.50	5.50	8.25	**6.05**
Core supply: S:G	3.67	3.67	2.75	3.67	2.75	3.67	2.75	3.67	5.50	**3.67**

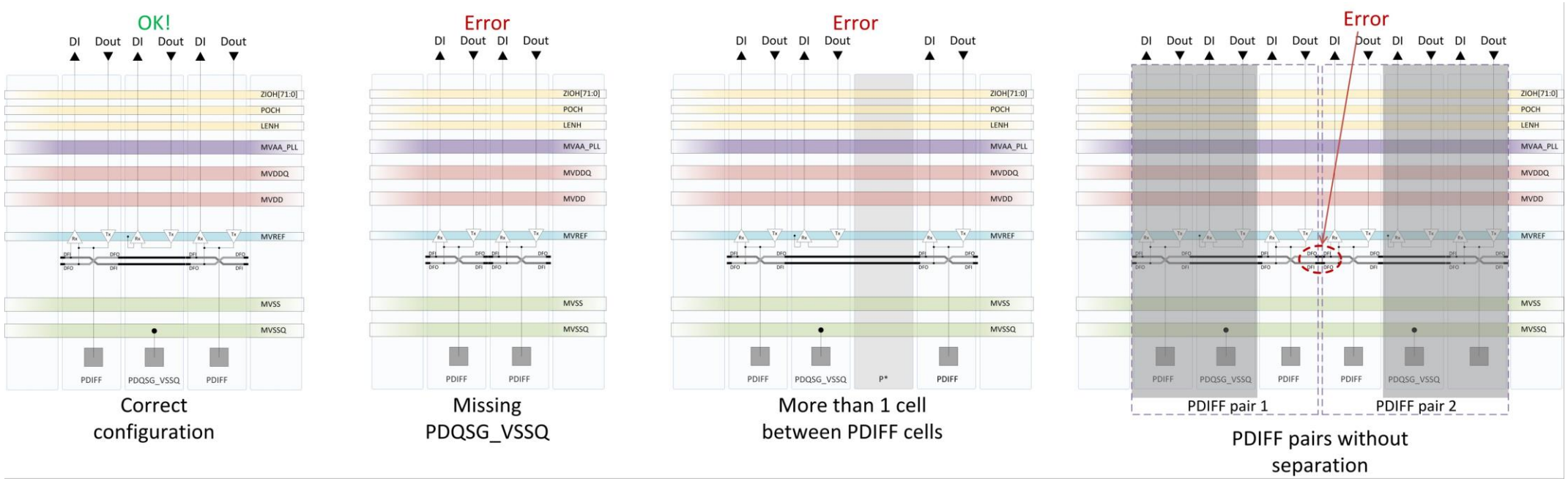
Floating rails

- The DDR PHY IO ring contains a number of rails, created through the abutment of PHY cells
- These rails are used to distribute supply, reference and logical voltages through the ring
- The rails can be broken to add/enable additional functionalities
- However it must be ensured that all the rail sections created are connected to a sufficient number of the corresponding driver cells



PDIFF cell analysis

- PDIFF must be used for DQS/DQS# signals
- A PDQSG cell needs to be added between the 2 PDIFF in order to effectively suppress the postamble glitch created at the end of a read burst
- Different PDIFF pair must be separated by at least 1 cell.
- As can be seen in the picture bellow, the DFI/DFO pins need to be manually connected in the layout



PDIFF cell analysis

- The position of the PDIFF and PDQSG cells was identified in the IO ring and its relative position was analyzed
- Cells seem to be properly instantiated
- Please, check the table in the following slide

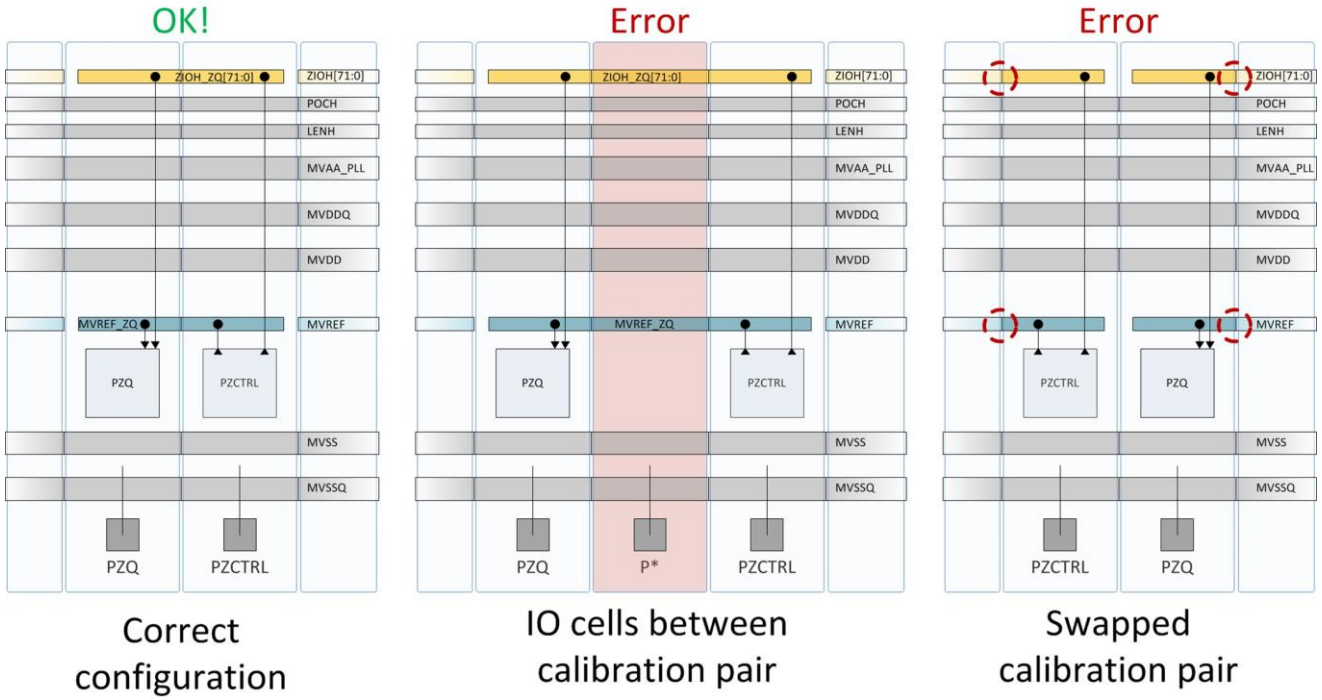
PDIFF cell analysis

- Cells seem to be properly instantiated
- Results are shown in the following table

Pair number	1st PDIFF pad number	2nd PDIFF pad number	PDQSG pad number	N cells between pair (not counting with fillers)	Obs.
Pair 1	191	193	192	1	OK
Pair 2	230	232	231	1	OK
Pair 3	259	261	260	1	OK
Pair 4	298	300	299	1	OK
Pair 5	428	430	429	1	OK
Pair 6	467	469	468	1	OK
Pair 7	496	498	497	1	OK
Pair 8	535	537	536	1	OK

Calibration pair analysis

- The cells in the calibration pair - PZCTRL and PZQ - will break the ZIOH and the VREF rails in the IO ring
- These rails will still exist inside the pair, created by the abutment of the 2 cells
- It needs to be verified if this abutment is correctly done
- Also, no cell can be placed between the two cells



Calibration pair analysis

- The relative position of PZCTRL and PZQ cells was analyzed in the floorplan
- Based on the CSV floorplan, the calibration pair cells - PZQ/PZCTRL - do not seem to be correctly placed in the IO ring.
- Make sure that the placement guidelines are followed in the GDS.
- Please, check the comments in the following table

Calibration pair analysis

- Cells are not being used properly in the IO ring
- Please, check the comments in the following table

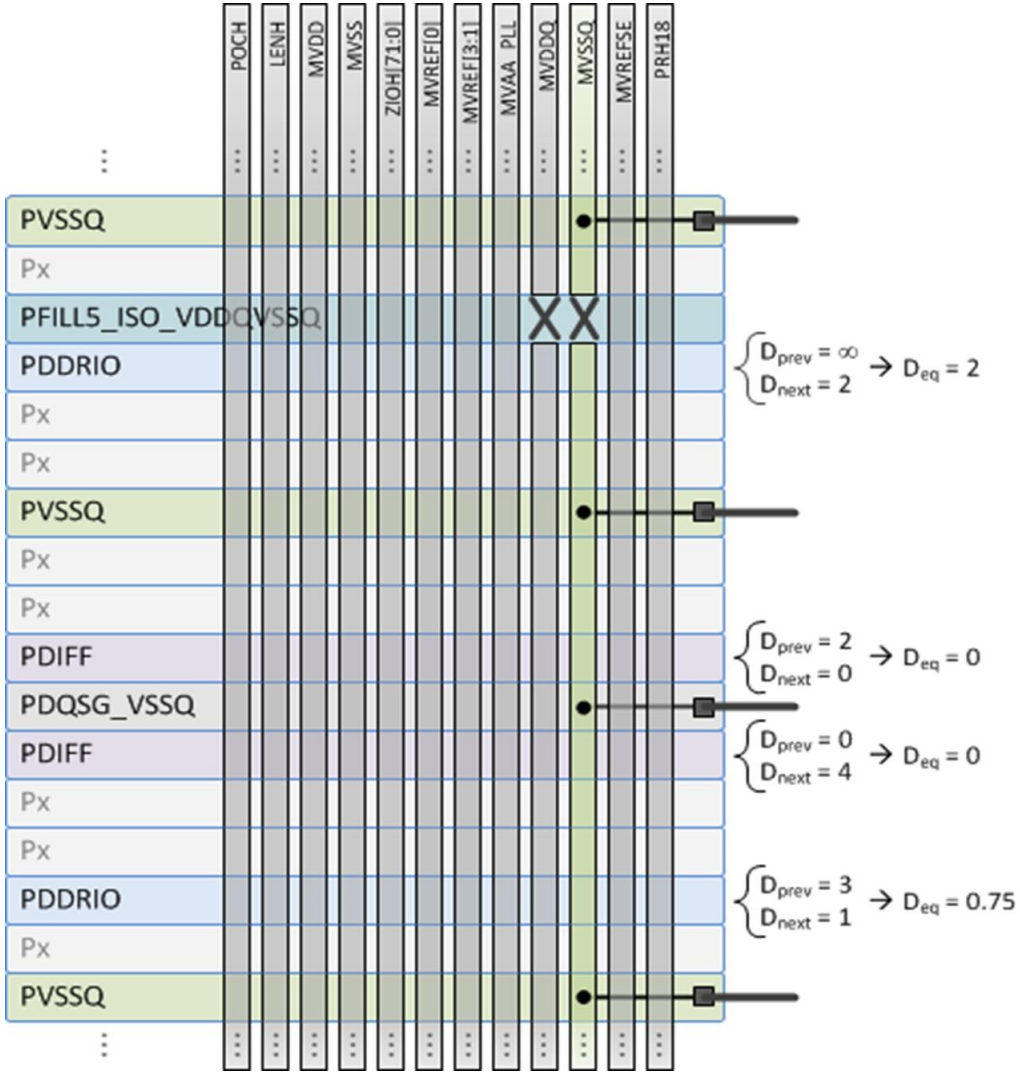
	Calibration pair 1	
PZQ cell	DWC_D4MV_PZQ_EW	
PZCTRL cell	DWC_D4MV_PZCTRL_EW	
PZQ cell position	322	
PZCTRL cell position	323	**Comments**
Number of cells between between pair (not counting with fillers)	0	
Relative position	OK	Relative position needs to be double checked, as rotation was not taken into account. In a north/south configuration, PZCTRL cell must always be placed at right hand side of PZQ cell. In a east/west configuration, PZCTRL cell must always be placed above PZQ cell.

Power/ground distribution analysis

- In order to achieve optimal performance, it is important that the power and ground cells are uniformly distributed along the IO ring

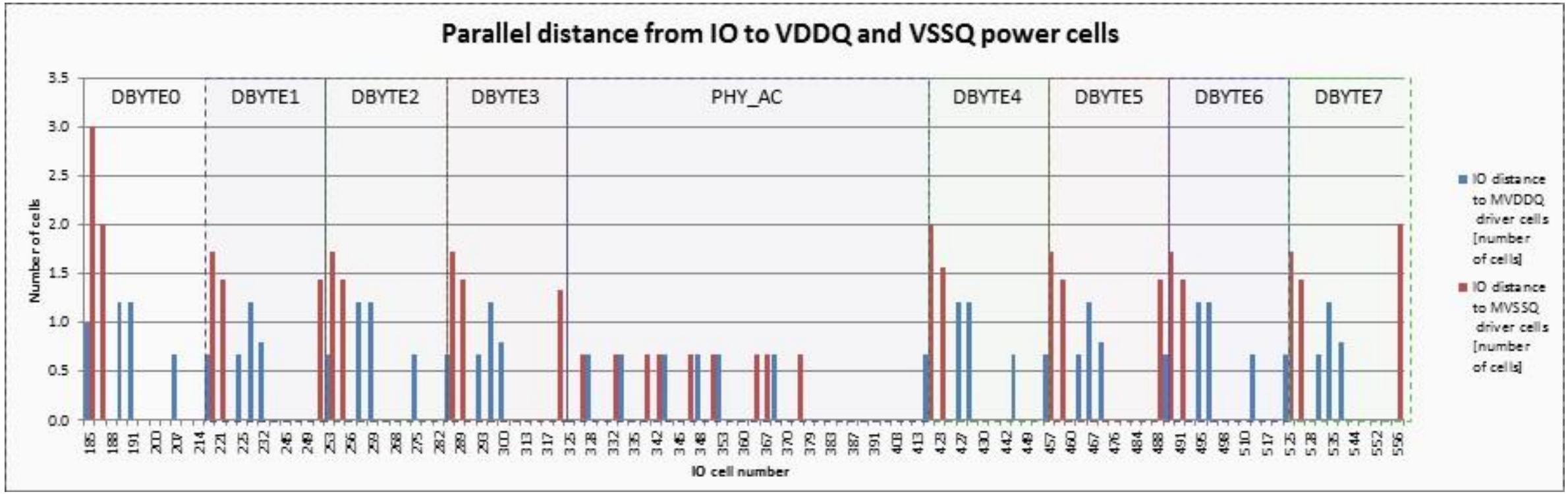
- In order to evaluate how power cells are distributed along the IO ring, a distance measurement between each IO cell and the next/previous power cell was determined, for all power rails

- This measurement is calculated as the parallel of the distances from an IO cell to the next and previous power cellsand it is given in number of cells, as shown in the picture



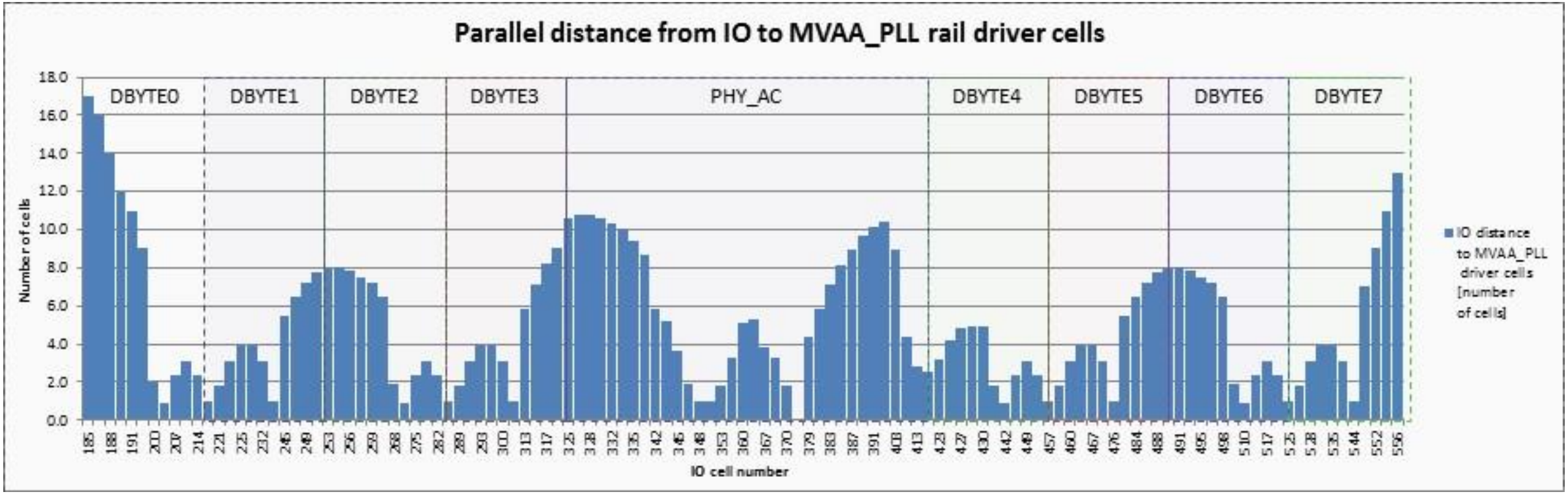
Power/ground distribution analysis

- The following charts show the distance measurements for each one of the rails
- Parallel distance from IO cells to MVDDQ and MVSSQ



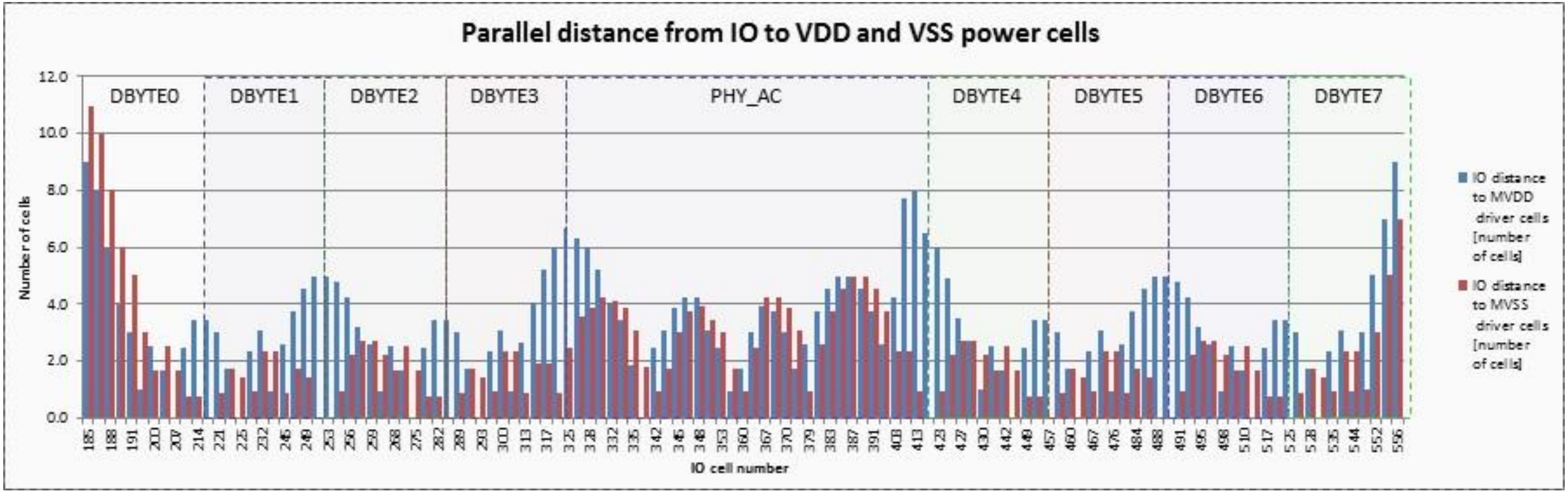
Power/ground distribution analysis

- Parallel distance from IO cells to MVAA_PLL



Power/ground distribution analysis

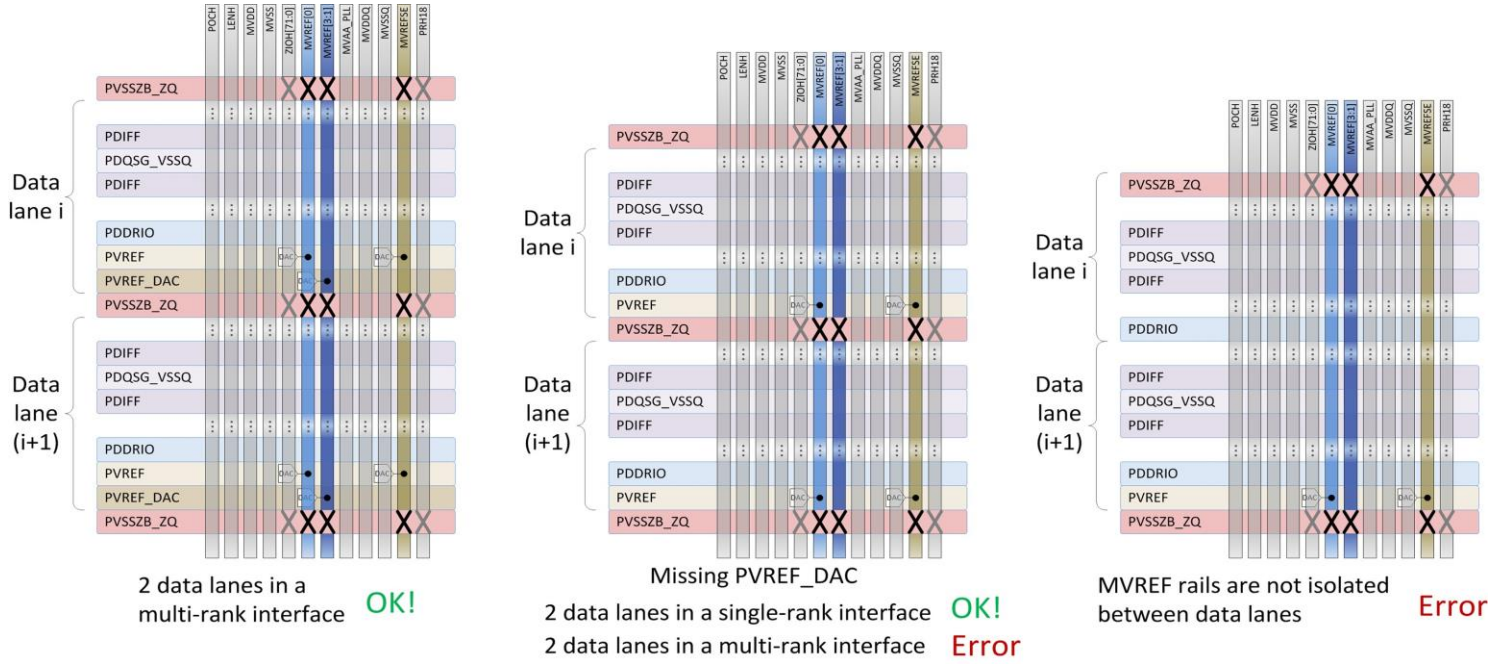
- Parallel distance from IO cells to MVDD and MVSS



DDR4 functionality

Vref training

- In DDR4, Vref training is applied individually to each byte/nibble lane.
- In order to enable VREF training, the following requirements must be met in the IO ring:
  - Each byte/nibble lane must have its own PVREF cell
  - For multi rank operation, a PVREF_DAC cell must be added in each byte/nibble lane section
  - The MVREF rail(s) of each byte/nibble lane section must be isolated



DDR4 functionality

Vref training

- It was verified if the IO ring meets the requirements needed for Vref training, based on the width of the data bus (byte/nibble), data mask availability, and number of required ranks
- Separated MVREF sections were identified and both IO cells and PVREF cells were analyzed
- IO ring seems to be properly built
- Results are shown in the following table

MVREF section associated to data lane	First cell in section (not counting with fillers)	Last cell in section (not counting with fillers)	Number of PDIFF cells in section	Number of PDDRIO cells in section	Number of PVREF cells in section	Number of PVREF_DAC cells in section	Pass/fail	Comments
Section1	185	218	2	9	1	1	OK	-
Section2	220	251	2	9	1	1	OK	-
Section3	253	286	2	9	1	1	OK	-
Section4	288	320	2	9	1	1	OK	-
Section5	422	455	2	9	1	1	OK	-
Section6	457	488	2	9	1	1	OK	-
Section7	490	523	2	9	1	1	OK	-
Section8	525	556	2	9	1	1	OK	-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