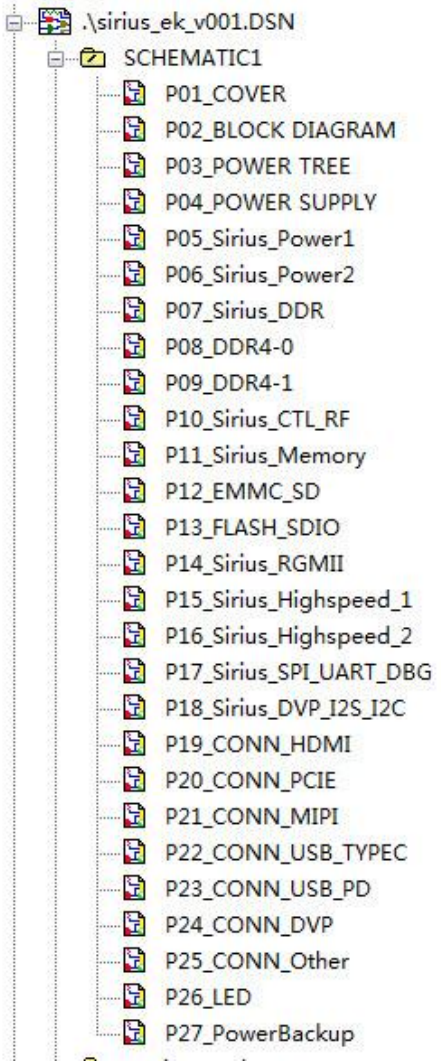

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Date 2017.11.22	Size A4	Page Title P01_COVER
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Date 2017.11.22	Size A4	Page Title P02_BLOCK DIAGRAM
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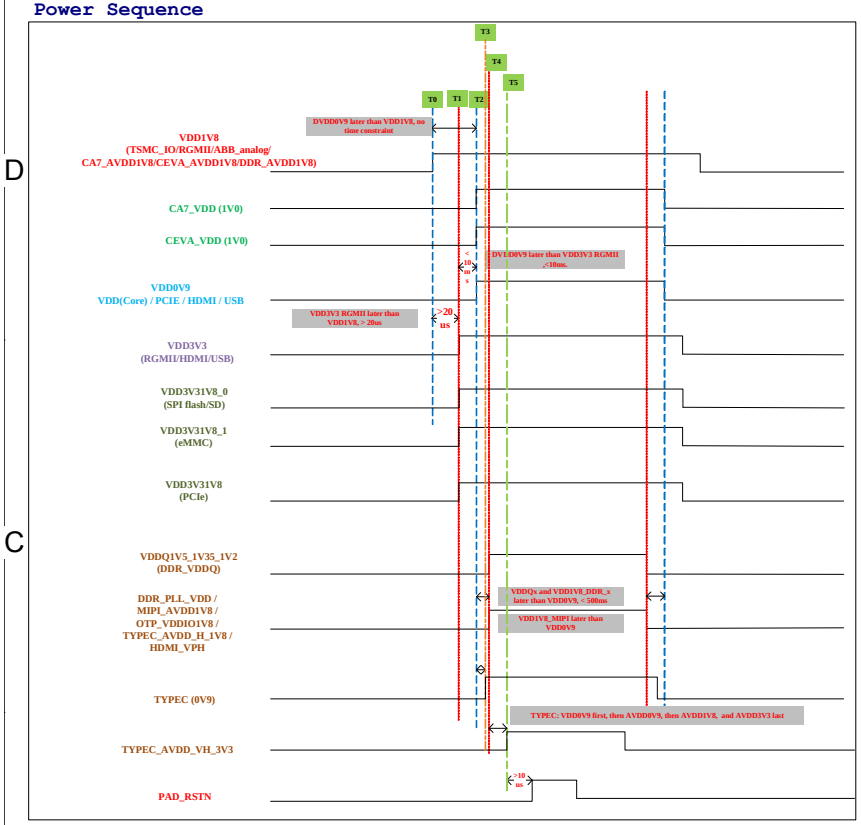
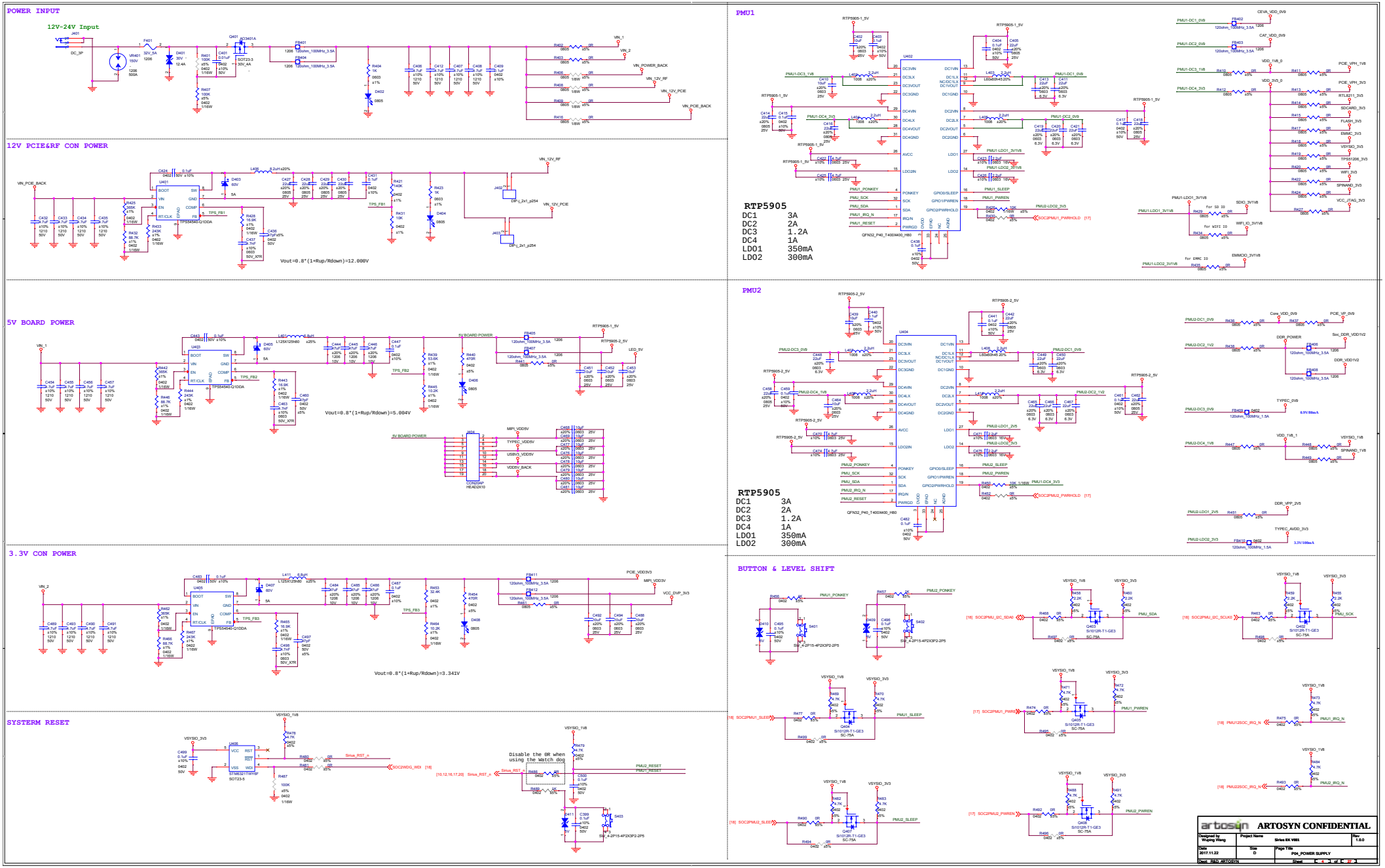
Power Sequence



Power Tree


POWER INPUT
12V-24V Input
12V PCIE&RF CON POWER
Vout=0.8*(1+Rup/Rdown)=12.000V
5V BOARD POWER
Vout=0.8*(1+Rup/Rdown)=5.004V
3.3V CON POWER
Vout=0.8*(1+Rup/Rdown)=3.341V
SYSTERM RESET
Disable the 0R when using the Watch dog
PMU1
RTP5905
DC1 3A
DC2 2A
DC3 1.2A
DC4 1A
LDO1 350mA
LDO2 300mA
PMU2
RTP5905
DC1 3A
DC2 2A
DC3 1.2A
DC4 1A
LDO1 350mA
LDO2 300mA
BUTTON & LEVEL SHIFT
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Size D
Page Title P04_POWER SUPPLY
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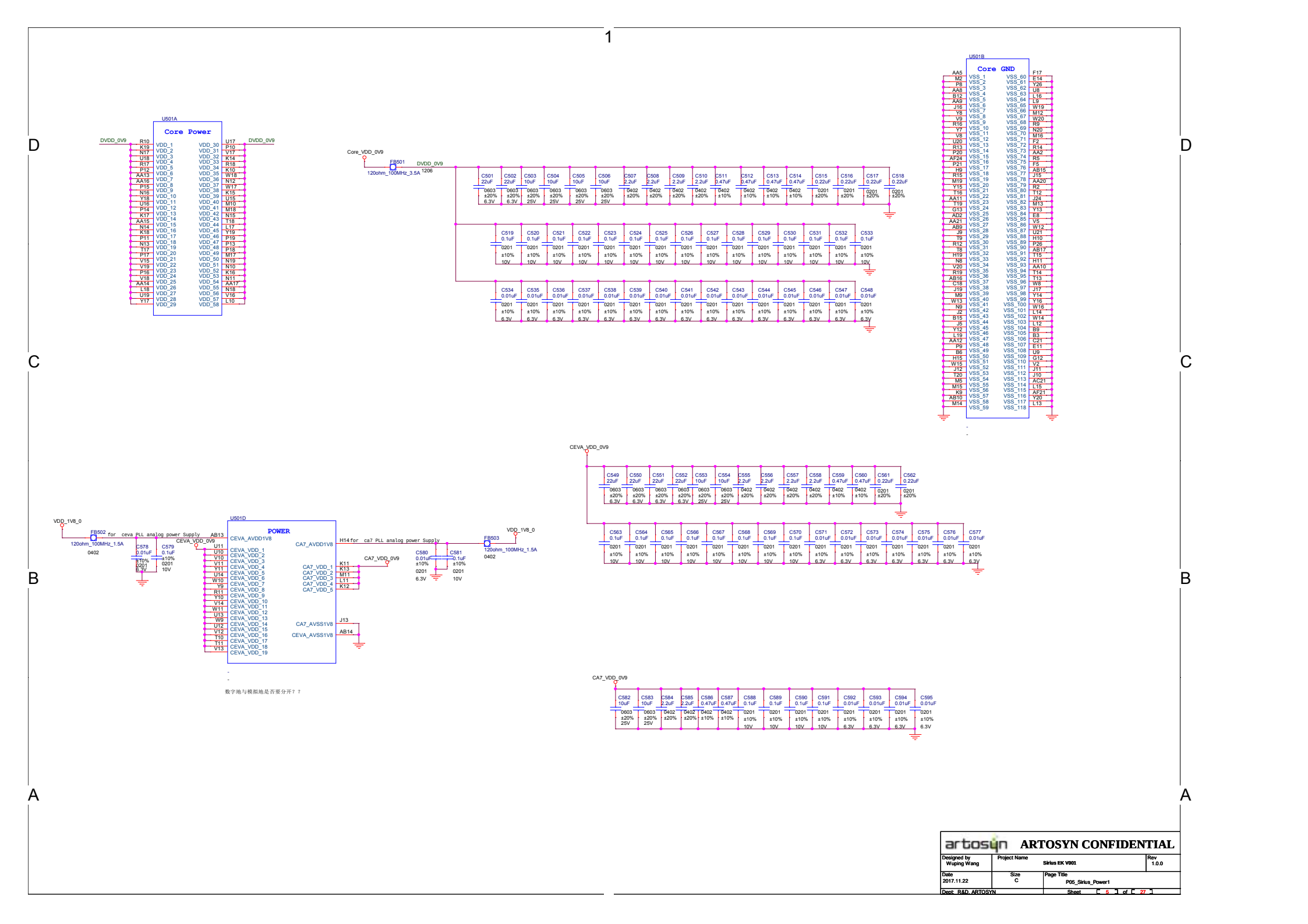
Sheet


U501A
Core Power
DVDD_0V9
DVDD_0V9
U501B
Core GND
Core_VDD_0V9
FB501
120ohm_100MHz_3.5A
1206
DVDD_0V9
CEVA_VDD_0V9
VDD_1V8_0
FB502
for ceva PLL analog power Supply
120ohm_100MHz_1.5A
0402
CEVA_VDD_0V9
U501D
POWER
H14 for ca7 PLL analog power Supply
CA7_VDD_0V9
FB503
120ohm_100MHz_1.5A
0402
VDD_1V8_0
CA7_VDD_0V9
数字地与模拟地是否要分开？？
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Project Name Sirius EK V001
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Size C
Page Title P05_Sirius_Power1
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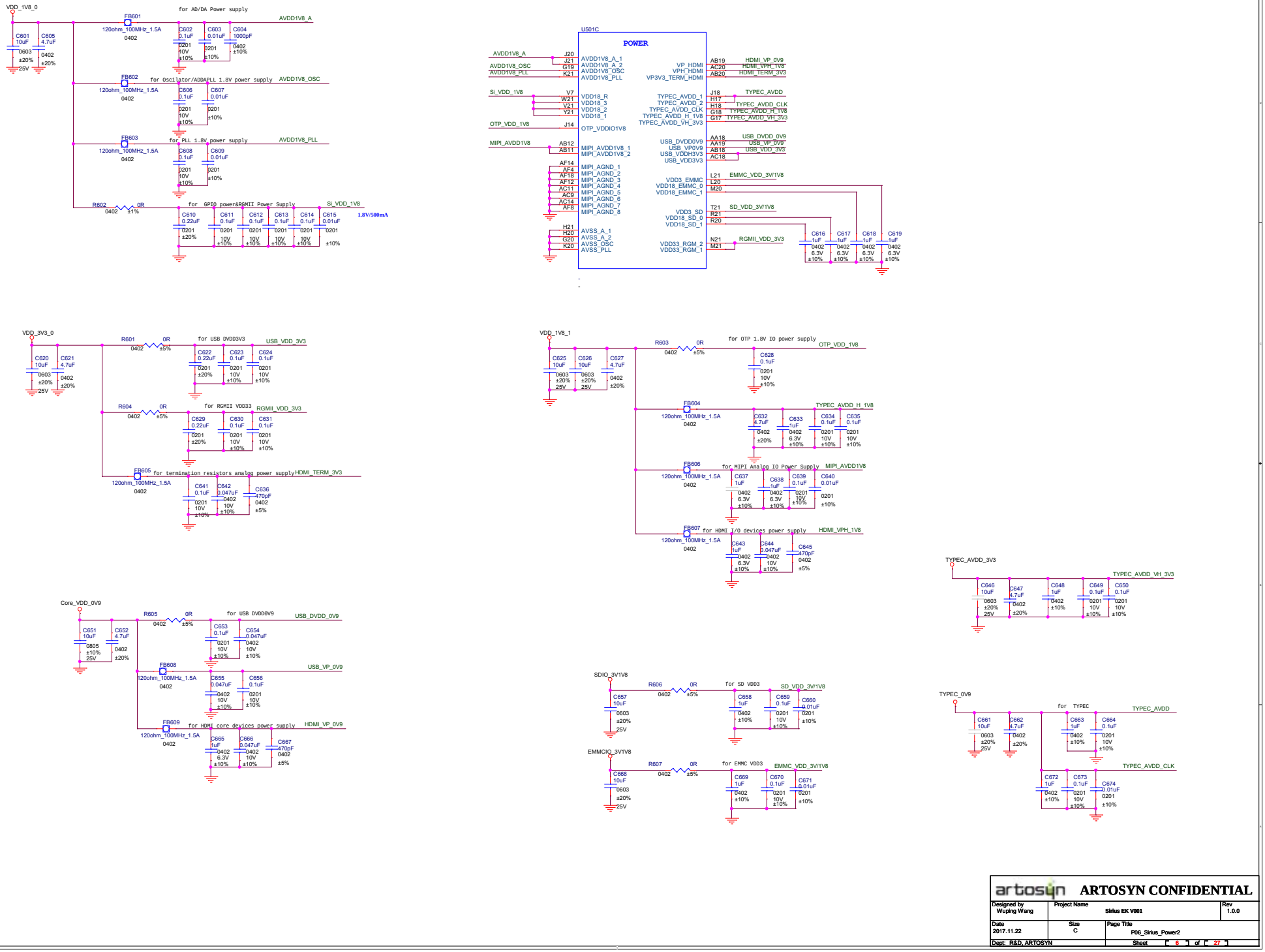
VDD_1V8_0
for AD/DA Power supply
FB601
120ohm_100MHz_1.5A
0402
AVDD1V8_A
C601 10uF 0603 ±20% 25V
C605 4.7uF 0402 ±20%
C602 0.1uF 0201 10V ±10%
C603 0.01uF 0201 ±10%
C604 1000pF 0402 ±10%
FB602
for Oscilator/ADDAPLL 1.8V power supply
AVDD1V8_OSC
120ohm_100MHz_1.5A
0402
C606 0.1uF 0201 10V ±10%
C607 0.01uF 0201 ±10%
FB603
for PLL 1.8V power supply
AVDD1V8_PLL
120ohm_100MHz_1.5A
0402
C608 0.1uF 0201 10V ±10%
C609 0.01uF 0201 ±10%
R602 0402 0R ±1%
for GPIO power&RGMII Power Supply
Si_VDD_1V8
1.8V/500mA
C610 0.22uF 0201 ±20%
C611 0.1uF 0201 10V ±10%
C612 0.1uF 0201 10V ±10%
C613 0.1uF 0201 10V ±10%
C614 0.1uF 0201 10V ±10%
C615 0.01uF 0201 ±10%
U501C
POWER
AVDD1V8_A
AVDD1V8_OSC
AVDD1V8_PLL
J20 AVDD1V8_A_1
J21 AVDD1V8_A_2
G19 AVDD1V8_OSC
K21 AVDD1V8_PLL
VP_HDMI
VPH_HDMI
VP3V3_TERM_HDMI
AB19 HDMI_VP_0V9
AC20 HDMI_VPH_1V8
AB20 HDMI_TERM_3V3
Si_VDD_1V8
V7 VDD18_R
W21 VDD18_3
V21 VDD18_2
Y21 VDD18_1
TYPEC_AVDD_1
TYPEC_AVDD_2
TYPEC_AVDD_CLK
TYPEC_AVDD_H_1V8
TYPEC_AVDD_VH_3V3
J18 TYPEC_AVDD
H17
H18 TYPEC_AVDD_CLK
G18 TYPEC_AVDD_H_1V8
G17 TYPEC_AVDD_VH_3V3
OTP_VDD_1V8
J14 OTP_VDDIO1V8
MIPI_AVDD1V8
AB12 MIPI_AVDD1V8_1
AB11 MIPI_AVDD1V8_2
USB_DVDD0V9
USB_VP0V9
USB_VDD3V3
AA18 USB_DVDD_0V9
AA19 USB_VP_0V9
AB18 USB_VDD_3V3
AC18
AF14 MIPI_AGND_1
AF4 MIPI_AGND_2
AF18 MIPI_AGND_3
AF12 MIPI_AGND_4
AC11 MIPI_AGND_5
AC9 MIPI_AGND_6
AC14 MIPI_AGND_7
AF8 MIPI_AGND_8
VDD3_EMMC
VDD18_EMMC_0
VDD18_EMMC_1
L21 EMMC_VDD_3V/1V8
L20
M20
VDD3_SD
VDD18_SD_0
VDD18_SD_1
T21 SD_VDD_3V/1V8
R21
R20
H21 AVSS_A_1
H20 AVSS_A_2
G20 AVSS_OSC
K20 AVSS_PLL
VDD33_RGM_2
VDD33_RGM_1
N21 RGMII_VDD_3V3
M21
C616 1uF 0402 6.3V ±10%
C617 1uF 0402 6.3V ±10%
C618 1uF 0402 6.3V ±10%
C619 1uF 0402 6.3V ±10%
VDD_3V3_0
R601 0402 0R ±5%
for USB DVDD3V3
USB_VDD_3V3
C620 10uF 0603 ±20% 25V
C621 4.7uF 0402 ±20%
C622 0.22uF 0201 ±20%
C623 0.1uF 0201 10V ±10%
C624 0.1uF 0201 10V ±10%
R604 0402 0R ±5%
for RGMII VDD33
RGMII_VDD_3V3
C629 0.22uF 0201 ±20%
C630 0.1uF 0201 10V ±10%
C631 0.1uF 0201 10V ±10%
FB605
for termination resistors analog power supply
HDMI_TERM_3V3
120ohm_100MHz_1.5A
0402
C641 0.1uF 0201 10V ±10%
C642 0.047uF 0402 10V ±10%
C636 470pF 0402 ±5%
VDD_1V8_1
C625 10uF 0603 ±20% 25V
C626 10uF 0603 ±20% 25V
C627 4.7uF 0402 ±20%
R603 0402 0R ±5%
for OTP 1.8V IO power supply
OTP_VDD_1V8
C628 0.1uF 0201 10V ±10%
FB604
120ohm_100MHz_1.5A
0402
TYPEC_AVDD_H_1V8
C632 4.7uF 0402 ±20%
C633 1uF 0402 6.3V ±10%
C634 0.1uF 0201 10V ±10%
C635 0.1uF 0201 10V ±10%
FB606
for MIPI Analog IO Power Supply
MIPI_AVDD1V8
120ohm_100MHz_1.5A
0402
C637 1uF 0402 6.3V ±10%
C638 1uF 0402 6.3V ±10%
C639 0.1uF 0201 10V ±10%
C640 0.01uF 0201 ±10%
FB607
for HDMI I/O devices power supply
HDMI_VPH_1V8
120ohm_100MHz_1.5A
0402
C643 1uF 0402 6.3V ±10%
C644 0.047uF 0402 10V ±10%
C645 470pF 0402 ±5%
TYPEC_AVDD_3V3
TYPEC_AVDD_VH_3V3
C646 10uF 0603 ±20% 25V
C647 4.7uF 0402 ±20%
C648 1uF 0402 ±10%
C649 0.1uF 0201 10V ±10%
C650 0.1uF 0201 10V ±10%
Core_VDD_0V9
R605 0402 0R ±5%
for USB DVDD0V9
USB_DVDD_0V9
C651 10uF 0805 ±10% 25V
C652 4.7uF 0402 ±20%
C653 0.1uF 0201 10V ±10%
C654 0.047uF 0402 10V ±10%
FB608
120ohm_100MHz_1.5A
0402
USB_VP_0V9
C655 0.047uF 0402 10V ±10%
C656 0.1uF 0201 10V ±10%
FB609
for HDMI core devices power supply
HDMI_VP_0V9
120ohm_100MHz_1.5A
0402
C665 1uF 0402 6.3V ±10%
C666 0.047uF 0402 10V ±10%
C667 470pF 0402 ±5%
SDIO_3V1V8
R606 0402 0R ±5%
for SD VDD3
SD_VDD_3V/1V8
C657 10uF 0603 ±20% 25V
C658 1uF 0402 ±10%
C659 0.1uF 0201 10V ±10%
C660 0.01uF 0201 ±10%
EMMCIO_3V1V8
R607 0402 0R ±5%
for EMMC VDD3
EMMC_VDD_3V/1V8
C668 10uF 0603 ±20% 25V
C669 1uF 0402 ±10%
C670 0.1uF 0201 10V ±10%
C671 0.01uF 0201 ±10%
TYPEC_0V9
for TYPEC
TYPEC_AVDD
C661 10uF 0603 ±20% 25V
C662 4.7uF 0402 ±20%
C663 1uF 0402 ±10%
C664 0.1uF 0201 10V ±10%
TYPEC_AVDD_CLK
C672 1uF 0402 ±10%
C673 0.1uF 0201 10V ±10%
C674 0.01uF 0201 ±10%
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Project Name
Sirius EK V001
Rev
1.0.0
Date
2017.11.22
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Page Title
P06_Sirius_Power2
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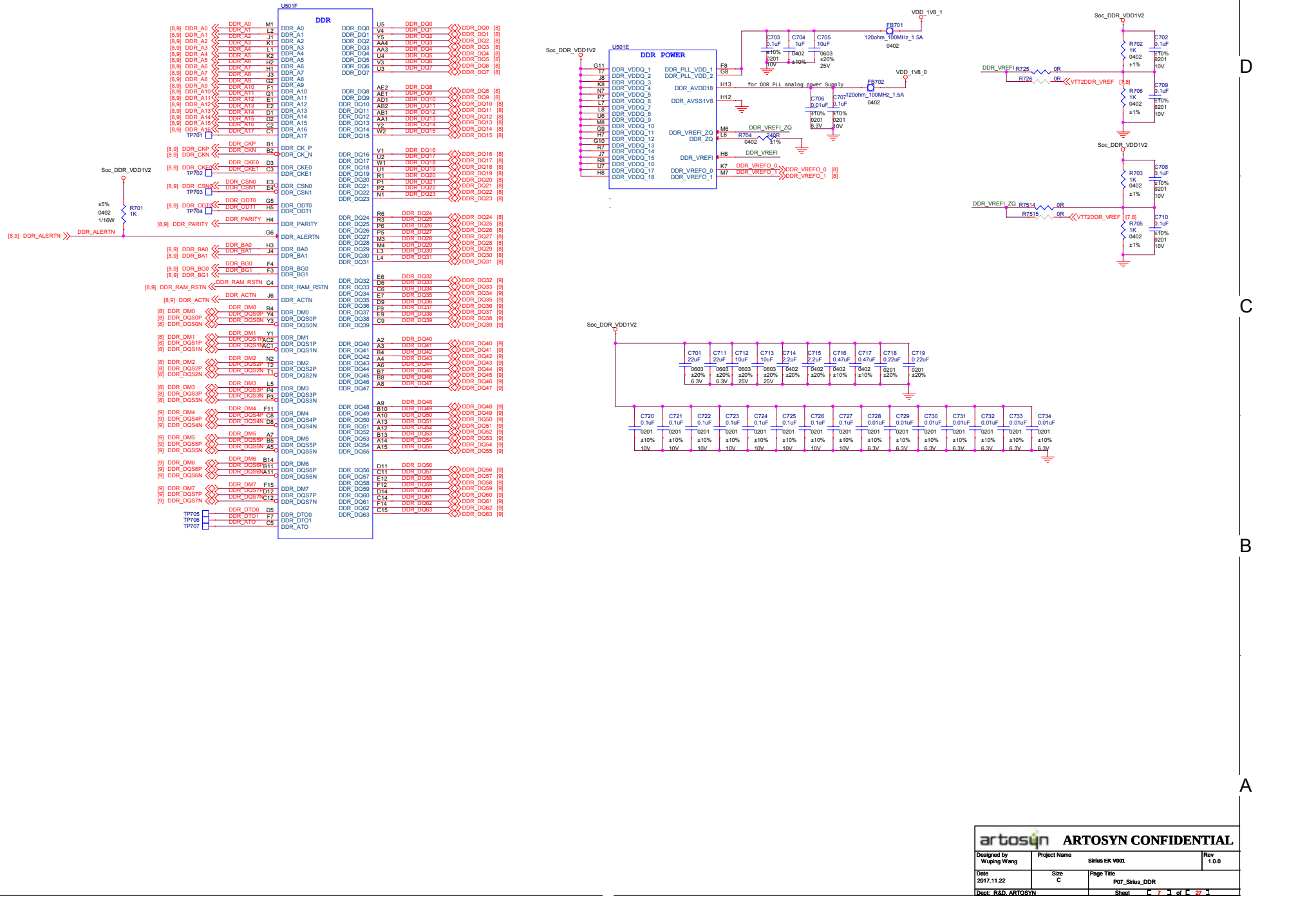
U501F
DDR
U501E
DDR POWER
Soc_DDR_VDD1V2
VDD_1V8_1
VDD_1V8_0
FB701
FB702
120ohm_100MHz_1.5A
for DDR PLL analog power Supply
DDR_VREFI
DDR_VREFI_ZQ
DDR_ZQ
DDR_AVDD18
DDR_AVSS1V8
DDR_PLL_VDD_1
DDR_PLL_VDD_2
DDR_VREFO_0
DDR_VREFO_1
R701 1K 0402 1/16W ±5%
R704 240R 0402 ±1%
R725 0R
R726 0R
R7514 0R
R7515 0R
VTT2DDR_VREF
DDR_ALERTN
DDR_PARITY
DDR_ACTN
DDR_RAM_RSTN
DDR_CKP
DDR_CKN
DDR_CKE0
DDR_CKE1
DDR_CSN0
DDR_CSN1
DDR_ODT0
DDR_ODT1
DDR_BA0
DDR_BA1
DDR_BG0
DDR_BG1
DDR_DM0
DDR_DM1
DDR_DM2
DDR_DM3
DDR_DM4
DDR_DM5
DDR_DM6
DDR_DM7
DDR_DQS0P
DDR_DQS0N
DDR_DQS1P
DDR_DQS1N
DDR_DQS2P
DDR_DQS2N
DDR_DQS3P
DDR_DQS3N
DDR_DQS4P
DDR_DQS4N
DDR_DQS5P
DDR_DQS5N
DDR_DQS6P
DDR_DQS6N
DDR_DQS7P
DDR_DQS7N
DDR_DTO0
DDR_DTO1
DDR_ATO
TP701
TP702
TP703
TP704
TP705
TP706
TP707
C701 22uF 0603 ±20% 6.3V
C711 22uF 0603 ±20% 6.3V
C712 10uF 0603 ±20% 25V
C713 10uF 0603 ±20% 25V
C714 2.2uF 0402 ±20%
C715 2.2uF 0402 ±20%
C716 0.47uF 0402 ±10%
C717 0.47uF 0402 ±10%
C718 0.22uF 0201 ±20%
C719 0.22uF 0201 ±20%
C720 0.1uF 0201 ±10% 10V
C721 0.1uF 0201 ±10% 10V
C722 0.1uF 0201 ±10% 10V
C723 0.1uF 0201 ±10% 10V
C724 0.1uF 0201 ±10% 10V
C725 0.1uF 0201 ±10% 10V
C726 0.1uF 0201 ±10% 10V
C727 0.1uF 0201 ±10% 10V
C728 0.01uF 0201 ±10% 6.3V
C729 0.01uF 0201 ±10% 6.3V
C730 0.01uF 0201 ±10% 6.3V
C731 0.01uF 0201 ±10% 6.3V
C732 0.01uF 0201 ±10% 6.3V
C733 0.01uF 0201 ±10% 6.3V
C734 0.01uF 0201 ±10% 6.3V
C703 0.1uF 0201 ±10% 10V
C704 1uF 0402 ±10%
C705 10uF 0603 ±20% 25V
C706 0.01uF 0201 ±10% 6.3V
C707 0.1uF 0201 ±10% 10V
R702 1K 0402 ±1%
R706 1K 0402 ±1%
C702 0.1uF 0201 ±10% 10V
C709 0.1uF 0201 ±10% 10V
R703 1K 0402 ±1%
R705 1K 0402 ±1%
C708 0.1uF 0201 ±10% 10V
C710 0.1uF 0201 ±10% 10V
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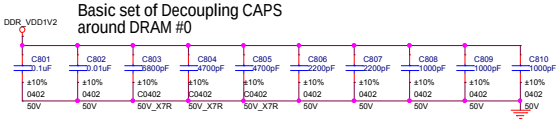
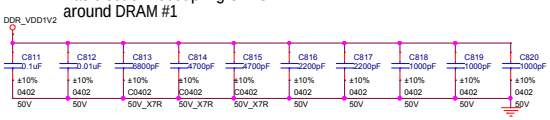
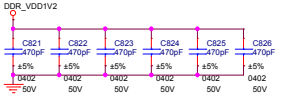
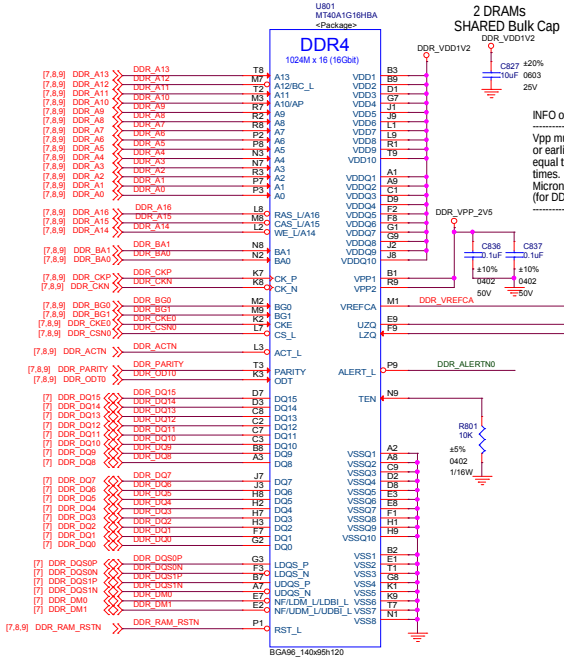
Basic set of Decoupling CAPS around DRAM #0

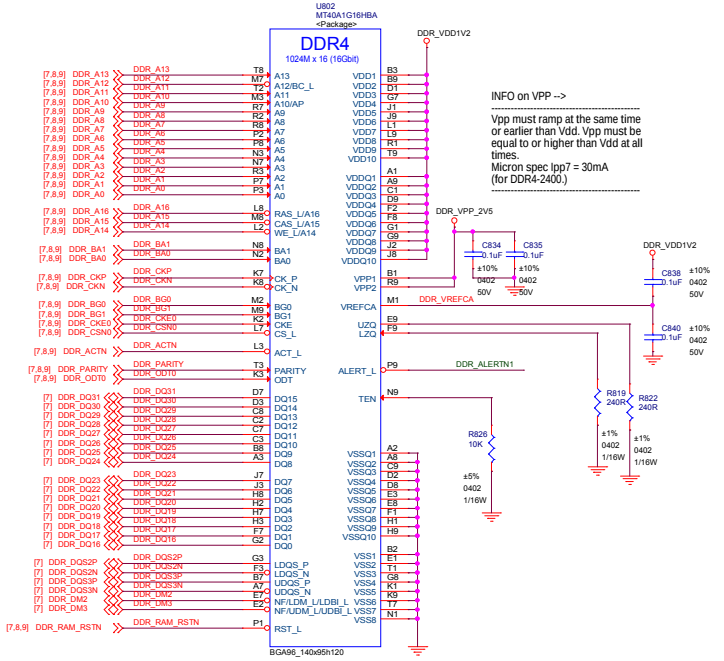


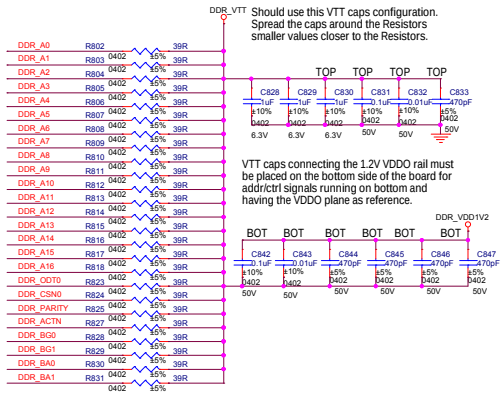
Basic set of Decoupling CAPS around DRAM #1

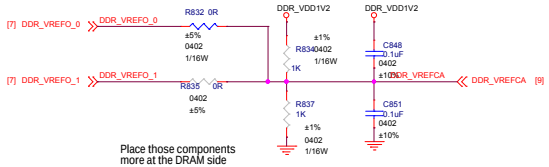


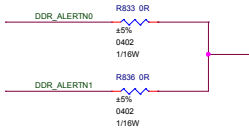


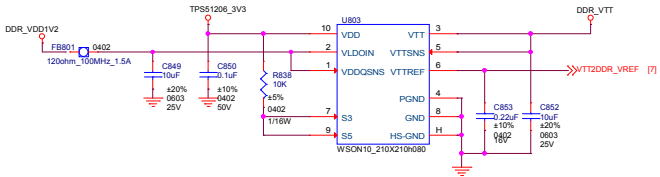


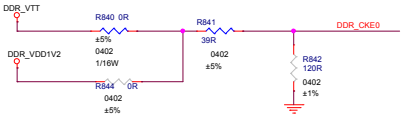


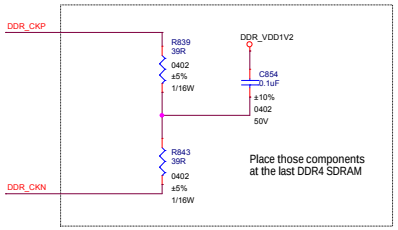












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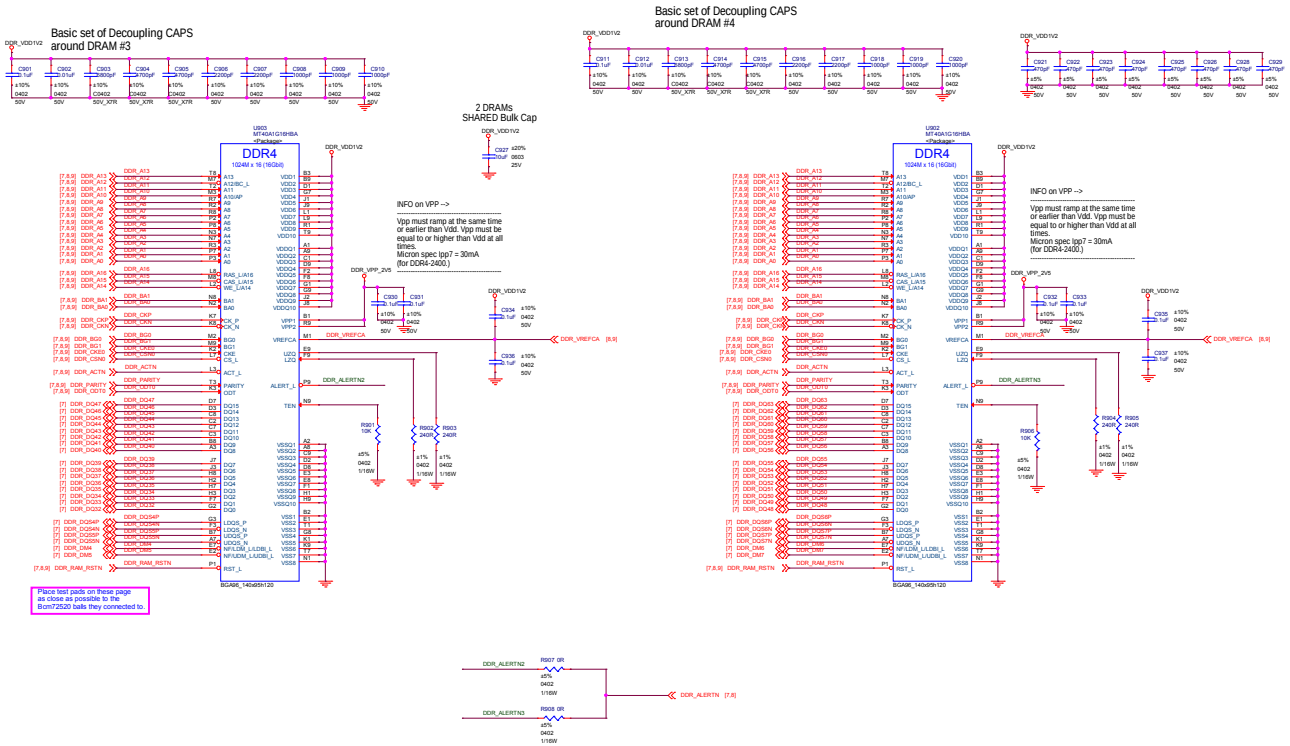
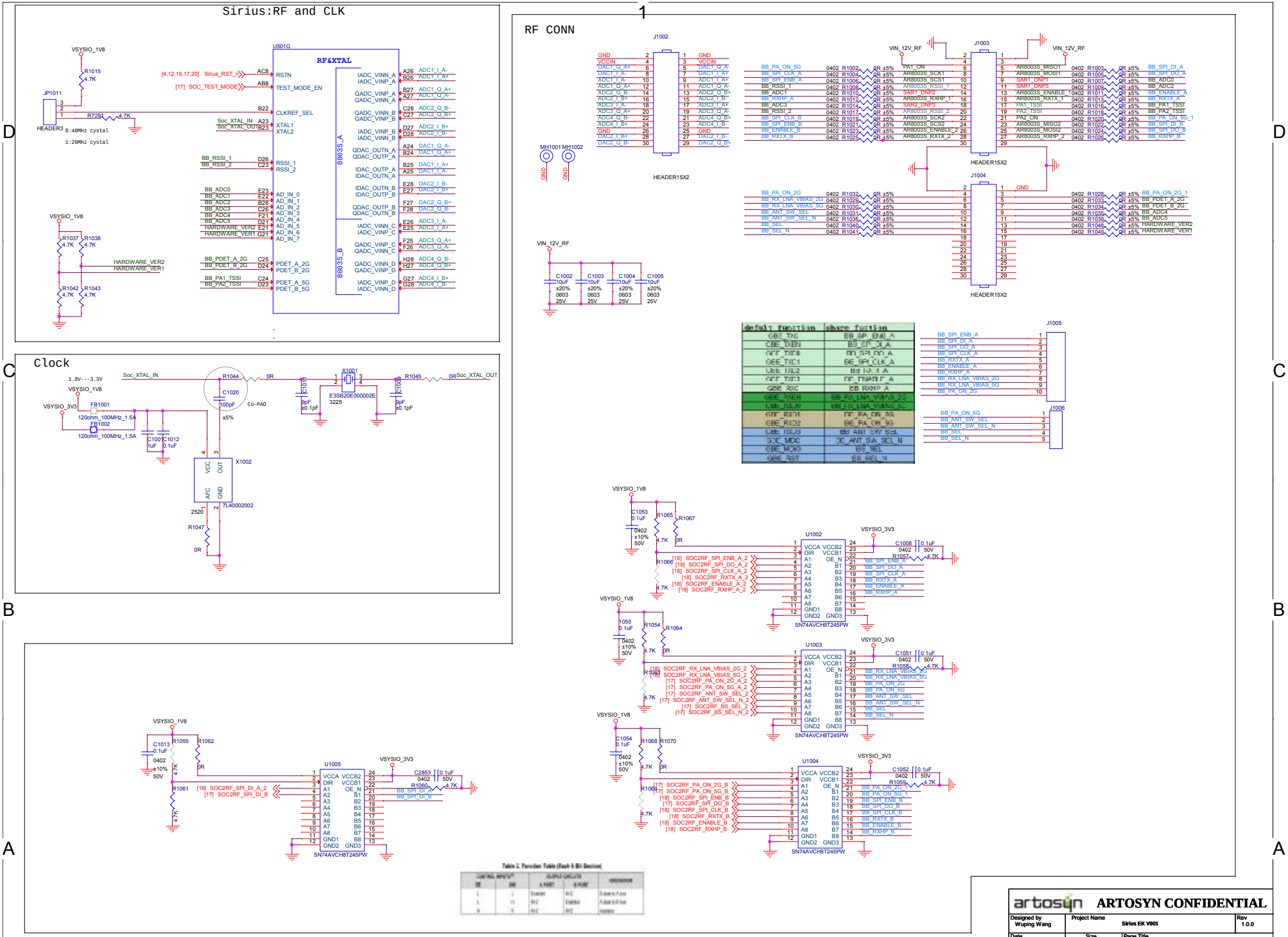


Designed by: Wuqing Wang	Project Name: Sirius BK V001	Rev: 1.0.0
Date: 2017.11.22	Size: D	Page Title: P09_DDR4-1
Chief: R&D_ARTOSYN		Sheet: 9 of 39


Sirius:RF and CLK
RF CONN
Clock
RF&XTAL
SN74AVCH8T245PW
HEADER15X2
ARTOSYN CONFIDENTIAL
Designed by Wuping Wang
Project Name Sirius EK V001
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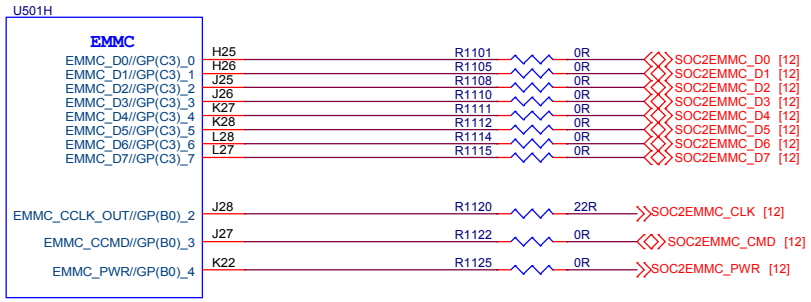
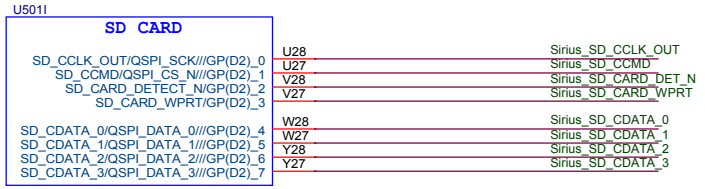
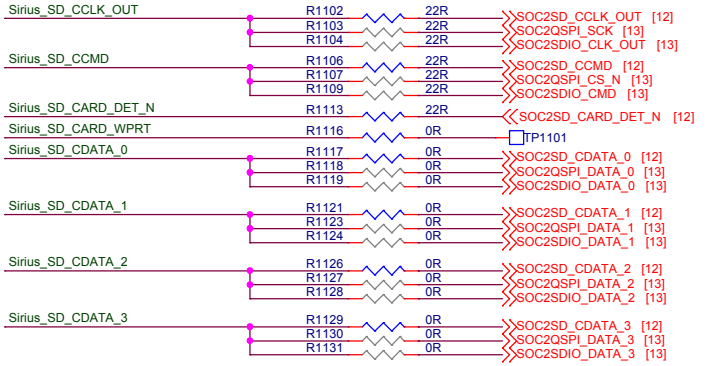
SOC EMMC & SD







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Designed by Wuping Wang	Project Name Sirius EK V001	Rev 1.0.0
Date 2017.11.22	Size B	Page Title P11_Sirius_Memory
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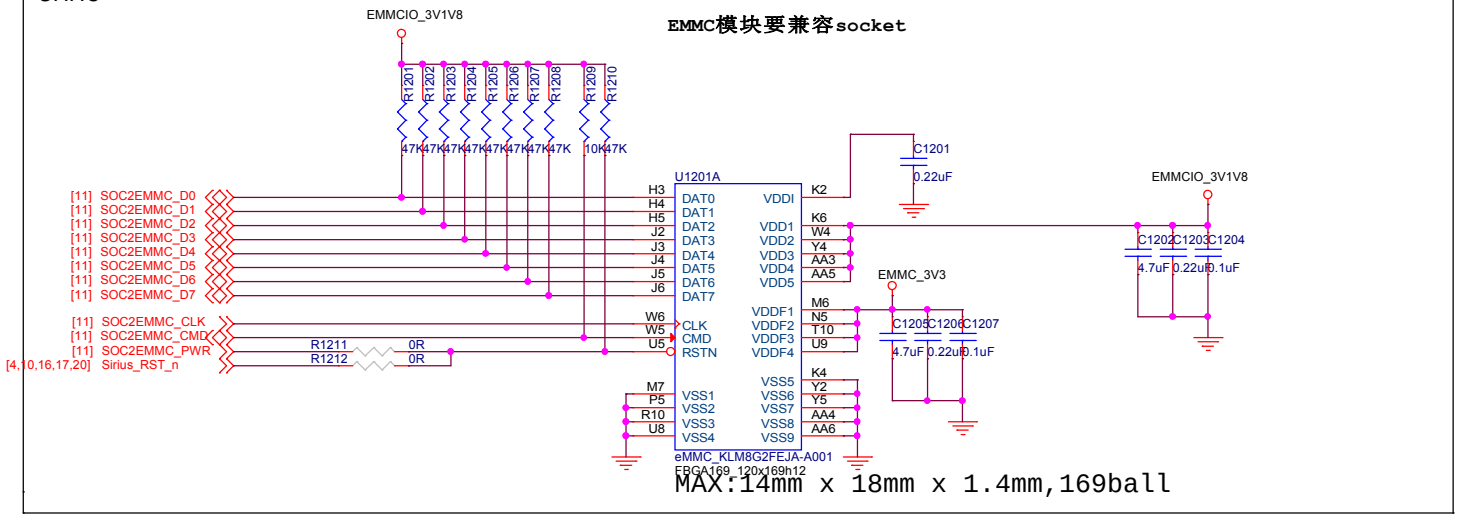
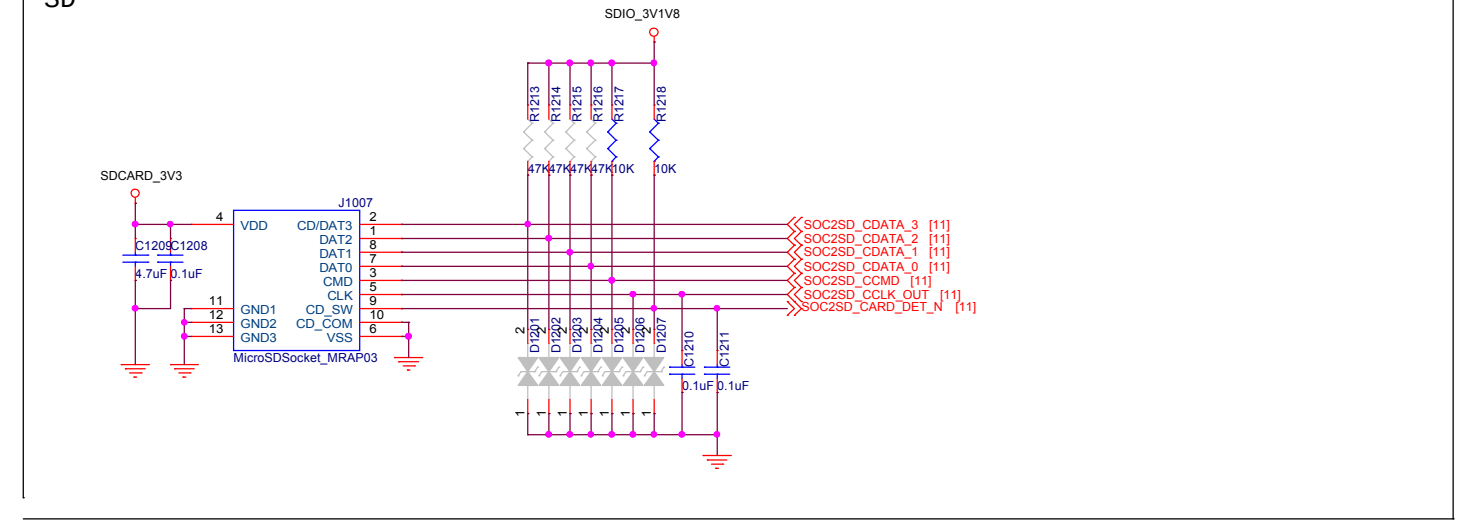
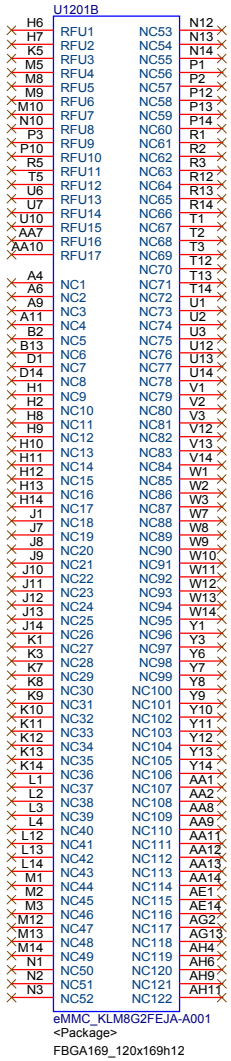
eMMC



SD





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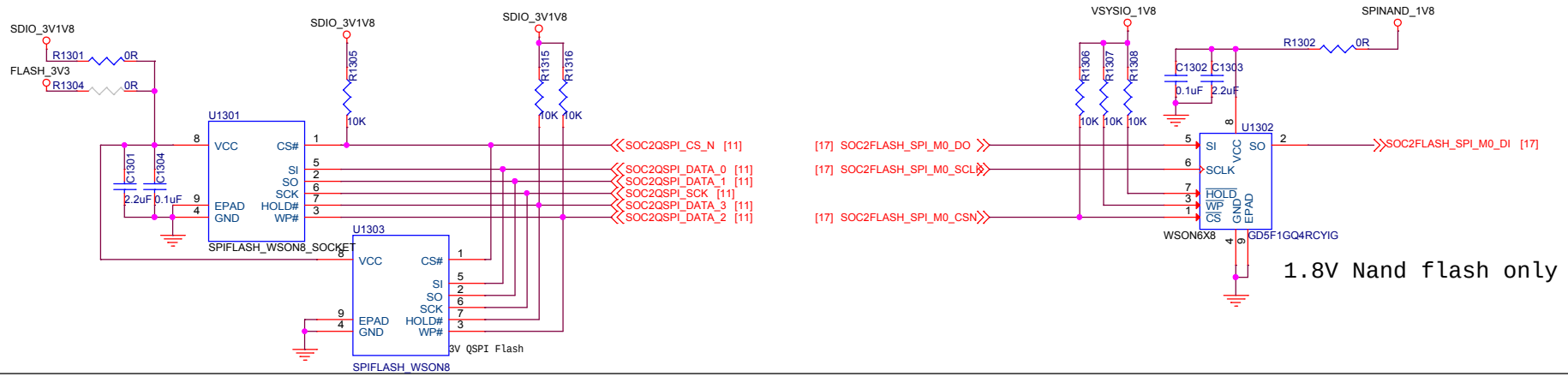
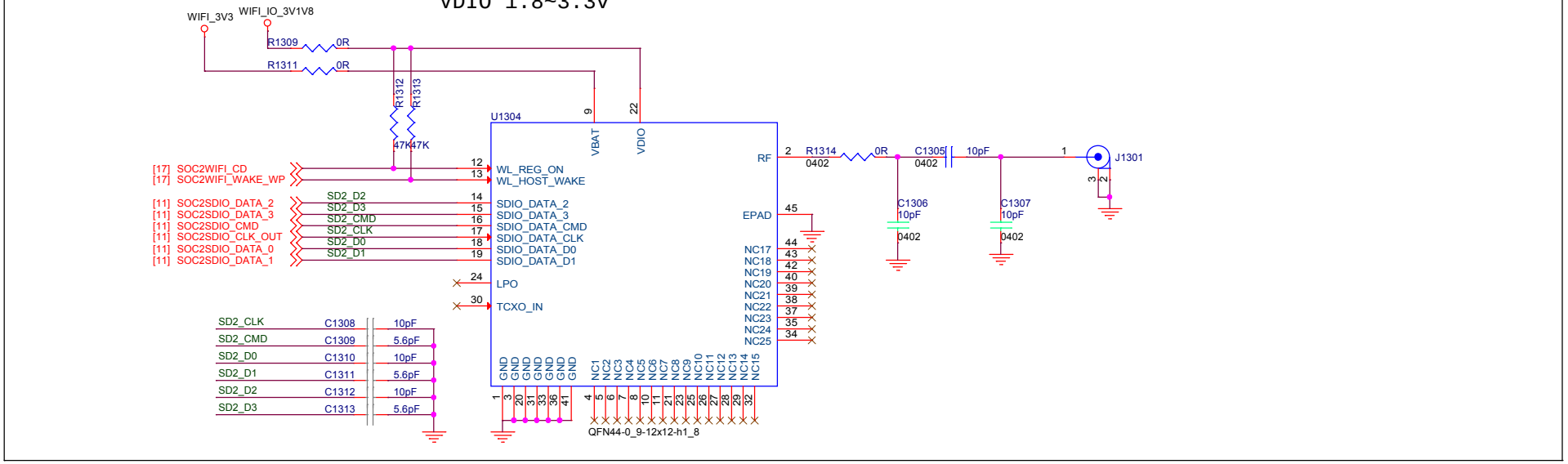
QSPI & SPI Nand flash



SDIO WIFI Module



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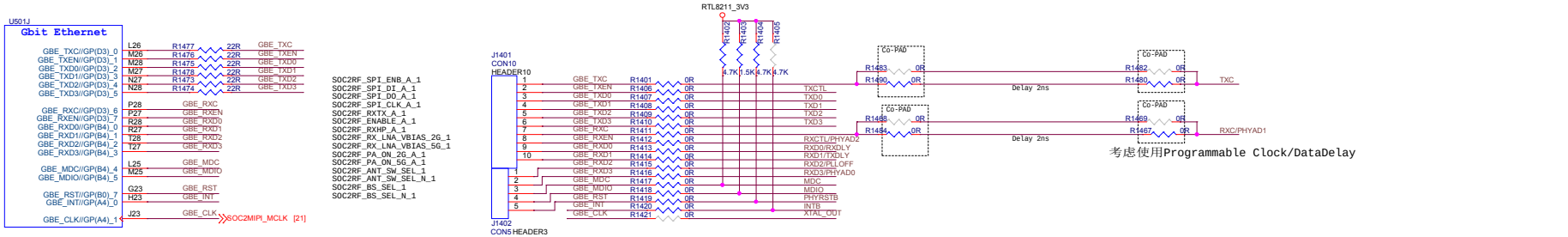
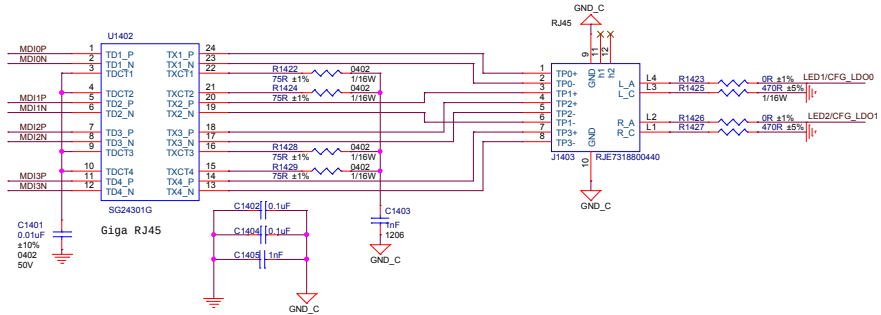
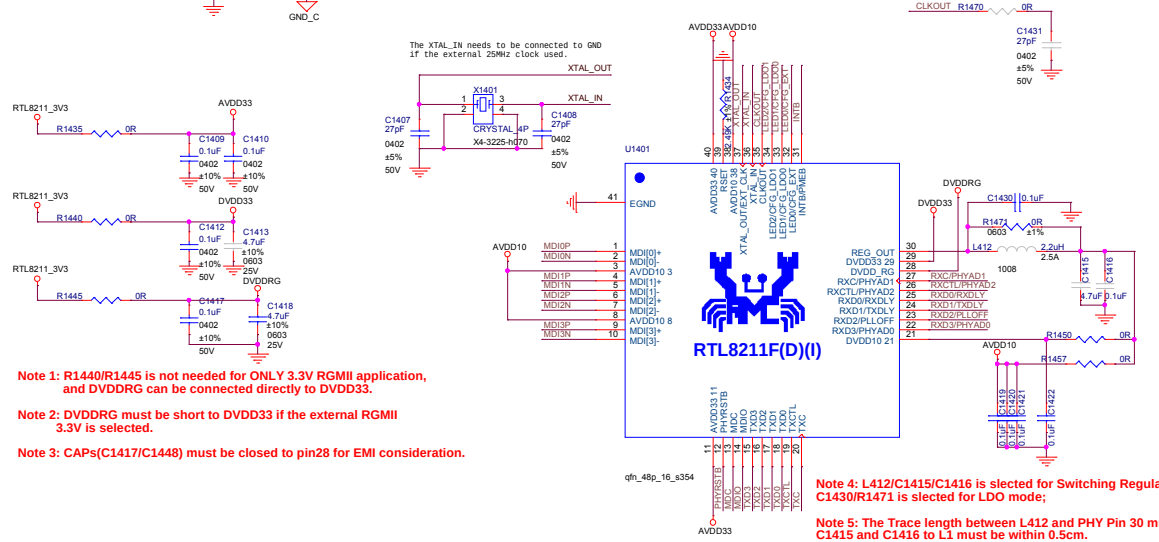




PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V (default)	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11

	LED Resistances Setting
CFG_EXT=1'b1	R1430(NC), R1431, R1432, R1433(NC)
CFG_EXT=1'b0	R1430, R1431(NC), R1432(NC), R1433
CFG_LDO0=1'b1	R1434(NC), R1437, R1438, R1439(NC)
CFG_LDO0=1'b0	R1434, R1437(NC), R1438(NC), R1439
CFG_LDO1=1'b1	R1441(NC), R1442, R1443, R1444(NC)
CFG_LDO1=1'b0	R1441, R1442(NC), R1443(NC), R1444



Note 1: R1440/R1445 is not needed for ONLY 3.3V RGMII application, and DVDDRG can be connected directly to DVDD33.

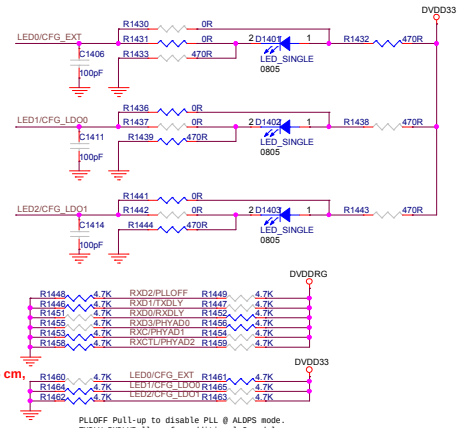
Note 2: DVDDRG must be short to DVDD33 if the external RGMII 3.3V is selected.

Note 3: CAPs(C1417/C1448) must be closed to pin28 for EMI consideration.

Note 4: L412/C1415/C1416 is slected for Switching Regulator mode; C1430/R1471 is slected for LDO mode;

Note 5: The Trace length between L412 and PHY Pin 30 must be within 0.5 cm, C1415 and C1416 to L1 must be within 0.5cm.

Note 6: Any inductance or bead except L1 is not allowed on the path from REGOUT to DVDD10/AVDD10.



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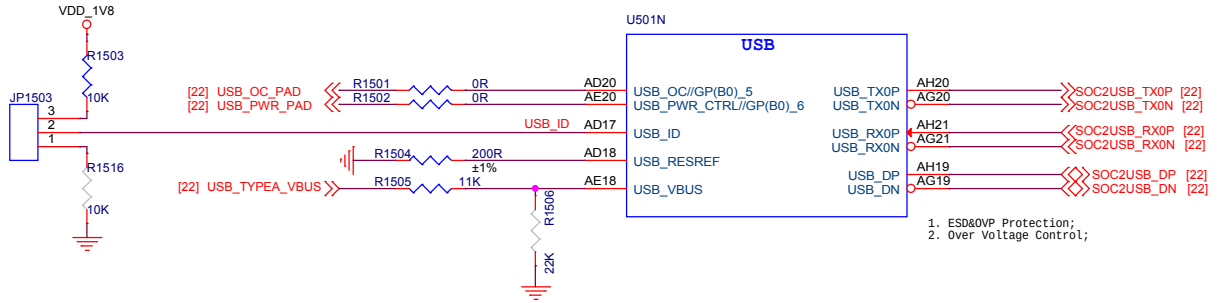
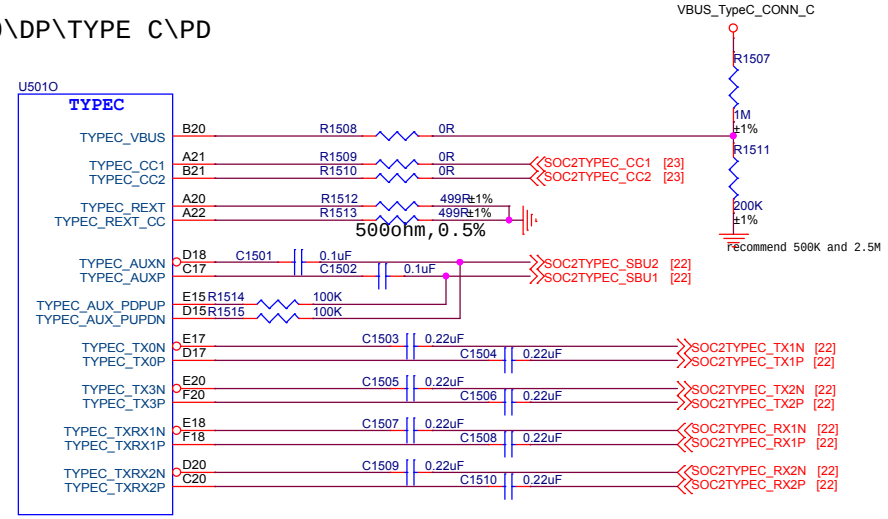
SOC:USB3.0 AND USB2.0



SOC:USB3.0\DP\TYPE C\PD



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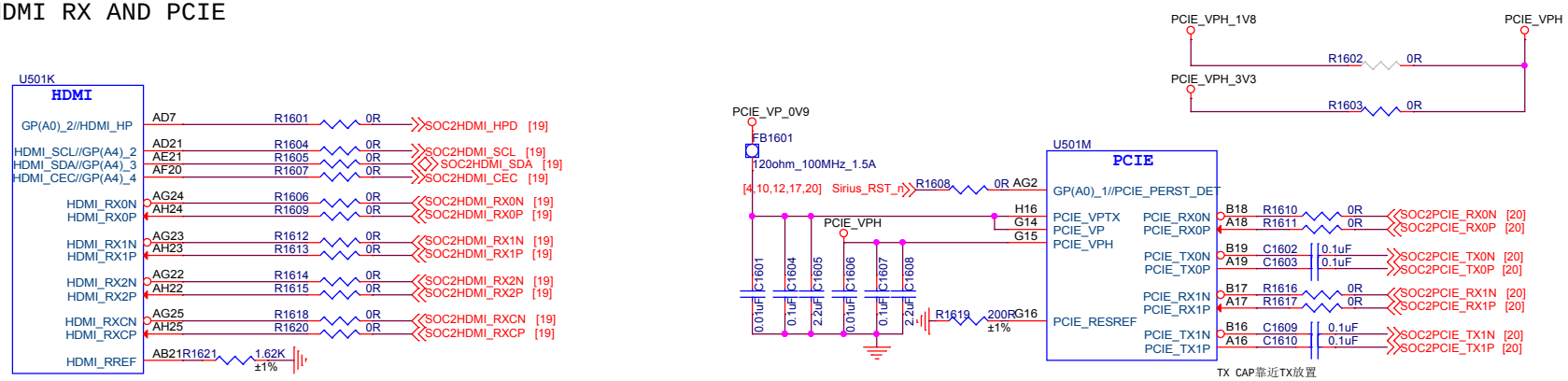
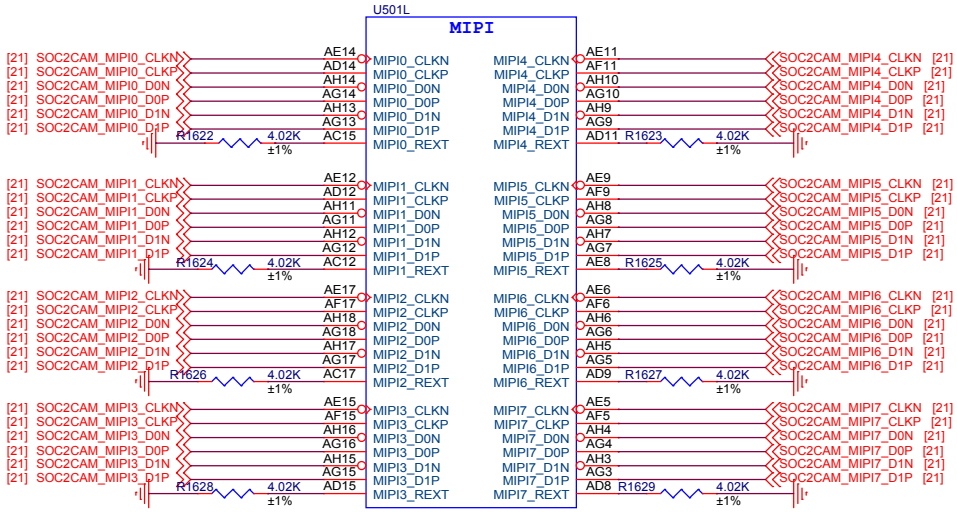
SOC:HDMI RX AND PCIE



SOC:MIPI CSI RX*8 AND TX*2



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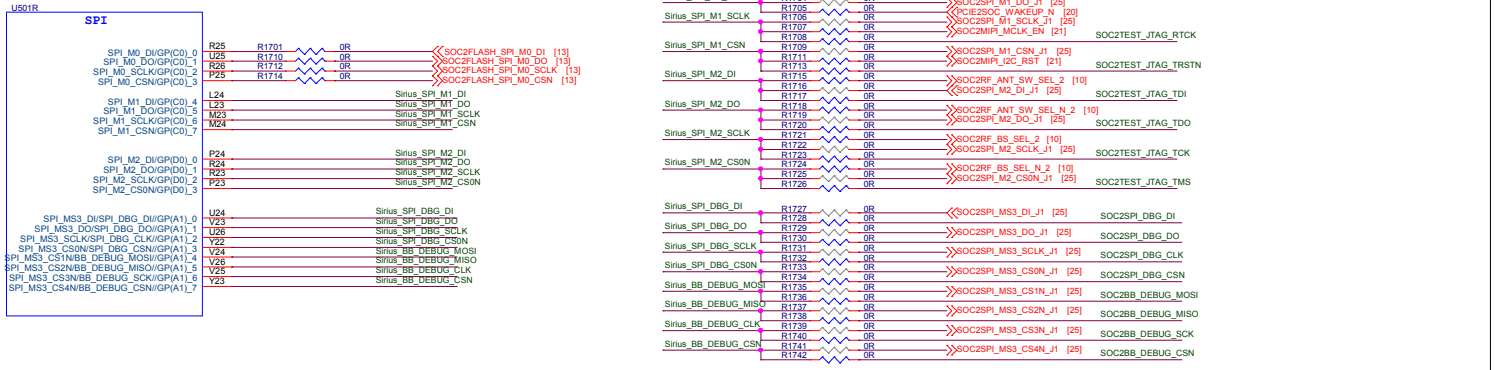
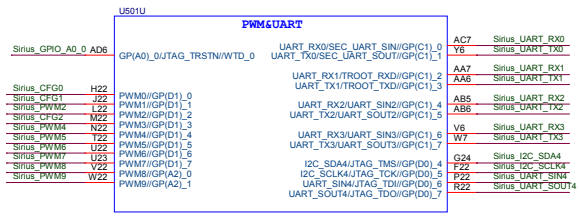
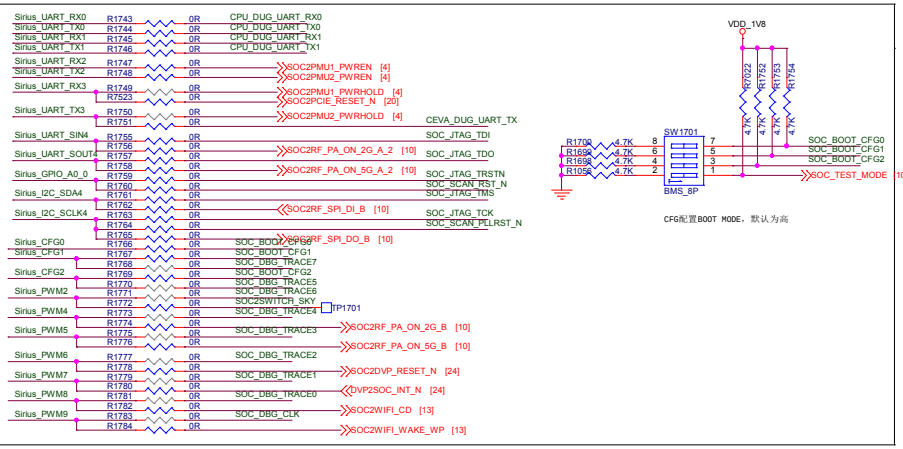
SOC SPI



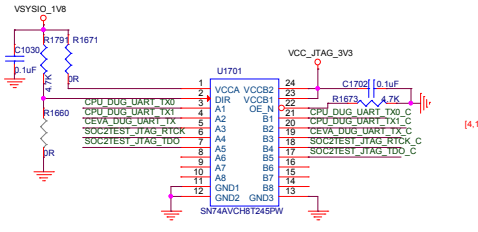
UART&CFG

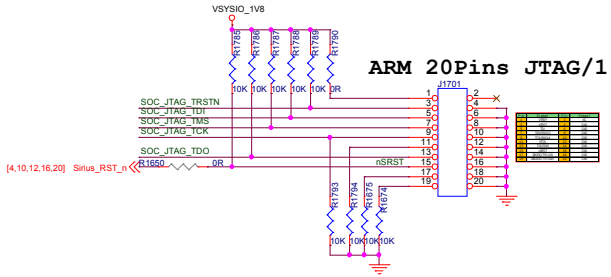


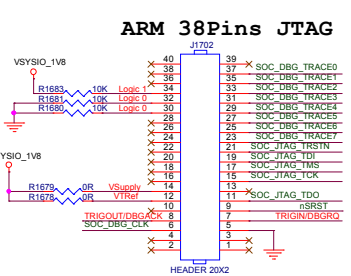
1.8v digital IO

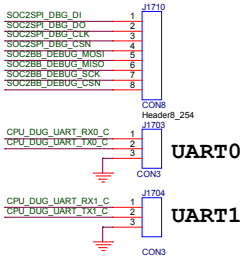


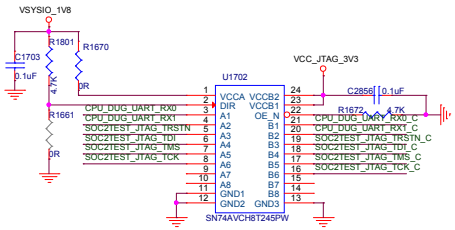
Debug UART & SPI & JTAG

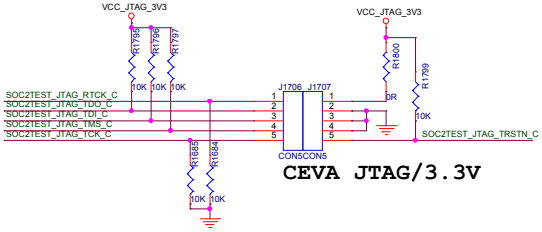












Pin	Signal	Pin	Signal
38	TRACEDATA[0]	37	TRACEDATA[8]
36	TRACECTL	35	TRACEDATA[9]
34	Logic1	33	TRACEDATA[10]
32	Logic0	31	TRACEDATA[11]
30	Logic0	29	TRACEDATA[12]
28	TRACEDATA[1]	27	TRACEDATA[13]
26	TRACEDATA[2]	25	TRACEDATA[14]
24	TRACEDATA[3]	23	TRACEDATA[15]
22	TRACEDATA[4]	21	nTRST
20	TRACEDATA[5]	19	TDI
18	TRACEDATA[6]	17	TMS/SWDIO
16	TRACEDATA[7]	15	TCK/SWCLK
14	VSupply	13	RTCK
12	VTRef	11	TDO/SWO
10	No connection	9	nSRST
8	TRIGOUT/DBGACK	7	TRIGIN/DBGRQ
6	TRACECLK	5	GND
4	No connection	3	No connection
2	No connection	1	No connection

TRIGIN/DBGRQ R1677 10K
TRIGOUT/DBGACK R1676 10K

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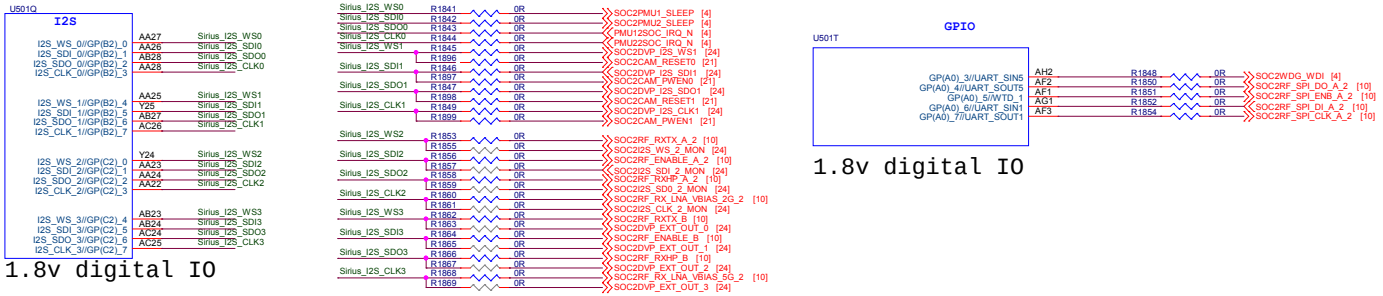
Sirius DVP

DVP 0和MON OUT复用接口
DVP 1和MON OUT复用接口
DVP 0和TYPE C 兼容设计

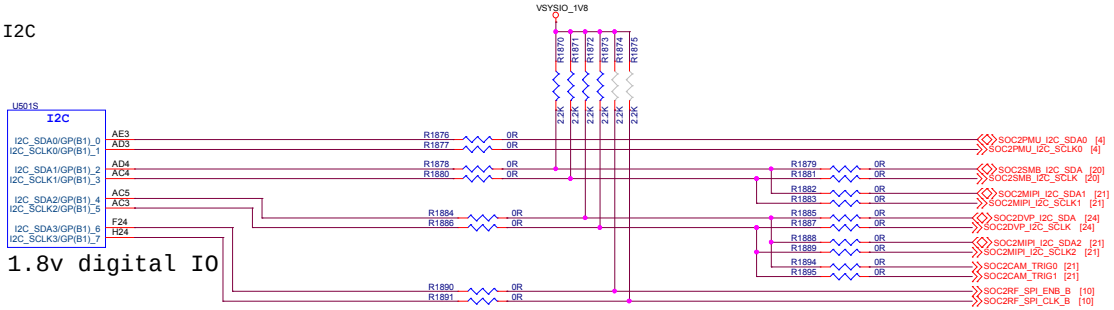
Sirius I2S&GPIO



1.8v digital IO

1.8v digital IO

Sirius I2C



1.8v digital IO

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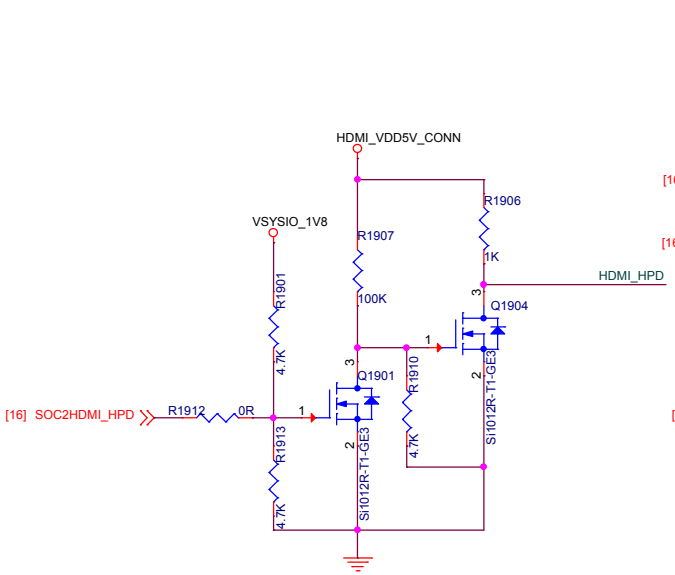
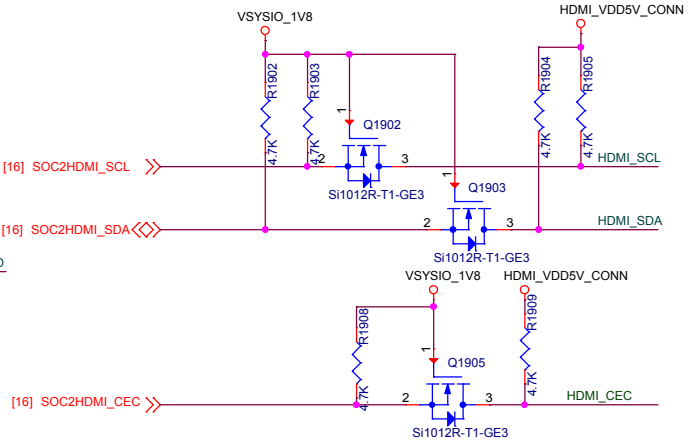
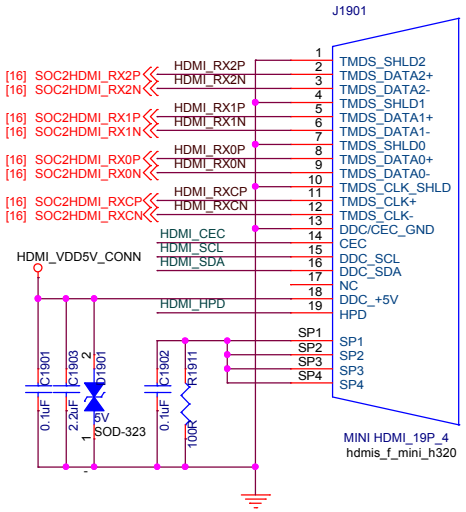
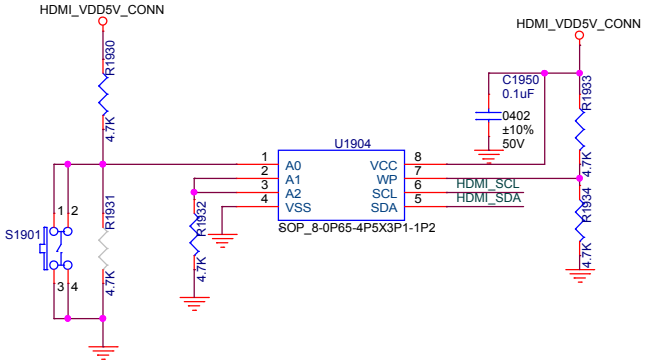
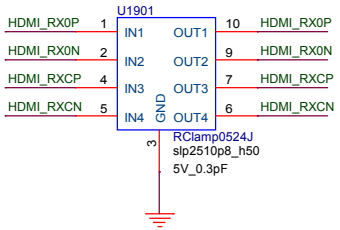


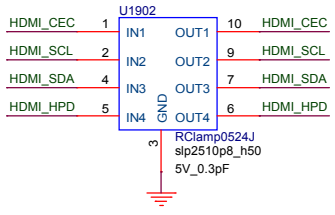


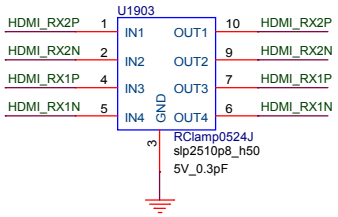


VBUS=5V
TVS器件重新选型！！！









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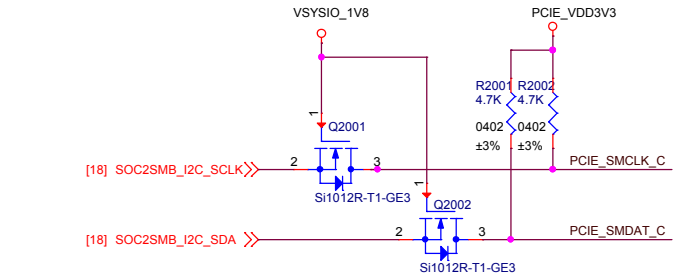

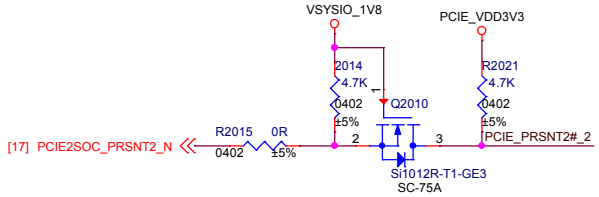

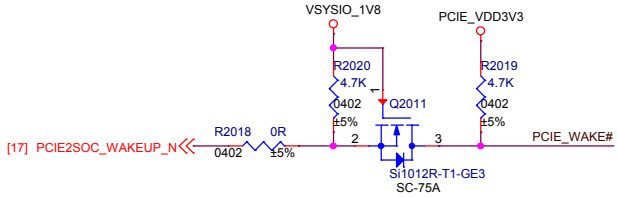

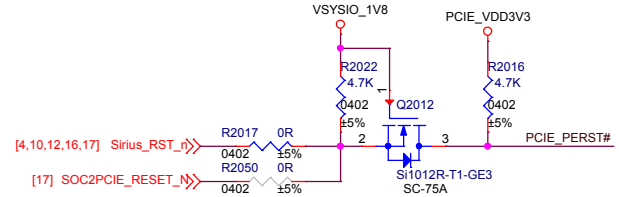

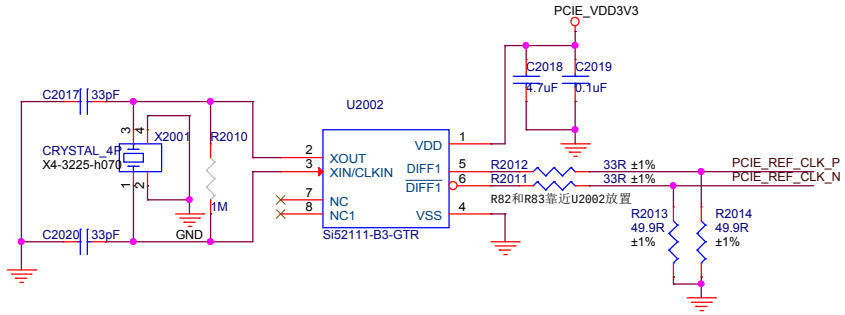

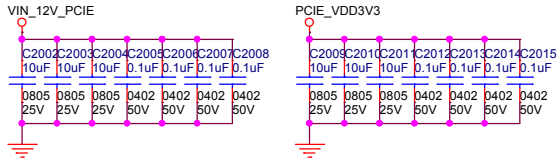

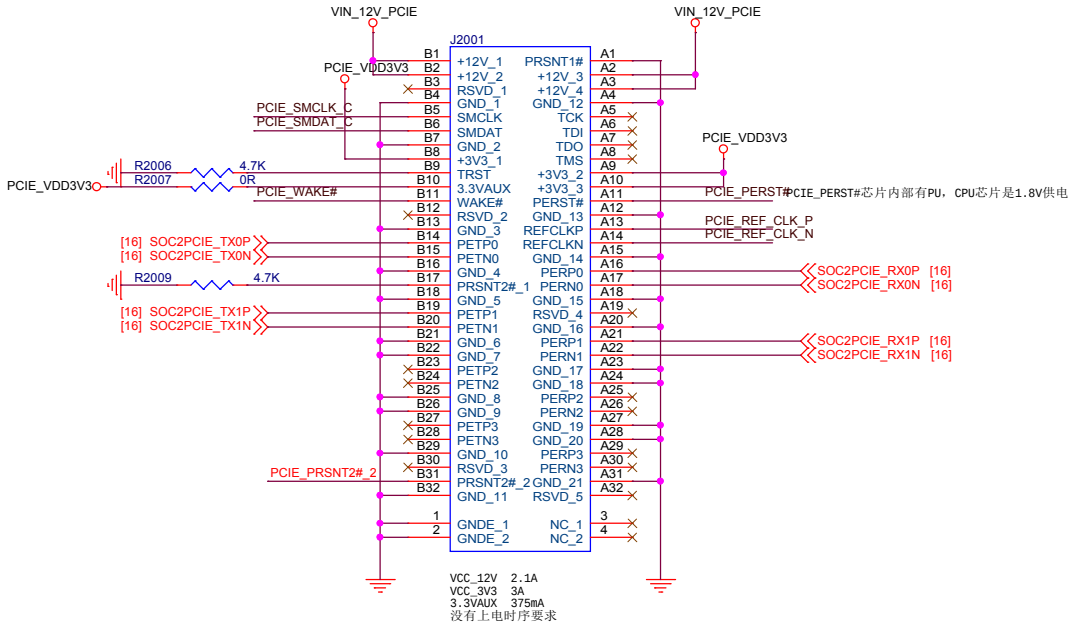

PCIE接口保护？

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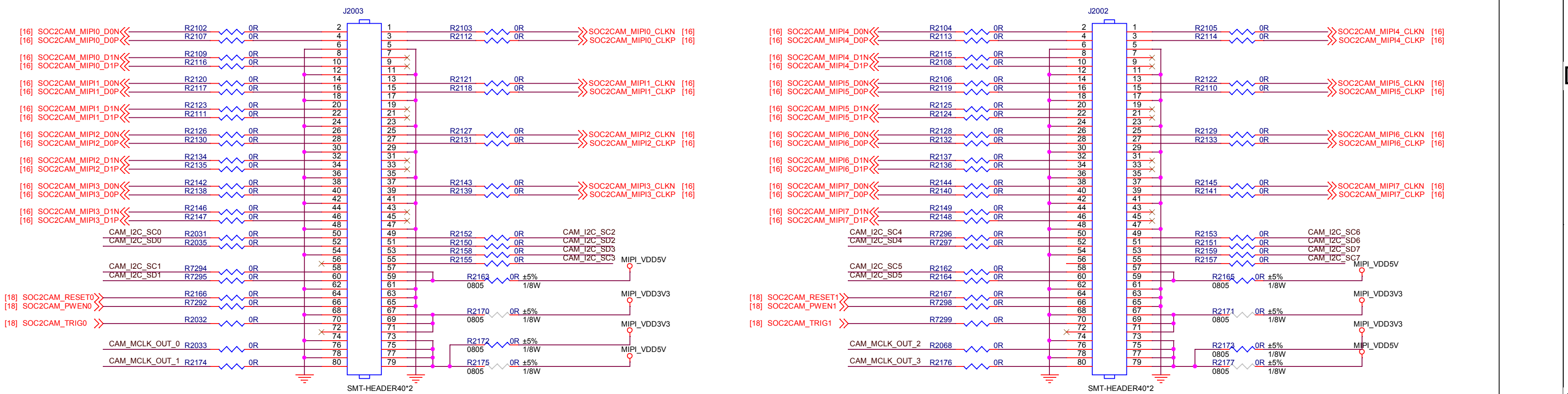
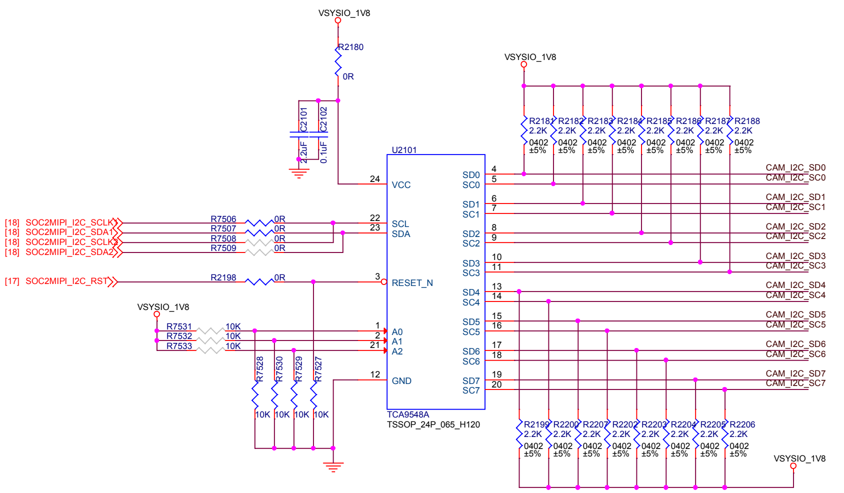
Sensor Connecter



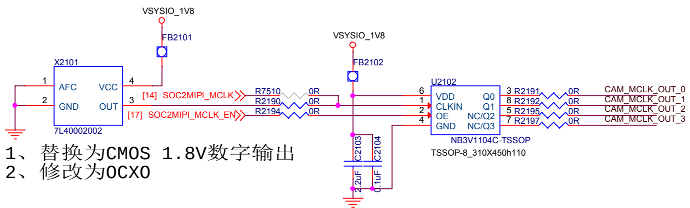
接口定义

4Lane 时使用为pin13/15, pin37/39
需要重新做转接板？
同一个sensor需要使用
同一个clk到sensor

Sensor I2C Switch

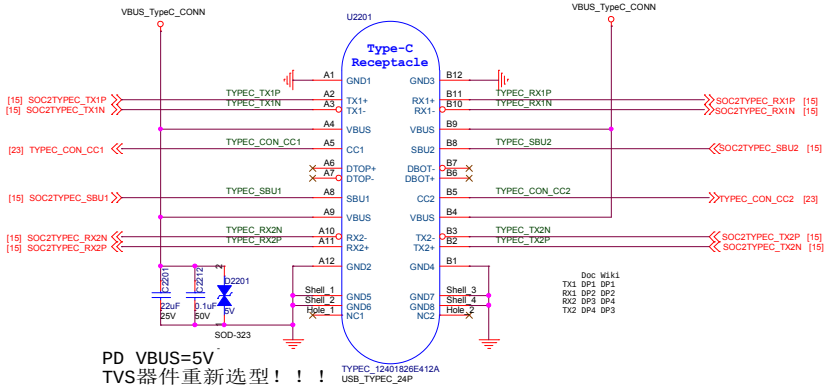


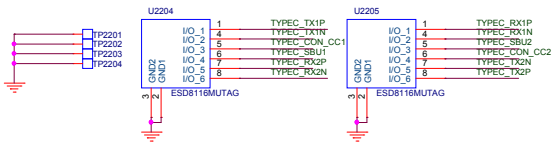
Sensor MLCK router



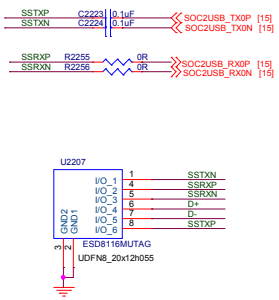
1、替换为CMOS 1.8V数字输出
2、修改为OCXO

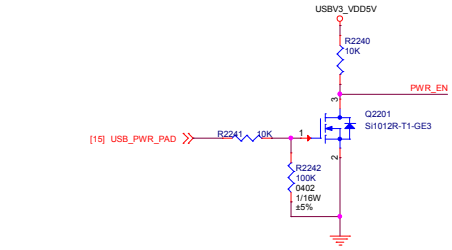
TYPE C Conn：USB3.0、DP and PD

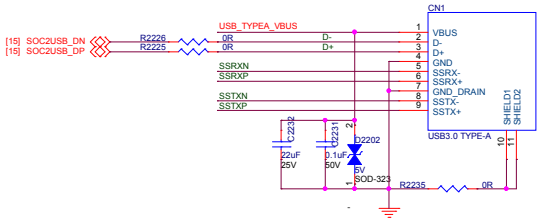


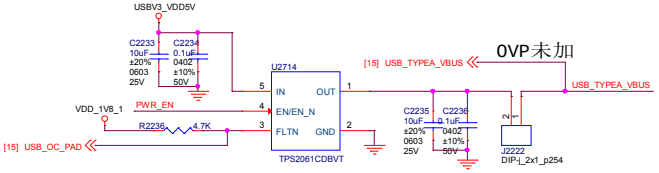


TYPE A Conn：USB3.0 and USB2.0









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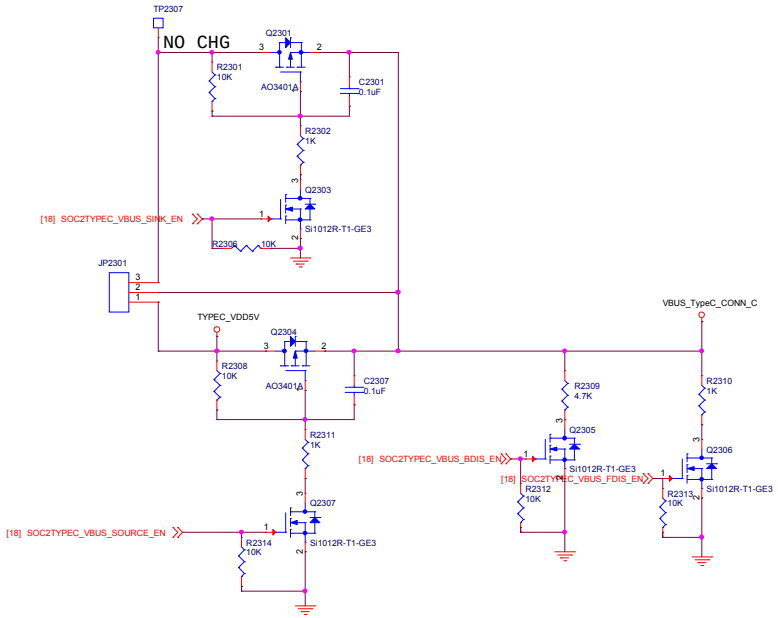
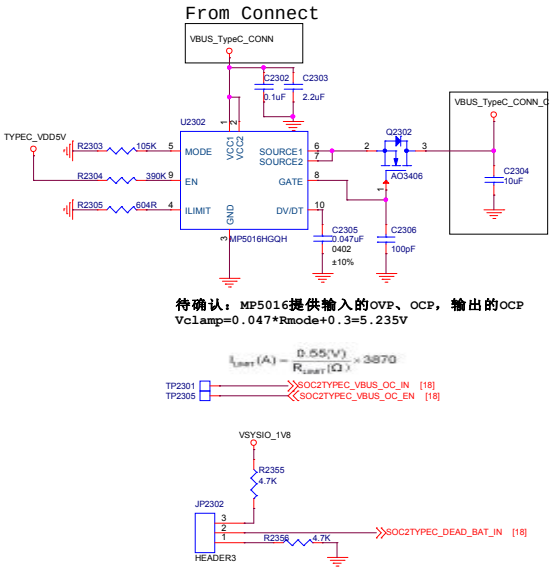
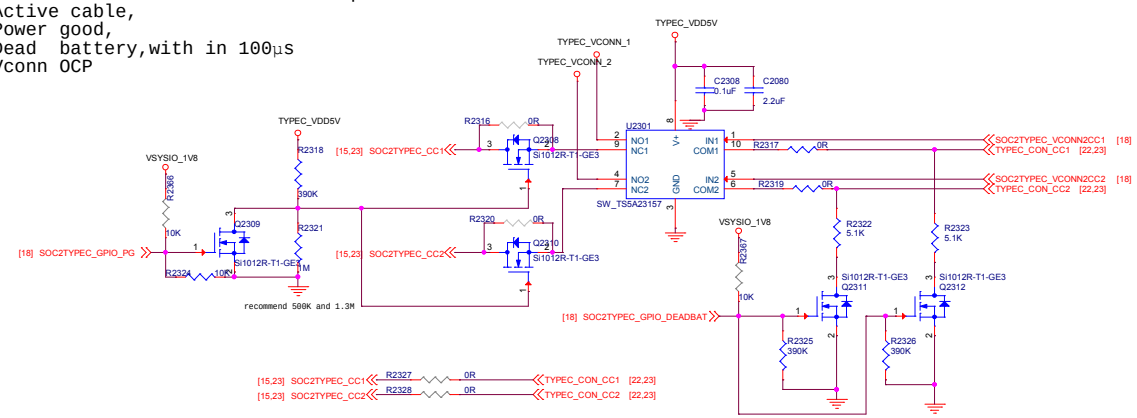
PD Feature option:
1)Discharge,2)Sink/chg and source router

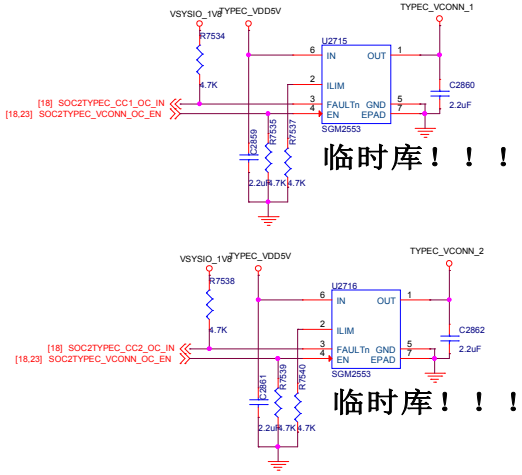


PD Feature option:
1)Input OVP,2)VBUS Input/Output OCP



Type C cc Feature and PD Feature option:
1)Active cable,
2)Power good,
3)Dead battery,with in 100μs
4)Vconn OCP





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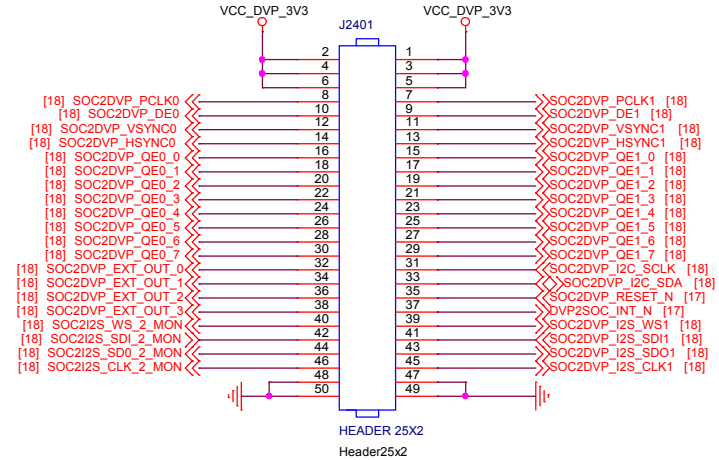

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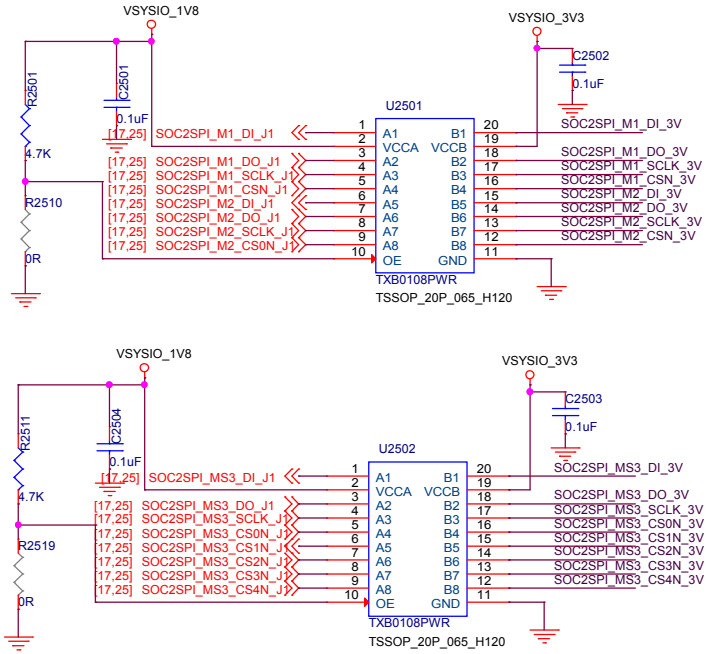

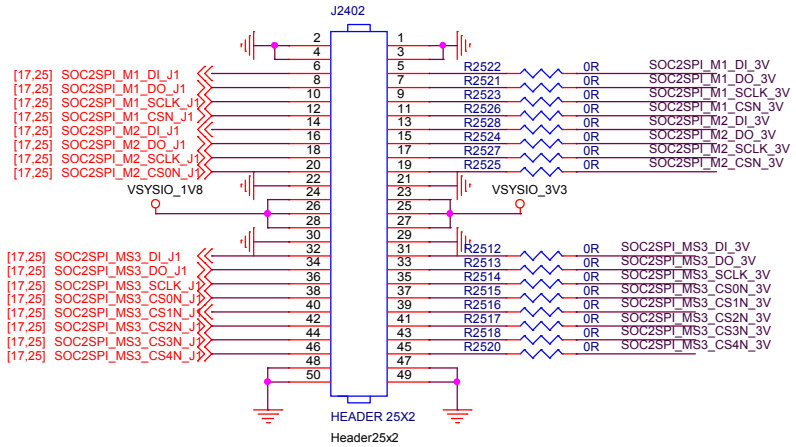

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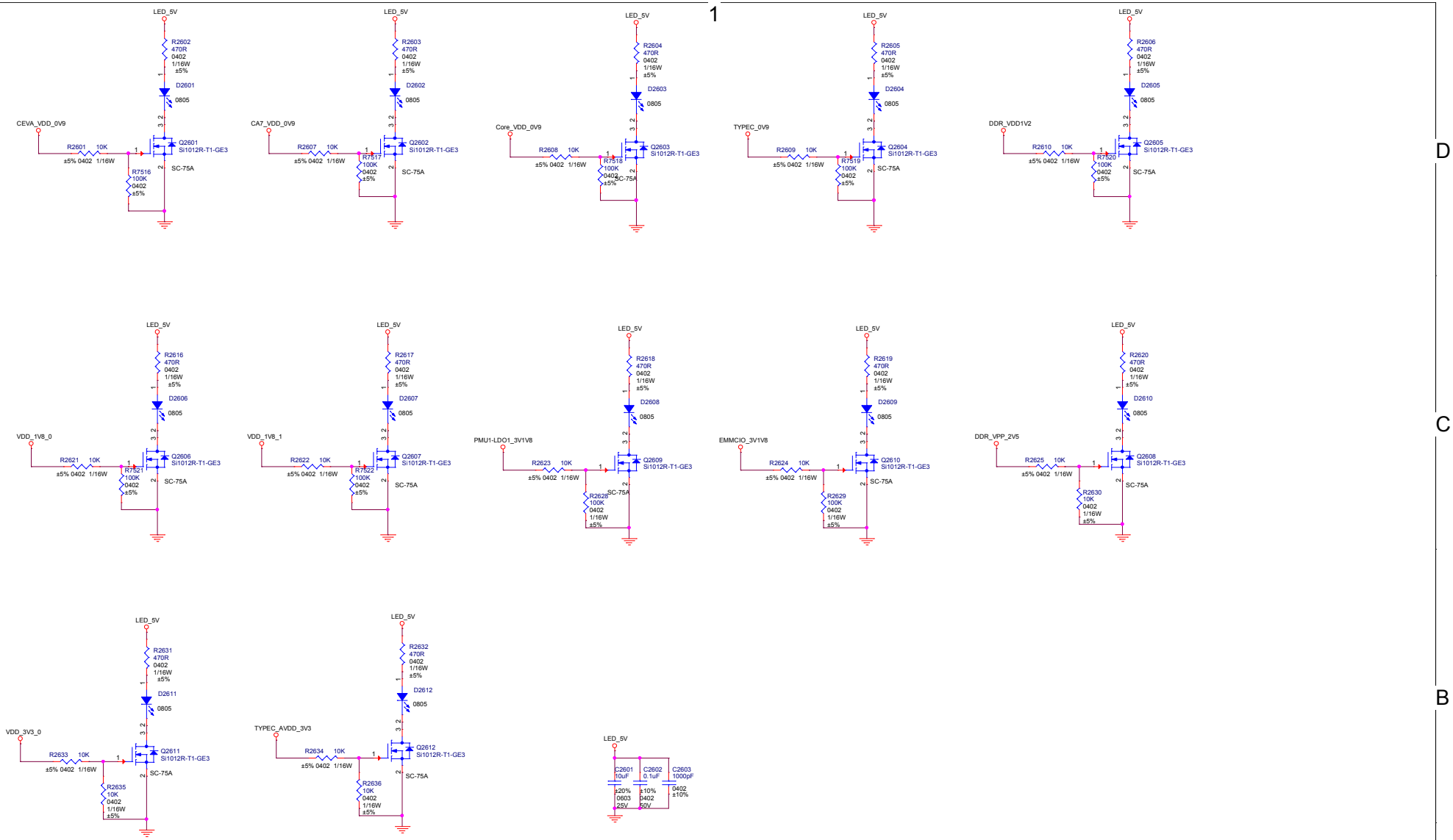

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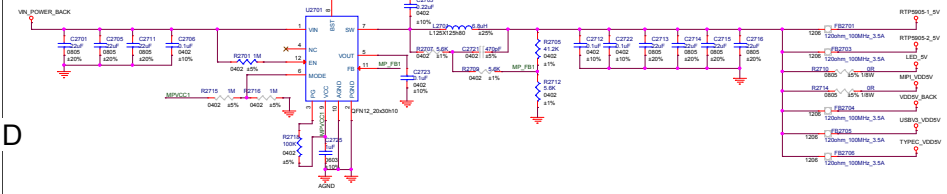
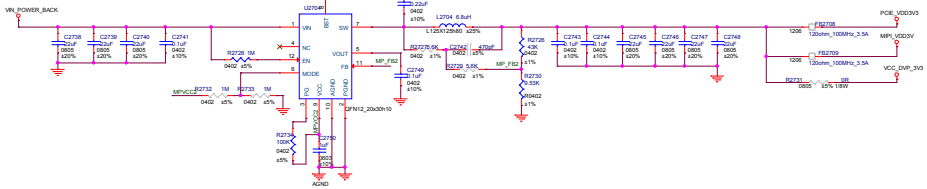
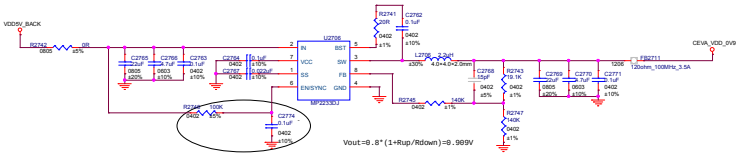
5V POWER BACKUP



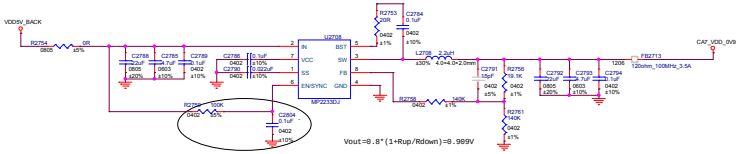
3.3V POWER BACKUP



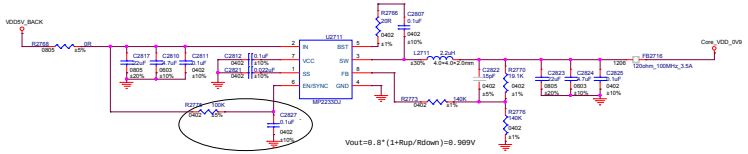
0.9V FOR CEVA POWER BACKUP



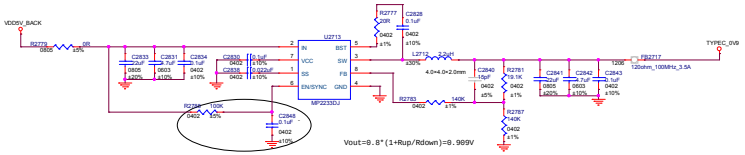
0.9V FOR CA7 POWER BACKUP



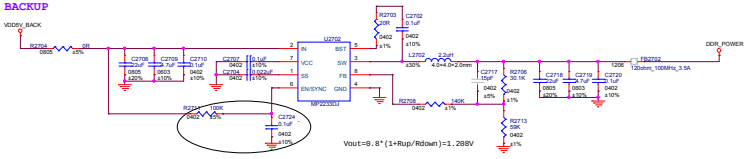
0.9V FOR CORE POWER BACKUP



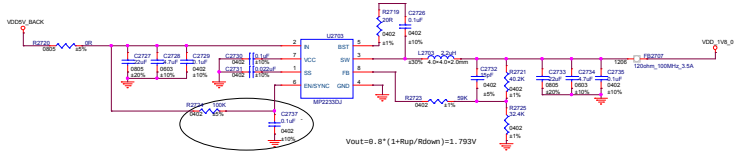
0.9V FOR TYPEC POWER BACKUP



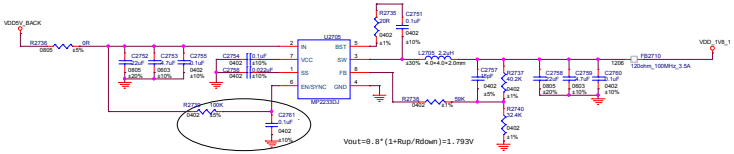
1.2V FOR DDR4 POWER BACKUP



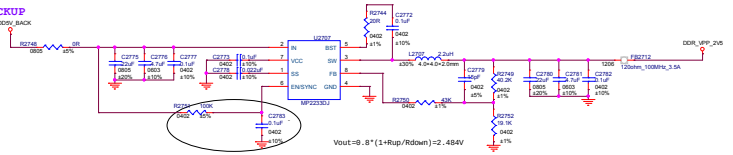
1.8V POWER BACKUP1



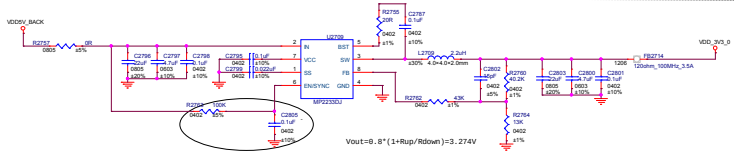
1.8V POWER BACKUP2



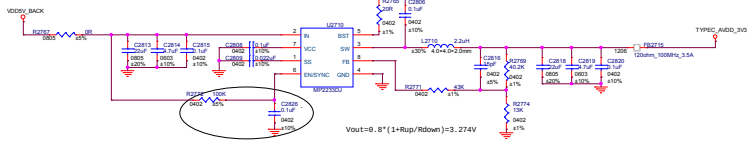
2.5V FOR DDR4 POWER BACKUP



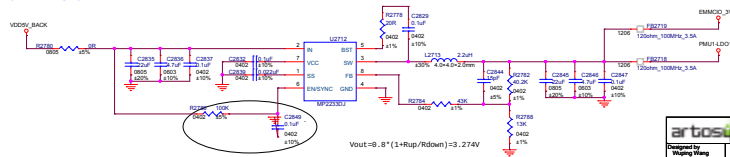
3.3V POWER BACKUP



3.3V FOR TYPEC POWER BACKUP



3.3V FOR SDIO/EMMCIO POWER BACKUP



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