**Version 0.1**

**2017-12-06**

**DSI\_TX ASIC Design Spec**

**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Version | Author | Comments |
| 2017/12/06 | 0.1 | Zheng Xie | Initial Version |
|  |  |  |  |

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1. **DSI\_TX Top** 
   1. **DSI\_TX Top Feature**

The main features of DSI\_TX Top is as follows:

* Max support four data lane, 2.5Gbps/lane.
* Support all the datatype defined in DSI specification v1.2. Included
  + YUV420\_8
  + YUV422\_8/YUV422\_10
  + RGB444/RGB565/RGB666/RGB888/RGB\_10
* Support all kinds of display module;
  + TYPY1: Frame Memory
  + TYPY2: Partial-frame Memory
  + TYPY3: No-frame Memory
  1. **DSI\_TX Top Interface**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **In/out** | **Width** | **Sync dom** | **description** |
| dsi\_rstn | In | 1 | Async | System rstn, low active |
| **APB Interface** | | | | |
| apb\_clk | In | 1 | N/A | 150Mhz, From NOC |
| apb\_rstn | In | 1 | Async |  |
| apb\_sel | In | 1 | apb\_clk |  |
| apb\_write | In | 1 | apb\_clk |  |
| apb\_enable | In | 1 | apb\_clk |  |
| apb\_ready | In | 1 | apb\_clk |  |
| apb\_addr | In | [9:0] | apb\_clk |  |
| apb\_wdata | In | [31:0] | apb\_clk |  |
| apb\_rdata | Out | [31:0] | apb\_clk |  |
| **Display Engine interface** | | | | |
| dis\_clk | in | 1 | N/A | Max476Mhz |
| dis\_vsync | in | 1 | dis\_clk | Vertical sync signal |
| dis\_hsync | in | 1 | dis\_clk | Horizontal sync signal |
| dis\_de | in | 1 | dis\_clk | Pixel data valid signal |
| dis\_data | in | [29:0] | dis\_clk | Pixel data |
| **PPI Control Signals** | | | | |
| rstn | out | 1 | async |  |
| shutdown | out | 1 | async |  |
| masterslave | out | 1 | async |  |
| enableclk | out | 1 | async |  |
| enable\_data | out | [3:0] | async |  |
| **PPI Clock Lane Signals** | | | | |
| txbyteclkhs | In | 1 | --- | Max 312.5Mhz, From PLL |
| txrequesthsclk | out | 1 | txbyteclkhs |  |
| txulpsclk | out | 1 | txclkesc |  |
| txulpsexitclk | out | 1 | txclkesc |  |
| **PPI High-Speed Data TX Signals** | | | | |
| txclkesc | in | 1 | --- | Max 20Mhz, External |
| txrequestdatahs | Out | [3:0] | txbyteclkhs |  |
| txreadyhs | In | [3:0] | txbyteclkhs |  |
| txdatahs | Out | [31:0] | txbyteclkhs |  |
| **PPI Escape Mode TX Signals** | | | | |
| turnrequest | out | 1 | txclkesc |  |
| direction | In | 1 | txclkesc |  |
| txrequestesc | Out | 1 | txclkesc |  |
| txlpdtesc | Out | 1 | txclkesc |  |
| txreadyesc | In | 1 | txclkesc |  |
| txvalidesc | Out | 1 | txclkesc |  |
| txdataesc | Out | [7:0] | txclkesc |  |
| **PPI Escape Mode RX Signals** | | | | |
| rxclkesc | in | 1 | N/A |  |
| rxlpdtesc | in | 1 | rxclkesc |  |
| rxvalidesc | in | 1 | rxclkesc |  |
| rxdataesc | in | [7:0] | rxclkesc |  |

* 1. **DSI\_TX Top architecture**



* 1. **DSI\_TX Clock Domain**



Note: 1. Is Txbyteclk alwasys on? ?? <SIM With CSI TX>

If PLL is not lock, switch to TXCLKESC.

2. The ram size and data mapping in pixel2byte module.

4096X36 🡪 1152X128

3. Colour space switch.

RGB🡪YUV444; data discard before writing into ram.

4. The data process in RXCLKESC domain? < <Reference MIPI dphy>>

1. **Sub Module**
   1. **DEIF**
      1. **DEIF Interface**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **In/out** | **Width** | **Sync dom** | **description** |
| dis\_clk\_de | In | 1 | N/A | Max 457Mhz |
| dis\_rstn\_de | In | 1 | Async | Sync From System rstn |
| dis\_clk\_cgu | In | 1 | N/A | Max 457Mhz |
| dis\_rstn\_cgu | In | 1 | Async | Sync From System rstn |
| txbyteclk | In | 1 | N/A | Max 312.5Mhz |
| txbyte\_rstn | In | 1 | Async | Sync From System rstn |
| **Display Engine interface** | | | | |
| dis\_vsync | in | 1 | dis\_clk | Vertical sync signal |
| dis\_hsync | in | 1 | dis\_clk | Horizontal sync signal |
| dis\_de | in | 1 | dis\_clk | Pixel data valid signal |
| dis\_data | in | [29:0] | dis\_clk | Pixel data |
| **Patten\_Gen Interface** | | | | |
| pg\_enable | In | 1 | txbyteclk |  |
| pg\_format | In | [3:0] | txbyteclk |  |
| pg\_mode | In | [3:0] | txbyteclk |  |
| pg\_hsa | In | [15:0] | txbyteclk |  |
| pg\_hbp | In | [15:0] | txbyteclk |  |
| pg\_hfp | In | [15:0] | txbyteclk |  |
| pg\_hactive | In | [15:0] | txbyteclk |  |
| pg\_vsa | In | [15:0] | txbyteclk |  |
| pg\_vbp | In | [15:0] | txbyteclk |  |
| pg\_vfp | In | [15:0] | txbyteclk |  |
| pg\_vactive | In | [15:0] | txbyteclk |  |
| **Output interface** | | | | |
| vsync\_sync | Out | 1 | txbyteclk | Sync Vertical sync signal |
| hsync\_sync | Out | 1 | txbyteclk | Sync Horizontal sync signal |
| de\_sync | Out | 1 | txbyteclk | Sync Pixel data valid signal |
| data\_sync | Out | [29:0] | txbyteclk | Sync Pixel data |

* + 1. **DEIF Architecture**



* 1. **Timing Det&Gen**
     1. **Timimg Det&Gen Interface**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **In/out** | **Width** | **Sync dom** | **description** |
| txbyteclk | In | 1 | N/A | Max 312.5Mhz |
| txbyte\_rstn | In | 1 | Async | Sync From System rstn |
| **Input signal** | | | | |
| vsync | in | 1 | txbyteclk | Sync Vertical sync signal |
| Hsync | in | 1 | txbyteclk | Sync Horizontal sync signal |
| De | in | 1 | txbyteclk | Sync Pixel data valid signal |
| **Output signal** | | | | |
| hsa | Out | [15:0] | txbyteclk | Horizontal active time |
| hbp | Out | [15:0] | txbyteclk | Horizontal back porch time |
| hfp | Out | [15:0] | txbyteclk | Horizontal front porch time |
| htotal | Out | [15:0] | txbyteclk | Horizontal total time |
| vcnt | Out | [15:0] | txbyteclk | Line cnt |
| hcnt | Out | [15:0] | txbyteclk | Pixel cnt |

* + 1. **Timimg Det&Gen Architecture**



* 1. **Pixel2byte**
     1. **Pixel2byte Interface**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **In/out** | **Width** | **Sync dom** | **description** |
| txbyteclk | In | 1 | N/A | Max 312.5Mhz |
| txbyte\_rstn | In | 1 | Async | Sync From System rstn |
| **Input signal** | | | | |
| data\_type | in | [3:0] | txbyteclk | Data format of input video |
| vsync | in | 1 | txbyteclk | Sync Vertical sync signal |
| hsync | in | 1 | txbyteclk | Sync Horizontal sync signal |
| de | in | 1 | txbyteclk | Sync Pixel data valid signal |
| pix\_data | in | [29:0] | txbyteclk | Sync Pixel data |
| lane\_num | in | [1:0] | txbyteclk | Data lane used |
| rd\_start | in | 1 | txbyteclk | Start output |
| **output signal** | | | | |
| Payload\_valid | out | [3:0] | txbyteclk |  |
| payload | out | [31:0] | txbyteclk |  |

* + 1. **Pixel2byte Architecture**



* 1. **Display Init**
     1. **Display Init Interface**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **In/out** | **Width** | **Sync dom** | **description** |
| txbyteclk | In | 1 | N/A | Max 312.5Mhz |
| txbyte\_rstn | In | 1 | Async | Sync From System rstn |
| **Input signal** | | | | |
| vsync | In |  |  |  |
| Vcnt | In |  |  |  |
| hcnt |  |  |  |  |
| display\_init\_reg | in | [31:0] |  |  |
| **PPI Escape Mode RX Signals** | | | | |
| rxdataesc | in | [7:0] | rxclkesc |  |
| rxvalidesc | In | 1 | rxclkesc |  |
| **PPI Escape Mode TX Signals** | | | | |
| txvalidesc | Out | 1 | txclkesc |  |
| txdataesc | Out | [7:0] | txclkesc |  |

* + 1. **Display Init Architecture**

The process of display initialization is working through software.The CPU send a packet command set to DSITX and DSITX will execute it as order and feedback data to cpu. Data architecture of packet with control signal is as follows:



The architecture of it is as follow:



* 1. **Command Mode**
     1. **Command Mode Interface**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **In/out** | **Width** | **Sync dom** | **description** |
| txbyteclk | In | 1 | N/A | Max 312.5Mhz |
| txbyte\_rstn | In | 1 | Async | Sync From System rstn |
| **Input signal** | | | | |
| Payload\_valid | In | [3:0] | txbyteclk |  |
| payload | In | [31:0] | txbyteclk |  |
| cyc\_cnt | In | [15:0] | txbyteclk |  |
| line\_cnt | In | [15:0] | txbyteclk |  |
| **Output signal** | | | | |
| lp\_triger | out | 1 | txbyteclk |  |
| Format\_change | Out | 1 | txbyteclk |  |
| Packet\_type | Out | [3:0] | Txbyteclk |  |
| Word\_count | out | [15:0] | txbyteclk |  |

* + 1. **Command Mode Architecture**



* 1. **Video Mode**
     1. **Video Mode Interface**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **In/out** | **Width** | **Sync dom** | **description** |
| txbyteclk | In | 1 | N/A | Max 312.5Mhz |
| txbyte\_rstn | In | 1 | Async | Sync From System rstn |
| **Input signal** | | | | |
| lane\_num | in | [1:0] | txbyteclk |  |
| vsa | In | [15:0] | txbyteclk |  |
| vbp | In | [15:0] | Txbyteclk |  |
| vfp | In | [15:0] | txbyteclk |  |
| vact | in | [15:0] | txbyteclk |  |
| hsa | Out | [15:0] | txbyteclk | Horizontal active time |
| hbp | Out | [15:0] | txbyteclk | Horizontal back porch time |
| htotal | Out | [15:0] | txbyteclk | Horizontal total time |
| **Output signal** | | | | |
| lpm\_triger | out | 1 | txbyteclk |  |
| new\_packet\_start | Out | 1 | txbyteclk |  |
| packet\_type | Out | [3:0] | Txbyteclk |  |
| word\_count | out | [15:0] | txbyteclk |  |

* + 1. **Video Mode Architecture**



* 1. **Protocol Layer**
     1. **Protocol Layer Interface**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **In/out** | **Width** | **Sync dom** | **description** |
| txbyteclk | In | 1 | N/A | Max 312.5Mhz |
| txbyte\_rstn | In | 1 | Async | Sync From System rstn |
| **Input signal** | | | | |
| Tx\_readyhs | in | 1 | txbyteclk |  |
| Virtual\_channel | In | [1:0] | txbyteclk |  |
| Data\_format | In | [5:0] | txbyteclk |  |
| Word\_counter | In | [15:0] | txbyteclk |  |
| Payload\_valid | In | [3:0] | txbyteclk |  |
| payload | In | [31:0] | txbyteclk |  |
| **output signal** | | | | |
| Payload\_read | In | 1 | txbyteclk |  |
| data\_valid | Out | [3:0] | txbyteclk |  |
| Byte\_data | out | [31:0] | txbyteclk |  |

* + 1. **Protocol Layer Architecture**



* 1. **Dphyif**
     1. **Dphyif Interface**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PPI interface** | | | | |
| txbyteclkhs | In | 1 | --- | Max 312.5Mhz, From PLL |
| txclkesc | in | 1 | --- | Max 20Mhz, External |
| **PPI Control Signals** | | | | |
| rstn | out | 1 | async |  |
| shutdown | out | 1 | async |  |
| masterslave | out | 1 | async |  |
| enableclk | out | 1 | async |  |
| enable\_data | out | [3:0] | async |  |
| **PPI Clock Lane Signals** | | | | |
| txrequesthsclk | out | 1 | txbyteclkhs |  |
| txulpsclk | out | 1 | txclkesc |  |
| txulpsexitclk | out | 1 | txclkesc |  |
| **PPI High-Speed Data TX Signals** | | | | |
| txreadyhs | In | [3:0] | txbyteclkhs |  |
| txrequestdatahs | Out | [3:0] | txbyteclkhs |  |
| txdatahs | Out | [31:0] | txbyteclkhs |  |
| **PPI Escape Mode TX Signals** | | | | |
| txrequestesc | Out | 1 | txclkesc |  |
| txlpdtesc | Out | 1 | txclkesc |  |
| txreadyesc | In | 1 | txclkesc |  |
| txvalidesc | Out | 1 | txclkesc |  |
| txdataesc | Out | [7:0] | txclkesc |  |
| turnrequest | out | 1 | txclkesc |  |
| direction | In | 1 | txclkesc |  |
| **PPI Escape Mode RX Signals** | | | | |
| rxclkesc | in | 1 | N/A |  |
| rxlpdtesc | in | 1 | rxclkesc |  |
| rxvalidesc | in | 1 | rxclkesc |  |
| rxdataesc | in | [7:0] | rxclkesc |  |

* + 1. **Dphyif Architecture**



1. **Register List**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Register name** | **address** | **width** | **R/W** | **Description** |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

**Appendix A**

**A.1 Initialization Flow of Display**



**A.2 DCS Packet**

DCS is a standardized command set intended for Command Mode display modules.There is four kinds of packet about read/write.

* **DCS Short Write Command, 0 or 1 parameter, Data Types = 00 0101 (0x05), 01** 1309 **0101 (0x15), Respectively**



* **DCS Read Request, No Parameters, Data Type = 00 0110 (0x06)**



The peripheral shall respond to DCS READ Request in one of the following ways:

* If an error was detected by the peripheral, it shall send Acknowledge and Error Report. If an ECC error in the request was detected and corrected, the peripheral shall send the requested READ data packet followed by the Acknowledge and Error Report packet in the same transmission.
* If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled.
* **DCS Long Write / write\_LUT Command, Data Type = 11 1001 (0x39)**



* **Set Maximum Return Packet Size, Data Type = 11 0111 (0x37)**

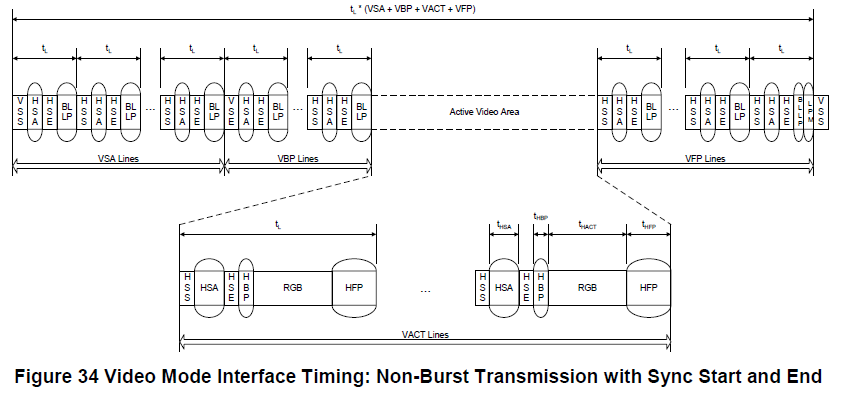


**A.3 Display Control command**

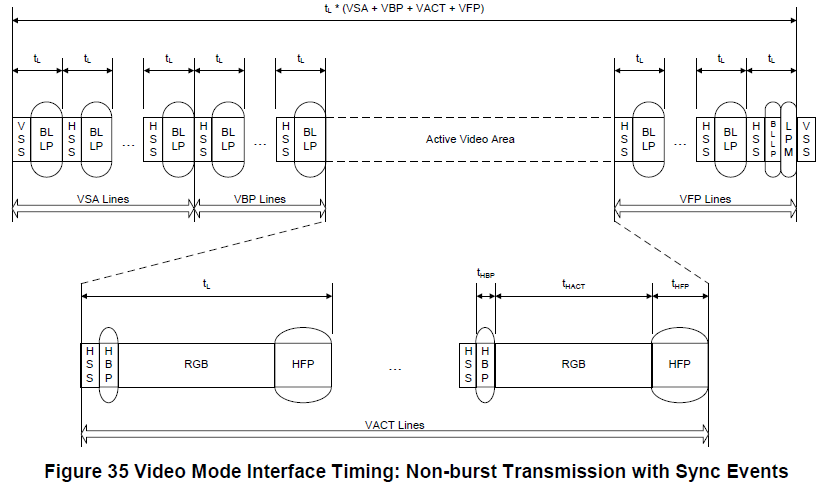
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Command** | **address** | **parameter** | **R/W** | **Description** |
| **DCS command** | | | | |
| set\_display\_on | 29h | 0 | W |  |
| set\_display\_off | 28h | 0 | W |  |
| set\_gamma\_curve | 26h | 1 | W |  |
| enter\_idle\_mode | 39h | 0 | W |  |
| enter\_invert\_mode | 21h | 0 | W |  |
| enter\_normal\_mode | 13h | 0 | W |  |
| set\_partial\_columns | 31h | 4 | w |  |
| set\_partial\_rows | 30h | 4 | w |  |
| enter\_partial\_mode | 12h | 0 | W |  |
| enter\_sleep\_mode | 10h | 0 | w |  |
| exit\_idle\_mode | 38h | 0 | w |  |
| exit\_invert\_mode | 20h | 0 | w |  |
| exit\_sleep\_mode | 11h | 0 | w |  |
| get\_address\_mode | 0bh | 1 | R |  |
| get\_blue\_channel | 08h | 1 | R |  |
| get\_diagnostic\_result | 0fh | 1 | R |  |
| get\_display\_mode | 0dh | 1 | R |  |
| get\_green\_channel | 07h | 1 | R |  |
| get\_pixel\_format | 0ch | 1 | R |  |
| get\_power\_mode | 0AH | 1 | R |  |
| get\_red\_channel | 0AH | 1 | R |  |
| get\_scanline | 45H | 2 | R |  |
| get\_signal\_mode | 0EH | 1 | R |  |
| nop | 00H | 0 | W |  |
| read\_DDB\_continue | A8H | variable | R |  |
| read\_DDB\_start | A1H | variable | R |  |
| read\_memory\_continue | 3EH | variable | R |  |
| read\_memory\_start | 2EH | variable | R |  |
| set\_3D\_control | 3DH | 2 | W |  |
| set\_address\_mode | 36H | 1 | W |  |
| set\_column\_address | 2AH | 4 | W |  |
| set\_page\_address | 2BH | 4 | W |  |
| set\_pixel\_format | 3AH | 1 | W |  |
| set\_scroll\_area | 33H | 6 | W |  |
| set\_scroll\_start | 37H | 2 | W |  |
| set\_tear\_off | 34H | 0 | W |  |
| set\_tear\_on | 35H | 1 | W |  |
| set\_tear\_scanline | 44H | 2 | W |  |
| set\_vsync\_timing | 40H | 1 | W |  |
| soft\_reset | 01H | 0 | W |  |
| write\_LUT | 2DH | variable | w |  |
| write\_memory\_continue | 3ch | variable | w |  |
| write\_memory\_start | 2ch | variable | w |  |
| **Non DCS Command** | | | | |
| Compression Mode Command | 0x07 |  |  |  |
| Color Mode Off Command | 0x02 |  |  |  |
| Color Mode On Command | 0x12 |  |  |  |
| Shut Down Peripheral Command | 0x22 |  |  |  |
| Turn On Peripheral Command | 0x32 |  |  |  |
| Execute Queue | 0x16 |  |  |  |
| Set Maximum Return Packet Size | 0x37 |  |  | short |
| Null Packet, no data | 0x09 |  |  |  |
| Picture Parameter Set | 0x0a |  |  |  |
| Compressed Pixel Stream | 0x0b |  |  |  |
| **DCS R/W** | | | | |
| DCS Short WRITE, no parameters | 0x05 |  |  |  |
| DCS Short WRITE, 1 parameter | 0x15 |  |  |  |
| DCS READ, no parameters | 0x06 |  |  |  |
| DCS Long Write Packet | 0x39 |  |  |  |

**A4 Video Mode Interface Timing**

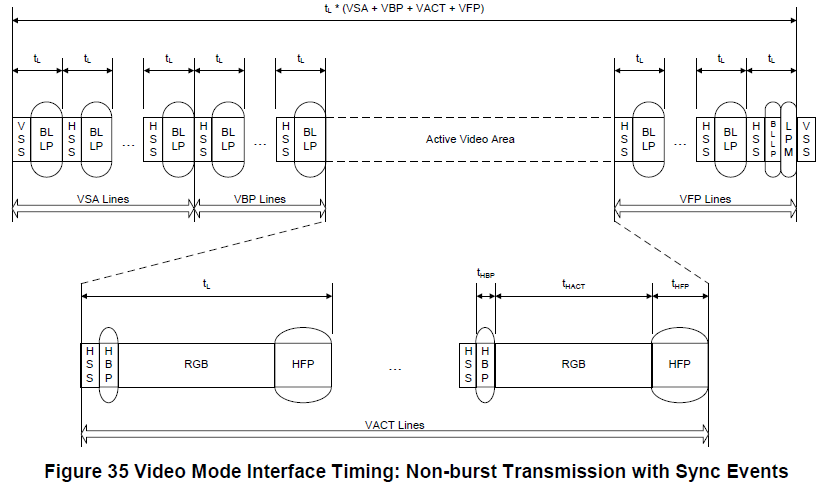
**A4.1 Non-Burst Mode with Sync Pulses**

****

**A4.2 Non-Burst Mode with Sync Events**

****

**A4.3 Burst Mode**

****

**A5 Different Data Type Data Mapping**

