CLN28HP\_8M\_5X2Z\_002.17b.encrypt

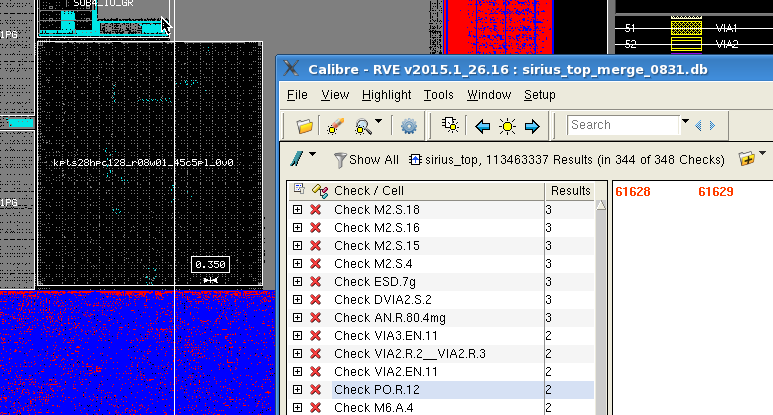
|  |  |  |
| --- | --- | --- |
| **Check** | **Results** | **Comments** |
| ESD.3g | 4 | HDMI(4) |
| ESD.6g | 816 | DDRIO(816) |
| ESD.7g | 3 | ABB(3) |
| ESD.18g | 8 | HDMI(8) |
| ESD.31g | 4 | USB IO (4) |
| ESD.52g | 3 | HDMI(3) |
| HIA.3g | 91 | TypeC(56);PCIe(21);USB(14) |
| HIA.4g | 176 | TypeC(176); |
| HIA.5g | 320 | TypeC(176); MIPI-IO(34\*2);PCIe(76) |
| NW.S.2 | 5 | OTP(5) |
| NW.S.3 | 9 | OTP(9) |
| NW.S.4 | 61 | OTP(61) |
| NW.S.3\_\_NW.S.4:SUGGESTED | 71 | OTP(71) |
| PO.A.3 | 536 | OTP(6) |
| PO.L.3 | 49 | OTP(49) |
| PO.R.12 | 2 | OTP(2) |
| PO.W.17 | 1092 | OTP(1092) |
| PO.DN.3.1 | 1 | Between DDR IO and core, Dummy exclude cover DDR-IO, can’t add PO dummy at that area. Artosyn confirm to waive. |
| DIODMY\_L:WARNING | 1 | Full chip(1), Artosyn waive { @ Each low leakage concern diode must be covered by DIODMY\_L.@ If there's no low leakage diode concern cell in the chip, the violation can be ignored.} |
| MFU.R.1 | 1 | Full chip(1), need Artosyn waive {@ Mask Field Utilization (MFU) is a ratio of mask utilized region which is calculated by (multiple die area + scribe\_line area) / (scanner maximum field area) >= 80%} |
| SRAM.WARN.1 | 1 | Full chip(1), need Artosyn waive memory redundancy missing |
| **Total** | **3255** |  |

CN28\_LEADFREE\_BUILD\_UP\_BUMP\_8M\_5X2Z.12a

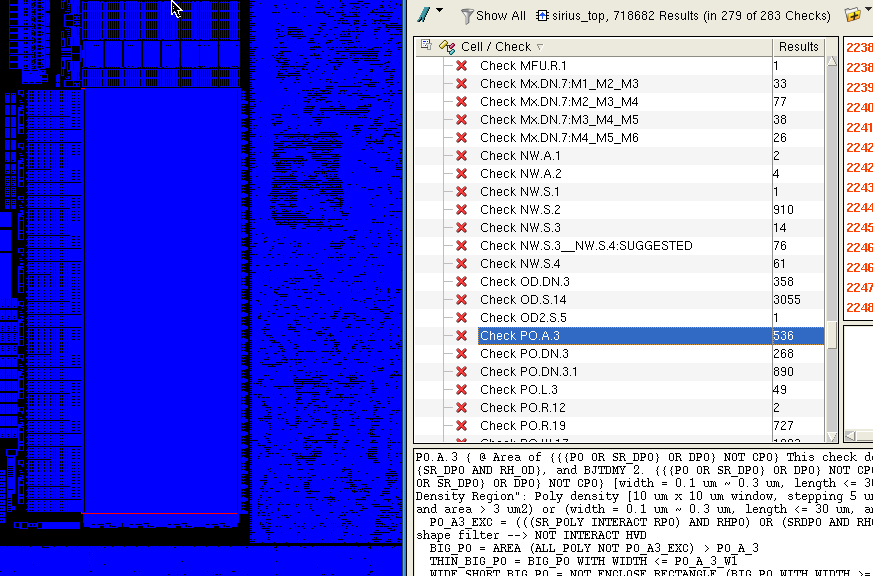
|  |  |  |
| --- | --- | --- |
| **Checks** | **Results** | **Comments** |
| PM.W.4 | 23 | OTP(23) |
| PM.S.2 | 2 | OTP(2) |
| PM.EN.2 | 23 | OTP(23) |
| **Total** | **48** |  |

**OTP:**

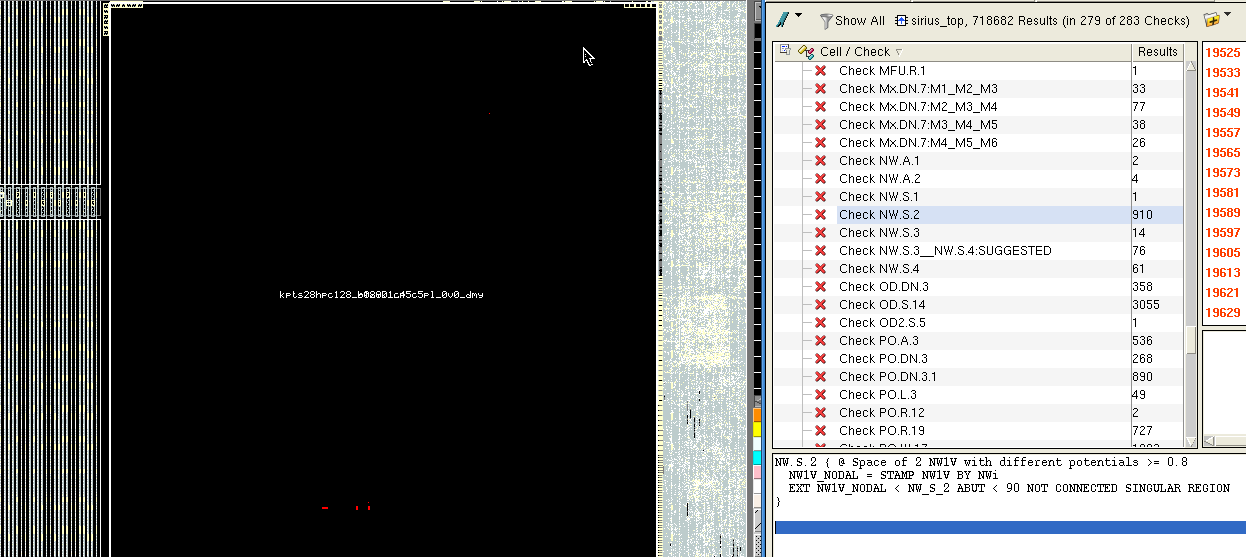
PO.R.12 ……2



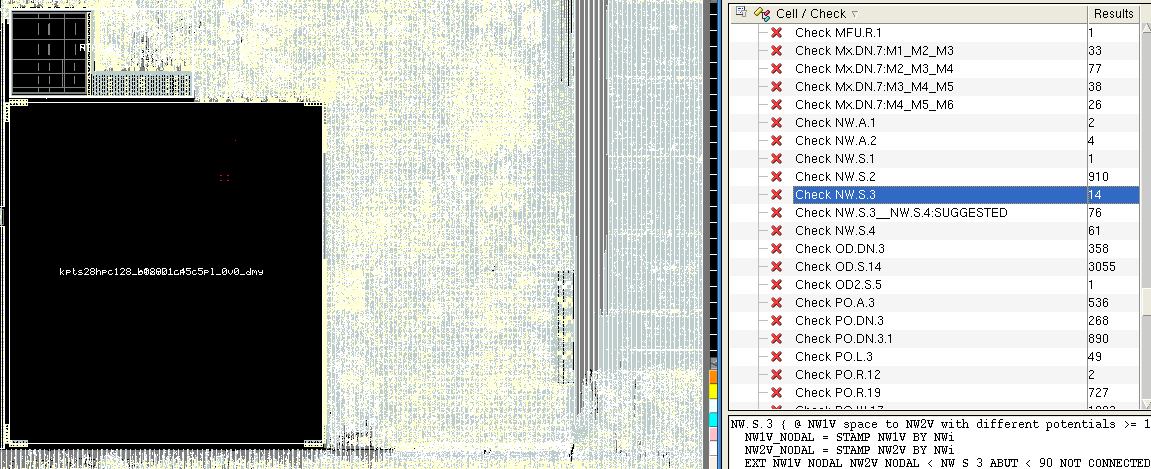
PO.A.3……6



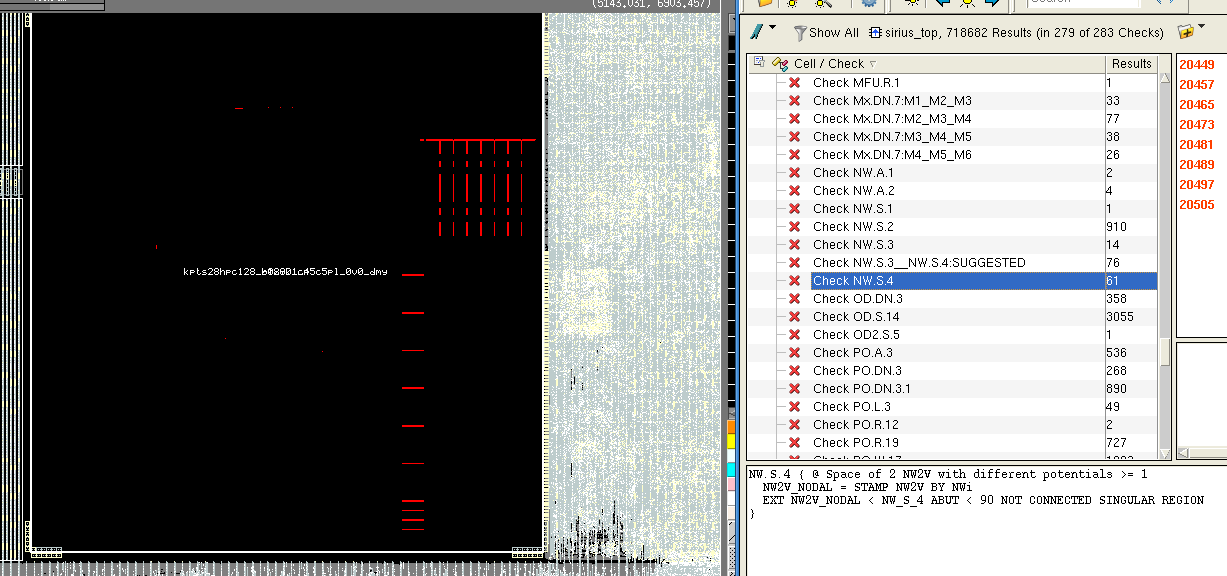
NW.S.2……5



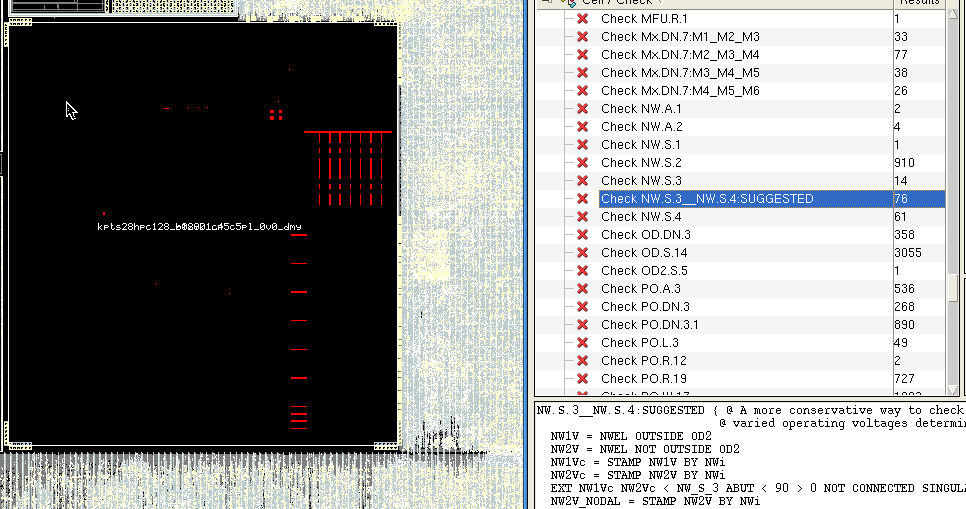
NW.S.3……9



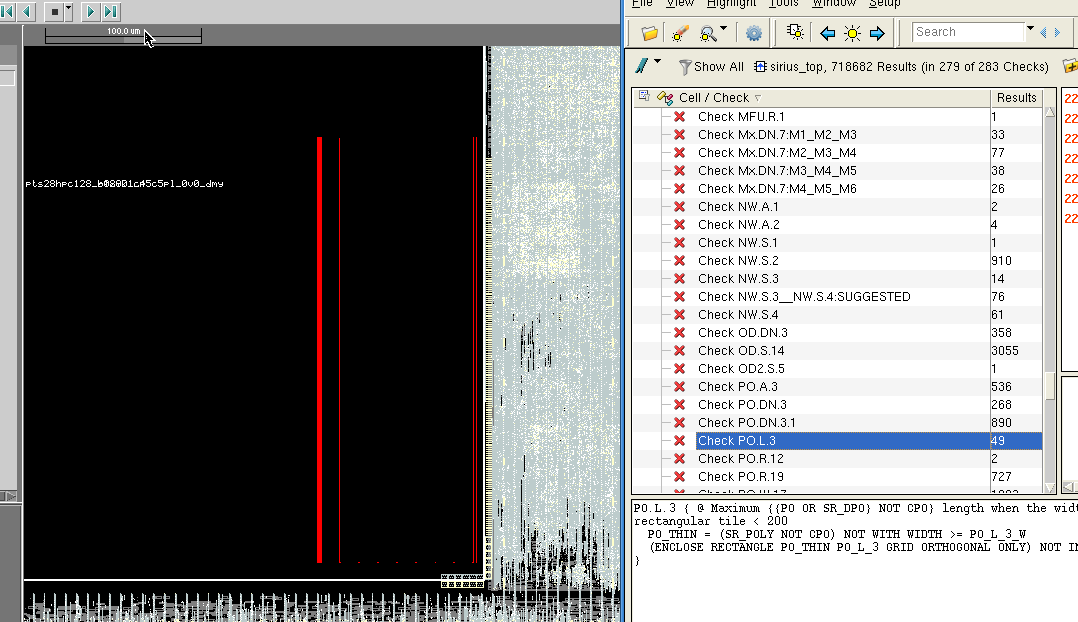
NW.S.4……61



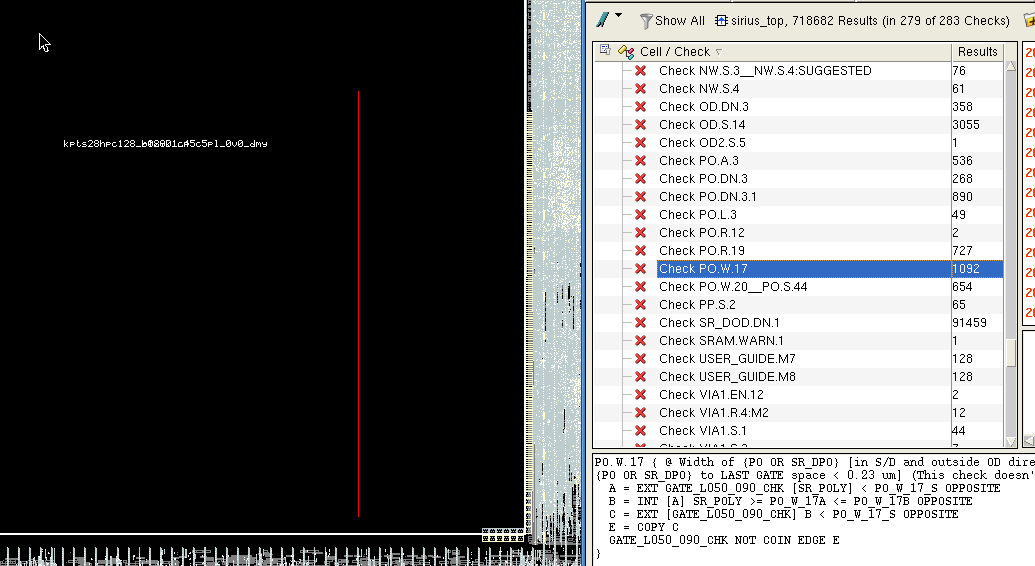
NW.S.3\_\_NW.S.4:SUGGESTED……71



PO.L3……79

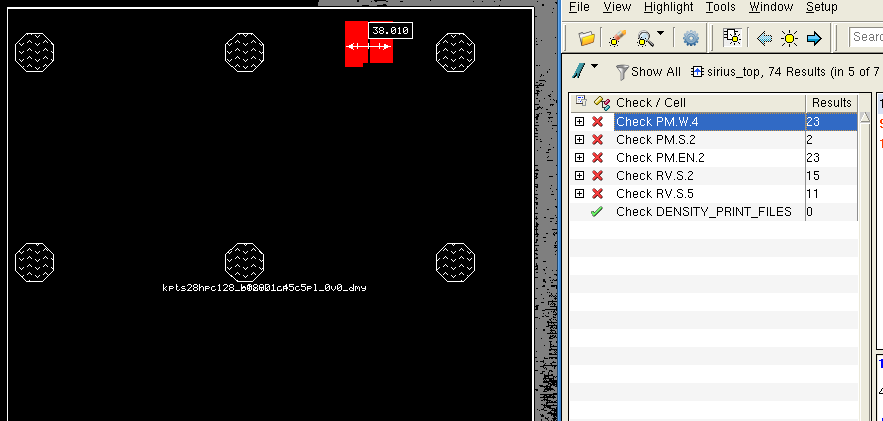


PO.W.17……1092



PM.W.4… 23

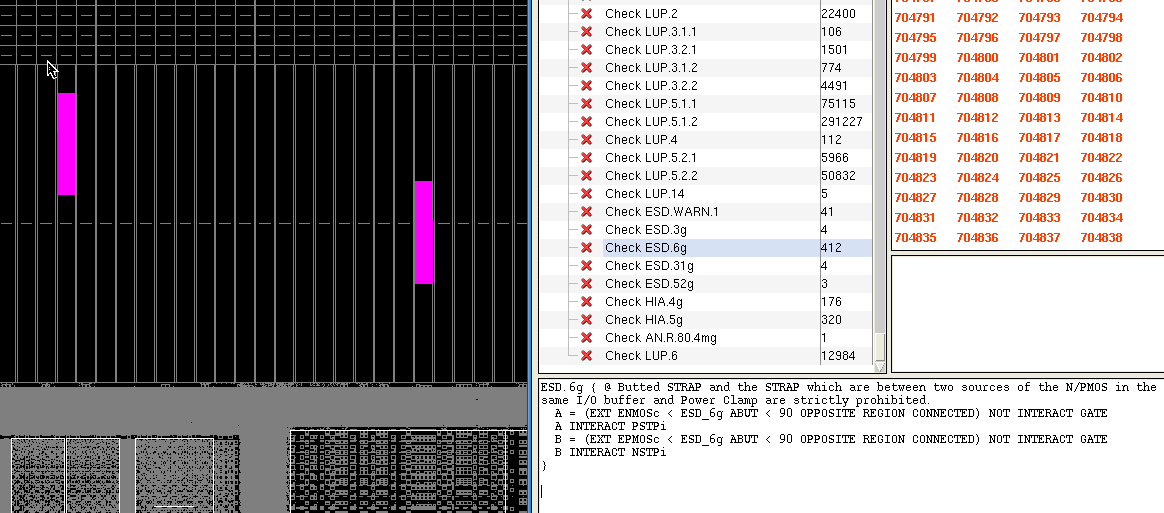
PM.S.2...



**DDR IO:**

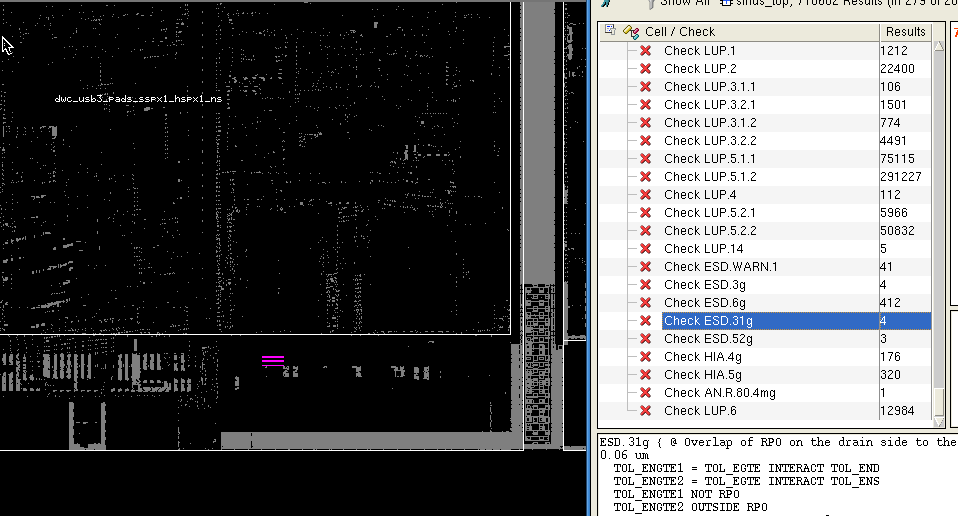
ESD.6g……412



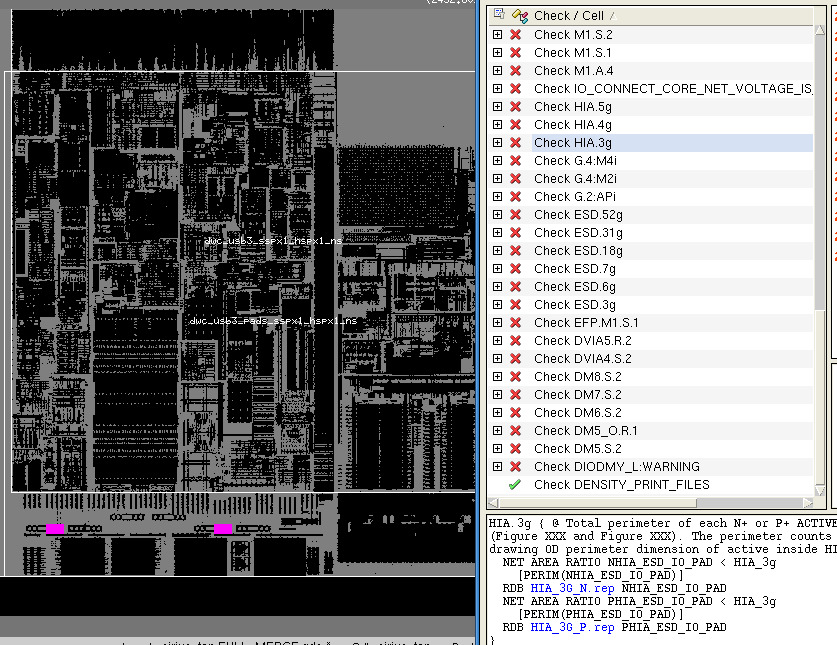
****

**USB IO:**

ESD.31g……4



HIA.3g……14

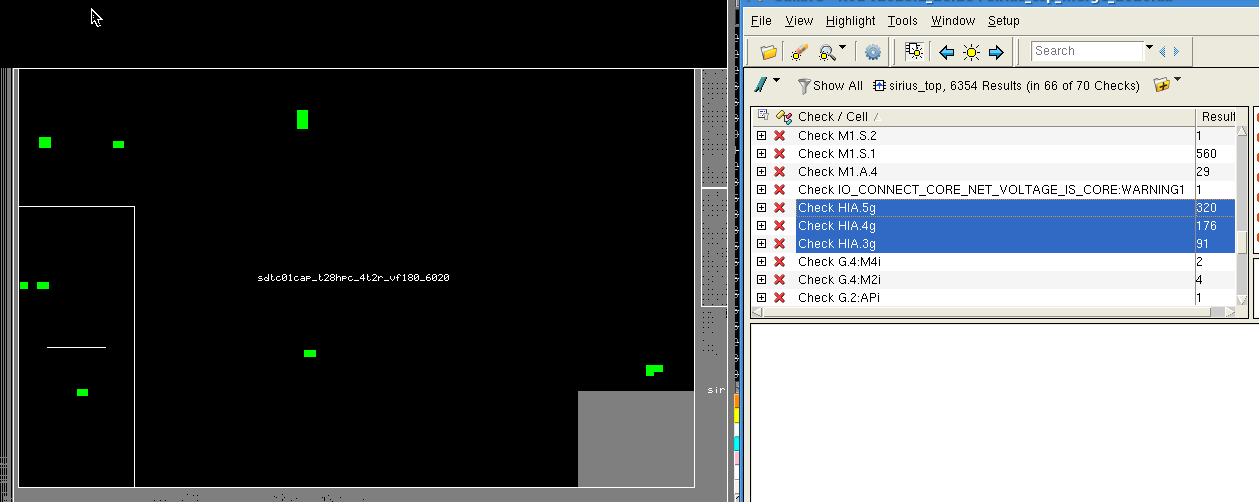


**TYPEC:**

HIA.3g…… 56

HIA.4g……176

HIA.5g……176

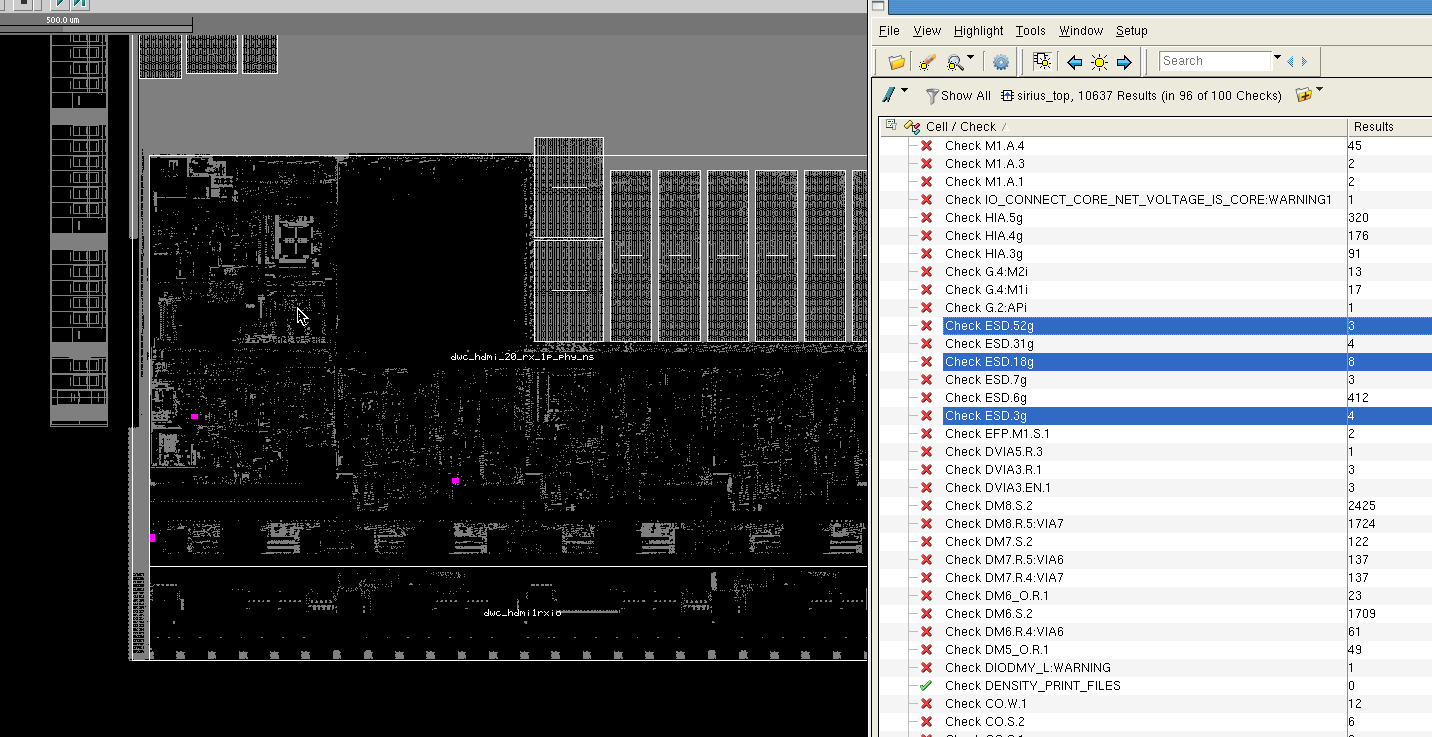


**HDMI PHY:**

ESD.3g…….4

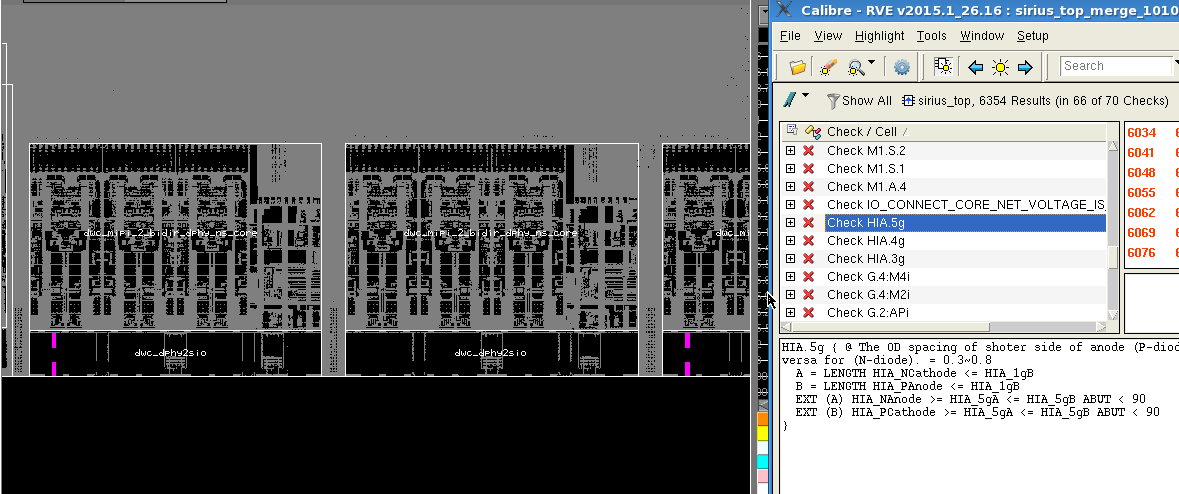
ESD.18g……8

ESD.52g……3



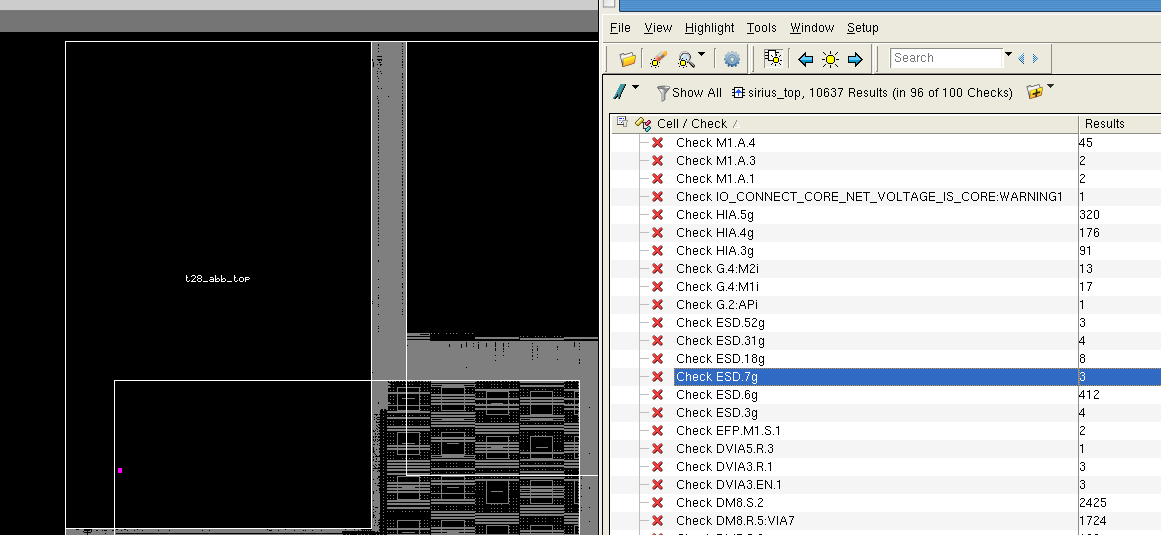
**MIPI IO:**

HIA.5g……34\*2



**t28\_abb\_top:**

ESD.7g……3



**PCIe:**

HIA.3g……21

HIA.5g……76

