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| Project Name | **Sirius** | ECO # | SIR-224 |
| Version No. | **Rev. A** |  |  |
| Requesting Engineer | Song Pan | Request Date | 20170828 |
| Approve Manager | Song Pan | Request Date |  |
| Problem to be fixed | 1. **Bug/Issue description:**   **Add a bypass function for A7 PLL.**   1. **Impact if this ECO is not implemented:**   If PLL doesn’t work at default configuration, there is no clock for a7 and a7 global register, so a7 pll can’t be reconfigured. | | |
| Affected Parts | 1. **Affected IP(s)**   **A7 PLL.**   1. **Affected Partition(s)**   **SUB CA7**   1. **Current status of affected Partitions(s)  (Placement, Pre-CTS, Post-CTS, Post-Route, STA, etc)**   **STA** | | |
| Fix Solution | **Describe briefly how to solve the problem.**  **Add a bypass function for A7 plll and it’s controlled by b6[7] bit.**  **Use a global register to control this bit.** | | |
| Change Description | 1. **Change method (manual ECO fix on netlist or partial Re-synthesis):**   Manual ECO fix **@SUB CA7**   1. **Change effort :** 2. **Connection change or Logic fix:**   Disconnect B6[7] with register and connect it to global register at top throuth a7\_cgu, a7\_harden\_subsystem, a7\_subsystem and Sirius\_sub\_ca7.   1. **How many DFFs or combinational cells will be added or affected in this ECO?**     **0**   1. **Does it have interface change on IP top level? If yes, please describe it in detail**     Add a clk\_bypass pin at a7\_cgu, no other pins change.   1. **Change Schematics:** 2. **Others (for analog macros):** | | |
| IP interface change | **Add a clk\_bypass in at a7\_cgu** | | |
| File to be changed | **A7\_cgu.v, a7\_harden\_subsystem.v, a7\_subsystem.v, Sirius\_sub\_ca7.v** | | |
| Change Impacts | 1. **Impacts on scan chain :**   **NO**   1. **Impacts on timing critical path:**   **NO**   1. **Impacts on IP size and/or floorplan:**   No | | |
| Verification status |  | | |