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| Project Name | **Sirius** | ECO # | SIR-252 |
| Version No. | **Rev. A** |  |  |
| Requesting Engineer | Lei Yang | Request Date | 25-8-2018 |
| Approve Manager | Song Pan | Request Date | 25-8-2018 |
| Problem to be fixed | 1. **Bug/Issue description:**   **CPU access SRAM space halt when in BB enable mode**   1. **Impact if this ECO is not implemented:**   CPU | | |
| Affected Parts | 1. **Affected IP(s)**   **SRAM\_TOP**   1. **Affected Partition(s)**   **SUB4**   1. **Current status of affected Partitions(s)  (Placement, Pre-CTS, Post-CTS, Post-Route, STA, etc)** | | |
| Fix Solution | **Describe briefly how to solve the problem.**   1. **Add Slave Error Response form sram\_top AXI write and read channel** | | |
| Change Description | 1. **Change method (manual ECO fix on netlist or partial Re-synthesis):**   Manual ECO fix **@SUB4**   1. **Change effort :** 2. **Connection change or Logic fix:**   **Change tie 0 of bresp[1] and rresp[1] to the logic like rid and bid**   1. **How many DFFs or combinational cells will be added or affected in this ECO?**     **Add 4 DFFs, other 77 combinational cell was added.**   1. **Does it have interface change on IP top level? If yes, please describe it in detail**     No   1. **Change Schematics:** 2. **Others (for analog macros):** | | |
| IP interface change | **NO** | | |
| File to be changed | **axi\_mux\_mem\_0p5Mb.v**  **axi\_mux\_mem\_0p75Mb.v**  **axi\_mux\_mem\_1p5Mb.v**  **axi\_mux\_mem\_4p5Mb.v** | | |
| Change Impacts | 1. **Impacts on scan chain :**   **NO**   1. **Impacts on timing critical path:**   **NO**   1. **Impacts on IP size and/or floorplan:**   NO | | |
| Verification status | Done | | |