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| Project Name | **Sirius** | ECO # | SIR-253 |
| Version No. | **Rev. A** |  |  |
| Requesting Engineer | Jinfeng.Huang | Request Date | 20170809 |
| Approve Manager | Song Pan | Request Date |  |
| Problem to be fixed | 1. **Bug/Issue description:**   DP fw APB bus sync from dp system clock to APB clock domain.   1. **Impact if this ECO is not implemented:**   If not implement, the DP FW can not access PHY registers correctly. | | |
| Affected Parts | 1. **Affected IP(s)**   TypeC.   1. **Affected Partition(s)**   SUB 3.   1. **Current status of affected Partitions(s)  (Placement, Pre-CTS, Post-CTS, Post-Route, STA, etc)**   **STA** | | |
| Fix Solution | **Describe briefly how to solve the problem.**   1. .reproduce the apb bus select signal according to sync\_apb ready and fifo empty signal; 2. .reproduce both the apb wen and ren signal as one cycle pulse signal, then the apb bus will be sampled once per each access. | | |
| Change Description | 1. **Change method (manual ECO fix on netlist or partial Re-synthesis):**   Manual ECO fix @SUB 3.   1. **Change effort :** 2. **Connection change or Logic fix:** 3. change apb bus select signal from apb\_empty to a reproduced signal eco\_typec\_net\_apb\_data\_sel; 4. reproduce signal apb\_wen and apb\_ren. 5. **How many DFFs or combinational cells will be added or affected in this ECO?**   Add 3 DFFs , 8 combinational cells; other 4 combinational cells were affected.     1. **Does it have interface change on IP top level? If yes, please describe it in detail**     No.   1. **Change Schematics:**   Refer to file SUB\_3\_TypeC\_apb2apb\_sync.vsd.   1. **Others (for analog macros):** | | |
| IP interface change |  | | |
| File to be changed | apb\_sync.v apb\_async\_fifo.v | | |
| Change Impacts | 1. **Impacts on scan chain :**   NO.   1. **Impacts on timing critical path:**   NO.   1. **Impacts on IP size and/or floorplan:**   NO. | | |
| Verification status | Done. | | |