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| Project Name | **Sirius** | ECO # | SIR-221 |
| Version No. | **Rev. A** |  |  |
| Requesting Engineer | Song Pan | Request Date | 8-28-2014 |
| Approve Manager | Song Pan | Request Date |  |
| Problem to be fixed | 1. **Bug/Issue description:**   **Add PLL bypass mode to enhance PLL testability**   1. **Impact if this ECO is not implemented:**   **If there were some bugs in PLL, we can’t debug it.** | | |
| Affected Parts | 1. **Affected IP(s)**   **IO share (test function)**   1. **Affected Partition(s)**   **SUB\_TOP**   1. **Current status of affected Partitions(s)  (Placement, Pre-CTS, Post-CTS, Post-Route, STA, etc)** | | |
| Fix Solution | **Describe briefly how to solve the problem.**   1. **Use the configure pins to generate the PLL bypass mode to bypass PLL** | | |
| Change Description | 1. **Change method (manual ECO fix on netlist or partial Re-synthesis):**   Manual ECO fix **@SUB\_TOP**   1. **Change effort :** 2. **Connection change or Logic fix:**   Add one MUX2   1. **How many DFFs or combinational cells will be added or affected in this ECO?**   No   1. **Does it have interface change on IP top level? If yes, please describe it in detail**   No   1. **Change Schematics:** 2. **Others (for analog macros):** | | |
| IP interface change | **sirius\_test\_func add a port, pll\_bypass\_mode\_o**  **sirius\_sub\_top no interface change** | | |
| File to be changed | **sirius\_cfg\_mode.v**  **sirius\_test\_func.v** | | |
| Change Impacts | 1. **Impacts on scan chain :**   **No**   1. **Impacts on timing critical path:**   **No**   1. **Impacts on IP size and/or floorplan:**   No | | |
| Verification status | Done | | |