**A7 PLL Introduction**

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## Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Version | Author | Comments |
| 04/17/2017 | 0.1 | Zhe.Li | Initial Version |
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# IP Overview

## General IP Description

A7 PLL IP (t28\_pll\_arm\_top) is an integer divider PLL with wide frequency tuning range and 10M per tuning step. This IP also supports dynamic frequency change with no frequency overshoot/undershoot during frequency change.

This IP has its own IO circuit which can only be placed inside chip, as the AAIO (all area IO) is used. Users need to place bump and connect bump to IO with resistance less than 0.05 Ohm.

**Key Feature:**

* 20M~2.55G output frequency range; 10M frequency tuning step;
* Dynamic frequency change, no frequency overshoot/undershoot during frequency change;
* Lower power: 2 mA for 1.8V, 1mA for 0.9V;
* Dimensions 473um by 205um (IO included);

## Floorplan



Fig.1 A7PLL IP floorplan

## Specification

Table.1 A7PLL IP specs

|  |  |  |
| --- | --- | --- |
| Specification | Description | Specs |
| Process | Target process technology: | TSMC 28nm HPC 0.9/1.8V 1P6M2Z |
| Temp Range | Temperature detect range: | 40 ~ 125℃; |
| Fin\_ref | Reference input clock frequency | 20M; |
| Fout | Output clock frequency | 20M~2.55G |
| Fstep | Freq. tuning step | 10M |
| Dutycycle | Output clock dutycycle | 45~55% |
| PJp-p | Peak to peak period jitter, 2000T | 4ps (typical) |
| Iq | Current consumption | AVDD: 2mA; (typical)  DVDD: 1mA; |
| Ipd | Power down current | <5uA; |
| Dimension | Drawn silicon area without pad | 300 \* 190 um2; |
| Dimension(t28\_pll\_arm\_top) | Drawn silicon area with pad | 473 \* 205 um2; |

# Mixed-Signal Interface

Table.2 Power signals

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Pin name | I/O | pad | voltage | default | description | Comments |
| AVDD | AIO | PAD | 1.8 |  | analog 1.8V power | Individual bump |
| AVSS | AIO | PAD | 0 |  | analog ground | Individual bump |
| DVDD | AIO |  | 0.9 |  | digital power from SOC |  |
| DVSS | AIO |  | 0 |  | digital ground from SOC |  |

Table.3 t28\_pll\_arm\_top mixed-signal interface

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Reg name** | **I/O** | **Power** | **default** | **Description** |
| B1<7:0> | I | DVDD | 8’d0 |  |
| B2<7:0> | I | DVDD | 8'b0011,0010 | Frequency Control  8'b0000\_0100: 40MHz (cannot be set less than 40MHz)  8'b0000\_0101: 50MHz  ……  8'b0011\_0010: 500MHz (default)  ……  8'b1111\_1111: 2550MHz |
| B3<7:0> | I | DVDD | 8’d0 |  |
| B4<7:0> | I | DVDD | 8’d0 |  |
| B5<7:0> | I | DVDD | 8’d0 |  |
| B6<7:0> | I | DVDD | 8’d0 |  |
| CLKREF\_OSC09 | I | DVDD |  | Input reference clock (default 40M) |
| CLKOUT09 | O | DVDD |  | PLL output clock |
| LOCK09 | O | DVDD |  | PLL lock signal (0: unlock, 1: lock) |

# Clock and Timing

Reference clock for A7PLL is 20M, in DVDD power domain.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Min | Typ | Max | Unit | notes |
| CLKREF\_OSC09 |  | 20 |  | MHz | Input reference clock |
| Input Tr |  | 20 | 100 | ps | Input clock rise time(20%~80%) |
| Input duty cycle | 30 |  | 70 | % | Input clock duty cycle |
| Cin |  |  | 0.02 | pF | Capacitance on each input |
| Cout |  |  | 0.04 | pF | Load capacitance on each output |
| PLLOUT09 | 20 | 500 | 2550 | MHz | PLL output frequency |

# Physical Implementation

As A7PLL uses AAIO, please place this IP inside chip, and take special care for whole chip DRC LatchUp errors.

Please place one AVDD18 and one AVSS bump near this IP (**DO NOT place bump on A7PLL**), and ensure the routing resistance of RDL is **less than 0.05Ohm**.

Note that there is **NO** **DVDD and DVSS IO clamp cell** inside this IP, therefore please add external ESD protection for DVDD and DVSS.

The following rule must be considered when integrating pll to Soc:

1. Place this IP away from any other block that might generate noise and cause degradation of cell performace.
2. No routing is allowed on top of IP(except RDL).
3. No unrelated routing should exist within 10um of the IP
4. No device with 10um of the IP
5. Routing should be done orthogonally to IP core cell
6. This IP has no DVDD/DVSS clamp cell so please make sure DVDD/DVSS connect to clamp first and then to its input pin. Please ensure DVDD/DVSS bump to any input DVDD/DVSS pin metal bus resistance is lower than 1ohm.
7. Please place one AVDD18 and one AVSS bump near this IP (**DO NOT place bump on A7PLL**), and ensure the routing resistance of RDL is **less than 0.05Ohm**.