**TS IP Introduction**

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## Revision History

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# IP Overview

## General IP Description

The Temperature Sensor (TS) IP is a high accuracy, low power IP with compact silicon footprint suitable for on-die temperature smart monitoring and diverse voltage & frequency control. The TS IP is optimized for an SOC design targeted to the TSMC 28nm HPC 0.9/1.8V fabrication process.

The TS IP supports maximum 4 auxiliary bipolar sensors, which can be scattered around SOC for global junction temperature monitoring.

There are two conversion modes available in TS IP: continuous mode (default) and burst mode. In continuous mode, the TS IP outputs temperature continuously. In burst mode, the TS IP outputs one temperature and then holds until TS\_EN is de-asserted and asserted. **The TS IP may need an additional digital controller to achieve burst mode, configurable data capture interval and perform temperature averaging. ATE and Software calibration is also required to achieve guaranteed accuracy.**

**Key Feature:**

* ±10℃ untrimmed accuracy;
* ±3℃ trimmed accuracy;
* 9 bit resolution;
* Lower power 125uA in continuous mode;
* Dimensions 200um by 200um;

## Application

T28\_TS\_TOP is the main block of TS IP, whereas the T28\_TS\_BJT\_SENSOR is the bipolar sensor which can be arbitrarily placed on SOC and detect local temperature. Note that the connection between T28\_TS\_BJT\_SENSORs and T28\_TS\_TOP are all sensitive signals, which should be double shielded and be kept away from high frequency noisy clocks. (Please refer to Chapter 4 for detail.)



Fig.1 TS IP application

## Specification

Table.1 TS IP specs

|  |  |  |
| --- | --- | --- |
| Specification | Description | Value |
| Process | Target process technology: | TSMC 28nm HPC 0.9/1.8V; |
| Temp Range | Temperature detect range: | 40 ~ 125℃; |
| Accuracy | Absolute accuracy: | ±10℃ before FT calibration; |
| ±3℃ after FT calibration; |
| Output data bits | Output data bits: | 9 bits. |
| Resolution | Temperature resolution: | 0.5℃ per code; |
| Tconv | Conversion time to obtain one temperature: | 28.16us; |
| Fref | TS default input clock frequency: | 390.625K; |
| Iq | Current consumption in continuous conversion mode: | 125uA; |
| Ipd | Power down current: | <1uA; |
| Dimension(T28\_TS\_TOP) | Drawn silicon area without pad for t28\_ts\_top: | 200 \* 200 um2; |
| Dimension (T28\_TS\_BJT\_SENSOR) | Drawn silicon area without pad for t28\_ts\_bjt\_sensor: | 50 \* 50 um2; |
| Auxiliary bipolar sensors supported: | | max 4 BJT sensors. |

## IP Working Principle Introduction

The TS IP is composed of a high accuracy reference generator and a 9-bit internal ADC, as Fig.2 shown. A voltage proportional to temperature is generated by reference generator, and then quantized by the internal ADC. In this way, the temperature is now linear to ADC outputs.



Fig.2 T28\_TS\_TOP architecture

The digital output can be converted to a valid temperature reading by the following equation.

*Temp(℃)=K\*X-B*

Where

* Temp = Temperature in degrees centigrade
* K = 0.488 ℃/lsb
* B = 82.254 ℃
* X is the decimal value of TS\_DOUT09<8:0>
* **Note:**

The parameter K and B are acquired by post layout simulation. Please double confirm with the author for explicit data before ATE calibration.

# Mixed-Signal Interface

Table.2 Power signals

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Pin name | I/O | pad | voltage | default | description | Comments |
| AVDD18 | AIO | PAD | 1.8 |  | analog 1.8V power |  |
| AVSS | AIO | PAD | 0 |  | analog ground |  |
| DVDD | AIO |  | 0.9 |  | digital power from SOC |  |
| DVSS | AIO |  | 0 |  | digital ground from SOC |  |

Table.3 T28\_TS\_TOP mixed-signal interface

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Reg name** | **Name** | **Bit** | **I/O** | **Power** | **Description** | **Default** |
| B0<0> | TS\_EN | [0] | I | DVDD | TS enable; 0 = disable; 1 = normal function; | 1'b0 |
| B1<7:0> | REG\_APROBE\_EN | [7] | I | DVDD | analog test probe enable signal; 0 = disable (floating TS\_APROBE); 1 = enable; | 1'b0 |
| REG\_APROBE\_SEL | [6] | I | DVDD | test probe voltage select; 0 = VDAC; 1 = VBE; | 1'b0 |
| REG\_BJT\_SEL<1:0> | [5:4] | I | DVDD | remote temp sensor location select: 00 = BJT0; 01 = BJT1; 10 = BJT2; 11 = BJT3; | 2'b00 |
| REG\_BJT\_LOCAL\_EN | [3] | I | DVDD | temp sensor local bjt enable signal; 0 = local bjt; 1 = remote bjt; | 1'b0 |
| REG\_DATA\_BPEN | [2] | I | DVDD | testmode bypass data input enable; 0 = disable; (DAC input data from SAR) 1 = enable; | 1'b0 |
| REG\_RSTN\_SEL | [1] | I | DVDD | SAR logic resetb signal select; 0 = auto reset; (continuous conversion) 1 = external reset; (controlled by TS\_RSTN18) | 1'b0 |
| TS\_RSTN | [0] | I | DVDD | TS digital resetb signal; 0 = reset; 1 = normal function; | 1'b0 |
| B2<7:0> | reserved | [7:4] | I | DVDD | Reserved bits | 4'b0000 |
| REG\_CLKPH\_SEL | [3] | I | DVDD | CLK sample phase select: 0: posedge sampling; 1: negedge sampling; | 1'b0 |
| REG\_CLKDIV\_SEL<1:0> | [2:1] | I | DVDD | Internal ADC CLK freq select: 00: 390.625K; 01: 195.3125K; 10: 781.25K; 11: 390.625K; | 2'b00 |
| REG\_BPDATA<0> | [0] | I | DVDD | bit<0> of bypass input 9 bit data to DAC; | 1'b0 |
| B3<7:0> | REG\_BPDATA<8:1> | [7:0] | I | DVDD | bit<8:1> of bypass input 9 bit data to DAC; | 8'b00000000 |
| TS\_CLK50M18 |  |  | I | AVDD18 | System clock input, typical 50M |  |
| TS\_DOUT09 |  |  | O | DVDD | 9 bits data output. |  |
| TS\_DATA\_VALID09 |  |  | O | DVDD | Temperature conversion done signal. |  |
| TS\_APROBE |  |  | AO | AVDD18 | Analog test pin. |  |
| TS\_VBEI\_0 |  |  | AI | AVDD18 | Voltage input from TS\_BJT\_SENSOR0 |  |
| TS\_VBEI\_1 |  |  | AI | AVDD18 | Voltage input from TS\_BJT\_SENSOR1 |  |
| TS\_VBEI\_2 |  |  | AI | AVDD18 | Voltage input from TS\_BJT\_SENSOR2 |  |
| TS\_VBEI\_3 |  |  | AI | AVDD18 | Voltage input from TS\_BJT\_SENSOR3 |  |
| TS\_IBEO\_0 |  |  | AO | AVDD18 | Current output to TS\_BJT\_SENSOR0 |  |
| TS\_IBEO\_1 |  |  | AO | AVDD18 | Current output to TS\_BJT\_SENSOR1 |  |
| TS\_IBEO\_2 |  |  | AO | AVDD18 | Current output to TS\_BJT\_SENSOR2 |  |
| TS\_IBEO\_3 |  |  | AO | AVDD18 | Current output to TS\_BJT\_SENSOR3 |  |
| TS\_RGND |  |  | AIO | AVSS | Connect to TS\_SENSOR\_RNGD in TS\_BJT\_SENSOR |  |

Table.4 T28\_TS\_BJT\_SENSOR interface

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pin name | IO | Power domain | Description | Default |
| TS\_SENSOR\_IBEI | AI | AVDD18 | Current input from TS\_TOP |  |
| TS\_SENSOR\_VBEO | AO | AVDD18 | Voltage output to TS\_TOP |  |
| TS\_SENSOR\_RGND | AIO | AVSS | Connect to TS\_RGND in TS\_TOP |  |

* **Note:**

Signals connect between TS\_TOP and TS\_SENSORs (like \*IBEI\*, \*VBEO\*) are no-buffer-nets, please keep them away from parallel noisy signals.

# Clock and Timing

For continuous mode (default), the timing diagram is shown in Fig. 3.

Where T is the unit cycle of internal ADC clock, T=2.56us (default).

Tconv=11T=28.16us.

Tvalid=3T=7.68us.

There is a 0.5T setup time guaranteed between TS\_DATA\_VALID09 (clk) and TS\_DOUT09<8:0> (data).

The internal ADC frequency (CLK\_INT) can be changed by register **B2<2:1>** (REG\_CLKDIV\_SEL<1:0>) to make the temperature acquisition faster. Please refer to the register description below.

Table. 5 Change internal clock freq. by REG\_CLKDIV\_SEL<1:0>

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Register Number** | **Block** | **Name** | **Effective bits** | **Description** | **Default Value** |
| 2 | TS | REG\_CLKDIV\_SEL<1:0> | [2:1] | Internal ADC CLK freq select: 00: 390.625K; 01: 195.3125K; 10: 781.25K; 11: 390.625K; | 2b'00 |



Fig. 3 Continuous mode timing diagram

**When B1<1:0> (REG\_RSTN\_SEL and TS\_RSTN) is set to 2’b11, the TS IP is working in burst mode**, where TS\_DOUT09<8:0> will hold one temperature data until **TS\_EN is de-asserted (at least one cycle) and asserted again**. The timing diagram for burst mode is shown in Fig. 4.



Fig.4 Burst mode timing diagram

# Physical Implementation

Since the connection between TS\_TOP and TS\_BJT\_SENSOR (TS\_IBEO\* and TS\_VBEI\*) are analog signals, its routing pattern should be carefully designed to keep away from parallel noisy signals.

A routing example is shown below. TS\_IBEO\* and TS\_VBEI\* are 1um wide, both sides shielded by TS\_RGND in M2 or M3, with its top shielded by TS\_RGND in M3 or M4.

Please be aware that it would occupy a total area of 3.6um (width) \* X um (length) for routing in this example.



Fig. 5 Suggested routing pattern for TS\_IBEO\* and TS\_VBEI\*

Since the sheet resistor for M2~M4 are 0.4 Ohm/um\*um, the total routing resistance can be calculated as Rrouting=0.5X Ohm, where X (um) is the routing distance. As the current flow in TS\_IBEO is 10uA, the total IR drop can be figured out as Vrouting = 5u\*X Ohm.

**Therefore, it is recommended that the routing distance between TS\_TOP and TS\_BJT\_SENSOR should not exceed 10000um (which means X < 10000) for IR consideration (IR<50mV).**

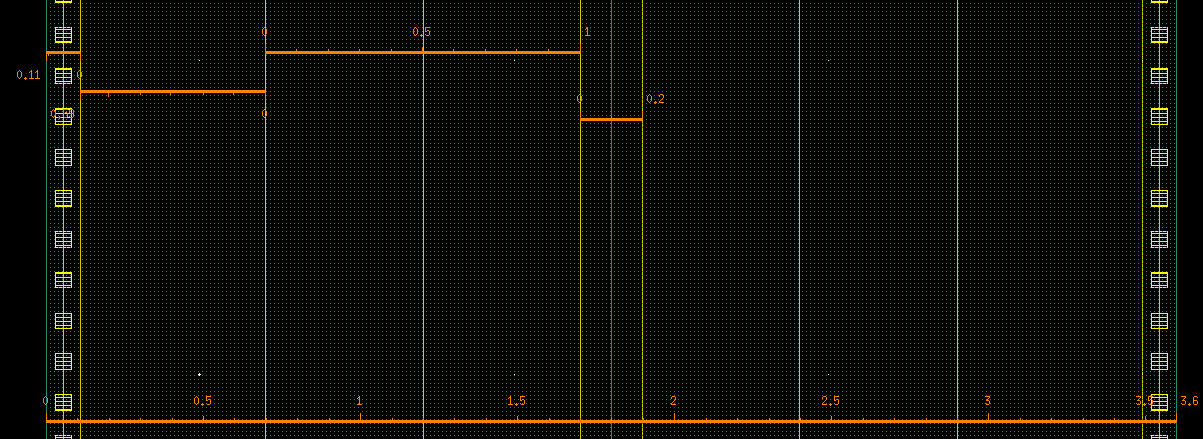


Fig. 6 Layout example of routing pattern for TS\_IBEO\* and TS\_VBEI\*

* **NOTE:**

Since the IR drop between TS\_TOP and TS\_BJT\_SENSOR is a fixed offset in terms of temperature accuracy, **the offset should be calculated or tested during ATE and stored in efuse for software compensation in real use.**

For example, a routing distance of 5000 um indicates 25mV IR drop, which means an temperature offset of about +22℃ **(1℃ is about 1.145mV)** .

The following rule must be considered when integrating t28\_ts\_bjt\_sensor to Soc:

1. Place this IP away from any other block that might generate noise and cause degradation of cell performace.
2. No routing is allowed on top of IP(except RDL).
3. No unrelated routing should exist within 10um of the IP
4. No device with 10um of the IP
5. Routing should be done orthogonally to IP core cell
6. Signal routing rule is as below picture



# Controller Suggestion

As T28\_TS\_TOP and T28\_TS\_BJT\_SENSOR detect silicon die temperature in high accuracy, the output temperature might toggle within ±2℃ from cycle to cycle even in temperature steady state. It is highly recommended to implement a dedicated TS Digital Controller to perform configurable data averaging before output to software platform. (Here, data means TS\_DOUT09<8:0>)

**The TS Controller is advised to have following features**

* Direct control of T28\_TS\_TOP registers;

Eg. TS\_PD/RSTN, continuous mode/burst mode switch;

* Configurable data sampling intervals;

Eg. Sample every 1 (default), 2, 4, 8 … period.

* Configurable data averaging times;

Eg. Average time = 2, 4, 8, 16 …

* Configurable moving averaging function:

Eg. Dout = (3\*Dout+Din)/4; Dout = (7\*Dout+Din)/8 …

* Over Temperature Protection (OTP) and Interrupt:

Eg. If Dout>DOTP, (DOTP is input by user, with default value of 85℃) perform certain interrupt;

* Under Temperature Protection (UTP) and Interrupt:

Eg. If Dout<DUTP, (DUTP is input by user, with default value of -15℃) perform certain interrupt;

* Configurable hysteresis near OTP and UTP to prevent mode change too frequently.

Eg. Set THYSTER to 10℃ means if OTP happened in 85℃, the system should keep cooling down until 75℃.



Fig.7 Over/Under temperature protection diagram

# Production Test and Debug Implementation

Since the existence of process skew and local mismatch, the offset B in temperature conversion equation needs to be calibrated, whereas the variation of slope K is guaranteed by design.

Therefore, the calibration principle can be simplified to find out the precise temperature drift, store it in effuse and then compensate it in software stage.

## 6.1 Load Board Requirement

To perform ATE calibration, **a commercial temperature sensor** is required to place near the test Site to provide reference temperature. For multi-Site load board design, the placement of commercial TS are suggested to avoid cross heating, as Fig.7 shown.

To achieve ±3℃ accuracy after trimming, the commercial temperature sensor itself should ensure ±0.5℃ accuracy. The available high accuracy commercial TS products are **ADT7420/7320** etc., just for reference.



Fig.7 Commercial TS placement suggestion in multi-site load board

## 6.2 Production Test Procedure

* **Pin WR in ATE Testmode**

During ATE test mode, it is recommended to pull out the following signals to PAD and FDMA for direct external control.

Table 6 Pin attribute in testmode

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pin name | I/O | Power domain | PAD in testmode | FDMA in testmode |
| TS\_CLK50M18; | Input | AVDD18 | Y | Y |
| TS\_EN; | Input | DVDD | Y | Y |
| TS\_RSTN\_SEL; | Input | DVDD | Y | Y |
| TS\_RSTN; | Input | DVDD | Y | Y |
| TS\_PD; | Input | DVDD | Y | Y |
| TS\_DATA\_VALID | Output | DVDD | Y | Y |
| TS\_DOUT09<8:0> | Output | DVDD | Y | Y |

If the above pins can only be accessed by SPI, please save the total current on AVDD18 and DVDD (whole chip current during this IP ATE test) in log file for leakage monitor.

* **ATE Environment Requirement**

Please ensure that ATE environment temperature is about 20~33℃.

**Please also ensure TS IP is the first test after IO OS, and keep all other blocks power down** (except CLK source and REG controller). Because ensuring die temperature the same as load board temperature is of vital importance, any additional leakage induced on-die heating will contribute to absolute temperature error beyond this calibration. Here, the reference temperature is the commercial TS on load board, with ±0.5℃ accuracy.

Please keep the commercial TS working during ATE.

**Each data acquisition may need about 250us (8 times averaging as an example).**

**The TS calibration in ATE will need 5 bit efuse to store temperature offset (for TS IP local temperature).**

* **NOTE:**

If several T28\_TS\_BJT\_SENSORs are placed in SOC distant afar from T28\_TS\_TOP, the routing resistor also contributes great offset. It is recommended to use 5 efuse bits each to store every T28\_TS\_BJT\_SENSORs’ offset. If additional efuse bits are not available, the temperature offset of T28\_TS\_BJT\_SENSOR caused by routing resistor can only be compensated in software stage by layout parasitic estimation.

* **ATE Calibration Steps**

Detailed TS ATE calibration procedure and timing diagram is described below.

Table 7 ATE procedures

|  |  |  |
| --- | --- | --- |
| ATE calibration steps | | |
| steps | function | detailed procedure |
| 1 | initial system setting | power down all other blocks except clock source and test mode controller; Power ready for TS:  AVDD18=1.8V; AVSS=0;  DVDD=0.9V, DVSS=0; Commercial TS on load board keep working; |
| 2 | initial IP reg setting | TS\_CLK50M18=50M Hz; all reg default setting except: TS\_RSTN\_SEL=1; TS\_RSTN=1; TS\_PD=0; |
| 3 | data acquisition | wait 20us after TS\_PD=0; set TS\_EN=1; wait 30us or wait until TS\_DATA\_VALID09=1, readout TS\_DOUT09<8:0>; set TS\_EN=0, wait 2.56us and then set TS\_EN=1 to start a new conversion; repeat this procedure 8 times and calculate average TS\_DOUT\_avg |
| 4 | convert raw data to temp | calculate temperature use following equation: T=0.488\* bin2dec(TS\_DOUT\_avg) – 82.254; denoted as T\_ate; |
| 5 | efuse storage | readout average commercial TS temperature (at least 8 times average); denoted as T\_ext; T\_os = T\_ate - T\_ext+16; store T\_os into efuse[4:0].  Please also save the total current on AVDD18 and DVDD (whole chip current during this IP ATE test) in log file for leakage check. |



Fig. 8 ATE timing diagram

## 6.3 Software Calibration Steps

Since the temperature drift is measured during ATE and stored in efuse, it should be compensated in actual use during software stage. Detailed software calibration steps are shown below.

Table 8 Software calibration steps

|  |  |  |
| --- | --- | --- |
| Software steps | | |
| steps | function | detailed procedure |
| 1 | efuse usage | readout efuse[4:0]; T\_os = bin2dec(efuse[4:0])-16 |
| 2 | raw temperature calculate | readout TS\_DOUT<8:0>; convert to temperature use following equation: T\_raw=0.488\* bin2dec(TS\_DOUT) – 82.254; |
| 3 | final temp calculate | T\_final = T\_raw - T\_os |

For T28\_TS\_BJT\_SENSORs placed in SOC, they have additional offsets caused by routing resistance, which should be calculated and included in software real use. For example, if T28\_TS\_BJT\_SENSOR1 has a routing distance of 5000um, its final temperature conversion should be

T\_final = T\_raw-T\_os+5000\*5u/1.145 = T\_raw – T\_os +22℃

Please refer to Chapter 4 for detailed relationship between routing length and its temperature offsets contribution.