**Abb\_top Introduction**

[Revision History 2](#_Toc480273263)

[1. IP Overview 3](#_Toc480273264)

[1.1 General IP Description 3](#_Toc480273265)

[1.2 Floorplan 3](#_Toc480273266)

[1.3 Specification 4](#_Toc480273267)

[2. Mixed-Signal Interface 4](#_Toc480273268)

[3. Clock and Timing 6](#_Toc480273269)

[4. Physical Implementation 6](#_Toc480273270)

## Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Version | Author | Comments |
| 04/18/2017 | 0.1 | Yuan.Yuan | Initial Version |
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# IP Overview

## General IP Description

**Key Feature:**

* Main blocks: 4 channel IQ ADC and 2 channel IQ DAC, temperature sensor, PMU, XTAL driver, ADDAPLL, PVT sensor, DSPPLL0/1/2, PIXPLL, AUDIO PLL, SD card PLL, internal LDO, etc;
* It has its own IO and bump and can not be crossed over by any bump or metal;
* It has no DVDD/DVSS IO or bump so it requires external bump and clamp cells;
* It has three analog power/ground domain: AVDD/AVSS, AVDD\_OSC/AVSS\_OSC, AVDD\_PLL/AVSS\_PLL, and one digital power/ground domain: DVDD/DVSS. Analog power/ground will have its own ball. Digital power/ground is from outside core VDD/VSS and need to connect them all using metal.
* VSS\_ESD is for IO ring ESD ground connection;
* Dimensions 1268 um by 2019 um (IO and bump included);

## Floorplan



Fig.1 abb\_top floorplan

## Specification

Table.1 ABB\_TOP IP specs

|  |  |  |
| --- | --- | --- |
| Specification | Description | Specs |
| Process | Target process technology: | TSMC 28nm HPC 0.9/1.8V 1P8M(5X2Z) |
| Temp Range | Temperature detect range: | -40 ~ 125℃; |
| Dutycycle | Output clock dutycycle | 45~55% |
| AVDD/AVSS | Current consumption | 150mA |
| AVDD\_OSC/AVSS\_OSC | Current consumption | 5mA |
| AVDD\_PLL/AVSS\_PLL | Current consumption | 11mA |
| DVDD/DVSS | Current consumption | 0.2mA |
|  | Power down current | <20uA; |
| Dimension | Drawn silicon area with IO and bump | 473 \* 205 um2; |

# Mixed-Signal Interface

Table.2 analog signals

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pin name | I/O | pad | value | unit | description |
| VSS\_ESD |  |  | 0 | V | ESD ground from IO ring |
| DVDD |  |  | 0.9 | V | digital power from SOC |
| DVSS |  |  | 0 | V | digital ground from SOC |
| POUT\_IB20U |  |  | 20u | A | PMOS output current to DDRPLL,  Need shielded by DDRPLL’s ground |

# Input/Output

Please refer to Reg\_sirius\_abb\_2.0.xls for register table and input/output definition.

Below table is input/output clock/data from digital which has speed or timing requirement.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **in/out** | **pin name** | **Block** | **Effective bits** | **Description** |
| input | CLK\_SYNTH\_PIX | PIXPLL |  | pixpll input reference clock from pixpll\_synth\_dig\_top(50MHz~100MHz) |
| input | CLK\_SYNTH\_SDC | SDCPLL |  | sdcpll input reference clock from sdcpll\_synth\_dig\_top(50MHz~100MHz) |
| input | IDAC\_IN\_A | DAC | [11:0] | IDAC\_A input data |
| input | IDAC\_IN\_B | DAC | [11:0] | IDAC\_B input data |
| input | QDAC\_IN\_A | DAC | [11:0] | QDAC\_A input data |
| input | QDAC\_IN\_B | DAC | [11:0] | QDAC\_B input data |
| input | AUPLL\_CLK\_REQ | AUPLL |  | audio request clock from hdmi\_rx phy(170MHz~370MHz) |
| input | AUPLL\_DSM | AUPLL | [7:0] | audio pll loop divider ratio from aupll\_synth\_dig\_top |
| output | IADC\_DOUT\_A | ADC | [11:0] | ADC\_A I channel data out |
| output | IADC\_DOUT\_B | ADC | [11:0] | ADC\_B I channel data out |
| output | IADC\_DOUT\_C | ADC | [11:0] | ADC\_C I channel data out |
| output | IADC\_DOUT\_D | ADC | [11:0] | ADC\_D I channel data out |
| output | QADC\_DOUT\_A | ADC | [11:0] | ADC\_A Q channel data out |
| output | QADC\_DOUT\_B | ADC | [11:0] | ADC\_B Q channel data out |
| output | QADC\_DOUT\_C | ADC | [11:0] | ADC\_C Q channel data out |
| output | QADC\_DOUT\_D | ADC | [11:0] | ADC\_D Q channel data out |

AC requirement is as below table.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Min | Typ | Max | Unit | notes |
| Data skew |  | 0.2 | 0.5 | ns | Maximum skew among one group of input/output data({IDAC\_IN\_A, IDAC\_IN\_B, QDAC\_IN\_A, QDAC\_IN\_B}, AUPLL\_DSM, {IADC\_DOUT\_A, IADC\_DOUT\_B, IADC\_DOUT\_C, IADC\_DOUT\_D, QADC\_DOUT\_A, QADC\_DOUT\_B, QADC\_DOUT\_C, QADC\_DOUT\_D})  4 DAC as 1 group, 8 ADC as 1 group, AUPLL\_DSM as 1 group |
| Rise/fall time |  | 30 | 100 | ps | Input clock rise/fall time(20%~80%) |
| Input duty cycle | 30 |  | 70 | % | Input clock duty cycle |
| Cin |  |  | 0.02 | pF | Capacitance on each input |
| Cout |  |  | 0.04 | pF | Load capacitance on each output |

# Physical Implementation

This IP should be placed in corner and can be mirrored. Rotation is not allowed.

This IP has no DVDD/DVSS clamp cell so please make sure DVDD/DVSS connect to clamp first and then to its input pin. Please ensure DVDD/DVSS bump to any input DVDD/DVSS pin metal bus resistance is lower than 1ohm.

TS\_IBEO\_0/1/2/3, TS\_RGND, TS\_VBEI\_0/1/2/3 should follow TS\_introduction.docx.

The following rule must be considered when integrating abb\_top to Soc:

1. Place abb\_top away from any other block that might generate noise and cause degradation of cell performace.
2. No routing is allowed on top of IP.
3. No unrelated routing should exist within 10um of the IP
4. No device with 10um of the IP
5. Routing should be done orthogonally to IP core cell
6. I/O RING: VSS\_ESD pin must be connected to global ESD ground
7. This IP has no DVDD/DVSS clamp cell so please make sure DVDD/DVSS connect to clamp first and then to its input pin. Please ensure DVDD/DVSS bump to any input DVDD/DVSS pin metal bus resistance is lower than 1ohm.