Physical floorplan:

Pll\_ddr\_top has its analog power/ground IO circuit, but needs bump outside. All layer can not cross over this IP, except for AP because you will need RDL from bump to IO. The power/ground metal bus resistance from bump to IO connection point must be less than 0.05ohm. This IP has no DVDD/DVSS clamp cell so please make sure DVDD/DVSS connect to clamp first and then to its input pin. Please ensure DVDD/DVSS bump to any input DVDD/DVSS pin metal bus resistance is lower than 1ohm.

This IP could be mirrored but could not be rotated. Recommended minimum distance the PHY can be placed from any adjacent cell is 5um.



IB\_IN\_20U is the current signal path from t28\_abb\_top. It should be pipe shielded by DDRPLL’s AVSS all the way. And the shielding structure is as below picture.



DDRPLL’s internal architecture is as below.



Below table is current

|  |  |  |
| --- | --- | --- |
| Specification | Description | Specs |
| Process | Target process technology: | TSMC 28nm HPC 0.9/1.8V 1P8M(5X2Z) |
| Temp Range | Temperature detect range: | -40 ~ 125℃; |
| Dutycycle | Output clock dutycycle | 45~55% |
| AVDD/AVSS | Current consumption | 150mA |
| AVDD\_OSC/AVSS\_OSC | Current consumption | 5mA |
| AVDD\_PLL/AVSS\_PLL | Current consumption | 11mA |
| DVDD/DVSS | Current consumption | 0.2mA |
|  | Power down current | <20uA; |
| Dimension | Drawn silicon area with IO and bump | 473 \* 205 um2; |

Below table is DDRPLL’s input and output AC spec.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Min | Typ | Max | Unit | notes |
| CLK\_SYNTH\_DDR | 50 |  | 100 | MHz | Input reference clock from ddrpll\_synth\_dig\_top |
| CLK\_50M\_CORE |  | 50 |  | MHz | Input reference clock from abb\_top CLK\_ADCPLL\_50M |
| Input Tr/Tf |  | 20 | 100 | ps | Input clock rise/fall time(20%~80%) |
| Input duty cycle | 30 |  | 70 | % | Input clock duty cycle |
| Cin |  |  | 0.02 | pF | Capacitance on each input |
| Cout |  |  | 0.04 | pF | Load capacitance on each output |
| PLLOUT\_X1 | 1 |  | 667 | MHz | PLLOUT\_X1 output frequency |
| PLLOUT\_X4 | 1 |  | 800 | MHz | PLLOUT\_X4 output frequency |

The following rule must be considered when integrating ddrpll to Soc:

1. Place this IP away from any other block that might generate noise and cause degradation of cell performace.
2. No routing is allowed on top of IP(except RDL).
3. No unrelated routing should exist within 10um of the IP
4. No device with 10um of the IP
5. Routing should be done orthogonally to IP core cell
6. This IP has no DVDD/DVSS clamp cell so please make sure DVDD/DVSS connect to clamp first and then to its input pin. Please ensure DVDD/DVSS bump to any input DVDD/DVSS pin metal bus resistance is lower than 1ohm.
7. Pll\_ddr\_top has its analog power/ground IO circuit, but needs bump outside. All layer can not cross over this IP, except for AP because you will need RDL from bump to IO. The power/ground metal bus resistance from bump to IO connection point must be less than 0.05ohm.