CGU SPEC

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| --- | --- | --- | --- |
| Revision | Date | Description | Author |
| 0.1 | 2016-11-16 | Initial | pchen |
|  |  |  |  |
|  |  |  |  |

# 1 Structure



Figure 1 structure

As Figure 1 shows, it’s the structure of the CGU. The CGU consist of register file, PLL, throttle, Divider 1/4, and PVT\_OSC\_ABS. The CLKREF\_OSC09 is the source of the PLL. RSTN09 is the power on reset. After power on reset, the PLL’s default output is 500MHZ, so the CLKOUT09 is 500MHZ. And the APB CLK is the 1/4 divided version of the CLKOUT09, and the APB CLK is 125MHZ. The throttle realizes fractional frequency from 1/32 to 32/32. The PVT\_OSC\_ABS is a PVT sensor, it’s controlled by register in the register file. Its FCLK is the 1/4 divided version of the CLK\_REF09, and the FCLK is 10MHZ.

# 2 Pin assignments

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pin name | Width | Description | PAD | Direction | A7TOP PIN |
| CLKREF\_OSC09 | 1 | 40Mhz, reference clock for PLL | N | Input | Y |
| RSTN09 | 1 | Power on reset | N | Input | Y |
| TST\_PLL\_CPU | 1 | Test clock for PLL, observed in the top port | Y | Output | Y |
| APB\_CLK | 1 | APB bus and APB slaves’ clock | N | Output | N |
| Cortexa7\_clk | 1 | The clock of the Cortexa7 cores | N | Output | N |
| Pclk | 1 | APB slave clock | N | Input | N |
| Present | 1 | APB slave reset signal | N | Input | N |
| Penable | 1 | APB slave data valid signal | N | Input | N |
| Pwrite | 1 | APB slave read/write signal | N | Input | N |
| Pwdata | 32 | APB slave write data bus | N | Input | N |
| Paddr | 16 | APB slave address | N | Input | N |
| Psel | 1 | APB slave select signal | N | Input | N |
| Pready | 1 | APB slave ready signal | N | Output | N |
| Prdata | 32 | APB slave read data bus | N | Output | N |
| PVT\_ABS\_FOUT | 1 | TEST clock output | Y | Output | Y |

# 3 Register definition

The base address is 0x6061\_0000.

|  |  |  |  |
| --- | --- | --- | --- |
| Addr\_offset | width | Register Name | Default value |
| 0x0 | 32 | CGU\_PLL\_CONFIG | 0x0000\_0000 |
| 0x4 | 32 | CGU\_PLL\_CTRL\_1 | 0x0000\_0000 |
| 0x8 | 32 | CGU\_PLL\_CTRL\_2 | 0X0000\_0001 |
| 0xC | 32 | CGU\_TRT\_CONFIG | 0XFFFF\_FFFF |
| 0x10 | 32 | CGU\_TRT\_CTRL | 0x0000\_0000 |
| 0x14 | 32 | CGU\_PVT\_DATA | 0x0000\_0000 |
| 0x18 | 32 | RESERVED1 | 0x0000\_0000 |
| 0x1C | 32 | RESERVED2 | 0x0000\_0000 |

For more information about the register, please check CGU\_registers.xlsx.

The default value need to be confirmed by Yuan Yuan.