RGU SPEC

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| --- | --- | --- | --- |
| Revision | Date | Description | Author |
| 0.1 | 2016-11-17 | Initial | pchen |
|  |  |  |  |
|  |  |  |  |

# 1 Structure



Figure 1 structure

As Figure 1 shows, it’s the structure of the RGU. The RGU consist of Reg\_file, delay\_module, Reset\_sync, Reset delay, Reset\_sync \_1 and Reset\_sync\_2.

The Reset\_sync is used to synchronize the POR\_RST.

The Delay\_module is used to delay 1ms after POR\_RST release.

When anyone in the register\_file is written zero, it returns to one after one APB\_CLK cycle.

The Reset\_sync\_1 is used to synchronize the reset signal and delay 32 cortexa7\_clk cycles.

The Reset\_sync\_2 is used to synchronize the reset signal and delay 16 cortexa7\_clk cycles.

The Reset\_delay is used to delay 4 APB\_CLK cycles.

# 2 Reset sequence

The reset sequence model is like Figure2 and the reset sequence waveform is like Figure3.



Figure 2 Reset sequence model



Figure 3 Reset sequence waveform

# 3 Pin assignments

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pin name | Width | Description | PAD | Direction | A7TOP PIN |
| CLKREF\_OSC09 | 1 | 40Mhz, reference clock for PLL | N | Input | Y |
| RSTN09 | 1 | Power on reset | N | Input | Y |
| Cortexa7\_clk | 1 | The clock of the Cortexa7 | N | Input | N |
| Pclk | 1 | APB slave clock | N | Input | N |
| Preset | 1 | APB slave reset signal | N | Input | N |
| Penable | 1 | APB slave data valid signal | N | Input | N |
| Pwrite | 1 | APB slave read/write signal | N | Input | N |
| Pwdata | 32 | APB slave write data bus | N | Input | N |
| Paddr | 16 | APB slave address | N | Input | N |
| Psel | 1 | APB slave select signal | N | Input | N |
| Pready | 1 | APB slave ready signal | N | Output | N |
| Prdata | 32 | APB slave read data bus | N | Output | N |
| COREPORRST[3:0] | 4 | Cortexa7 core power on reset | N | Output | N |
| CORERST[3:0] | 4 | Cortexa7 core reset | N | Output | N |
| DBGRST[3:0] | 4 | Debug logic reset | N | Output | N |
| MBISTRST | 1 | MBIST reset signal | N | Output | N |
| PERIRST | 1 | The bridges’ reset signal | N | Output | N |
| L2RST | 1 | L2 cache reset | N | Output | N |
| APBRST | 1 | APB bus and device reset signal | N | Output | N |

# 4 Register definition

The base address is 0x6061\_0020.

|  |  |  |  |
| --- | --- | --- | --- |
| Addr\_offset | width | Register Name | Default value |
| 0x0 | 32 | RESET\_CTRL | 0xFFFF\_FFFF |
| 0x4 | 32 | RESERVED1 | 0x0000\_0000 |
| 0x8 | 32 | RESERVED2 | 0x0000\_0000 |

For more information about the register, please check RGU\_registers.xlsx.