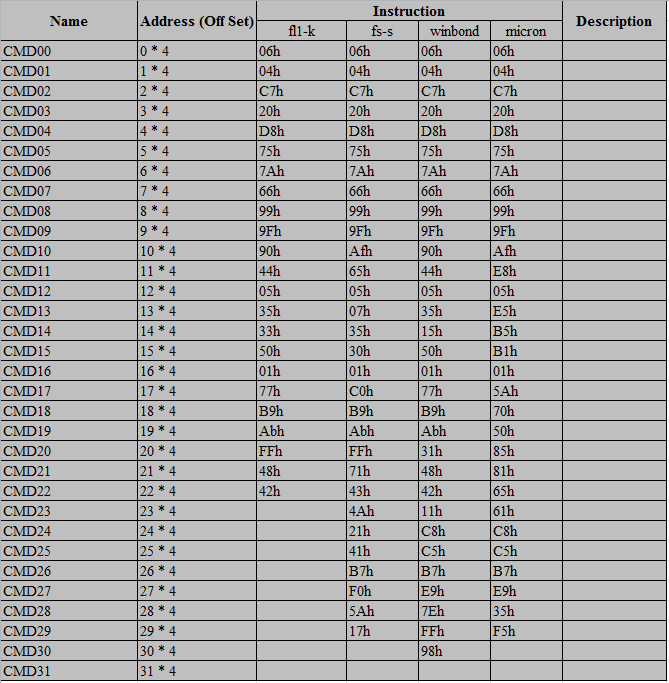
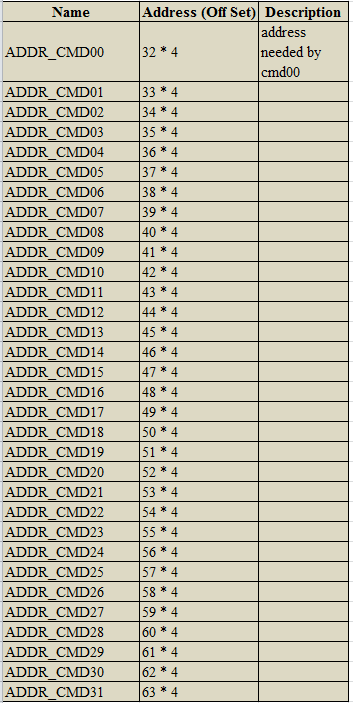
QSPI flash Controller

# Register

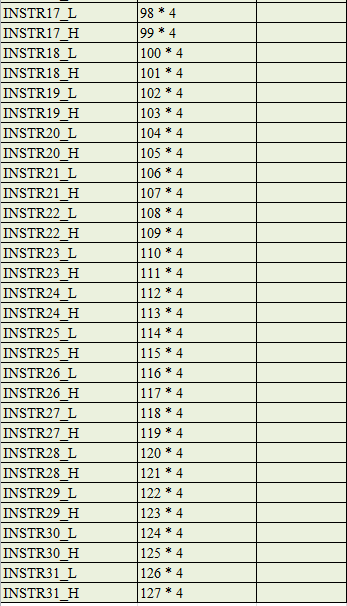
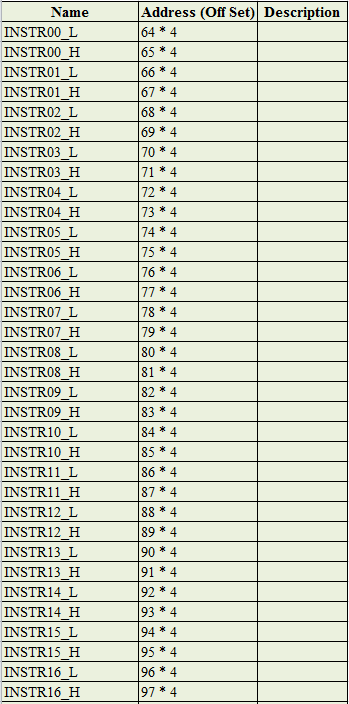
## CMD register



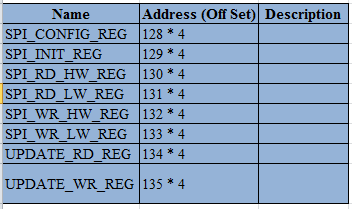
## Address for CMD register



## Code initial register



## Others



SPI\_CONFIG\_REG:

[0] -

[1] – clock polar;

[3:2] – clock speed;

[4] –

[5] – edge sel.

# Instruction

An instruction is defined as follows,

Instruction high word = { bus width, // 2bit, 00-8bit, 01-16bit, 10-32bit, 11-reserved

Mode bit width, //2bit, 00-1bit, 01-2bit, 10-4bit, 11-reserved

Tag, //1bit, 0-APB, 1-AHB

direction, //1bit, 0-read, 1-write

cmd bit width, //2bit, 00-1bit, 01-2bit, 10-4bit, 11-reserved

cmd, //8bit, command

mode cycle} //3bit, the cycle of mode

Instruction low word = { mode, //8bit, mode

Dummy cycle, //5bit,

Data bit width, //2bit, 00-1bit, 01-2bit, 10-4bit, 11-reserved

Data cycle, //9bit

Address bit width,//2bit, 00-1bit, 01-2bit, 10-4bit, 11-reserved

Address cnt sel, //2bit, 00-0, 01-23, 10-31, 11-reserved

Cmd quad mode, //1bit,

Addr quad mode,//1bit,

Mode quad mode,//1bit,

Data quad mode} //1bit

# Software configuration

Step1. Configure the instruction, that is configuring the CODE\_INIT\_REG;

Step2. Flush the instruction through writing 1’b1 to SPI\_INIT\_REG;

Step3. Normal function begins:

Write ADDR\_CMDnn registers to make sure the address needed by CMDnn;

Write CMDnn to active the CMDnn